Application Note

Biasing GaN and LDMOS RF Power Amplifiers in Aerospace Applications Using AFE11612-SEP

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ABSTRACT

This application note details the basic functions and benefits of the AFE11612-SEP in voltage biasing for radio frequency power amplifiers in space-rated applications. This report reviews the fundamentals of power amplifier biasing and supporting circuitry.

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Trademarks

1 LDMOS and GaN Power Amplifier FET PA Basics

Most radio frequency (RF) antenna systems feature power amplifiers (PA) for their RF transmitter design. Many aerospace and space applications include antenna systems, such as:

- Radar
- Radar Imaging Payload
- Communications Payload
- Telemetry

PA biasing circuits are implemented in RF antenna systems to ensure two things. First, that the power output of the amplifier is known and controlled, and second, that the system is powered on and off safely to reduce the risk of damaging the PA. PAs are commonly designed with gallium nitride (GaN), gallium arsenide (GaAs), or laterally diffused MOSFET (LDMOS) transistors. Power output in both GaN and LDMOS FETs (field-effect transistors) is dependent on the current that flows through the device from the drain to the source (I_{DS}).

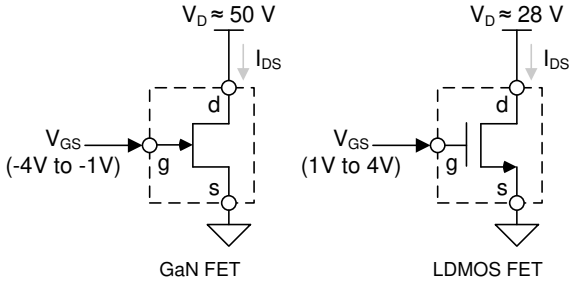


Figure 1-1. GaN and LDMOS FETs

I_{DS} is determined by a few variables: the drain voltage (V_{DRAIN}), the gate voltage (V_{GS}), and temperature. Figure 1-2 shows an example of I_{DS} values against the V_{DRAIN} for a selection of V_{GS} voltages for a GaN PA. The higher V_{GS} voltages result in a higher I_{DS}, or more power from the amplifier. When V_{GS} is sufficiently low, the PA allows virtually zero I_{DS} current. This V_{GS} voltage is called the *pinch-off* voltage. I_{DS} is also dependent on the V_{DRAIN}, but most designers do not vary the V_{DRAIN}. Instead, designers use optimized V_{DRAIN} voltages for the desired power levels. The V_{DRAIN} values are usually about 50 V for GaN PAs and 28 V for LDMOS PAs.

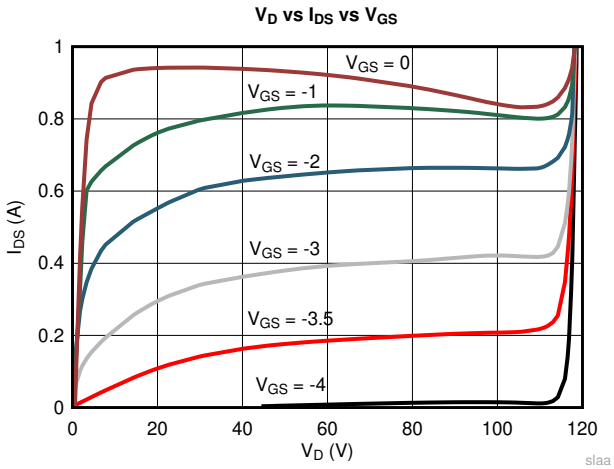


Figure 1-2. FET V_{DRAIN}, I_{DS}, and V_{GS} Behavior

2 V_{GS} Compensation

I_{DS} is dependent on the temperature of the PA. The I_{DS} variations due to thermal drift create the need to compensate the PA by adjusting one of the other two variables in the system: V_{DRAIN} or V_{GS}. Although there are many reasons why adjusting V_{DRAIN} is implemented in different RF applications, the response of the output power is minimal compared to the change in the V_{DRAIN} voltage, as shown in Figure 1-2. Adjusting V_{GS} allows for faster response time and total amplitude of the output power making it more practical for temperature compensation and other applications.

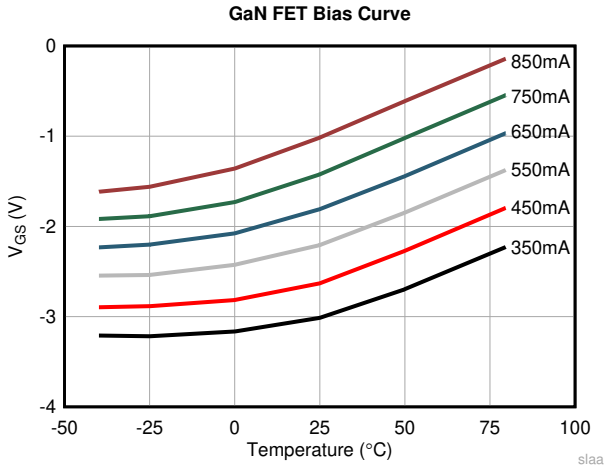


Figure 2-1. GaN PA V_{GS} Bias Voltage vs Temperature to maintain constant I_{DS}

Figure 2-1 shows V_{GS} needs to be adjusted to ensure a static I_{DS} due to thermal drift. Applications utilizing these PAs require implementing this kind of compensation to ensure that the power of the antenna system is tightly controlled. V_{GS} compensation can be implemented by either measuring the temperature of the PA, or measuring the I_{DS} using a current shunt and adjusting the V_{GS} accordingly.

3 Sequencing

Powering the PA on and off in a controlled routine is necessary to prevent the V_{GS} voltage from being too high when the V_{DRAIN} is applied. Such a state causes the PA to operate in saturation mode which may result in thermal damage in the PA or the board it is mounted on. Powering on a PA requires the following steps:

1. First, apply the V_{GS} signal to the PA. The V_{GS} voltage must transition to the V_{GS} pinch-off voltage or lower. This ensures that when the V_{DRAIN} voltage is applied, the gate is already low.
2. Next, enable the drain voltage supply and allow the V_{DRAIN} to be powered to the nominal value (50 V, for example). As the V_{GS} is at the pinch-off voltage, I_{DS} must be minimal.
3. After the V_{DRAIN} is applied, increase the V_{GS} bias voltage to set the desired power output of the PA.
4. Finally, enable the RF signal. This allows the PA to transmit a signal.

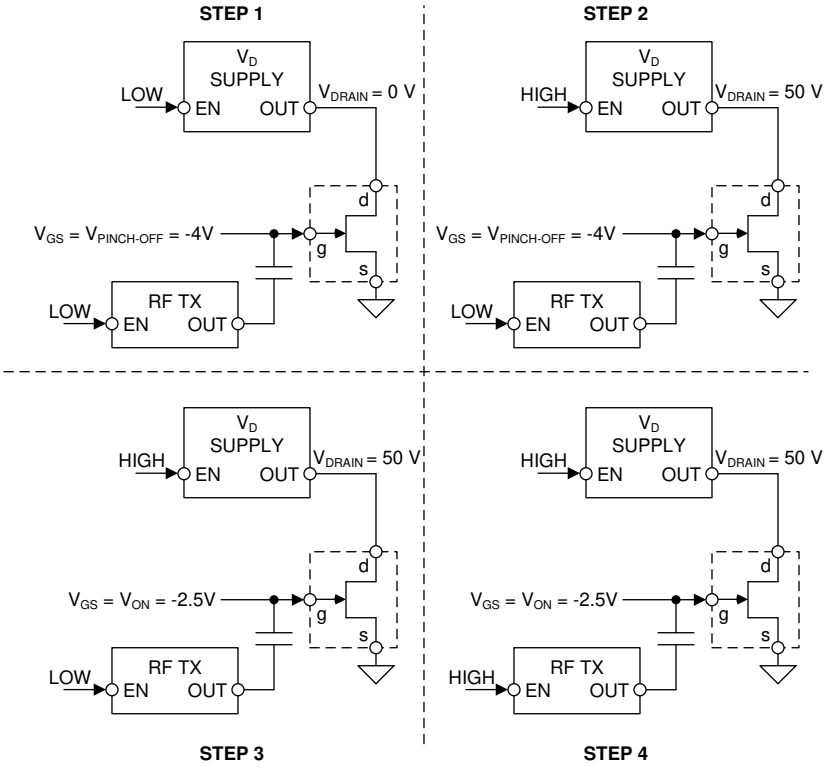


Figure 3-1. GaN Power Sequencing

The PA can be safely shut down by reversing the power-on steps.

1. Disable the RF signal from the PA.
2. Reduce the V_{GS} voltage to the pinch-off value, eliminating the power output of the PA.
3. Disable the V_{DRAIN} voltage by sending a disable signal to the drain supply.
4. Finally, the V_{GS} voltage can be allowed to collapse to ground as the PA is fully disabled.

4 An Integrated PA Biasing Solution

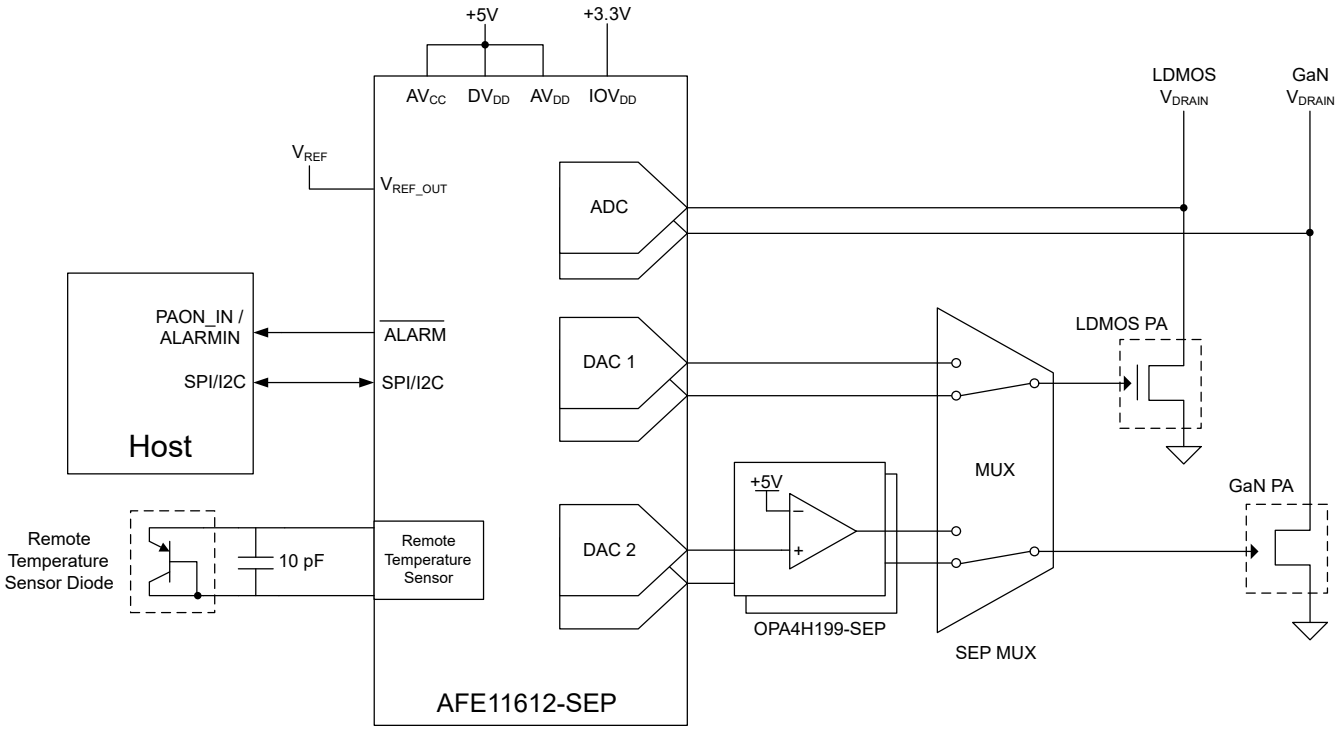


Figure 4-1. AFE11612-SEP Typical Application

The AFE11612-SEP is an integrated power-amplifier biasing solution that features twelve 12-bit precision Digital-to-Analog Converters (DACs), a sixteen-input 12-bit Analog-to-Digital Converter (ADC), and two pairs of remote temperature sensor inputs. The DAC outputs enable V_{GS} control of up to twelve LDMOS PAs. GaN PAs can be supported with additional circuitry. The device also features robust PA monitoring and protection with programmable thresholds for the two remote temperature sensors and four of the ADC inputs.

5 Negative Biasing for GaN PAs

The AFE11612-SEP has an internal 2.5V reference that scales the DAC output range from 0V to 5V. GaN PAs require negative gate voltage to be properly biased, with pinch-off voltages being more negative than the on voltages. The DAC output can be shifted to a negative voltage through the use of a differential op-amp circuit. The circuit example in Figure 5-1 uses the radiation hardened op-amp OPA4H199-SEP to offset and scale the DAC output to the negative range. A differential op-amp circuit is used to protect the PA in case of an alarm shutdown. In an alarm state, the DAC drives the voltage to 0V. The differential circuit outputs the most negative voltage to the GaN gate, thus ensuring the GaN PA turns off.

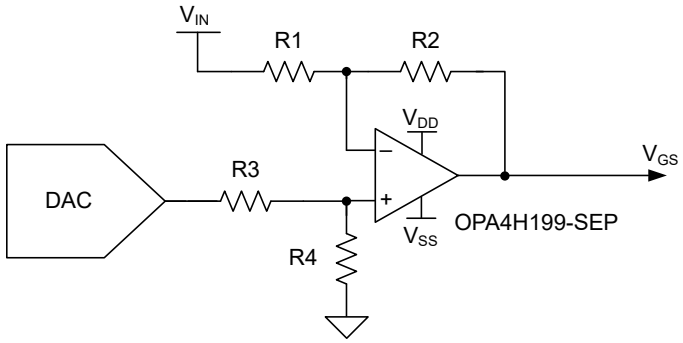


Figure 5-1. Differential Operational Amplifier Circuit

Resistor values are chosen based on the desired op-amp output, V_{IN}, and DAC range. The following equations provide a guideline for selecting the resistor values:

$$V_{GS} = -\left(V_{IN} \times \frac{R2}{R1}\right) + DAC \times \left(\frac{R4}{R4+R3}\right) \times \left(\frac{R1+R2}{R1}\right) \quad (1)$$

When DAC = 0V:

$$V_{GS}(\text{MIN}) = -\left(V_{IN} \times \frac{R2}{R1}\right) \quad (2)$$

V_{GS}(MIN) is selected to be –7.5V, and V_{IN} is selected to be 5V.

$$-7.5V = -\left(5 \times \frac{R2}{R1}\right) \quad (3)$$

$$\frac{R2}{R1} = 1.5 \quad (4)$$

Select R2 and R1 values in accordance with this ratio. In this example, R1 = 10kΩ and R2 = 15kΩ. To calculate R3 and R4, use the maximum desired DAC value and V_{GS} value. In this example, DAC = 5V, and V_{GS}(MAX) = 0V.

$$V_{GS}(\text{MAX}) = -\left(V_{IN} \times \frac{R2}{R1}\right) + DAC \times \left(\frac{R4}{R4+R3}\right)\left(\frac{R1+R2}{R1}\right) \quad (5)$$

$$0 = -\left(5 \times \frac{15k}{10k}\right) + 5 \times \left(\frac{R4}{R4+R3}\right) \times \left(\frac{10k+15k}{10k}\right) \quad (6)$$

$$7.5 = 12.5 \times \left(\frac{R4}{R4+R3}\right) \quad (7)$$

Reducing the equation gives the resistor ratio in Equation 8.

$$\frac{R4}{R3} = 1.5 \quad (8)$$

Since this is the same ratio as R2/R1, the same values will be used for R3 and R4 : R3 = 10kΩ and R4 = 15kΩ. Figure 5-2 shows the DAC vs V_{GS} output with these resistor values.

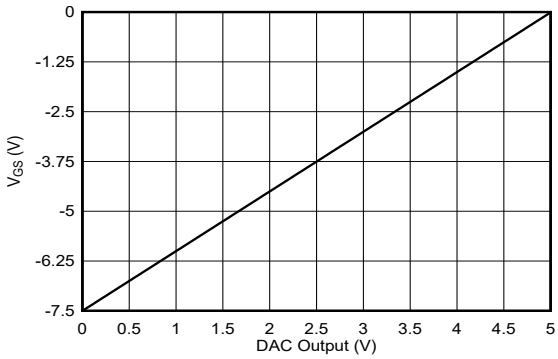


Figure 5-2. Differential Operational Amplifier Output

6 Fast Switching for TDD Applications

Some PA biasing applications such as time division duplexing require fast on-off gate switching. Fast gate switching is achieved by using the a low resistance space-rated MUX and capacitive charge sharing.

Capacitive charge sharing is used to achieve fast output switching. Figure 6-1 shows suggested capacitance of input and output capacitors. The two input voltages have large capacitors, an the output must have a small capacitor. When the MUX switches, the input capacitor quickly charges the smaller output capacitor, giving the required fast switching.

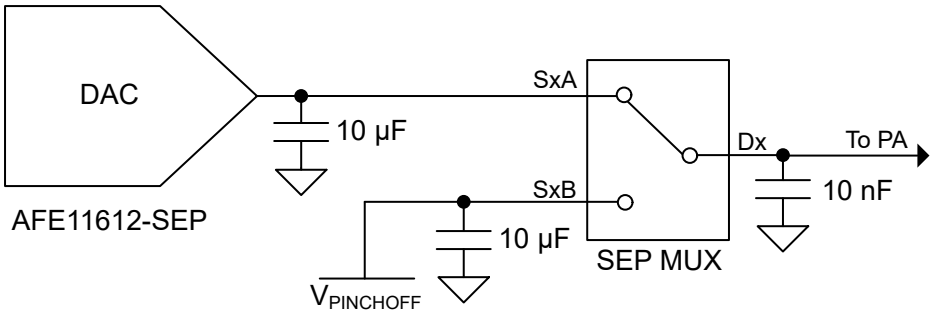


Figure 6-1. Gate Switching Circuit

7 V_{DRAIN} Switching Circuit

The V_{DRAIN} protection circuit uses NMOS and PMOS transistors to disable the voltage being applied to the PA drain. This PA_ON circuit functions as a high-voltage switch. The V_{DRAIN} needs to be disabled at key times during startup, shutdown, and alarm events. This is achieved in this design by an NMOS and PMOS circuit. When the PA_ON voltage is applied to the NMOS gate, the circuit turns on to allow V_{DRAIN} through the PMOS.

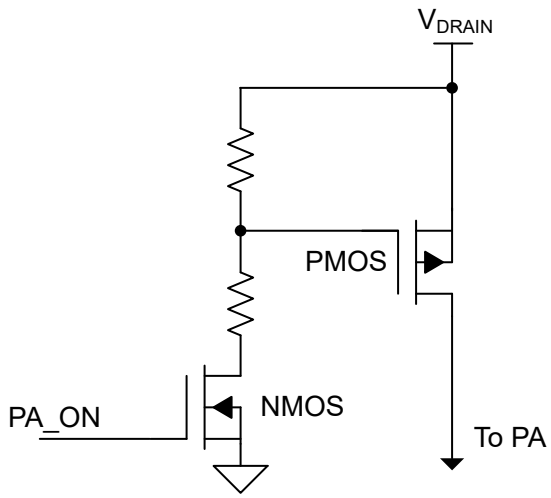


Figure 7-1. V_{DRAIN} Enable Circuit

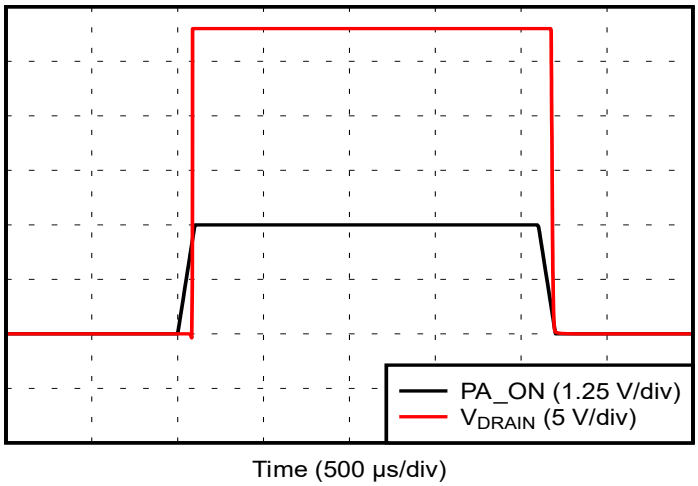


Figure 7-2. V_{DRAIN} Enable Plot

8 Controlled Gate-Sequencing Circuit

There is importance to control the PA during start-up, shutdown, and alarm conditions, to make sure that the PA is not damaged during these events. This is accomplished by creating a three input logic AND gate of key signals: $V_{REF,}$ HOST PA_EN, and $\overline{ALARM}$.

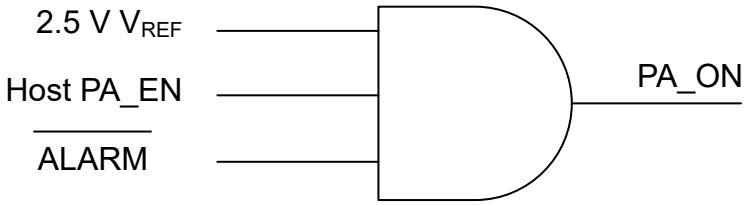


Figure 8-1. PA_ON AND Gate

V_{REF} is used as the *device good* signal for the PA_ON output. This makes sure that the PA never has the drain voltage applied at start-up, as the V_{REF} must be enabled by the host controller after the AFE11612-SEP starts up. The $\overline{ALARM}$ signal from the AFE11612-SEP circuit can force the PA_ON to 0 V if the AFE11612-SEP detects any alarms. Finally, the host micro controller has the option of turning off PA_ON. Table 8-1 shows how all of the digital outputs interact with the PA_ON.

Table 8-1. PA_ON Truth Table

VREF	PA_EN	ALARM	PA_ON
0V	X	X	Low
X	0V	X	Low
X	X	0V	Low
2.5V	High	High	High

Here is an example of the PA_ON power on sequence:

1. The AFE11612-SEP is initialized. The host sends the command to turn on the V_{REF}. With no alarm state at startup, the $\overline{ALARM}$ pin is High-Z. The host keeps PA_EN Low to keep the PA off.
2. Next, the drain power is turned on. The host sets PA_EN High, enabling the PA_ON signal.
3. Third, an alarm condition is shown. The $\overline{ALARM}$ goes to 0V, turning off the PA_ON and thus turning off the PA to protect the PA.
4. Fourth, the alarm condition is cleared. $\overline{ALARM}$ returns to High-Z, and the PA_ON is on.
5. Lastly, before the part powers off, disable PA_EN to turn off the PA_ON. Power down the AFE11612-SEP.

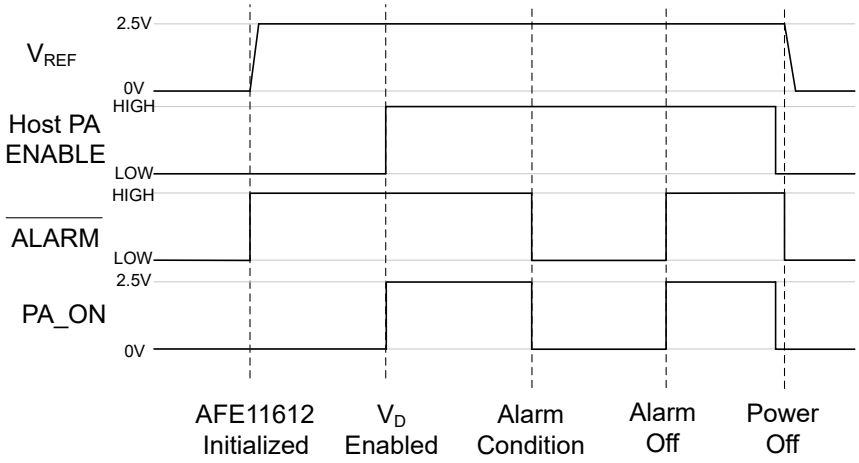


Figure 8-2. PA_ON Power Sequence Control

9 V_{DRAIN} Monitoring

It is important to monitor the V_{DRAIN} voltage to ensure the PA Drain supply is operating at the expected voltage. This can be accomplished using the ADC in the AFE11612-SEP. A resistor divider is required to properly scale the V_{DRAIN} voltage to the 5V ADC range. The impedance of the resistor divider must be limited, ideally under 10kΩ, to allow sufficient current to charge the sampling capacitor. An external capacitor (C_{FILT}) of approximately 1nF is required to quickly charge the ADC sampling capacitor.

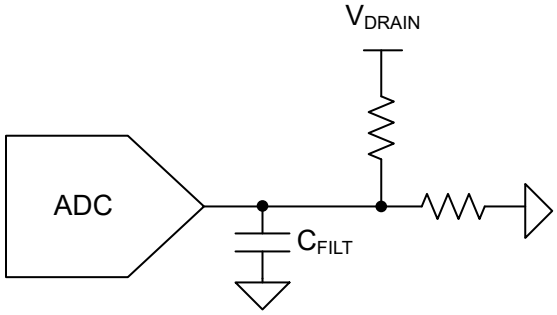


Figure 9-1. V_{DRAIN} Monitor Circuit

10 External Negative Power Supply Monitoring

GaN PAs can be damaged if the V_{GS} potential is too high, resulting in PA saturation. If the V_{SS} supply collapses the differential op-amp output will slew to 0V. Thus, it is critical to monitor the V_{SS} supply for collapse events. Monitoring can be done using a simple resistor divider biased by an external reference voltage, such as the 5V used for the device analog supply. A zener diode can be added for additional protection in case of the external 5V supply collapsing.

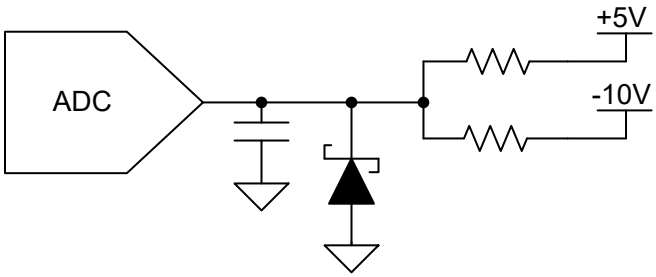
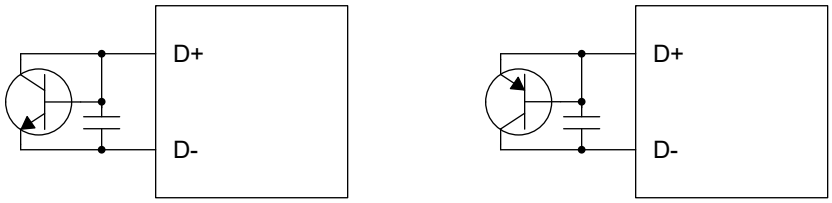


Figure 10-1. V_{SS} Monitor Circuit

11 PA Temperature Monitoring

The AFE11612-SEP has two sets of remote temperature sensor inputs that can be used to monitor the temperature of two diode-connected transistors placed near the PAs. The two temperature sensors have programmable alarm thresholds that can trigger an alarm state and disable the DAC outputs.



(a) NPN (b) PNP

Figure 11-1. Remote Temperature Circuit

12 Summary

Power amplifier behavioral nuances make discrete V_{GS} compensation solutions complex and costly. The AFE11612-SEP simplifies the solution while adding beneficial features, such as gate monitoring, V_{DRAIN} monitoring, temperature monitoring, and supply collapse detection for start-up and shutdown sequence control, to make the device an excellent value.

Table 12-1. Device Recommendations

Device	Optimized Parameters	Total Ionizing Dose (TID) Characterized	Single Event Latch-Up (SEL) Characterized
AFE11612-SEP	Space enhanced 12 12-bit DACs with 16 12-bit ADC inputs.	20 krad(SI)	Immune to 43 MeV-cm^2/mg at 125°C
OPA4H199-SEP	Space enhanced high voltage quad-output operational amplifier.	30 krad(SI)	Immune to 43 MeV-cm2 /mg at 125°C

13 References

- Texas Instruments, *AFE11612-SEP Radiation-Tolerant, Analog Monitor and Controller With Multichannel ADC, DACs, and Temperature Sensors*, data sheet.
- Texas Instruments, *OPA4H199-SEP 40-V, Radiation Hardened, Rail-to-Rail Input/Output, Low Offset Voltage, Low Noise Op Amp in Space Enhanced Plastic*
- Texas Instruments, *Temperature Compensation of Power Amplifier FET Bias Voltages*, application note.

14 Revision History

Changes from Revision * (June 2023) to Revision A (September 2025) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Removed references to unreleased products..... 1

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