Application Note

Comparator Output Types

Paul Grohe

ABSTRACT

This application note discusses the differences between the various output types found with comparators and the associated applications, advantages, and disadvantages.

Table of Contents

1 Introduction....2
2 Output Types....2
2.1 Open Collector or Open Drain....2
2.1.1 Selectable Open Collector or Open Emitter Output....3
2.2 Push-Pull....5
2.2.1 Push-Pull with Separate Supplies....6
2.3 Differential....7
2.3.1 Differential Push Pull....7
2.3.2 ECL, RSECL, PECL, RSPECL, and LVPECL....8
2.3.3 Low Voltage Differential Signaling....9
2.3.4 Current Mode Logic....10
3 Summary....12
4 References....14

Trademarks

1 Introduction

There are several types of outputs for comparators, and the variety can cause some confusion. The following application note explains and clarifies the various differences between the output types and the reasons for these different types.

2 Output Types

2.1 Open Collector or Open Drain

The *Open Collector* or *Open Drain* (used interchangeably) output consists of a single transistor that can only sink current. This can be thought as a mechanical (SPST) switch from the output to ground.

A pull-up resistor is required to create the output *high* voltage. The termination voltage applied to the *top* of the termination resistor sets the output *high* (V_{OH}) voltage. When the output is logic *High*, the transistor is off (not conducting), and the pull-up resistor *pulls* the output node up to the termination voltage.

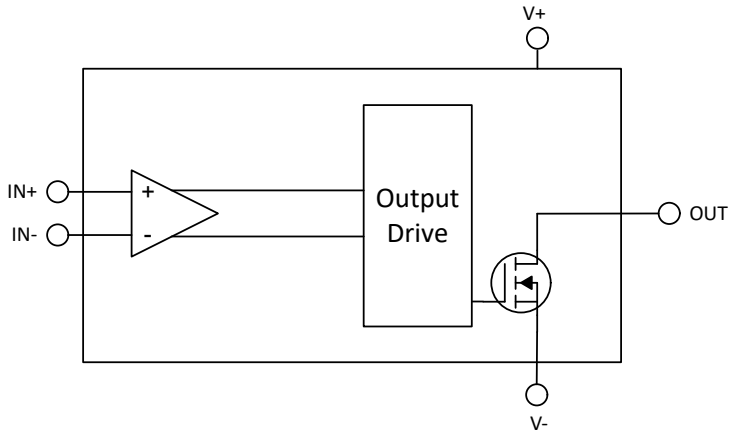


Figure 2-1. Open Drain Output

NOTE: The output can be pulled up to any voltage less than the comparator supply voltage. In most cases, the comparator allows the output to be *pulled* above the comparator supply voltage up to a maximum voltage. However, some devices have an upper ESD clamp diode on the output that limits the maximum pull-up voltage to the supply voltage. Pulling up to a different voltage is known as *Level-Shifting*.

The data sheet Features or Electrical Specification table notes can mention if the output can be pulled above the supply. If not, then the *Output Voltage* line of the Absolute Maximum Ratings or Recommended Operating Conditions can give a clue.

- If the output voltage rating is an absolute number, such as 5V or 36V, then this is a good sign that the output can be pulled above the comparator supply.
- If the rating references the supply, such as VCC + 0.3 or (V+) + 0.3V, then the maximum output pull-up voltage is limited to the comparator supply voltage.

An advantage of the open collector output is that multiple outputs can be tied together to form a *OR'ed* output bus, where any output can pull the output bus low. This is common for system error buses and window comparators.

A list of Open Collector output devices is shown in Table 3-1.

Table 2-1. Advantages and Disadvantages of Open Drain or Open Collector Outputs

Advantages	Disadvantages
• Allows different Output High (V_{OH}) voltage (Level shifting) • Allows OR'ing of multiple outputs • Allows charging or discharging capacitors in timing applications • Pullup voltage can be higher than supply voltage (in most cases)	• Cannot source (output) current • Requires external Pull-Up resistor • Rise time dependent on capacitive loading • Asymmetrical output rise and fall times at high speeds • Dissipates current when output is low

2.1.1 Selectable Open Collector or Open Emitter Output

A unique output is seen in the LM111/211/311 and LM119/219/319 families. The output transistor exposes both the emitter and the collector creating a *floating* output.

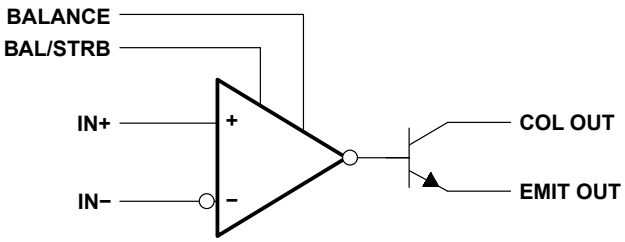


Figure 2-2. LM311 Block Diagram

A problem arises when the comparator inputs require a split power supply to accept bipolar input signals. For most open collector output comparators, this results in an output Low swing that is equal to the negative power supply pin (V- or V_{EE}). If the comparator is using a split supply, such as +12V and -12V, the output LOW is -12V and NOT ground (0V). Allowing for a negative supply allows the comparator to directly accept bipolar input signals without level shifting, attenuation or clamping, thus improving accuracy. Level shifting is possible at the output by using a resistor- divider string to achieve an above ground swing, but this is not the best way.

The exposed output transistor pins allows the floating output to be either Common Collector (load to pull-up voltage, or sinking current), or common emitter (with the load to ground, or sourcing current), as shown in the following images. This allows the user to determine the output High and Low voltage levels independent of the V_{CC} and V_{EE} voltages.

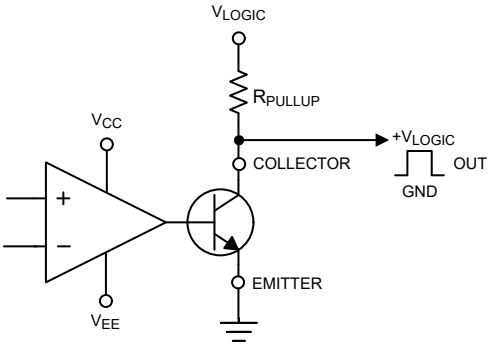


Figure 2-3. Open Collector Configuration

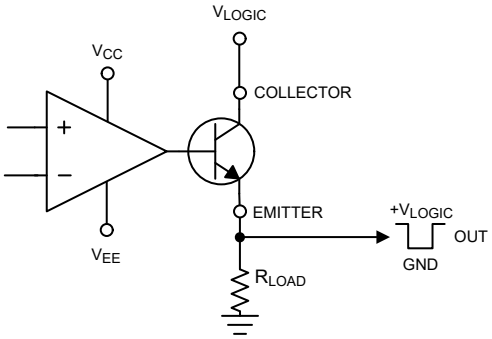


Figure 2-4. Open Emitter Configuration

As shown in Section 2.1, if a Common Collector logic output is required (the most common use), the Emitter pin is tied to system ground, and the pull-up resistor is connected between the Collector pin and a positive logic supply. The logic output is taken from the Collector pin, as shown in Figure 2-3. This is the same configuration as the Open Collector output, except that the output now swings Low to system ground (0V).

A usage example is where the input section power supplies (V+ and V-) are a split supply of +12V and -12V to accept bipolar input signals, but the output has to drive 3.3V digital logic. This configuration is shown in Figure 2-5 .

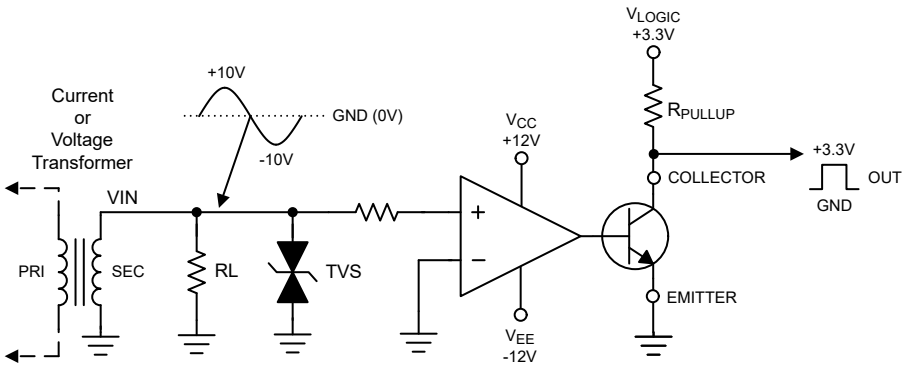


Figure 2-5. Bipolar Input Using Open Collector Output Example

The output Emitter is tied to GND, and the pull-up resistor is placed between the Collector pin and the pull-up voltage. The Collector pin becomes the output. If the pull-up voltage is +3.3V, this creates a 0 to 3.3V ground referenced output swing directly compatible with 3.3V digital logic. No level shifting required!

If a high side sourcing or a grounded load is required, the *Common Emitter* configuration can be used, as shown in Figure 2-6. For a Common Emitter output, the Collector pin is tied to the positive source voltage, and the load is connected between the Emitter pin and negative voltage (usually ground). This is useful when the load must be returned to ground, as shown in Figure 2-6.

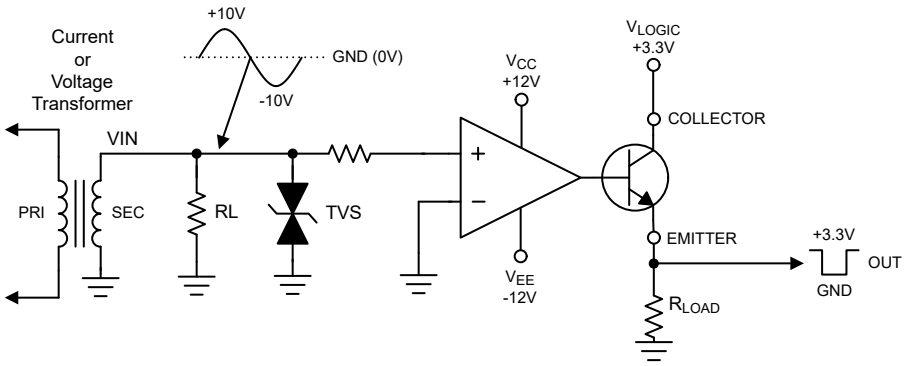


Figure 2-6. Bipolar Input With Open Emitter Output Example

Logic output is now taken from the Emitter pin. Note there is an *inversion* in the logic when using common emitter output. The inputs can be simply reversed to correct the logic. Observe limits on the output stage voltages in the Absolute Maximum table.

Examples of the OC/OE output is the LM111, LM211, LM311, LM119, LM219, LM319 and LM6511.

Table 2-2. Advantages and Disadvantages of Open Emitter or Open Collector Outputs

Advantages	Disadvantages
• Allows level shifting • Allows OR'ing of multiple outputs • Allows charging or discharging capacitors in timing applications • Selectable high (Sourcing) or low side (sinking) drive • Pull-up voltage can exceed positive supply voltage.	• Requires external resistor • Rise or Fall time dependent on capacitive loading • Asymmetrical output rise and fall times at high speeds • Dissipates current in one state

2.2 Push-Pull

A Push-Pull (also called Totem-Pole) output consists of both a positive and negative output devices, such that the output can both sink and source current. Since the output can source current, a pull-up resistor is no longer required. Most commonly, the High and Low output voltages are equal to the comparator V+ and V- power supplies.

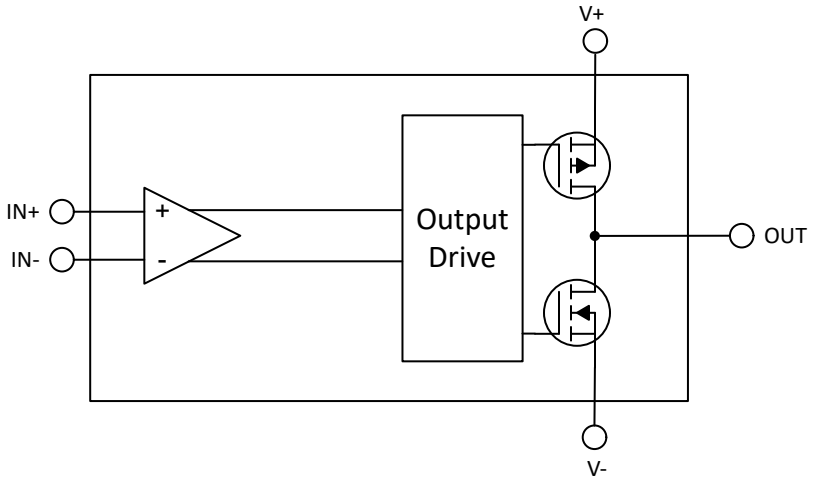


Figure 2-7. Push Pull Output Stage

High speed devices (<100ns) primarily use Push Pull outputs because symmetrical rise and fall times are required for the fast edges. The rise time is no longer reliant on the pull-up resistor and load capacitance as the push-pull output can now charge and discharge the load capacitance directly, resulting in faster, straighter pulse edges.

Push-Pull outputs are also used for micro and nanopower devices and designs to eliminate wasting power in the pull-up resistor.

A list of Push-Pull output devices is shown in Table 3-1.

Table 2-3. Advantages and Disadvantages of Push-Pull Outputs

Advantages	Disadvantages
• Output can sink and source current • No Pull-up resistor required - saves power • Symmetrical rise and fall times • No extra current when output high or low.	• Outputs cannot be tied together • Output votlage swing is the same as the supply voltage

2.2.1 Push-Pull with Separate Supplies

The Push-Pull with separate output supplies has the advantage of the floating OC/OE output while providing the advantages of a push-pull output with a defined output swing.

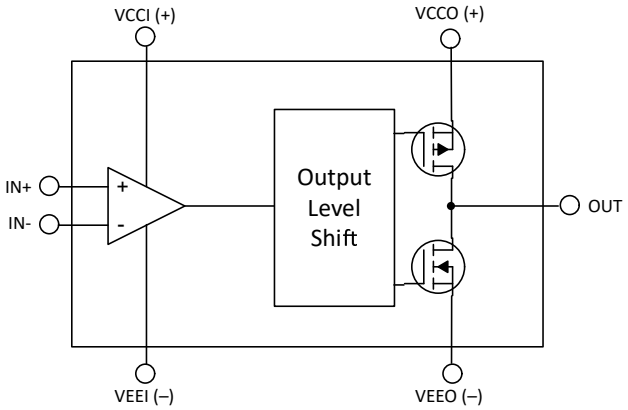
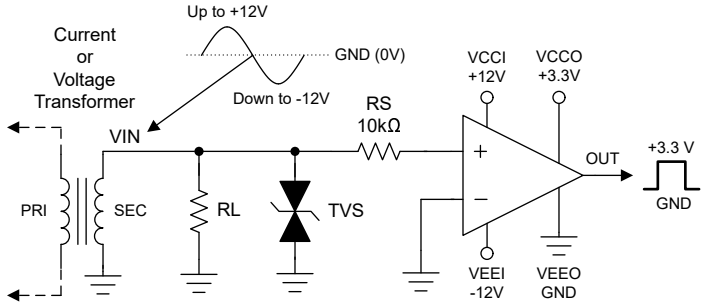


Figure 2-8. Push-Pull with Separate Supplies

A problem arises when the comparator inputs require a wide supply voltage or a split power supply to accept large or bipolar signals. For most push-pull output comparators, this results in an output swing that is equal to the power supplies (such as 0 and 12V or ±5V) and is not compatible with digital logic. This requires external level shifting or clamping to feed digital logic.

This problem is solved with a push-pull output with seporate input and output power supplies, such as the TLV1871/2 shown above. This allows the output swing to be directly set by the output power supply pins (VCCO and VEEO), and the input voltage range set by the input power supplies (VCCI and VEEI).

An example is where the input supplies (VCCI and VEEI) can be a split supply of +12V and -12V to accept bipolar input signals. The output supplies (VCCO and VEEO) can be set to +3.3V and ground, creating a 0 to 3.3V ground referenced output swing compatible with 3.3V digital logic. No level shifting required!



Another advantage is that the input range is not set by the required output swing, which requires attenuation of the input signal. Instead, input supply pins can be powered from a larger supply voltage to accept a direct, or a lesser attenuated input signal, improving accuracy.

The TLV1871/2 (Push-Pull) and TLV3801/2 (LVDS) have separate output power supplies.

Table 2-4. Advantages and Disadvantages of Push-Pull with Separate Supplies Outputs

Advantages	Disadvantages
• Output swing set by output supply pins • Separate input power supplies allow wider input range or split supplies. • Output can sink and source current • No Pull-up resistor required - saves power • Symmetrical rise and fall times	• Outputs cannot be tied together

2.3 Differential

Differential outputs use two outputs that are always 180° out of phase. The differential scheme has a tremendous advantage over single-ended schemes as differential is less susceptible to common mode noise. The receivers respond only to differential voltages. Noise coupled onto the interconnect is seen as common mode modulations by the receivers and is rejected. Conversely, the balanced current paths can reduce radiated EMI by using balanced lines or twisted pairs.

2.3.1 Differential Push Pull

The differential push-pull out is a comparator with two identical Push-Pull outputs, where one output is inverted 180° from the other and swing close to the supply rails. Because the inversion is done internally from a common node, there is minimal skewing (delay) between the two outputs that can be caused by using an external inverter logic gate.

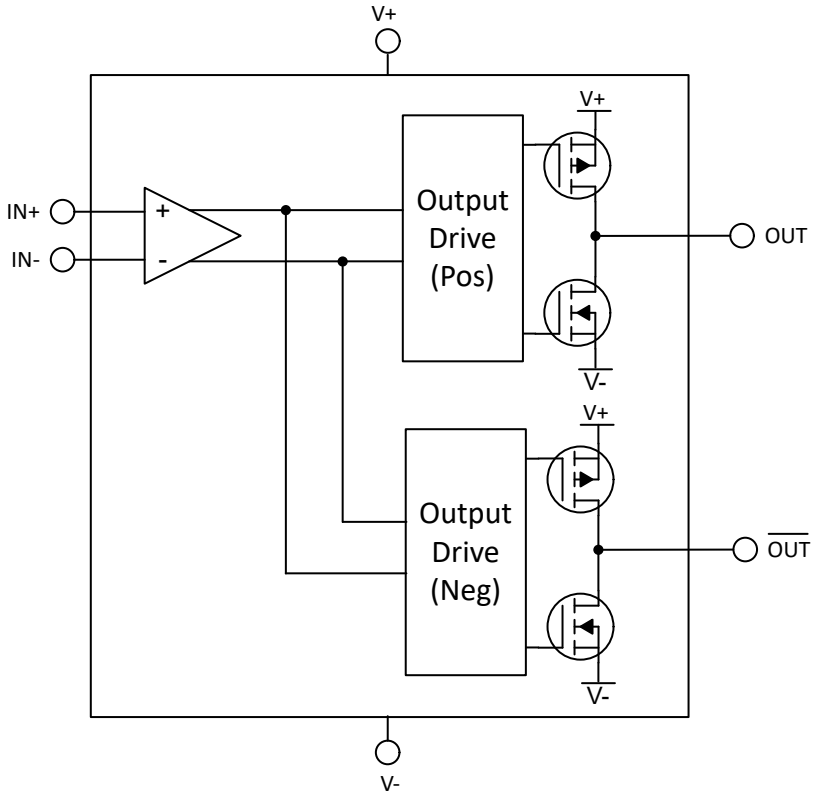


Figure 2-9. Differential Push-Pull Output

The differential outputs can be used to create a differential transmission scheme, or, as two single outputs 180° apart to drive loads such as H bridge transistors or MOSFETs.

Devices that support this standard are the TL3016, TL3116, TL712 and TL714.

Table 2-5. Advantages and Disadvantages of Differential Push-Pull Outputs

Advantages	Disadvantages
• Outputs can sink and source current • No Pull-up resistor required - saves power • Symmetrical rise and fall times • Allows for differential signaling	• Outputs cannot be tied together • Output voltage swing is the same as the supply voltage • Large output swing can cause EMI

2.3.2 ECL, RSECL, PECL, RSPECL, and LVPECL

As speeds get into the nanoseconds, creating single-ended sub-nanosecond edge rates becomes problematic when using large output swings (such as 3V or 5V).

i = c × ΔV/ΔT starts to create peak currents into the ampere range as the edge rates (rise and fall times) get into the nanosecond range. These edges increase power consumption and can produce EMI and noise.

The time spent in rising or falling times between logic thresholds limits the maximum output transition time (speed).

To overcome these issues, the output swings were reduced to 800mV. The smaller output swing is easier for the output devices to generate, saves power, and also reduces radiated noise and increases the maximum speed.

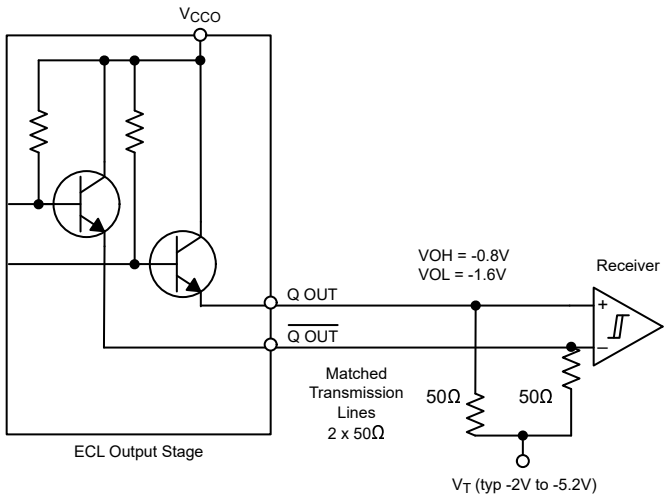


Figure 2-10. ECL Output

Emitter Coupled Logic, or *ECL*, was developed in the early 1960's, and is the oldest of the high speed logic family. The drivers are low impedance emitter follower outputs that generate a typical 800mV output differential voltage. The output transistors are operated in the linear region and not saturated to provide the fastest response. The outputs are typically terminated with 50Ω to a termination voltage rail that is two volts less than the output supply. ECL devices are commonly terminated with -2V to -5.2V, creating a typical output swing of -0.9V to -1.8V. Because of the low value termination resistors, ECL is the highest power dissipation interface by far.

RSECL, or Reduced Swing ECL is similar to ECL, but reduces the swing to *400mV*, but still requires a negative termination voltage.

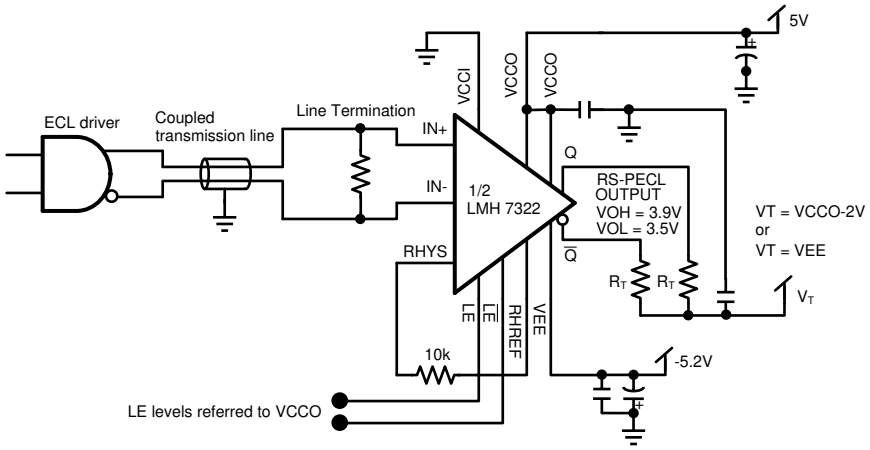


Figure 2-11. RSPECL Termination

PECL, or Positive ECL eliminates the negative supplies and shifts the swings above ground for positive swings of +3.2V and +4V and maintains the 800mV differential.

LVPECL, or Low Voltage PECL is the same as PECL, but lowers the thresholds to +1.6V and +2.4V to allow for lower supply voltages.

RSPECL, or Reduced Swing PECL reduces the swing to 400mV.

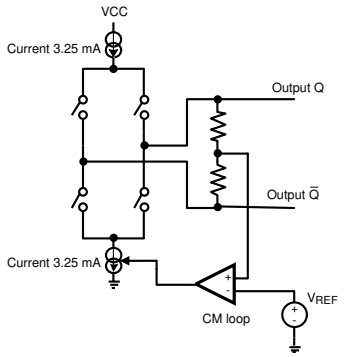
The devices that can support the 400mV swing standards are the LMH7322 and LMH7324.

Table 2-6. Advantages and Disadvantages of ECL Family Outputs

Advantages	Disadvantages
• Reduced output swing increases speed • Rise/Fall times into the picoseconds • Directly interfaces with matched impedance lines • High common mode rejection • Balanced lines reduce radiated EMI	• ECL requires large negative supply voltages (-5.2V) • Low valued terminations (50-100Ω) draw high current • High power dissipation (100's mW) per channel

2.3.3 Low Voltage Differential Signaling

The Low Voltage Differential Signaling (LVDS) output stage uses a switched ±4mA current between the outputs and eliminates the negative supplies and the two pull-down resistors as required for ECL based outputs. LVDS further reduces the output swing to ±400mV centered on +1.2V.



Equivalent Output Circuitry

Figure 2-12. LVDS Output

The LVDS termination is easy to implement with just a single 100Ω termination resistor between the outputs at the receiver. The 100Ω resistor combined with the ±4mA differential current creates the ±400mV differential signal at the receiver.

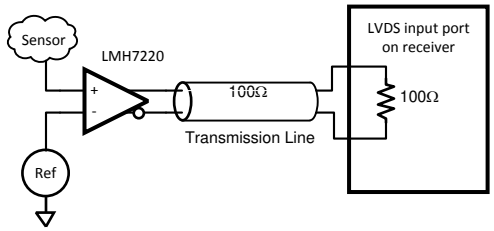


Figure 2-13. LVDS Termination

LVDS, also known as TIA/EIA-644, is also the basis of many popular interlink protocols, such as Display Port, FPD-Link, Channel Link, Firewire, and Serial ATA. Many processors and ASIC's have native LVDS inputs with internal termination resistors.

Examples of devices that support the LVDS standard are the LMH7220, TLV3604/5/7, TLV3801/2 and TLV3811/11C.

Table 2-7. Advantages and Disadvantages of LVDS Outputs

Advantages	Disadvantages
• Even lower output swing increases speed • Single supply operation down to +1.8V • Lower power (50-100mW) • Single 100Ω termination resistor • Directly interfaces with matched impedance lines • High common mode rejection • Balanced lines reduce radiated EMI • Common standard on ASIC and processor inputs • Capable of multi-point distribution • TIA standard TIA-644	• Maximum bitrate up to 3Gbit/s

2.3.4 Current Mode Logic

Current Mode Logic (CML) is a switched-current output, similar to LVDS, but utilized at higher speeds. The termination is normally 50Ω on each output to the positive output termination voltage (V_{CCO}) at the receiver.

The CML differential output swing and common mode voltage is not standardized, and can range from 400mV to 800mV differential. At speeds above 6Gbit/s, the differential is commonly reduced to 400mV.

The output stage consists of two 50Ω resistors to the output supply voltage with two associated switching transistors and a shared current source, as shown in Figure 2-14.

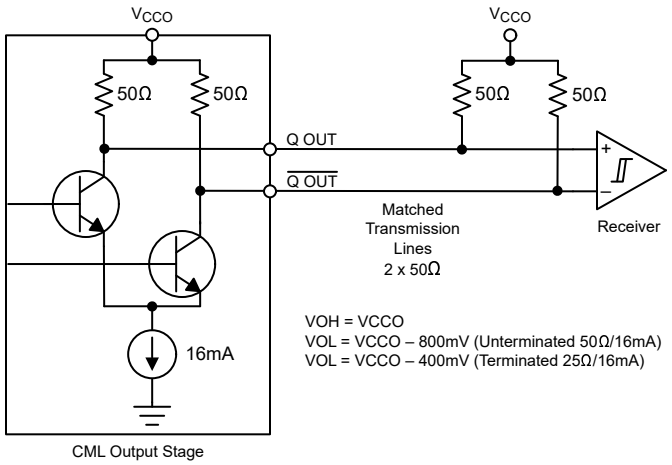


Figure 2-14. CML Output

One output transistor is conducting at a time, depending on the desired output state. The *on* transistor passes the 16mA through the corresponding 50Ω resistor creating a 50Ω/16mA=800mV voltage difference between the output and V_{CCO}.

The other 50Ω resistor acts as a pull-up resistor and pull's the respective output to V_{CCO} as no current is flowing through the resistor.

Because the load termination lines present a parallel 50Ω load to each output, the output swing is now half, or 400mV below V_{CCO} at the receiver.

For CML output, please see the TLV3901 (Preliminary - contact Sales).

Table 2-8. Advantages and Disadvantages of CML Outputs

Advantages	Disadvantages
• Up to 12Gbit/s or more • User selectable differential voltage (reduces crosstalk and EMI) • Directly interfaces with matched impedance lines • High common mode rejection • Balanced lines reduce radiated EMI • Can be AC coupled	• Requires two external 50Ω pull-up resistors • Only supports point-to-point • Higher power dissipation than LVDS • No defined standard - output thresholds can vary between manufacturers

3 Summary

Table 3-1 is a summary table showing the various output type available and the limitations.

Table 3-1. Comparator Output Types

Device Family	Output Type	Can Be Pulled Above Supply	Maximum Pullup Voltage
LM111/211/311	OC/OE	Y	30
LM119/319	OC/OE	Y	36
LMx39/x93/B	OC	Y	38
LM2901/3/B	OC	Y	38
LM306	Differential PP	-	-
LM360	Differential PP	-	-
LM361	Differential PP	-	-
LM397	OC	Y	30
LM6511	OC/OE	Y	30/50
LMC6762	PP	-	-
LMC6772	OC	N	VCC
LMC7211	PP	-	-
LMC7215	PP	-	-
LMC7221	OC	Y	15
LMC7225	OC	N	VCC
LMH7220	LVDS	-	-
LMH7322	RSPECL	-	-
LMH7324	RSPECL	-	-
LMV331	OC	N	VCC
LMV339	OC	N	VCC
LMV393	OC	N	VCC
LMV7219	PP	-	-
LMV7235	OC	N	VCC
LMV7239	PP	-	-
LMV7271/2	PP	-	-
LMV7275	OC	Y	5.5
LMV761/2	PP	-	-
LP111/211/311	OC/OE	Y	30/40
LP339/393	OC	Y	36
LPV7215	PP	-	-
TL3016/3116	PP	-	-
TL331/391	OC	Y	36
TL712/4	Differential PP	-	-
TLC139/339	OC	Y	16
TLC352/4	OC	Y	16
TLC372/4	OC	Y	16
TLC3702/4	PP	-	-
TLC393	OC	Y	16
TLC1391	OC	Y	7
TLV1701/2/4	OC	Y	36
TLV1805	PP	-	-
TLV181x	PP	-	-
TLV182x	OC	Y	40
TLV183x	OC	Y	40
TLV184x	PP	-	-
TLV185x	PP	-	-
TLV186x	OC	Y	40
TLV187x	PP with separate supplies	-	40

Table 3-1. Comparator Output Types (continued)

Device Family	Output Type	Can Be Pulled Above Supply	Maximum Pullup Voltage
TLV192x	OC	Y	65
TLV2302/4	OC	N	VCC
TLV2352/4	OC	Y	8
TLV2702/4	PP	-	-
TLV3011/2	OC	Y	5.5
TLV3231/2	PP	-	-
TLV340x	OC	N	VCC
TLV349x	PP	-	-
TLV350x	PP	-	-
TLV3601/2/3	PP	-	-
TLV3604/5/7	LVDS	-	-
TLV3691	PP	-	-
TLV370x	PP	-	-
TLV3801/2	LVDS with separate supplies	-	-
TLV3811C	LVDS	-	-
TLV3901	CML	-	-
TLV4011	OC	Y	5.5
TLV4021R	PP	-	-
TLV4021S	OC	Y	5.5
TLV4031	PP	-	-
TLV4041	OC	Y	5.5
TLV4051	OC	Y	5.5
TLV4062	PP	-	-
TLV4082	OC	Y	5.5
TLV6700/3	OC	Y	18
TLV6710/13	OC	Y	25
TLV701x	PP	-	-
TLV702x	OC	Y	7
TLV703x	PP	-	-
TLV704x	OC	Y	7
TLV7081	OC	Y	5.5
TLV7211	PP	-	-
TLV902x	OD	Y	6
TLV903x	PP	-	-
TSM102	OC	Y	36
TSX03121	OC/OE	N	3.6

OC = Section 2.1

PP = Section 2.2

OC/OE = *Floating* output capable of Section 2.1.1

LVDS = Section 2.3.3

RSPECL = Section 2.3.2

CML = Section 2.3.4

4 References

- Texas Instruments, *Interfacing Between LVPECL, VML, CML, and LVDS Levels*, application note.
- Texas Instruments, *LVDS, CML, ECL-differential interfaces with odd voltages*, application note.
- Texas Instruments, *An Overview of LVDS Technology*, application note.
- Texas Instruments, *LMH7322 Dual 700ps High Speed Comparator with RSPECL Outputs*, data sheet.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265