Configuring the bq26500 for Gas Gauge Applications

Portable Power Management

ABSTRACT

This application note describes the ten EEPROM locations that can be programmed by the user to optimize the setup for the particular battery and host requirements.

Contents

1   Programming the EEPROM

The EEPROM locations are mapped directly to RAM locations $0x76$ to $0x7f$. These locations cannot be written by the host except during a special test mode. This test mode may be entered by writing $0xdd$ to address $0x6e$. This action then allows write access to these RAM locations and allows transferring the RAM contents into EEPROM. The bq26500 processing is inhibited while $0x6e$ contains $0xdd$ and when EEPROM programming is complete, address $0x6e$ must be written back to $0x00$. The bq26500 processor is reset by this action, but a full reset is not forced. When ILMD is changed, it is necessary to force a full reset to cause the bq26500 to use the new desired LMD value. All other EEPROM values are used on all resets. A full reset may be forced by setting bit 1 = 1 in address $0x01$ and then writing $0xa9$ to address $0x00$.

The actual EEPROM programming is accomplished by reading each address (after previously writing it with the desired data) and then applying a 21-V programming pulse 10 ms – 100 ms wide. After all programming changes have been accomplished, the test system must write $0x00$ to address $0x6e$. This action disables write access to the EEPROM values, resets the bq26500, and allows normal execution to resume.

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2   Initial Last Measured Discharge (ILMD)

This value is the design capacity of the battery. The high byte of Last Measured Discharge (LMD) is set equal to ILMD on a full reset. LMD is then used for the 100% full capacity reference. The bq26500 subsequently updates this value with the learned capacity of the battery. It is wise to program ILMD with a value slightly smaller than the expected initial capacity of the battery. This reduces the perturbation that may occur later in the equipment lifetime due to some unexpected reset, where corruption of RAM values is evident. A reset without RAM corruption (RBI maintains the RAM content) leaves the LMD value at its learned value and does not cause it to be reinitialized to ILMD. Units for ILMD are $256 \times 3\mu$Vh per least significant bit (LSB).

The EEPROM value for ILMD is programmed in address $\texttt{0x76}$. The formula for determining the EEPROM value for ILMD is:

$$\text{ILMD} = \text{DesignCapacity (mAh)} \times \frac{R_S(\Omega)}{256 \times 0.003 \text{ mVh}} \tag{1}$$

Example: If the battery capacity is typically 1000 mAh and the sense resistor value is 20 mΩ, the value to be programmed in ILMD is calculated as:

$$\text{ILMD} = \frac{1000 \text{ mAh} \times 0.02 \text{ } \Omega}{(256 \times 0.003 \text{ mVh})} = 26.04 \tag{2}$$

The next smaller value is 26 decimal, or 1a hexadecimal. Setting ILMD to $\texttt{0x1a}$ initializes LMD to $\texttt{0x1a00}$ (6656 decimal), or 998 mAh with a 20 mΩ sense resistor.

3   Scaled End-of-Discharge Voltage Final (SEDVF)

This voltage should be set to the threshold where the battery is expected to have zero capacity. This threshold is typically 3000 mV. NAC is adjusted to zero during a discharge if this voltage threshold is reached. Units for SEDVF are 8 mV, with a 2048 mV offset.

The EEPROM value for SEDVF is programmed in address $\texttt{0x77}$. The formula for determining the EEPROM value for SEDVF is:

$$\text{SEDVF} = \frac{\text{Design EDVF (mV)}}{8} - 256 \tag{3}$$

Example: To set the EDVF threshold to 3000mV, the value to be programmed in SEDVF is:

$$\text{SEDVF} = \frac{3000 \text{ (mV)}}{8} - 256 = 119 \text{ (decimal) or 77 (hexadecimal)} \tag{4}$$

4   Scaled End-of-Discharge Voltage First (SEDV1)

This voltage should be set to the threshold where the battery is expected to have 6.25% capacity remaining under typical load conditions. This threshold is typically 3350 mV. NAC is adjusted down to LMD/16 during a discharge (unless NAC is already a smaller value) if this voltage threshold is reached. If NAC reaches LMD/16 before the EDV1 threshold is reached and the discharge is a full discharge from full with VDQ = 1, NAC is held at the LMD/16 value until the EDV1 threshold is reached. Thus NAC is synchronized to the 6.25% capacity level at the EDV1 threshold. This threshold also terminates a learning cycle. The learned capacity has LMD $\times$ 6.25% added to the measured discharge from full to EDV1, so setting the EDV1 threshold to a value appropriate to the 6.25% remaining capacity is critical. Units for SEDV1 are 8 mV, with a 2048-mV offset.

The EEPROM value for SEDV1 is programmed in address `0x78`. The formula for determining the EEPROM value for SEDV1 is:

$$SEDVF1 = \frac{Design\ EDVF1\ (mV)}{8} - 256 \qquad (5)$$

Example: To set the EDV1 threshold to 3350 mV, the value to be programmed in SEDV1 is:

$$SEDVF1 = \frac{3350\ (mV)}{8} - 256 = 162.75\ (decimal) \qquad (6)$$

The closest value is 163 decimal or a3 hexadecimal. Setting SEDV1 to `0xa3` sets the EDV1 threshold at 3352 mV.

5 Initial Standby Load Current

The ISLC value programmed in EEPROM should be the estimated standby load current. The bq26500 disables learning a new LMD if a learning dischage cycle terminates at EDV1 when the average discharge current is less than or equal to two times the programmed standby load current value. Units for ISLC are 6 µV per least significant bit.

The EEPROM value for ISLC is programmed in address 0x79. The formula for determineing the EEPROM value for ISLC is:

$$ISLC = \frac{Design\ Standby\ Current\ (mA) \times R_S(m\Omega)}{6\ \mu V} \qquad (7)$$

Example: To set the ISLC value to 20 mA with a 20-Ω sense resistor. The value to be programmed in ISLC is:

$$ISLC = \frac{20\ mA \times 20m\Omega}{6\ \mu V} = 66.7 \qquad (8)$$

The closest value is 67 decimal or 43 hexadecimal. Setting the ISLC at `0x43` sets the initial standby current to 20.1-mA with a 20-mΩ sense resistor. The bq26500 disqualifies a learning cycle if the measured discharge current is less than or equal to 40.2 mA when EDV1 is detected.

6 Digital Magnitude Filter and Self-Discharge Rate (DMFSD)

The digital magnitude filter (DMF) threshold sets the signal level across the sense resistor that is greater than the minimum operational voltage drop. If the signal level measured by the VFC is less than this threshold, the signal is ignored and assumed to be zero. If the signal level measured by the VFC is higher than this threshold, the signal is accepted as measured. The DMF prevents a small VFC offset due to device characteristics as well as any additional offset due to PCB layout from accumulating a large error over a long period of time. During periods with no charge or discharge, any small signal due to offset that is less than the DMF threshold is ignored. If the DMF value is set.

Only multiples of 12 µV are valid for the DMF threshold. Odd multiples of 6 µV are rounded up to the next even multiple. A typical value for the DMF threshold is between 24 µV and 36 µV. The formula for determining the EEPROM value for DMF is:

$$DMF[3:0] = \frac{Design\ Threshold\ (\mu V)}{6\ \mu V} \qquad (9)$$

The self-discharge rate estimate sets the rate at 25°C that is used to estimate the self-discharge capacity loss in one day when the battery is not being charged. This rate is automatically compensated for temperature by doubling the programmed rate for every 10°C increase or halving the programmed rate for every 10°C decrease. A typical value for Lithium-Ion batteries is 0.2% per day at 25°C. The formula for determining the EEPROM value for SD is:

$$SD[3:0] = \frac{2.34}{\text{Design SD } (\%/\text{day @ 25°C})} \tag{10}$$

The EEPROM values for DMF and SD are combined into a single byte and programmed in address `0x7a`.

Example: To set the DMF threshold to 36 μV and the self-discharge rate to 0.2% per day, the value to be programmed in the upper nibble of DMFSD is:

$$DMFSD = \frac{36\mu V}{6\mu V} = 6 \tag{11}$$

The value to be programmed in the lower nibble of DMFSD is:

$$DMFSD = \frac{2.34}{0.2\% \text{ per day}} = 11.7 \tag{12}$$

The closest values are 6 and 12 decimal or 6 and c hexadecimal, so the hexadecimal value for DMFSD is `0x6c`. Setting DMFSD = `0x6c` sets the DMF threshold to 36 μV and the self-discharge rate to 0.195% per day at 25°C.

7   Taper Current (TAPER)

The taper current threshold sets the threshold that average discharge current must fall below for the bq26500 to detect that the battery has received a full charge. The average current must be less than two times the taper current for one measurement and less than the taper current for a second successive measurement to qualify as a taper current charge termination. Voltage must also meet a qualifying threshold that is set in PKCFG for both successive measurements to qualify as a valid taper current charge termination. Typical values for the taper threshold are in the range of LMD/20 to LMD/10. The value programmed in the bq26500 should be a little higher in value than the expected charge termination current of the charger. If the charger terminates before the bq26500 can detect the charge termination, the bq26500 does not adjust the displayed capacity to the full (NAC=LMD) condition. Units for TAPER are 192 μV per LSB.

The EEPROM value for TAPER is programmed in address `0x7b`. The formula for determining the EEPROM value for TAPER is:

$$TAPER = \frac{\text{Design Taper Current (mA)} \times R_S(m\Omega)}{192\ \mu V} \tag{13}$$

Example: To set the taper charge termination threshold to 100 mA:

$$TAPER = \frac{100\ (mA) \times 20(m\Omega)}{192\ \mu V} = 10.4 \tag{14}$$

The EEPROM value for TAPER should be programmed to 10 decimal or `0a` hexadecimal. Setting TAPER=`0x0a` sets the taper termination current to 96 mA with a 20 mΩ sense resistor.

8   Pack Configuration (PKCFG)

The pack configuration value is used to set four different user options.

8.1   PKCFG [7]

Bit 7 sets the initial state of the GPIO pin when power is applied to the bq26500. The host can write to the MODE register to change the GPIO configuration at any time if the GPIO configuration needs to be dynamically changed. If bit 7 = "0", then the GPIO is initialized as an open-drain output. If bit 7 = "1", then the GPIO is initialized as an input. If the GPIO pin is unused, the preferred setup is to program bit 7 = "0" to set the GPIO pin as an output. The GPSTAT bit in MODE register is set to a "1" on POR and turns the open drain FET output "off".

8.2   PKCFG [6:5]

Bit 6 (QV1) and bit 5 (QV0) are used to set the qualification voltage threshold for a current taper charge termination. VOLT must be greater than or equal to the threshold determined by the QV1 and QV0 setup to qualify a charge termination detection. The qualification voltage may be programmed to 3968 mV, 4016 mV, 4064 mV, or 4112 mV (see Table 3 in data sheet). The qualification voltage chosen should be as high as possible to minimize the chance for any premature termination due to a reduction in charge current due to some system or charger issue that may occur before the battery is full. For example, if the system has an operating mode that robs the charger of most of its available power and the remaining charge current for the battery is less than the taper current termination threshold, the taper qualification voltage threshold can prevent a possible false charge termination detection. The qualification voltage threshold should not be set so high that the tolerance of the charger voltage and measurement accuracy of the bq26500 could prevent the reported voltage from exceeding the taper qualification voltage threshold.

Example: With the charger set for 4200mV nominal, with a ±2% tolerance, the minimum charger voltage is 4116 mV. The voltage measurement accuracy of the bq26500 is ±20mV, so an applied 4116 mV source can measure as low as 4096 mV. The taper qualification threshold should be set to 4064 mV, as the highest 4112 mV setting is too high with worst case tolerances. This selection requires setting QV1 (bit 6) = "1" and QV0 (bit 5) = "0".

8.3   PKCFG[4–2]

These bits are unused by the bq26500.

8.4   PKCFG [1]

This bit (DCFIX) can be used to select a fixed discharge rate compensation value and allow the DCOMP location in EEPROM to be used for a customer identification or serial number. If DCFIX = "0", DCOMP specifies the discharge compensation value to be used in computing CACD and ARTTE. If DCFIX = "1", then a fixed default compensation value for DCOMP is used and the DCOMP location in EEPROM is free for the user to program to any desired value. The fixed default compensation value equals 6.25% of the discharge current that exceeds C/4. Most applications find the fixed discharge compensation value to be satisfactory and set DCFIX = "1".

8.5 PKCFG [0]

This bit (TCFIX) can be used to select a fixed temperature compensation value and allow the TCOMP location in EEPROM to be used for a customer identification or serial number. If TCFIX = "0", TCOMP specifies the temperature compensation value to be used in computing CACT and ARTTE. If TCFIX = "1", then the TCOMP location in EEPROM is free for the user to program to any desired value. The fixed default temperature compensation value equals 0.68% of the initial LMD value (design capacity) per degree centigrade below 12°C. This setting also disables learning of new capacity values if the temperature is less than or equal to 12°C . Most applications find the fixed temperature compensation value to be satisfactory and set TCFIX = "1".

The EEPROM bit values for the desired PKCFG options should be combined into a single hexadecimal value and then programmed in address `0x7c`.

Example: To program PKCFG for the unused GPIO pin, 4064 mV taper qualification voltage, and use TCOMP and DCOMP for customer identification information, the programming should be set to `01000011`, or `0x43`.

9   Identification Byte #3 (ID3)

The ID3 value in EEPROM at address `0x7c` may be used to store a customer identification or serial number.

10   Discharge Rate Compensation (DCOMP)

The DCOMP value in EEPROM sets the factors used to calculate the reduction in NAC due to load current. The resulting CACD value is the available capacity, compensated for discharge rate. The EEPROM value may alternatively be used for used for a customer identification or serial number if DCFIX (bit 1 in PKCFG) is set to "1". When this option is used, a default compensation of 6.25% of the discharge current that exceeds C/4 is used for the discharge rate compensation factor and the value in the DCOMP location is ignored. The default discharge rate compensation is equivalent to programming DCOMP with `0x42`.

The discharge rate compensation is used to prevent an overstated run time when a heavy load is applied. When a learning cycle terminates, LMD is adjusted up or down to a value that corresponds to the load current applied at the time that EDV1 is detected. This LMD adjustment automatically compensates NAC to the discharge rate applied at the time EDV1 was detected during a learning cycle discharge. If EDV1 is detected on a non-learning discharge, there is no LMD adjustment, but NAC may have been adjusted at EDV1 due to a heavy load when EDV1 was detected. To properly compute CACD, the discharge compensation adjustment is reduced by the DCMP value computed when EDV1 was last detected. After a full condition is detected, the compensation is reduced by the DCMP value at EDV1 during the last learning cycle discharge. A discharge at a lighter load than during previous discharges projects less capacity than is actually available at the lighter load, but if the load should suddenly increase to the prior level, the bq26500 should accurately reflect the available capacity at the heavier load, preventing a surprise loss of capacity without warning from the bq26500.

The discharge rate compensation values should be chosen to accurately represent the reduction in capacity versus load characteristics of the battery. There are two factors that can be set. One is the discharge offset (DCOFF) value. If the load current is below this value, no capacity reduction occurs. The second factor is the discharge compensation gain factor (DCGN) that determines the slope or rate at which the capacity is reduced as the load current exceeds the discharge offset value.

The DCOFF thresholds are set at 0, C/2, C/4, and C/8 for values of DCOFF of 0, 1, 2, and 3, respectively. DCOFF values are stored as DCOMP[1:0]. The DCGN value is determined by DCOMP[7:2]. The value for DCGN is determined by the desired gain/slope for the capacity reduction in % reduction per unit of current that exceeds the DCOFF threshold. The formula for DCGN is:

$$DCGN[5:0] = 2.56 \times \text{Design Discharge Compensation Gain \%} \tag{15}$$

Once the DCOFF and DCGN values have been determined, they can be combined into a single word and programmed in address `0x7e`.

CACD may be computed from NAC by the following equations:

$$DCMP = DCGN \times \frac{AI - DCOFF}{256}, \text{ for } AI \text{ (Average Discharge Current)} > DCOFF \tag{16}$$

$$DCMP = 0 \text{ for } AI \leq DCOFF \tag{17}$$

$$CACD = NAC - (DCMP - DCMPADJ), \text{ if } DCMP > DCMPADJ \tag{18}$$

$$CACD = NAC \text{ if } DCMP \leq DCMPADJ \tag{19}$$

After an EDV1 detection, the DCMPADJ value is equal to the saved value of DCMP at the last EDV1 detection. This computation continues until a battery full detection occurs. This adjusts CACD for any NAC adjustment at EDV1. After a full battery detection, the DCMPADJ value is changed to the saved value of DCMP at EDV1 from the last learning cycle discharge. This computation continues until EDV1 is again detected. This adjusts CACD for any LMD adjustment during the last learning cycle.

The above equations are also used to compute the discharge compensated available capacity when computing ARTTE. The DCMP equation uses *at rate* (AR) in place of AI for the computation.

Programming example: A battery for use in a system with load currents up to 1C rate has a flat discharge capacity curve for load currents up to about C/4. At a 1C rate, the available battery capacity is down about 5% from the C/4 rate. The DCOFF value of C/4 can be selected with a DCOFF value of 2. At 1C, the current exceeds the DCOFF value by 0.75C, so the desired capacity reduction slope is 5%/0.75C or 6.67%/1C. This yields a DCGN value of:

$$2.56 \times 6.67 = 17.07 \tag{20}$$

The closest value is 17 decimal, or 11 hexadecimal. Setting DCGN to 17 yields a capacity reduction slope of 6.64%. Combining the binary values of `010001` for DCGN and 10 for DCOFF yields a DCOMP value of `01000110`, or `0x46`. This may be easier to compute by noting that shifting the DCGN into the 3rd bit position in DCOMP is the same as multiplying the raw DCGN value by 4. This results in combining $4 \times$ DCGN and DCOFF as follows:

$$4 \times 17 + 2 = 70 \text{ (decimal) or 46 (hexadecimal)} \tag{21}$$

CACD calculation example: ILMD is programmed for a design capacity of 976 mAh. The gauge has not learned a new capacity value, so LMDCMP = 0. The bq26500 measures a load current of 600 mA. The discharge rate compensation reduction is:

$$DCMP = 17 \times \frac{\left(600 - \frac{976}{4}\right)}{256} = \frac{(17 \times 356)}{256} = 23.6 \tag{22}$$

CACD computes to 23.6 mAh less than NAC. CACD is not allowed to increase while discharging, so if the load current drops, CACD remains at the lowest computed CACD value. As discharging continues, NAC continues to drop, but CACD holds steady until NAC drops enough that the new computed CACD value is again less than the previous holding value. Then CACD again starts decreasing as the discharge continues with the lighter load.

DCGN and DCOFF determination: The optimal discharge rate compensation coefficients may be determined from the typical discharge curves on the battery. Discharge curves at various discharge rates are generally available from the cell manufacturer. The capacity of the cells at the various discharge rates may be determined from the discharge curves. If the discharge curves show time instead of capacity, the capacity may be computed by multiplying the discharge rate by the discharge time to reach the chosen EDV0 voltage threshold. The curves are generally plotted at various C–rates. The 1C rate is normally the current in mA that equals the cell capacity in mAh at a C/5 discharge rate. These capacity values in mAh may be plotted versus current as shown in Figure 1.
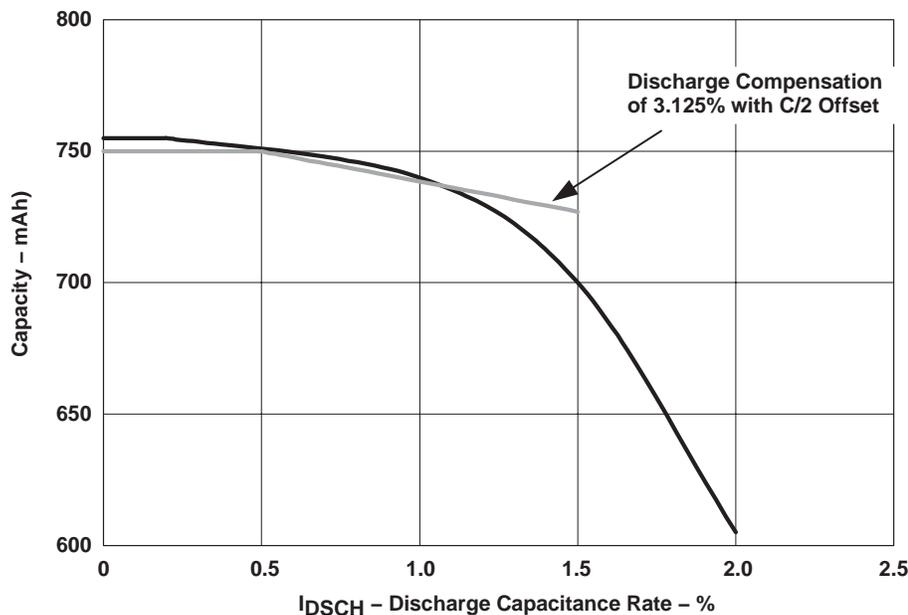

Figure 1.

The cell capacitance at the minimum load current where learning is allowed (excludes standby load current) should be the value used to compute ILMD. Choose the DCOFF value (C/8, C/4, or C/2) and a DCGN (slope) that best matches the capacity versus load curve from the minimum load current value to the maximum (steady-state) load value expected. Figure 1 shows discharge compensation with DCOFF of C/2 and a slope of 3.125% reduction that would be appropriate for operation up to 1.25°C. The ILMD value is programmed to 750 mAh in this example.

11   Temperature Compensation (TCOMP)

The TCOMP value in EEPROM sets the factors used to calculate the reduction in CACD due to temperature. The resulting CACT value is the available capacity, compensated for both discharge rate and temperature. The EEPROM value may alternatively be used for used for a customer identification or serial number if TCFIX (bit 0 in PKCFG) is set to "1". When this option is used, a default compensation of 0.6836% of design capacity per degree C below 12°C is used for the temperature compensation factor and the value in the TCOMP location is ignored. The 12°C threshold is also used to disqualify any learning cycles where the temperature is less than or equal to 12°C. The default temperature compensation is equivalent to programming TCOMP with `0x7c`.

The battery impedance increases rapidly at cold temperature. This causes additional capacity loss at a given load current, since the battery voltage drops to the minimum system operating level more quickly than at higher temperatures. If the temperature increases, the impedance decreases again and the available capacity increases. The temperature compensation is used to prevent overstating the available run time at cold temperatures. The increased impedance at cold temperature causes the EDV1 condition to be reached much sooner than at higher temperatures and if TCOMP is properly set, CACT shows the actual available capacity at cold temperatures. NAC may be adjusted down when EDV1 is detected and reflects the temperature compensated available capacity without any additional reduction due to TCOMP until the battery is again charged to full. To correctly compute CACT, the TCMP temperature compensation reduction value is saved when EDV1 is detected. The TCMP temperature compensation reduction is reduced by this value until the battery full condition is again detected. If the battery temperature increases after EDV1 is detected, it is possible for CACT to be larger than NAC.

Temperature compensation factors should be chosen that represent the battery capacity variation with temperature at the nominal expected load. There are two factors that can be set. The temperature compensation offset threshold TOFF, sets the temperature threshold for disqualification of a learning cycle and also the temperature threshold above which there is no temperature compensation. The applied temperature compensation is proportional to the temperature drop below this threshold. The second factor is the temperature compensation gain threshold TCGN. This factor sets the percentage of design capacity (DC), or initial LMD value that is used to reduce the available capacity for each degree that temperature is below TOFF. (design capacity = initial LMD value = ILMD × 256)

The TOFF threshold is the low nibble of TCOMP and reads directly in degrees C (or °K – 273). The upper nibble of TCOMP is the TCGN factor. The formula for TCGN is:

$$\text{TCGN[3:0]} = 10.24 \times \text{Design Temp Compensation Gain} \, (\% \text{ of DC}/°\text{C}) \tag{23}$$

Once the TOFF and TCGN values have been determined, they can be combined into a single word and programmed in address `0x7f`.

$$TCMP = TCGN \times ILMD \times \frac{273 + TOFF - T}{4}, \text{ for } T < 273 + TOFF \quad (24)$$

$$TCMP = 0, \text{ for } T \geq 273 + TOFF \quad (25)$$

$$CACT = CACD - (TCMP - TCMPADJ) \quad (26)$$

After an EDV1 detection, TCMPADJ equals the TCMP value when EDV1 was detected. This computation continues until a full battery detection is made. This compensates for any NAC adjustment made at EDV1 due to cold temperature. After a full battery detection, TCMPADJ is set to zero. This computation continues until EDV1 is again detected.

Equations (21) through (24) are also used to compute the temperature compensated available capacity when computing ARTTE. The CACD value in the above equations is computed with a DCMP value that uses AR in place of AI for the computation.

Programming example: Desired temperature compensation is a 1% reduction in capacity for each degree below 10°C, with no reduction at temperatures higher than 10°C. The learning of new LMD values is disabled for temperatures at or below 10°C. TOFF is 10 decimal or a hexadecimal and is the lower nibble of TCOMP.

$$TCGN = 10.24 \times 1 \left(\% \text{ of } DC/°C\right) = 10.24 \quad (27)$$

The closest value is 10 decimal, or a hexadecimal. Setting TCGN = 10 yields a compensation value of 0.976 % reduction in capacity per degree Centigrade below 10°C. Combining TCGN and TOFF yields a value of `0xaa` to program in TCOMP.

CACT calculation example: ILMD is programmed for a design capacity of 998 mAh. ILMD is the high byte of the design capacity and has a value of 998 mAh/256. The temperature is 5°C, or 278 K.

$$TCMP = \frac{10 \times \left(\frac{998 \text{ mAh}}{256}\right) \times (273 + 10 - 278)}{4} = 48.7 \text{ mAh} \quad (28)$$

At 5°C, CACT is reduced from CACD by 48.7 mAh. This is a reduction of 9.75 mAh per degree Centigrade, or about 0.98% of the 998-mAh design capacity for each degree below 10°C.

TCGN and TOFF determination: The TCGN and TOFF values may be determined by first plotting the battery capacity versus temperature at the nominal load condition. TCGN and TOFF values may be chosen that give a best fit to this curve over the expected cold temperature operating range. This operation is much the same as determining DCGN and DCOFF from Figure 1.

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