Application Note

Driving SiC MOSFETs with Non-Isolated Gate Drivers

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ABSTRACT

The need for higher power density in smaller form factors has increased the prevalence of wide-bandgap semiconductor technologies like silicon carbide (SiC). These switches have traditionally been used in higher power (>10kW) designs often requiring isolated gate drivers, particularly in electric vehicles and charging stations. As SiC technology continues to scale, there are increasing numbers of industrial customers considering SiC technology for lower power, non-isolated applications. This application note outlines the Texas Instruments (TI) portfolio of non-isolated low-side gate drivers for SiC MOSFETs, including key considerations for proper system design, and a power factor correction (PFC) design example.

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Trademarks

1 Introduction

Silicon Carbide (SiC) power switches are becoming more popular in both industrial and automotive applications due to the support for high switching frequency, high voltage, and high current. SiC MOSFET designs provide a good balance between high frequency and high power applications. Gate drivers play a critical role in controlling SiC MOSFETs effectively, and careful system design of the gate driver is essential for verifying the SiC MOSFET stays within its safe operating area.

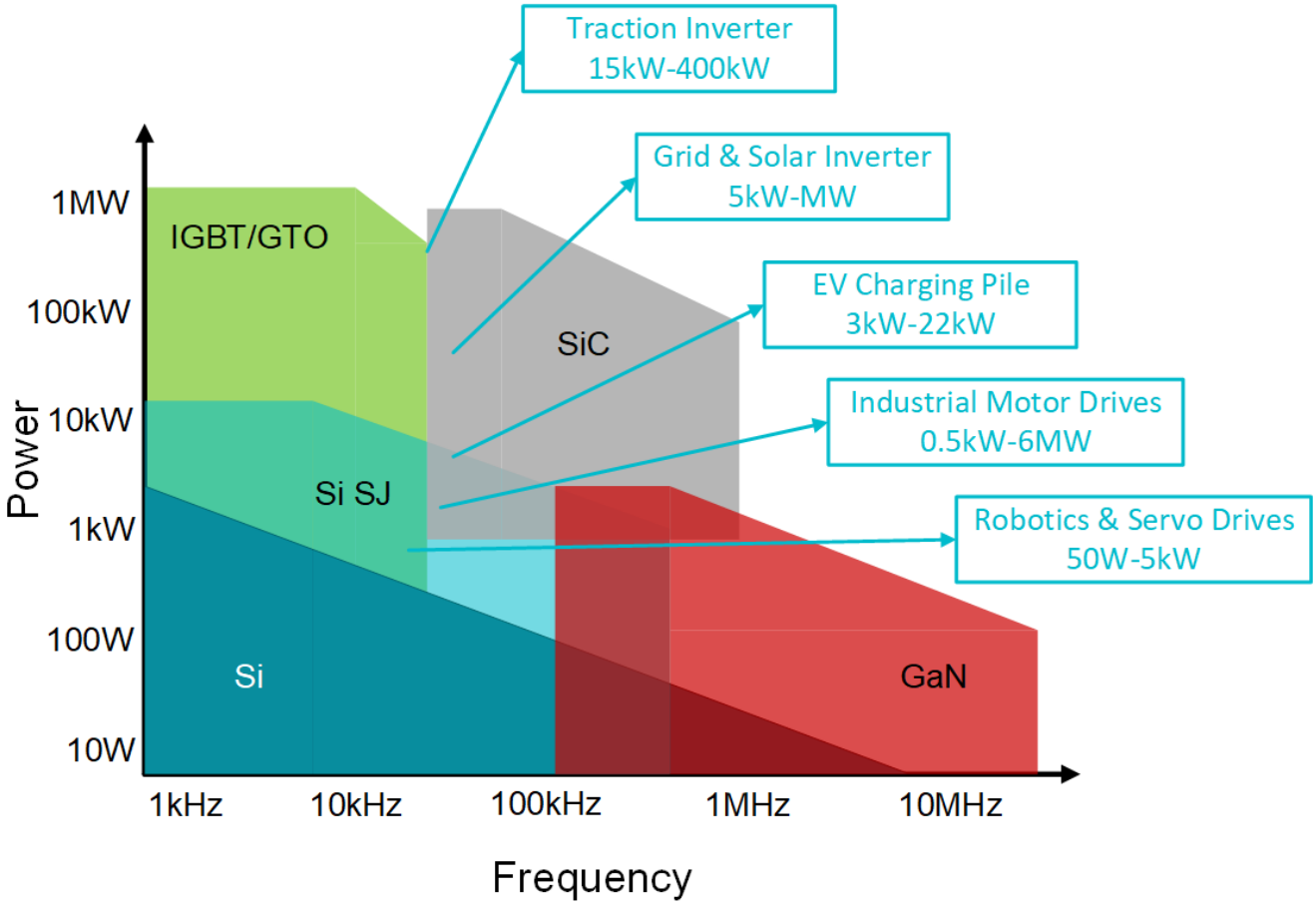

Figure 1-1. Power Switch Technologies and Common Applications

This application note discusses Texas Instruments non-isolated low side gate driver products, including design details for features such as undervoltage lockout (UVLO), short-circuit protection, and support for a negative bias supply. A gate driver design example is presented for a power factor correction (PFC) continuous conduction mode (CCM) boost topology. The gate driver requirements are discussed with respect to max supply voltage (V_{DD}) rating, peak current capability, UVLO threshold, short-circuit protection design, external gate drive resistor, and power dissipation.

2 TI Non-Isolated SiC MOSFET Gate Drivers Overview

TI's latest low-side gate drivers, UCC5710X, UCC5713x, and UCC5714x, are the first non-isolated drivers from TI to feature integrated short-circuit protections. The UCC5710x has DESAT protection, and the UCC5713x or UCC5714x have positive or negative, respectively, over-current protection (OCP). While these methods of short-circuit protection achieve the same goal, each method has advantages: OCP is simpler to implement with more customizability, while DESAT is inherently more efficient as there is no sense resistor to dissipate power.

UCC5710X, UCC5713x, and UCC5714x also have additional features that make them preferred for driving SiC MOSFETs. This includes high UVLO options to prevent switch damage and power loss as the system powers up or experiences supply failures, negative bias supply capability to help hold the power switch gate as low as -15V to protect from accidental turn on, and thermal shutdown function to turn off the driver when an over temperature condition is detected. These features in addition to negative IN voltage capability and short propagation delay make UCC5170x, UCC5713x, and UCC5714x robust and efficient drivers for systems using SiC MOSFETs. Table 2-1 shows more detailed specifications for these drivers.

Table 2-1. Non-Isolated Low Side SiC MOSFET Gate Drivers

PARAMETER		UCC27614	UCC27531	UCC5710x	UCC5713x / UCC5714x
Protection Features	Integrated Protection	None	None	DESAT	OCP
Absolute Maximum Ratings	Supply Voltage, V_{DD}	30V	35V	30V	30V
Recommended Operating Conditions	Supply Voltage, V_{DD}	26V	32V	26V	26V
	Input Voltage: IN_A, IN_B, EN_A, EN_B	-10 to 26V	-5 to 25V	-5 to 26V	-5 to 26V
	Negative Supply Voltage, V_{EE}	N/A	N/A	-15V(B variant)	-15V(B variant)
	Operating Junction Temperature Range	-40°C to 150°C	-40°C to 150°C	-40°C to 150°C	-40°C to 150°C
UVLO	Supply Start Threshold	4.1V	8.9V	8.0V / 13.5V	8.0V / 13.5V
Outputs	Sink / Source Peak Current	10A / 10A	2.5A / 5A	3A / 3A	3A / 3A
Switching Characteristics (C_{Load} = 1.8nF)	Rise Time, t_R (10% to 90%) Fall Time, t_F (90% to 10%)	5ns, 4ns	15ns, 7ns	8ns, 14ns	8ns, 14ns
	Input to Output Propogation Delay	17ns	17ns	26ns	26ns
Additional Features	Enable	Yes	Yes	W variant	Yes
	Split Output	No	Yes	C variant	C variant
	Soft Turn Off	No	No	Yes	No

3 SiC MOSFET Gate Driver Design Considerations

SiC MOSFETs are used in high power systems and are primarily implemented in applications using high switching frequencies (>50kHz). Several gate driver design considerations are required to verify proper and efficient SiC MOSFET operation. This section describes the most important considerations for SiC MOSFET gate drivers.

3.1 Undervoltage Lockout (UVLO)

UVLO is a key gate driver feature that protects the SiC MOSFET by turning off the gate driver output when the bias supply voltage is less than expected. If the bias supply of the gate driver without UVLO drops to a lower voltage, then the gate driver outputs a voltage that can still reach the SiC MOSFET gate-source voltage (V_{GS}) turn-on threshold, but this results in severe conduction losses because the SiC MOSFET is not fully turned on.

This conduction loss can be shown by the I-V curve relationship between drain current (I_D) and drain-source voltage (V_{DS}) of a SiC MOSFET, relative to V_{GS}. A low V_{GS} can cause the SiC MOSFET to saturate sooner and prevent the MOSFET from fully turning on due to high drain-source on-resistance ($R_{DS(on)}$).

Figure 3-1 shows the typical I-V curves for Si MOSFET vs. SiC MOSFET; if the V_{GS} is lower, then the MOSFET saturates faster. For both Si MOSFET and SiC MOSFET, there are large margins between each curve for V_{GS} < 10V, indicating that the MOSFET is not fully turned on. Lower V_{GS} results in higher conduction losses due to higher $R_{DS(on)}$.

However, the difference between Si MOSFET and SiC MOSFET is more clear for V_{GS} ≥ 10V. For Si MOSFET, the curves at V_{GS} = 10V and V_{GS} = 15V are nearly identical, indicating that the Si MOSFET has fully turned on at V_{GS} = 10V. Increasing V_{GS} for Si MOSFET beyond 10V will have minimal effect in reducing conduction losses. For SiC MOSFET, there are still large margins between the curves at V_{GS} = 10V and V_{GS} = 15V, indicating that the SiC MOSFET has not fully turned on at V_{GS} = 10V like its Si MOSFET counterpart. Operating the SiC MOSFET at V_{GS} = 10V results in more conduction loss when compared to operating at V_{GS} = 15V.

As a result, high UVLO is often a requirement for SiC MOSFETs to minimize conduction losses during bias supply start-up or shutdown.

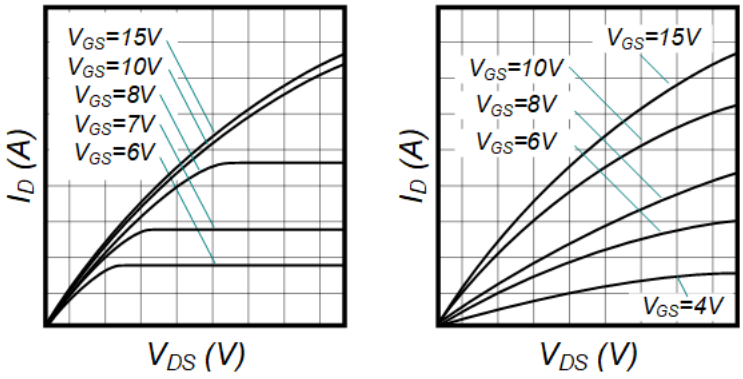

Figure 3-1. I-V Curves for a Si MOSFET (left) and SiC MOSFET (right)

3.2 Negative Bias Supply (Bipolar Drive)

Negative bias supply is another common requirement for driving SiC MOSFETs. High-power applications may result in high dv/dt that induces current through the Miller capacitances of the SiC MOSFET and charges the gate of the SiC MOSFET. The SiC MOSFET can inadvertently turn on and result in destructive consequences. Negative bias voltage can be used to prevent spikes from reaching the turn-on threshold, verifying that the SiC MOSFET stays off (also known as bipolar drive). Figure 3-2 shows how a transient 2.5V spike can affect a SiC MOSFET with a 2.5V gate-source threshold: using 0V turn-off results in accidental turn-on, while using -5V turn-off verifies that the SiC MOSFET stays off.

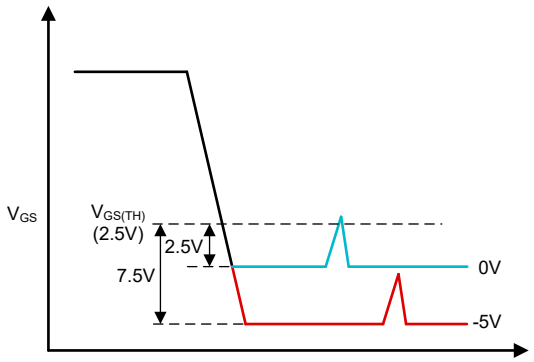

Figure 3-2. Turn-Off Level Comparison

3.3 Short-Circuit Protection

High-power applications carry a large risk of short-circuit events, which can severely damage the SiC MOSFET and other components in the system. Different short-circuit protection methods can be implemented with fast detection and limited false trigger to mitigate damage from short-circuit events.

3.3.1 Desaturation Protection

Desaturation (DESAT) protection is a type of short-circuit protection that is voltage-based. Figure 3-3 shows a typical DESAT circuit.

When the SiC MOSFET is on during normal operation, then I_D is within specifications, keeping the drain voltage low $\left(V_{DS} = I_D \times R_{DS(on)}\right)$. This keeps the high-voltage blocking diode (D_{HV}) forward-biased, allowing the current sourced from I_{CHG} (indicated in the figure by the down arrow from VDD) to flow through D_{HV} without charging the blanking capacitor (C_{BLK}).

When a short-circuit occurs, then large I_D causes the drain voltage to rise high. This causes D_{HV} to become reverse-biased, blocking the flow of current sourced from I_{CHG}. The charging current now charges C_{BLK}, and once the C_{BLK} voltage exceeds the internal DESAT voltage threshold (V_{DESAT}), the comparator indicates that short-circuit is detected.

The time to charge the capacitor is the blanking time, which can be calculated in Equation 1 by using the internal V_{DESAT} and I_{CHG}. Reducing the capacitor value can shorten the time to trigger DESAT protection, which can be useful for SiC MOSFET applications.

$$t_{BLK} = \frac{V_{DESAT} \times C_{BLK}}{I_{CHG}} \quad (1)$$

While the internal V_{DESAT} is set by design, the drain voltage needed to trigger DESAT protection can be adjusted by modifying the components in series between the DESAT pin and SiC MOSFET drain, which can be calculated in Equation 2. $V_{DESAT(actual)}$ refers to the drain voltage that triggers DESAT.

$$V_{DESAT(actual)} = V_{DESAT} - \left(I_{CHG} \times R_{BLK}\right) - V_{F(D_{HV})} \quad (2)$$

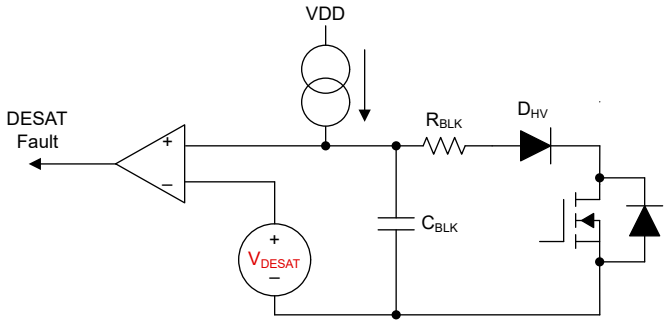

Figure 3-3. DESAT Protection Circuit

3.3.2 Overcurrent Protection

Overcurrent protection (OCP) is another type of short-circuit protection that is current-based. Figure 3-4 shows the OCP circuit. A shunt resistor is used to measure I_D, which yields the shunt voltage. When a short-circuit occurs, then large I_D causes the shunt voltage to rise high. If the shunt voltage rises above the OCP voltage threshold, then the comparator indicates that short-circuit is detected.

The shunt resistor value is selected based on the required drain current to trigger OCP (typically just below the maximum drain current that the SiC MOSFET can handle), which can be calculated in Equation 3.

$$R_S = V_{OCTH} / I_{D(OC)} \tag{3}$$

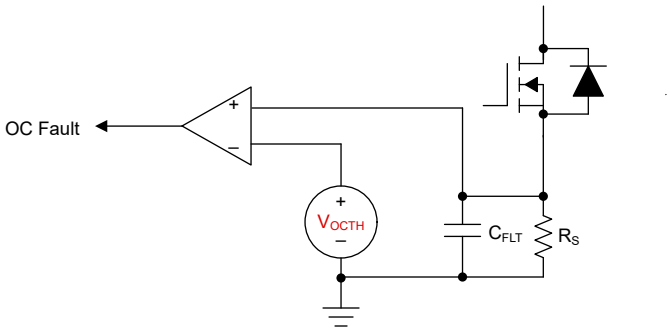

Figure 3-4. OCP Circuit

3.3.3 Soft Turn-Off

After a short-circuit event is detected, the SiC MOSFET needs to be turned off safely to minimize damage to the system.

Parasitic inductances can interact with fast I_D switching to induce voltage $\left(V = L \times \frac{di}{dt}\right)$ across the SiC MOSFET. Under nominal events where I_D is within the rated limits, using normal turn-off induces voltage that is within limits of the SiC MOSFET. However, during short-circuit events, the induced voltage can reach catastrophic levels that can destroy the SiC MOSFET.

Soft turn-off is a design that increases the turn-off time, which consequently reduces the switching speed when turning off the SiC MOSFET. This decreases di/dt to minimize the induced voltage. Figure 3-5 shows a plot illustrating how OUT turns off slowly when short-circuit is detected via DESAT protection in UCC5710x. Other conceptual timing characteristics related to DESAT protection are included in the diagram: t_{DESLEB} (leading edge blanking time to prevent false trigger from SiC MOSFET turn-on transient), t_{DESFIL} (deglitch filter time to prevent false trigger from noise while SiC MOSFET is on), $t_{DES2OUT}$ (time between reaching DESAT threshold and OUT falling to 90%), $t_{DES2FLT}$ (time between reaching DESAT threshold and $\overline{FLT}$ falling).

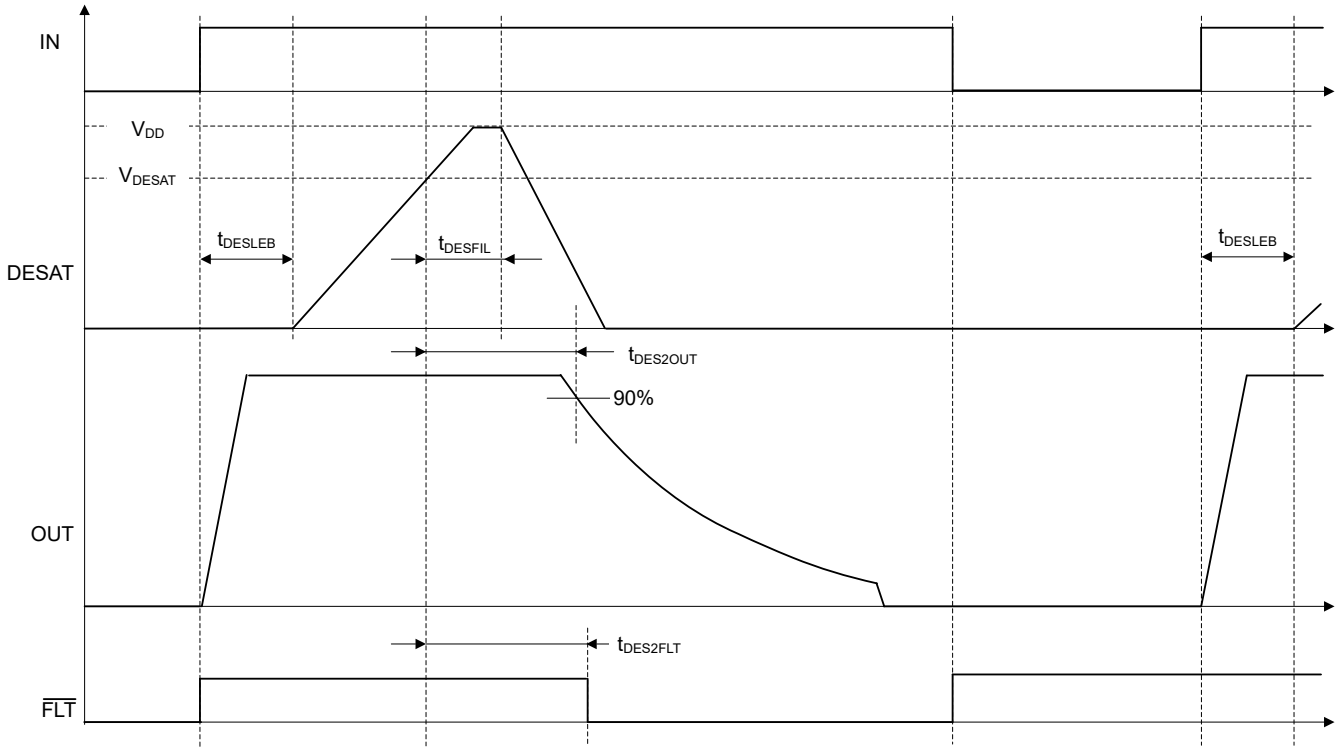

Figure 3-5. Soft Turn-Off

4 PFC CCM Boost Low-Side Gate Driver Example

In a power factor correction (PFC) continuous conduction mode (CCM) boost application, SiC MOSFETs can offer substantial benefits. The low conduction and switching losses in SiC MOSFETs enable higher efficiency and increased power density for applications above 1kW. Higher switching frequencies can be realized with SiC technology, contributing to magnetics size and cost reduction opportunities. In this example, this application note outlines the low side gate driver considerations for a 3kW PFC CCM boost. Target design parameters are outlined in Table 4-1.

Table 4-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
PFC Input Voltage Range	185-265Vac, 60Hz
PFC Nominal Output Voltage	400VDC
Maximum Steady-State Output Power	3000W
SiC MOSFET Positive Bias Supply	+20V
SiC MOSFET Negative Bias Supply	-5V
Switching Frequency	60kHz
Switching Slew Rate	20V/ns
Short-circuit Detection	Yes
Maximum Ambient Temperature	100°C

In this example the chosen SiC MOSFET has ratings as follows: 650V maximum V_{DS}, 35A continuous I_D rating (at T_c = 100C), total Q_G of 73nC, and 45mΩ typical $R_{DS(on)}$ at V_{GS} = 20V. Figure 4-1 shows the components needed for a typical PFC CCM boost application.

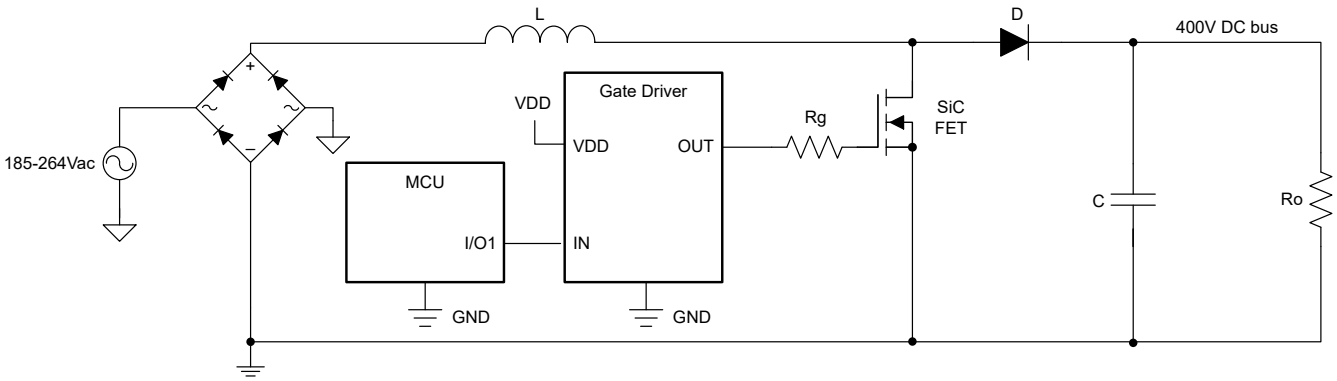

Figure 4-1. Typical Application of Gate Driver in PFC System

4.1 Gate Driver Requirements

Choosing the proper gate driver for a SiC MOSFET involves careful consideration of the bias voltage rating, peak current capability, protection features, gate resistor, and power dissipation.

To minimize conduction loss, the bias voltage is set to 20V, and a negative bias of -5V is set to prevent accidental turn-on from transients. The potential difference yields the V_{DD} requirement for the gate driver to be at least 25V.

To minimize switching loss, the gate driver must also be capable of providing the required peak current to achieve the target switching speed. The system requirement for switching speed is typically described in terms of slew rate. For the PFC in this example, the requirements state that the SiC MOSFET needs to be turned on with a slew rate of 20V/ns or higher under a DC bus voltage of 400V. This means that the full V_{DS} swing during the SiC MOSFET turn-on needs to occur in 20ns $\left(= 400V/20\frac{V}{ns}\right)$ or less. During V_{DS} swing, the Miller charge of the SiC MOSFET (Q_{GD} parameter, which is 27nC for the chosen SiC MOSFET) is charged by the peak current of the gate driver; the peak current needs to charge the Q_{GD} in 20ns or less. This yields the required peak current to be at least 1.35A $(= 27nC/20ns)$.

UVLO is a key protection feature to minimize damage to the SiC MOSFET in case of a power supply failure. If a failure causes V_{GS} to fall to unsafe levels, then the SiC MOSFET can experience conduction losses. This can diminish efficiency, increase heating, and reduce lifetime of the SiC MOSFET. A gate driver with a high UVLO rating is beneficial in this application.

Having a form of short-circuit detection is another important protection feature for the SiC MOSFET. Since SiC MOSFETs do not have a clear transition from linear to saturation region like the transition from saturation to active region in IGBTs, using a single-voltage threshold detection such as DESAT protection cannot be accurate without extensive modification. OCP is a more preferred choice, which uses a shunt resistor to measure current.

4.2 Gate Driver Selection

The UCC57132B is preferred for this application. The UCC57132B is a 30V low-side gate driver with 3A source/sink peak current rating, OCP, and fault report. The UCC57132B also accommodates negative bias input, detects OCP with fault indication, and has a high UVLO threshold of 13.5V (typ).

The bypass capacitors for the bias supply are critical components to consider when designing the UCC57132B into the system. These bypass capacitors need to be as close as possible to VDD/VEE pin and GND pin of the UCC57132B to increase noise immunity. TI recommends having at least two bypass capacitors in parallel, where the first capacitor is 0.1uF, and the second capacitor is 1uF or larger (0.1uF capacitor must be closer to the IC than the larger capacitor). Adding a small bypass capacitor or RC filter on the IN pin to increase noise immunity for the input PWM signal is useful.

The OCP pin has a 500mV threshold, which can be used to calculate the shunt resistor value. The SiC MOSFET has a maximum continuous I_D rating at T_c = 100C of 35A, leave room for margin; the shunt resistor can be calculated to be 25mΩ $(= 500mV/20A)$. An addition of a small RC filter close to the OCP pin can help mitigate noise that falsely triggers OCP.

The fault signal recovery time is calculated by the RC filter at the EN/$\overline{\text{FLT}}$ pin using Equation 4. R_{ENU} refers to the internal pull-up resistance of the EN/$\overline{\text{FLT}}$ pin, and V_{ENH} refers to the enable signal rising threshold. Both values can be found in the UCC57132B data sheet (R_{ENU} = 2MΩ and V_{ENH} = 2.2V). Using R_{FLTC} = 5kΩ and C_{FLTC} = 100pF, the fault recovery time can be calculated as t_{FLTC} = 58ns.

$$t_{FLTC} = -\left(\frac{R_{FLTC} \times R_{ENU}}{R_{FLTC} + R_{ENU}}\right) \times C_{FLTC} \times \ln\left(1 - \frac{V_{ENH}}{V_{DD}}\right) \quad (4)$$

Adding an external gate resistor has several benefits. Gate resistors limit the output turn-on and turn-off time, reducing EMI, and takes on some of the gate-charge-related power dissipation. The UCC57132B does not have split output feature to individually control turn-on and turn-off time, but a blocking diode can be used to simulate split outputs. Selecting a gate resistor involves experimenting with bench testing, but a good starting point is 2.2Ω for turn-on and 1.1Ω for turn-off (effective with blocking diode by paralleling two 2.2Ω resistors).

Figure 4-2 shows the design values for the UCC57132B. Careful testing is required to validate the component values, and modification can be required accordingly.

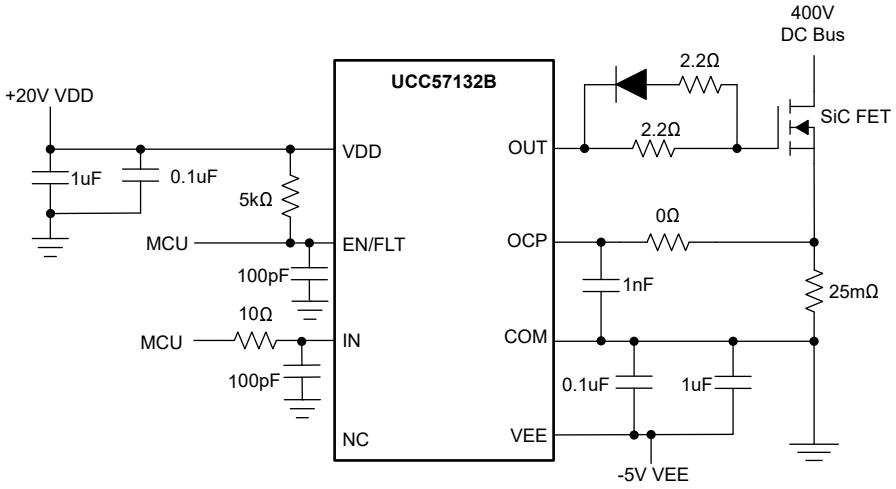

Figure 4-2. UCC57132B With Design Values

4.3 Gate Driver Power Dissipation

Check if the power dissipation of the selected gate driver is within specifications. The total power dissipation (P_{tot}) in a low side gate driver can be broken down into two portions: DC losses and switching losses. DC losses (P_{DC}) are a function of the gate driver's quiescent current consumed to bias the internal circuits. The switching losses (P_{SW}) depend on the gate charge, bias voltage, switching frequency, and internal/external gate resistance of the power switch.

The thermal specifications found in the gate driver data sheet and estimated ambient temperature can be used to estimate the maximum allowable power dissipation of the gate driver (P_{max}). P_{max} can be compared to the calculated P_{tot} to make sure the gate driver is within specifications. Equation 5 and Equation 6 estimates the maximum power dissipation for the UCC57132B.

$$P_{max} = \frac{T_J - T_A}{R_{\theta JA}} \tag{5}$$

$$P_{max} = \frac{150°C - 100°C}{126.6\frac{°C}{W}} = 395mW \tag{6}$$

UCC57132B has a maximum VDD quiescent current of 1.3mA and maximum VEE quiescent current of 1.1mA. With a +20V VDD supply and -5V VEE supply, the DC losses are 31.5mW $(= (1.3mA \times 20V) + (-1.1mA \times -5V))$.

Switching losses can be estimated using Equation 7 and Equation 8. $R_{OH(eff)}$ represents the effective pull-up resistance of the output structure during output turn-on (1Ω); this is due to the hybrid pull-up structure of the UCC57132B output stage, which contains a pull-up NMOS in parallel with the pull-up PMOS. This is distinct from the R_{OH} parameter in the data sheet, which only represents the pull-up PMOS (using R_{OH} instead of $R_{OH(eff)}$ is okay if overestimation is needed). The R_{OL} refers to the typical pull-down NMOS and can be found in the data sheet (1Ω). $R_{GATE(H)}$ refers to the turn-on external gate resistance, and $R_{GATE(L)}$ refers to the turn-off external gate resistance. $R_{GATE(I)}$ refers to the intrinsic gate resistance of the selected SiC MOSFET (2Ω).

$$P_{SW} = Q_g \times \left(V_{DD} - V_{EE}\right) \times f_{sw} \times \frac{1}{2}\left(\frac{R_{OH(eff)}}{R_{OH(eff)} + R_{GATE(H)} + R_{GATE(I)}} + \frac{R_{OL}}{R_{OL} + R_{GATE(L)} + R_{GATE(I)}}\right) \tag{7}$$

$$P_{SW} = 73nC \times \left(20V - \left(-5V\right)\right) \times 60kHz \times \frac{1}{2}\left(\frac{1\Omega}{1\Omega + 2.2\Omega + 2\Omega} + \frac{1\Omega}{1\Omega + 1.1\Omega + 2\Omega}\right) = 23.9mW \tag{8}$$

The estimated total power dissipated in the package is calculated in Equation 9 and Equation 10.

$$P_{tot} = P_{DC} + P_{SW} \quad (9)$$

$$P_{tot} = 31.5mW + 23.9mW = 55.4mW \quad (10)$$

For initial design purposes, the calculated P_{tot} is much smaller than the estimated P_{max} of the UCC57132B, keeping the device within specifications. Further thermal analysis must be completed throughout the design phase to verify proper cooling. More information about thermal analysis can be found by reading *Semiconductor and IC Package Thermal Metrics* app note.

5 Summary

This application note articulates the non-isolated low side gate driver designs from Texas Instruments (TI) for Silicon Carbide (SiC) switches. TI gate drivers can control SiC power switches with the necessary protection features required, enabling higher power density and smaller form factor designs in industrial and automotive systems.

6 References

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- Texas Instruments, *Why is high UVLO important for safe IGBT & SiC MOSFET power switch operation*, application note.
- Texas Instruments, *External Gate Resistor Design Guide for Gate Drivers*, application note.
- Texas Instruments, *How to drive a SiC FET or IGBT with a negative bias using a low side gate driver (bipolar drive)?*, E2E™ design support forum.
- Texas Instruments, *SiC Gate Driver Fundamentals*, electronic book.
- Texas Instruments, *Power Loss and Thermal Considerations for Gate Drivers*, video.

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