PR2000: A 90-W, High-Efficiency, LLC Series-Resonant Converter with Secondary-Side Synchronous Rectification

Power Management – Consumer Isolated Power

1 INTRODUCTION

This guide documents the design of a low-profile, high-efficiency, LLC series-resonant DC/DC converter that incorporates secondary-side synchronous rectifiers (SR). The converter is optimized for a 90-W laptop adapter application and designed to operate from the high-voltage output produced by an upstream AC/DC boost power factor correction (PFC) converter. The boost PFC converter would allow this adapter to operate from a universal line-voltage input. The LLC resonant converter provides an isolated output of 19.5 VDC from an input voltage range of 320–420 VDC. At a rating of 90 W the circuit has a maximum continuous load of 4.6 A.

Off-line ac adapters used for powering laptop PCs demand increasingly higher operating efficiencies in ever smaller packages. The combination of high efficiency operation and a low-profile package reduces the adapter's overall size, weight and cost by minimizing the need for thermal management. The improved efficiency of this design is made possible by replacing the Schottky rectifiers that are normally used in the secondary circuit with synchronously controlled MOSFETs. Due to their low drain-source 'on' resistance, synchronously switched MOSFETs can operate with a much lower voltage drop than regular diode rectifiers. Depending on the combination of load current and output voltage the power dissipation of an adapter can be reduced by several watts using this design.

The circuit features four integrated circuit devices from Texas Instruments. They include the UCC25600; a low-cost resonant converter controller, and the UCC24610; a green rectifier controller. Other parts used include the TL431A shunt regulator and the TPS71550 low drop-out linear regulator. The circuit requires a 12-VDC external bias supply to operate. In a regular adapter design the bias power would be produced by the boost PFC AC/DC converter stage that would normally precede this circuit.

2 SCOPE

The UCC24610 Green Rectifier Controller is optimized for 5-V systems and can be used for LLC outputs up to 15 V when a separate 5-V supply is available. Above 15 V the UCC24610 is limited by the 50-V maximum voltage rating of the VD pin. This is because in a conventional secondary rectifier arrangement, that employs two rectifiers with a center-tapped secondary winding, each rectifier sees a peak reverse voltage equal to twice the regulated output.

The scope of this reference design guide is to describe the design and performance of a functional circuit that extends the application of the UCC24610 to systems with output voltages up to 30 V. This is achieved using an alternate topology for secondary rectification and addressing the design constraints that the topology presents. Two configurations are described for synchronizing the turn-off of each SR circuit using the gate-drive signals on the primary side of the converter.

An area not addressed by this guide is electromagnetic compatibility (EMC). For most applications, EMI filter components are added so that the design meets applicable environmental and system compatibility requirements. To comply with EMC standards, components such as input and output filters are required to suppress electromagnetic interference (EMI).

3 ELECTRICAL PERFORMANCE

Table 1 Performance Specifications

Symbol	Parameter	Notes and Conditions	Min	Nom	Max	Units
INPUT CHARACTERSTICS						
V_I	Input Voltage		320		420	VDC
I_I	Input Current				0.5	A
V_{CC}	Bias supply voltage		11.5		16	V
I_{CC}	Bias supply current	Output enabled		20		mA
OUTPUT CHARACTERSTICS						
V_O	Output Voltage		19.2	19.5	19.8 (1)	V
I_O	Output Current		1 (2)		4.6	A
P_O	Output Power				90	W
I_{LIM}	Current Limit	ΔV_O = -2 V		6		A
ΔV_{LOAD}	Load Regulation	V_I =390 V		0.05		$\%V_O$
ΔV_{LINE}	Line Regulation	I_O =3 A		0.1		
V_O(ripple)	Output Voltage Ripple	V_I =390 V, I_O =3 A		150		mV_{PP}
SYSTEM CHARACTERSTICS						
η	Efficiency	V_I =390 V, I_O =3 A		94		%
	Overall thickness (3)				18	mm
	Temp. Range	Nat'l Conv. airflow	0		50	°C

(1) Equivalent to an output voltage tolerance of ±1.5%.

(2) Operates at no load with reduced regulation and burst mode operation.

(3) Excludes terminal blocks for power input and output connections.

4 BACKGROUND

4.1 LLC Series-Resonant Topology

Figure 1 shows the topology of this LLC series-resonant converter. The input is powered from a high-voltage DC source. This is normally the regulated output of the boost PFC pre-regulator. The circuit comprises of a ½-bridge power stage (Q1, Q2), which is connected to the series elements of an LLC resonant circuit. The LLC resonant circuit is formed by the series combination of the magnetizing inductance (L_M) and low-value leakage inductance of the main transformer (L_R), and the combined capacitance on the passive side of the bridge (C_R). The resonant frequency is set by the low-value leakage inductance of the main transformer (approx. 80 µH) and total bridge capacitance (0.02 µF). These values set the resonant frequency at approximately 123 kHz.

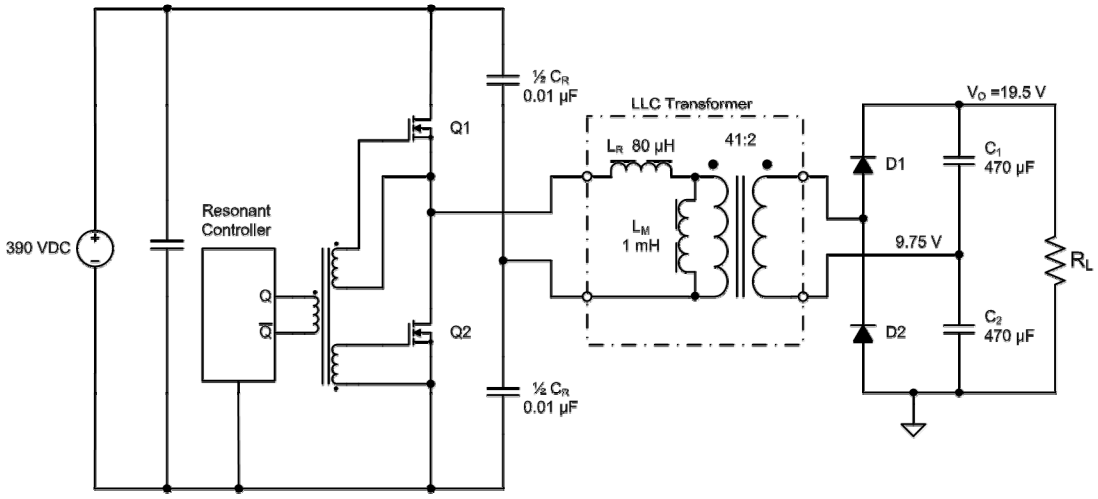

Figure 1 LLC Series-Resonant Converter

The ½-bridge power stage operates at a fixed 50% duty and varying frequency. At resonant frequency the voltages across the resonant components of the circuit cancel, allowing the full peak-peak voltage from the power stage to be applied across the transformer primary. This is the unity gain operating condition. By varying the frequency either below or above the circuit's resonance, the output voltage of the converter, can be increased or decreased respectively. The operating frequency is the control parameter that regulates the output of a resonant converter.

In this design the resonant inductor is integrated into the main transformer as a leakage component. The magnetizing inductance (L_M) also affects the gain of the circuit versus frequency and plays an important role in limiting the switching losses of the MOSFET drivers. Energy stored in the magnetizing inductance forces current to circulate during the short period when both MOSFET switches are 'off'. The phase of this current has the effect of reducing the voltage across each MOSFET prior to it turning on. This is referred to as zero-voltage switching (ZVS). ZVS improves efficiency by reducing the switching losses of the converter. It also reduces the electrical noise produced by the circuit compared to the rapid collapse of the MOSFET drain voltage with normal switching.

4.2 Secondary Rectifier Configuration

LLC converters generally use a center-tapped transformer secondary winding with two rectifiers; one at each end of the winding. This allows the rectifiers and each half winding to share the load current by conducting alternate half cycles. However the rectifiers must be rated at more than 2× the output voltage.

To limit the peak voltage to the VD pin of the UCC24610 SR controller, the rectifiers in this design are stacked in a voltage doubling arrangement. This reduces the voltage seen by each rectifier to 1× the output voltage, allowing MOSFETS with a lower V_{DS} (max) and on resistance to be used. It also eliminates the requirement for a center tap on the main transformer secondary winding, reducing manufacturing cost. However there are compromises. Both rectifiers are now required to conduct the full load current. This doubles the peak current in the secondary winding, which must now pass current in both half cycles. The combination of twice the current magnitude and full-cycle conduction increases the rms current in the secondary winding by a factor of $2 \times \sqrt{2}$. Secondly the rectifiers no longer share a common anode, requiring the control circuit for the upper rectifier (D1 in Figure 2) to float on the ac-voltage end of the transformer secondary winding. This is the switch node between the two rectifiers.

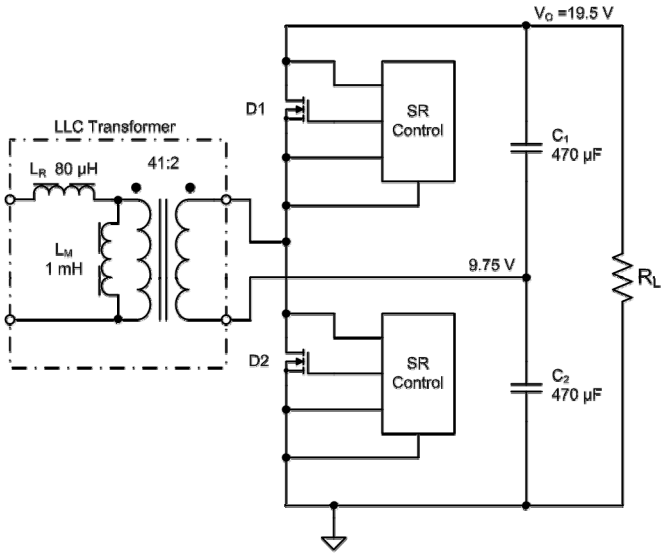

Figure 2 Voltage-Doubling Rectifier Circuit with Synchronously Switched MOSFETs

5 SCHEMATICS AND CIRCUIT DESCRIPTION

The schematics provided in this section are for reference only. For the purposes of clarity some of the detailed component parameters are not shown. Consult the list of materials for additional information.

Three versions of the schematic are presented. The choice depends on the desired synchronization method for turning the UCC24610 SR controllers off, using the gate-drive signals from the primary side of the converter. The synchronization configurations are described in detail in the section 5.2, Secondary-Side Synchronous Rectifier Circuit. The primary circuit and feedback control is the same for all three synchronization methods. The following description refers to Figure 3, Figure 4, and Figure 5.

5.1 Primary Circuit and Feedback Control

The half-bridge power stage is comprised of the MOSFETs Q1, Q2. These are controlled by the UCC25600 via an isolated gate drive, T2. The UCC25600 is a very simple and low-cost part to use. In addition to providing a variable drive frequency for the ½-bridge power stage, it includes a soft-start feature, over-current shutdown protection, and adjustment of the switch dead time between Q1 and Q2.

Load current is sensed through the resonant capacitance using a parallel 0.001-µF capacitor to ground (C7). This capacitor is in parallel with the 0.02-µF of resonant capacitance (C5+C6) to form a 1:21 impedance divider. Current through C7 is half-wave rectified (D3) and then passed through a sense resistor (R19). The resulting signal is then filtered (R18 and C25) and fed to the OC pin (pin 3) of the UCC25600 (U1). This method of sensing current provides less variation in the sensed current versus the switching frequency.

The resonant current is susceptible to a high surge current during converter start-up. For this reason it is recommended that the sensitivity of the current sense circuit is reduced during converter start up. This circuit accomplishes this using a p-channel JFET (Q6) and a divider resistor (R20). The gate of the JFET is connected to the SS pin (pin 4) of the UCC25600, which is initially low during converter start up. The JFET places the divider resistor in circuit during the period that its gate voltage is low. When the soft-start period is complete the rising gate voltage to the JFET pinches off its channel. This isolates the divider resistor and returns the current sense gain to normal.

A limitation of LLC series-resonant converters is that they operate over a limited input voltage range. This is because below a certain operating frequency the frequency-gain relationship of the converter is reversed. The operating frequency of the UCC25600 is controlled by the magnitude of current flowing from the RT pin (pin 2). A resistor to ground, R22, sets the minimum operating frequency to approximately 70 kHz.

To help limit the surge current during start-up the UCC25600 incorporates a soft-start feature. The maximum control frequency is set by R23. The value of this resistor sets the maximum frequency of the UCC25600 above 360 kHz. Above 360 kHz the device will enter burst-mode in order to maintain control of the output at light loads.

The converter output voltage is regulated by a TL431A shunt regulator (U7) located in the secondary. The error signal generated from the TL431A is passed back to the converter primary using a coupler (U6). A decrease in the voltage at the output of the coupler increases the current pulled from RC pin (pin 2) of the UCC25600. This increases the switching frequency of the converter to reduce its gain and output voltage.

5.2 Secondary-Side Synchronous Rectifier Circuit

The control circuit for the two synchronous rectifiers (SRs) in the secondary is identical. The only difference is the method by which the circuits are powered. The upper SR circuit formed by U2, U4, Q3 and C19 effectively sits on top of the lower SR circuit formed by U3, U5, Q4, and C20. The voltage developed across each circuit's capacitor (C19 and C20) is approximately 9.75 VDC, producing a total of 19.5 VDC across both capacitors. The supply voltage to each UCC24610 controller (U4, U5) is tightly regulated to 5 VDC by a low-cost linear regulator (U2, U3).

The lower SR circuit is referenced to secondary ground (SECGND) and can be powered directly from the steady-state 9.75 VDC produced across C20. However the upper SR circuit floats on the 10 VAC produced at one end of the transformer secondary winding. The voltage at this node swings approximately ±10 V with respect to the junction of C19 and C20, requiring the upper circuit to be powered using the bootstrap diode (D1). During operation

the upper SR circuit common swings 10 V below the C19/C20 junction, allowing D1 to charge the capacitor (C9) at the input to the linear regulator, U2.

It is important that the SR FETs turn off correctly without any conduction overlap. This is especially when the rate of change in voltage (dv/dt) produced across secondary winding is high. The reference circuit offers two methods for synchronizing the turn off of the UCC24610 SR controllers using a gate-drive signal on the primary side of the converter.

5.2.1 Self-Synchronization Configuration

Figure 3 shows the schematic for the "self-synchronizing"' circuit configuration. This synchronization method has the minimum component count but relies on the UCC24610 SR controllers to turn themselves off after sensing that the FET drain current has decayed. The method is made possible by the device's ability to sense milli-volts of voltage drop across the FET. Each FET must turn off prior to the reversal in the main transformer secondary voltage. Otherwise the transformer output is shorted. The most vulnerable condition occurs when the converter is operating at a frequency well above resonance at relatively high input voltages; 390-420 VDC. Above resonance the primary current is interrupted prior to completing the resonant half-cycle and drops dramatically. The rate of decay is limited only be the relatively low resonant inductance provided by the transformer's leakage. The ability for the SR controllers to turn off in a timely manner is conditional on a moderate rate of decay of the resonant current.

5.2.2 Pulse Transformer Synchronization

One reliable method of passing synchronization signals between the primary and secondary circuit is with a small pulse transformer. Not only are the primary and secondary circuits isolated, but the zero-volt reference to the upper SR FET and control circuit (Q3, U4) floats on a switch node. This switch node is stepped up and down by 10 V with respect to the primary and secondary ground at the switch frequency of the converter.

The schematic for this method is detailed in Figure , and the additional components are listed in Table 3. They include the pulse transformer, T3. The external pull-up resistors, R32 and R33 are added to dampen oscillations from each primary transition due to the pulse transformer's leakage inductance.

5.2.3 Synchronization Using 'Y' Type Safety-Rated Capacitors

Figure 5 shows how 'Y' type, safety-rated capacitors (C15, C16), can be used to provide synchronization signals to the UCC24610 SR controllers. This works fairly well but results in a shorter conduction period for the upper SR FET. As the 0-V reference for the upper SR-FET and controller (Q3, U4) floats on a switch node, a false negative pulse is produced due to the 0-V to the upper SR circuit rising sharply at the start of this rectifier's conduction period. This "false" pulse momentarily inhibits the upper SR controller from turning on its FET (Q3) by approximately 0.2 µs.

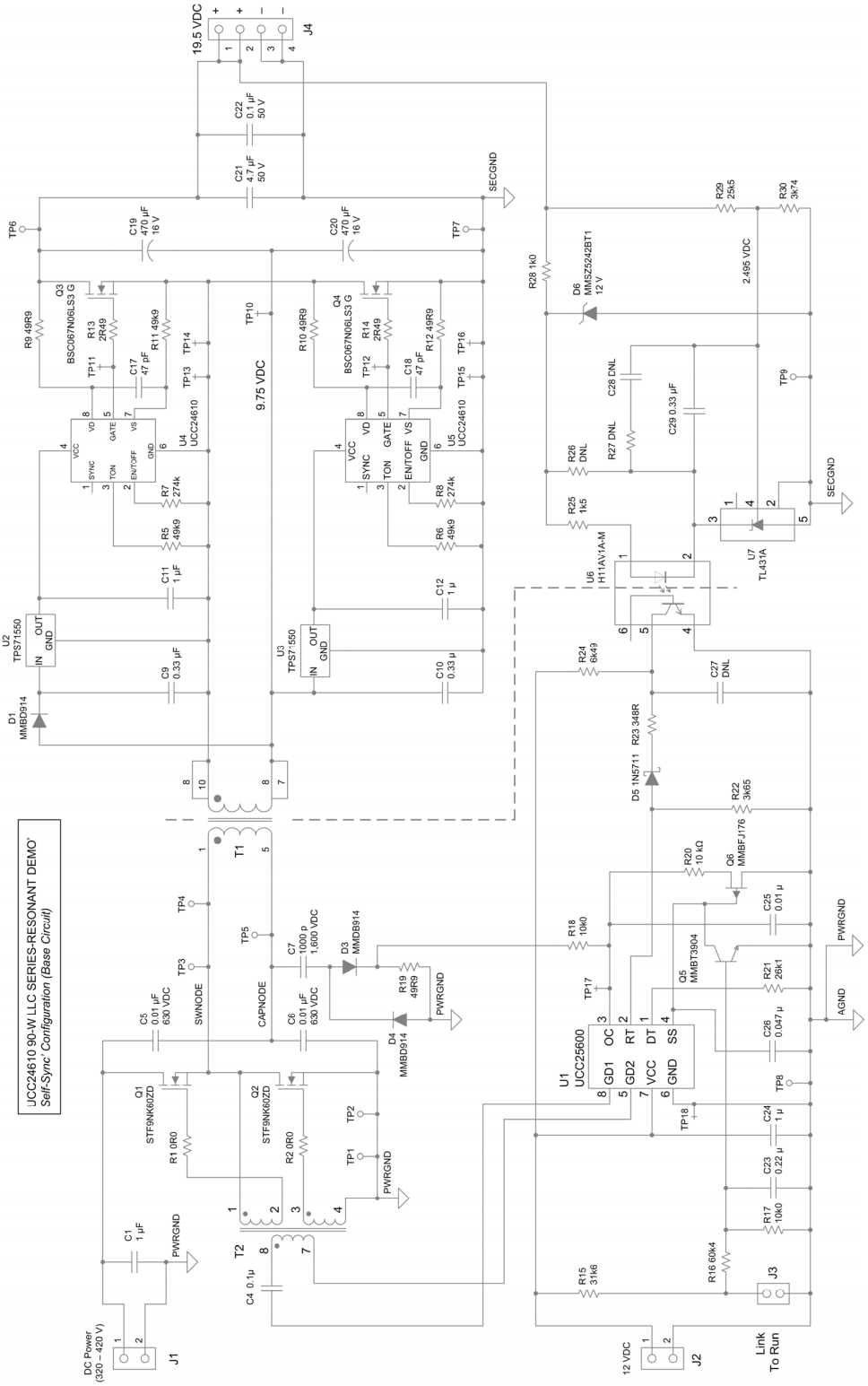

Figure 3 Schematic, UCC24610 LLC Series-Resonant Converter – Self Synchronization Configuration

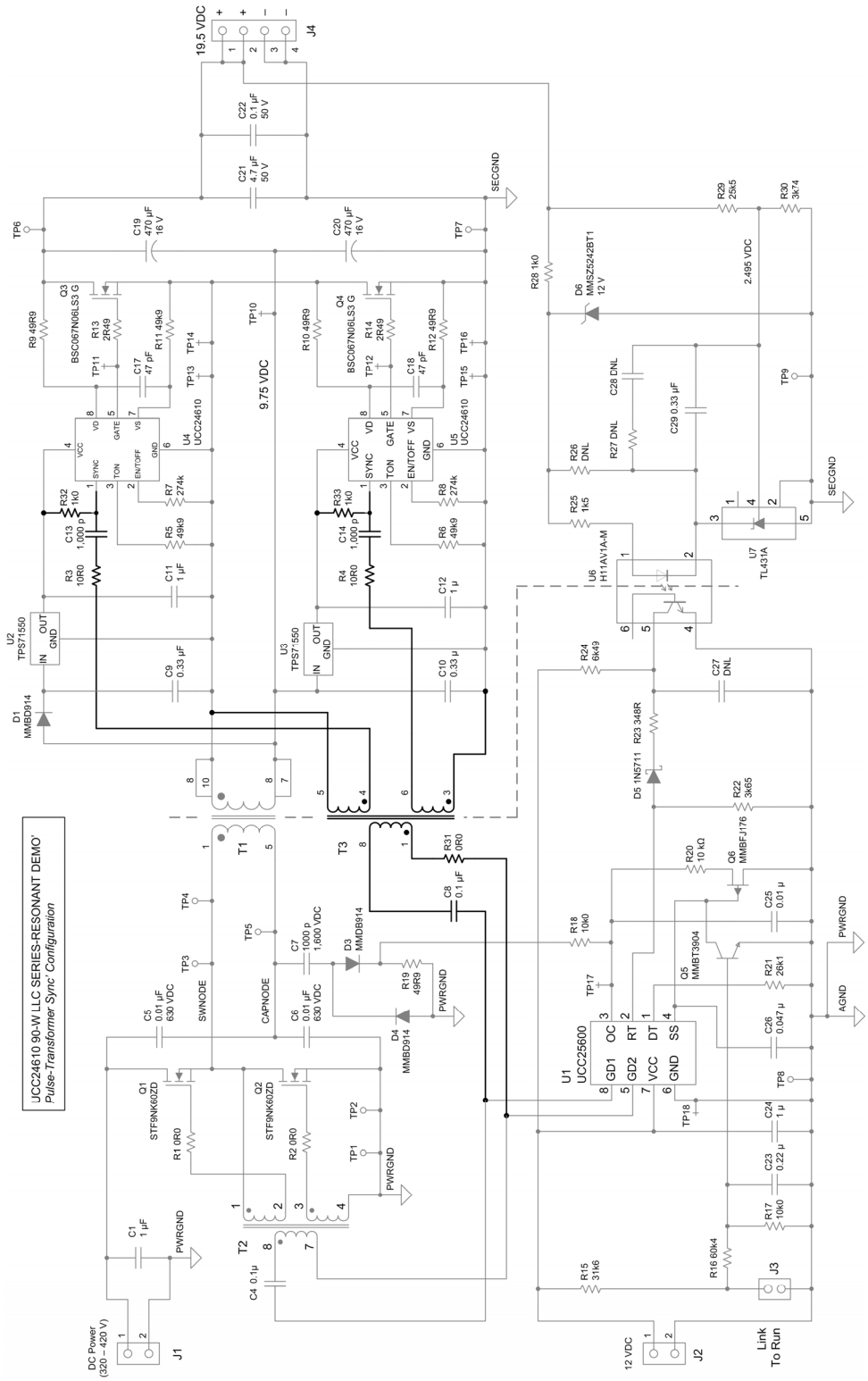

Figure 4 Schematic, UCC24610 LLC Series-Resonant Converter – Transformer Configuration

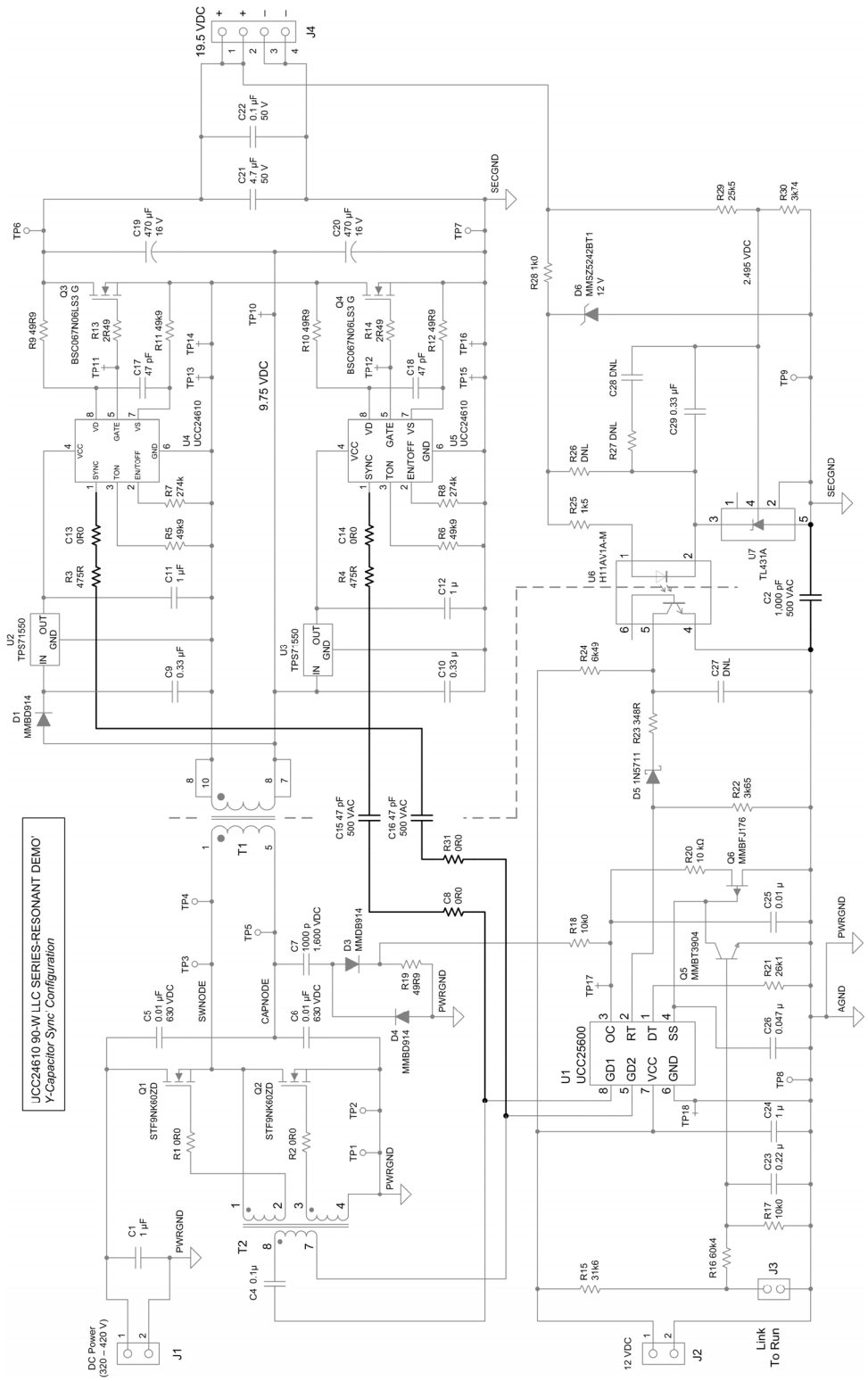

Figure 5 Schematic, UCC24610 LLC Series-Resonant Converter – Capacitor Configuration

6 LIST OF MATERIALS

The component list for the three build configurations described herein is defined by combining the contents of up to two of the three tables in this section. Table 2 lists the components for the "self-synchronization" configuration. The self-synchronization configuration has the minimum component count and is common to all three configurations. For this reason it is defined as the *base circuit* for the "Transformer Synchronization" and "Capacitor Synchronization" configurations. The following summary identifies the material list for each configuration.

1. Self-Synchronization: Use only Table 2
2. Transformer Synchronization: Combine Table 2 with the changes outlined in Table 3.
3. Capacitor Synchronization: Combine Table 2 with the changes outlined in Table 4.

Table 2 Components for Self-Synchronization Configuration (Base Circuit)

Ref.	Value	Tol.	Description	Part Number	Manufacturer
C1	1.0 µF	10%	Capacitor, Film (PP), 630 V	B32674D6105K	EPCOS
C2	N/A		Not Fitted		
C4	0.1 µF	10%	Capacitor, MLC, 0805, 25 V	Generic	Multi-Sourced
C5	0.01 µF	5%	Capacitor, Film (PP), 630 V	B32621A6103J	EPCOS
C6	0.01 µF	5%	Capacitor, Film (PP), 630 V	B32621A6103J	EPCOS
C7	0.001 µF	10%	Capacitor, Film, (PP), 1600 V	MKP10 1000/1600/10	WIMA
C8	N/A		Not Fitted		
C9	0.33 µF	20%	Capacitor, MLC, 0805, 50 V	Generic	Multi-Sourced
C10	0.33 µF	20%	Capacitor, MLC, 0805, 50 V	Generic	Multi-Sourced
C11	1 µF	10%	Capacitor, MLC, 0805, 16 V	Generic	Multi-Sourced
C12	1 µF	10%	Capacitor, MLC, 0805, 16 V	Generic	Multi-Sourced
C13	N/A		Not Fitted		
C14	N/A		Not Fitted		
C15	N/A		Not Fitted		
C16	N/A		Not Fitted		
C17	47 pF	5%	Capacitor, MLC, 0603, 50 V	Generic	Multi-Sourced
C18	47 pF	5%	Capacitor, MLC, 0603, 50 V	Generic	Multi-Sourced
C19	470 µF	20%	Capacitor, Electrolytic, 16 V	ORZ471M1CSA-10127S	Surge Components Inc.
C20	470 µF	20%	Capacitor, Electrolytic, 16 V	ORZ471M1CSA-10127S	Surge Components Inc.
C21	4.7 µF	20%	Capacitor, MLC, 1210, 50 V	Generic	Multi-Sourced
C22	0.1 µF	20%	Capacitor, MLC, 1206, 50 V	Generic	Multi-Sourced
C23	0.22 µF	10%	Capacitor, MLC, 0603, 10 V	Generic	Multi-Sourced
C24	1 µF	10%	Capacitor, MLC, 0805, 16 V	Generic	Multi-Sourced
C25	0.01 µF	10%	Capacitor, MLC, 0603, 50 V	Generic	Multi-Sourced
C26	0.047 µF	10%	Capacitor, MLC, 0603, 25 V	Generic	Multi-Sourced
C27	N/A		Not Fitted		
C28	N/A		Not Fitted		
C29	0.33 µF	5%	Capacitor, MLC, 0805, 50 V	Generic	Multi-Sourced

Ref.	Value	Tol.	Description	Part Number	Manufacturer
D1			Diode, Switching, 100 V, 200 mA	MMBD914	Multi-Sourced
D3			Diode, Switching, 100 V, 200 mA	MMBD914	Multi-Sourced
D4			Diode, Switching, 100 V, 200 mA	MMBD914	Multi-Sourced
D5			Diode, Schottky, 70 V, 15 mA	1N5711	ST Microelectronics
D6			Diode, Zener, 0.5-W, 12 V	MMSZ5242BT1	ON Semiconductor
J1			Term Block, Eurostyle, 3-Way	39390-0103	Molex
J2			Terminal Block, 2-Way	ED120/2DS	On-Shore Technology
J3			Header, 0.025 Sq., 2-Way	68001-203HLF	FCI BergStik
J4			Terminal Block, 4-Way	ED120/4DS	On Shore Technology
Q1			N-MOSFET, TO-220, 600 V, 7 A	STF9NK60ZD	ST Microelectronics
Q2			N-MOSFET, TO-220, 600 V, 7 A	STF9NK60ZD	ST Microelectronics
Q3			N-MOSFET, LF-PACK, 60 V, 50 A	BSC067N06LS3 G	Infineon
Q4			N-MOSFET, LF-PACK, 60 V, 50 A	BSC067N06LS3 G	Infineon
Q5			TRANSISTOR, NPN, 40 V, 200 mA	MMBT3904	Multi-Sourced
Q6			JFET, P-CHL, 30 V, 50 mA	MMBFJ176	Fairchild
R1	15R0	1%	Resistor, SMD, 0805	Generic	Multi-Sourced
R2	15R0	1%	Resistor, SMD, 0805	Generic	Multi-Sourced
R3	N/A		Not Fitted		
R4	N/A		Not Fitted		
R5	49k9	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R6	49k9	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R7	274k	1%	Resistor, SMD, 0603	RK73H1JTTD2743F	KOA
R8	274k	1%	Resistor, SMD, 0603	RK73H1JTTD2743F	KOA
R9	49R9	1%	Resistor, SMD, 0805	RK73H2ATTD49R9F	KOA
R10	49R9	1%	Resistor, SMD, 0805	RK73H2ATTD49R9F	KOA
R11	49R9	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R12	49R9	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R13	2R49	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R14	2R49	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R15	31k6	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R16	60k4	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R17	10k	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R18	10k	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R19	49R9	1%	Resistor, SMD, 0805	RK73H2ATTD49R9F	KOA
R20	10k	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R21	26k1	1%	Resistor, SMD, 0603	RK73H1JTTD2612F	
R22	3k65	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R23	348R	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R24	6k49	1%	Resistor, SMD, 0603	Generic	Multi-Sourced

Ref.	Value	Tol.	Description	Part Number	Manufacturer
R25	1k5	1%	Resistor, SMD, 0805	Generic	Multi-Sourced
R26	DNL	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R27	N/A		Not Fitted		
R28	1k	1%	Resistor, T/H, 0.25 W	271-1K/AP-RC	Xicon
R29	25k5	1%	Resistor, SMD, 0805	Generic	Multi-Sourced
R30	3k74	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R31	N/A		Not Fitted		
R32	N/A		Not Fitted		
R33	N/A		Not Fitted		
T1			LLC Power Transformer	YS01361903	Taiwan Transmore Elect.
T2			Transformer, Gate Drive, 1:1:1	HA3858-AL	Coilcraft
T3	N/A		Not Fitted		
TP1			Test Point, Loop w/ Insulator	5012	Keystone
TP2			Test Point, Loop w/ Insulator	5012	Keystone
TP3			Test Point, Loop w/ Insulator	5012	Keystone
TP4			Test Point, Loop w/ Insulator	5012	Keystone
TP5			Test Point, Loop w/ Insulator	5012	Keystone
TP6			Test Point, Loop w/ Insulator	5012	Keystone
TP7			Test Point, Loop w/ Insulator	5012	Keystone
TP8			Test Point, Loop w/ Insulator	5012	Keystone
TP9			Test Point, Loop w/ Insulator	5012	Keystone
U1			Resonant-Mode Controller	UCC25600D	Texas Instruments
U2			Linear Regulator	TPS71550DCKR	Texas Instruments
U3			Linear Regulator	TPS71550DCKR	Texas Instruments
U4			SR Controller	UCC24610D	Texas Instruments
U5			SR Controller	UCC24610D	Texas Instruments
U6			Opto-Coupler	H11AV1A-M	Fairchild
U7		1%	Shunt Regulator, 2.495 V	TL431AIDBV	Texas Instruments
Q1, Q2			Heat Sink, Low-Profile, TO-220	274-1AB	Wakefield
Q1, Q2			Screw, Panhead, #4-40 x 3/8	#4-40 x 3/8	Fastener Supply
Q1, Q2			Nut, Stainless Steel, #4-40	#4-40	Fastener Supply

Table 3 Component Changes for Transformer Synchronization Configuration

Ref.	Value	Tol.	Description	Part Number	Manufacturer
C2	N/A		Not Fitted		
C8	0.1 µF	10%	Capacitor, MLC, 0805, 25 V	Generic	Multi-Sourced
C13	1000 pF	10%	Capacitor, MLC, 0603, 50 V	Generic	Multi-Sourced
C14	1000 pF	10%	Capacitor, MLC, 0603, 50 V	Generic	Multi-Sourced
C15	N/A		Not Fitted		
C16	N/A		Not Fitted		
R3	10R0	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R4	10R0	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R31	0R0		Link, SMD, 0805	Generic	Multi-Sourced
R32	1k	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R33	1k	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
T3			Pulse Transformer (2:1:1), SMD	PA2008NL	Pulse

Table 4 Component Changes for Capacitor Synchronization Configuration

Ref.	Value	Tol.	Description	Part Number	Manufacturer
C2	1,000 pF	20%	Capacitor, Ceramic T/H, 500 VAC	VY1102M35Y5UQ63V0	Vishay-BCcomponents
C8	0R0		Link, SMD, 0805	Generic	Multi-Sourced
C13	0R0		Link, SMD, 0603	Generic	Multi-Sourced
C14	0R0		Link, SMD, 0603	Generic	Multi-Sourced
C15	47 pF	10%	Capacitor, Ceramic T/H, 500 VAC	VY1470K31Y5SQ63V0	Vishay-BCcomponents
C16	47 pF	10%	Capacitor, Ceramic T/H, 500 VAC	VY1470K31Y5SQ63V0	Vishay-BCcomponents
R3	475R	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R4	475R	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R31	0R0		Link, SMD, 0805	Generic	Multi-Sourced
R32	N/A		Not Fitted		
R33	N/A		Not Fitted		
T3	N/A		Not Fitted		

7 PCB DESIGN

7.1 General

Figure 6 and Figure 7 show the component placement and copper routing of the printed circuit board (PCB) used to test and characterize this design. The PCB design is based on a double-sided 2-oz. copper-foil layout. A double-sided PCB provides the flexibility to optimize the layout of the SR FETs and control circuitry. A combination of both through-hole (T/H) and surface mount devices (SMD) were placed on the top side, and SMD parts on the foil side.

7.2 Grounding

High-frequency transient current associated with switched-power converters induce differential noise voltages in the ground system. Any voltage differential in the ground can cause spurious operation of the control circuits. The design dedicates large areas of copper to power ground (PWRGND) and analog ground (AGND). PWRGND provides the return path for the power circuitry on the primary side of the converter. AGND is used by the control circuits as the primary-side zero-volt reference. To prevent the AGND from being used as current path by high-frequency power signals, AGND is referenced to PWRGND at just one location. This single-point grounding technique forces the high-frequency ground currents generated by the power circuitry to be directed around (as opposed to through) the quiet ground area of the sensitive control circuits.

It is important to keep the ground connections contiguous. Ground connections should take priority over the routing of other signals. Where necessary, use vias and T/H components to pass signals to other areas of the board. These techniques minimize the impedance to high-frequency ground currents to ensure low-noise and reliable operation.

7.3 Creepage and Clearance

Both the component placement and spacing between the copper areas or the PCB were designed to comply with the creepage and clearance requirements defined in the UL 60950 safety standard. The board was designed to meet the requirements for functional isolation for the high-voltage nodes on the primary (ac-line) side of the power supply, and reinforced isolation between all primary and secondary circuits. To comply with the UL standard 4 mm of separation was used for the primary-side high-voltage traces, and 8 mm between all primary and secondary side traces. The default trace separation for low-voltage nodes, as used for control circuits, was 0.3 mm.

7.4 Thermal Considerations

Although this circuit and topology operates with high efficiency, some components on the PCB assembly dissipate a moderate amount of heat. This may require thermal management initiatives to be implemented when the converter operates in an enclosure. A thermally conductive path to the surfaces of the enclosure may be required for these components. Table 5 provides a list of the components that have significant heat dissipation.

Table 5 Parts with High Thermal Dissipation

Reference Designator	Description	Dissipation (1)/
Q3, Q4	Secondary SR FETs	1 W
T1	LLC converter transformer	3 W

(1) Estimated dissipation at maximum load and 390 V input voltage.

7.5 Board Layout

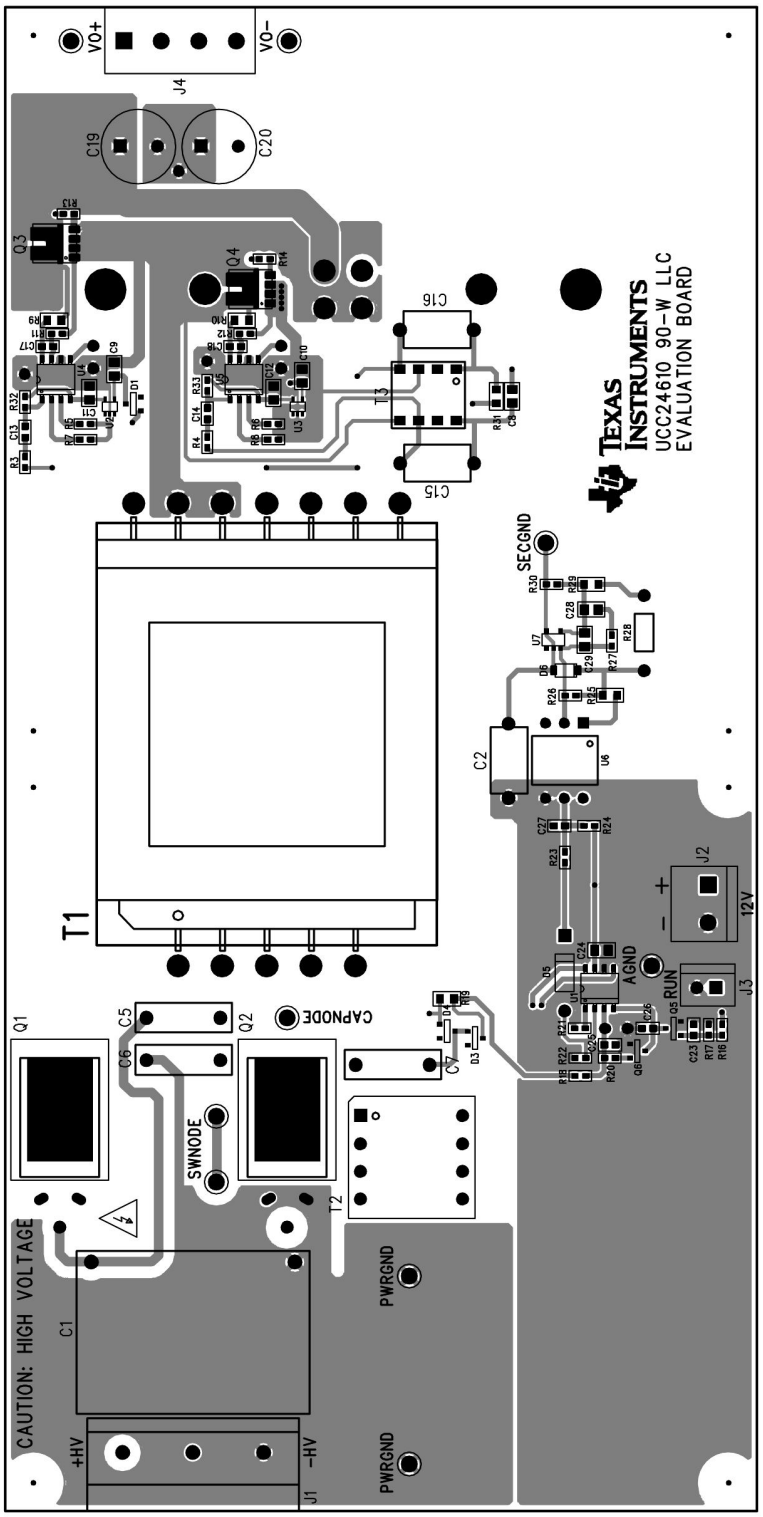

Figure 6 PCB Layout; Component-Side View

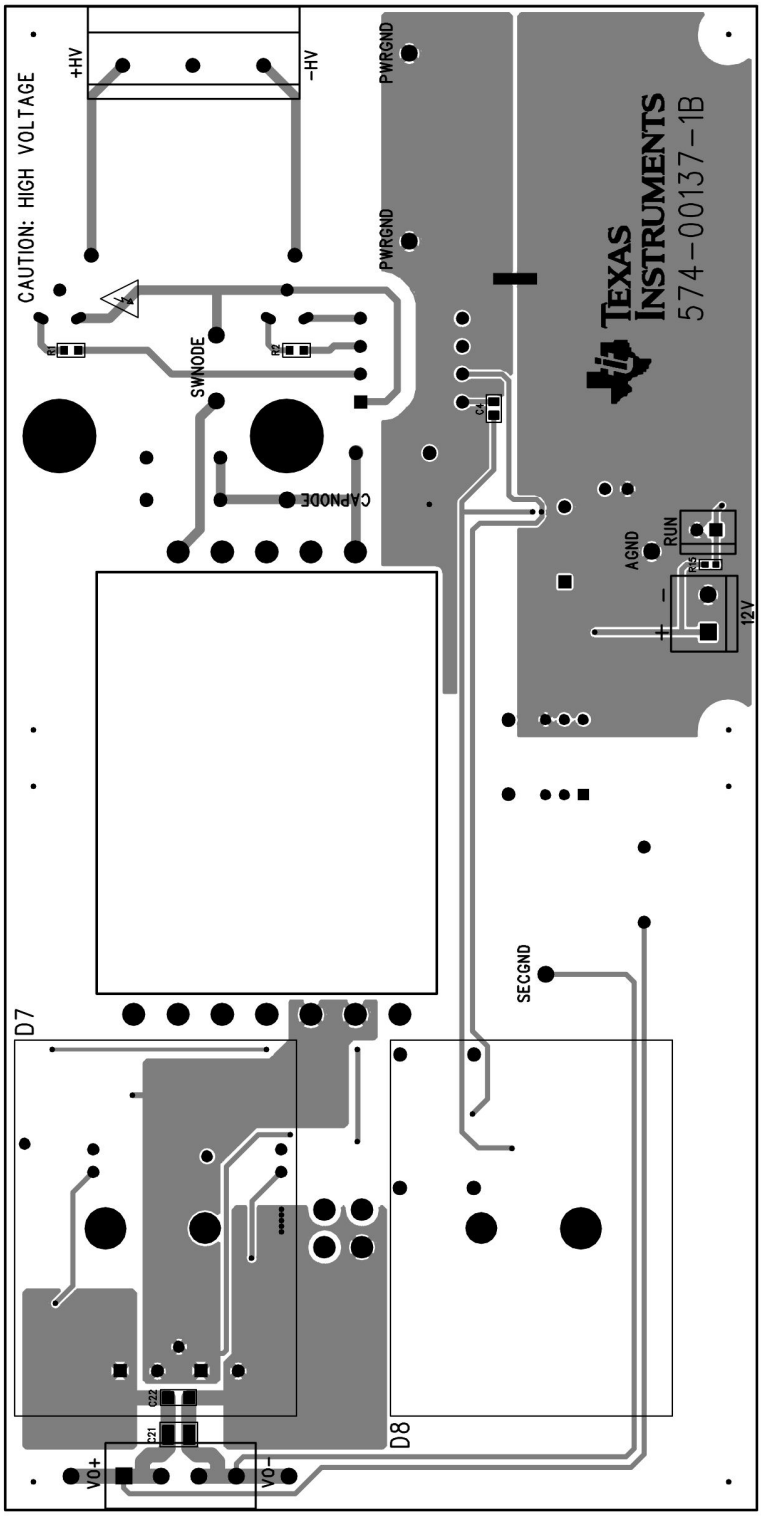

Figure 7 PCB Layout; Foil-Side View

7.6 Power Inputs

7.6.1 HVDC Input

The power input to the circuit requires a high-voltage DC source, capable of supplying up to 420 VDC at 0.5 A max. This can be provided by a high-voltage adjustable bench supply, the output from a boost PFC circuit, or the rectified output from a 0–280 V, 1-kVA rated power rheostat. Ensure that the source is either current limited or is fitted with a fuse with a rating of no more than 1 A.

The HVDC power can be safely applied without the bias supply being present.

7.6.2 Bias Supply

A bias supply of 12–16 VDC at 50 mA is required to operate the converter. The bias power is applied to the J2 terminal block and can be supplied from a small adjustable bench supply or 12-V lamp battery. The current consumption is typically 20 mA when the converter is operating. The polarity is correct when the negative connection is closest to the J3 connector.

7.7 J3 Header

The PCB design includes a 0.1-in spaced pin header, J3. This header provides on/off control of the converter when both HVDC input and bias power is applied. This interface can be used to hold down the SS pin (pin 4) until there is sufficient output voltage for the converter to produce a regulated output. The converter runs only when the open-circuit voltage at pin 1 of J3 is pulled to GND (J3/Pin 2) using either a jumper or NPN bipolar transistor.

Place a standard 2-pin shorting jumper at J3 to enable the converter to run and produce a DC output. When the converter is enabled the UCC25600 resonant controller initiates a soft start. Removal of the J3 jumper promptly shuts down the converter.

The application and removal of the bias supply has the same effect as the removal and replacement of the shorting jumper at J3.

7.8 Monitoring Primary Current

By making a small modification to the PCB the primary current can be monitored using a current probe. This is also the current flowing between the series-resonant components, L_R and C_R.

The PCB layout in Figure 6 shows two test points labeled “SWNODE” located close to and just above the primary switch, Q2. They are identified TP3 and TP4 on the schematic. The 0.05-in trace connecting these two test points carries the transformer primary current. This trace can easily be cut, and replaced with a loop of wire connecting TP3 and TP4. The primary current can then be measured using a clip-on current probe.

8 PERFORMANCE VERSUS SCHOTTKY RECTIFIERS

Figure 8 through Figure 13 compares the typical performance of the 90-W LLC series-resonant converter, when operating with the UCC24610 synchronous rectifier controller versus regular Schottky rectifiers. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

8.1 Typical Operating Efficiency

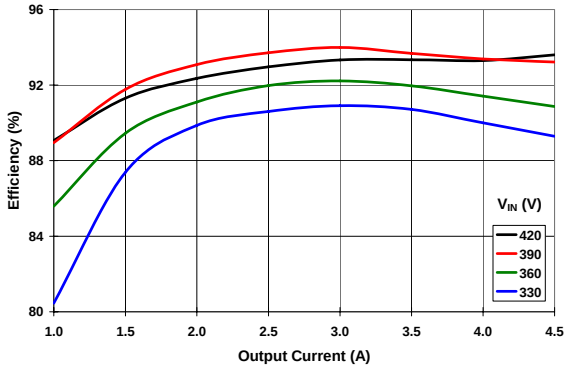

Figure 8 Operating Efficiency with UCC24610 Rectifier Controllers and FETs

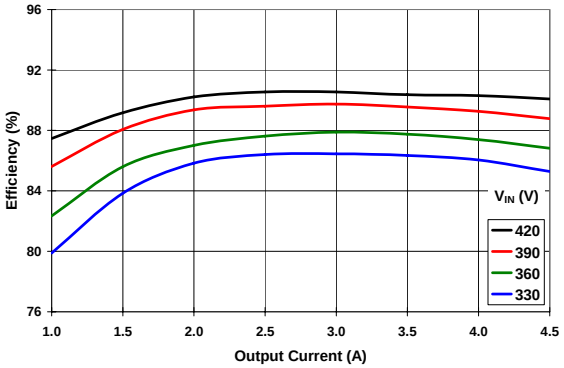

Figure 9 Operating Efficiency with MBR1645 Schottky Rectifiers

8.2 Typical Power Dissipation

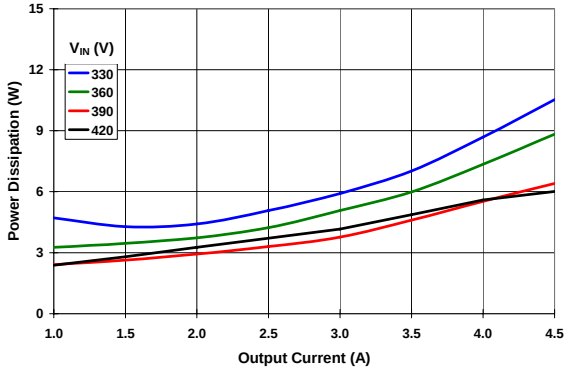

Figure 10 Power Dissipation with UCC24610 Rectifier Controllers and FETs (1)

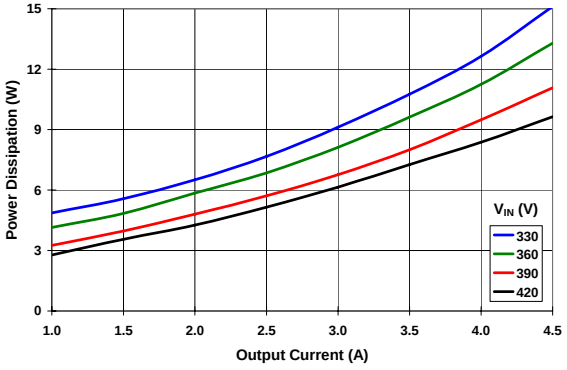

Figure 11 Power Dissipation with MBR1645 Schottky Rectifiers (1)

(1) When operating at 390-V input and at 3-A load, the converter dissipates 3.75 W using the UCC24610 rectifier controllers and FETs, compared to 6.75 W using regular Schottky rectifiers.

8.3 Typical Output AC Ripple Voltage

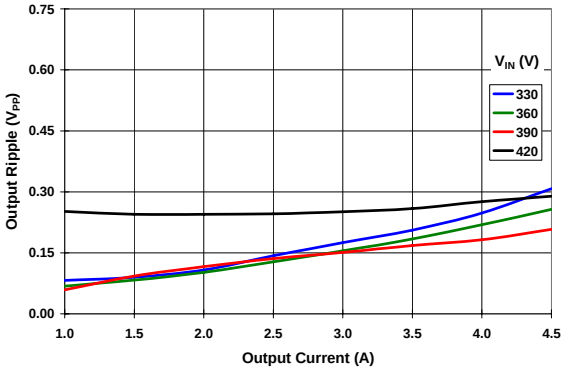

Figure 12 Output AC-Ripple with UCC24610 Rectifier Controllers and FETs (2)

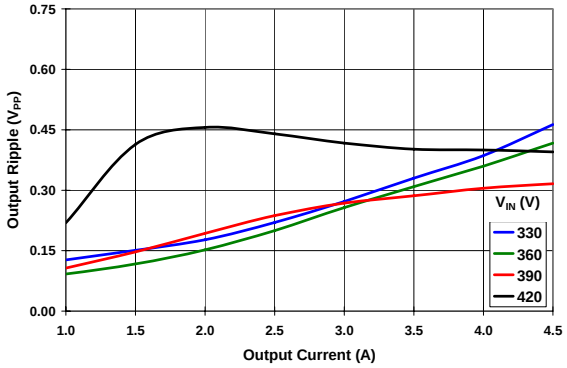

Figure 13 Output AC-Ripple with MBR1645 Schottky Rectifiers (2), (3)

(2) Peak-to-peak output ripple derived from V_{OUT} rms measurement using an oscilloscope with 20-MHz bandwidth limit.

(3) The Schottky diode rectifiers show a higher magnitude of ac rippled at high input voltage (420 V). This is due to an increase in high-frequency ringing from these devices at this input voltage.

9 CIRCUIT WAVEFORMS

The oscilloscope waveforms in this section, captured in Figure 14 through Figure 29, can be identified using the same color for source identification. The color key to the signals is provided in Table 6.

Table 6 Color Key for Oscilloscope Waveforms

Trace Color	Signal Description
Black	Main transformer secondary winding output voltage
Blue	Main transformer primary current
Green	Upper SR GATE signal waveform (U4/pin 5)
Brown	Upper SR SYNC signal waveform (U4/pin 1)
Red	Lower SR GATE signal waveform (U5/pin 5)
Orange	Lower SR SYNC signal waveform (U5/pin 1)

9.1 SR Synchronization with Pulse Transformer

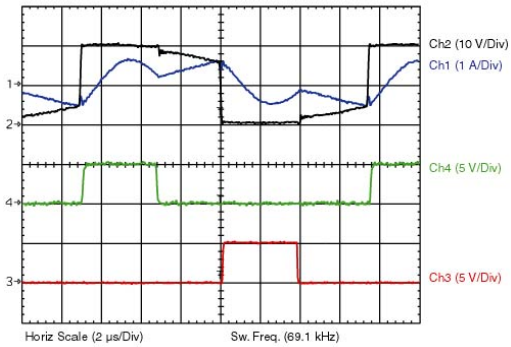

Figure 14 Upper and Lower SR Gate Signals at 320-VDC and 1-A Load ($f_{SW} < f_R$)

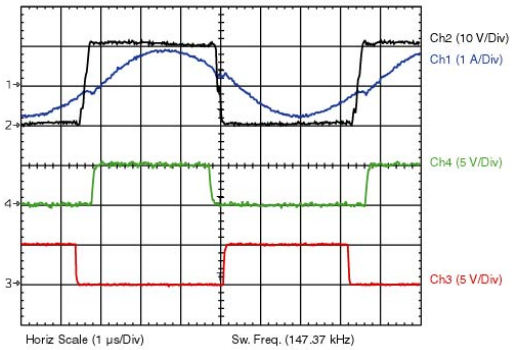

Figure 15 Upper and Lower Gate Signals at 400-VDC Input and 4.6-A Load ($f_{SW} \approx f_R$)

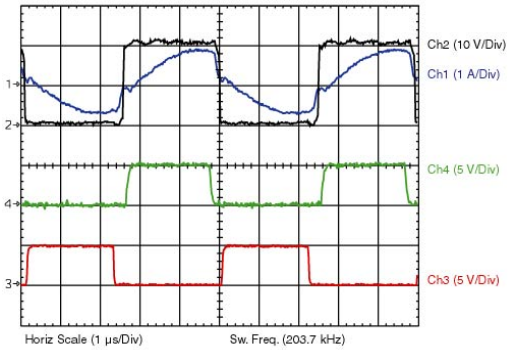

Figure 16 Upper and Lower SR Gate Signals at 420-VDC Input and 4.6-A Load ($f_{SW} > f_R$)

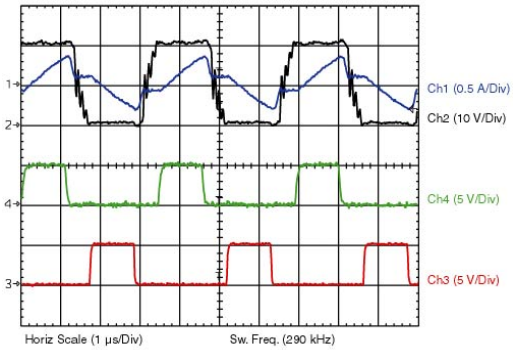

Figure 17 Upper and Lower SR Gate Signals at 420-VDC Input and 1-A Load ($f_{SW} > f_R$)

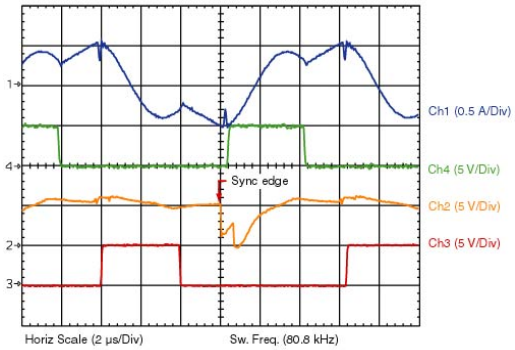

Figure 18 Upper/Lower SR Gate and Lower SYNC Signals at 340-VDC Input and 1-A Load (1)/

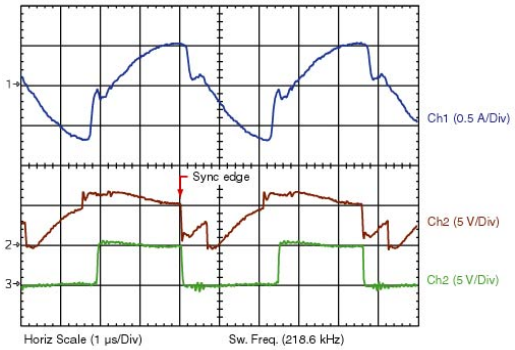

Figure 19 Upper SR Gate and SYNC Signals at 420-VDC and 3-A Load (2)/

(1) Below resonance the lower SR controller has set the gate signal (Red) low before the negative SYNC pulse (Orange).

(2) Above resonance the upper SR controller sets the gate signal (Green) low about the same time as the SYNC pulse (Brown). This forces the gate output low irrespective of whether the UCC24610 controller has sensed the FET is no longer conducting.

9.2 SR Synchronization with Capacitors

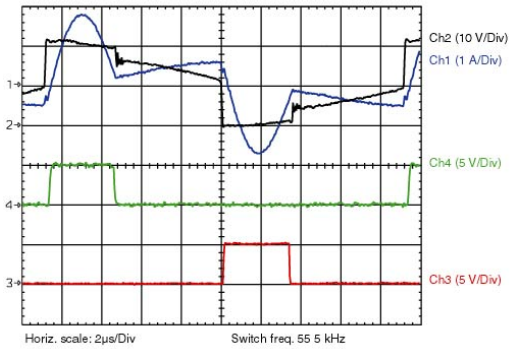

Figure 20 Upper and Lower SR Gate Signals at 320-VDC Input and 4.6-A Load ($f_{SW} < f_R$)

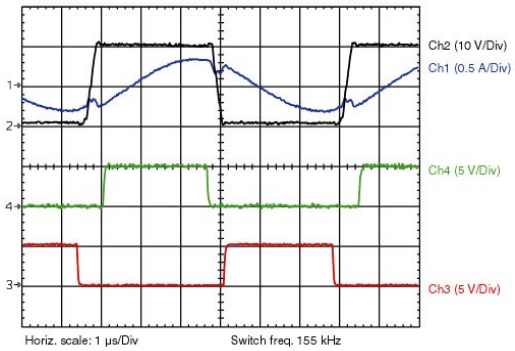

Figure 21 Upper and Lower Gate Signals at 390-VDC Input and 1-A Load ($f_{SW} \approx f_R$)

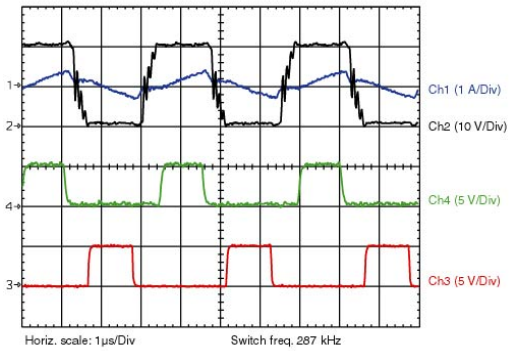

Figure 22 Upper and Lower SR Gate Signals at 420-VDC and 1-A Load ($f_{SW} > f_R$)

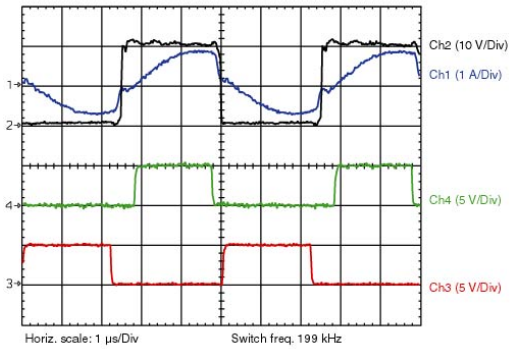

Figure 23 Upper and Lower SR Gate Signals at 420-VDC Input and 4.6-A Load ($f_{SW} > f_R$)

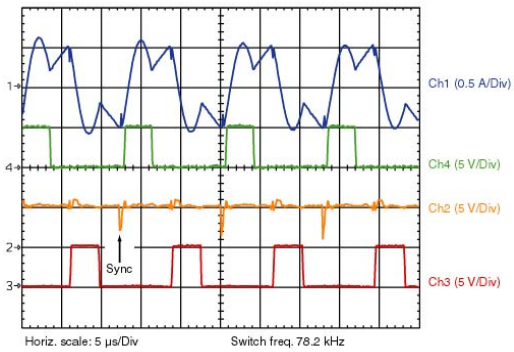

Figure 24 Upper/Lower SR Gate and Lower SYNC Signals at 340-VDC Input and 1-A Load (3)

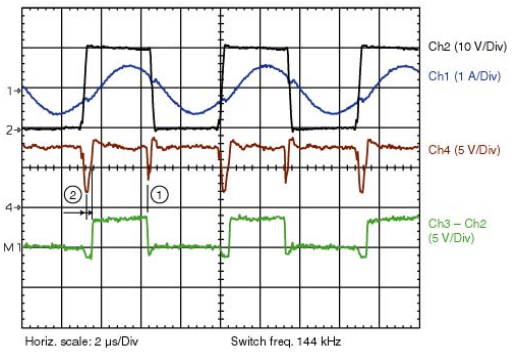

Figure 25 Upper SR Gate and SYNC Signals at 393-VDC Input and 3-A Load (4) ($f_{SW} \approx f_R$)

(3) The SYNC signal negative pulse for the lower SR circuit is generated by the high-to-low transition of the gate signal that drives the low-side MOSFET in the converter primary (U1/pin 8).

(4) Because the upper SR floats on the transformer secondary winding, it sees two negative pulses. The smaller, identified ①, is generated by the high-to-low transition of the gate signal that drives the high-side primary MOSFET (U1/pin 5). This is the edge that the controller should respond to. The larger, ②, is produced when the 0-V return of the circuit rises with the secondary winding voltage. The additional pulse delays (and thus shortens) the length of the gate signal from the upper controller by as much as 0.3 µs.

9.3 Self-Synchronization Configuration

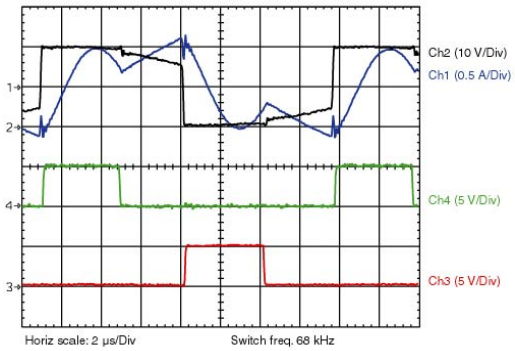

Figure 26 Upper and Lower SR Gate Signals at 320-VDC and 1-A Load

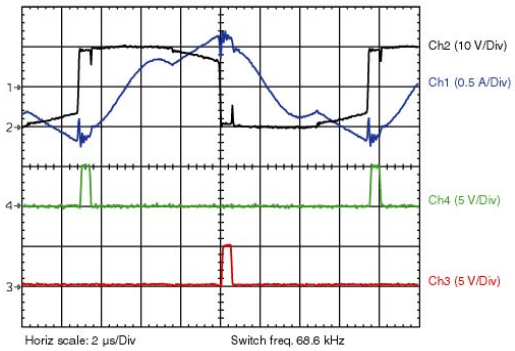

Figure 27 Upper and Lower SR Gate Signals at 340-VDC Input and 1-A Load (5)/

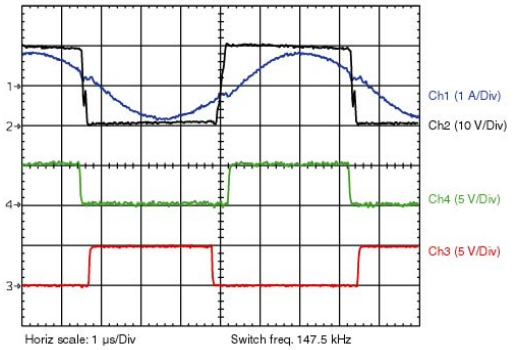

Figure 28 Upper and Lower SR Gate Signals at 400-VDC and 4.6-A Load

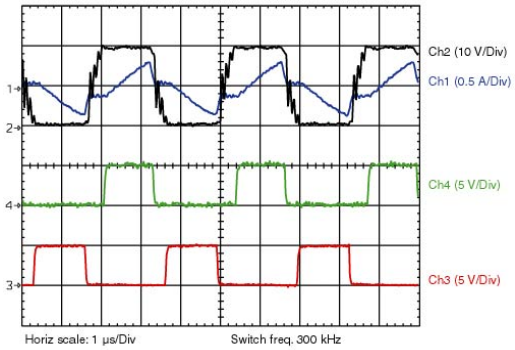

Figure 29 Upper and Lower SR Gate Signals at 420-VDC and 1-A Load

(5) Under the conditions of low input voltage and output load the drain-source voltage produced across the SR FETs does not always rise fast enough to keep each FET turned on. In this case the gate-drive outputs from both SR controllers (UCC24610) have turned off early, requiring the body diode of each FET to conduct for the rest of the cycle.

10 Performance Observations and Comments

The UCC24610 performs well in an LLC series-resonant converter application. This is especially when required to operate in a voltage-doubling rectifier configuration, which requires the upper SR circuit to float on the AC side of the transformer secondary winding.

The UC24610 is a single independent synchronous rectifier controller that includes features such as light-load management control. The threshold of this function is subject to both component tolerances and circuit variances. So when two devices are employed in either a center-tapped or voltage-doubling full-wave bridge rectifier they cannot make coordinated decisions. This was noted with all three circuit configurations; synchronization with a pulse transformer, capacitors, or without any synchronization (self-synchronization configuration).

There is always a risk of cross conduction when using two UCC24610 devices in a full-wave rectifier configuration. This risk is minimized, or even eliminated, when the devices are provided a synchronization signal. Synchronization prevents cross conduction by not only ensuring that an SR FET turns off at the end of its conduction period, but that it does not turn on at that point. The negative pulses at the UCC24610 SYNC pin occur just prior to the converter beginning its transition to the opposite half cycle. This has the effect of inhibiting the GATE output from each device at a point when it is subject to being turned on due to circuit noise generated during the phase transition.

Only when the SR circuits are operated *without* an external synchronization signal can cross conduction occur, and then only at low input voltages and load. The conduction overlap is extremely short (<10 ns) as reverse FET current is quickly detected by one of the SR controllers, which promptly turns off its gate drive. Series-resonant LLC converters also tend to be very robust as fault current is limited by the series-resonant inductance. Whenever cross-conduction occurred during testing of this design the over-current limit was promptly triggered. This allowed the converter to recover without any significant drop in the output voltage. The problem was eliminated by placing just 47 pF of capacitance across pins 7 and 8 of U4 and U5.

At zero loads the magnitude of current through the SR FETs can be sufficiently low that the SR controllers may periodically operate in either no-load mode or with the minimum t_{ON} gate period (0.5 µs). To maintain regulation the feedback control loop forces the converter frequency higher. The frequency is highest when the input voltage is also at a maximum (420 VDC). If the switch frequency rises above 350 kHz the UCC25600 can revert to burst-mode operation. This further helps keep the output voltage in regulation.

11 References

The following is a list of data sheets, evaluation guides, and papers that were used to design of the UCC24610 90-W LLC series-resonant converter.

[1] UCC24610 Data Sheet, Texas Instruments Ref. SLUSA87

[2] UCC25600 Data Sheet; Texas Instruments Ref. SLUS846

[3] TPS715xx Data Sheet, Texas Instruments Ref. SLVS338

[4] Bing Lu, Wenduo Liu,Yan Liang, Fred C. Lee, and Jacobus D. van Wyk, “Optimal Design Methodology for LLC Resonant Converter,” IEEE APEC 2006.

12 Additional Information

The PCB layout for this reference design was created using PADS version 9 CAD software by Mentor Graphics. PADS Logic was used for schematic capture, and PADS Layout was used to design the PCB. The Gerber file, silk screen, solder mask, and drill drawing files produced by PADS, including the program files that created them, are available to customers and designers. Enquiries should be made to the regional Texas Instruments Product Information Center (PIC), or a local TI sales representative. Use the prototype reference design number, PR2000, for this request.

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