Functional Safety Information

TPS4H160-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS4H160-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

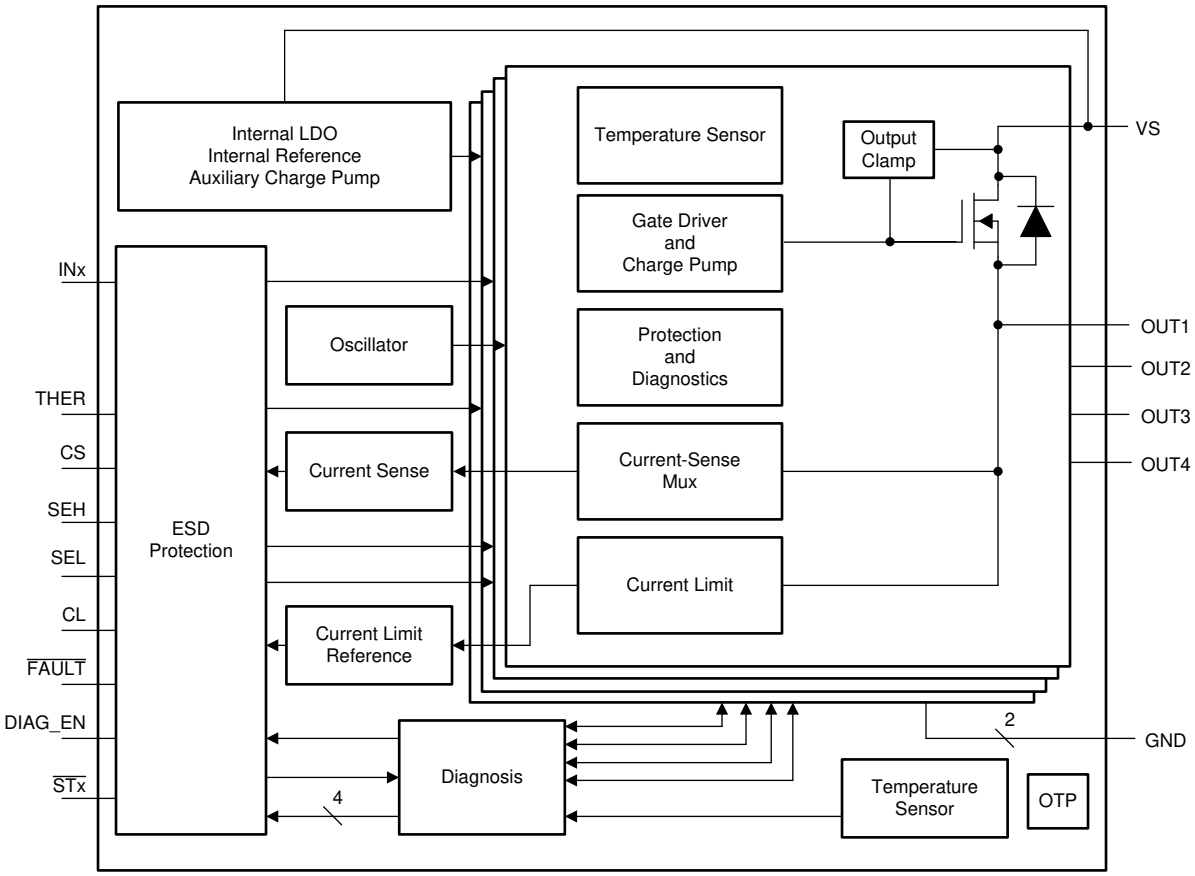

Figure 1-1. Functional Block Diagram

TPS4H160-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS4H160-Q1 based on an industry-wide used reliability standard:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	25
Die FIT rate	6
Package FIT rate	19

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual TJ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS4H160-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT1, OUT2, OUT3, OUT4 open (Hi-Z)	20
OUT1, OUT2, OUT3, OUT4 stuck on (VS)	10
OUT1, OUT2, OUT3, OUT4 not in specification – voltage or timing	45
Diagnostics not in specification	10
Protection functions fail to trip	10
Pin to pin short any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS4H160-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 and Figure 4-2 shows the TPS4H160-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS4H160-Q1 datasheet.

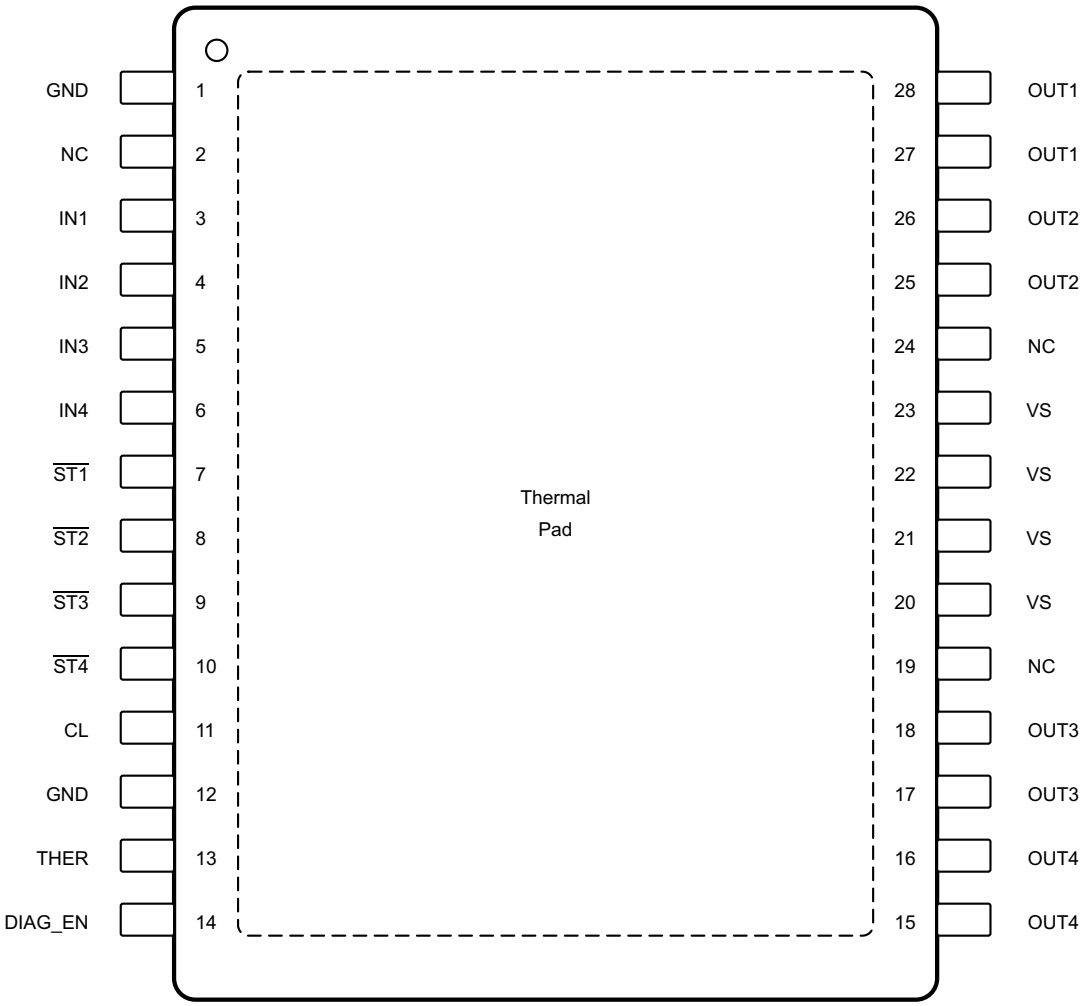

Figure 4-1. Pin Diagram (Version A)

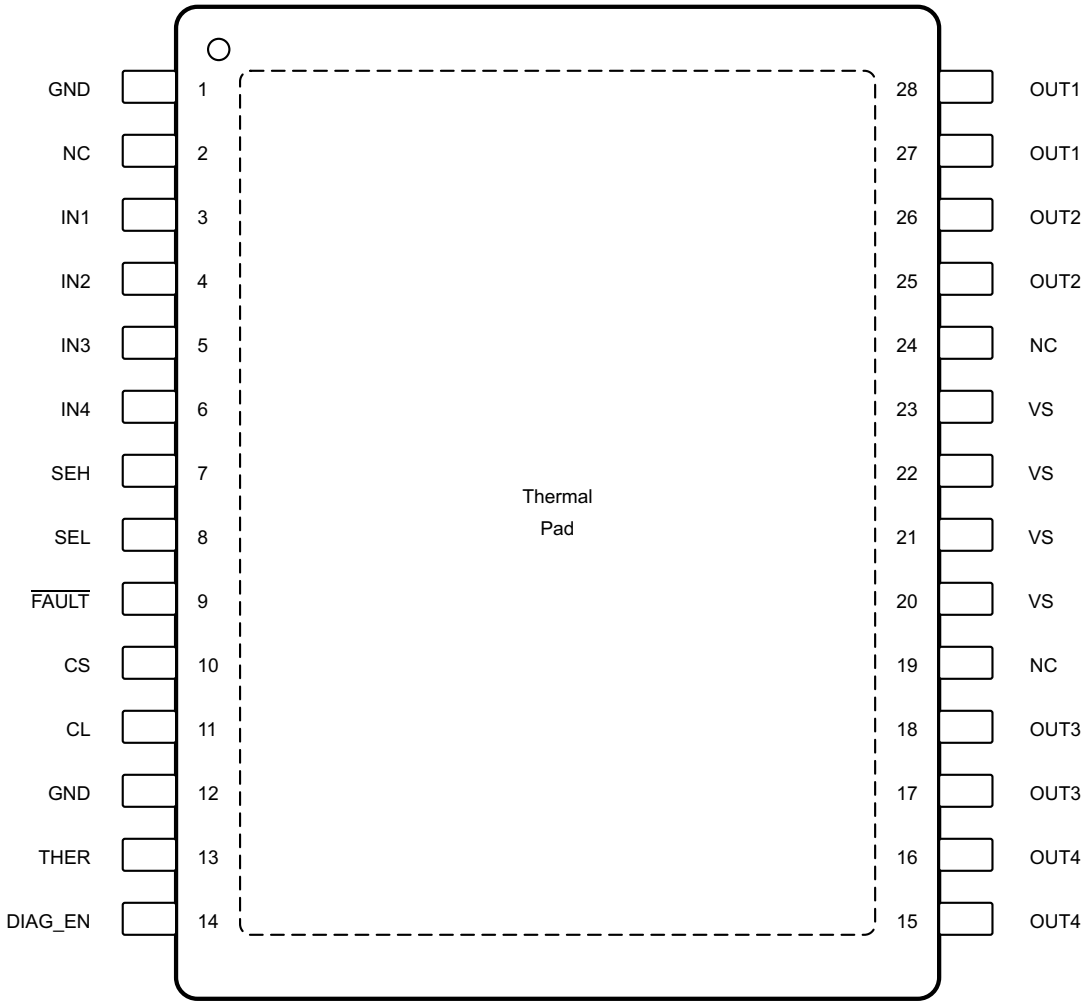

Figure 4-2. Pin Diagram (Version B)

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Follows the datasheet recommendations for operating conditions, external components selection, and PCB layout

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1, 12	The resistor or diode network is bypassed if present.	B
NC	2, 19, 24	There is no effect on the device.	D
INx	3, 4, 5, 6	Shuts down the corresponding channel.	B
$\overline{\text{STx}}$	7, 8, 9, 10	Version A only. The status reported is potentially erroneous.	B
SEH	7	Version B only. If DIAG_EN is high, then only the sense current output of channel 3 or 4 (depending on SEL) is on the SNS pin.	B
SEL	8	Version B only. If DIAG_EN is high, then only the sense current output of channel 1 or 2 (depending on SEH) is on the SNS pin.	B
$\overline{\text{FAULT}}$	9	Version B only. The status reported is potentially erroneous.	
CS	10	Version B only. The sense current is not valid from the CS pin.	B
CL	11	The device defaults to the internal current limit.	C
THER	13	The device defaults to auto-retry mode when encountering a thermal fault.	B
DIAG_EN	14	The diagnostics are disabled.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUTx	15,16,17, 18, 25, 26, 27, 28	The current limit of the device engages.	B
VS	20, 21, 22, 23	The device has no input supply, and therefore, does not function.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1, 12	Loss of ground detection engages and the device shuts off.	B
NC	2, 19, 24	There is no effect on the device.	D
INx	3, 4, 5, 6	Corresponding channel is shut down and INx is pulled down internally.	B
$\overline{\text{STx}}$	7, 8, 9, 10	Version A only. The $\overline{\text{STx}}$ pin cannot pull high and diagnostics cannot be reported.	B
SEH	7	Version B only. Pulled low internally, however, the wrong SNS current is potentially reported on CS if DIAG_EN is high.	B
SEL	8	Version B only. If DIAG_EN is high, then only the sense current output of channel 1 or 2 (depending on SEH) is on the SNS pin.	B
$\overline{\text{FAULT}}$	9	Version B only. The fault signal is not reported.	B
CS	10	Version B only. The correct sense current cannot be read.	B
CL	11	The device defaults to the internal current limit.	C
THER	13	Internally pulled down. The device defaults to auto-retry mode when encountering a thermal fault.	B
DIAG_EN	14	Internally pulled down. The diagnostics are disabled.	B
OUTx	15, 16, 17, 18, 25, 26, 27, 28	There is no effect on the device. If configured, open load detection triggers.	B
VS	20, 21, 22, 23	The device has no input supply, and therefore, does not function.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	NC	There is no effect on the device.	D
NC	2	IN1	There is no effect on the device.	D
IN1	3	IN2	The IN1 signal affects the IN2 signal and vice versa.	B
IN2	4	IN3	The IN2 signal affects the IN3 signal and vice versa.	B
IN3	5	IN4	The IN3 signal affects the IN4 signal and vice versa.	B
IN4	6	ST1	Version A only. If ST1 is high, then channel 4 is on.	B
IN4	6	SEH	Version B only. The IN4 signal affects the SEH and vice versa.	B
$\overline{\text{ST1}}$	7	$\overline{\text{ST2}}$	Version A only. The fault reporting of channel 1 and channel 2 is potentially erroneous.	B
SEH	7	SEL	Version B only. The SEH signal affects the SEL and vice versa. If DIAG_EN is high, only channel 1 or 4 can be read at SNS.	B
$\overline{\text{ST2}}$	8	$\overline{\text{ST3}}$	Version A only. The fault reporting of channel 2 and channel 3 is potentially erroneous.	B
SEL	8	$\overline{\text{FAULT}}$	Version B only. If $\overline{\text{FAULT}}$ is high and DIAG_EN is high, only channel 2 or channel 4 can be read at SNS.	B
$\overline{\text{ST3}}$	9	$\overline{\text{ST4}}$	Version A only. The fault reporting of channel 3 and channel 4 is potentially erroneous.	B
$\overline{\text{FAULT}}$	9	CS	Version B only. The fault reporting and current sense reporting are erroneous.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
$\overline{ST4}$	10	CL	Version A only. The $\overline{ST4}$ voltage can cause an erroneous current limit to be set on the device.	B
CS	10	CL	Version B only. The voltage level on CS can cause an erroneous current limit to be set on the device.	B
CL	11	GND	The device defaults to the internal current limit.	C
GND	12	THER	The device is in auto-retry mode when encountering a thermal fault.	B
THER	13	DIAG_EN	The THER signal affects the the DIAG_EN signal and vice versa.	B
OUT4	15	OUT4	There is no effect on the device.	D
OUT4	16	OUT3	The output of channel 4 is tied to the output of channel 3.	B
OUT3	17	OUT3	There is no effect on the device.	D
OUT3	18	NC	There is no effect on the device.	D
NC	19	VS	There is no effect on the device.	D
VS	20	VS	There is no effect on the device.	D
VS	23	NC	There is no effect on the device.	D
NC	24	OUT2	There is no effect on the device.	D
OUT2	25	OUT2	There is no effect on the device.	D
OUT2	26	OUT1	The output of channel 2 is tied to the output of channel 1.	B
OUT1	27	OUT1	There is no effect on the device.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (VS)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1, 12	The supply power is bypassed and the device is not turned on.	B
NC	2, 19, 24	There is no effect on the device.	D
INx	3, 4, 5, 6	There is a potential violation of the absolute maximum rating of the pin, and a breakdown of the ESD cell is possible.	A
$\overline{STx}$	7, 8, 9, 10	Version A only. There is a potential violation of the absolute maximum rating of the pin, and a breakdown of the ESD cell is possible.	A
SEH	7	Version B only. There is a potential violation of the absolute maximum rating of the pin, and a breakdown of the ESD cell is possible.	A
SEL	8	Version B only. There is a potential violation of the absolute maximum rating of the pin, and a breakdown of the ESD cell is possible.	A
$\overline{FAULT}$	9	Version B only. There is a potential violation of the absolute maximum rating of the pin, and a breakdown of the ESD cell is possible.	A
CS	10	Version B only. There is a potential violation of the absolute maximum rating of the pin, and a breakdown of the ESD cell is possible.	A
CL	11	There is a potential violation of the absolute maximum rating of the pin, and a breakdown of the ESD cell is possible.	A
THER	13	There is a potential violation of the absolute maximum rating of the pin, and a breakdown of the ESD cell is possible.	A
DIAG_EN	14	There is a potential violation of the absolute maximum rating of the pin, and a breakdown of the ESD cell is possible.	A
OUTx	15, 16, 17, 18, 25, 26, 27, 28	The output is pulled to the supply voltage. The short-to-battery detection is triggered if configured.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 29, 2021 to July 7, 2026 (from Revision B (May 2021) to Revision C (July 2026)) **Page**

- Added the *Component Failure Rates per IEC TR 62380 / ISO Part 11* 3

Changes from May 7, 2021 to June 28, 2021 (from Revision A (May 2021) to Revision B (June 2021)) **Page**

- Updated Failure Mode Distribution to 10% in *Protection functions fail to trip* row..... 4

Changes from January 17, 2020 to May 6, 2021 (from Revision * (January 2020) to Revision A (May 2021)) **Page**

- Updated to current TI format..... 2

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