Application Report

Optimizing Load Releasing Characteristics in TV Applications

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ABSTRACT

This application report presents how to achieve a good performance of TPS5432 which is a current mode-controlled DC/DC converter and is using SoC (System on chip) power rail in FHD LCD TV application. The load dump characteristics caused by SoC off sequence and the relation between an excessive overshoot voltage on switching node and OVT (overvoltage transition) / RCP (Reverse current protection) during load dump are analyzed.

In addition, the report verifies that an excessive overshoot voltage impacts on a long-term reliability of internal FETs and show feasible approaches to reduce the peak level. Furthermore, the life span of DC/DC against repetitive peak level is estimated.

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Trademarks

1 Introduction

General power rails on TV scaler board in FHD LCD TV include 1.5 V rail for DDR chipset, 1.2 V for SoC chipset, 3.5 V for u-Com, 3.3 V for peripheral rails such as I^2C pull up and the logic voltage of the audio amplifier and 5 V for HDMI, USB and HDD ports. In this application report, TPS5432 is used to generate 1.2 V rail for the core voltage of SoC chipset.

Because the TPS5432 is a 6 V, 3 A, low Iq, current mode, synchronous monolithic buck converter with integrated MOSFETs. The TPS5432 enables small designs by integrating the MOSFETs, implementing current mode control to reduce external component count, reducing inductor size by 700kHz switching frequency. SOIC-8 package with exposed thermal pad provides both thermally enhanced solution and easy to use.

In addition, the load release characteristics caused by SoC chipset during power off sequence is verified and it can trigger an unexpected OVTP (Overvoltage transition protection) and RCP (Reverse current protection) as well as. Furthermore, it results in generating a severe overshoot voltage on PH node.

2 Load Release Characteristics of SoC Chipset

Figure 2-1 (left) shows 1.2Vo rail for SoC core voltage during power on and off sequence as shown in Figure 2-1 (right). The Inductor current is sharply changed from a full load condition to a light load condition before 1.2Vo rail is trued off. It is a unique load characteristics caused by SoC chipset.

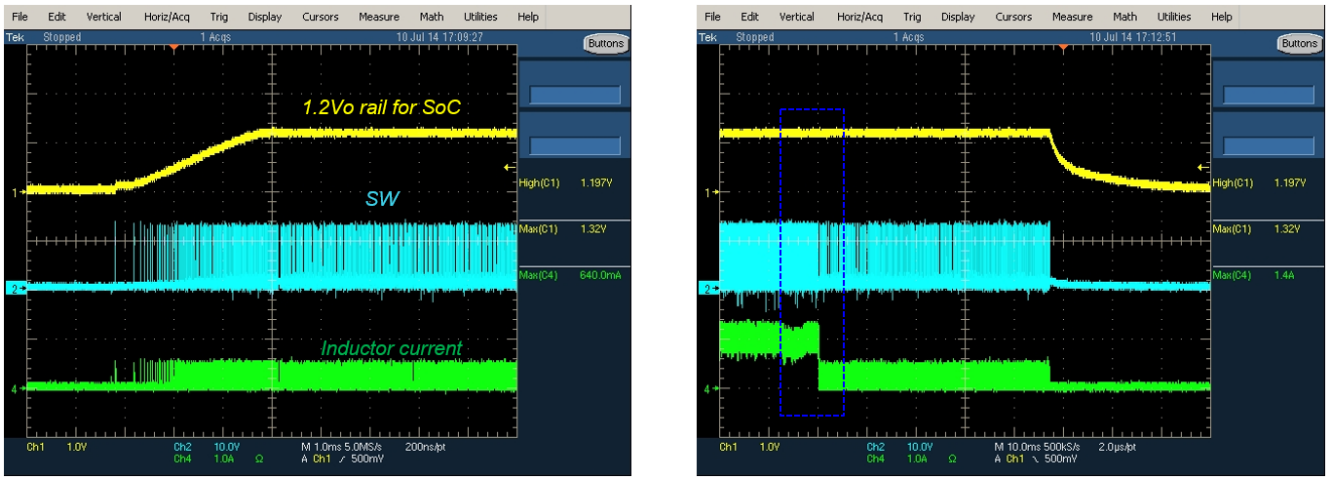


Figure 2-1. SoC core Voltage During Power On and Off Sequence

3 Unexpected Protection Behavior During the Load Release of SoC Chipset

Figure 3-1 (left) shows the TPS5432 application to generate 1.2Vo rail for SoC core voltage in the TV application. The problem is that there is an excessive overshoot voltage on PH node as shown in Figure 3-1 (right). As the root cause of the overshoot voltage, Vout (VSENSE pin voltage) is greater than the OVTP threshold during the load release of SoC chipset, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. However, the converter sinks current through its low side FET.

As an additional RCP (Reverse current protection) scheme, the control circuit turns off the low side MOSFET when the reverse current is more than 1.8 A. At this time, Current starts flowing though on the body diode of high side FET to input capacitor. When Vout drops lower than the OVTP threshold, high side MOSFET is allowed to turn on the next clock cycle. Then it causes a severe ring voltage because of an accumulated charge into input capacitor, the leakage inductance on PCB layout and capacitance of FETs.

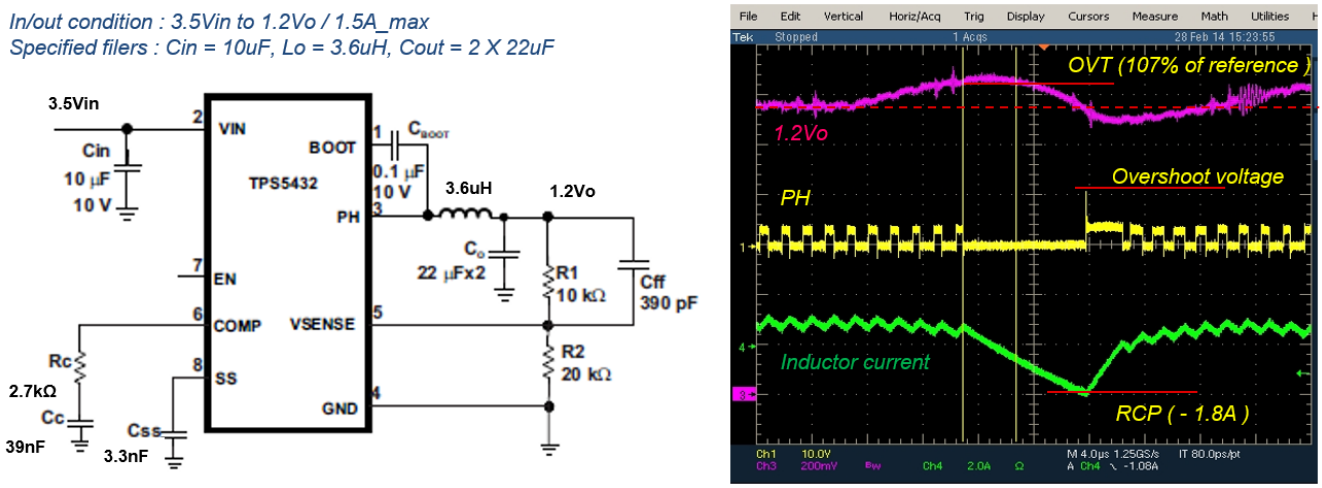


Figure 3-1. An Unexpected Protection Behavior During the Load Release of SoC chipset

The worst overshoot voltage reaches to 12.6 V peak for 3.5ns in this application as shown in Figure 3-2. To figure out the worst case, a high-resolution Oscilloscope (Tektronix DPO7354C model with 500MHz Bandwidth) and Probe (P6139B probe) are used. Even though this overshoot voltage will not cause immediate device damage, it can affect a long-term device reliability.

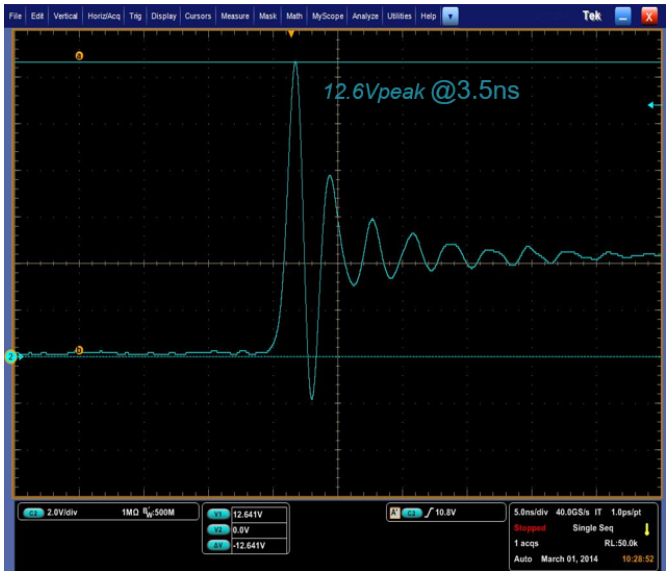
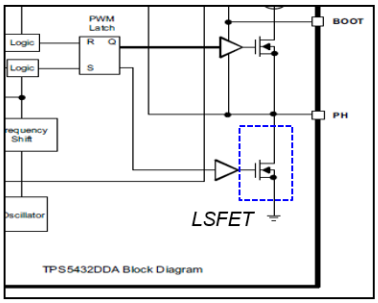


Figure 3-2. The Worst Overshoot Voltage in the Application

4 Investigation on a Long-Term Reliability

When looking into the breakdown voltage of LSFET and the distribution data in order to see whether the overstress on the switching node can reach the Breakdown voltage of LSFET as shown in Figure 4-1 (left). The worst voltage level, 12.6V is reaching minimum spec of the breakdown voltage of LSFET and some devices are in the risk zone (5 / 7,710 units) based on the distribution data as shown in Figure 4-1 (right).



	Typ.	LSL	USL		
BVdss	14	11.2	16.8	Volts	Vg=0V, Vs=0V, Vb=0V, Id=uA, T=27C, L=0.8du, W=39.8du, Nfi=1, Ndev=1, Id=1uA; Vs=Viso=0V, Cpk=1.67

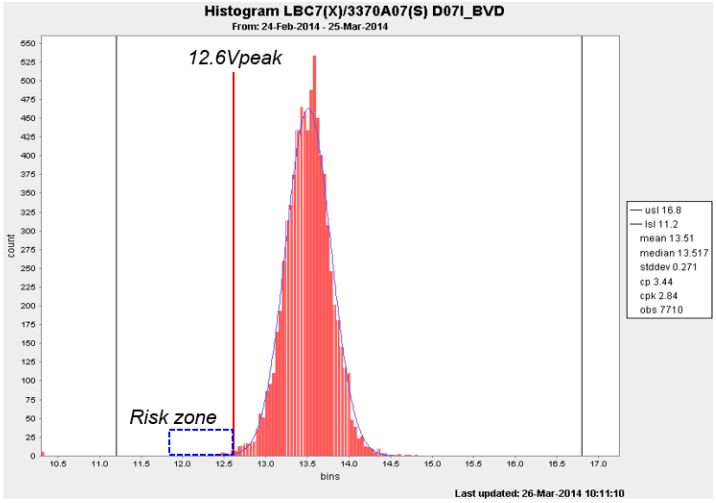
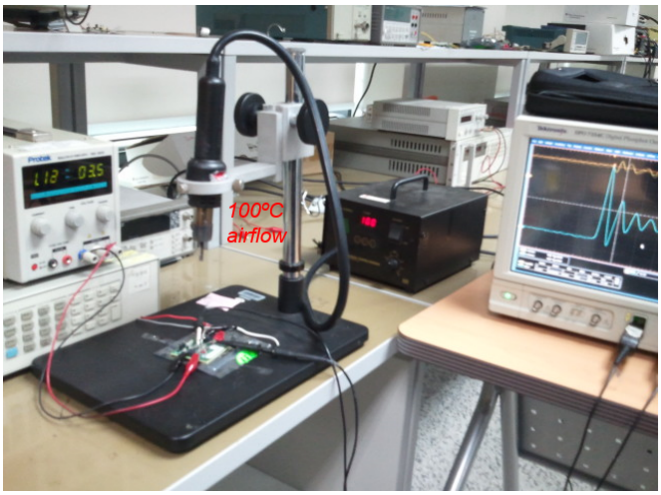
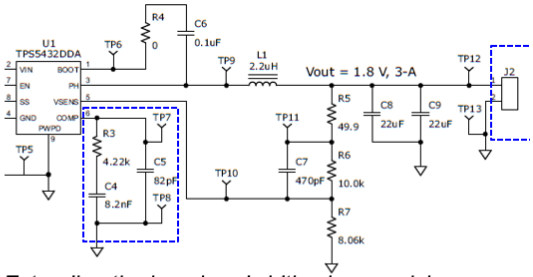


Figure 4-1. Breakdown Voltage and Distribution data

Figure 4-2 (left) shows the test bench and the duplication conditions in order to duplicate a similar overshoot voltage with TPS5432 EVMs. Duplication conditions are that Input voltage is changed from 3.3V to 3.5 V and temperature condition is 100ºC airflow to simulate real TV application condition. In addition, external components including compensation values and output filters are changed as a shown in Figure 3-1 (left). To make a similar load release as real TV application, the step load from 1.2 to 0A is applied on output node with dynamic electronic load. Totally, 40 pcs x TPS5432 EVMs is tested.





Extending the loop bandwidth when applying the step load (1.2A to 0A) to output node

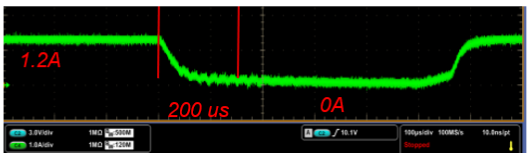


Figure 4-2. Reliability Test Set Up and Condition

When checking out the overshoot waveforms, repetitive spikes are observed with 3.5ns as transient time and 13 V peak as peak voltage level as shown in Figure 4-3. It is a similar level under a unique load characteristic of SoC chipset.

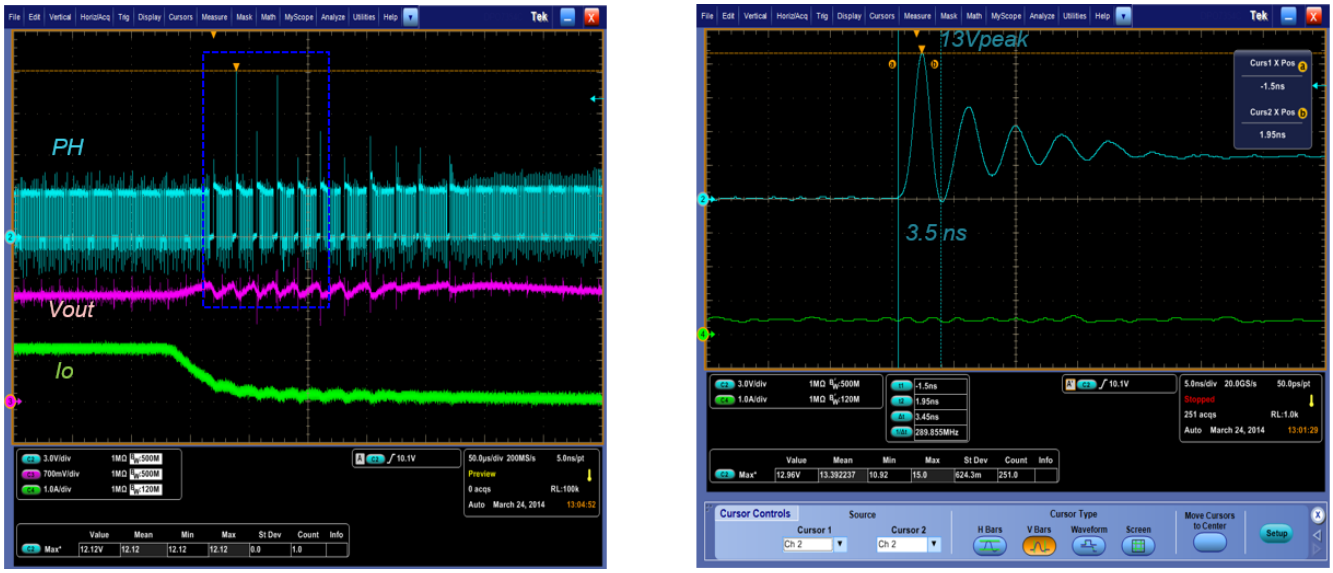


Figure 4-3. Duplicated Waveform

When continuing to apply the repetitive spikes to devices, LSFET gets softly damaged. 39pcs out of 40 EVMs can support more than 100,000 times without device damage. However, 1pcs out of 40 EVMs gets softly damage after 84,000 times as the worst case. at the time, Input current can be higher than initial level.

As shown in Figure 4-4, it is confirmed that Pin short (Pin 3/PH vs pin 4/GND) is observed and the damage as flashed metal is observed. therefore, it is obvious that a repetitive peak overstress can have a negative impact on a long-term device reliability.

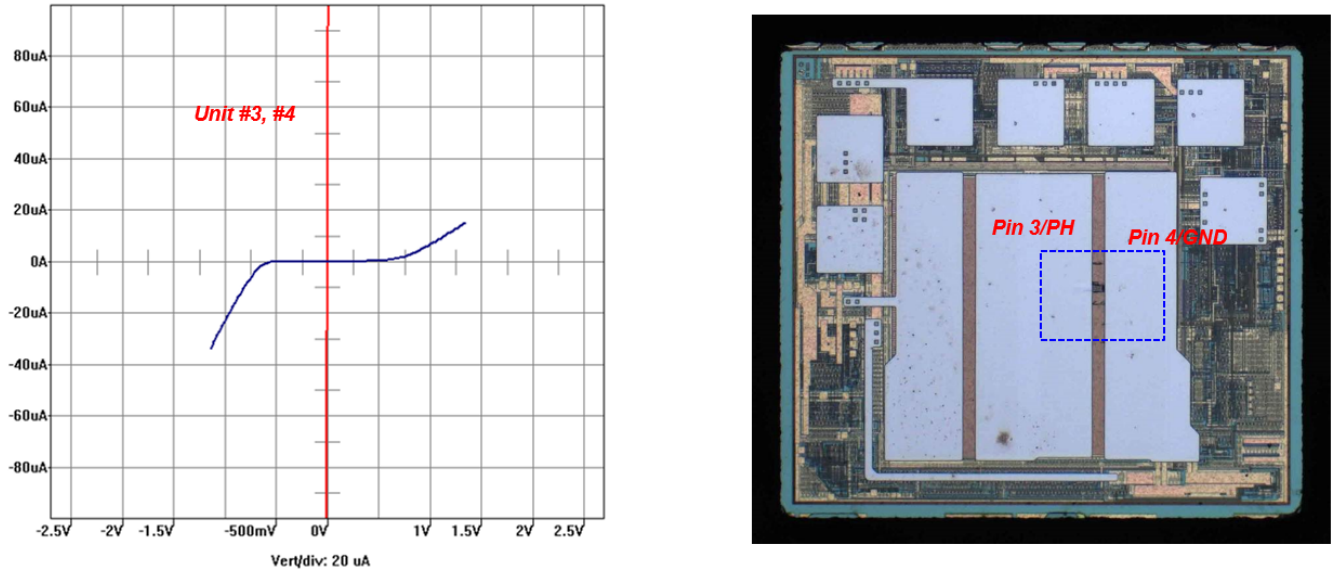


Figure 4-4. Failure Analysis

5 Design Approaches to Improve the Load Release Characteristics of SoC Chipset

General approaches to improve the load release are to move the input capacitor to device input pin or adding more input capacitors or adding Rboot in series with Cboot or add more output capacitors to achieve fast load transient. However, it doesn't work to reduce the overshoot voltage in the application. Instead when adding schottky diode (SX34) on HSFET for current bypass, it can reduce the positive overshoot voltage but it makes a negative ringing voltage higher as shown in Figure 5-1.

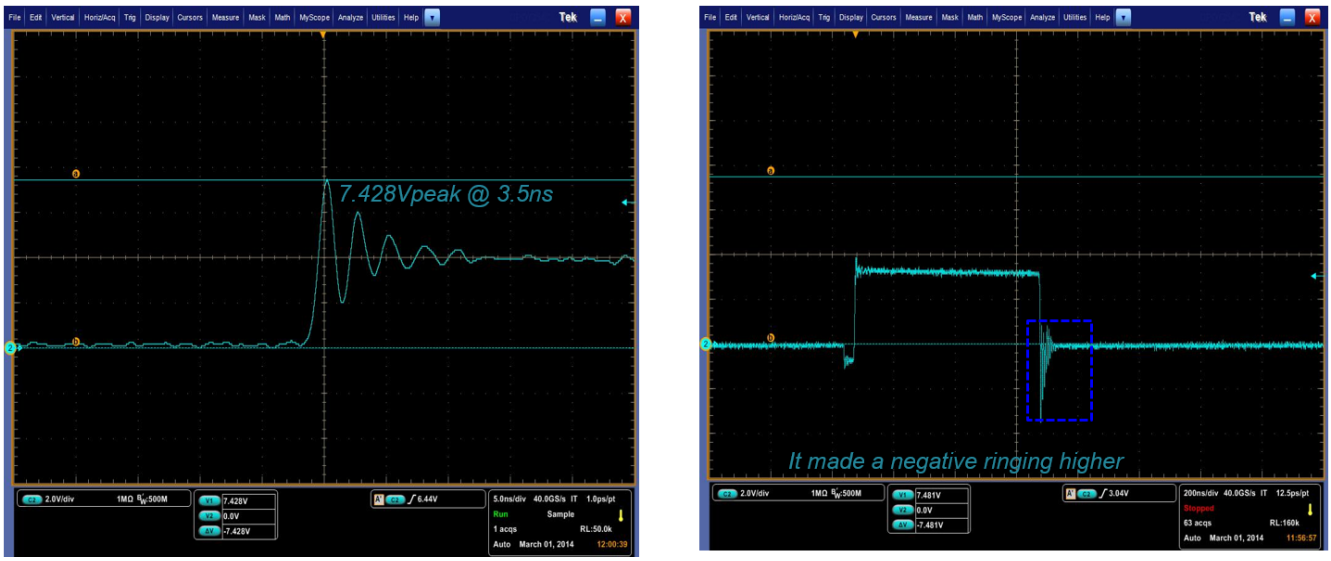


Figure 5-1. Added Schottky Diode (SX34) on PH Node

When adding RC snubber (3.3 ohm + 470pF) on PH node to damp the parasitic inductances and capacitances during the switching transitions, the overshoot voltage is reduced down to 7.7 V peak as shown in Figure 5-2.

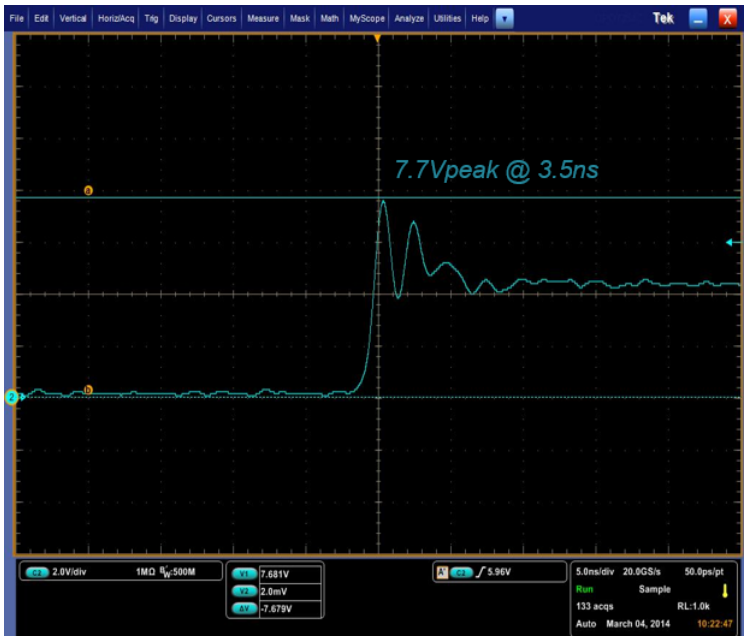


Figure 5-2. Added RC Snubber (3.3 ohm + 470pF) on PH node

Another approach is to extend TPS5432 loop bandwidth with optimizing compensation RC values in the application without adding external circuits such as schottky diode and RC snubber. Extending the loop bandwidth can achieve a fast load transient response as shown in Figure 5-3. OVT (pulse skip) and RCP is still observed when the loop bandwidth is 12kHz as shown in Figure 5-3 (left). There is still OVT (Shorter pulse skip time) when the loop bandwidth is 25kHz as shown in Figure 5-3 (middle). However, when the loop bandwidth is 37.57kHz, OVT and RCP is not observed in Figure 5-3 (right). In addition, there is no overshoot voltage on PH node any more.

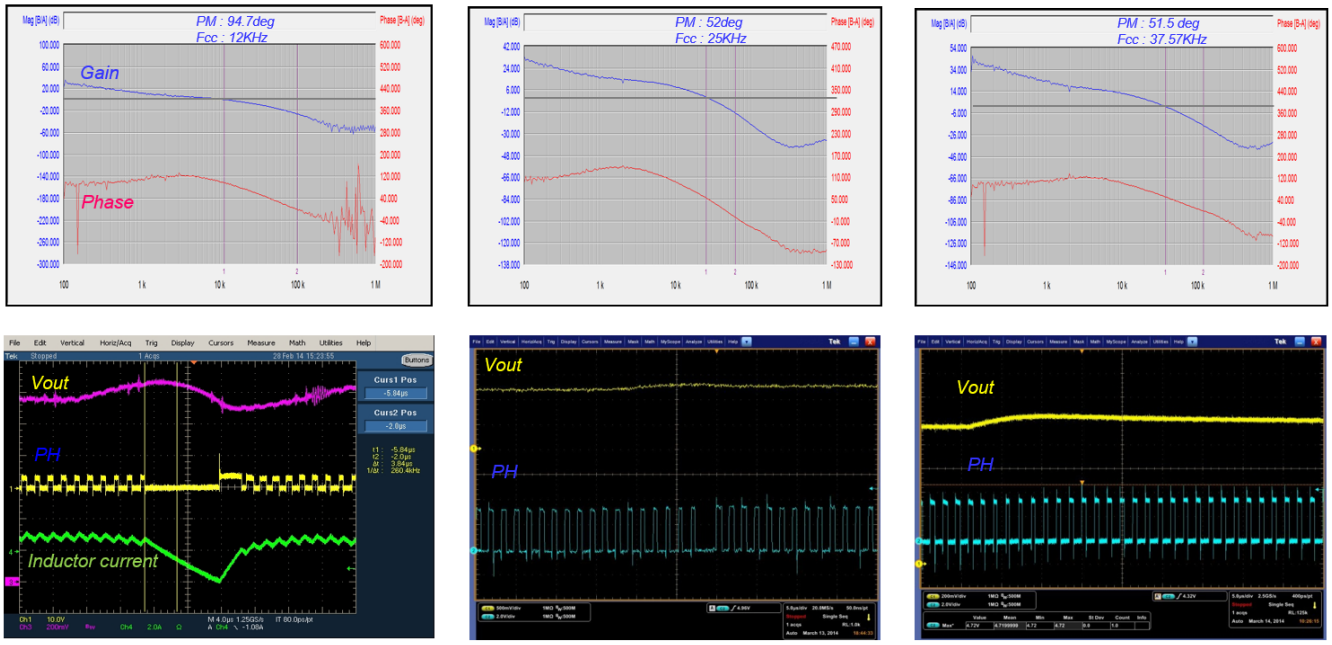


Figure 5-3. Extending the Loop Bandwidth

6 Conclusion

This application report shows the load release characteristics of SoC chipset using in FHD TV application. For the severe overshoot voltage on PH node in TPS5432 application which is for 1.2 V SoC rail, it can be caused by an unexpected OVT (Overvoltage transient protection) and RCP (Reverse current protection) under TV SoC load release condition.

In addition, when applying repetitive overshoot voltages to devices, LSFET gets softly damaged after 84,000 times as the worst case. therefore, the excessive overshoot voltage can impact a long-term device reliability.

A feasible approach is to add a RC snubber on the switch node (PH) to reduce the peak voltage level. Furthermore, in case the loop bandwidth is extended up to 37 kHz, an unexpected OVT and RCP is not observed. In the application, optimizing compensation network to extend the loop bandwidth is recommended approach.

7 References

- Texas Instruments, *TPS5432 2.95V to 6V Input, 3A Output, 700kHz Synchronous Step-Down Converter* data sheet.
- Texas Instruments, *TPS5432EVM-116 3-A, SWIFT™ Regulator Evaluation Module* User's Guide.

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