Application Note

Unraveling the Full-Scale Mysteries of Your RF Converter's Analog Inputs

Rob Reeder

ABSTRACT

This application note includes some of the details related to analog input trade-offs, and how to properly deduce the converter's full-scale range in reference to the analog input network in dBm.

Table of Contents

Trademarks

Marki® is a registered trademark of Marki Microwave.
All trademarks are the property of their respective owners.

1 Introduction

High-Speed/RF Analog-to-digital converters (ADCs) operate differently. The ADC analog inputs are voltage-input-sensitive devices that leave RF engineers wondering how to match the converter to the analog inputs. Adding to this confusion, analog input interfaces are typically differential by nature and host a time-varying type of input impedance as the internal sampling switch opens and closes at the speed of light or so this seems. This input impedance is thought to be a real resistive value across the converter's input bandwidth, but when plotted on a Smith chart, the trace curve just goes around and around.

2 Understanding Full-scale and ADC Headroom

Years ago, high-speed data converters were designed on process nodes that supported voltage swings as large as 10 Vpp full-scale.

The converters were even single-ended. Setting the converter's reference gave some flexibility to make the full-scale range unipolar or bipolar.

Today, the converter process nodes are small – 65nm or less – and the converter's internal analog input front end is biased at <2 V AVDD. This makes for significantly lower headroom, which can become a challenge when signal chain designs need to interface with 1 or 2 Vpp full-scale ranges, where the RF stops and the ADC begins.

Today, most high-speed data converters employ differential inputs. This implies we only have one-fourth the signal swing to wrap around the common-mode voltage (VCM) bias, or each analog input handles one-half the swing. Figure 1 illustrates single-ended vs. differential signal properties and definitions.

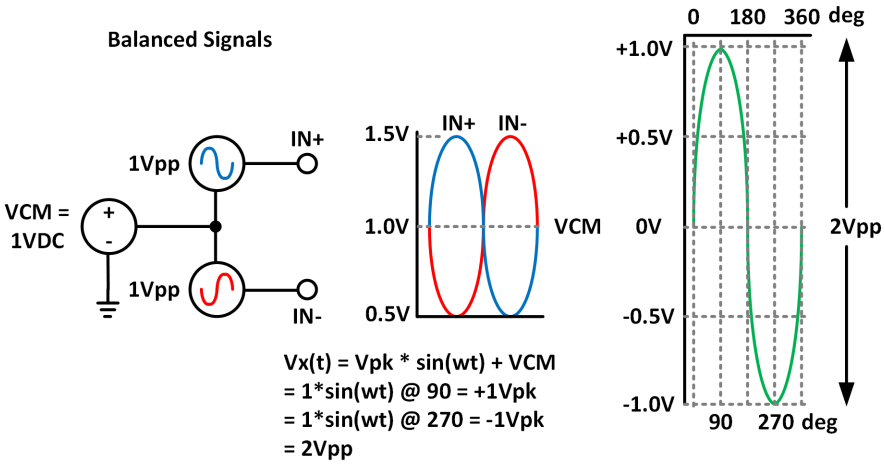

Figure 2-1. Single-Ended vs. Differential Analog Input Signals

The converter's analog input VCM is important and needs to be satisfied by the external input network front end; otherwise, the converter can have other performance issues.

By dividing up the signal swing differentially, this interface enables you to maintain higher voltage levels across the full-scale range (that is, 1 or 2Vpp); therefore, the differential nature of the analog input enables a smaller process node.

3 Full-Scale Trade-offs

Some converters are flexible and can dedicate a few, out of the few thousand, Serial Peripheral Interface (SPI) registers to change the full-scale swing. Keep in mind that a design with a larger full-scale range generally yields a better signal-to-noise ratio (SNR). But better SNR performance usually decreases the harmonic performance of the spurious free dynamic range (SFDR). The SNR increases because the analog input signal swing can be larger now, assuming that the noise stays constant. Conversely, a smaller full-scale range enables better SFDR (typically better HD2 and HD3) performance; however, there is a slight sacrifice in SNR. See Figure 3-1 and Figure 3-2 to understand these trade-offs.

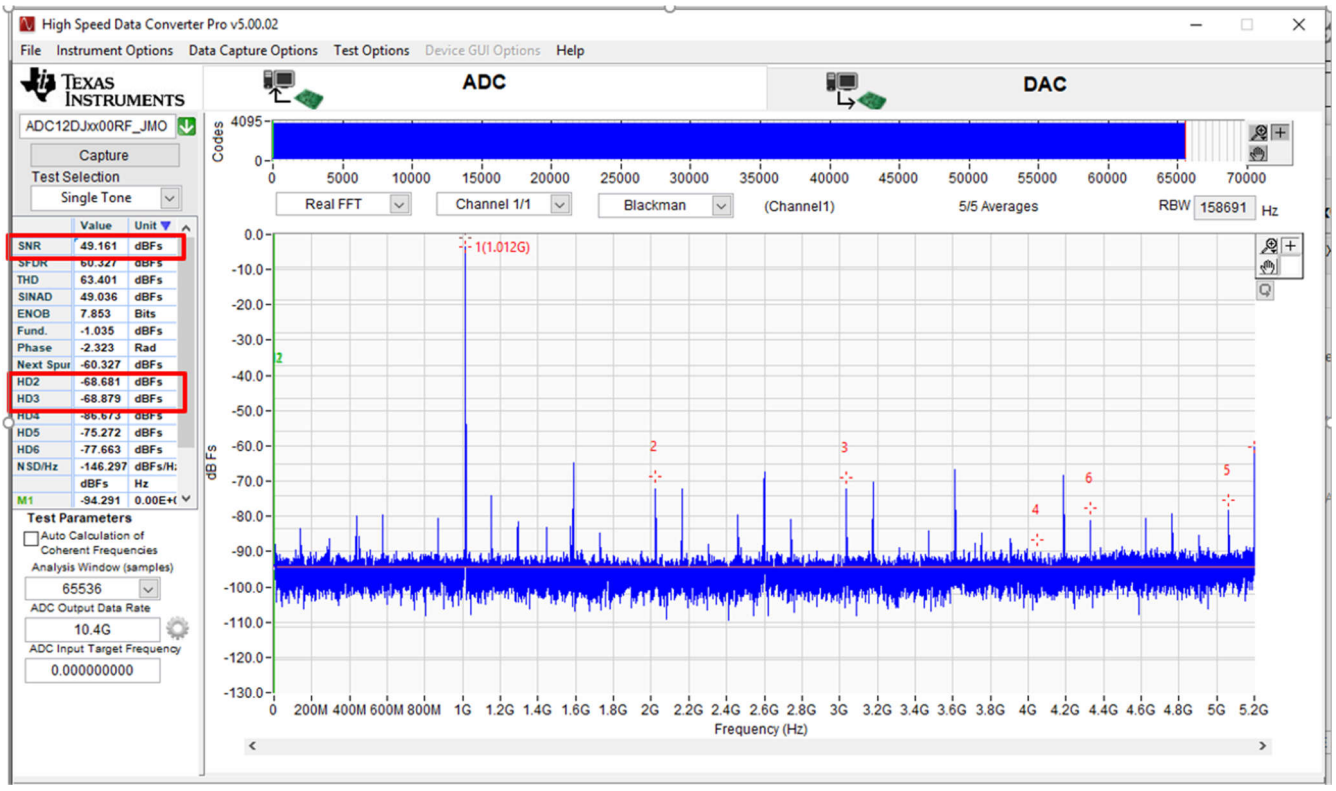

Figure 3-1. Minimum Full-Scale Value (430mVpp) = SFDR Increase or SNR Decrease

As shown in Figure 3-1 the input full-scale range changed from a default value of 800 mVpp to 430 mVpp. This reflects a slight increase in SFDR or HD2 and HD3. The input full-scale value changing from the default 800 mVpp to 1.0 Vpp yields a slight increase in SNR, as shown in Figure 3. Notice the HD2 and HD3 decrease in Figure 3-2 vs. Figure 3-1.

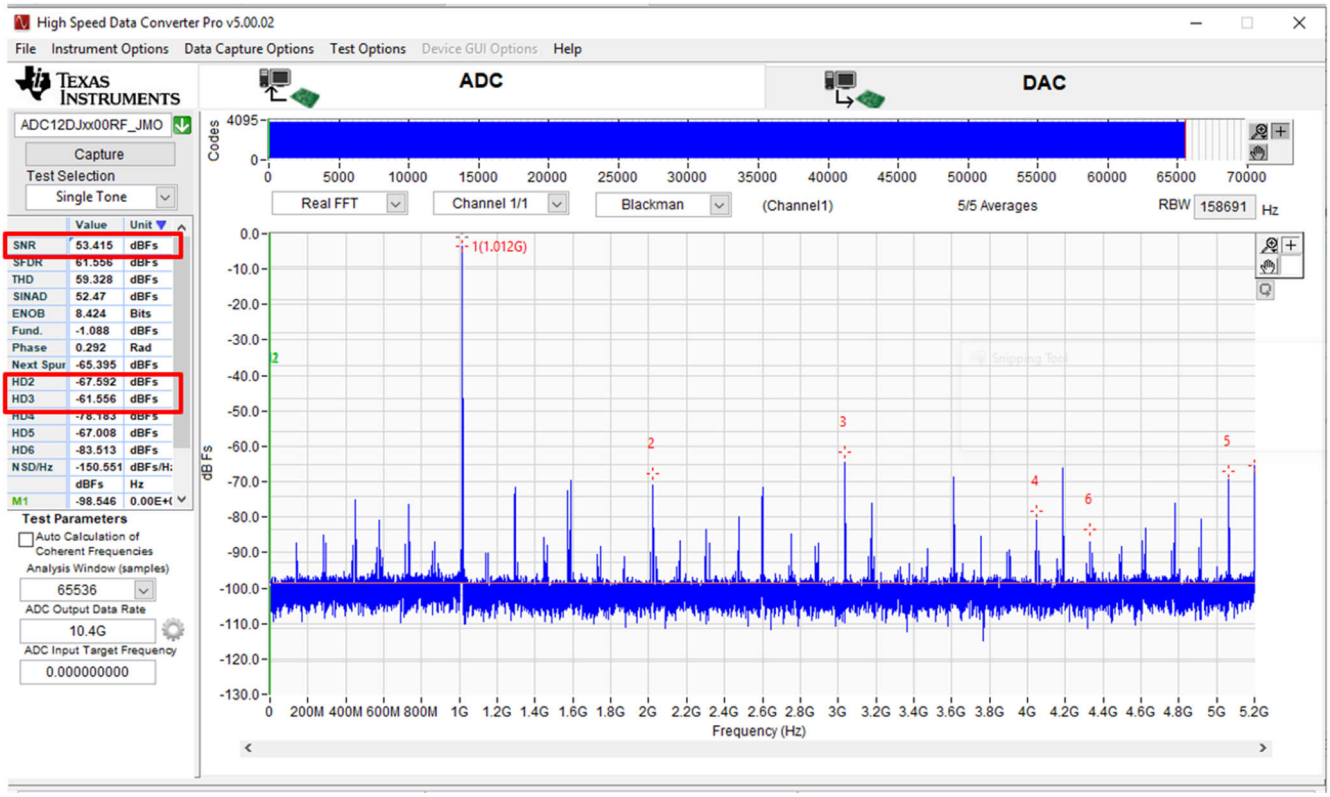

Figure 3-2. Maximum Full-Scale Value (1.0Vpp) = SNR Increase or SFDR Decrease

In either case, you can *dial in* the best AC performance for your application by optimizing the full-scale value.

Other SPI registers allows changes to the input impedance, possibly halving or doubling the input impedance on the differential inputs. This means that you can optimize the *matching* network when designing the frontend. The input full-scale range can once again change in value. Not all converters offer these features, but some do, which is easier than changing the frontend circuitry to accommodate different applications or adding additional components to the frontend network.

4 Full-Scale Breakdown

Following is an example that illustrates the trade-offs involved when designing a high-speed matching network to the ADC. Baluns and frontend networks can add loss and additional noise figure to the overall signal chain, so it is pertinent to understand the input-drive trade-offs during the design and optimize the full-scale value. The input drive defines the amount of signal (in dBm) required to drive the converter at a full-scale range in front of the interface network – in this case, a passive balun network.

In the example, the ADC is the RF-sampling, 12-bit *ADC12DJ5200RF* from Texas Instruments and the balun is the BAL-0009SMG from Marki® Microwave. A front-end resistive network interfaces the balun differential outputs to the ADC differential inputs. See Figure 4-1.

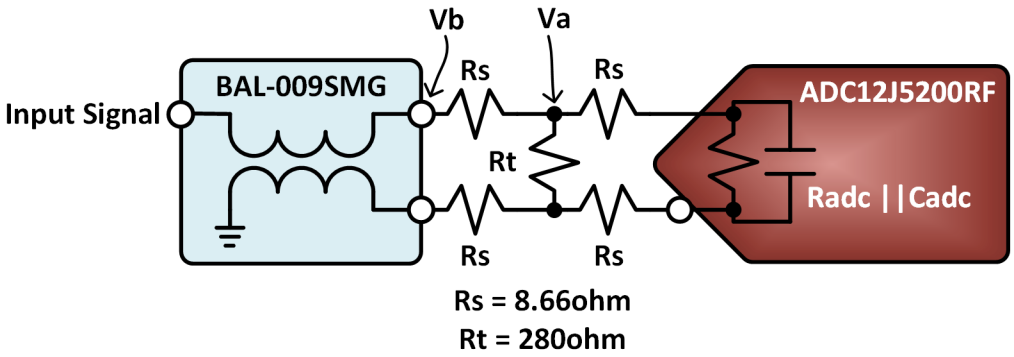

Figure 4-1. Example Front-End Network

Next are the calculations. If no dBm calculator is handy, the recommendation is to download the latest TI 84 Plus app to your mobile phone.

The ADC12DJ5200RF has a default analog input full-scale range of 800-mVpp(Vfs) with a 100Ω (Radc) differential load internally which is calculated in terms of dBm:

$$Padc = 10 \times \log\left(\frac{\left(\frac{\frac{Vfs}{2}}{\sqrt{2}}\right)^2}{\frac{Radc}{0.001}}\right) \quad or \quad 10 \times \log\left(\frac{\left(\frac{\frac{800m}{2}}{\sqrt{2}}\right)^2}{\frac{100}{0.001}}\right) = -0.97 \ dBm \tag{1}$$

Since the input network is differential, the network can become a little difficult to crunch through the numbers. But by using the single-ended approach, the full-scale voltage at the input of the converter has a value of 400mVpp (Vfs/2) or -3.97dBm.

By using a front-end resistive network as described, calculate the voltage dividers to understand the losses required to achieve a 400 mVpp (Vfs/2) full-scale value.

Radc/2 = 50Ω and Rs form a resistive divider or

$$Va = \left(\frac{Vfs}{2}\right) \times \left(\frac{\left(\left(\frac{Radc}{2}\right) + Rs\right)}{Radc}\right) = 0.47 \ V \tag{2}$$

which gives you a single-ended voltage input at Rs and Rt. Now, calculate the single-ended voltage at the balun output, or

$$Vb = Va \times \frac{\left(\left(\left(\frac{Radc}{2}\right) + Rs\right) \middle|\middle| \left(\frac{Rt}{2}\right)\right) + Rs}{\left(\left(\left(\frac{Radc}{2}\right) + Rs\right) \middle|\middle| \left(\frac{Rt}{2}\right)\right)} = 0.57 \ V \tag{3}$$

You can make this single-ended voltage a differential voltage or 2×Vb or 1.13V = Vdiffbo. The power at the balun's output is then

$$Pbo = 10 \times \log \frac{\left(\left(\frac{Vdiffbo}{\frac{2}{\sqrt{2}}}\right)^2\right)}{\frac{Radc}{0.001}} = +2.06 \ dBm \quad (4)$$

Now for the fun part: either consult the data sheet of the prospective balun or measure the balun on your nearest four-port vector network analyzer and take an SDS21 measurement. This can yield a single-ended-to-differential measurement and provide the correct insertion loss across the balun. In this example, measuring the BAL-0009SMG yields a loss of 4.2dB at 1GHz. See Figure 4-2.

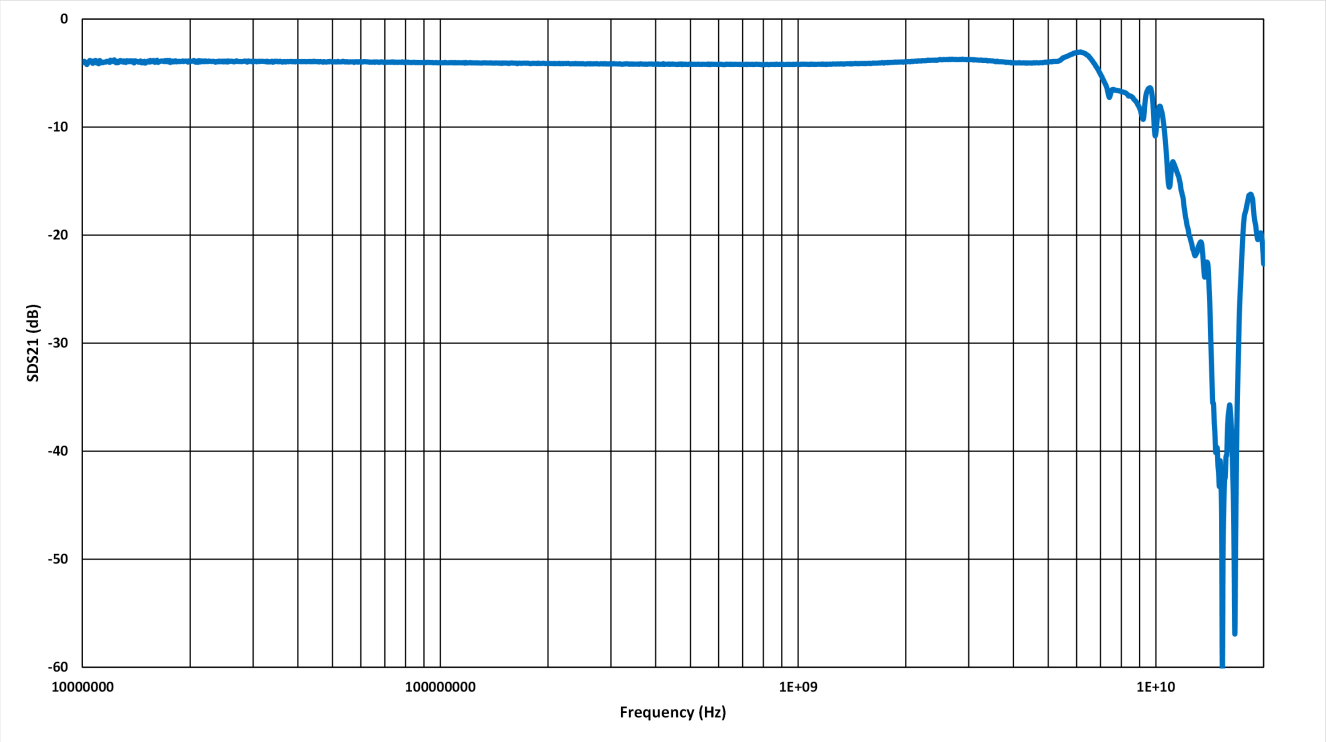

Figure 4-2. SDS21 Insertion ILoss Plot of the Marki Microwave BAL-0009SMG Balun

Adding the balun losses to the output power found at the balun's output (resistive network loss) determines what the input drive is: 2.06 + 4.2 or +6.26dBm. +6.26dBm is the required input amplitude required to drive the analog input signal on the primary of the balun to the full-scale range of the ADC.

Therefore, the total losses from top to bottom are 6.26 + 0.97, or a 7.26dBm loss. Remember the Padc equation (with the result of -0.97dBm) to achieve the full-scale value? Add that result back in, also to achieve 0dB fullscale of the ADC.

A quick note on noise figure: When designing an analog receiver chain, the loss in the balun and frontend network counts as well. For this case, the noise figure addition can be the loss found or 6.26dBm, which is a value of 1.3Vpp vs. the default full-scale value of 800mVpp. This means 20×log(1.3/0.8) = 4.22dB of additional noise figure in the receiver signal chain.

Looking at a different approach: measuring in the lab with the ADC12DJ5200RF evaluation module. Using the signal generator, dial in the output level until the converter is very near the full-scale value at 1GHz. In this case, the input full-scale value was +6.3 dBm from the signal generator reading. Keep in mind that balun variance and cable/connector losses can cause some differences. See Figure 4-3.

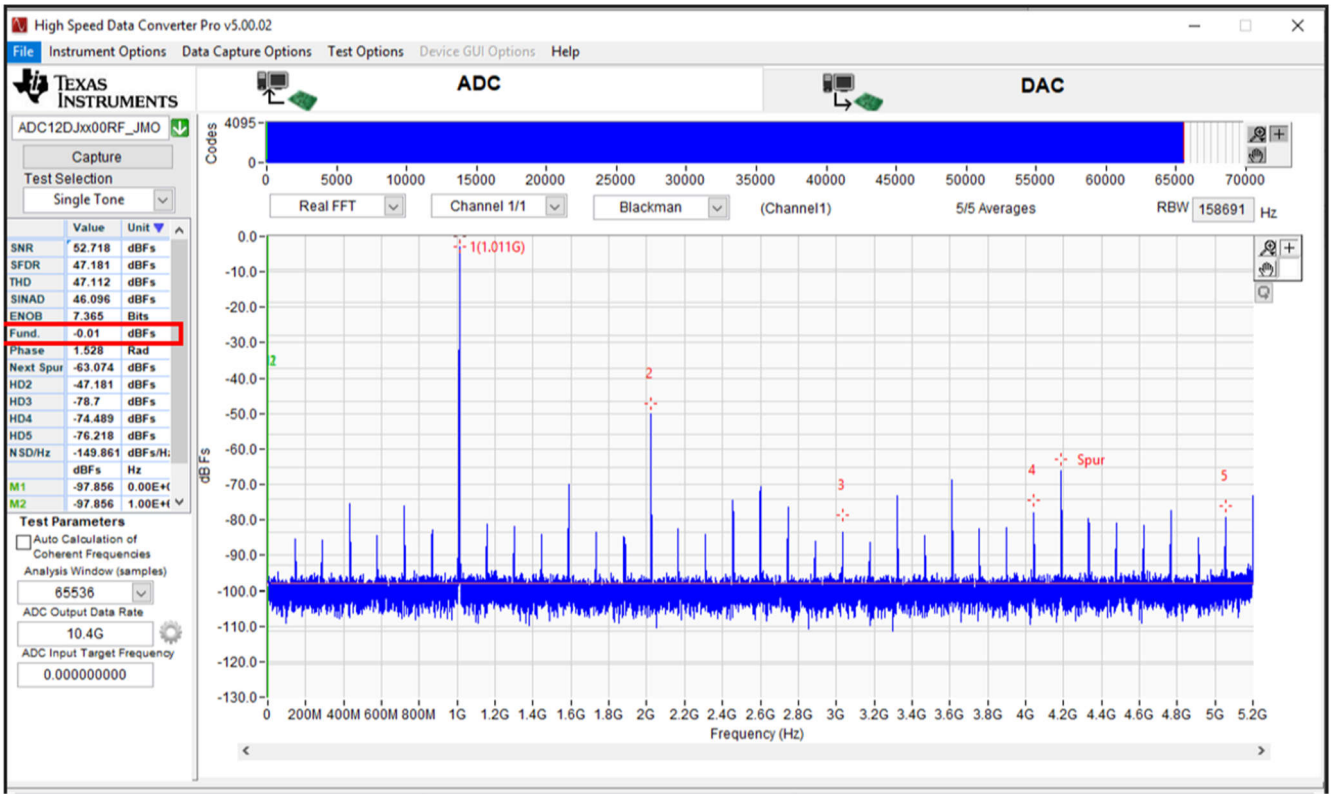

Figure 4-3. HSDC-Pro FFT Plot Showing an Unfiltered Intermediate Frequency of 1GHz at -0.01dBFS

5 Summary

Understanding the input drive and full-scale range trade-offs in converters can be vital when designing analog receiver front ends. The quick method described here in this application note is given for analyzing the front end can help keep trade-offs well within range. For a spreadsheet of the analysis described in this article, please email Rob Reeder at r-reeder@ti.com.

6 References

- Texas Instruments, *ADC12DJ5200RF 10.4GSPS Single-Channel or 5.2GSPS Dual-Channel, 12-bit, RF-Sampling Analog-to-Digital Converter (ADC)*, data sheet.
- Marki microwave, *BAL-0009SMG Surface Mount Broadband Balun*, device overview.
- Texas Instruments, *Input Voltage Range Calcs*, Excel spreadsheet.

7 Revision History

Changes from Revision * (March 2025) to Revision A (April 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed hyperlink to *Input Voltage Range Calcs*	8

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265