User's Guide

TPS54320 Step-Down Converter Evaluation Module User's Guide

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Trademarks

1 Introduction

This user's guide contains background information for the TPS54320 as well as support documentation for the TPS54320 evaluation module (HPA513). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54320.

1.1 Background

The TPS54320 dc/dc converter is designed to provide up to a 3 A output. The TPS54320 implements split input power rails with separate input voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 17 V while the control input (VIN) is rated for 4.5 to 17 V. The TPS54320 provides both inputs but is designed and tested using the PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54320 regulator. The switching frequency is externally set at a nominal 480 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54320 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS54320 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54320 provides adjustable slow start, tracking and undervoltage lockout inputs. The absolute maximum input voltage is 20 V for the TPS54320.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54320	VIN = 8 V to 17 V (VIN start voltage = 6.806 V)	0 A to 3 A

1.2 Performance Specification Summary

A summary of the TPS54320 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of 12 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54320 is designed and tested for V_{IN} = 8 V to 17 V with the VIN and PVIN pins connect together with the JP1 jumper. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54320 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range (PVIN = VIN)			8	12	17	V
V_{IN} start voltage				6.806		V
V_{IN} stop voltage				4.824		V
Output voltage set point				3.3		V
Output current range	V_{IN} = 8 V to 17 V		0		3	A
Line regulation	I_O = 3 A, V_{IN} = 8 V to 17 V			± 0.02		%
Load regulation	V_{IN} = 12 V, I_O = 0 A to 3 A			± 0.02		%
Load transient response	I_O = 0.75 A to 1.5 A	Voltage change		90		mV
		Recovery time		70		µs
	I_O = 1.5 A to 0.75 A	Voltage change		80		mV
		Recovery time		70		µs
Loop bandwidth	V_{IN} = 12 V, I_O = 3 A			32.1		kHz
Phase margin	V_{IN} = 12 V , I_O = 3 A			82		°
Input ripple voltage	I_O = 3 A			480		mV_{PP}
Output ripple voltage	I_O = 3 A			10		mV_{PP}
Output rise time				3.5		ms
Operating frequency				480		kHz
Maximum efficiency	TPS54320EVM-513, V_{IN} = 8 V, I_O = 0.9 A			94.9		%

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54320. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

The output voltage is set by the resistor divider network of R8 and R9. R9 is fixed at 10 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R8. Changing the value of R8 can change the output voltage above 0.8 V. The value of R8 for a specific output voltage can be calculated using Equation 1.

$$R8 = \frac{10\ k\Omega \left(V_{OUT} - 0.8\ V\right)}{0.8\ V} \tag{1}$$

Table 1-3 lists the R8 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 135 ns, and the maximum duty cycle is less than 95%. The values given in Table 1-3 are standard values, not the exact value calculated using Equation 1.

Table 1-3. Output Voltages Available

Output Voltage (V)	R_8 Value (kΩ)
1.8	12.4
2.5	21.5
3.3	31.6
5	52.3

1.3.2 Slow Start Time

The slow start time can be adjusted by changing the value of C7. Use Equation 2 to calculate the required value of C7 for a desired slow start time

$$C7(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)} \tag{2}$$

The EVM is set for a slow start time of 3.5 msec using C7 = 0.01 µF.

1.3.3 Track In

The TPS54320 can track an external voltage during start up. The J5 connector is provided to allow connection to that external voltage. Ratio-metric or simultaneous tracking can be implemented using resistor divider R5 and R6. See the TPS54320 data sheet (SLVS982) for details.

1.3.4 Adjustable UVLO

The under voltage lock out (UVLO) can be adjusted externally using R1 and R2. The EVM is set for a start voltage of 6.528 V and a stop voltage of 6.190 V using R1 = 511 kΩ and R2 = 100 kΩ. Use Equation 3 and Equation 4 to calculate the required resistor values for different start and stop voltages.

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \tag{3}$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \tag{4}$$

1.3.5 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected together using a jumper across JP1. The single input voltage is supplied at J1. If desired, these two input voltage rails may be separated by removing the jumper across JP1. Two input voltages, which could be at different voltages, must then be provided at both J1 and J2.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54320 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The TPS54320 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 2 A must be connected to J1 through a pair of 20 AWG wires. The jumper across JP1 must be in place. See Section 1.3.5 for split input voltage rail operation. The load must be connected to J3 through a pair of 20 AWG wires. The maximum load current capability must be 3 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP8 is used to monitor the output voltage with TP9 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	PVIN input voltage connector. (see Table 1-1 for V_{IN} range).
J2	VIN input voltage connector. Not normally used.
J3	V_{OUT}, 3.3 V at 3 A maximum.
J4	2-pin header for tracking output and ground.
J5	2-pin header for tracking voltage input and ground.
JP1	PVIN to VIN jumper. Normally closed to tie VIN to PVIN for common rail voltage operation.
JP2	2-pin header for enable. Connect EN to ground to disable, open to enable.
TP1	PVIN test point at PVIN connector.
TP2	GND test point at PVIN connector.
TP3	VIN test point at VIN connector.
TP4	GND test point at VIN connector.
TP5	PH test point.
TP6	Slow start / track in test point.
TP7	Test point between voltage divider network and output. Used for loop response measurements.
TP8	Output voltage test point at V_{OUT} connector.
TP9	GND test point at V_{OUT} connector.
TP10	PWRGD test point.

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.9 A and then decreases as the load current increases towards full load. Figure 2-1 shows the efficiency for the TPS54320 at an ambient temperature of 25°C.

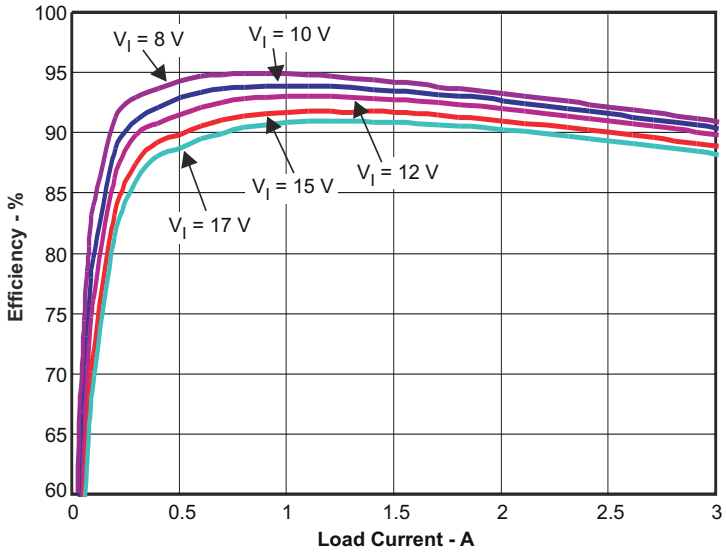

Figure 2-1. TPS54320 Efficiency

Figure 2-2 shows the efficiency for the TPS54320 at lower output currents below 0.20 A at an ambient temperature of 25°C.

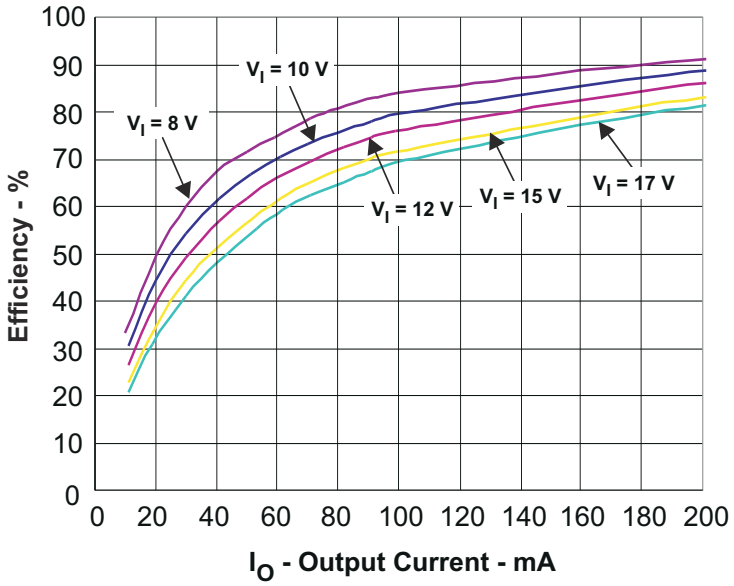

Figure 2-2. TPS54320 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 2-3 shows the load regulation for the TPS54320.

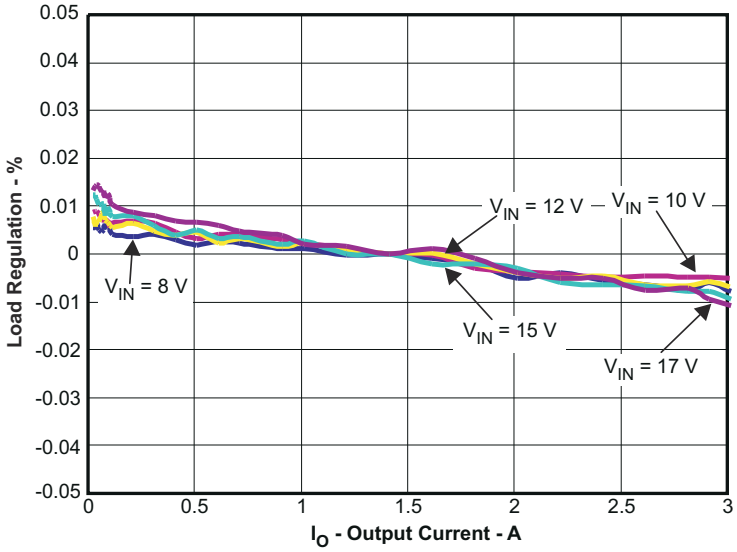

Figure 2-3. TPS54320 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-4 shows the line regulation for the TPS54320.

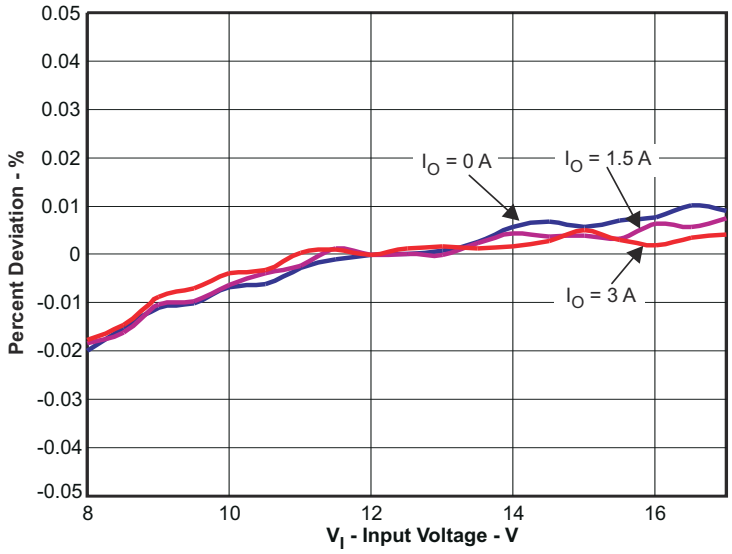

Figure 2-4. TPS54320 Line Regulation

2.5 Load Transients

Figure 2-5 shows the TPS54320 response to load transients. The current step is from 25% to 50% of maximum rated load at 12 V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

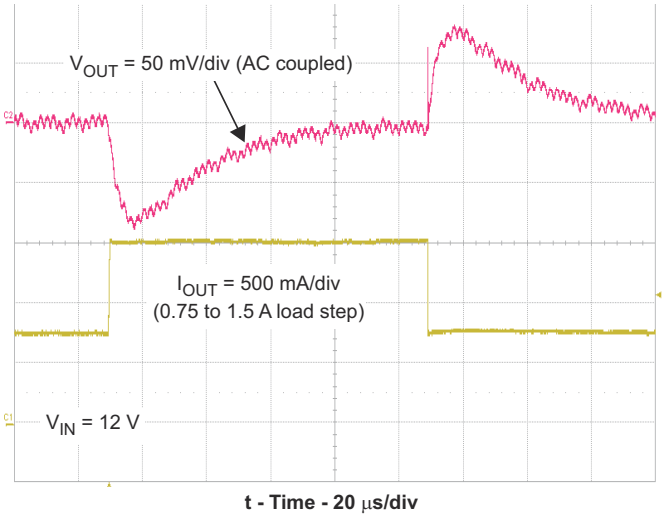

Figure 2-5. TPS54320 Transient Response

2.6 Loop Characteristics

Figure 2-6 shows the TPS54320 loop-response characteristics. Gain and phase plots are shown for V_{IN} of 12 V. Load current for the measurement is 3 A.

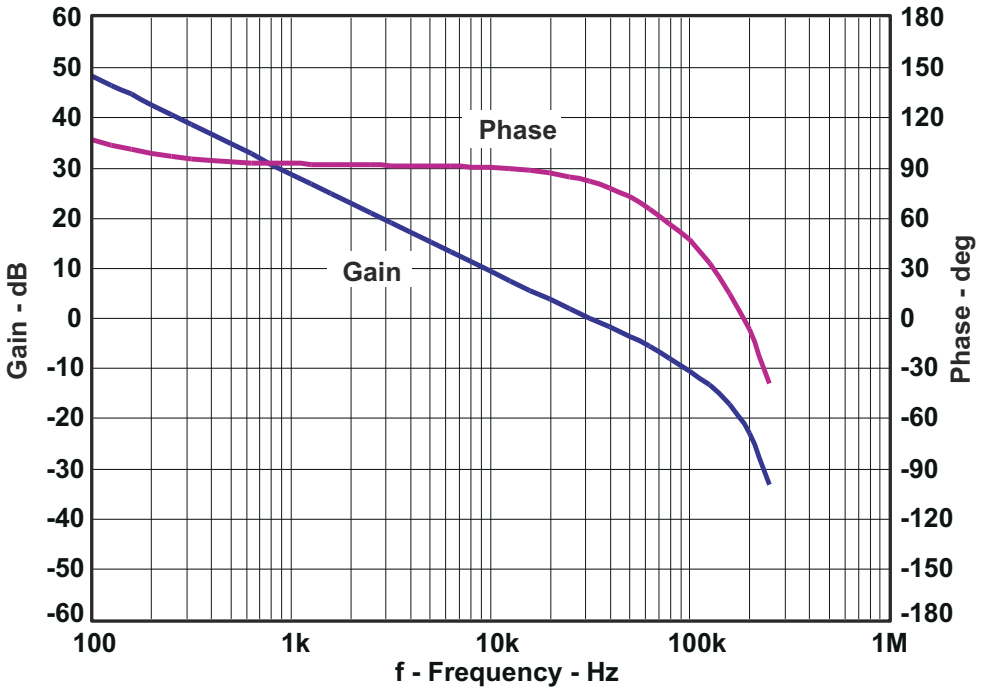

Figure 2-6. TPS54320 Loop Response

2.7 Output Voltage Ripple

Figure 2-7 shows the TPS54320 output voltage ripple. The output current is the rated full load of 3 A and V_{IN} = 12 V. The ripple voltage is measured directly across the output capacitors with a low inductance probe. Measuring at the output test points, TP8 and TP9, can pick up some radiated noise and give an erroneous measurement.

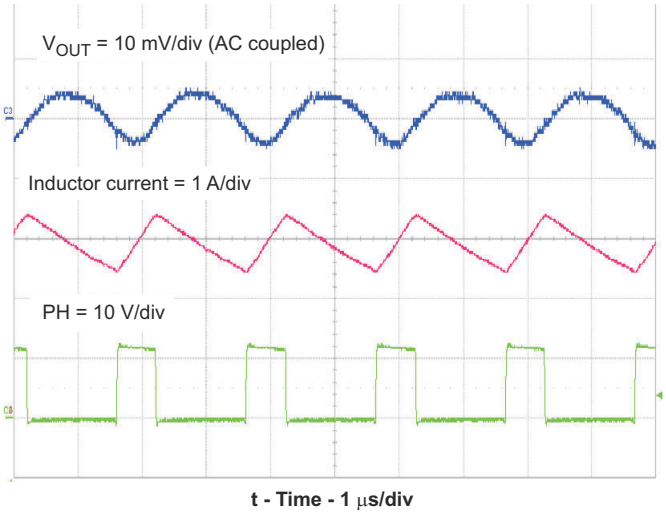

Figure 2-7. TPS54320 Output Ripple

2.8 Input Voltage Ripple

Figure 2-8 shows the TPS54320 input voltage. The output current is the rated full load of 3 A and V_{IN} = 12 V. The ripple voltage is measured directly across the input capacitors.

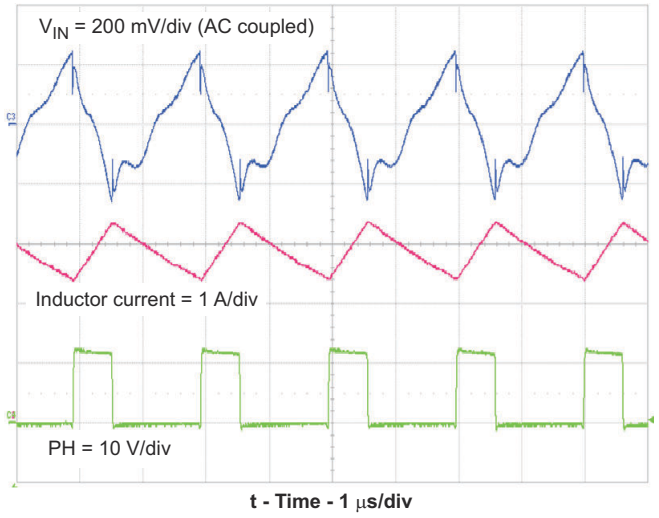

Figure 2-8. TPS54320 Input Ripple

2.9 Powering Up

Figure 2-9 and Figure 2-10 show the start-up waveforms for the TPS54320. In Figure 2-9, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1 and R2 resistor divider network. In Figure 2-10, the input voltage is initially applied and the output is inhibited by using a jumper at JP2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 12 V and the load is 1.1Ω.

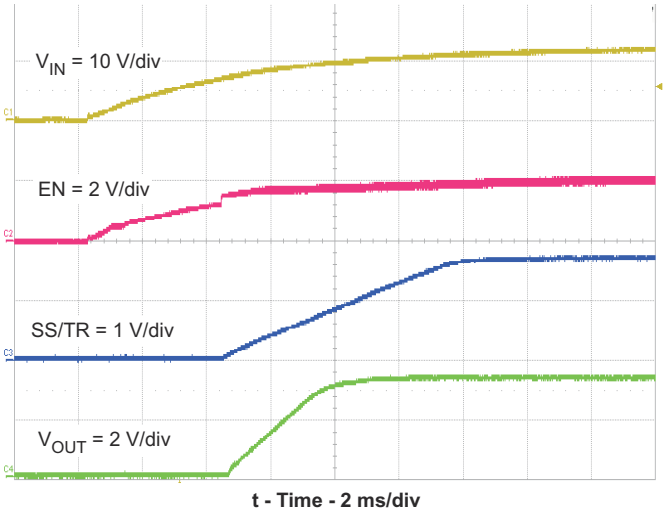

Figure 2-9. TPS54320 Start-Up Relative to V_{IN}

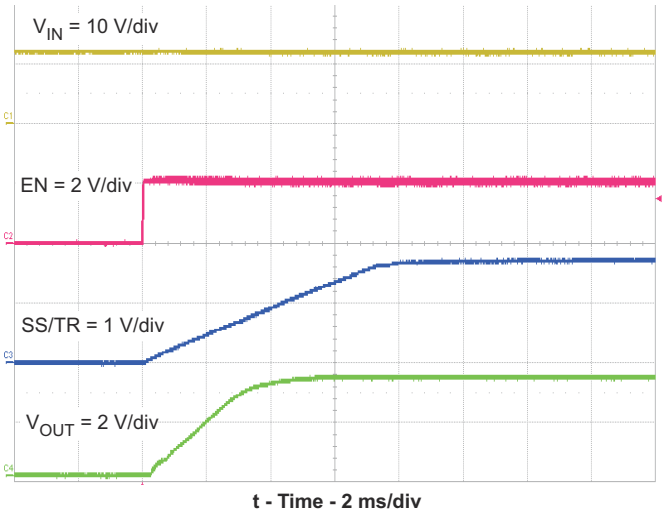

Figure 2-10. TPS54320 Start-Up Relative to Enable

2.10 Thermal Characteristics

This section shows a thermal image of the TPS54320 running at 12 V input and 3 A load. there is no air flow and the ambient temperature is 25°C. The peak temperature of the IC (59.5°C) is well below the maximum recommended operating condition listed in the data sheet of 150°C.

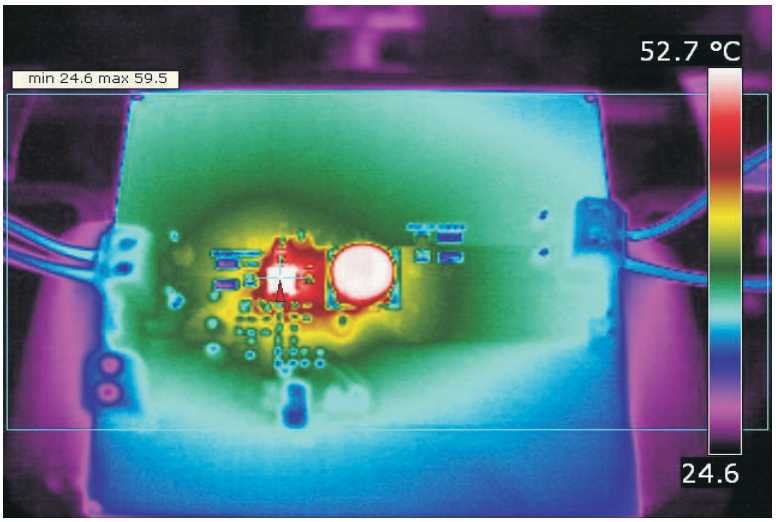

Figure 2-11. TPS54320 Thermal Image

3 Board Layout

This section provides a description of the TPS54320, board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54320 is shown in Figure 3-1 through Figure 3-3. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for PVIN, VIN, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54320 and a large area filled with ground. The bottom ground layer contains a ground plane only. The top side ground traces are connected to the bottom ground plane with multiple vias placed around the board including nine vias directly under the TPS54320 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C2, and C3) and bootstrap capacitor (C5) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the J3 output connector. For the TPS54320, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage setpoint divider, frequency set resistor, slow start capacitor and compensation components are terminated to ground using a wide ground trace separate from the power ground pour.

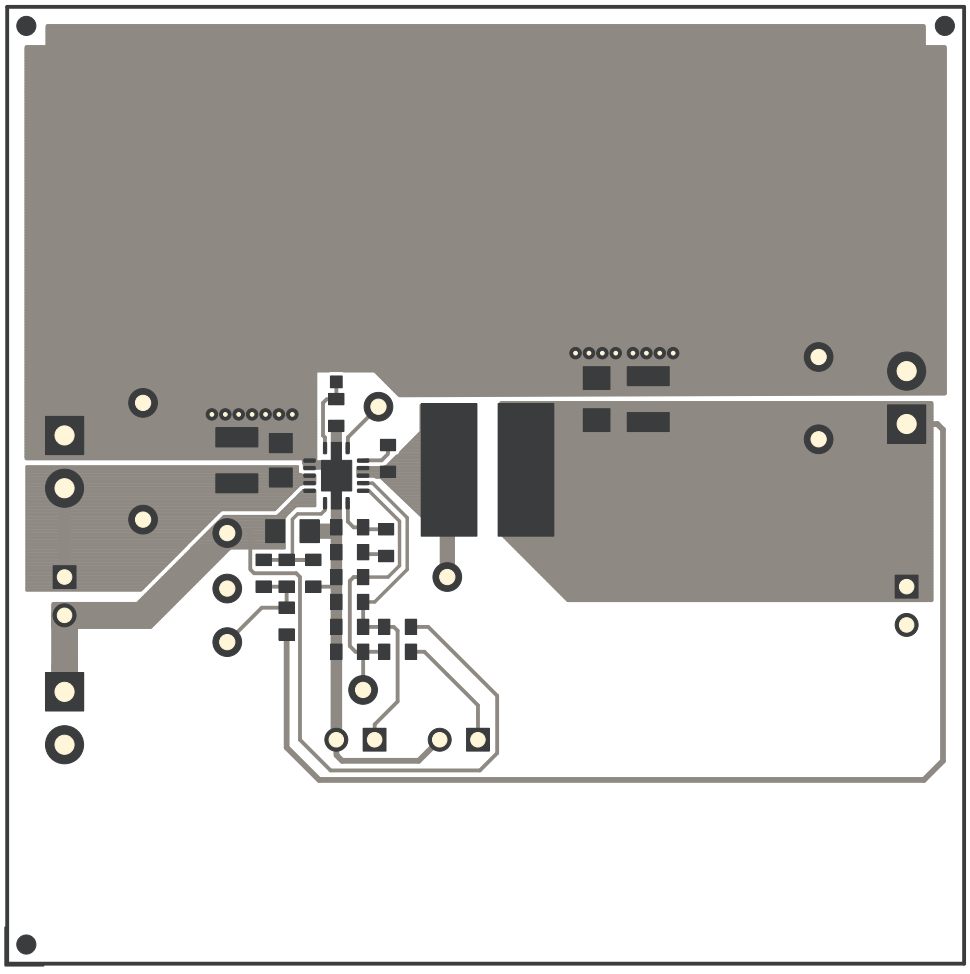

Figure 3-1. TPS54320 Top-Side Layout

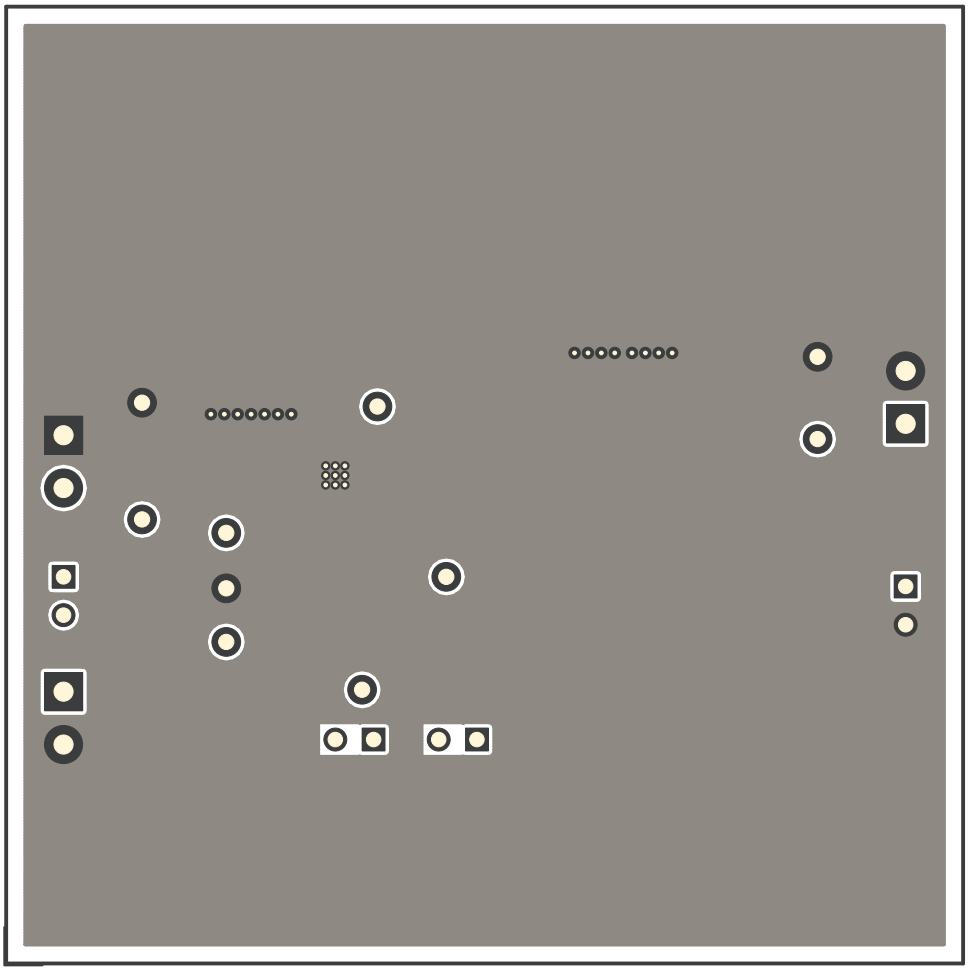

Figure 3-2. TPS54320 Bottom-Side Layout

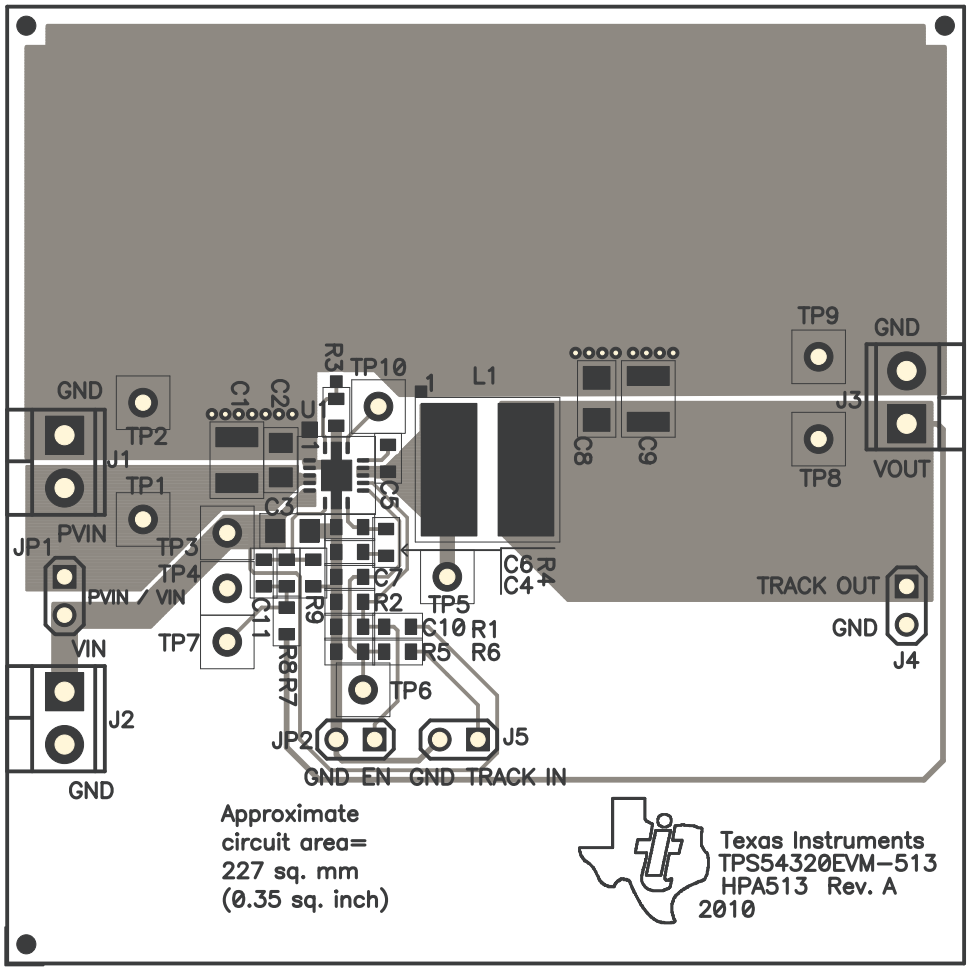

Figure 3-3. TPS54320 Top-Side Assembly

3.2 Estimated Circuit Area

The estimated printed circuit board area for the components used in this design is 0.35 in^2 (227 mm^2). This area does not include test point or connectors.

4 Schematic and Bill of Materials

This section presents the TPS54320 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54320.

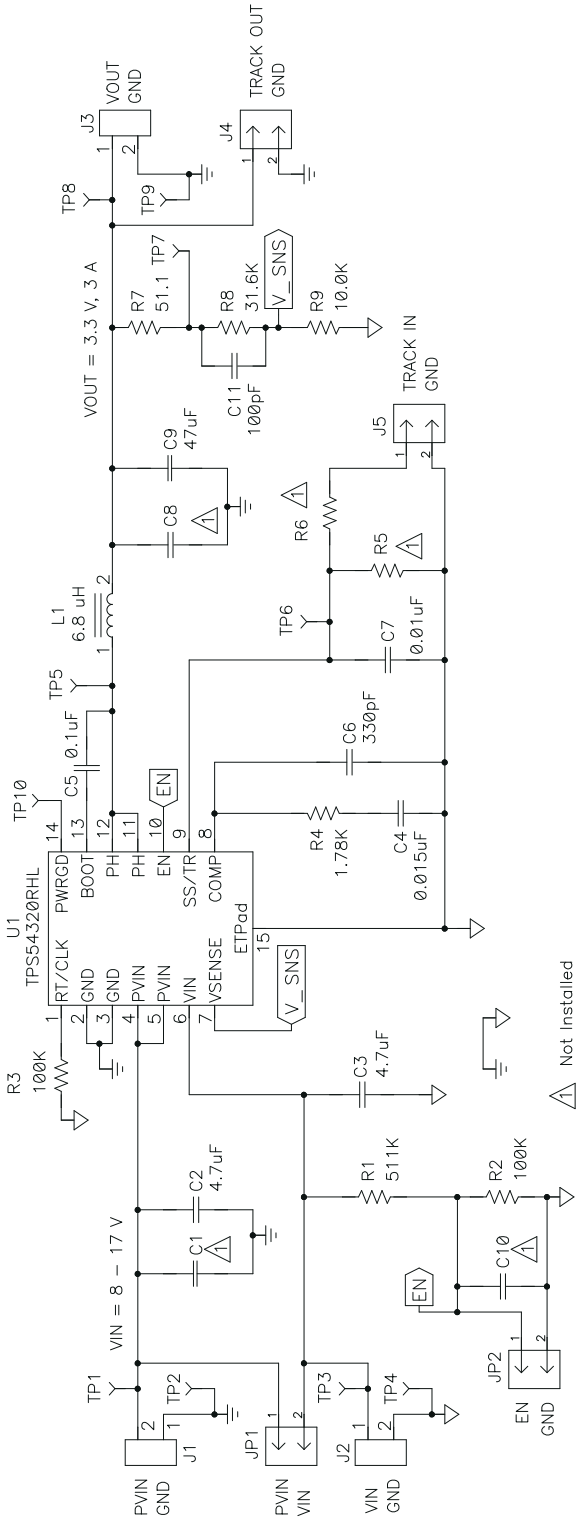

Figure 4-1. TPS54320EVM-513 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54320.

Table 4-1. TPS54320 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C2, C3	4.7µF	Capacitor, Ceramic, 25V, X5R, 10%	0805	Std	Std
1	C4	0.015µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C5	0.1µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C6	330pF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
1	C7	0.01µF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
1	C9	47µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	Std	Std
1	C11	100pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std
1	L1	6.8 µH	Inductor, SMT, 3.6A, 24 milliohm	8.7 mm x 8.6 mm	VLP8040T-6R8M	TDK
1	R1	511KΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R2, R3	100KΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	1.78KΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	51.1Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	31.6KΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	10.0KΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS54320RHL	IC, 17V Input, 3A Output, Sync. Step Down Switcher with Integrated FET	QFN14	TPS54320RHL	TI

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2010) to Revision A (October 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title..... 2

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