

**ABSTRACT**

This user's guide contains information for the TPS54328 as well as support documentation for the TPS54328EVM-686 evaluation module. Included are the performance specifications, schematic, and the bill of materials of the TPS54328EVM-686.

**Table of Contents**

<b>1 Introduction</b> .....	3
<b>2 Performance Specification Summary</b> .....	4
<b>3 Modifications</b> .....	5
3.1 Output Voltage Setpoint.....	5
3.2 Output Filter and Closed Loop Response.....	5
<b>4 Test Setup and Results</b> .....	6
4.1 Input/Output Connections.....	7
4.2 Start-Up Procedure.....	7
4.3 Efficiency.....	8
4.4 Load Regulation.....	9
4.5 Line Regulation.....	10
4.6 Load Transient Response.....	10
4.7 Output Voltage Ripple.....	11
4.8 Input Voltage Ripple.....	12
4.9 Start-Up.....	13
<b>5 Board Layout</b> .....	14
5.1 Layout.....	14
<b>6 Schematic, Bill of Materials, and Reference</b> .....	17
6.1 Schematic.....	17
6.2 Bill of Materials.....	17
6.3 Reference.....	17
<b>7 Revision History</b> .....	18

**List of Figures**

Figure 4-1. TPS54328EVM-686 Efficiency.....	8
Figure 4-2. TPS54328EVM-686 Light Load Efficiency.....	8
Figure 4-3. TPS54328EVM-686 Load Regulation, $V_{IN} = 5$ V.....	9
Figure 4-4. TPS54328EVM-686 Load Regulation, $V_{IN} = 12$ V.....	9
Figure 4-5. TPS54328EVM-686 Line Regulation.....	10
Figure 4-6. TPS54328EVM-686 Load Transient Response.....	10
Figure 4-7. TPS54328EVM-686 Output Voltage Ripple.....	11
Figure 4-8. TPS54328EVM-686 Eco-mode™ Output Voltage Ripple.....	11
Figure 4-9. TPS54328EVM-686 Input Voltage Ripple.....	12
Figure 4-10. TPS54328EVM-686 Start-Up Relative to $V_{IN}$ .....	13
Figure 4-11. TPS54328EVM-686 Start-Up Relative to EN.....	13
Figure 5-1. Top Assembly.....	14
Figure 5-2. Top Layer.....	15
Figure 5-3. Bottom Layer.....	15
Figure 5-4. Bottom Assembly.....	16
Figure 6-1. TPS54328EVM-686 Schematic Diagram.....	17

---

<b>List of Tables</b>	
Table 1-1. Input Voltage and Output Current Summary.....	3
Table 2-1. TPS54328EVM-686 Performance Specifications Summary.....	4
Table 3-1. Output Voltages.....	5
Table 4-1. Connection and Test Points.....	7
Table 6-1. Bill of Materials.....	17

## Trademarks

SWIFT™ and D-CAP2™ are trademarks of Texas Instruments.

Eco-mode™ are trademarks of TI.

All trademarks are the property of their respective owners.

## 1 Introduction

The TPS54328 is a single, adaptive on-time, D-CAP2™-mode, synchronous buck converter requiring a very low external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 700 kHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS54328 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS54328 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS54328 also features auto-skip Eco-mode for improved light load efficiency. The TPS54328 DC/DC synchronous converter is designed to provide up to a 3-A output from an input voltage source of 4.5 V to 18 V. The output voltage range is from 0.76 V to 7.0 V. Rated input voltage and output current range for the evaluation module are given in [Table 1-1](#).

The TPS54328EVM-686 evaluation module is a single, synchronous buck converter providing 1.05 V at 3 A from 4.5-V to 18-V input. This user's guide describes the TPS54328EVM-686 performance.

**Table 1-1. Input Voltage and Output Current Summary**

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54328EVM-686	$V_{IN} = 4.5 \text{ V to } 18 \text{ V}$	0 A to 3 A

## 2 Performance Specification Summary

A summary of the TPS54328EVM-686 performance specifications is provided in [Table 2-1](#). Specifications are given for an input voltage of  $V_{IN} = 12$  V and an output voltage of 1.05 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

**Table 2-1. TPS54328EVM-686 Performance Specifications Summary**

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range ( $V_{IN}$ )		4.5	12	18	V
Output voltage			1.05		V
Operating frequency	$V_{IN} = 12$ V, $I_O = 1$ A		675		kHz
Output current range		0		3	A
Line regulation	$I_O = 1.5$ A		+/- 0.2		%
Load regulation	$V_{IN} = 12$ V		+1.1/- 0.03		%
Over current limit	$V_{IN} = 12$ V, $L_O = 1.5$ $\mu$ H	3.5	4.2	5.7	A
Output ripple voltage	$V_{IN} = 12$ V, $I_O = 3$ A		15		mV <sub>PP</sub>
Maximum efficiency	$V_{IN} = 5$ V, $I_O = 0.5$ A		86.9		%

## 3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54328. Some modifications can be made to this module.

### 3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.765 V. The value of R1 for a specific output voltage can be calculated using [Equation 1](#).

For output voltage from 0.76 V to 7.0 V:

$$V_O = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

[Table 3-1](#) lists the R1 values for some common output voltages. For higher output voltages of 1.8 V or above, a feedforward capacitor (C4) may be required to improve phase margin. Pads for this component (C4) are provided on the printed-circuit board. Note that the values given in [Table 3-1](#) are standard values and not the exact value calculated using [Table 3-1](#).

**Table 3-1. Output Voltages**

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L1 (μH)	C9, C10, C11 TOTAL CAPACITANCE (μF)
1.0	6.81	22.1		1.5	22 - 68
1.05	8.25	22.1		1.5	22 - 68
1.2	12.7	22.1		1.5	22 - 68
1.8	30.1	22.1	5 - 22	2.2	22 - 68
2.5	49.9	22.1	5 - 22	2.2	22 - 68
3.3	73.2	22.1	5 - 22	2.2	22 - 68
5.0	124	22.1	5 - 22	3.3	22 - 68
6.5	165	22.1	5 - 22	3.3	22 - 68

### 3.2 Output Filter and Closed Loop Response

The TPS54328 relies on the output filter characteristics to ensure stability of the control loop. The recommended output filter components for common output voltages are given in [Table 3-1](#). It may be possible for other output filter component values to provide acceptable closed loop characteristics. R3 and TP4 are provided for convenience in breaking the control loop and measuring the closed loop response.

## 4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54328EVM-686. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

## 4.1 Input/Output Connections

The TPS54328EVM-686 is provided with input/output connectors and test points as shown in [Table 4-1](#). A power supply capable of supplying 2 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J2 through a pair of 20 AWG wires. The maximum load current capability is 3 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the  $V_{IN}$  input voltages with TP2 providing a convenient ground reference. TP8 is used to monitor the output voltage with TP9 as the ground reference.

**Table 4-1. Connection and Test Points**

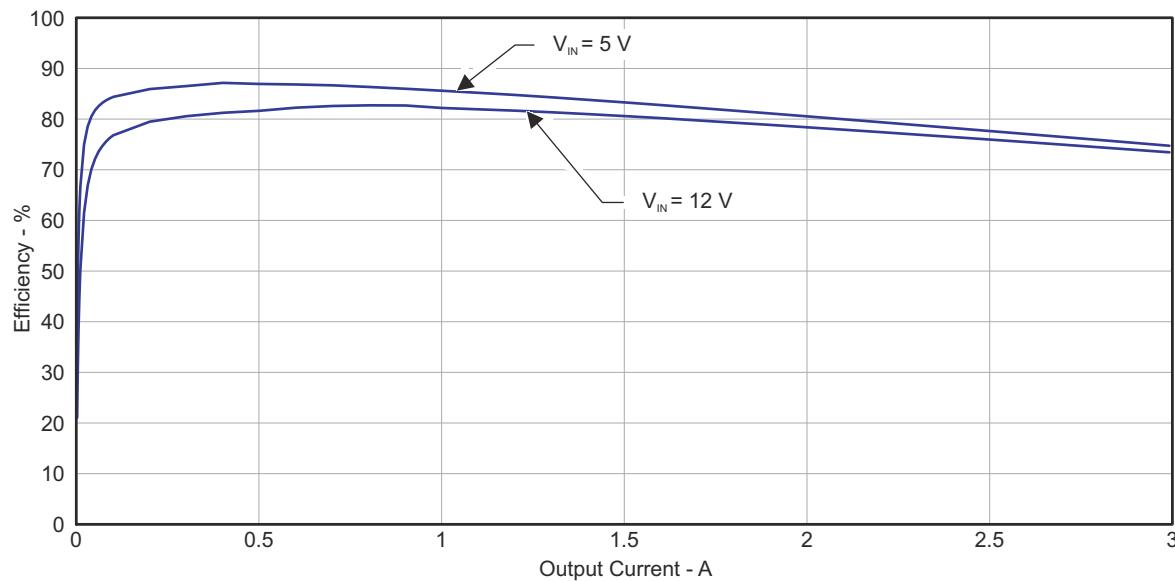
REFERENCE DESIGNATOR	FUNCTION
J1	$V_{IN}$ (see <a href="#">Table 1-1</a> for $V_{IN}$ range)
J2	$V_{OUT}$ , 1.05 V at 3 A maximum.
JP1	EN control. Connect EN to OFF to disable, connect EN to ON to enable.
TP1	$V_{IN}$ test point at $V_{IN}$ connector.
TP2	GND test point at $V_{IN}$ .
TP3	EN test point.
TP4	Loop response measurement test point.
TP5	VREG5 test point.
TP6	Switch node test point.
TP7	Analog ground test point.
TP8	Output voltage test point.
TP9	Ground test point at output connector.

## 4.2 Start-Up Procedure

1. Ensure that the jumper at JP1 (Enable control) is set from EN to OFF.
2. Apply appropriate VIN voltage to VIN and PGND terminals at J1.
3. Move the jumper at JP1 (Enable control) to cover EN and ON. The EVM enables the output voltage.

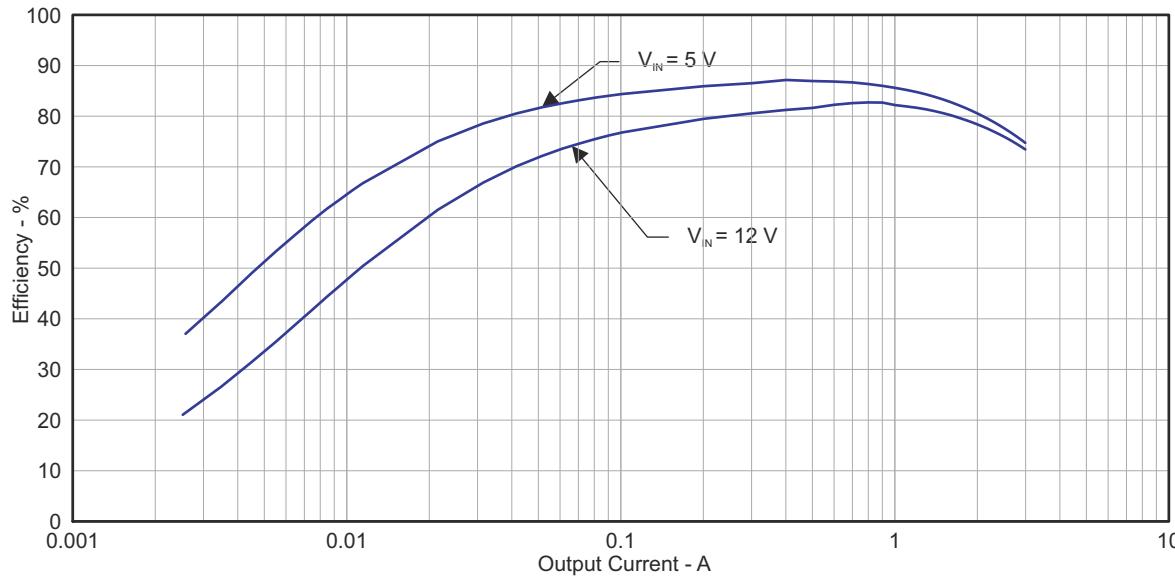
### 4.3 Efficiency

Figure 4-1 shows the efficiency for the TPS54328EVM-686 at an ambient temperature of 25°C.



**Figure 4-1. TPS54328EVM-686 Efficiency**

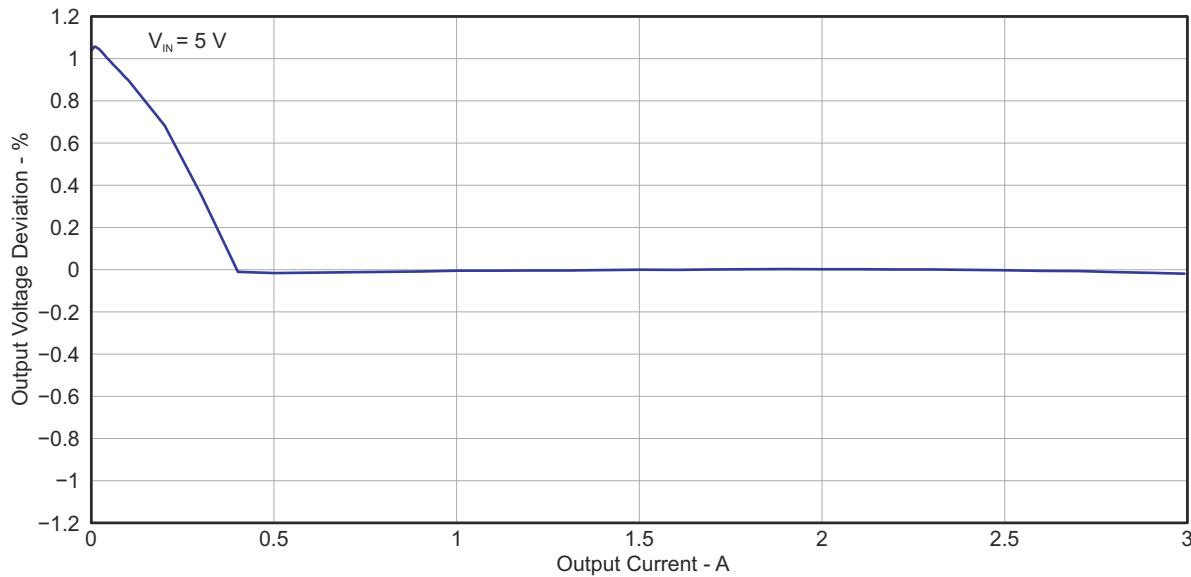
Figure 4-2 shows the efficiency at light loads for the TPS54328EVM-686 at an ambient temperature of 25°C.



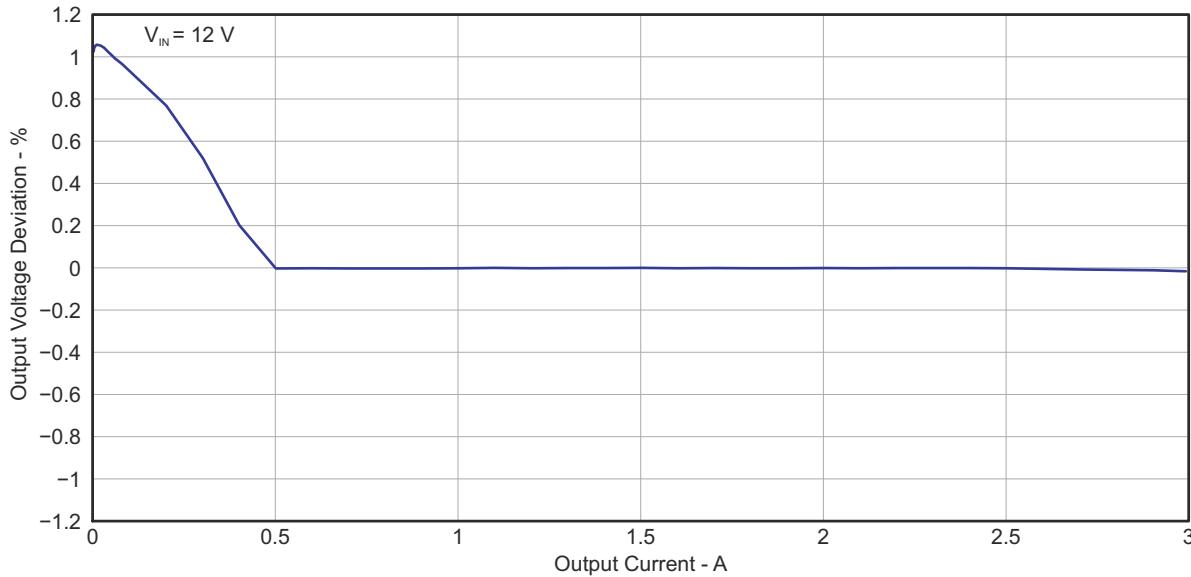
**Figure 4-2. TPS54328EVM-686 Light Load Efficiency**

## 4.4 Load Regulation

The load regulation for the TPS54328EVM-686 is shown in [Figure 4-3](#) and [Figure 4-4](#).



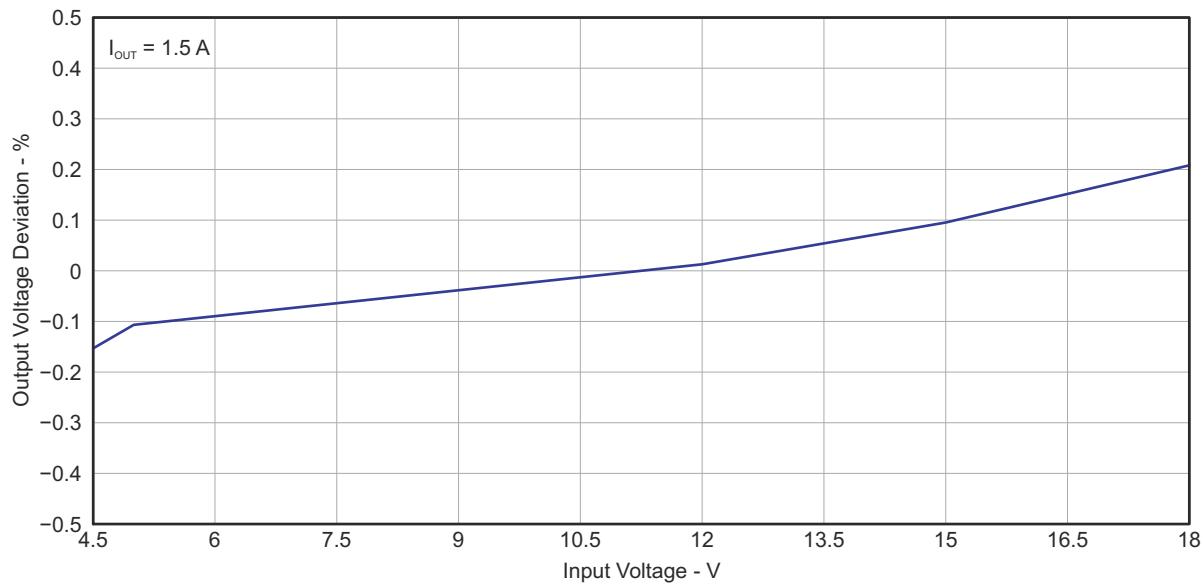
**Figure 4-3. TPS54328EVM-686 Load Regulation,  $V_{IN} = 5\text{ V}$**



**Figure 4-4. TPS54328EVM-686 Load Regulation,  $V_{IN} = 12\text{ V}$**

## 4.5 Line Regulation

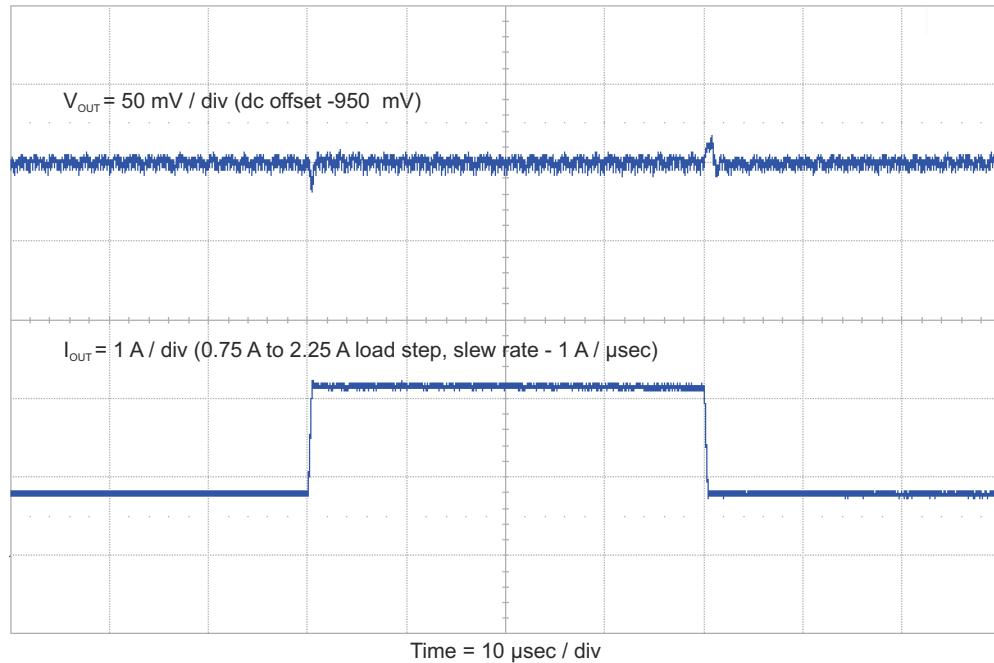
The line regulation for the TPS54328EVM-686 is shown in [Figure 4-5](#).



**Figure 4-5. TPS54328EVM-686 Line Regulation**

## 4.6 Load Transient Response

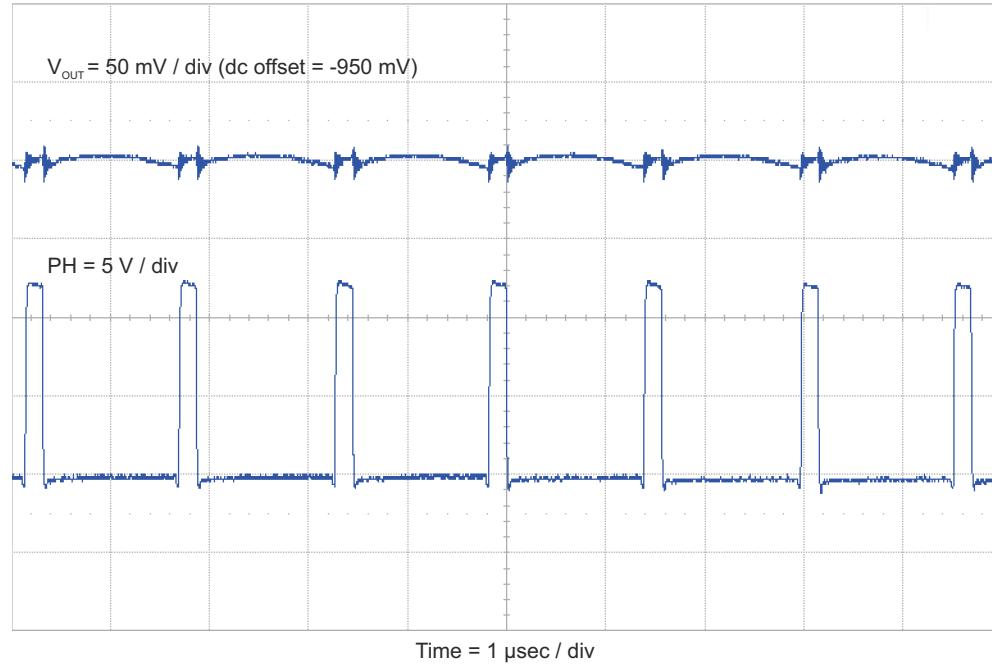
The TPS54328EVM-686 response to load transient is shown in [Figure 4-6](#). The current step is from 0.75 A to 2.25 A. Total peak-to-peak voltage variation is as shown.



**Figure 4-6. TPS54328EVM-686 Load Transient Response**

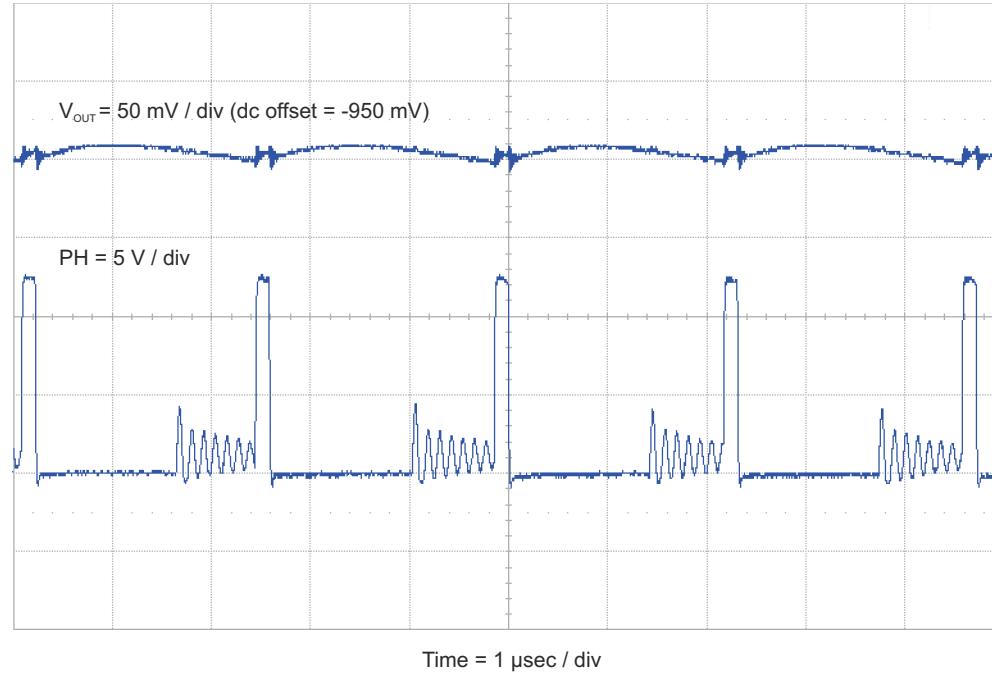
## 4.7 Output Voltage Ripple

The TPS54328EVM-686 output voltage ripple is shown in [Figure 4-7](#). The output current is the rated full load of 3 A.



**Figure 4-7. TPS54328EVM-686 Output Voltage Ripple**

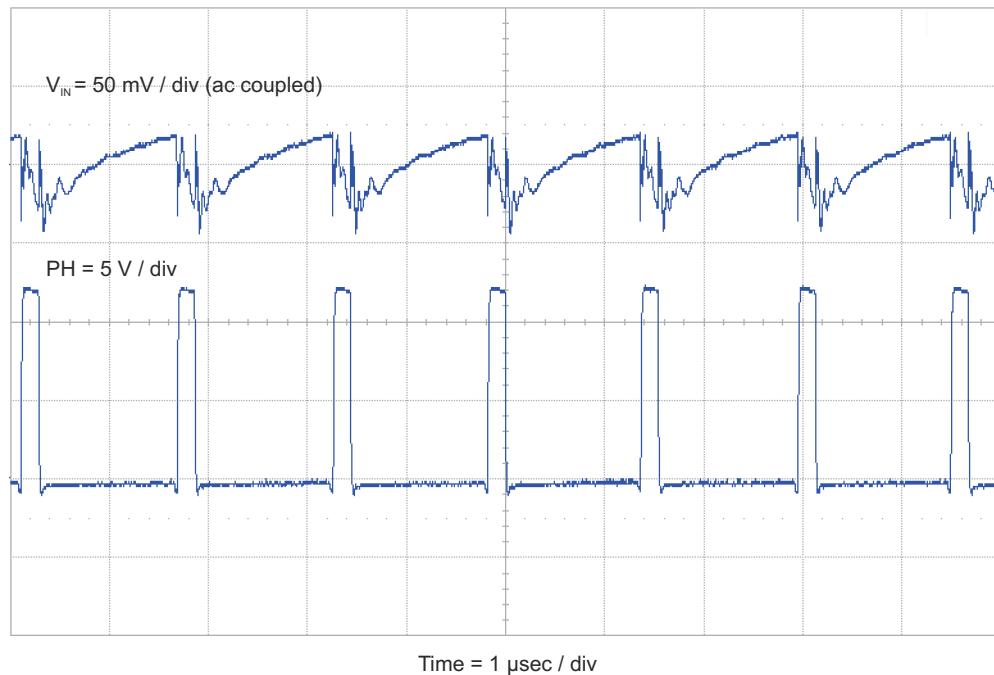
The TPS54328EVM-686 output voltage ripple during Eco-mode™ operation is shown in [Figure 4-8](#). The output current is 30 mA.



**Figure 4-8. TPS54328EVM-686 Eco-mode™ Output Voltage Ripple**

## 4.8 Input Voltage Ripple

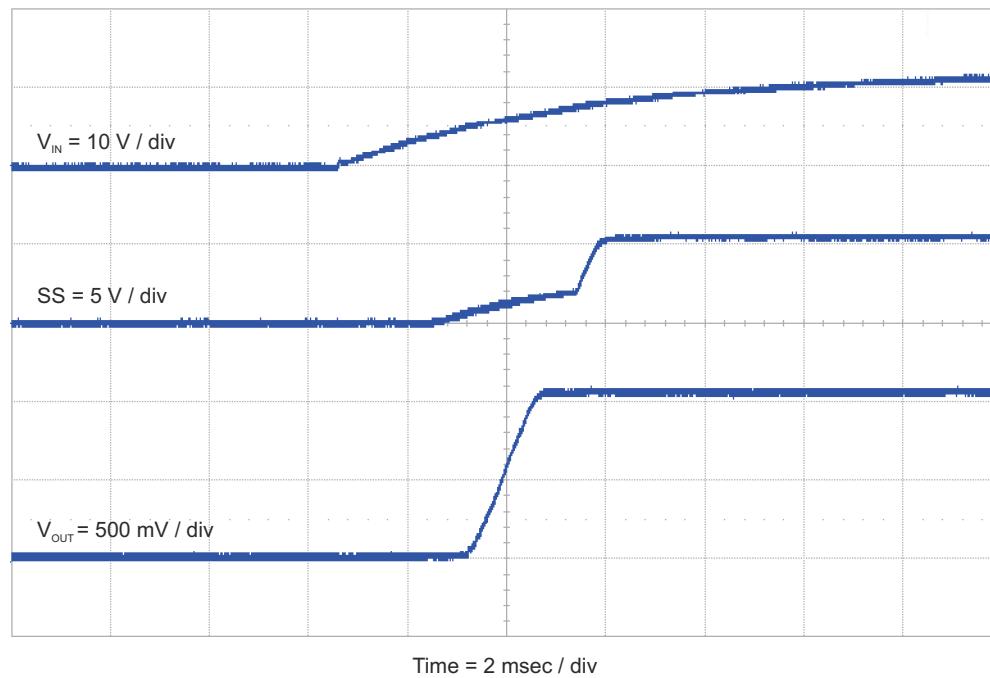
The TPS54328EVM-686 input voltage ripple is shown in [Figure 4-9](#). The output current is the rated full load of 3 A.



**Figure 4-9. TPS54328EVM-686 Input Voltage Ripple**

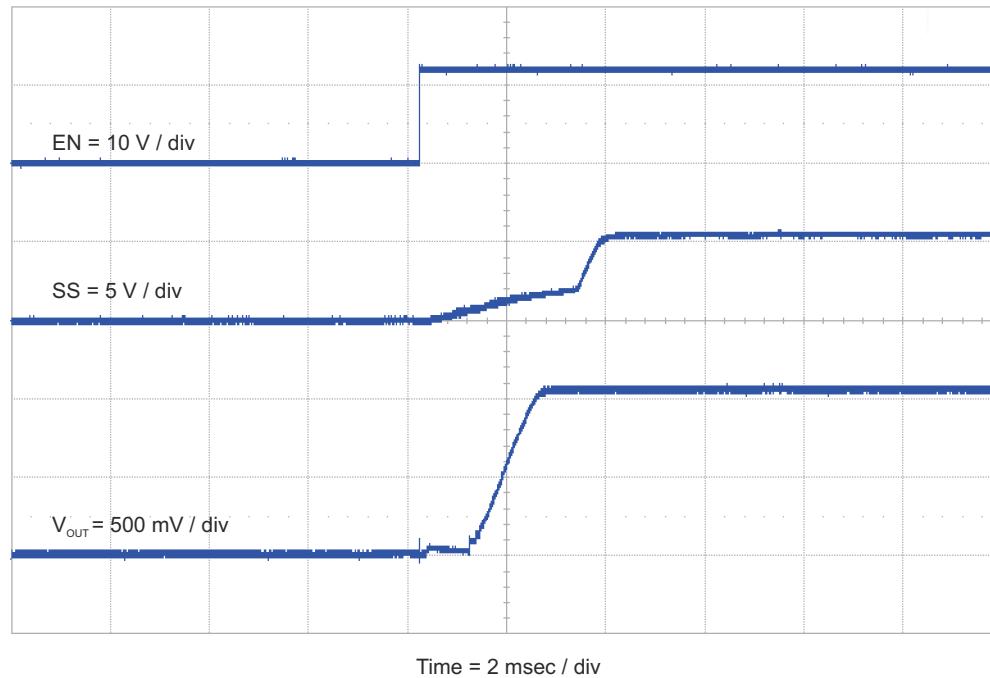
## 4.9 Start-Up

The TPS54328EVM-686 start-up waveform relative to  $V_{IN}$  is shown in [Figure 4-10](#).



**Figure 4-10. TPS54328EVM-686 Start-Up Relative to  $V_{IN}$**

The TPS54328EVM-686 start-up waveform relative to enable (EN) is shown in [Figure 4-11](#).



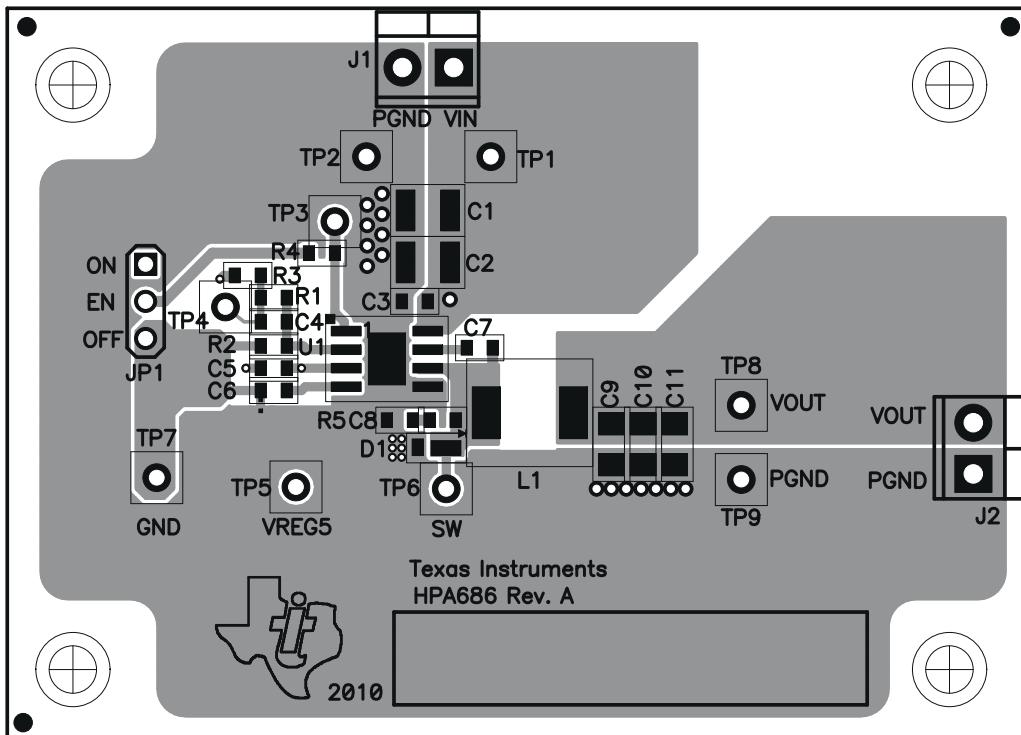
**Figure 4-11. TPS54328EVM-686 Start-Up Relative to EN**

## 5 Board Layout

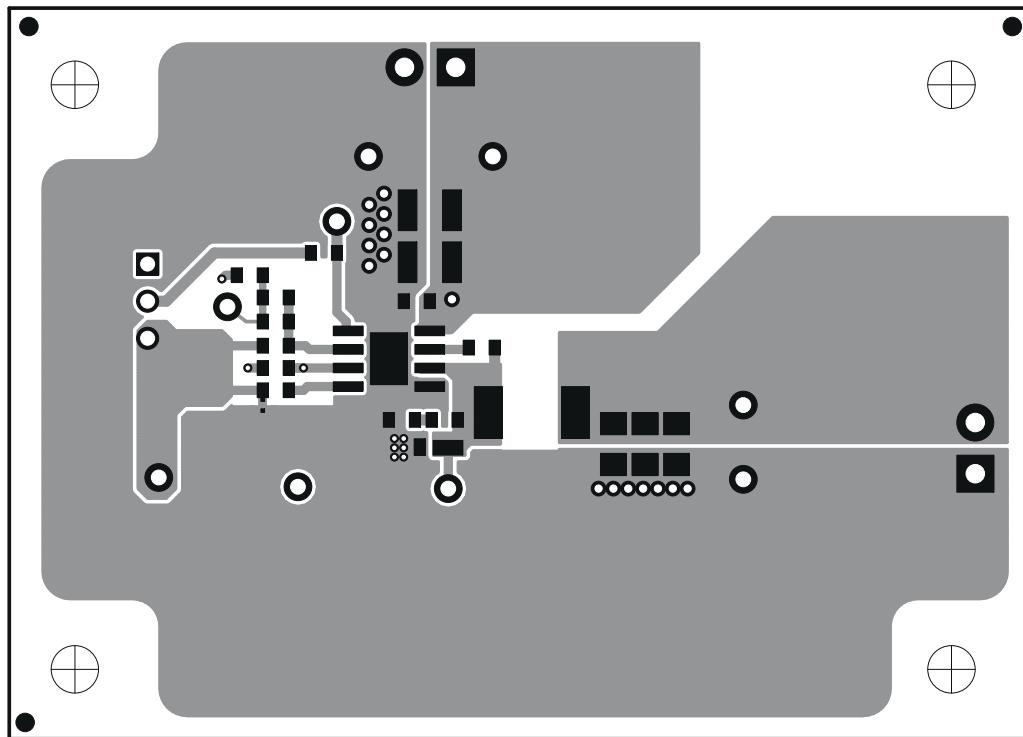
This section provides description of the TPS54328EVM-686, board layout, and layer illustrations.

### 5.1 Layout

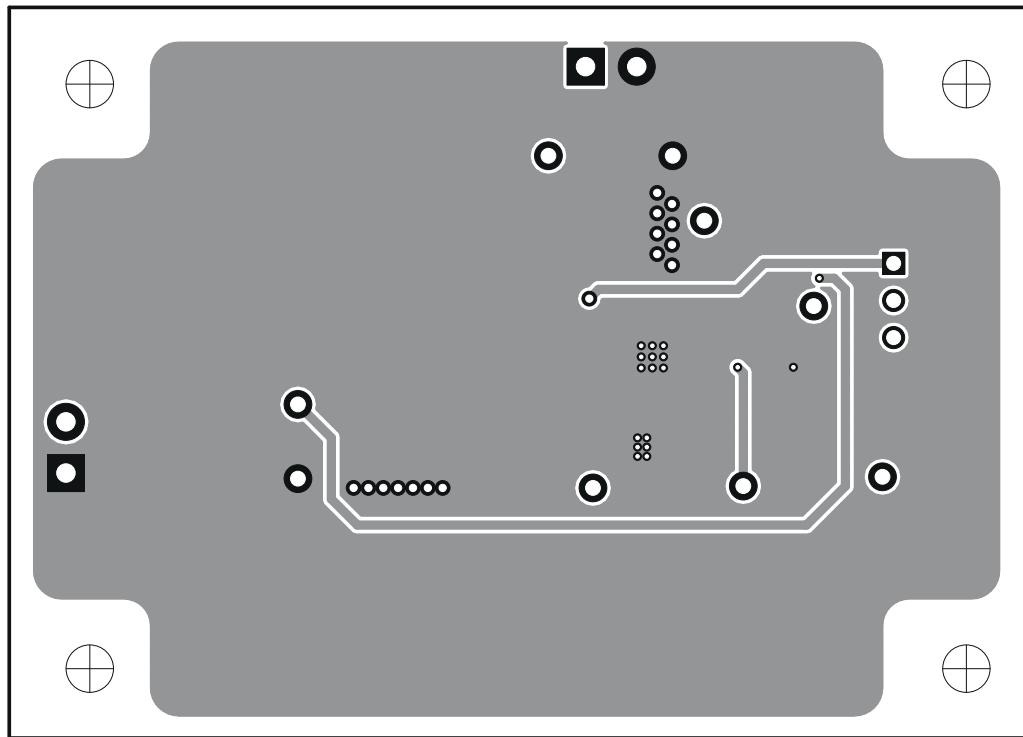
The board layout for the TPS54328EVM-686 is shown in [Figure 5-1](#) through [Figure 5-4](#). The top layer contains the main power traces for VIN, VO, and ground. Also on the top layer are connections for the pins of the TPS54328 and a large area filled with ground. Many of the signal traces also are located on the top side. The input decoupling capacitors are located as close to the IC as possible. The input and output connectors, test points, and all of the components are located on the top side. An analog ground (GND) area is provided on the top side. Analog ground (GND) and power ground (PGND) are connected at a single point on the top layer near C6. The bottom layer is primarily power ground but also has a trace to connect VIN to the enable jumper, a trace to connect VREG5 to TP5, and the feedback trace from VOUT to the voltage setpoint divider network.



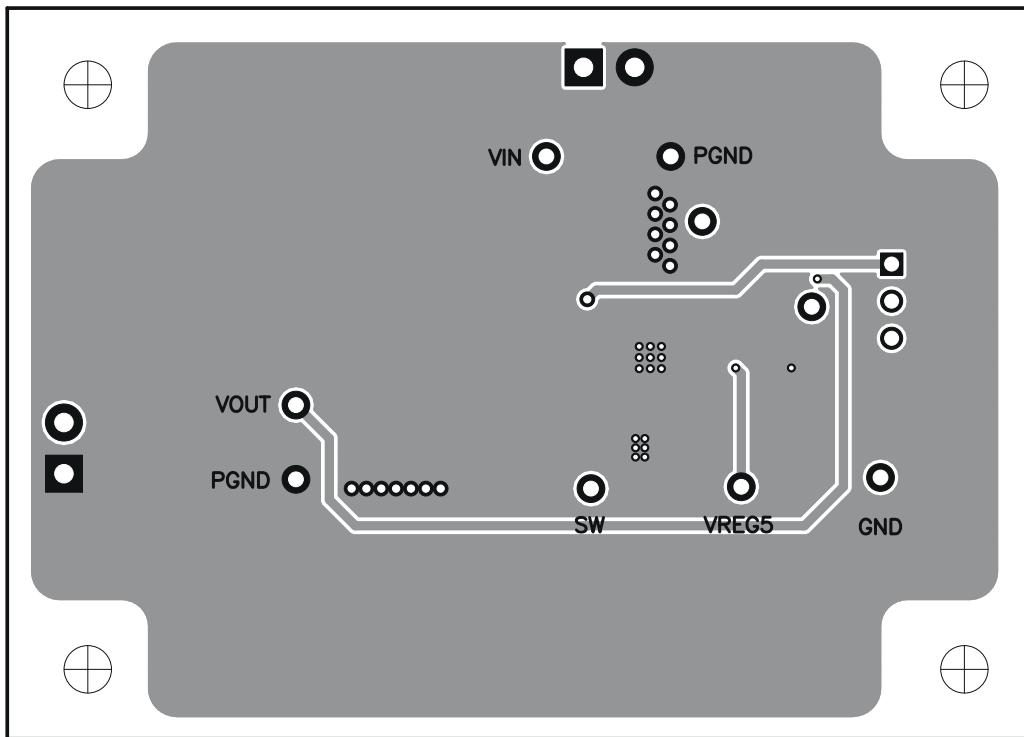
**Figure 5-1. Top Assembly**



**Figure 5-2. Top Layer**



**Figure 5-3. Bottom Layer**

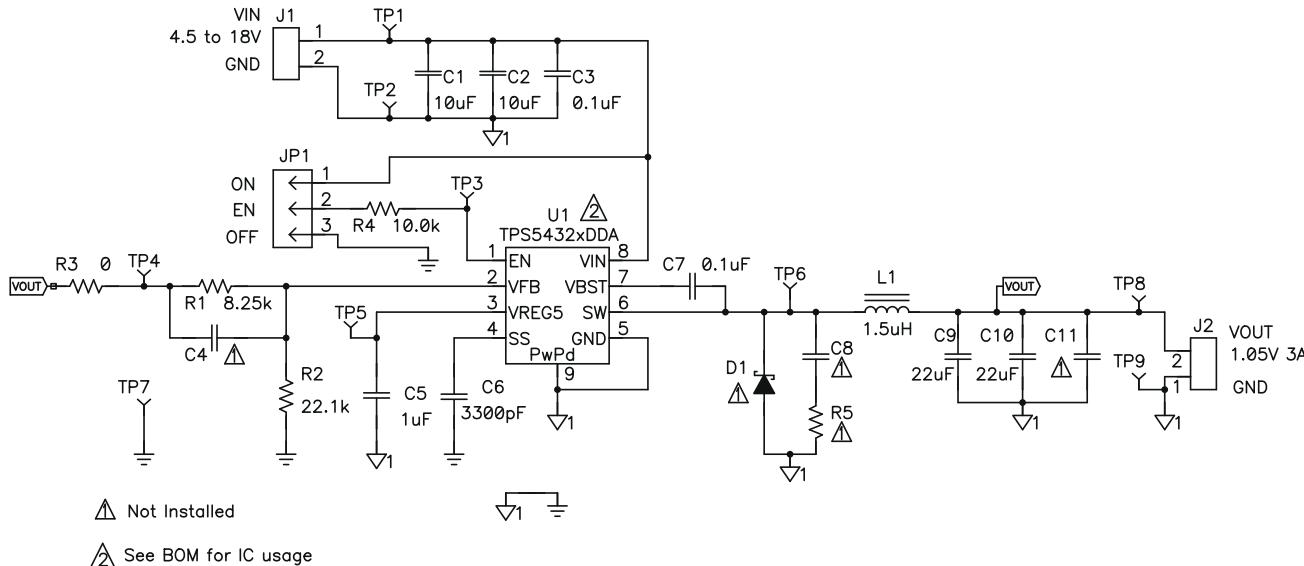


**Figure 5-4. Bottom Assembly**

## 6 Schematic, Bill of Materials, and Reference

## 6.1 Schematic

Figure 6-1 is the schematic for the TPS54328EVM-538.



**Figure 6-1. TPS54328EVM-686 Schematic Diagram**

## 6.2 Bill of Materials

**Table 6-1. Bill of Materials**

REFDES	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C1, C2	2	10uF	Capacitor, Ceramic, 25V, X5R, 20%	1210	Std	Std
C11	0	Open	Capacitor, Ceramic	1206	Std	Std
C3, C7	2	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
C4, C8	1	Open	Capacitor, Ceramic	0603	Std	Std
C5	1	1.0uF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
C6	1	3300pF	Capacitor, Ceramic, 25V, X7R , 10%	0603	Std	Std
C9, C10	2	22uF	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	C3216X5R0J226M	TDK
J1, J2	2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	Sullins
JP1	1	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
L1	1	1.5uH	Inductor, SMT, 11 A, 9.7 mΩ	0.256 x 0.280 inch	SPM6530T-1R5M100	TDK
R1	1	8.25k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R2	1	22.1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R3	1	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R4	1	10.0k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R5	0	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
TP1, TP3, TP4, TP5, TP6, TP8	3	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
TP2, TP7, TP9	3	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
U1	1	TPS54328DDA	IC, 3-A Output Single Sync. Step-Down	SO8[DDA]	TPS54328DDA	TI
-	1		Shunt, 100-mil, Black	0.100	929950-00	3M
-	1		PCB, 2.76 In x 1.97 In x 0.062 In		HPA686	Any

## 6.3 Reference

Texas Instruments, *TPS54328, Single Synchronous Converter With Integrated High Side and Low Side MOSFET Data Sheet*

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (December 2010) to Revision A (October 2021)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document. ....	3
• Updated the user's guide title.....	3

---

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025