Evaluation Module for LM5069EVM-627 with Surge Stopper and Reverse Voltage Protection

This user's guide describes the evaluation module (EVM) for the LM5069. The LM5069 is a positive high voltage hotswap/inrush current controller with power limiting.

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1 Introduction

The LM5069EVM-627 provides the design engineer with a fully-functional hotswap controller board designed for surge clamping, reverse voltage protection and reverse current protect. This board contains an LM5069-2, the auto restart version of this IC. This user's guide describes the various functions of the board: how to test and evaluate it, and how to change the components for a specific application. For more information, view the *LM5069 Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting* (SNVS452) data sheet.

1.1 Features

- General board specifications include:
  - Input voltage range: –40 V to +38 V maximum
  - Output voltage clamped: +32 V maximum
  - Current limit: 2.5 A, ±10%
  - Q1 power limit: 30 W
  - UVLO thresholds: 16 V, ±4% and 14 V, ±3%
  - OVLO thresholds: 36 V, ±2% and 34 V, ±3%
  - Insertion delay: 410 ms
  - Fault timeout period: 26 ms
  - Restart time: 5.3 seconds
  - Size: 4.0" x 1.8"
- Reverse connection protection with diode D1
- Input surge clamping with TVS diode Z1
- Reverse current blocking from load with FET Q2
- FET SOA protection with resistor R9
- Optional FET Q3 for small input surge

1.2 Applications

- Automotive
- 24-V industrial systems
- General hot plug

2 Board Description

The schematic of LM5069EVM-627 is shown in Figure 18. Input power is applied at J1 while J2 provides the output connection to the load. Slide switch SW1 provides a means to ENABLE and shutdown the hotswap circuit with UVLO protection. Capacitors C3 and C4 (100 µF/50 V, Alum Electrolytic capacitor) represent capacitance which is typically present on the input of the load circuit and are present on this evaluation board so the turn-on characteristics of the LM5069 may be tested without having to connect a load.

The LM5069EVM-627 is supplied with pins 2–3 connected on JMP1, and pins 1–2 connected on JMP2.

3 Theory of Operation

The LM5069 provides intelligent control of the power supply connections of a load which is to be connected to a live power source. The three primary functions of this LM5069EVM-627 are reverse input voltage hookup, surge clamping and in-rush current limiting during turn-on, and reverse load current protection when pull out from power source. Additional functions include undervoltage lock-out (UVLO) and overvoltage lock-out (OVLO) to ensure the system input voltage is supplied to the load within a defined range, monitoring of the load current for faults during normal operation, power limiting in the series pass FET (Q1) during turn-on, and a power good logic output (PGD) to indicate the circuit status.

Upon applying the input voltage to the LM5069EVM-627 (for example, SW1 is switched on), Q1 is initially held off for the insertion delay (≈410 ms) to allow ringing and transients at the input to subside. At the end of the insertion delay, if the input voltage at VIN is between the UVLO and OVLO thresholds, Q1 is turned on in a controlled manner to limit the in-rush current, Q2 is also turned on controlled by GATE. If the in-rush current were not limited during turn-on, the current would be very high as the load capacitors (C3, C4) charge up, limited only by the surge current capability of the voltage source, and the wiring resistance (a few milliohms). That very high current could damage the edge connector, PC board traces, and possibly the load capacitors receiving the high current. Additionally, the dV/dt at the load's input is controlled to reduce possible EMI problems.

The LM5069EVM-627 protects from reverse connection with diode D1. When a reverse power source is connected, there will be no voltage at each pin of LM5069, as this diode can hold the reverse voltage in a range, and prevent destroying the IC.

The LM5069EVM-627 limits in-rush current to a safe level using a two-step process. In the first portion of the turn-on cycle, when the voltage differential across Q1 is highest, Q1's power dissipation is limited to a peak of 30 W by monitoring its drain current (the voltage across R5) and its drain-to-source voltage. Their product is maintained constant by controlling the drain current as the drain-to-source voltage decreases (as the output voltage increases). This is shown in the constant power portion of Figure 1 where the drain current is increasing to ILIM. When the drain current reaches the current limit threshold (2.5 A), it is then maintained constant as the output voltage continues to increase. When the output voltage reaches the input voltage (VDS decreases to near zero), the drain current then reduces to a value determined by the load. Q1's gate-to-source voltage then increases to ≈12 V above the OUT voltage. The circuit is now in normal operation mode.

Monitoring of the load current for faults during normal operation is accomplished using the current limit circuit described previously. If the load current increases to 2.5 A (55 mV across R5), Q1's gate is controlled to prevent the current from increasing further. When current limiting takes effect, the fault timer limits the duration of the fault. At the end of the fault timeout period (≈26 ms) Q1 is shut off, denying current to the load. The LM5069-2 then initiates a restart every 5.3 seconds. The restart consists of turning on Q1 and monitoring the load current to determine if the fault is still present. After the fault is removed, the circuit powers up to normal operation at the next restart.

In a sudden overload condition (the output is shorted to ground), it is possible the current could increase faster than the response time of the current limit circuit. In this case, the circuit breaker sensor shuts off Q1's gate rapidly when the voltage across R5 reaches ≈105 mV. When the current reduces to the current limit threshold, the current limit circuitry then takes over.

The PGD logic level output is low during turn-on, and switches high when the output voltage at OUT has increased to within 1.25 V of the input voltage, signifying the turn-on procedure is essentially complete. If the OUT voltage decreases more than 2.5 V below VIN due to a fault, PGD switches low. The high level voltage at PGD can be any appropriate voltage up to +80 V, and can be higher or lower than the voltages at VIN and OUT.

The UVLO and OVLO thresholds are set by resistors R1–R3. The UVLO and OVLO thresholds are reached when the voltage at the UVLO and OVLO pins each reach 2.5 V to GND (not SGND), respectively. The internal 21-µA current sources provide hysteresis for each of the thresholds.

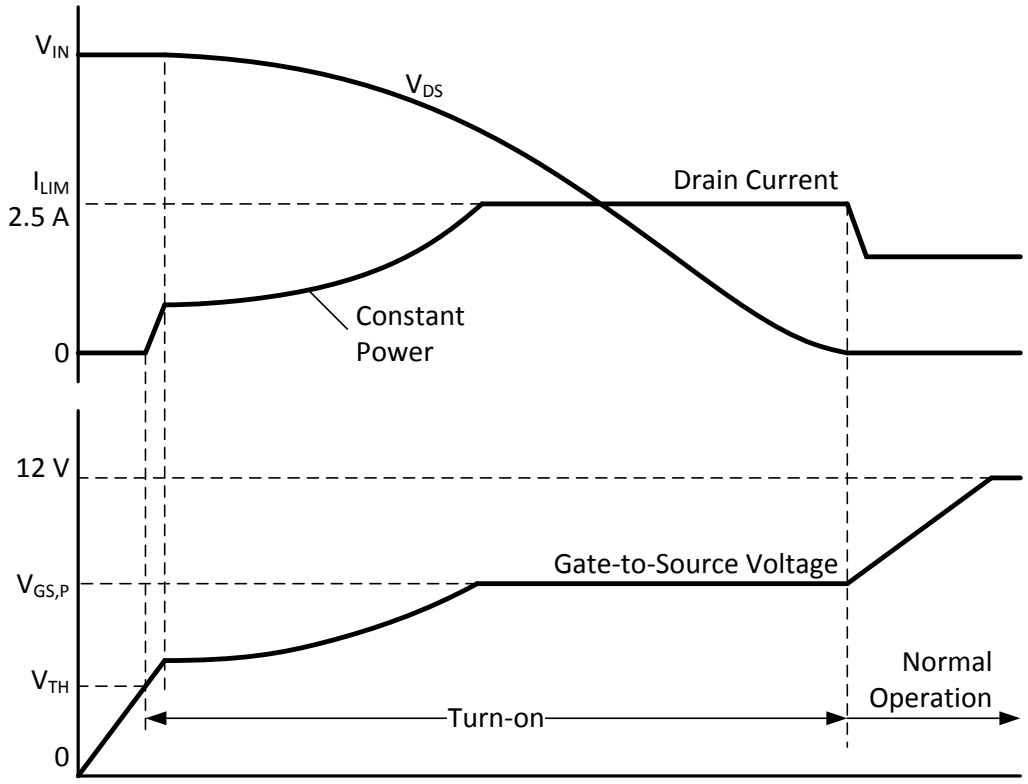

Figure 1. Power Up Using Power Limit and Current Limit

4 Board Connection/Setup and Probe Cautions

The input voltage source is connected to the J1 connector, and the load is connected to the J2 connector at the OUT and GND terminals. *Use twisted wires*. A voltmeter should be connected to the input terminals and one to the output terminals. The input current can be monitored with an ammeter or current probe. To monitor the status of the PGD output, connect a voltmeter from PGOOD to GND on the J2 terminal block. Put the slide switch in the ON position.

Increase the input voltage gradually. The input current should remain less than 2 mA until the upper UVLO threshold is reached (≈16 V). When the threshold is reached, Q1 and Q2 are turned on as described in Section 3. If viewed on an oscilloscope, the input current increases as shown in Figure 1 before settling at the value defined by the load. The turn-on timing depends on the input voltage, power limit setting, current limit setting, and the final load current, and is between ≅3.0 ms with no load current, and ≅7 ms with a 1-A load current, with VIN = 24 V. See Figure 1, Figure 10, and Figure 11.

The following should be kept in mind when the board is powered:

1. High voltage, equal to system input VSYSIN, is present on C3, C4, Q1, Q2 and various points within the circuit. Use *caution* when probing the circuit to prevent injury, as well as possible damage to the circuit.
2. At maximum load current (2.5 A), the wire size and length used to connect the power source and the load become important. The wires connecting this evaluation board to the power source *should be twisted together* to minimize inductance in those leads. The same applies for the wires connecting this board to the load. This recommendation is made in order to minimize high voltage transients from occurring when the load current is shut off.

5 Circuit Parameter Changes

5.1 Current Limit

The current limit threshold is set by R5 according to Equation 1:

$$I_{LIM} = \frac{55\ mV}{R_S} = \frac{55\ mV}{R_5} \quad (1)$$

If the load current increases such that the voltage across R5 reaches 55 mV, the LM5069 then modulates Q1's gate to limit the current to that level. This evaluation board is supplied with a 22-mΩ resistor for R5, resulting in a current limit of 2.5 A. To change the current limit threshold, replace R5 with a resistor of the required value and power capability.

For proper operation, the R_S resistor value should be no larger than 100 mΩ.

5.2 Power Limit

The maximum power dissipated in Q1 during turn-on, or due to a fault, is limited by R9 and R5 according to Equation 2:

$$P_{FET,LIM} = \frac{R_{PWR}}{1.25 \times 10^5 \times R_S} = \frac{R_9}{1.25 \times 10^5 \times R_5} \quad (2)$$

With the components supplied on the evaluation board, PFET(LIM) = 30 W. During turn-on, when the voltage across Q1 is high, its gate is modulated to limit its drain current so the power dissipated in Q1 does not exceed 30 W. As the drain-to-source voltage decreases, the drain current increases, maintaining the power dissipation constant. When the drain current reaches the current limit threshold set by R5 (2.5 A), the current is then maintained constant until the output voltage reaches its final value. The current then decreases to a value determined by the load, see Figure 10, and Figure 11.

Each time Q1 is subjected to the maximum power limit conditions it is internally stressed for a few milliseconds. For this reason, keep in mind that the power limit threshold must be set lower than the limit indicated by the FET's SOA chart. In this evaluation board, the power limit threshold is set at 30 W, compared to ≈80 W limit indicated in the Vishay SUM50N06-16L data sheet. The FET manufacturer should be contacted for more information on this subject.

5.3 Insertion Time

The insertion time starts when the input voltage at VIN reaches 7.6 V, and its duration equals:

$$t_{insertion} = C_T \times \frac{4\ V}{5.5\ \mu A} = C_8 \times 7.24 \times 10^5 \quad (3)$$

During the insertion time, Q1 is held off regardless of the voltage at VIN. This delay allows ringing and transients at VIN to subside before the input voltage is applied to the load via Q1. The insertion time on this evaluation board is ≈400 ms (see Figure 7).

5.4 Fault Detection and Restart

If the load current increases to the fault level (the current limit threshold, 2.5 A), an internal current source charges the timing capacitor C8 at the TIMER pin. When the voltage at the TIMER pin reaches 4.0 V, the fault timeout period is complete, and the LM5069 shuts off Q1. The restart sequence then begins, consisting of seven cycles at the TIMER pin between 4.0 V and 1.25 V, as shown in Figure 2. When the voltage at the TIMER pin reaches 0.3 V during the eighth high-to-low ramp, Q1 is turned on. If the fault is still present, the fault timeout period and the restart sequence repeat.

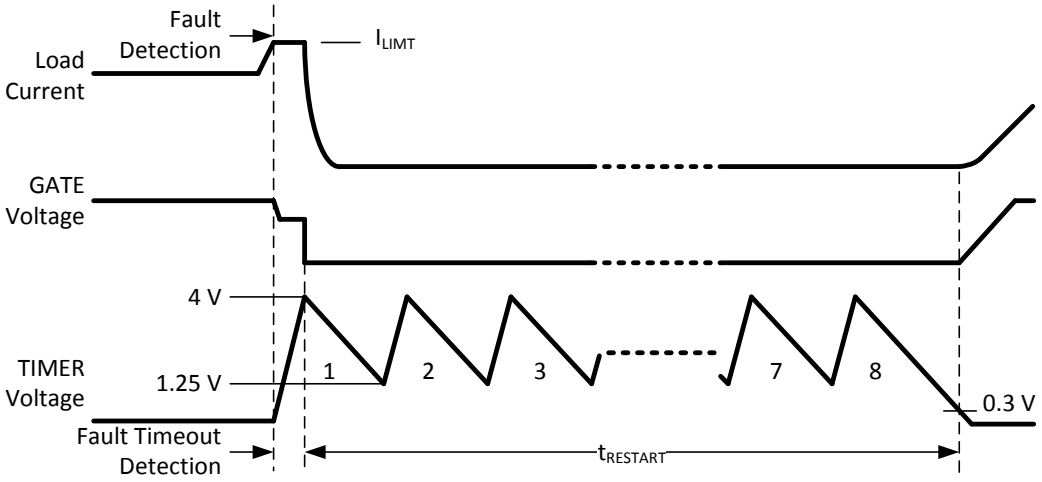

Figure 2. Fault Timeout and Restart Sequence

The fault timeout period and the restart timing are determined by the TIMER capacitor C8 according to Equation 4 and Equation 5:

$$t_{fault} = C_T \times \frac{4\ V}{85\ \mu A} = C_8 \times 4.7 \times 10^4 \quad (4)$$

$$t_{restart} = C_T \times \left[\frac{7 \times 2.75\ V}{2.5\ \mu A} + \frac{7 \times 2.75\ V}{85\ \mu A} + \frac{3.7\ V}{2.5\ \mu A} \right] = C_8 \times 9.4 \times 10^6 \quad (5)$$

The waveform at the TIMER pin can be monitored at the test pad located between C8 and R9. In this evaluation board, the fault timeout period is ≈26 ms, and the restart time is ≈5.3 seconds (see Figure 8 and Figure 9).

5.5 UVLO/OVLO Input Voltage Thresholds

As supplied, the input voltage UVLO thresholds on this evaluation board are approximately 16 V increasing, and 14 V decreasing. The OVLO thresholds are approximately 36 V increasing, and 34 V decreasing. The four thresholds are determined by resistors R1–R4. The threshold voltage at each pin is 2.5 V to GND (not SGND), and internal 21-µA current sources provide hysteresis for each threshold. See the device data sheet for more details.

Option A: This evaluation board is supplied with the jumper at JMP1 on pins 2–3, resulting in the configuration shown in Figure 3.

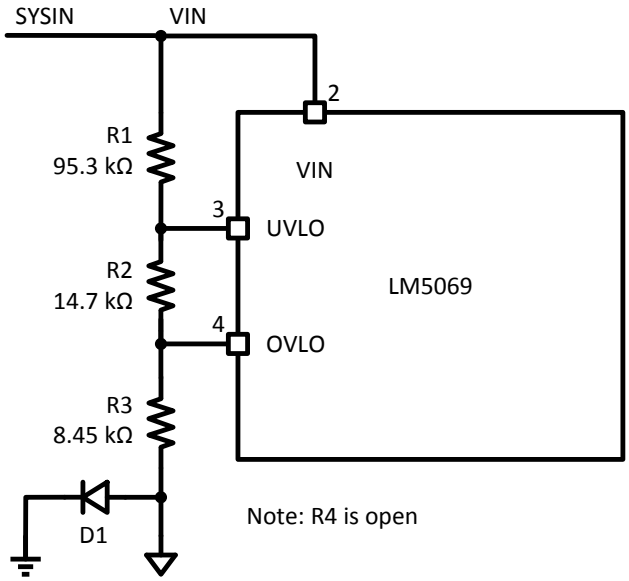

Figure 3. UVLO, OVLO Inputs (Option A)

To change the thresholds in this configuration, resistors R1–R3 are calculated using the following procedure:

- Choose the upper UVLO threshold (V_{UVH}), and the lower UVLO threshold (V_{UVL})
- Choose the upper OVLO threshold (V_{OVH})

The lower OVLO threshold (VOVL) cannot be chosen in advance in this case, but is determined after the values for R1–R3 are determined. If VOVL must be accurately defined in addition to the other three thresholds, see **Option B** following Equation 7.

The resistors are calculated as follows:

$$R_1 = \frac{(V_{UVH} - V_F) - (V_{UVL} - V_F)}{21\ \mu A}$$

$$R_3 = \frac{2.5\ V \times R_1 \times (V_{UVL} - V_F)}{(V_{OVH} - V_F) \times (V_{UVL} - V_F - 2.5\ V)}$$

$$R_2 = \frac{2.5\ V \times R_1}{V_{UVL} - V_F - 2.5\ V} - R_3$$

$$V_F = V_{F,D1} \quad (6)$$

NOTE: V_F is the forward voltage of diode D1.

The lower OVLO threshold is calculated from:

$$V_{OVL} = \left[(R_1 + R_2) \times \left(\frac{2.5V}{R_3} - 21\ \mu A \right) \right] + 2.5\ V + V_F \quad (7)$$

Option B: If all four thresholds must be determined accurately, move the jumper at JMP1 to pins 1–2, and add R4, resulting in the configuration shown in Figure 4:

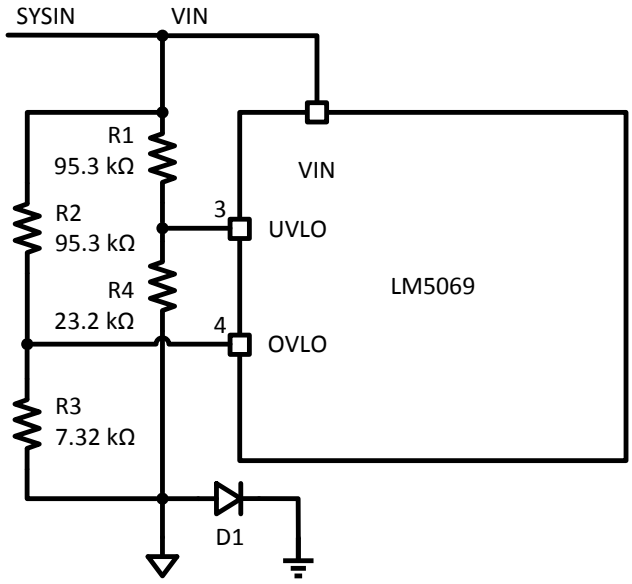

Figure 4. UVLO, OVLO Inputs (Option B)

The four resistor values are calculated as follows:

Choose the upper and lower UVLO thresholds (V_{UVH}) and (V_{UVL}):

$$R_1 = \frac{(V_{UVH} - V_F) - (V_{UVL} - V_F)}{21\ \mu A} \quad (8)$$

$$R_4 = \frac{2.5\ V \times R_1}{V_{UVL} - V_F - 2.5\ V} \quad (9)$$

Choose the upper and lower OVLO threshold (V_{OVH}) and (V_{OVL}):

$$R_2 = \frac{(V_{UVH} - V_F) - (V_{UVL} - V_F)}{21\ \mu A}$$

$$R_3 = \frac{2.5\ V \times R_2}{V_{OVH} - V_F - 2.5\ V} \quad (10)$$

CAUTION

The absolute maximum rating for the OVLO pin is 7 V. Do not let the voltage on OVLO exceed 7 V when VIN is at its maximum value. The absolute maximum rating for the UVLO pin is 100 V.

Option C: The minimum UVLO level is obtained by positioning the jumper at JMP1 on pins 1–2, and leaving R4 open, resulting in the configuration shown in Figure 5. Q1 is switched on when the voltage at VIN reaches the POR_{EN} threshold (≈8.4 V). The OVLO thresholds are set by R2 and R3, and their values are calculated using the procedure in Option B. The value for R1 is not critical, and can be as supplied. Please adhere to the previous **CAUTION**.

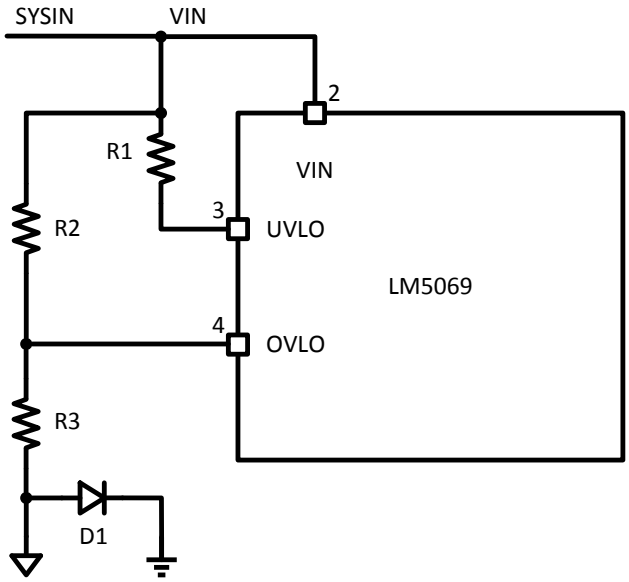

Figure 5. Minimum UVLO Threshold, Adjustable OVLO

Option D: The OVLO function can be disabled by removing the jumper from JMP1. The UVLO thresholds are set by R1 and R4 using the procedure in Option B or C.

5.6 Surge Clamping

Surge clamping is performed by the FET, Q1 (see Figure 18), which will clamp any input voltages that rise above the level programmed by Z2. As input voltage increases during a surge event, the output voltage will also increase and the internal charge pump will try to keep V_{GATE} 12 V above V_{OUT}. Because of Z2, V_{GATE} cannot rise above V_{Z_Z2}; therefore, V_{OUT} cannot rise above ($V_{Z\text{-}Z2} – V_{THRESHOLD\_Q1}$).

For a different surge clamp voltage, use the following equation to select an alternate Zener Diode;

$$V_{ZENER} = V_{LOAD\_MAX\_SURGE} + V_{THRESHOLD\_Q1} \quad (11)$$

NOTE: If there is a resistive path < 1 MΩ from V_{IN} (LM5069 pin 2) to GND (LM5069 pin 5) then D2 and R6 are not required. OV, UV programming resistors often provide this resistive path. D2 and R6 are intended to provide a weak gate pin pull down during reverse hookup conditions in cases where there is no external pull down.

5.7 Shutdown

With the circuit in normal operation, the LM5069 can be shut down by grounding the UVLO pin. Slide switch SW1, left bottom side of the board, can be used for this purpose. See Figure 12.

5.8 Power Good Output

The PGOOD logic output provides an indication of the circuit's condition. This output is high when the circuit is in normal operation – the OUT voltage is within 1.25 V of the input. PGOOD is low when the circuit is shutdown, either intentionally or due to a fault. PGOOD is also high when VIN is less than 5 V. As the output voltage will be clamped at 32 V, the PGOOD is low when input voltage exceeds 33.5 V.

This EVB is supplied with pins 1–2 connected on JMP2, powering the PGD pin from the output voltage through a 100-kΩ pull-up resistor. To change the high-level PGOOD voltage, move the jumper on JMP2 to pins 2–3, and supply the appropriate pull-up voltage to terminal P1 (located next to JMP2). If the UVLO pin is taken low to disable the LM5069, PGOOD switches low within 10 µs without waiting for the OUT voltage to fall, see Figure 13.

If a delay at the PGOOD output is desired, a resistor and capacitor can be added at positions R8 and C6.

5.9 Reverse Hookup Protection

When power feeds are incorrectly connected and polarity to the EVM is reversed, a simple low-power diode (D1) between supply GND and LM5069 GND protects the LM5069 by keeping it off and without power.

To prevent current from flowing through the body diode of Q1 during reverse supply connection, a second FET, (Q2), is put in series with Q1. Q1 drain and Q2 Drain connected, creating a back to back FET configuration.

When $V_{IN} < UV_{LM5069}$, the gate pin is internally pulled to GND, keeping Q1 and Q2 off.

6 Performance Characteristics Plots

6.1 Reverse Polarity Input

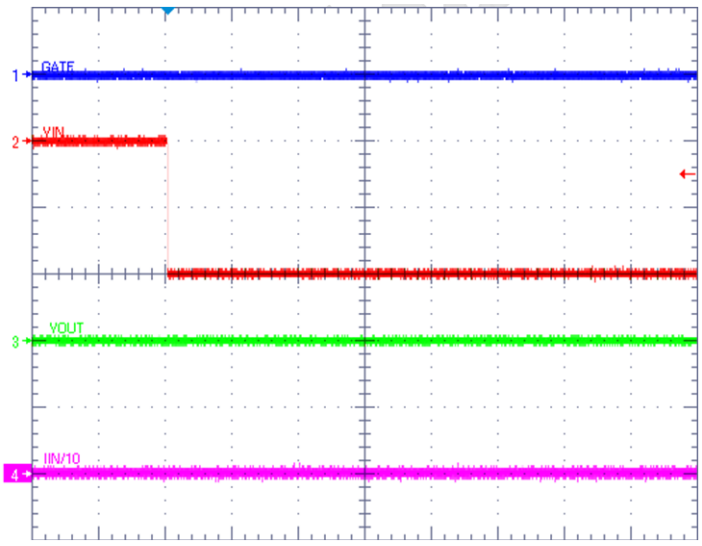

Figure 6. Reverse Polarity Input

Horizontal resolution: 40 ms/div
Channel 1: GATE, 50 V/div
Channel 2: SYS IN, 20 V/div
Channel 3: SYS OUT, 20 V/div
Channel 4: I_{IN}, 1 A/div
SYS VIN = –40 V

6.2 Insertion Time Delay

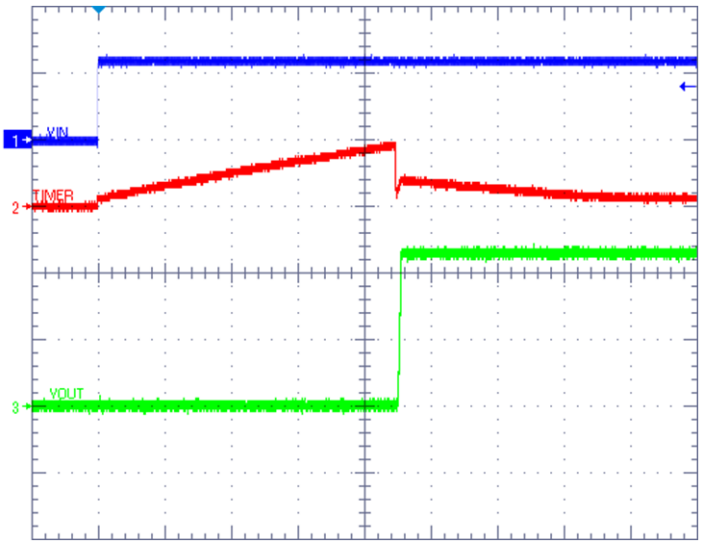

Figure 7. Insertion Timer Delay

Horizontal resolution: 100 ms/div
Channel 1: SYS IN, 20 V/div
Channel 2: TIMER, 5 V/div
Channel 3: SYS OUT, 10 V/div
C_T = 0.56 µF
SYS IN = 24 V

6.3 Fault Timeout

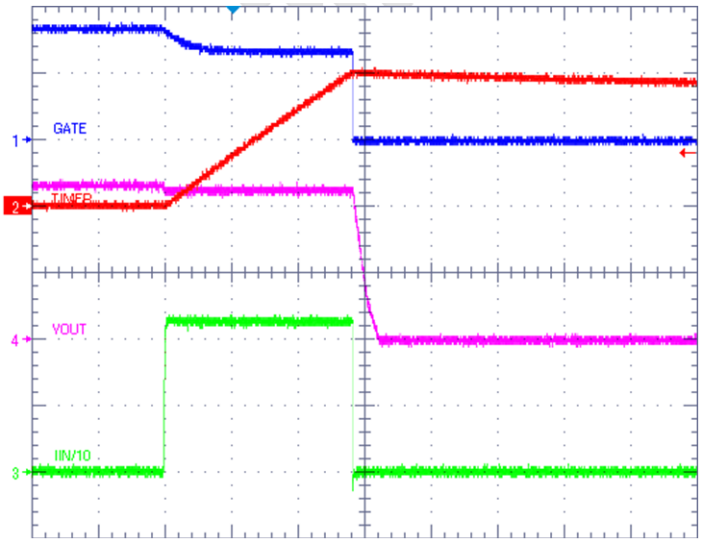

Figure 8. Fault Timeout

Horizontal resolution: 100 ms/div
Channel 1: GATE, 20 V/div
Channel 2: TIMER, 2 V/div
Channel 3: I_{IN}, 1 V/div
Channel 4: SYS OUT, 10 V/div
C_T = 0.56 µF
SYS IN = 24 V

6.4 Restart Timing

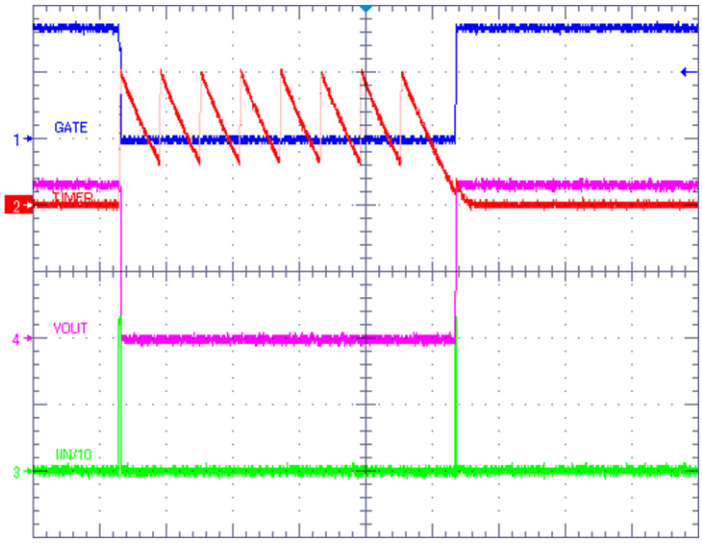

Figure 9. Restart Timing

Horizontal resolution: 1.0 s/div
Channel 1: GATE, 20 V/div
Channel 2: TIMER, 2 V/div
Channel 3: I_{IN}, 1 A/div
Channel 4: SYS OUT, 10 V/div
C_T = 0.56 µF
SYS IN = 24 V

6.5 Turn-on Sequence with No Load Current

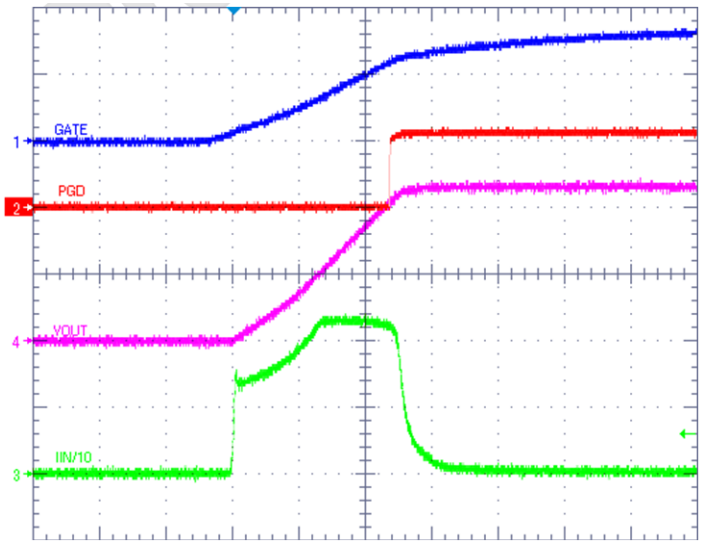

Figure 10. Turn-on Sequence with No Load Current

Horizontal resolution: 1.0 ms/div
Channel 1: GATE, 20 V/div
Channel 2: PGD, 20 V/div
Channel 3: I_{IN}, 1 A/div
Channel 4: SYS OUT, 10 V/div
SYS IN = 24 V

6.6 Turn-on Sequence with 1-A Load Current

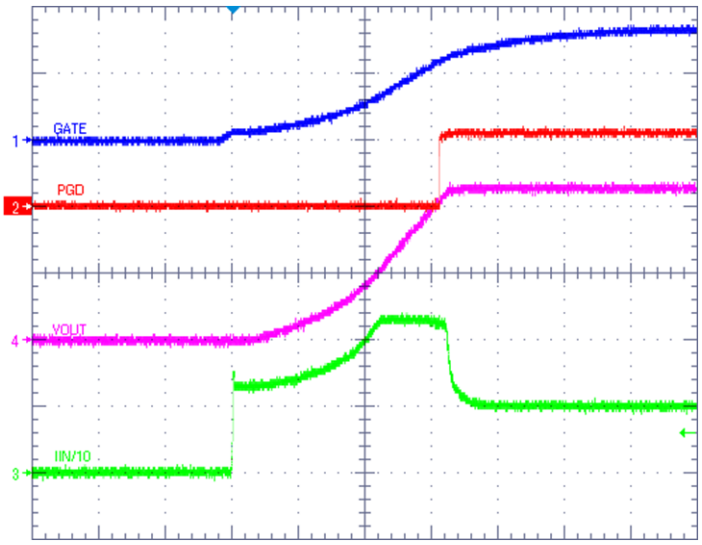

Figure 11. Turn-on Sequence with 1-A Load Current

Horizontal resolution: 2.0 ms/div
Channel 1: GATE, 20 V/div
Channel 2: PGD, 20 V/div
Channel 3: I_{IN}, 1 A/div
Channel 4: SYS OUT, 10 V/div
SYS IN = 24 V

6.7 Output Shutdown Using UVLO Pin

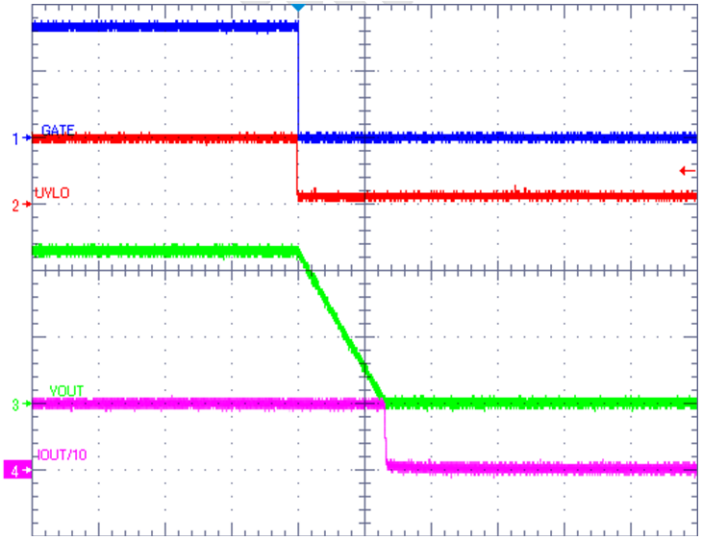

Figure 12. Output Shutdown Using UVLO Pin

Horizontal resolution: 4.0 ms/div
Channel 1: GATE, 20 V/div
Channel 2: UVLO, 5 V/div
Channel 3: SYS OUT, 10 V/div
Channel 4: I_{OUT}, 1 A/div
SYS IN = 24 V

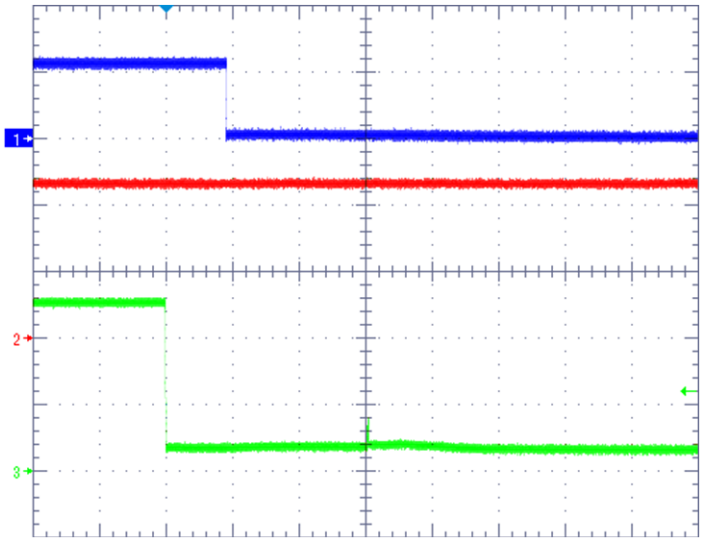

Figure 13. Output Shutdown Using UVLO Pin

Horizontal resolution: 10 µs/div
Channel 1: PGD, 20 V/div
Channel 2: SYS OUT, 10 V/div
Channel 3: UVLO, 2 V/div
SYS IN = 24 V

6.8 Input Surge

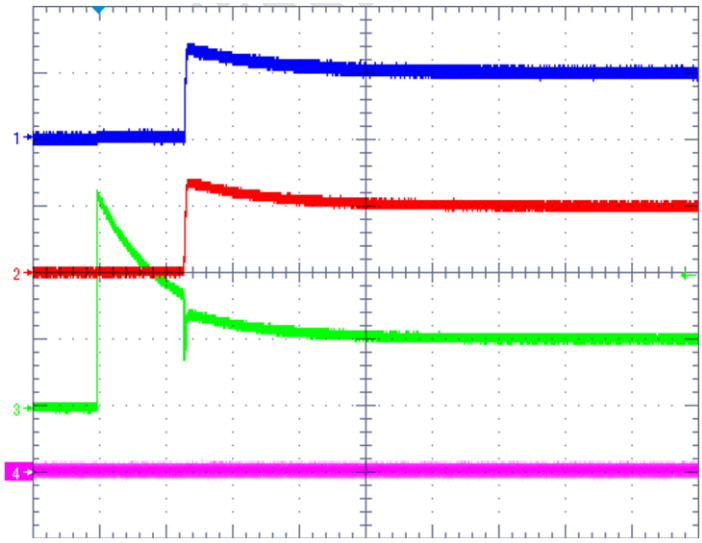

Figure 14. Input Surge (Not Clamped)

Horizontal resolution: 400 ms/div
Channel 1: PGD, 20 V/div
Channel 2: SYS OUT, 20 V/div
Channel 3: SYS IN, 20 V/div
Channel 4: I_{IN}, 1 A/div

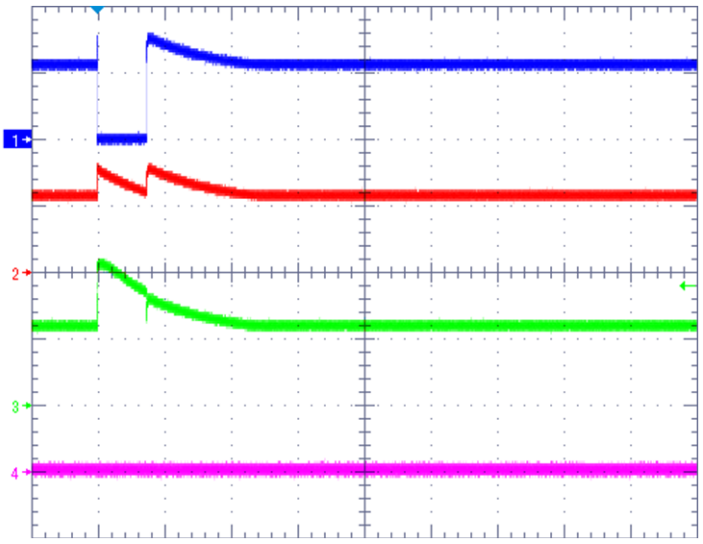

Figure 15. Input Surge (Clamped)

Horizontal resolution: 400 ms/div
Channel 1: PGD, 20 V/div
Channel 2: SYS OUT, 20 V/div
Channel 3: SYS IN, 20 V/div
Channel 4: I_{IN}, 1 A/div

6.9 Inrush Current

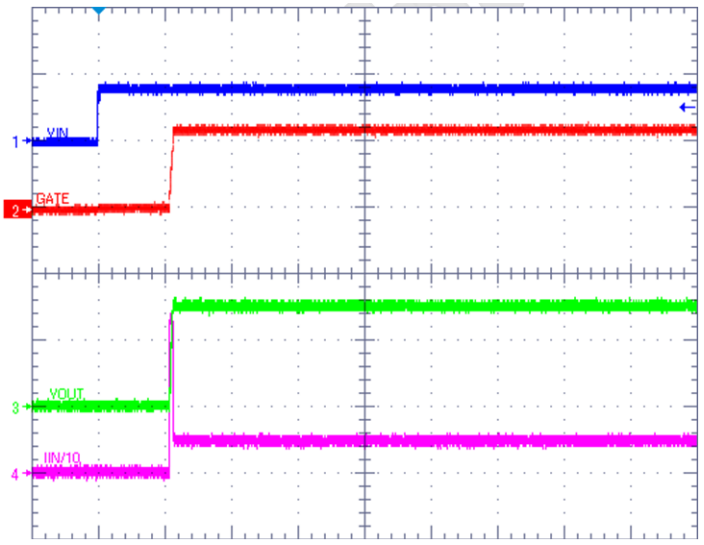

Figure 16. Inrush Current with 2550-µF Output Capacitor

Horizontal resolution: 400 ms/div
Channel 1: SYS IN, 20 V/div
Channel 2: GATE, 20 V/div
Channel 3: SYS OUT, 10 V/div
Channel 4: I_{OUT}, 1 A/div
SYS IN = 16 V
Output Capacitor: 470 µF × 5 + 100 µF × 2 = 2550 µF
Load: 32-Ω resistor

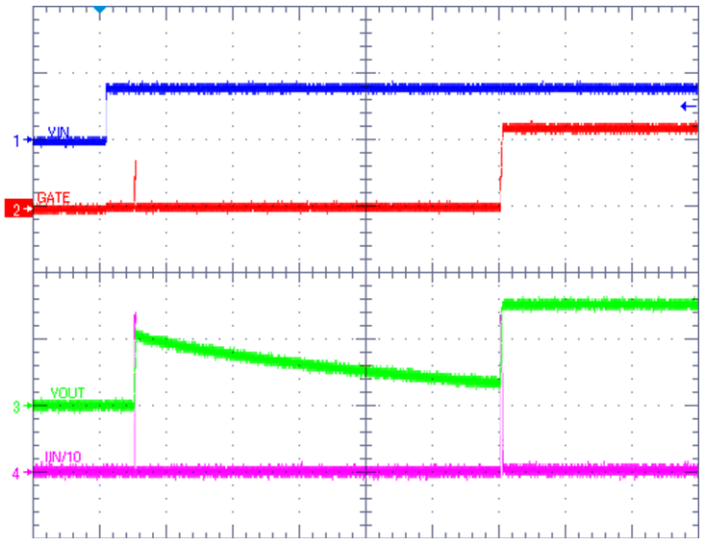

Figure 17. Inrush Current with 4900-µF Output Capacitor

Horizontal resolution: 1 s/div	Channel 4: I_{OUT}, 1 A/div
Channel 1: SYS IN, 20 V/div	SYS IN = 16 V
Channel 2: GATE, 20 V/div	Output Capacitor: 470 µF × 10 + 100 µF × 2 = 4900 µF
Channel 3: SYS OUT, 10 V/div	Load: 900-Ω resistor

7 Schematic

The schematic for this EVM is shown in Figure 18.

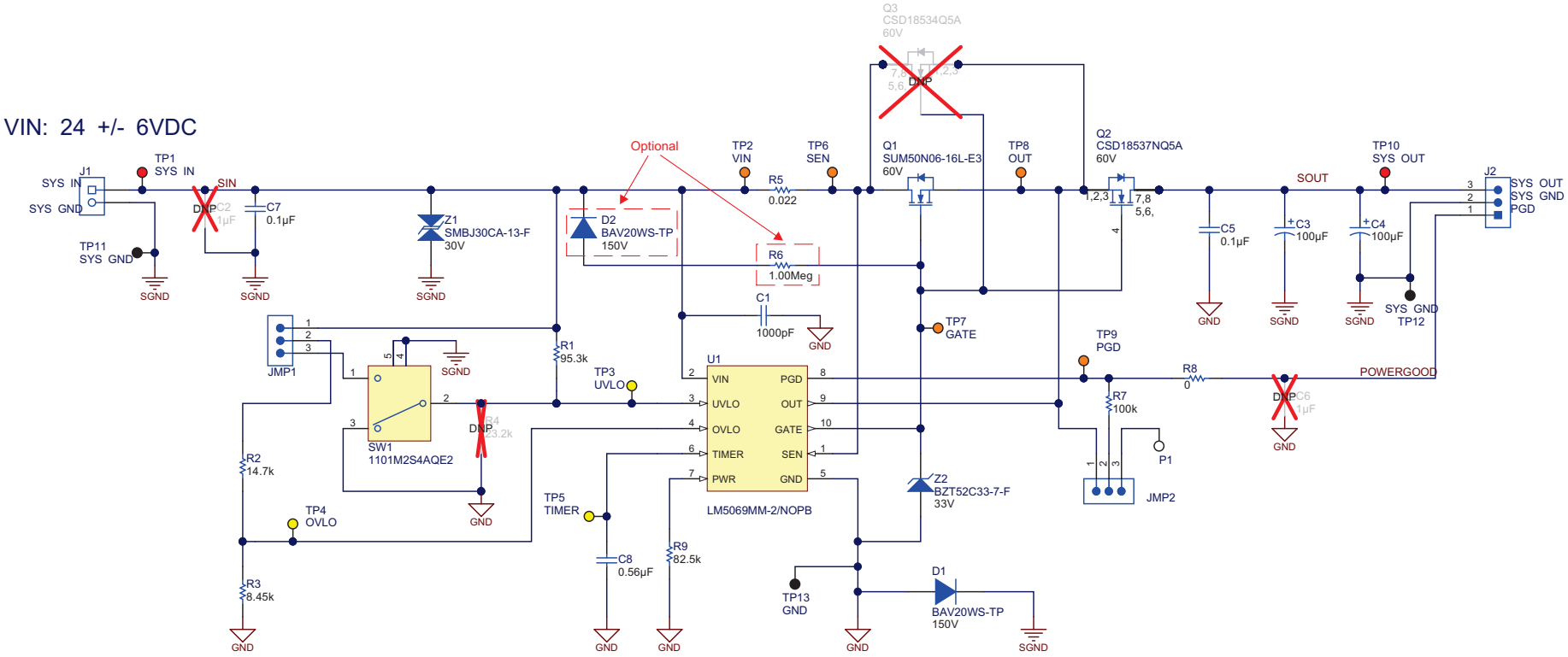

Figure 18. LM5069EVM-627 Schematic

8 PCB Layout

Figure 19 through Figure 21 illustrate the PCB layouts.

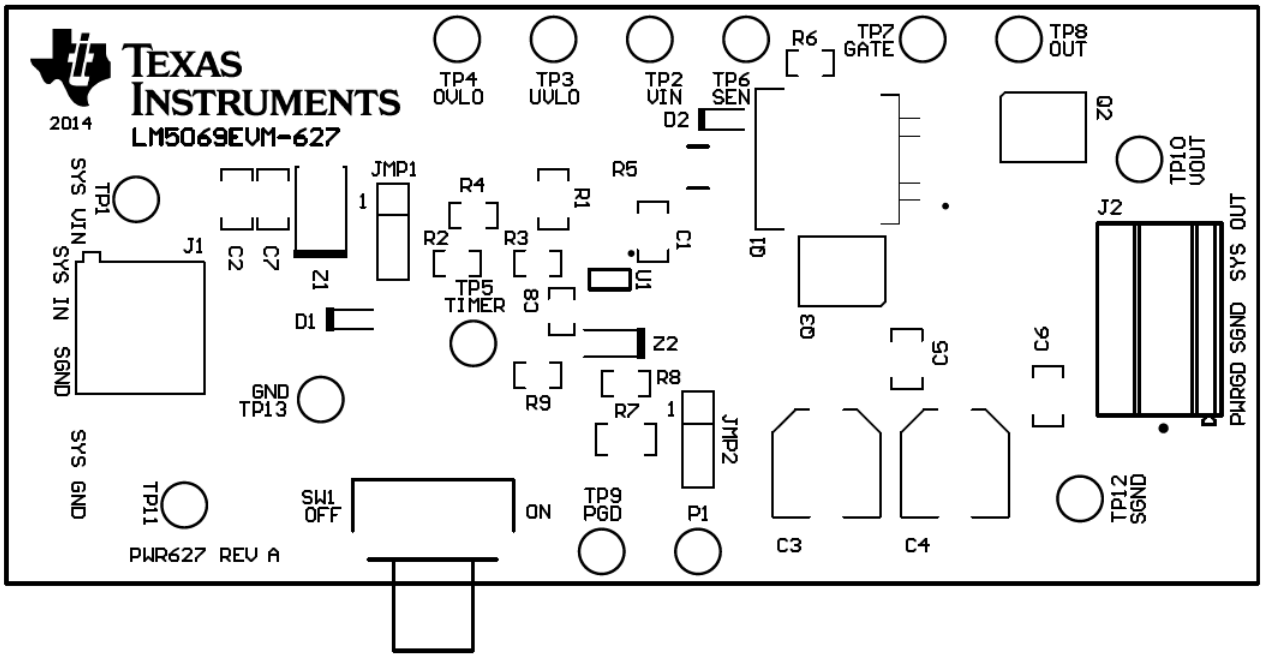

Figure 19. Top Side Placement

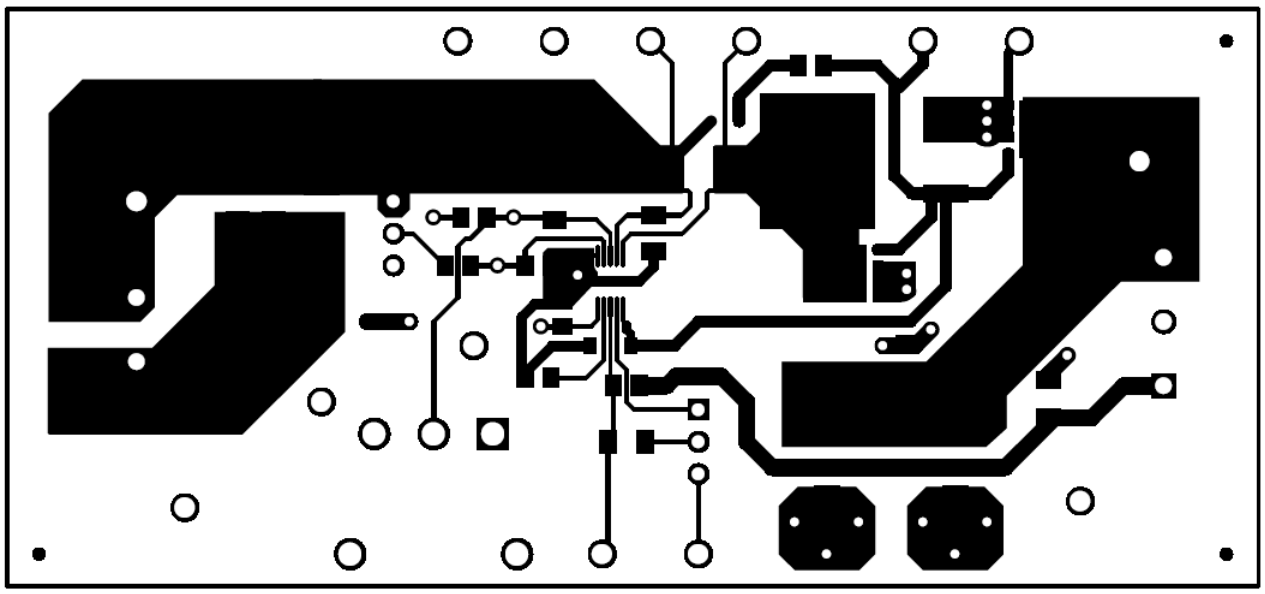

Figure 20. Top Layer

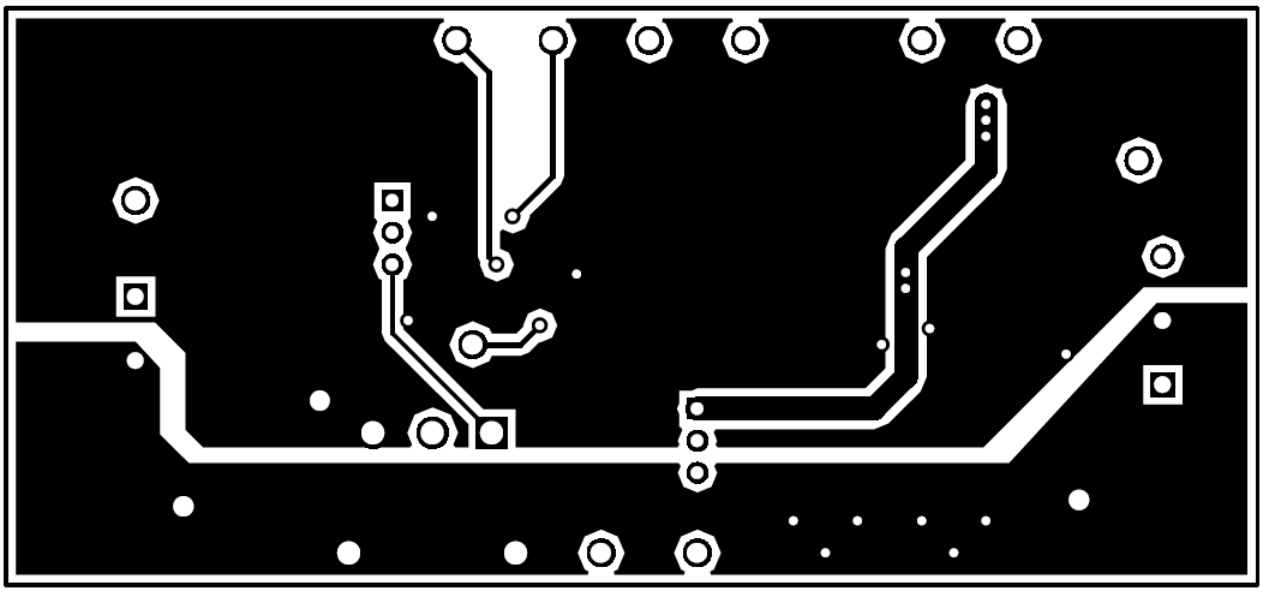

Figure 21. Bottom Layer

9 Bill of Materials (BOM)

Table 1 lists the BOM for this EVM.

Table 1. Bill of Materials

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
!PCB	1		Printed Circuit Board		PWR627	Any
C1	1	1000pF	CAP, CERM, 1000pF, 50V, +/-10%, X7R, 1206	1206	12065C102KAT2A	AVX
C3, C4	2	100uF	CAP, AL, 100uF, 50V, +/-20%, 0.34 ohm, SMD	SMT Radial F	EEE-FK1H101P	Panasonic
C5	1	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 1206	1206	12065C104KAT2A	AVX
C7	1	0.1uF	CAP, CERM, 0.1uF, 100V, +/-20%, X7R, 1206	1206	C3216X7R2A104M	TDK
C8	1	0.56uF	CAP, CERM, 0.56uF, 25V, +/-10%, X7R, 0805	0805	C0805C564K3RACTU	Kemet
D1, D2	2	150V	Diode, P-N, 150V, 0.2A, SOD-323	SOD-323	BAV20WS-TP	Micro Commercial Components
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
H1, H2, H3, H4	4		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M
J1	1	2x1	Conn Term Block, 2POS, 5.08mm, TH	2POS Terminal Block	1715721	Phoenix Contact
J2	1		TERM BLOCK 3POS 5.08MM, TH	15.24x13.8x9.8mm	1715734	Phoenix Contact
JMP1, JMP2	2	1x3	Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
P1	1	White	Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone
Q1	1	60V	MOSFET, N-CH, 60V, 50A, DDPAK	DDPAK	SUM50N06-16L-E3	Vishay-Siliconix
Q2	1	60V	MOSFET, N-CH, 60V, 50A, SON 5x6mm	SON 5x6mm	CSD18537NQ5A	Texas Instruments
R1	1	95.3k	RES, 95.3k ohm, 1%, 0.25W, 1206	1206	CRCW120695K3FKEA	Vishay-Dale
R2	1	14.7k	RES, 14.7k ohm, 1%, 0.125W, 0805	0805	CRCW080514K7FKEA	Vishay-Dale
R3	1	8.45k	RES, 8.45k ohm, 1%, 0.125W, 0805	0805	CRCW08058K45FKEA	Vishay-Dale
R5	1	0.022	RES, 0.022 ohm, 1%, 0.5W, 1812	1812	ERJ-L12KF22MU	Panasonic
R6	1	1.00Meg	RES, 1.00Meg ohm, 1%, 0.125W, 0805	0805	CRCW08051M00FKEA	Vishay-Dale
R7	1	100k	RES, 100k ohm, 1%, 0.25W, 1206	1206	CRCW1206100KFKEA	Vishay-Dale
R8	1	0	RES, 0 ohm, 5%, 0.125W, 0805	0805	CRCW08050000Z0EA	Vishay-Dale
R9	1	82.5k	RES, 82.5k ohm, 1%, 0.125W, 0805	0805	CRCW080582K5FKEA	Vishay-Dale
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
SW1	1		Slide Switches SPDT R/A, TH	12.7x6.6x6.35mm	1101M2S4AQE2	C&K Components
TP1, TP10	2	Red	Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP2, TP6, TP7, TP8, TP9	5	Orange	Test Point, Multipurpose, Orange, TH	Orange Multipurpose Testpoint	5013	Keystone
TP3, TP4, TP5	3	Yellow	Test Point, Multipurpose, Yellow, TH	Yellow Multipurpose Testpoint	5014	Keystone
TP11, TP12, TP13	3	Black	Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
U1	1		Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting, 10-pin MSOP, Pb-Free	MUB10A	LM5069MM-2/NOPB	Texas Instruments
Z1	1	30V	Diode, TVS, Bi, 30V, 600W, SMB	SMB	SMBJ30CA-13-F	Diodes Inc.
Z2	1	33V	Diode, Zener, 33V, 500mW, SOD-123	SOD-123	BZT52C33-7-F	Diodes Inc.
C2	0	1uF	CAP, CERM, 1uF, 100V, +/-20%, X7R, 1206	1206	C3216X7R2A105M160AA	TDK
C6	0	1uF	CAP, CERM, 1uF, 50V, +/-10%, X7R, 1206	1206	C3216X7R1H105K	TDK
Q3	0	60V	MOSFET, N-CH, 60V, 50A, SON 5x6mm	SON 5x6mm	CSD18534Q5A	Texas Instruments
R4	0	23.2k	RES, 23.2k ohm, 1%, 0.125W, 0805	0805	CRCW080523K2FKEA	Vishay-Dale

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

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This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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