User's Guide

Powering Jacinto ™ J7 SoC Family For Isolated Power Groups With TPS6594133A-Q1 PMIC and Dual HCPS Converters

ABSTRACT

This user's guide can be used as a guide for integrating the TPS6594-Q1 power management integrated circuit (PMIC) into a system powering the Automotive Jacinto J784S4 or J721S2 processors with isolated MCU and Core power groups.

Table of Contents

Trademarks

Jacinto™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

This user's guide describes two options of power distribution network (PDN), PDN-3A and PDN-3F, using the TPS6594133A-Q1 PMIC to supply and control power to J784S4 or J721S2 processors with independent MCU and Main power rails. These PDNs enable board level isolation of the MCU safety island and main voltage resources as required for implementing two desirable features of the processor:

- MCU processor acts as independent safety monitor (MCU Safety Island) over the Main processing resources to maintains safe system operations.
- MCU processor maintains minimum system operations (MCU Only) to significantly reduce processor power dissipation thereby extending battery life during stand-by use cases and reducing component temperature.

The following topics are described to clarify platform system operation:

- PDN power resource connections
- PDN digital control connections
- PMIC (TPS6594133A-Q1) static NVM contents
- PMIC sequencing settings to support different PDN power state transitions.

PMIC and processor data manuals provide recommended operating conditions, electrical characteristics, recommended external components, package details, register maps, and overall component functionality. In the event of any inconsistency between any user's guide, application report, or other referenced material, the data sheet specification is the definitive source.

2 Processor Connections

This section details how the TPS6594133A-Q1 power resources and GPIO signals are connected to the processor, discrete power resources, and other peripheral components.

2.1 Power Mapping

The PDN-3x base power resources are the TPS6594133A-Q1 PMIC, two High-Current Power Stages (HCPS-A & HCPS-B), two TPS389006004-Q1 Safety Voltage Supervisors, two TPS74501P-Q1 LDOs and one TPS622965-Q1 load switch. The processor CPU and CORE power rails are powered by HCPS-A and HCPS-B respectively. Each HCPS consists of one or multiple, stackable TPS6287xY1-Q1 buck converters. For recommended HCPS configurations based upon JS84S4 or J721S2 processor type, see Table 2-1. The PMIC has built-in input supply voltage level detection, which enables it to use either a 3.3V or 5V system input voltage. If a system does use a 5V input, then the load switches used to supply the processor with 3.3V for IO signaling need to be replaced with either a buck converter or LDO depending upon overall system needs.

Table 2-1. CPU and CORE Power Resources

Processor	HCPS - A (CPU Power)	HCPS - B (CORE Power)
J784S4	3 x TPS62873Y1 - Q1	2 x TPS62873Y1 - Q1
J721S2	1 x TPS62873Y1 - Q1	2 x TPS62871Y1 - Q1

For Functional Safety applications, the PMIC provides majority of all key requirements, see TPS6594 Data Sheet. In addition, there is a protection FET before VCCA that connects to the OVPGDRV pin of the PMIC, allowing voltage monitoring of the input supply. Two TPS389006004-Q1 Safety Voltage Supervisors (SVS) are used for OV/UV monitoring on all discrete power resource voltages as required for functional safety systems that are ASIL-B/D capable.

Figure 2-1 shows PDN-3A power map for supplying a J784S4 or J721S2 processor platform (SoC, Flaxh & LPDDR4 memories, power resources) with base features plus all optional features that includes three processor low power modes (MCU Only, GPIO Retention and DDR Retention) and three optional functions (UHS-I SD card, USB2.0 interface and HS eFuse programming). PDN - 3A.I Power Connections - Full Features, Industrial Application is the same as the PDN-3A but intended for industrial applications and uses a slightly different voltage monitoring strategy. Figure 2-3 depicts the PDN-3F power map using only the PDN-3x base power resources to support the base feature set (ASIL-D safety capable system, MCU and Main supply isolation, MCU Safety Island, MCU Only low power mode, dual voltage 1.8/3.3V IO signaling, four LPDDR4 memories, OSPI boot Flash & eMMC storage Flash).

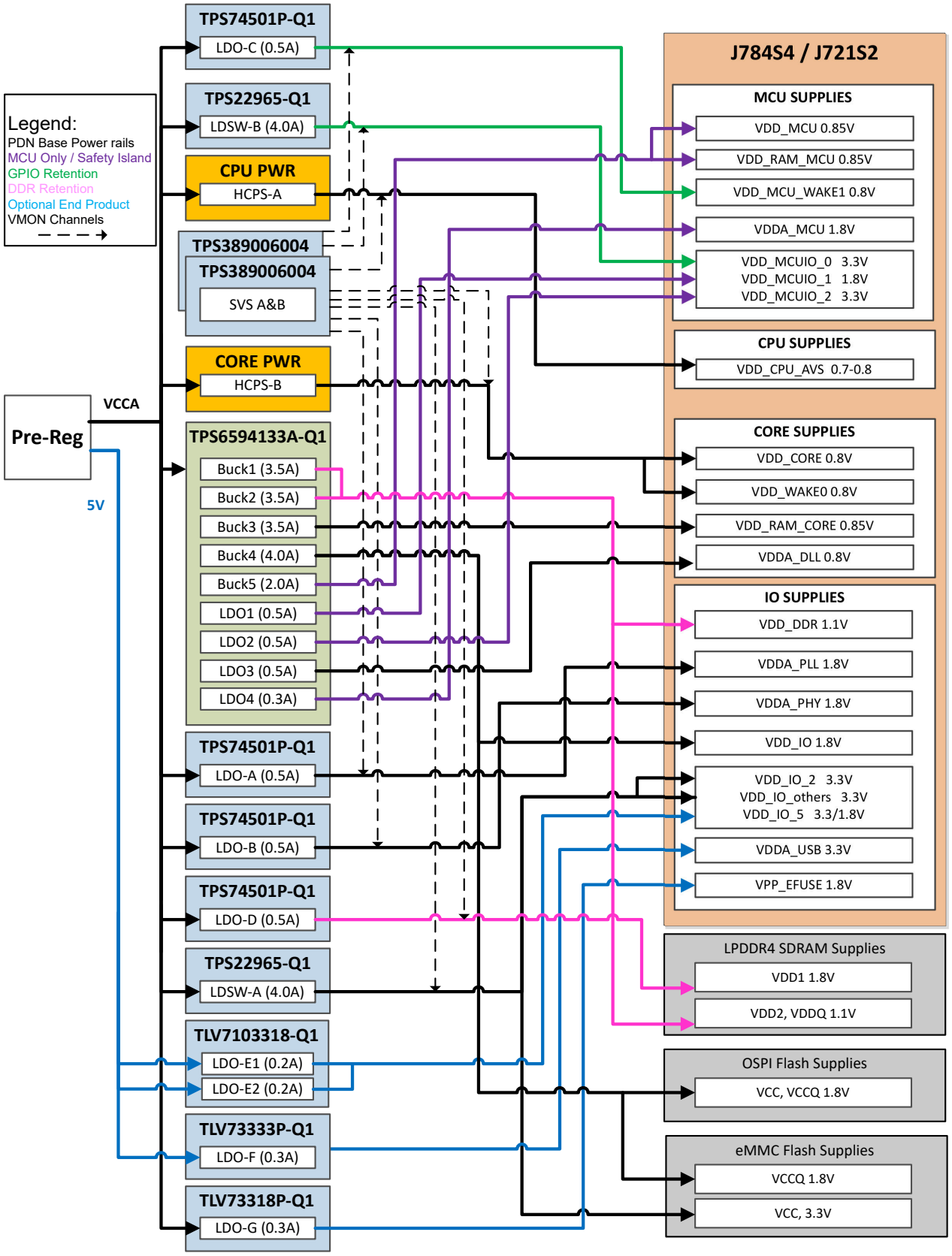


Figure 2-1. PDN-3A Power Connections - Full Features

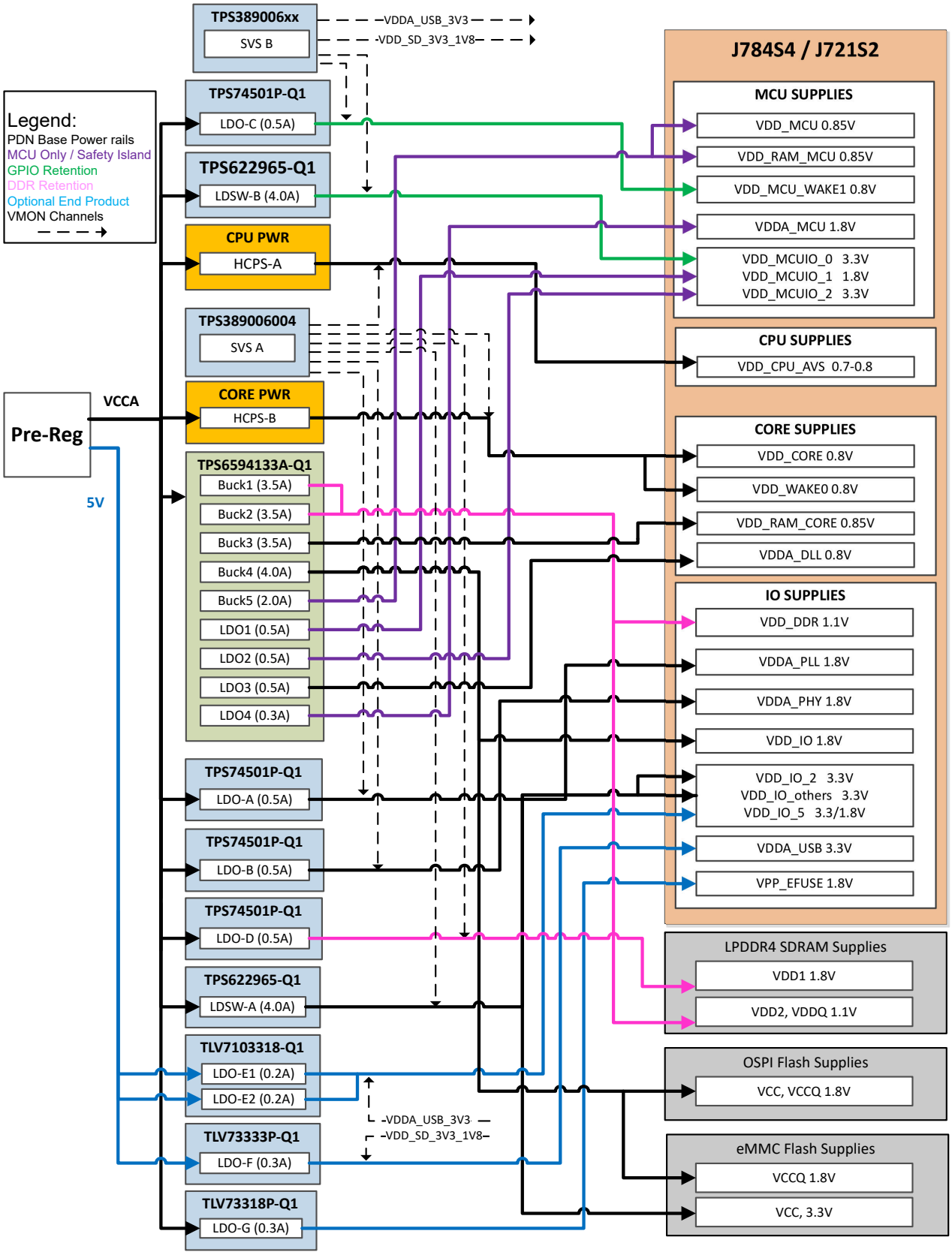


Figure 2-2. PDN - 3A.I Power Connections - Full Features, Industrial Application

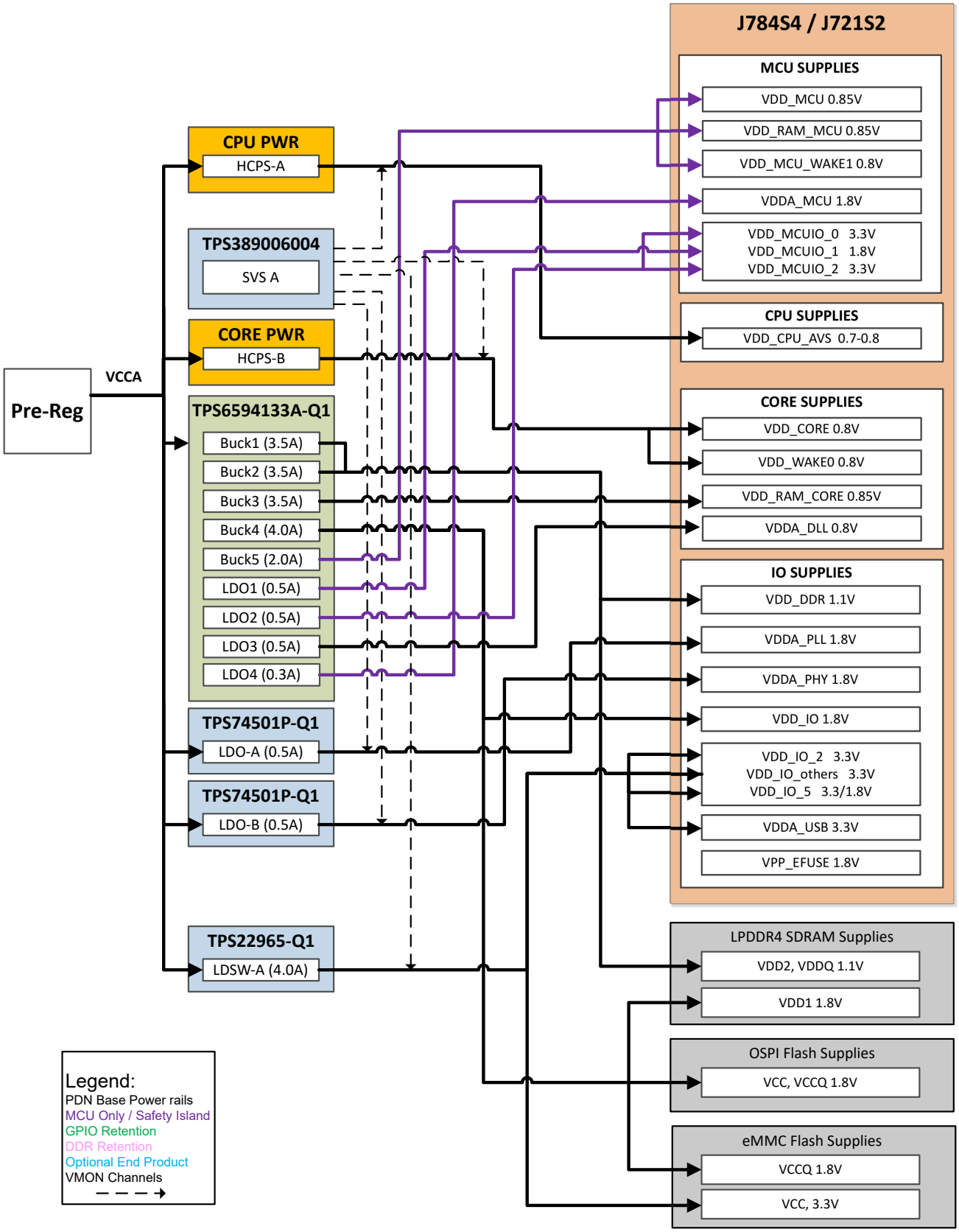


Figure 2-3. PDN-3F Power Connections - Reduced Features

Table 2-2 identifies the required power resources and rails needed to support PDN-3A full featured system. If a feature is not desired, the power resource and rail can be removed but the processor input supply must be connected to another power rail of like voltage and type since all supplies need to be energized for full active operations. Table 2-3 gives guidance on grouping of processor input supplies into base power rails if any of the three low power modes or optional functions are not desired. Applying this guidance to the full featured PDN-3A scheme enables other PDN-3x variants (x = B/C/D/E/ F) that support end products with different feature sets in between PDN-3A and PDN-3F.

Table 2-2. PDN-3A Power Map vs. System Features

Power Mapping				System Features[1]						
Device	Power Resource	Power Rails	Processor and Memory Domains	Active SoC	MCU Only	DDR Ret	GPIO Ret	SD Card	EFUSE	USB
TPS6594133A-Q1	BUCK12	VDD_DDR_1V1	VDDS_DDR, VDDS_DDR_C3:0 Mem: VDD2, VDDQ	R		R				
	BUCK3	VDD_RAM_0V85	VDDAR_CORE, VDDAR_CPU	R						
	BUCK4	VDD_IO_1V8	VDDS_MMC0	R						
	BUCK5	VDD_MCU_0V85	VDD_MCU, VDDAR_MCU	R	R					
	LDO1	VDD_MCUIO_1V8	VDDSHV1_MCU	R	R					
	LDO2	VDD_MCUIO_3V3	VDDSHV2_MCU	R	R					
	LDO3	VDA_DLL_0V8	VDDA_0P8_PLL_DDR3:0, VDDA_0P8_DLL_MMC0	R						
	LDO4	VDA_MCU_1V8	VDDA_MCU_PLLGRP0, VDDAMCU_TEMP, VDDA_POR_WKUP, VDDA_WKUP, VDDA_ADC1:0	R	R					
TPS22965-Q1	Load Switch-A	VDD_IO_3V3	VDDSHV0, VDDSHV2	R						
TPS22965-Q1	Load Switch-B	VDD_MCU_GPIO RET_3V3	VDDSHV0_MCU	R	R		R			
CPU PWR HCPS-A	HCPS-A	VDD_CPU_AVS	VDD_CPU	R						
CORE PWR HCPS-B	HCPS-B	VDD_CORE_0V8	VDD_CORE, VDD_WAKE0, VDDA_0p8_CSIRX, VDDA_0P8_DSITX, VDDA_0P8_DSITX_C, VDDA_0P8_SERDES, VDDA_0P8_SERDES_C, VDDA_0P8_USB, VDDA_0P8_UFS	R						
TLV73318P-Q1	LDO-G	VPP_EFUSE_1V8	VPP_x(EFUSE)						R	
TLV3333-Q1	LDO-F	VDD_USB_3V3	VDDA_3P3_USB	R						R
TLV7103318-Q1	LDO-E	VDD_SD_DV	VDDSHV5 (3.3V or 1.8V)	R				R		
TPS74501P-Q1	LDO-D	VDD1_DDR_1V8	Mem: VDD1	R		R				
TPS74501P-Q1	LDO-C	VDD_MCU_GPIO RET_0V8	VDD_MCU_WAKE1	R	R		R			
TPS74501P-Q1	LDO-B	VDA_PHY_1V8	VDDA_1P8_CSI_RX, VDDA_1P8_DSITX, VDDA_1P8_SERDES, VDDA_1P8_USB, VDDA_1P8_UFS	R						

Table 2-2. PDN-3A Power Map vs. System Features (continued)

Power Mapping				System Features(1)						
Device	Power Resource	Power Rails	Processor and Memory Domains	Active SoC	MCU Only	DDR Ret	GPIO Ret	SD Card	EFUSE	USB
TPS74501P-Q1	LDO-A	VDA_PLL_1V8	VDDA_OSC1, VDDA_PLLGRP13:0, VDDA_TEMP4:0	R						

(1) 'R' is required.

Table 2-3. Power Resource Adjustments for Feature Removal

Feature Removal	Power Resource and Power Rail Removal	New Supply Mappings
HS SoC EFUSE Programming	Discrete LDO-G: VPP_EFUSE_1V8	SoC: VPPs → No Connect
Compliant, USB 2.0 Data Eye	Discrete LDO-F: VDA_USB_3V3	SoC: VDDA_3P3_USB → Filtered VDD_IO_3V3
Compliant, High-Speed SD Card	Discrete LDO-E: VDD_SD_DV	SoC: VDDSHV5 → VDD_IO_3V3 or VDD_IO_1V8
DDR Retention Low Power Mode	Discrete LDO-D: VDD1_DDR_1V8	LPDDR4: VDD1 → VDD_IO_1V8
MCU GPIO Retention Low Power Mode	Discrete LDO-C: VDD_MCU_GPIORET_0V8	SoC: VDD_MCU_WAKE1 → VDD_MCU_0V85
	Discrete LDSW-B: VDD_MCU_GPIORET_3V3	SoC: VDDSHV0_MCU → VDD_MCUIO_3V3 or VDD_MCUIO_1V8
	Discrete SVS	PMIC: GPIO10 pulled up to VCCA_3V3

2.2 Control Mapping

Figure 2-4 shows the digital control signal mapping for PDN-3A between the PMIC, discrete power resources, and the processor. These connections enable a full feature system including MCU Only, DDR and GPIO Retention low power modes, functional safety up to ASIL-D, and compliant USB2.0, UHS-I SD card, and HS SoC eFuse programming on-board.

In this PDN, GPIO8 has been designed to provide run-time PDN configuration resulting in a flexible PMIC that adapts to each board design. A logic low input at the beginning of the power up sequence commands the PMIC to support isolated MCU and Main power groups which includes BUCK5 in the power up sequence. A logic high commands the PMIC to group MCU & Main power groups and exclude BUCK5 from power sequences. For isolated PDN scheme (variants A - F), the GPIO8 pin is connected to HCPS buck enable inputs which have a pull-up resistor to the input voltage of each buck. The VDA_DLL_0V8 power rail (sourced from LDO3 of the PMIC) is enabled at the same time stamp as the CPU & CORE rails. Therefore, it can be used to drive the input to a low voltage translator with an open-drain output that connects to HCPS enable net (MAIN_PWRGRP_IRQn). This buck pin is bi-directioinal and acts as both an enable input and status output. Internal buck faults result in the pin pulling the MAIN_PWRGRP_IRQn net low. Pulling the MAIN_PWRGRP_IRQn net low disables the buck and asserts an interrupt to PMIC via GPIO8 net connection. If GPIO8 goes low, the PMIC reacts as if SOC_PWR_ERROR has occurred causing a PDN state transition to MCU Only mode.

After the nRSTOUT PMIC signal goes high at the end of the TO_ACTIVE Sequence shown in Figure 5-11, GPIO10 is pulled high awaiting an active low MCU_PWRGRP_IRQn interrupt signal from the SVS-B voltage monitor. If GPIO10 goes low, the PMIC reacts as if an MCU_PWR_ERROR has occurred and executes an orderly shutdown. As shown in Figure 2-4, connect GPIO8 and GPIO10 with a 3.3V level translator from VDA_DLL_0V8 (PMIC LDO3) and the open drain interrupt outputs from voltage monitors SVS-A and SVS-B, respectively.

Other digital connections from the PMIC to the processor provide error monitoring, processor reset, processor wake up, and system low-power modes. Specific GPIO pins have been assigned to key signals in order to maintain proper operation during low power modes when only a few GPIO pins remain operational.

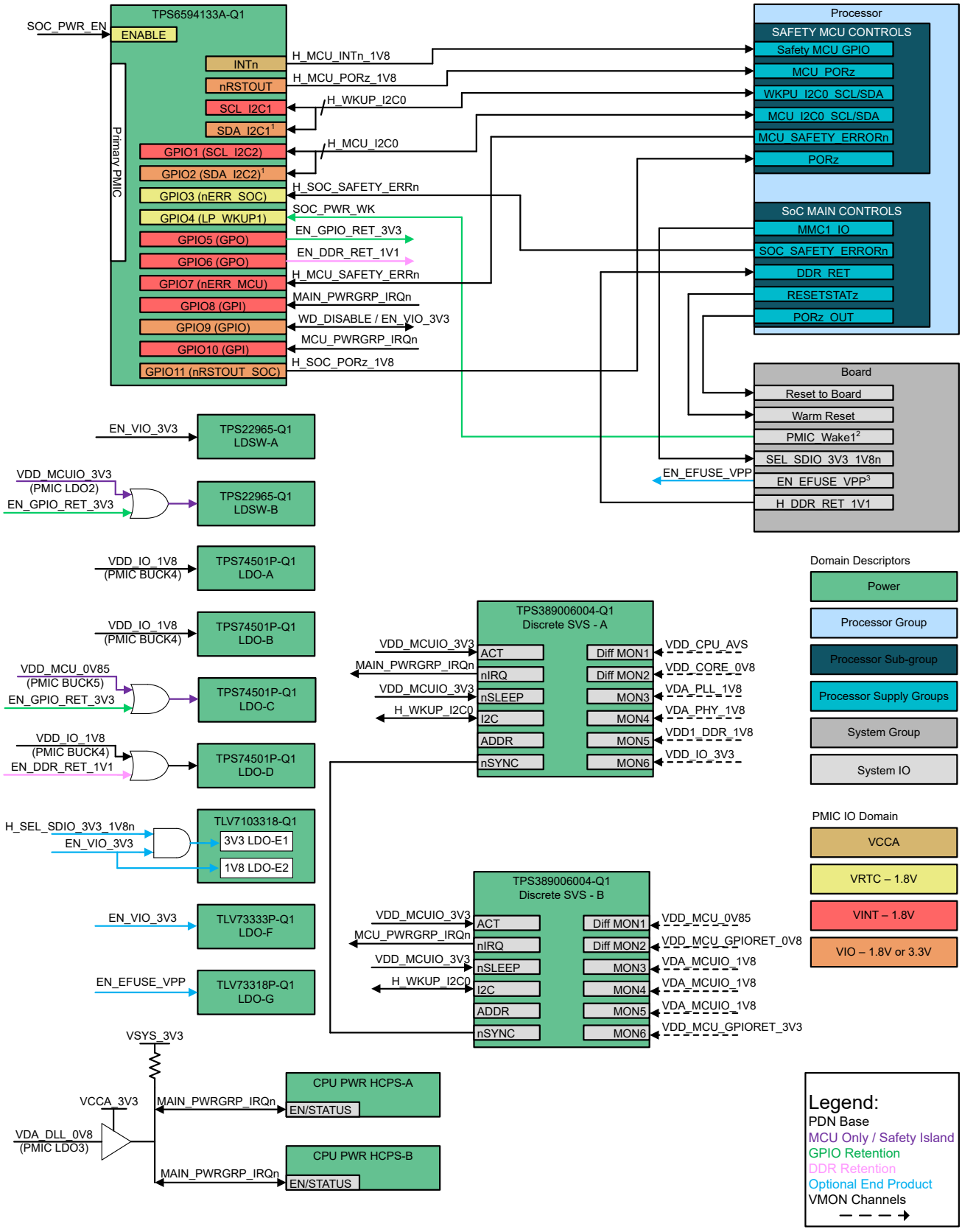


Figure 2-4. TPS6594133A Digital Connections for PDN-3A

1. PMIC IO can have distinct power domains for input and output functionality. The SDA function for I2C1 and I2C2 use the VINT voltage domain as an input and the VIO voltage domain as an output. For more information, see the device data sheet. The PMIC voltage domains indicated are for the TPS6594133A NVM configuration.
2. PMIC_Wake1 is typically a CAN PHY INH output.
3. LP_WKUP1 and WKUP1 transition to the ACTIVE state.

Note

For SVS-B, only VDD_MCU_GPIORET_0V8 and VDD_MCU_GPIORET_3V3 connections are need to provide OV/UV coverage on the MCU input supplies. The other connections shown in Table 5-1 allow the same SVS PN to be used for both SVS-A and SVS-B.

Note

The PMIC voltage domain of an IO can be different depending upon configuration. When configured as an input GPIO3 and GPIO4 are in the VRTC domain. When configured as an output, GPIO3 and GPIO4 are in the VINT domain.

Note

In addition to the I2C signals, five additional signals are open-drain outputs and require a pullup to a specific power rail. For a list of the signals and the specific power rail, see Table 2-4.

Table 2-4. Open-Drain Signals and Power Rail

PDN Signal	Pullup Power Rail
H_MCU_INTn_1V8	VDD_MCUIO_1V8
H_MCU_PORz_1V8	VDA_MCU_1V8
H_SOC_PORz_1V8	VDA_MCU_1V8
H_MCU_PORz_1V8	VDA_MCU_1V8
EN_DDR_RET_1V1	VDD_DDR_1V1
H_WKUP_I2C0	VDD_GPIORET_IO_3V3
H_MCU_I2C0	VDD_GPIORET_IO_3V3

Use Table 2-5 as a guide to understand GPIO assignments required for each PDN system feature. If the feature listed is not required, the digital connection can be removed; however, the GPIO pin is still configured per NVM defined default function shown. After the processor has booted up, the processor can reconfigure unused GPIOs to support new functions. Reconfiguration is possible as long as that function is only needed after boot and default function does not cause any conflicts with normal operations (for example, two outputs driving same net). For details on how functional safety related connections help achieve functional safety system-level goals, see Section 3.

Table 2-5. Digital Connections by System Feature

Device	GPIO Mapping			System Features[1]				
	PMIC Pin	NVM Function	PDN Signals	Active SoC	Functional Safety	MCU-Only	DDR Ret	GPIO Ret
TPS6594133A-Q1	nPWRON/ ENABLE	Enable	SOC_PWR_EN	R				
	nINT	INT	H_MCU_INTn		R			
	nRSTOUT	nRSTOUT	H_MCU_PORz_1V8	R				
	SCL_I2C1	SCL_I2C1	H_WKUP_I2C0_SCL	R				
	SDA_I2C1	SDA_I2C1	H_WKUP_I2C0_SDA	R				
	GPIO_1	SCL_I2C2	H_MCU_I2C0_SCL		R			
	GPIO_2	SDA_I2C2	H_MCU_I2C0_SDA		R			
	GPIO_3	nERR_SoC	H_SOC_SAFETY_ERRn	R				
	GPIO_4	LP_WKUP1[2]	SOC_PWR_WKn				R	R
	GPIO_5	EN_GPIO_RET_3V3	EN_GPIO_RET_3V3					R
	GPIO_6	EN_DDR_RET_1V1	EN_DDR_RET_1V1				R	
	GPIO_7	nERR_MCU	H_MCU_SAFETY_ERRn		R			
	GPIO_8	GPI	MAIN_PWRGRP_IRQn		R			
	GPIO_9	GPO	EN_3V3_VIO	R				
	GPIO_10	GPI	MCU_PWRGRP_IRQn		R			
	GPIO_11	nRSTOUT_SOC	H_SOC_PORz_1V8			R		

(1) R is Required. O is optional.
(2) LP_WKUP1 function is masked in the static settings. Instructions for unmasking the function are provided in Section 6.2.3, Section 6.3 and Section 6.4.

3 Supporting Functional Safety Systems

By using the PDN-3A power solution, the system can leverage the following PMIC functional safety features:

- Input Supply Monitoring
- Output Voltage and Current Monitoring
- Question and Answer Watchdog
- Fault Reporting Interrupts
- Enable Drive Pin that provides an independent path to disable system actuators
- Error Pin Monitoring
- Internal Diagnostics including voltage monitoring, temperature monitoring, and built-in self-test

Refer to the Safety Manual of the TPS6594133A for full descriptions and analysis of the PMIC functional safety features. These functional safety features can assist in achieving up to ASIL-D rating for a system. Additionally, these features help in achieving the functional safety assumptions utilized by the processor to achieve up to ASIL-D rating. See the Safety Manual for Jacinto™ 7 Processors for a complete list of functional safety system assumptions.

3.1 Achieving ASIL-B System Requirements

To achieve a system functional safety level of ASIL-B, the following PDN features are available:

- PMIC over voltage and under voltage monitoring on the power resource voltage outputs
- Over voltage and under voltage monitoring on discrete power resources
- Watchdog monitoring of safety processor
- MCU error monitoring
- MCU reset
- I2C communication
- Error indicator, EN_DRV, for driving external circuitry (optional)
- Read-back of EN_DRV pin

For functional safety applications, as an in-line, external power FET must be placed between the output of the 5V or 3.3V supply and the VCCA line. The voltage before and after the FET is monitored by the PMIC, and the PMIC controls the FET through the OVPGDRV pin. The FET can quickly isolate the PMIC when an over-voltage event greater than 6V is detected on the input supply to protect the system from being damaged. This system protection includes all power rails sourced from the FET along the VCCA line. Any power connected upstream from the FET is not protected from over voltage events. In Figure 2-1 all power resources are connected after the FET to extend the over voltage protection to all processor domains and key discrete components. The only exceptions being the discrete LDOs for the SD card and 3.3V USB.

The PMIC internal over voltage and under voltage monitoring and their respective monitoring threshold levels are enabled by default and can be updated through I2C after start-up. PMIC power rails connected directly to the processor are monitored by default. Two TPS389006004 voltage monitors are used to monitor power resources not provided by the PMIC. Connect the interrupt signals of these voltage monitors to the PMIC as described in Section 2.2. The second voltage monitor SVS-B is not required if GPIO and DDR retention low power modes are not used.

The internal Q&A Watchdog is disabled on the TPS6594133A device by default and can be enabled after the powers up. Once the device is in ACTIVE state, the trigger or Q&A watchdog settings can be configured through I2C in the device. The I2C CRC is not enabled by default but must be enabled with the I2C_2 trigger described in Table 5-1. It is recommended to enable I2C CRC and wait a minimum of 2ms before starting the Q&A Watchdog. The steps for configuring and starting the watchdog can be found in the TPS6594-Q1 data sheet.

GPIO_7 of the TPS6594133A PMIC is configured as the MCU error signal monitor, and must be enabled though the ESM_MCU_EN register bit. MCU reset is supported through the connection between the PMIC nRSTOUT pin and the MCU_PORz of the processor. Lastly, there are two I2C ports between the TPS6594133A and the processor. The first is used for all non-watchdog communication, such as voltage level control, and the second allows the watchdog monitoring to be on an independent communication channel.

There is an option to use the EN_DRV of the TPS6594133A PMIC to indicate an error has been detected and the system is entering SAFE state. This signal can be utilized if the system has external circuitry that needs to be driven by an error event. In this PDN, the EN_DRV is not utilized, but available if needed.

3.2 Achieving up to ASIL-D System Requirements

For ASIL-C or ASIL-D systems, the following features in addition to the ones described in Section 3.1 can be used:

- PMIC over-voltage monitoring and protection on the input to the PMIC (VCCA)
- PMIC current monitoring on all output power rails
- SoC error monitoring
- Switch short-to-ground detection on BUCK regulator pins (SW_Bx)
- Residual Voltage Monitoring
- Read-back of Logic Output Pins
  - nINT of the PMIC
  - nRSTOUT and nRSTOUT_SOC of the PMIC

The current monitoring is enabled by default for all BUCKs and LDOs for the TPS6594133A.

GPIO_3 of the TPS6594133A PMIC is configured as the SoC error signal monitor. Similar to the MCU error signal monitor, this feature is enabled through I2C using the ESM_SOC_EN register bit. The SoC reset functionality is supported through the connection of GPIO_11 on the TPS6594133A, configured as nRSTOUT_SoC, to the PORz pin of the processor.

Table 3-1. System Level Safety Features

ASIL-B						**ASIL-D**	
Safety Monitoring Processor	External SW Wdog	INTn	Safety MCU Processing ESM Safety MCU Reset	Safety Status Signal with IO Read-Back feature	System Input Voltage Monitoring	SoC Main Processing ESM	IO Read-Back Feature
SoC: MCU Island R5 Cores	PMIC: Q&A Watchdog and I2C2	PMIC : nINT	PMIC: nERR_MCU connected to SOC: MCU_SAFETY_ERRz PMIC: nRSTOUT connected to MCU_PORz_1V8	PMIC: ENDRV	PMIC: VSYS_SENSE -OV with Safety FET OVPGDRV with VCCA OV & UV and SoC (VMON1) -UV	PMIC: nERR_SoC connected to SOC: SOC_SAFETY_ERRz	PMIC: nINT, nRSTOUT, nRSTOUT_SOC

Table 3-2. Power Monitoring Safety Features

				ASIL-B	**ASIL-D Adds**	
Device	Power Resource	PDN Power Rail	Safe State Power Group1	Supply Voltage Monitoring	Supply Current Monitoring	Residual Voltage Monitoring
TPS6594133A-Q1 (PMIC)	BUCK1-2	VDD_DDR_1V1	MCU	PMIC - OV and UV2	PMIC -CM2	PMIC -RVM2
	BUCK3	VDD_RAM_0V85	SOC	PMIC - OV and UV	PMIC -CM	PMIC -RVM
	BUCK4	VDD_IO_1V8	SOC	PMIC - OV and UV	PMIC -CM	PMIC -RVM
	BUCK5	VDD_MCU_0V85	MCU	PMIC - OV and UV	PMIC -CM	PMIC -RVM
	LDO1	VDD_MCUIO_1V8	MCU	PMIC - OV and UV	PMIC -CM	PMIC -RVM
	LDO2	VDD_MCUIO_3V3	MCU	PMIC - OV and UV	PMIC -CM	PMIC -RVM
	LDO3	VDA_DLL_0V8	SOC	PMIC - OV and UV	PMIC -CM	PMIC -RVM
	LDO4	VDA_MCU_1V8	MCU	PMIC - OV and UV	PMIC -CM	PMIC -RVM
TPS22965-Q1	LDSW- A	VDD_IO_3V3	SOC 6	Discrete SVS-A	NA4 5	
TPS22965-Q1	LDSW- B	VDD_MCU_GPIORET_3V3	MCU 6	Discrete SVS-B 8	NA	
HCPS-A	HCPS-A	VDD_CPU_AVS	SOC 6	Discrete SVS-A	BUCK-OC	
HCPS-B	HCPS-B	VDD_CORE_0V8	MCU 6	Discrete SVS-A	BUCK-OC	
TPS74501P-Q1	LDO-A	VDA_PLL_1V8	SOC 6	Discrete SVS-A	LDO-OCP 7	
TPS74501P-Q1	LDO-B	VDA_PHY_1V8	SOC 6	Discrete SVS-A	LDO-OCP 7	
TPS74501P-Q1	LDO-C	VDD_MCU_GPIORET_0V8	MCU 6	Discrete SVS-B 8	LDO-OCP 7	
TPS74501P-Q1	LDO-D	VDD1_DDR_1V8	SOC 6	Discrete SVS-A	LDO-OCP 7	
TLV7103318-Q1	LDO-E	VDD_SD_DV	None	NA 3	NA 3	
TLV73333P-Q1	LDO-F	VDA_USB_3V3	None	NA 3	NA 3	

Table 3-2. Power Monitoring Safety Features (continued)

				ASIL-B	ASIL-D Adds
TLV73318P-Q1	LDO-G	VPP_EFUSE_1V8	None	NA 3	NA 3

1. Rail Group settings for the TPS6594133A-Q1 is found in Table 4-7.
2. Power rail VDD_DDR_1V1 is *safety critical* but do not required direct voltage or current monitoring since other means are available (for example, SoC internal *timeout gaskets* and *ECC checkers*) provide diagnostic coverage to detect faults in the DDR voltage.
3. Power rails VDD_SD_DV, VPP_EFUSE_1V8, and VDA_USB_3V38 are *not safety critical*.
4. Power rail VDD_IO_3V3 is typically *not safety critical* since other means are available (for example, *black-channel checkers*) to provide diagnostic coverage to detect faults in SoC signaling interfaces (for example, CAN, UART, and SPI).
5. If an SoC GPIO control signal is used in a *safety critical* interface, then adding voltage and current monitoring to specific VIO power rail can be needed per customer's end product design.
6. For power resources not provided by the PMIC, the power group is determined by discrete SVS voltage monitor.
7. These discrete power resource feature built-in over current protection and a power good signal that can be routed back to the PMIC.
8. Discrete SVS-B is unnecessary in systems without LDSW-B and LDO-C.

4 Static NVM Settings

The TPS6594133A-Q1 device consists of user register space and an NVM. The settings in NVM, which are loaded into the user registers during the transition from INIT to BOOT BIST, are provided in this section. Note: The user registers can be changed during state transitions, such as moving from STANDBY to ACTIVE mode. The user register map is described in the TPS6594-Q1 data sheet.

4.1 Application-Based Configuration Settings

In the TPS6594133A data sheet, there are seven application-based configurations for each BUCK to operate within. The following list includes the different configurations available:

- 4.4MHz VOUT Less than 1.9V, Multiphase or High COUT Single Phase
- 2.2MHz Single Phase for DDR Termination
- 4.4MHz VOUT Less than 1.9V, Low COUT, Single Phase Only
- 4.4MHz VOUT Greater than 1.7V, Single Phase Only
- 2.2MHz Full VOUT Range and VIN Greater than 4.5V, Single Phase Only
- 2.2MHz VOUT Less than 1.9V Multiphase or Single Phase
- 2.2MHz Full VOUT and Full VIN Range, Single Phase Only

The seven configurations also have optimal output inductance values that optimize the performance of each buck under these various conditions. Table 4-1 shows the default configurations for the BUCKs. The loop parameters associated with the use cases cannot be changed after device startup.

Table 4-1. Application Use Case Settings

Device	BUCK Rail	Default Application Use Case	Recommended Inductor Value
TPS6594133A-Q1	BUCK1	4.4MHz VOUT Less than 1.9V, Multiphase	220nH
	BUCK2	4.4MHz VOUT Less than 1.9V, Multiphase	220nH
	BUCK3	4.4MHz VOUT Less than 1.9V, Low COUT, Single Phase Only	220nH
	BUCK4	4.4MHz VOUT Less than 1.9V, Low COUT, Single Phase Only	220nH
	BUCK5	4.4MHz VOUT Less than 1.9V, Low COUT, Single Phase Only	220nH

4.2 Device Identification Settings

These settings are used to distinguish which device is detected in a system. These settings cannot be changed after device startup.

Table 4-2. Device Identification NVM Settings

Register Name	Field Name	TPS6594	
		Value	Description
DEV_REV	DEVICE_ID	0x82	
NVM_CODE_1	TI_NVM_ID	0x3a	
NVM_CODE_2	TI_NVM_REV	0x5	
PHASE_CONFIG	MP_CONFIG	0x2	2+1+1+1

4.3 BUCK Settings

These settings detail the voltages, configurations, and monitoring of the BUCK rails stored in the NVM. All these settings can be changed though I2C after startup. Some settings, typically the enable bits, are also changed by the PFSM, as described in Section 5.3.

After the Section 5.3.8 sequence has completed, the BUCKx_EN bit is set for BUCK1, BUCK3, BUCK4, and BUCK5 in the TPS6594133A. The BUCKx_RV_SEL bit is cleared for all BUCKs. The other bits remain unchanged, but they are still accessible via I2C.

Table 4-3. BUCK NVM Settings

Register Name	Field Name	TPS6594	
		Value	Description
BUCK1_CTRL	BUCK1_EN	0x0	Disabled; BUCK1 regulator
	BUCK1_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK1_FPWM_MP	0x0	Automatic phase adding and shedding.
	BUCK1_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK1_VSEL	0x0	BUCK1_VOUT_1
	BUCK1_PLDN	0x1	Enabled; Pull-down resistor
	BUCK1_RV_SEL	0x1	Enabled
BUCK1_CONF	BUCK1_SLEW_RATE	0x4	2.5 mV/µs
	BUCK1_ILIM	0x5	5.5 A
BUCK2_CTRL	BUCK2_EN	0x0	Disabled; BUCK2 regulator
	BUCK2_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK2_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK2_VSEL	0x0	BUCK2_VOUT_1
	BUCK2_PLDN	0x1	Enabled; Pull-down resistor
	BUCK2_RV_SEL	0x1	Enabled
BUCK2_CONF	BUCK2_SLEW_RATE	0x4	2.5 mV/µs
	BUCK2_ILIM	0x5	5.5 A
BUCK3_CTRL	BUCK3_EN	0x0	Disabled; BUCK3 regulator
	BUCK3_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK3_FPWM_MP	0x0	Automatic phase adding and shedding.
	BUCK3_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK3_VSEL	0x0	BUCK3_VOUT_1
	BUCK3_PLDN	0x1	Enabled; Pull-down resistor
	BUCK3_RV_SEL	0x1	Enabled
BUCK3_CONF	BUCK3_SLEW_RATE	0x4	2.5 mV/µs
	BUCK3_ILIM	0x5	5.5 A

Table 4-3. BUCK NVM Settings (continued)

Register Name	Field Name	TPS6594	
		Value	Description
BUCK4_CTRL	BUCK4_EN	0x0	Disabled; BUCK4 regulator
	BUCK4_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK4_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK4_VSEL	0x0	BUCK4_VOUT_1
	BUCK4_PLDN	0x1	Enabled; Pull-down resistor
	BUCK4_RV_SEL	0x1	Enabled
BUCK4_CONF	BUCK4_SLEW_RATE	0x3	5.0 mV/µs
	BUCK4_ILIM	0x5	5.5 A
BUCK5_CTRL	BUCK5_EN	0x0	Disabled; BUCK5 regulator
	BUCK5_FPWM	0x0	PFM and PWM operation (AUTO mode).
	BUCK5_VMON_EN	0x0	Disabled; OV, UV, SC and ILIM comparators.
	BUCK5_VSEL	0x0	BUCK5_VOUT_1
	BUCK5_PLDN	0x1	Enable Pull-down resistor
	BUCK5_RV_SEL	0x1	Enabled
BUCK5_CONF	BUCK5_SLEW_RATE	0x4	2.5 mV/µs
	BUCK5_ILIM	0x3	3.5 A
BUCK1_VOUT_1	BUCK1_VSET1	0x73	1.10 V
BUCK1_VOUT_2	BUCK1_VSET2	0x73	1.10 V
BUCK2_VOUT_1	BUCK2_VSET1	0x73	1.10 V
BUCK2_VOUT_2	BUCK2_VSET2	0x73	1.10 V
BUCK3_VOUT_1	BUCK3_VSET1	0x41	0.850 V
BUCK3_VOUT_2	BUCK3_VSET2	0x41	0.850 V
BUCK4_VOUT_1	BUCK4_VSET1	0xb2	1.80 V
BUCK4_VOUT_2	BUCK4_VSET2	0xb2	1.80 V
BUCK5_VOUT_1	BUCK5_VSET1	0x41	0.850 V
BUCK5_VOUT_2	BUCK5_VSET2	0x41	0.850 V
BUCK1_PG_WINDOW	BUCK1_OV_THR	0x3	+5% / +50 mV
	BUCK1_UV_THR	0x3	-5% / -50 mV
BUCK2_PG_WINDOW	BUCK2_OV_THR	0x3	+5% / +50 mV
	BUCK2_UV_THR	0x3	-5% / -50 mV
BUCK3_PG_WINDOW	BUCK3_OV_THR	0x3	+5% / +50 mV
	BUCK3_UV_THR	0x3	-5% / -50 mV
BUCK4_PG_WINDOW	BUCK4_OV_THR	0x3	+5% / +50 mV
	BUCK4_UV_THR	0x3	-5% / -50 mV
BUCK5_PG_WINDOW	BUCK5_OV_THR	0x3	+5% / +50 mV
	BUCK5_UV_THR	0x3	-5% / -50 mV

4.4 LDO Settings

These settings detail the voltages, configurations, and monitoring of the LDO rails stored in the NVM. All these settings can be changed though I2C after startup. Some settings, typically the enable bits, are also changed by the PFSM, as described in Section 5.3.

After the Section 5.3.8 sequence has completed, the LDOx_EN and LDOx_VMON_EN bits are set and the LDOx_RV_SEL bit is cleared for all LDOs. LDO2 _BYPASS is 0 when power is first applied but changes to 1 if PMIC detects VCCA centered around 3.3V. The other bits remain unchanged, but they are still accessible via I2C.

Table 4-4. LDO NVM Settings

		TPS6594	
Register Name	**Field Name**	**Value**	**Description**
LDO1_CTRL	LDO1_EN	0x0	Disabled; LDO1 regulator.
	LDO1_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
	LDO1_PLDN	0x1	125 Ohm
	LDO1_VMON_EN	0x0	Disable OV and UV comparators.
	LDO1_RV_SEL	0x1	Enabled
LDO2_CTRL	LDO2_EN	0x0	Disabled; LDO2 regulator.
	LDO2_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
	LDO2_PLDN	0x1	125 Ohm
	LDO2_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO2_RV_SEL	0x1	Enabled
LDO3_CTRL	LDO3_EN	0x0	Disabled; LDO3 regulator.
	LDO3_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
	LDO3_PLDN	0x1	125 Ohm
	LDO3_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO3_RV_SEL	0x1	Enabled
LDO4_CTRL	LDO4_EN	0x0	Disabled; LDO4 regulator.
	LDO4_SLOW_RAMP	0x0	25mV/us max ramp up slew rate for LDO output from 0.3V to 90% of LDOn_VSET
	LDO4_PLDN	0x1	125 Ohm
	LDO4_VMON_EN	0x0	Disabled; OV and UV comparators.
	LDO4_RV_SEL	0x1	Enabled
LDO1_VOUT	LDO1_VSET	0x1c	1.80 V
	LDO1_BYPASS	0x0	Linear regulator mode.
LDO2_VOUT	LDO2_VSET	0x3a	3.30 V
	LDO2_BYPASS	0x0	Linear regulator mode.
LDO3_VOUT	LDO3_VSET	0x8	0.80 V
	LDO3_BYPASS	0x0	Linear regulator mode.
LDO4_VOUT	LDO4_VSET	0x38	1.800 V
LDO1_PG_WINDOW	LDO1_OV_THR	0x3	+5% / +50 mV
	LDO1_UV_THR	0x3	-5% / -50 mV
LDO2_PG_WINDOW	LDO2_OV_THR	0x7	+10% / +100mV
	LDO2_UV_THR	0x7	-10%/ -100mV
LDO3_PG_WINDOW	LDO3_OV_THR	0x3	+5% / +50 mV
	LDO3_UV_THR	0x3	-5% / -50 mV

Table 4-4. LDO NVM Settings (continued)

Register Name	Field Name	TPS6594	
		Value	Description
LDO4_PG_WINDOW	LDO4_OV_THR	0x3	+5% / +50 mV
	LDO4_UV_THR	0x3	-5% / -50 mV

4.5 VCCA Settings

These settings detail the default monitoring on VCCA. When voltage is first applied to VCCA that is greater than UVLO, the PMIC sets VCCA_VMON_EN high and sets VCCA_PG_SET to 3.3V or 5V based on sensed VCCA voltage. The settings found in registers VCCA_VMON_CTRL and VCCA_PG_WINDOW can be changed though I2C after startup.

Table 4-5. VCCA NVM Settings

Register Name	Field Name	TPS6594	
		Value	Description
VCCA_VMON_CTRL	VMON_DEGLITCH_SEL	0x0	4 us
	VCCA_VMON_EN	0x0	Disabled; OV and UV comparators.
VCCA_PG_WINDOW	VCCA_OV_THR	0x7	+10%
	VCCA_UV_THR	0x7	-10%
	VCCA_PG_SET	0x1	5V
GENERAL_REG_1	FAST_VCCA_OVP	0x0	slow, 4us deglitch filter enabled
GENERAL_REG_3	LPM_EN_DISABLES_VCCA_VMON	0x1	VCCA_VMON enabled if VCCA_VMON_EN=1 and LPM_EN=0

4.6 GPIO Settings

These settings detail the default configurations of the GPIO rails. All of these settings can be changed though I2C after startup. Note that the contents of the GPIOx_SEL field determine which other fields in the GPIOx_CONF and GPIO_OUT_x registers are applicable. To understand which NVM fields apply to each GPIOx_SEL option, see the *Digital Signal Descriptions* section in TPS6594-Q1 data sheet.

Table 4-6. GPIO NVM Settings

Register Name	Field Name	TPS6594	
		Value	Description
GPIO1_CONF	GPIO1_OD	0x0	Push-pull output
	GPIO1_DIR	0x0	Input
	GPIO1_SEL	0x1	SCL_I2C2/CS_SPI
	GPIO1_PU_SEL	0x0	Pull-down resistor selected
	GPIO1_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO1_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO2_CONF	GPIO2_OD	0x0	Push-pull output
	GPIO2_DIR	0x0	Input
	GPIO2_SEL	0x2	SDA_I2C2/SDO_SPI
	GPIO2_PU_SEL	0x0	Pull-down resistor selected
	GPIO2_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO2_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO3_CONF	GPIO3_OD	0x0	Push-pull output
	GPIO3_DIR	0x0	Input
	GPIO3_SEL	0x2	NERR_SOC
	GPIO3_PU_SEL	0x0	Pull-down resistor selected
	GPIO3_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO3_DEGLITCH_EN	0x1	8 us deglitch time.

Table 4-6. GPIO NVM Settings (continued)

Register Name	Field Name	TPS6594	
		Value	Description
GPIO4_CONF	GPIO4_OD	0x0	Push-pull output
	GPIO4_DIR	0x0	Input
	GPIO4_SEL	0x6	LP_WKUP1
	GPIO4_PU_SEL	0x0	Pull-down resistor selected
	GPIO4_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO4_DEGLITCH_EN	0x1	8 us deglitch time.
GPIO5_CONF	GPIO5_OD	0x0	Push-pull output
	GPIO5_DIR	0x1	Output
	GPIO5_SEL	0x0	GPIO5
	GPIO5_PU_SEL	0x0	Pull-down resistor selected
	GPIO5_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO5_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO6_CONF	GPIO6_OD	0x1	Open-drain output
	GPIO6_DIR	0x1	Output
	GPIO6_SEL	0x0	GPIO6
	GPIO6_PU_SEL	0x0	Pull-down resistor selected
	GPIO6_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO6_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO7_CONF	GPIO7_OD	0x0	Push-pull output
	GPIO7_DIR	0x0	Input
	GPIO7_SEL	0x1	NERR_MCU
	GPIO7_PU_SEL	0x0	Pull-down resistor selected
	GPIO7_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO7_DEGLITCH_EN	0x1	8 us deglitch time.
GPIO8_CONF	GPIO8_OD	0x0	Push-pull output
	GPIO8_DIR	0x0	Input
	GPIO8_SEL	0x0	GPIO8
	GPIO8_PU_SEL	0x0	Pull-down resistor selected
	GPIO8_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO8_DEGLITCH_EN	0x1	8 us deglitch time.
GPIO9_CONF	GPIO9_OD	0x0	Push-pull output
	GPIO9_DIR	0x0	Input
	GPIO9_SEL	0x2	DISABLE_WDOG
	GPIO9_PU_SEL	0x0	Pull-down resistor selected
	GPIO9_PU_PD_EN	0x1	Enabled; Pull-up/pull-down resistor.
	GPIO9_DEGLITCH_EN	0x0	No deglitch, only synchronization.
GPIO10_CONF	GPIO10_OD	0x0	Push-pull output
	GPIO10_DIR	0x0	Input
	GPIO10_SEL	0x0	GPIO10
	GPIO10_PU_SEL	0x0	Pull-down resistor selected
	GPIO10_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO10_DEGLITCH_EN	0x1	8 us deglitch time.

Table 4-6. GPIO NVM Settings (continued)

Register Name	Field Name	TPS6594	
		Value	Description
GPIO11_CONF	GPIO11_OD	0x1	Open-drain output
	GPIO11_DIR	0x1	Output
	GPIO11_SEL	0x2	NRSTOUT_SOC
	GPIO11_PU_SEL	0x0	Pull-down resistor selected
	GPIO11_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	GPIO11_DEGLITCH_EN	0x0	No deglitch, only synchronization.
NPWRON_CONF	NPWRON_SEL	0x0	ENABLE
	ENABLE_PU_SEL	0x0	Pull-down resistor selected
	ENABLE_PU_PD_EN	0x0	Disabled; Pull-up/pull-down resistor.
	ENABLE_DEGLITCH_EN	0x0	No deglitch, only synchronization.
	ENABLE_POL	0x0	Active high
	NRSTOUT_OD	0x1	Open-drain output
GPIO_OUT_1	GPIO1_OUT	0x0	Low
	GPIO2_OUT	0x0	Low
	GPIO3_OUT	0x0	Low
	GPIO4_OUT	0x0	Low
	GPIO5_OUT	0x0	Low
	GPIO6_OUT	0x0	Low
	GPIO7_OUT	0x0	Low
	GPIO8_OUT	0x0	Low
GPIO_OUT_2	GPIO9_OUT	0x0	Low
	GPIO10_OUT	0x0	Low
	GPIO11_OUT	0x0	Low

4.7 Finite State Machine (FSM) Settings

These settings describe how the PMIC output rails are assigned to various system-level states. Also, the default trigger for each system-level state is described. All these settings can be changed though I2C after startup.

Table 4-7. FSM NVM Settings

Register Name	Field Name	TPS6594	
		Value	Description
RAIL_SEL_1	BUCK1_GRP_SEL	0x1	MCU rail group
	BUCK2_GRP_SEL	0x1	MCU rail group
	BUCK3_GRP_SEL	0x2	SOC rail group
	BUCK4_GRP_SEL	0x2	SOC rail group
RAIL_SEL_2	BUCK5_GRP_SEL	0x1	MCU rail group
	LDO1_GRP_SEL	0x1	MCU rail group
	LDO2_GRP_SEL	0x1	MCU rail group
	LDO3_GRP_SEL	0x2	SOC rail group
RAIL_SEL_3	LDO4_GRP_SEL	0x1	MCU rail group
	VCCA_GRP_SEL	0x1	MCU rail group
FSM_TRIG_SEL_1	MCU_RAIL_TRIG	0x2	MCU power error
	SOC_RAIL_TRIG	0x2	MCU power error
	OTHER_RAIL_TRIG	0x1	Orderly shutdown
	SEVERE_ERR_TRIG	0x0	Immediate shutdown
FSM_TRIG_SEL_2	MODERATE_ERR_TRIG	0x1	Orderly shutdown

4.8 Interrupt Settings

These settings detail the default configurations for what is monitored by nINT pin. All these settings can be changed though I2C after startup.

Table 4-8. Interrupt NVM Settings

Register Name	Field Name	TPS6594	
		Value	Description
FSM_TRIG_MASK_1	GPIO1_FSM_MASK	0x1	Masked
	GPIO1_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO2_FSM_MASK	0x1	Masked
	GPIO2_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO3_FSM_MASK	0x1	Masked
	GPIO3_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO4_FSM_MASK	0x1	Masked
	GPIO4_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_2	GPIO5_FSM_MASK	0x1	Masked
	GPIO5_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO6_FSM_MASK	0x1	Masked
	GPIO6_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO7_FSM_MASK	0x1	Masked
	GPIO7_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO8_FSM_MASK	0x1	Masked
	GPIO8_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_3	GPIO9_FSM_MASK	0x1	Masked
	GPIO9_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
	GPIO10_FSM_MASK	0x1	Masked
	GPIO10_FSM_MASK_POL	0x1	High; Masking sets signal value to '1'
	GPIO11_FSM_MASK	0x1	Masked
	GPIO11_FSM_MASK_POL	0x0	Low; Masking sets signal value to '0'
MASK_BUCK1_2	BUCK1_ILIM_MASK	0x0	Interrupt generated
	BUCK1_OV_MASK	0x0	Interrupt generated
	BUCK1_UV_MASK	0x0	Interrupt generated
	BUCK2_ILIM_MASK	0x0	Interrupt generated
	BUCK2_OV_MASK	0x0	Interrupt generated
	BUCK2_UV_MASK	0x0	Interrupt generated
MASK_BUCK3_4	BUCK3_ILIM_MASK	0x0	Interrupt generated
	BUCK3_OV_MASK	0x0	Interrupt generated
	BUCK3_UV_MASK	0x0	Interrupt generated
	BUCK4_OV_MASK	0x0	Interrupt generated
	BUCK4_UV_MASK	0x0	Interrupt generated
	BUCK4_ILIM_MASK	0x0	Interrupt generated
MASK_BUCK5	BUCK5_ILIM_MASK	0x0	Interrupt generated
	BUCK5_OV_MASK	0x0	Interrupt generated
	BUCK5_UV_MASK	0x0	Interrupt generated

Table 4-8. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS6594	
		Value	Description
MASK_LDO1_2	LDO1_OV_MASK	0x0	Interrupt generated
	LDO1_UV_MASK	0x0	Interrupt generated
	LDO2_OV_MASK	0x0	Interrupt generated
	LDO2_UV_MASK	0x0	Interrupt generated
	LDO1_ILIM_MASK	0x0	Interrupt generated
	LDO2_ILIM_MASK	0x0	Interrupt generated
MASK_LDO3_4	LDO3_OV_MASK	0x0	Interrupt generated
	LDO3_UV_MASK	0x0	Interrupt generated
	LDO4_OV_MASK	0x0	Interrupt generated
	LDO4_UV_MASK	0x0	Interrupt generated
	LDO3_ILIM_MASK	0x0	Interrupt generated
	LDO4_ILIM_MASK	0x0	Interrupt generated
MASK_VMON	VCCA_OV_MASK	0x0	Interrupt generated
	VCCA_UV_MASK	0x0	Interrupt generated
MASK_GPIO1_8_FALL	GPIO1_FALL_MASK	0x1	Interrupt not generated.
	GPIO2_FALL_MASK	0x1	Interrupt not generated.
	GPIO3_FALL_MASK	0x1	Interrupt not generated.
	GPIO4_FALL_MASK	0x1	Interrupt not generated.
	GPIO5_FALL_MASK	0x1	Interrupt not generated.
	GPIO6_FALL_MASK	0x1	Interrupt not generated.
	GPIO7_FALL_MASK	0x1	Interrupt not generated.
	GPIO8_FALL_MASK	0x1	Interrupt not generated.
MASK_GPIO1_8_RISE	GPIO1_RISE_MASK	0x1	Interrupt not generated.
	GPIO2_RISE_MASK	0x1	Interrupt not generated.
	GPIO3_RISE_MASK	0x1	Interrupt not generated.
	GPIO4_RISE_MASK	0x1	Interrupt not generated.
	GPIO5_RISE_MASK	0x1	Interrupt not generated.
	GPIO6_RISE_MASK	0x1	Interrupt not generated.
	GPIO7_RISE_MASK	0x1	Interrupt not generated.
	GPIO8_RISE_MASK	0x1	Interrupt not generated.
MASK_GPIO9_11 / MASK_GPIO9_10	GPIO9_FALL_MASK	0x1	Interrupt not generated.
	GPIO9_RISE_MASK	0x1	Interrupt not generated.
	GPIO10_FALL_MASK	0x0	Interrupt generated
	GPIO11_FALL_MASK	0x1	Interrupt not generated.
	GPIO10_RISE_MASK	0x1	Interrupt not generated.
	GPIO11_RISE_MASK	0x1	Interrupt not generated.
MASK_STARTUP	NPWRON_START_MASK	0x1	Interrupt not generated.
	ENABLE_MASK	0x0	Interrupt generated
	FSD_MASK	0x1	Interrupt not generated.
	SOFT_REBOOT_MASK	0x0	Interrupt generated
MASK_MISC	TWARN_MASK	0x0	Interrupt generated
	BIST_PASS_MASK	0x0	Interrupt generated
	EXT_CLK_MASK	0x1	Interrupt not generated.

Table 4-8. Interrupt NVM Settings (continued)

Register Name	Field Name	TPS6594	
		Value	Description
MASK_MODERATE_ERR	BIST_FAIL_MASK	0x0	Interrupt generated
	REG_CRC_ERR_MASK	0x0	Interrupt generated
	SPMI_ERR_MASK	0x1	Interrupt not generated.
	NPWRON_LONG_MASK	0x1	Interrupt not generated.
	NINT_READBACK_MASK	0x0	Interrupt generated
	NRSTOUT_READBACK_ MASK	0x0	Interrupt generated
MASK_FSM_ERR	IMM_SHUTDOWN_MASK	0x0	Interrupt generated
	MCU_PWR_ERR_MASK	0x0	Interrupt generated
	SOC_PWR_ERR_MASK	0x0	Interrupt generated
	ORD_SHUTDOWN_MASK	0x0	Interrupt generated
MASK_COMM_ERR	COMM_FRM_ERR_MASK	0x0	Interrupt generated
	COMM_CRC_ERR_MASK	0x0	Interrupt generated
	COMM_ADR_ERR_MASK	0x0	Interrupt generated
	I2C2_CRC_ERR_MASK	0x0	Interrupt generated
	I2C2_ADR_ERR_MASK	0x0	Interrupt generated
MASK_READBACK_ERR	EN_DRV_READBACK_ MASK	0x0	Interrupt generated
	NRSTOUT_SOC_ READBACK_MASK	0x0	Interrupt generated
MASK_ESM	ESM_SOC_PIN_MASK	0x0	Interrupt generated
	ESM_SOC_RST_MASK	0x0	Interrupt generated
	ESM_SOC_FAIL_MASK	0x0	Interrupt generated
	ESM_MCU_PIN_MASK	0x0	Interrupt generated
	ESM_MCU_RST_MASK	0x0	Interrupt generated
	ESM_MCU_FAIL_MASK	0x0	Interrupt generated
GENERAL_REG_1	PFSM_ERR_MASK	0x0	Interrupt generated

4.9 POWERGOOD Settings

These settings detail the default configurations for what is monitored by PGOOD pin. All these settings can be changed though I2C after startup.

Table 4-9. POWERGOOD NVM Settings

Register Name	Field Name	TPS6594	
		Value	Description
PGOOD_SEL_1	PGOOD_SEL_BUCK1	0x0	Masked
	PGOOD_SEL_BUCK2	0x0	Masked
	PGOOD_SEL_BUCK3	0x0	Masked
	PGOOD_SEL_BUCK4	0x0	Masked
PGOOD_SEL_2	PGOOD_SEL_BUCK5	0x0	Masked
PGOOD_SEL_3	PGOOD_SEL_LDO1	0x0	Masked
	PGOOD_SEL_LDO2	0x0	Masked
	PGOOD_SEL_LDO3	0x0	Masked
	PGOOD_SEL_LDO4	0x0	Masked

Table 4-9. POWERGOOD NVM Settings (continued)

Register Name	Field Name	TPS6594	
		Value	Description
PGOOD_SEL_4	PGOOD_SEL_VCCA	0x0	Masked
	PGOOD_SEL_TDIE_WARN	0x0	Masked
	PGOOD_SEL_NRSTOUT	0x0	Masked
	PGOOD_SEL_NRSTOUT_ SOC	0x0	Masked
	PGOOD_POL	0x0	PGOOD signal is high when monitored inputs are valid
	PGOOD_WINDOW	0x0	Only undervoltage is monitored

4.10 Miscellaneous Settings

These settings detail the default configurations of additional settings, such as spread spectrum, BUCK frequency, and LDO timeout. All these settings, except for those in registers GENERAL_REG_0 and GENERAL_REG_1, can be changed though I2C after startup.

Note

The PFSM of the TPS6594133A uses SCRATCH_PAD_1 and SCRATCH_PAD_4. Please avoid writing to these bit fields.

Table 4-10. Miscellaneous NVM Settings

Register Name	Field Name	TPS6594	
		Value	Description
PLL_CTRL	EXT_CLK_FREQ	0x0	1.1 MHz
CONFIG_1	TWARN_LEVEL	0x0	130C
	TSD_ORD_LEVEL	0x0	140C
	I2C1_HS	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode controller code.
	I2C2_HS	0x0	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode controller code.
	EN_ILIM_FSM_CTRL	0x0	Buck/LDO regulators ILIM interrupts do not affect FSM triggers.
	NSLEEP1_MASK	0x0	NSLEEP1(B) affects FSM state transitions.
	NSLEEP2_MASK	0x0	NSLEEP2(B) affects FSM state transitions.
CONFIG_2	BB_CHARGER_EN	0x0	Disabled
	BB_VEOC	0x0	2.5V
	BB_ICHR	0x0	100uA
RECOV_CNT_REG_2	RECOV_CNT_THR	0xf	0xf
BUCK_RESET_REG	BUCK1_RESET	0x0	0x0
	BUCK2_RESET	0x0	0x0
	BUCK3_RESET	0x0	0x0
	BUCK4_RESET	0x0	0x0
	BUCK5_RESET	0x0	0x0
SPREAD_SPECTRUM_1	SS_EN	0x0	Spread spectrum disabled
	SS_MODE	0x1	Mixed dwell
	SS_DEPTH	0x0	No modulation
SPREAD_SPECTRUM_2	SS_PARAM1	0x7	0x7
	SS_PARAM2	0xc	0xc

Table 4-10. Miscellaneous NVM Settings (continued)

Register Name	Field Name	TPS6594	
		Value	Description
FREQ_SEL	BUCK1_FREQ_SEL	0x1	4.4 MHz
	BUCK2_FREQ_SEL	0x1	4.4 MHz
	BUCK3_FREQ_SEL	0x1	4.4 MHz
	BUCK4_FREQ_SEL	0x1	4.4 MHz
	BUCK5_FREQ_SEL	0x1	4.4 MHz
FSM_STEP_SIZE	PFSM_DELAY_STEP	0xb	0xb
LDO_RV_TIMEOUT_ REG_1	LDO1_RV_TIMEOUT	0xf	16ms
	LDO2_RV_TIMEOUT	0xf	16ms
LDO_RV_TIMEOUT_ REG_2	LDO3_RV_TIMEOUT	0xf	16ms
	LDO4_RV_TIMEOUT	0xf	16ms
USER_SPARE_REGS	USER_SPARE_1	0x0	0x0
	USER_SPARE_2	0x0	0x0
	USER_SPARE_3	0x0	0x0
	USER_SPARE_4	0x0	0x0
ESM_MCU_MODE_ CFG	ESM_MCU_EN	0x0	ESM_MCU disabled.
ESM_SOC_MODE_ CFG	ESM_SOC_EN	0x0	ESM_SoC disabled.
CUSTOMER_NVM_ID_REG	CUSTOMER_NVM_ID	0x0	0x0
RTC_CTRL_2	XTAL_EN	0x0	Crystal oscillator is disabled
	LP_STANDBY_SEL	0x0	LDOINT is enabled in standby state.
	FAST_BIST	0x0	Logic and analog BIST is run at BOOT BIST.
	STARTUP_DEST	0x3	ACTIVE
	XTAL_SEL	0x0	6 pF
PFSM_DELAY_REG_1	PFSM_DELAY1	0x2d	0x2d
PFSM_DELAY_REG_2	PFSM_DELAY2	0x9d	0x9d
PFSM_DELAY_REG_3	PFSM_DELAY3	0x0	0x0
PFSM_DELAY_REG_4	PFSM_DELAY4	0x0	0x0
GENERAL_REG_0	FAST_BOOT_BIST	0x0	LBIST is run during boot BIST
GENERAL_REG_1	REG_CRC_EN	0x1	Register CRC enabled
SCRATCH_PAD_REG_1	SCRATCH_PAD_1	0x0	0x0
SCRATCH_PAD_REG_2	SCRATCH_PAD_2	0x0	0x0
SCRATCH_PAD_REG_3	SCRATCH_PAD_3	0x0	0x0
SCRATCH_PAD_REG_4	SCRATCH_PAD_4	0x0	0x0

4.11 Interface Settings

These settings detail the default interface, interface configurations, and device addresses. These settings cannot be changed after device startup.

Table 4-11. Interface NVM Settings

Register Name	Field Name	TPS6594	
		Value	Description
SERIAL_IF_CONFIG	I2C_SPI_SEL	0x0	I2C
	I2C1_SPI_CRC_EN	0x0	CRC disabled
	I2C2_CRC_EN	0x0	CRC disabled
I2C1_ID_REG	I2C1_ID	0x48	0x48
I2C2_ID_REG	I2C2_ID	0x12	0x12

4.12 Multi-Device Settings

The PMIC is designed for working as a single PMIC; its SPMI for multiple PMICs internal communication is disabled. No any multi-device settings are needed.

4.13 Watchdog Settings

These settings detail the default watchdog addresses. These settings can be changed though I2C after startup.

Table 4-12. Watchdog NVM Settings

Register Name	Field Name	TPS6594	
		Value	Description
WD_LONGWIN_CFG	WD_LONGWIN	0xff	0xff
WD_THR_CFG	WD_EN	0x1	Watchdog enabled.

5 Pre-Configurable Finite State Machine (PFSM) Settings

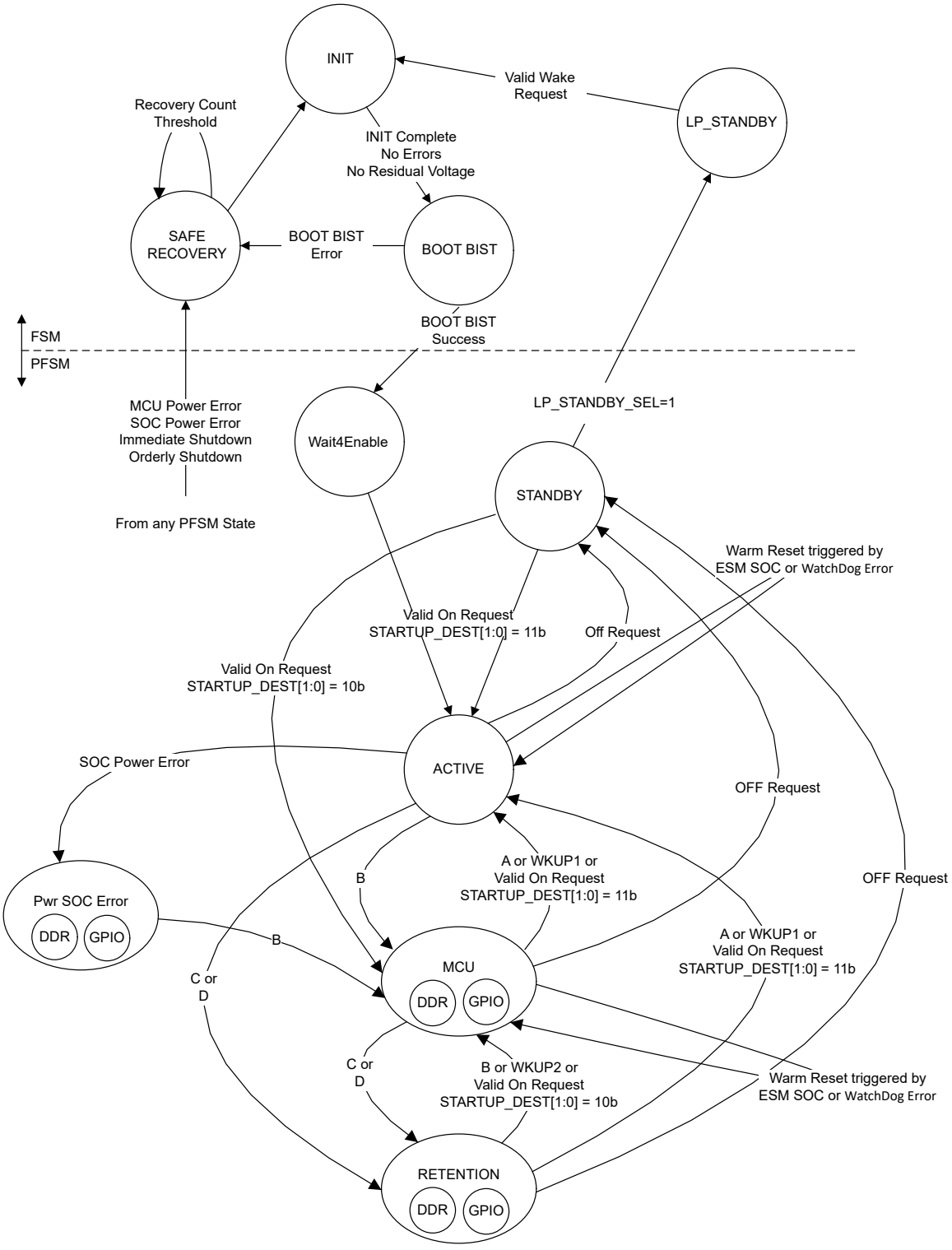
This section describes the default PFSM settings of the TPS6594133A devices. These settings cannot be changed after device startup.

5.1 Configured States

For the PDNs described in this user guide, the PMIC has the following five configured power states:

- Standby
- Wait4Enable
- Active
- MCU Only
- Pwr SoC Error
- Retention (GPIO and DDR)

In Figure 5-1, the configured PDN power states are shown, along with the transition conditions to move between the states. Additionally, the transitions to hardware states, such as SAFE RECOVERY and LP_STANDBY are shown. The hardware states are part of the fixed device power Finite State Machine (FSM) and described in the TPS6594-Q1 data sheet, see Section 8.



Trigger	NSLEEP2	NSLEEP1
A	1	1
B	1	0
C	0	1
D	0	0

Figure 5-1. Pre-Configurable Finite State Machine (PFSM) Mission States and Transitions

When the PMIC transitions from the FSM to the PFSM, several initialization instructions are performed to disable the residual voltage checks on both the BUCK and LDO regulators. Additionally, the FIRST_STARTUP_DONE bit is set and VCCA OV and UV masks are cleared (which are set in the static configurations, Table 4-8). After these instructions are executed the PMICs wait for a valid ON Request before entering the ACTIVE state. The definition for each power state is described below:

STANDBY The PMIC is powered by a valid supply on the system power rail (VCCA > VCCA_UV). All device resources are powered down in the STANDBY state. EN_DRV is forced low in this state. The processor is in the Off state, no voltage domains are energized. Refer to the Section 5.3.2 sequence description.

WAIT4ENABLE The WAIT4ENABLE state is entered when an error occurs and the PMIC transitions out of the PFSM mission states and into the FSM states. When the device returns from the FSM state the to PFSM the first state is represented by WAIT4ENABLE with all of the resources powered down and EN_DRV forced low. The sequence Section 5.3.1 is performed before the PMIC leaves the PFSM and enters the FSM state SAFE_RECOVERY.

ACTIVE The PMIC is powered by a valid supply. The PMIC is fully functional and supply power to all PDN loads. The processor has completed a recommended power up sequence with all voltage domains energized in both MCU and Main processor sections. Refer to the Section 5.3.8 sequence description.

MCU_ONLY The PMIC is powered by a valid supply. Only the power resources assigned to the MCU Safety Island are on. Refer to the Section 5.3.7 sequence description.

Pwr SoC Error The PMIC is powered by a valid supply. Only the power resources assigned to the MCU Safety Island are on. Refer to the Section 5.3.5 sequence description. The only active trigger is 'B', requiring the PMICs to return to the MCU_ONLY mode. The return to MCU_ONLY mode and eventually ACTIVE mode is only recommended after the interrupts which caused the SOC_PWR_ERROR have been cleared.

Retention The PMIC is powered by a valid supply. Only the power resources assigned to the retention rails are on or in LPM depending on the specific resource setting. If a given resource is maintained active, then all linked subsystems are automatically maintained active. ENABLE_DRV bit is cleared by the device in this state. If the I2C_5 bit is set high, the PMIC enters GPIO retention state. If the I2C_7 bit is set high, the PMIC enters DDR retention state. These bits need to be set before a trigger for the retention state occurs. Refer to the Section 5.3.9 sequence description.

5.2 PFSM Triggers

As shown in Figure 5-1, there are various triggers that can enable a state transition between configured states. Table 5-1 describes each trigger and its associated state transition from highest priority (Immediate Shutdown) to lowest priority (I2C_3). Active triggers of higher priority block triggers of lower priority and the associated sequence.

Table 5-1. State Transition Triggers

Trigger	Priority (ID)	Immediate (IMM)	REENTERANT	PFSM Current State	PFSM Destination State	Power Sequence or Function Executed
Immediate Shutdown(7)	0	True	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	SAFE(1)	TO_SAFE_SEVERE
MCU Power Error	1	True	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	SAFE(1)	TO_SAFE_ORDERLY
GPIO10 Low	2	True	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	SAFE(1)	
Orderly Shutdown(7)	3	True	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	SAFE(1)	

Table 5-1. State Transition Triggers (continued)

Trigger	Priority (ID)	Immediate (IMM)	REENTERANT	PFSM Current State	PFSM Destination State	Power Sequence or Function Executed
OFF Request	5(9)	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	STANDBY(2)	TO_STANDBY
WDOG Error	6	False	True	ACTIVE	ACTIVE	ACTIVE_TO_WARM
ESM MCU Error	7	False	True	ACTIVE	ACTIVE	
ESM SOC Error	8	False	True	ACTIVE	ACTIVE	ESM_SOC_ERROR
WDOG Error	9	False	True	MCU ONLY	MCU ONLY	MCU_TO_WARM
ESM MCU Error	10	False	True	MCU ONLY	MCU ONLY	
SOC Power Error	11	False	False	ACTIVE	MCU ONLY	PWR_SOC_ERR
GPIO8 Low	12	False	False	ACTIVE	MCU ONLY	
I2C_1 bit is high(3)	13	False	True	ACTIVE, MCU ONLY	No State Change	Execute RUNTIME BIST
I2C_2 bit is high(3)	14	False	True	ACTIVE, MCU ONLY	No State Change	Enable I^2C CRC on I^2C1 and I^2C2.(4)
ON Request	15	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	ACTIVE	TO_ACTIVE
WKUP1 goes high	16	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	ACTIVE	
NSLEEP1 and NSLEEP2 are high(5)	17	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	ACTIVE	
MCU ON Request	18	False	False	STANDBY, ACTIVE(6), MCU ONLY, Suspend-to-RAM	MCU ONLY	TO_MCU
WKUP2 goes high	19	False	False	STANDBY, ACTIVE, MCU ONLY, Suspend-to-RAM	MCU ONLY	
NSLEEP1 goes low and NSLEEP2 goes high(5)	20	False	False	ACTIVE, MCU ONLY, Suspend-to-RAM	MCU ONLY	
NSLEEP1 goes low and NSLEEP2 goes low(5)	21	False	False	ACTIVE, MCU ONLY	Suspend-to-RAM	TO_RETENTION
NSLEEP1 goes high and NSLEEP2 goes low(5)	22	False	False	ACTIVE, MCU ONLY	Suspend-to-RAM	
I2C_0 bit goes high(3)	23(8)	False	False	STANDBY, ACTIVE, MCU ONLY	LP_STANDBY(2)	TO_STANDBY

(1) From the SAFE state, the PFSM automatically transitions to the hardware FSM state of SAFE_RECOVERY. From the SAFE_RECOVERY state, the recovery counter is incremented and compared to the recovery count threshold (see RECOV_CNT_REG_2, in Table 4-10). If the recovery count threshold is reached, then the PMICs halt recovery attempts and require a power cycle. For more information, see the *TPS6594-Q1 Power Management IC (PMIC) with 5 BUCKs and 4 LDOs for Safety-Relevant Automotive Applications Data Sheet*.

(2) If the LP_STANDBY_SEL bit is set in the TPS6594133A-Q1 (see RTC_CTRL_2, in Table 4-10), then the PFSM transitions to the hardware FSM state of LP_STANDBY. When LP_STANDBY is entered, then please use the appropriate mechanism to wakeup the device as determined by the means of entering LP_STANDBY. For more information, see the *TPS6594-Q1 Power Management IC (PMIC) with 5 BUCKs and 4 LDOs for Safety-Relevant Automotive Applications Data Sheet*.

(3) I2C_0, I2C_1, and I2C_2 are self-clearing triggers.

(4) Enabling the I2C CRC, enables the CRC on both I2C1 and I2C2, however, the I2C2 is disabled for 2ms after the CRC is enabled. Be aware when using the watchdog Q&A before enabling I2C CRC. The recommendation is to enable the I2C CRC first, and then after 2ms, start the watchdog Q&A.

(5) NSLEEP1 and NSLEEP2 of the PMIC can be accessed through the GPIO pin or through a register bit. If either the register bit or the GPIO pin is pulled high, the NSLEEPx value is read as a *high* logic level.
(6) When in the ACTIVE mode, the ON Request to MCU ONLY trigger cannot be accessed while other higher priority triggers, like NSLEEP1=NSLEEP2=HIGH, are still active.
(7) These triggers can originate from the TPS6594133A.
(8) Trigger ID 23 not available until the NSLEEP bits are masked: NSLEEP2_MASK=NSLEEP1_MASK=1.
(9) Trigger IDs 4, 24, and 25 (not shown) are enabled and activated by the power sequences. These triggers are used to manage the transition between the PFSM and the FSM.

5.3 Power Sequences

5.3.1 TO_SAFE_SEVERE and TO_SAFE

The TO_SAFE_SEVERE and TO_SAFE are distinct sequences that occur before transitioning to the SAFE state. Both sequences shut down all rails without delay. The TO_SAFE_SEVERE sequence immediately ceases BUCK switching and enables the pulldown resistors of the BUCKs and LDOs. The objective of the TO_SAFE_SEVERE sequence is to prevent any damage to the PMIC in case of over voltage on VCCA or thermal shutdown. The timing is illustrated in Figure 5-2. The TO_SAFE sequence does not reset the BUCK regulators until after the regulators are turned off.

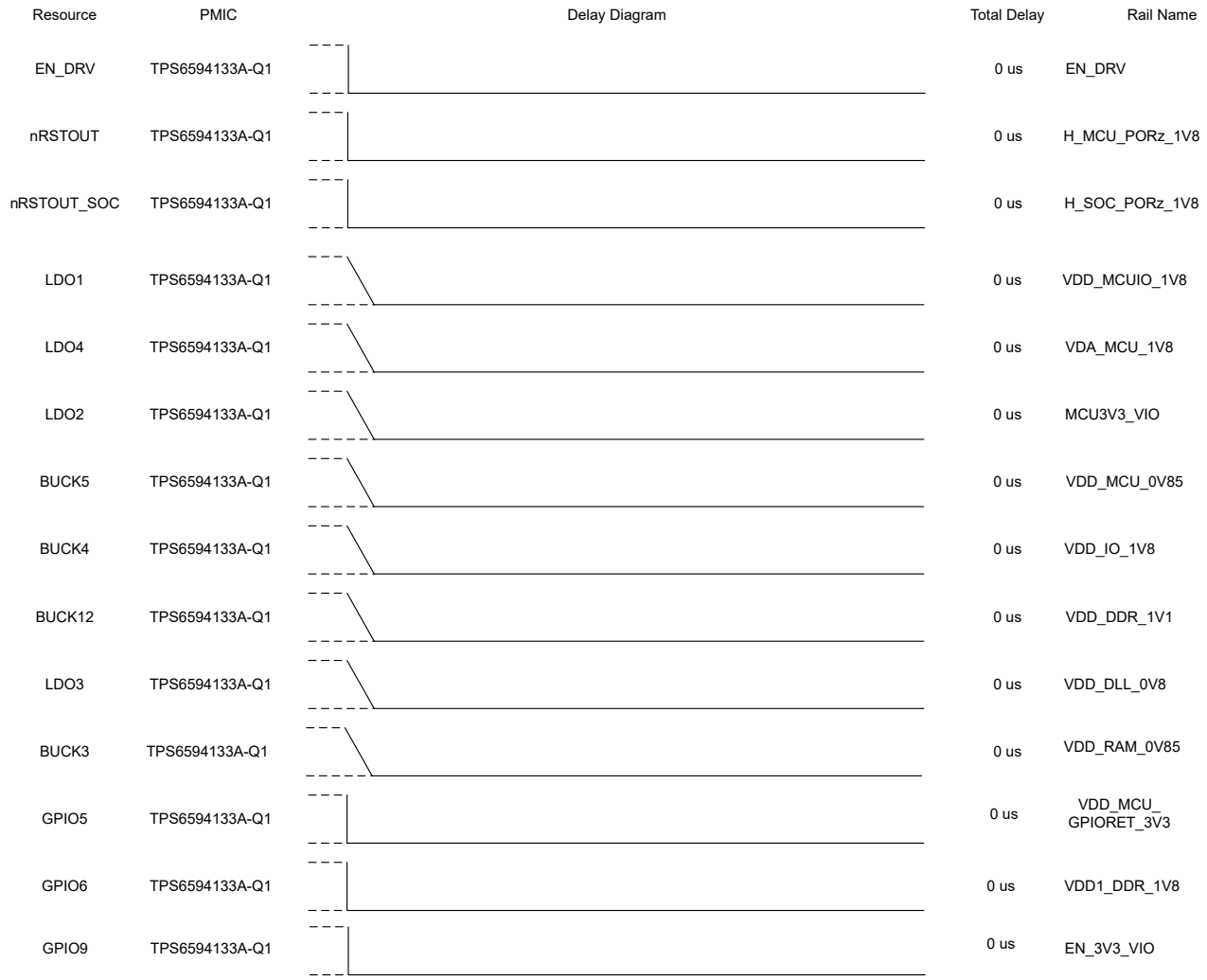


Figure 5-2. TO_SAFE_SEVERE and TO_SAFE Power Sequences

TO_SAFE sequence delays the TPS6594133A by 16 ms. The delay ensures that the PMIC finishes after . After these delays, the following instructions are executed on the PMIC:

After the power sequence shown in Figure 5-2, the TO_SAFE_SEVERE sequence executes the following instructions:

```
// TPS6594133A
// Clear AMUXOUT_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x00 MASK=0xEF
```

The TPS6594133A has an additional delay of 500 ms at the end of the TO_SAFE_SEVERE sequence. It is important to note that the recovery is not attempted until after the sequence delay is complete.

5.3.2 TO_SAFE_ORDERLY and TO_STANDBY

If a moderate error occurs, an orderly shutdown trigger is generated. This trigger shuts down the PMIC outputs using the recommended power down sequence and proceed to the SAFE state.

If an OFF request occurs, such as the ENABLE pin of the TPS6594133A device being pulled low, the same power down sequence occurs, except that the PMIC goes to STANDBY (LP_STANDBY_SEL=0) or LP_STANDBY (LP_STANDBY_SEL=1) states, rather than going to the SAFE state. The power sequence for both of these events is shown in Figure 5-3.

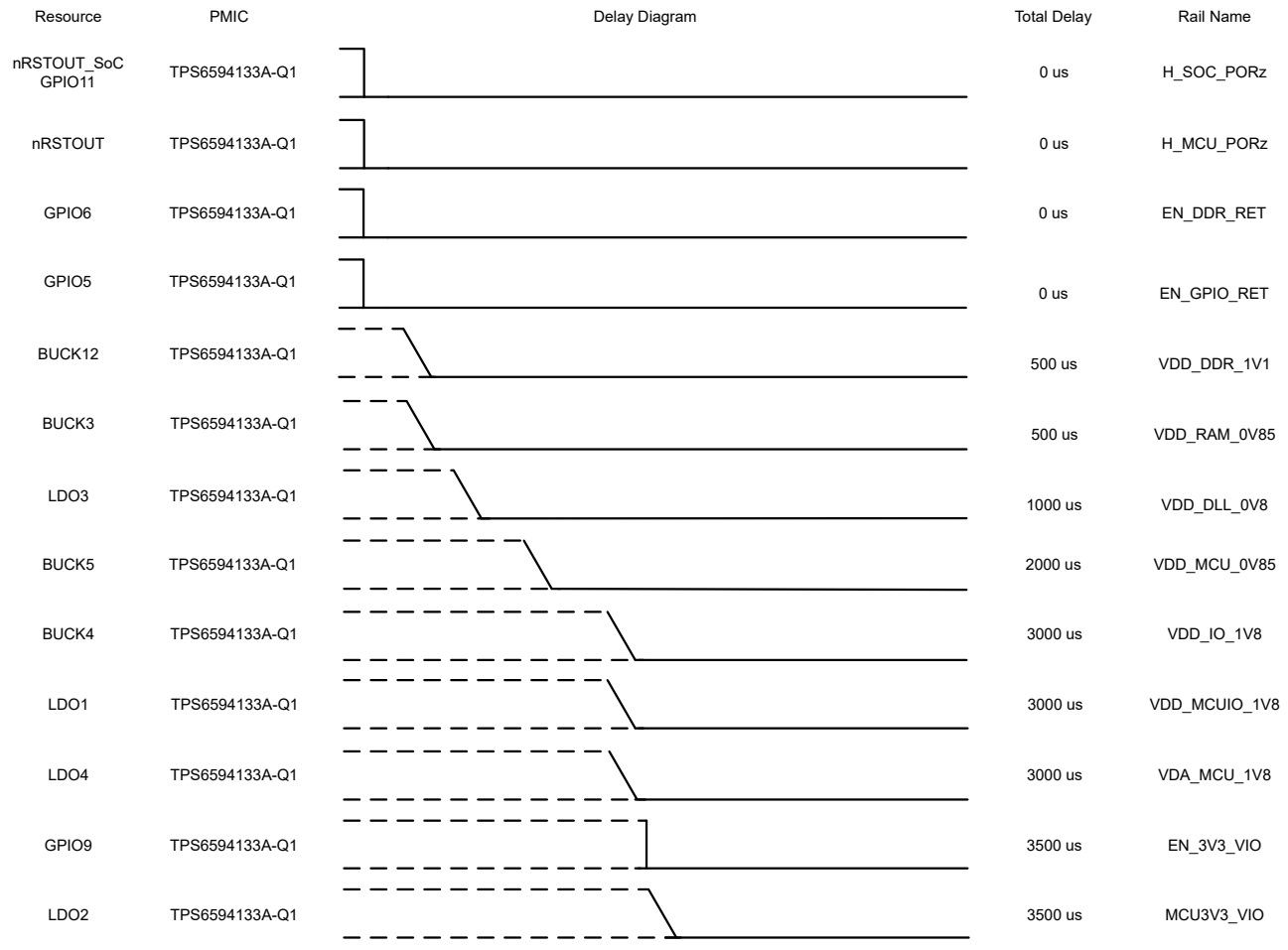


Figure 5-3. TO_SAFE_ORDERLY and TO_STANDBY Power Sequence

At the end of the TO_SAFE_ORDERLY the PMIC wait approximately 16ms before executing the following instructions:

```
 //TPS6594133A
// Set LPM_EN
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x04 MASK=0xEB
// Reset all BUCKs
REG_WRITE_MASK_IMM ADDR=0x87 DATA=0x1F MASK=0xE0
```

The resetting of the BUCK regulators is done in preparation to transitioning to the SAFE_RECOVERY state. SAFE_RECOVERY means that the PMIC leaves the mission state. The SAFE_RECOVERY state is where the recovery mechanism increments the recovery counter and determines if the recovery count threshold (see Table 4-10) is reached before attempting to recover.

At the end of the TO_STANDBY sequence, the same AMUXOUT_EN, CLKMON_EN, and LPM_EN bit manipulations are made in the PMIC. The BUCKs are not reset. After these instructions, the PMIC performs an additional check to determine if the LP_STANDBY_SEL (see Table 4-10) is true. If true then the PMICs enter the LP_STANDBY state and leave the mission state. If the LP_STANDBY_SEL is false, then the PMICs remain in the mission state defined by STANDBY in Section 5.1.

5.3.3 ACTIVE_TO_WARM

The ACTIVE_TO_WARM sequence can be triggered by either a watchdog or ESM_MCU error. In the event of a trigger, the nRSTOUT and nRSTOUT_SOC signals are driven low and the recovery count (register RECOV_CNT_REG_1) increments. Then, all BUCKs and LDOs are reset to their default voltages. The PMIC remains in the ACTIVE state.

Note

GPIOs do not reset during the sequence as shown in Figure 5-4

At the beginning of the sequence the following instructions are executed:

```
//TPS6594133A
// Set FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x08 MASK=0xF7
// Clear nRSTOUT and nRSTOUT_SOC
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x00 MASK=0xFC
// Increment the recovery counter
REG_WRITE_MASK_IMM ADDR=0xa5 DATA=0x01 MASK=0xFE
```

Note

The watchdog or ESM error is an indication of a significant error that has taken place outside of the PMIC. The PMIC does not actually transition through the safe recovery as with an MCU_POWER_ERR, however, in order to maintain consistency all of the regulators are returned to the values stored in NVM and the recovery counter is incremented. If the recovery counter exceeds the recovery count threshold the PMIC stays in the safe recovery state.

Note

After the ACTIVE_TO_WARM sequence the MCU is responsible for managing the EN_DRV and recovery counter. At the end of the sequence the 'FORCE_EN_DRV_LOW' bit is cleared so that the MCU can set the ENABLE_DRV bit.

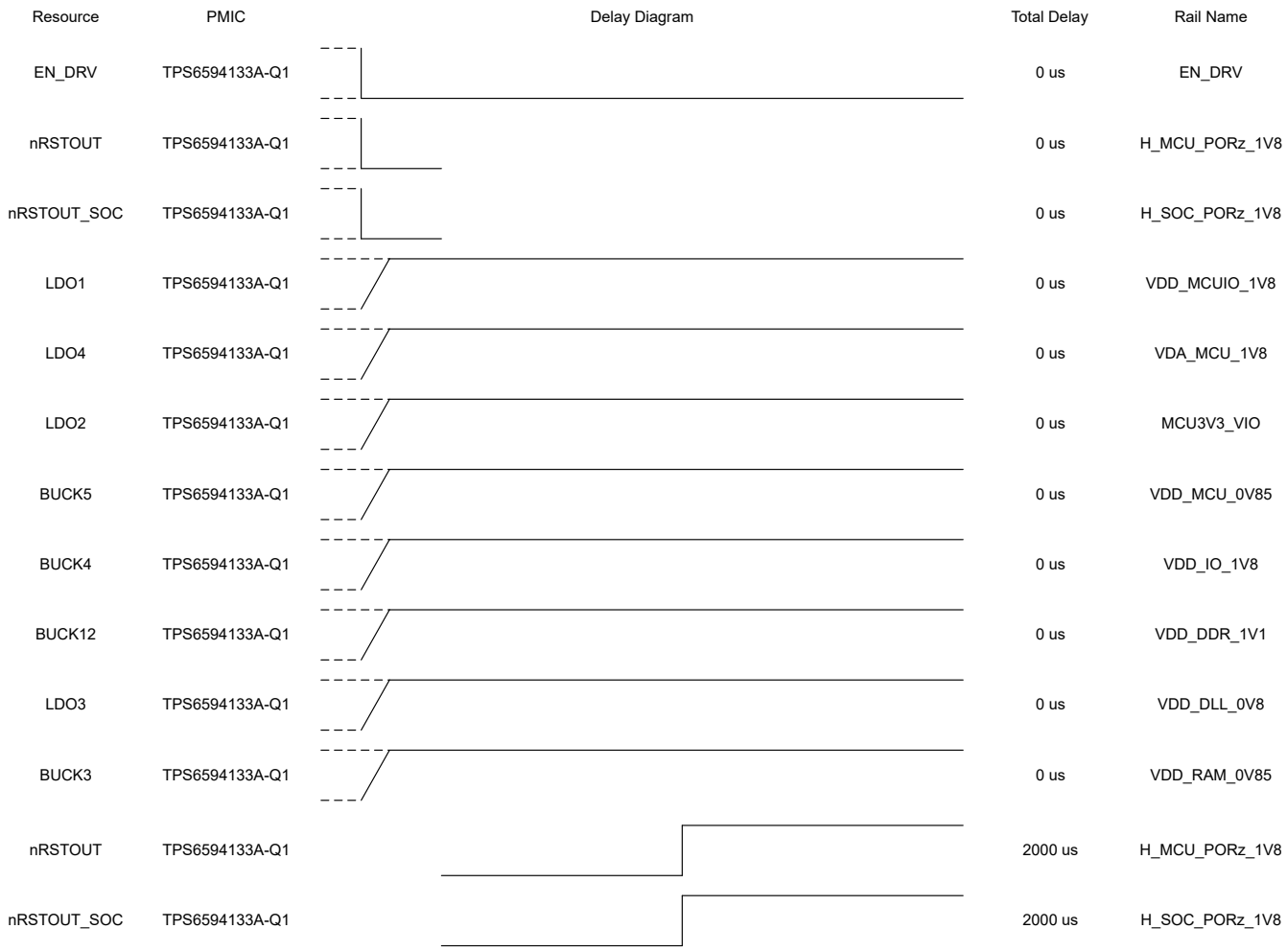


Figure 5-4. ACTIVE_TO_WARM Power Sequence

Note

The regulator transitions do not represent enabling of the regulators but the time at which the voltages are restored to their default values. Since this sequence originates from the ACTIVE state all of the regulators are on.

5.3.4 ESM_SOC_ERROR

In the event of an ESM_SOC error, the nRSTOUT_SOC signal is driven low and then driven high again after 200 µs. There is no change to the power rails. The sequence is shown in Figure 5-5.

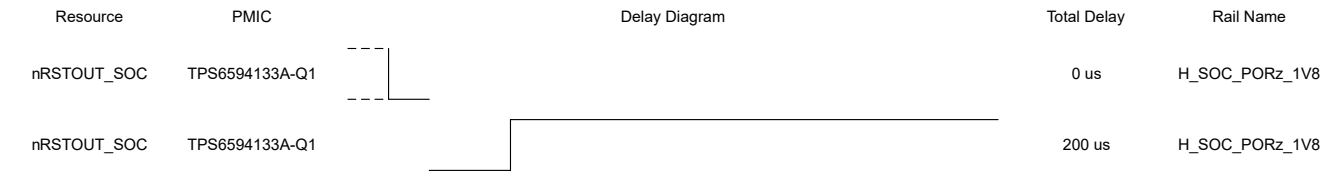


Figure 5-5. ESM_SOC_ERROR Sequence

5.3.5 PWR_SOC_ERROR

In the event of an error on any of the power rails which are part of the MAIN/SOC power rail group, the PWR_SOC_ERROR sequence is performed. The nRSTOUT_SOC pin is pulled low and the SOC power rails execute a normal processor power down sequence except the MCU power group remains energized as shown in Figure 5-6. The state of the I2C_7 trigger in the PMIC determines whether the DDR supplies and control signals remain energized (I2C_7=1) or disabled (I2C_7=0), as shown in Figure 5-7.

In the start of the sequence the following instructions are executed:

```
// TPS6594133A
// Set AMUXOUT_EN and CLKMON_EN, clear LPM_EN and nRSTOUT_SOC
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x18 MASK=0xE1
// Clear SPMI_LPM_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x00 MASK=0xEF
```

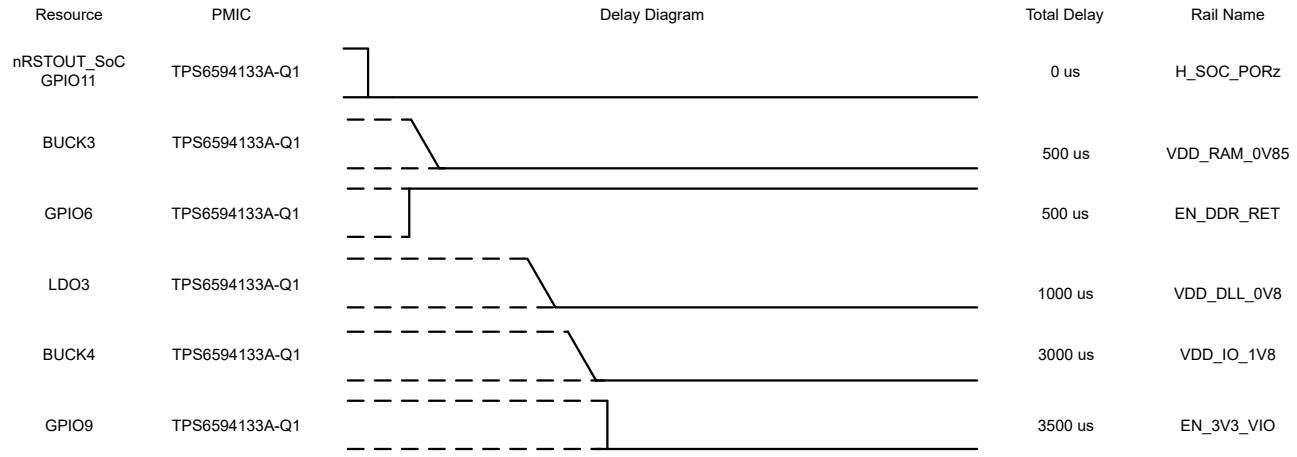


Figure 5-6. PWR_SOC_ERROR With I2C_7 High

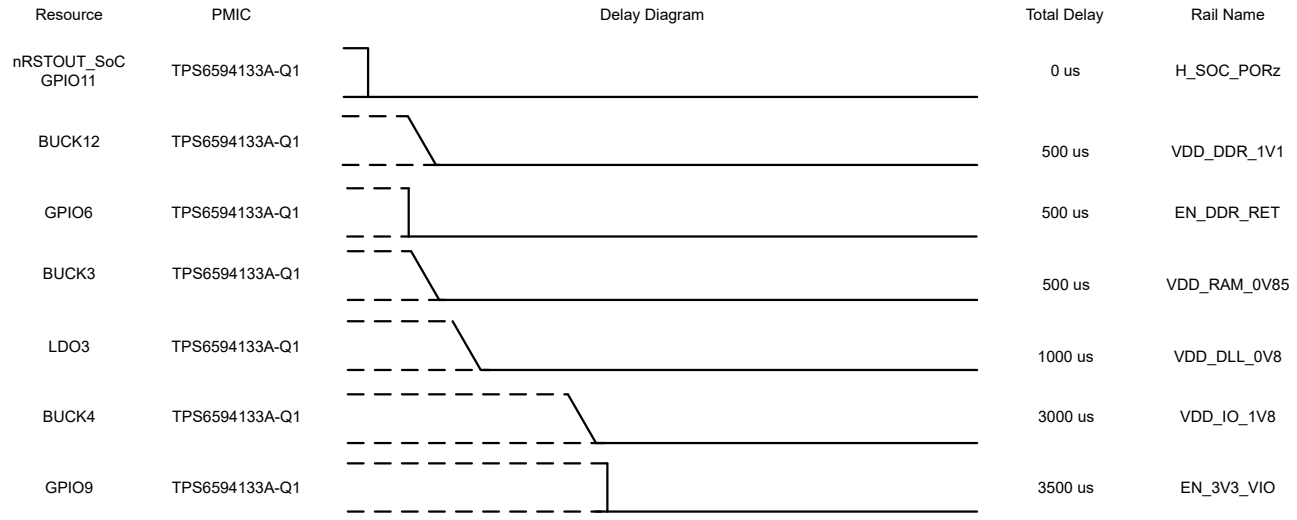


Figure 5-7. PWR_SOC_ERROR With I2C_7 Low

5.3.6 MCU_TO_WARM

The MCU_TO_WARM sequence is triggered by a WATCHDOG or ESM_MCU error. The MCU_TO_WARM, similar to the ACTIVE_TO_WARM sequence does not result in a state change. The event and sequence originate from the MCU_ONLY state and stays in the MCU_ONLY state. In the sequence, the recover counter (found in register, RECOV_CNT_REG_1) is incremented and the nRSTOUT (MCU_PORz) signal is driven low. The MCU relevant BUCK and LDOs are reset to their default voltages at the time indicated in Figure 5-8, and finally the MCU_PORz signal is set high after 2ms.

Note

GPIOs do not reset during the MCU warm reset event.

Also, at the beginning of the sequence the following instructions are executed to increment the recovery counter and configure the PMICs:

```
// TPS6594133A
// Set FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x08 MASK=0xF7
// Clear nRSTOUT
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x00 MASK=0xFE
// Increment Recovery Counter
REG_WRITE_MASK_IMM ADDR=0xa5 DATA=0x01 MASK=0xFE
```

Note

The watchdog or MCU error is an indication of a significant error which has taken place outside of the PMIC. The PMIC does not actually transition through the safe recovery as with an MCU_POWER_ERR, however, in order to maintain consistency all of the regulators are returned to the values stored in NVM and the recovery counter is incremented. If the recovery counter exceeds the recovery count threshold the PMIC stays in the safe recovery state.

Note

After the MCU_TO_WARM sequence the MCU is responsible for managing the EN_DRV and recovery counter. At the end of the sequence the 'FORCE_EN_DRV_LOW' bit is cleared so that the MCU can set the ENABLE_DRV bit.

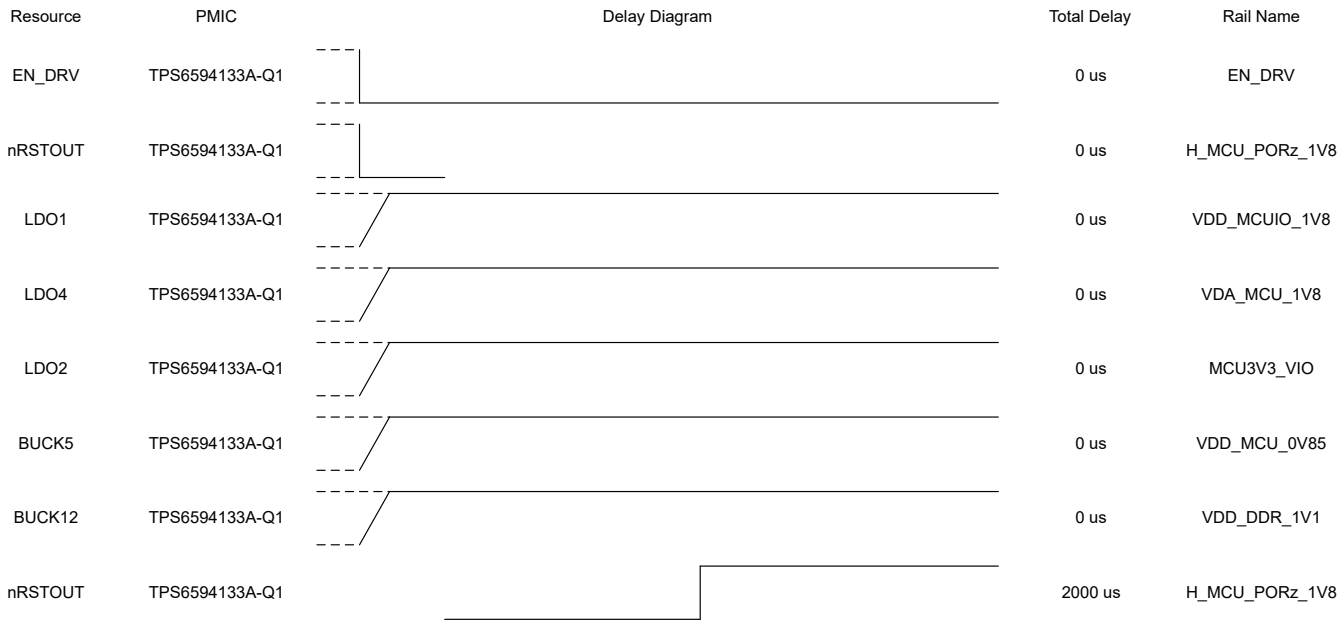


Figure 5-8. MCU_TO_WARM Sequence

Note

The regulator transitions do not represent enabling of the regulators but the time at which the voltages are restored to their default values. Since this sequence originates from the MCU_ONLY state these regulators are on.

5.3.7 TO_MCU

The TO_MCU sequence first turns off rails and GPIOs which are assigned to the SOC power group. The sequence enables the MCU rails, in the event that they are not already active (when transitioning from STANDBY to MCU_ONLY for example). There are two cases for this sequence, based off the value stored in the I2C_7 bit found in register FSM_I2C_TRIGGERS. If the bit is low, then VDD_DDR_1V1 and EN_DDR_RET are disabled; Figure 5-10. If the I2C_7 bit is high, then VDD_DDR_1V1 and EN_DDR_RET are enabled; Figure 5-9.

The first instructions of the TO_MCU sequence perform writes to the MISC_CTRL and ENABLE_DRV_STAT registers.

```
// TPS6594133A
// Set AMUXOUT_EN, CLKMON_EN
// Clear LPM_EN, NRSTOUT_SOC
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x18 MASK=0xE1
// Clear SPMI_LP_EN
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x00 MASK=0xEF
```

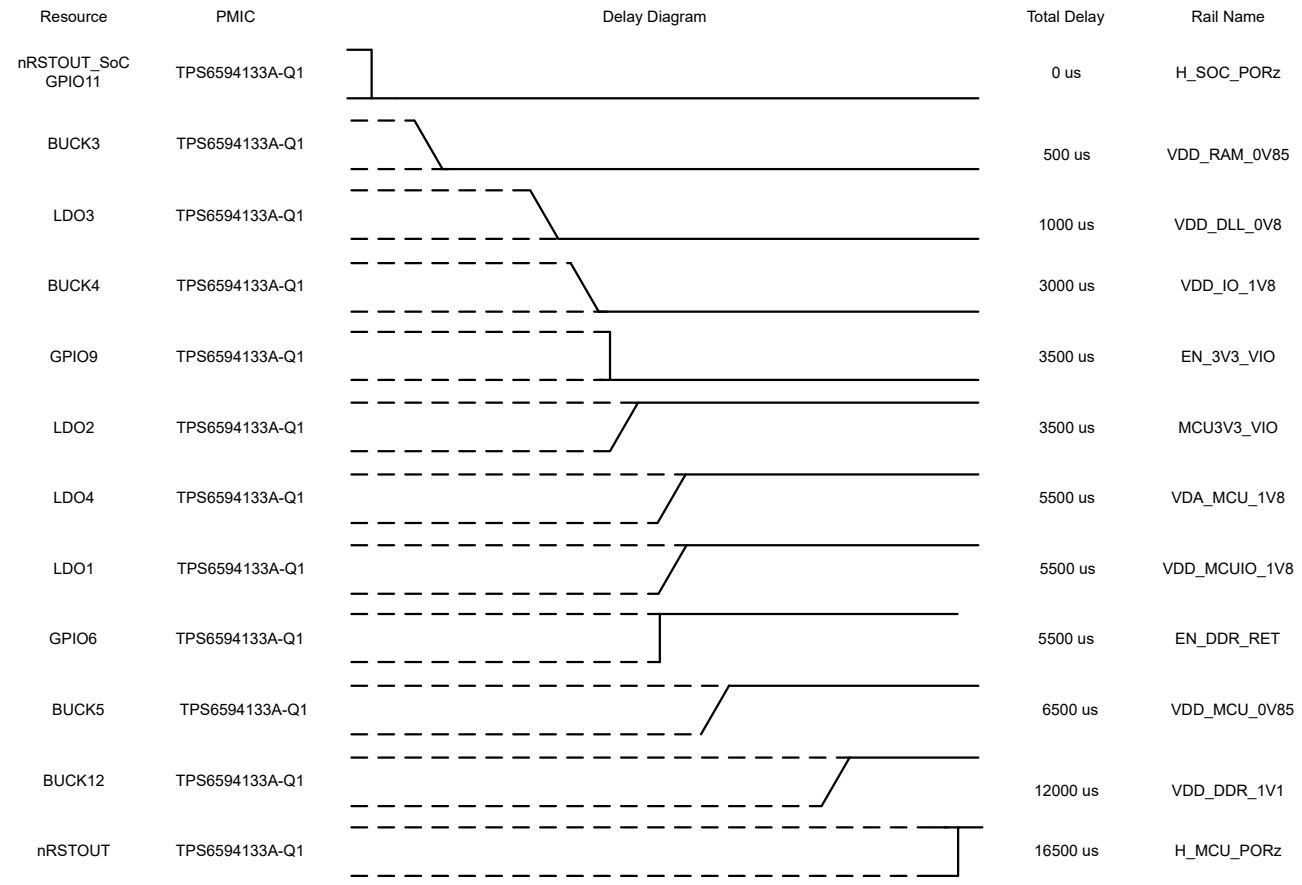


Figure 5-9. TO_MCU with I2C_7 High

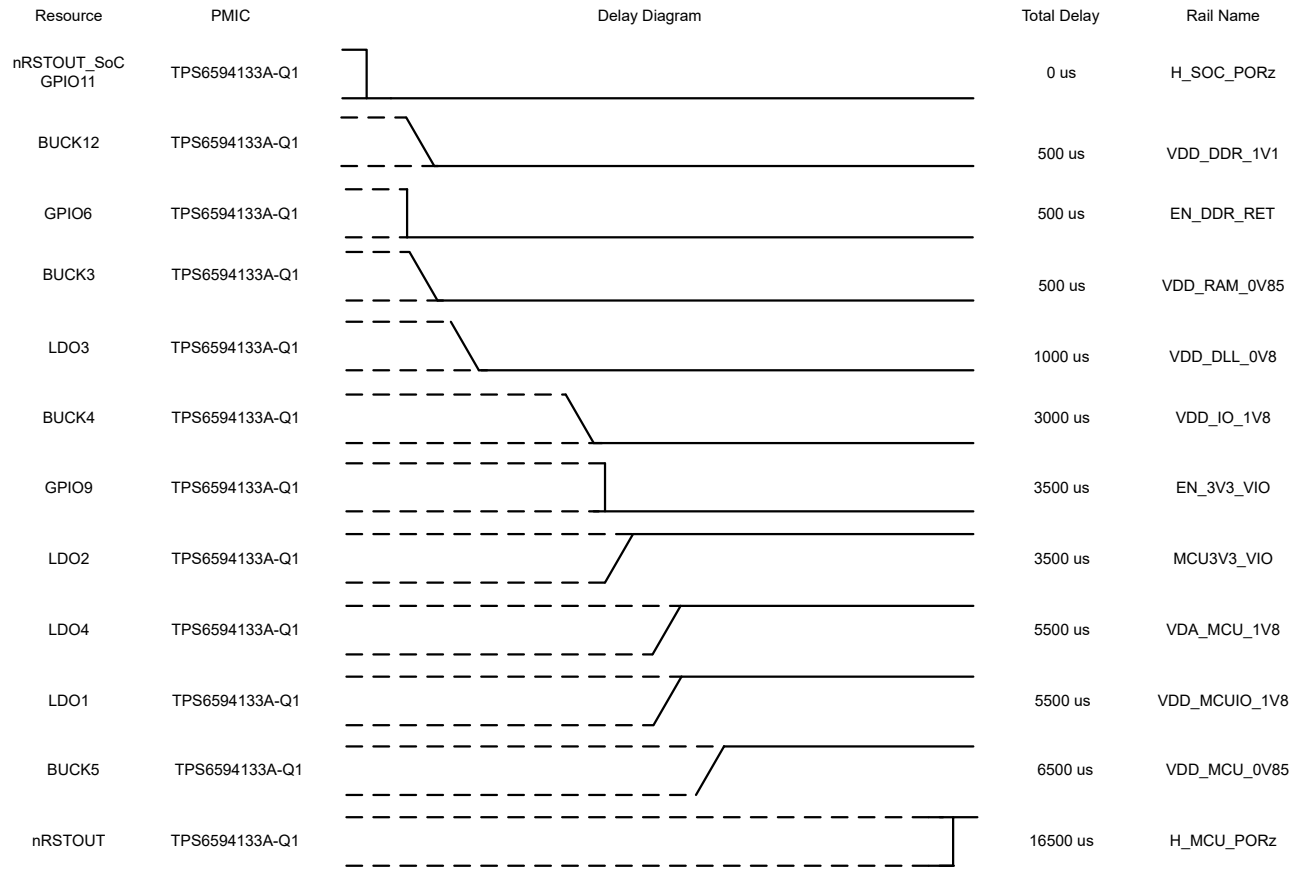


Figure 5-10. TO_MCU Sequence with I2C_7 Low

Amongst the last instructions of the TO_MCU sequence, the PMIC writes to the MISC_CTRL and ENABLE_DRV_STAT registers after the delay defined in the PFSM_DELAY_REG_1.

```
// TPS6594133A
SREG_READ_REG ADDR=0xCD REG=R1
DELAY_SREG R1
// Clear FORCE_EN_DRV_LOW
REG_WRITE_MASK_IMM ADDR=0x82 DATA=0x00 MASK=0xF7
// Set NRSTOUT (MCU_PORZ)
REG_WRITE_MASK_IMM ADDR=0x81 DATA=0x01 MASK=0xFE
```

Note

After the TO_MCU sequence the MCU is responsible for managing the EN_DRV.

5.3.8 TO_ACTIVE

When a trigger causes the TO_ACTIVE sequence to execute, all rails power up in the recommended power up sequence as shown in Figure 5-11.

At the beginning of the TO_ACTIVE sequence, the PMIC clears SPMI_LPM_EN and LPM_EN and sets AMUXOUT_EN and CLKMON_EN.

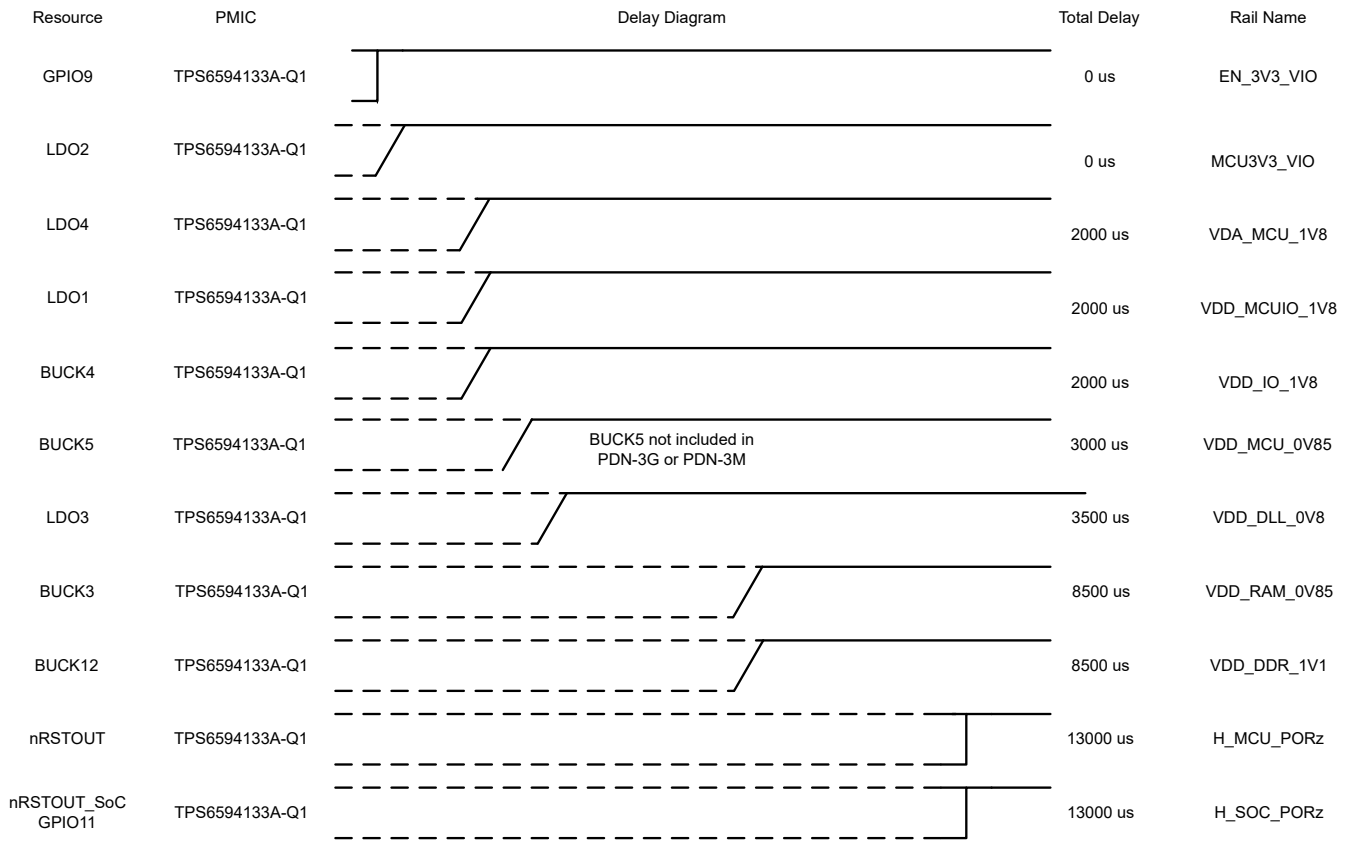


Figure 5-11. TO_ACTIVE Sequence

At the end of the TO_ACTIVE sequence the 'FORCE_EN_DRV_LOW' bit is cleared.

Note

After the TO_ACTIVE sequence the MCU is responsible for managing the EN_DRV.

5.3.9 TO_RETENTION

The C and D triggers, defined by the NSLEEPx bits or pins, trigger the TO_RETENTION sequence. This sequence disables all power rails and GPIOs that are not supplying the retention rails, as described in Figure 2-1. The sequence can be modified using the I2C_5 and I2C_7 bits found in register FSM_I2C_TRIGGERS. These bits need to be set by I^2C in the PMIC before a trigger for the retention state occurs. If the I2C_7 bit is set high, the PMIC enters the DDR retention state. If the I2C_5 bit is set high, the PMIC enters the GPIO retention state. The TO_RETENTION sequence with both GPIO and DDR retention is shown in Figure 5-13. If I2C_5 and I2C_7 are set low, the components associated with DDR and GPIO retention do not remain active, as shown in Figure 5-12.

Note

The I2C_5 and I2C_7 bits need to be set or cleared by I^2C in the PMIC before a trigger to the retention state occurs. The triggers are not self-clearing and must be maintained during operation.

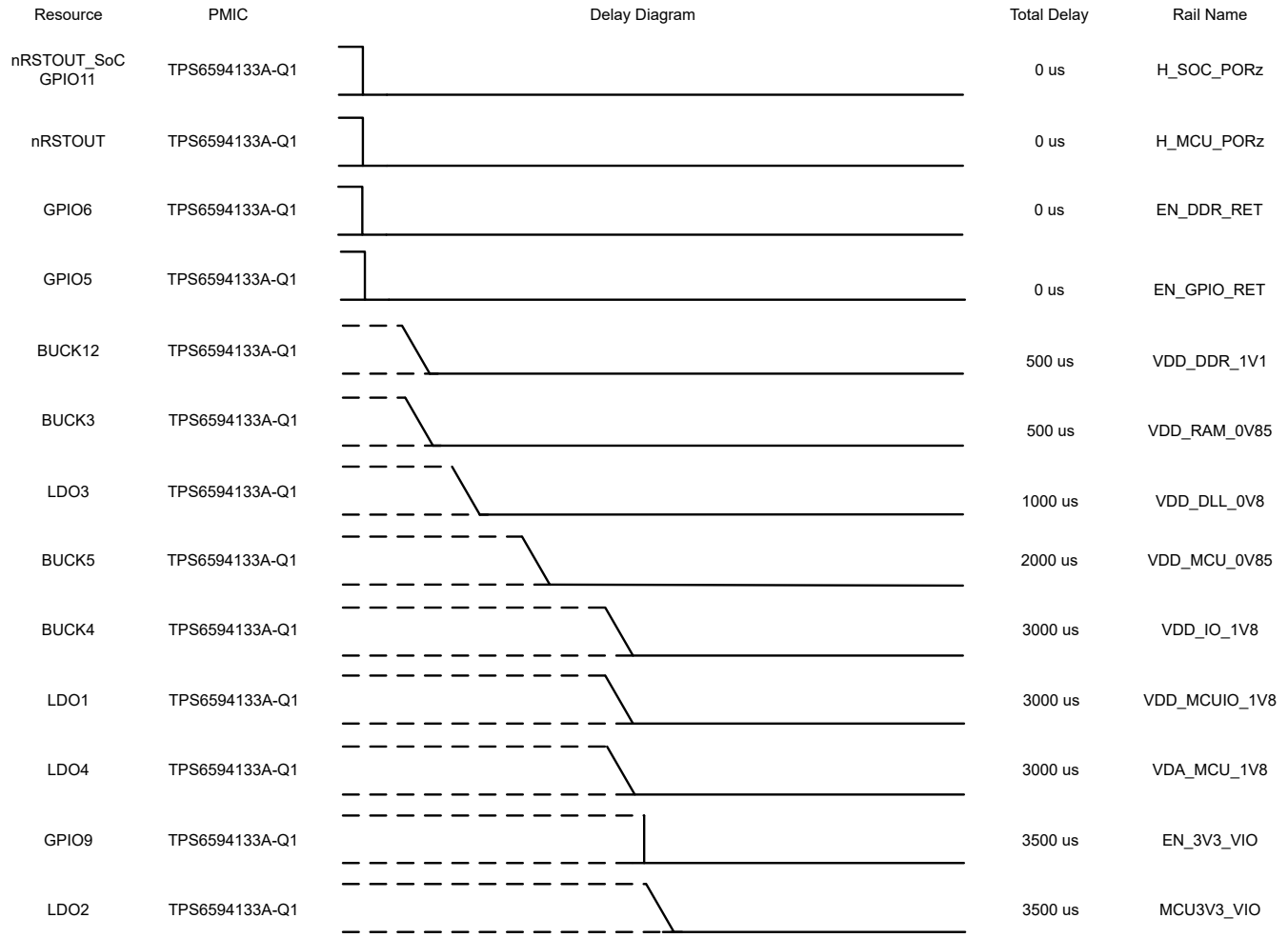


Figure 5-12. TO_RETENTION when I2C_5 and I2C_7 are Low

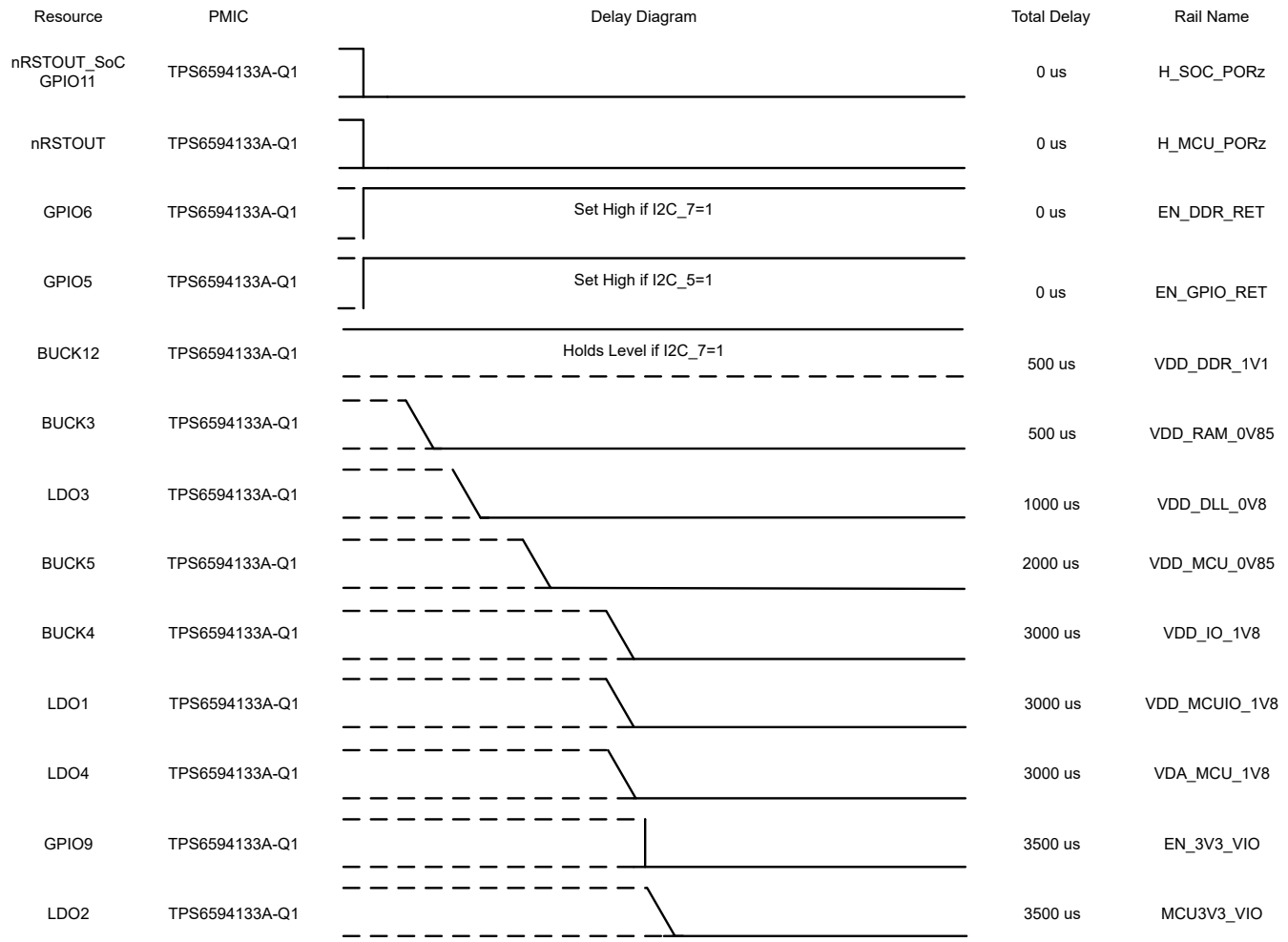


Figure 5-13. TO_RETENTION when I2C_5 and I2C_7 are High

At the end of the sequence, the PMIC set the LPM_EN and clear the AMUXOUT_EN. The TPS6594133A device also performs an additional 16 ms delay based upon the contents of the register PFSM_DELAY_REG_2.

6 Application Examples

This section provides examples of how to interact with the PMICs from the perspective of the MCU and over I2C. Table 6-1 shows how the I2C commands are presented in the following sections. These examples, when used in conjunction with the data sheet, can be generalized and applied to other use cases.

Table 6-1. I2C Instruction Format

	I2C Address	Register Address	Data	Mask
Write	0x48	0x00 - 0xFF	0x00 - 0xFF	0x00 - 0xFF
Read	0x48	0x00 - 0xFF	NA	NA

Note

When the MASK is non-zero, this assumes a read has taken place and then a logical operation applied to only change the desired bit fields before writing the data back.

6.1 Initialization

Upon a successful power up, the BIST_PASS_INT and ENABLE_INT interrupts are set. Any other interrupts indicate an issue but the automated recovery attempt was successful. The recommended procedure is to:

1. Interrogate the interrupts
2. Determine the course of action
3. Set the NSLEEP bits
4. Clear the interrupts

The following example assumes that there are no interrupts other than the BIST_PASS_INT and ENABLE_INT after power up and the enable pin goes high.

```
Read  0x48:0x5A              // Read INT_TOP to determine errors
Read  0x48:0x65              // Read the STARTUP_INT register
Read  0x48:0x66              // Read the MISC_INT register
Write 0x48:0x86:0x03:0xFC    // Set NSLEEP1 and NSLEEP2 in the PMIC
Write 0x48:0x66:0x01:0xFE    // Clear BIST_PASS_INT
Write 0x48:0x65:0x26:0xD9    // Clear all potential sources of the On Request
```

6.2 Moving Between States; ACTIVE, MCU ONLY and RETENTION

The default configuration of the NVM transitions the PMICs to the ACTIVE state when the ENABLE pin on the TPS6594133A goes high (rising edge triggered). The nINT pin goes high to indicate to the MCU that interrupts have occurred in the PMICs. After a normal power up sequence the interrupts are the ENABLE_INT and BIST_PASS_INT. The ENABLE_INT prohibits the PMICs from processing any lower priority triggers below the 'ON Request' in Table 5-1. The blocking of the lower priority triggers is why the PMICs are in the ACTIVE state even though the NSLEEP1 and NSLEEP2 bits are both cleared. Once the ENABLE_INT is cleared the state is defined by Table 6-2. The following sections describe the I^2C commands for transitioning between the different states.

Table 6-2. State Table

NSLEEP1	NSLEEP2	I2C_7	I2C_5	State
1	1	NA	NA	ACTIVE
0	1	1	NA	MCU Only with DDR Retention
0	1	0	NA	MCU Only without DDR Retention
Do not Care	0	1	NA	DDR Retention
	0	NA	1	GPIO Retention

6.2.1 ACTIVE

In this example the, PMIC is already in the ACTIVE state after a normal power up event. The PMIC is kept in the ACTIVE state by setting the NSLEEP1 and NSLEEP2 bits before clearing the ENABLE_INT.

```
Write 0x48:0x86:0x03:0xFC    // Set NSLEEP1 and NSLEEP2 in TPS65951213
Write 0x48:0x66:0x01:0xFE    // Clear BIST_PASS_INT
Write 0x48:0x65:0x26:0xD9    // Clear all potential sources of the On Request
```

6.2.2 MCU ONLY

Transitioning to the MCU ONLY state from the ACTIVE state, requires configuring the I2C_7 trigger before changing the NSLEEP bits.

```
Write 0x48:0x85:0x80:0x7F    // Set I2C_7 Triggers on TPS6594133A
Write 0x48:0x86:0x02:0xFC    // Set NSLEEP2 to trigger TO_MCU power sequence
```

Instead of writing to the NSLEEP bits to return to the ACTIVE state, it is also possible to use the WKUP1 pin on GPIO4 to return the PMIC to the ACTIVE state. Because of the similarity this is shown in the context of the RETENTION state.

6.2.3 RETENTION

As shown in Section 5.3.9, the MCU is powered off and therefore the transition out of the RETENTION to the MCU ONLY or the ACTIVE states must be configured before entering RETENTION. Similar to the MCU ONLY state the I2C_7 triggers must be set for the PMIC. In this example GPIO4 on the TPS6594133A is used to wake the device from RETENTION to ACTIVE.

Note

GPIO4 (WKUP1) must be HIGH before entering retention mode. PMIC is only compatible with falling edge trigger wake.

```
Write 0x48:0x34:0xC0:0x3F // Set GPIO4 to WKUP1 (goes to ACTIVE state)
Write 0x48:0x64:0x08:0xF7 // clear interrupt of gpio4, write to clear
Write 0x48:0x4F:0x00:0xF7 // unmask interrupt for GPIO4 falling edge
Write 0x48:0x86:0x00:0xFC // trigger the TO_RETENTION power sequence
After the GPIO4 has gone low and the PMIC has returned to the ACTIVE state
Write 0x48:0x86:0x03:0xFC // Set NSLEEPx bits for ACTIVE state
Write 0x48:0x64:0x08:0xF7 // clear interrupt of gpio4
```

In this example the TPS6594133A RTC Timer is used to wake the device from RETENTION to ACTIVE.

```
Write 0x48:0xC3:0x01:0xFE // Enable Crystal
Write 0x48:0xC5:0x05:0xF8 // minute timer, enable TIMER interrupts
Write 0x48:0xC2:0x01:0xFE // start timer, if the timer values are non-zero clear before starting
Write 0x48:0x86:0x00:0xFC // trigger the TO_RETENTION power sequence
After the RTC Timer interrupt has occurred and the PMIC has returned to the ACTIVE state
Write 0x48:0x86:0x03:0xFC // Set NSLEEPx bits for ACTIVE state
Write 0x48:0xC5:0x00:0xFB // disable timer interrupt, clear bit 2
Write 0x48:0xC4:0x00:0xDF // clear timer interrupt, clear bit 5.
```

6.3 Entering and Exiting Standby

STANDBY can be entered from the ACTIVE or the RETENTION states. In order to stay in the mission state of STANDBY and not enter the hardware state LP_STANDBY the LP_STANDBY_SEL bit must be cleared.

Similar to the RETENTION state, the STANDBY state turns off all regulators that power the processor. The ACTIVE state is the only destination state available that the STANDBY state returns to.

When the ENABLE pin goes low, the TO_STANDBY sequence is triggered. When the ENABLE pin goes high again, the PMICs return to the ACTIVE state, defined in the STARTUP_DEST bits. The TO_STANDBY sequence is also triggered by the I2C_0 trigger. When triggered from I2C_0 the PMIC can be triggered to return to the ACTIVE states by GPIO4, GPIO10, or and RTC timer or alarm. In this example, I2C_0 trigger is used to enter the STANDBY state and the GPIO4 is used to enter the ACTIVE state

```
Write 0x48:0xC3:0x00:0xF7  // LP_STANDBY_SEL=0
Write 0x48:0x7D:0xC0:0x3F  // Mask NSLEEP bits
Write 0x48:0x34:0xC0;0x3F  // Set GPIO4 to WKUP1 (goes to ACTIVE state)
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
Write 0x48:0x4F:0x00:0xF7  // unmask interrupt for GPIO4 falling edge
Write 0x48:0x85:0x01:0xFE  // set I2C_0 trigger, trigger TO_STANDBY sequence
After the GPIO4 has gone low and the PMICs have returned to the ACTIVE state
Write 0x48:0x7D:0x00:0x3F  // unmask NSLEEP bits
Write 0x48:0x86:0x03:0xFC  // Set NSLEEPx bits for ACTIVE state
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
```

6.4 Entering and Existing LP_STANDBY

Entering the LP_STANDBY hardware state is the same as entering STANDBY. Exiting LP_STANDBY is different and requires different initializations before entering LP_STANDBY. Also, when the PMICs return from LP_STANDBY the PFSM triggers are gated by the ENABLE_INT while in STANDBY the triggers were gated by the GPIO interrupt.

```
Write 0x48:0xC3:0x08:0xF7  // LP_STANDBY_SEL=1
Write 0x48:0x7D:0xC0:0x3F  // Mask NSLEEP bits
Write 0x48:0x34:0xC0;0x3F  // Set GPIO4 to WKUP1 (goes to ACTIVE state)
Write 0x48:0xC3:0x60;0x9F  // Set the STARTUP_DEST=ACTIVE
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
Write 0x48:0x4F:0x00:0xF7  // unmask interrupt for GPIO4 falling edge
Write 0x48:0x85:0x01:0xFE  // set I2C_0 trigger, trigger TO_STANDBY sequence
After the GPIO4 has gone low and the PMICs have returned to the ACTIVE state
Write 0x48:0x7D:0x00:0x3F  // unmask NSLEEP bits
Write 0x48:0x86:0x03:0xFC  // Set NSLEEPx bits for ACTIVE state
Write 0x48:0x64:0x08:0xF7  // clear interrupt of GPIO4
Write 0x48:0x65:0x02:0xFD  // clear ENABLE_INT
```

7 Impact of NVM Changes

Table 7-1. NVM Changes From Revision 3 to Revision 5

Change	Impact of change
Update NVM revision to 5, see Table 4-2.	None.
Watchdog enabled by default with 13 minute long window.	MCU software must boot and configure watchdog within 13 minutes of nRSTOUT going high.
Change default GPIO9 function from GPIO to WD_DISABLE.	GPIO9 starts as an input to set WD_PWRHOLD bit, then changes to an output. **In Development:** Customer has *option* to use external PU resistor to set WD_PWRHOLD =1 **In End Equipment:** No impact to function
TO_ACTIVE sequence has 500us delay between LDO3 and BUCK5, seeFigure 5-11	In systems with split power groups, PMIC BUCK5 powers up fully before PMIC LDO3. Overall sequence time remains the same.
LDO2 OV/UV Threshold changed from 5% to 10%, see Table 4-4	When used as 3.3V load switch, PG Window changes to that of VCCA. Customer can tighten after boot.

8 References

For additional information regarding the PMIC or processor devices, use the following:

- Texas Instruments, *J721S2 Jacinto™ Automotive Processors* Data Sheet
- Texas Instruments, *J721S2 Technical Reference Manual*
- Texas Instruments, *TPS6594-Q1 Power Management IC (PMIC) with 5 Bucks and 4 LDOs for Safety-Relevant Automotive Applications* Data Sheet
- Texas Instruments, TPS6594-Q1Safety Manual (request through mySecure)
- Texas Instruments, *TPS6594-Q1 Schematic PCB Checklist* Application Note

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2023) to Revision A (May 2025)	Page
• Updated abstract	1
• Added information about PDN-3A.I for industrial applications	2
• Updated TI_NVM_REV to 0x5	14
• Changed LDO2_PG_WINDOW from ± 5% to ± 10%	16
• Updated GPIO9 default settings to reflect NVM revision changes	17
• Added note about PFSM usage of SCRATCH_PAD_1 and SCRATCH_PAD_4	23
• Updated Watchdog Settings for latest NVM revision	25
• Updated list of configured powered states to include the Wait4Enable state	25
• Updated PFSM Mission States and Transistions diagram to include the Wait4Enable state	25
• Added 500us delay from BUCK5 to LDO3 in TO_ACTIVE sequence diagram	36
• Added note about WKUP1 signal for Retention mode exit	41
• Added table describing impact of NVM revision changes	42

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265