User's Guide

LM21305 Step-Down Converter Evaluation Module User's Guide

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Trademarks

1 LM21305 Overview

The LM21305 is a full-featured adjustable frequency synchronous buck point-of-load regulator capable of delivering up to 5 A of continuous output current. The device is optimized to work over an input voltage range of 3 V to 18 V and an output voltage range of 0.598 V to 5 V, making it suitable for wide variety of applications. The LM21305 provides excellent output voltage accuracy and superior line and load transient response for digital loads. The device offers flexible system configuration through programmable switching frequency through an external resistor with ability to synchronize the switching frequency to an external clock. The frequency can be set from 300 kHz to 1.5 MHz. The device also provides the following:

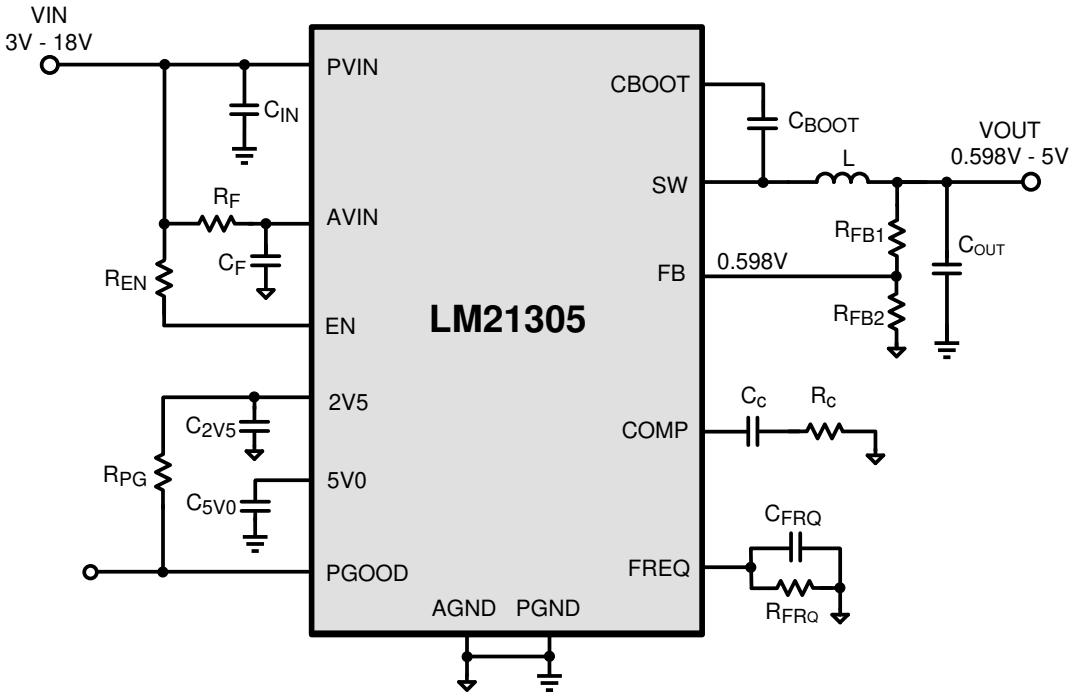
- Internal soft start to limit in-rush current
- Pre-biased and monotonic start up capability
- Cycle-by-cycle current limiting
- Thermal shutdown

The device features internal overvoltage protection (OVP) and overcurrent protection (OCP) circuits for increased system reliability. A precision enable pin and integrated undervoltage lockout (UVLO) allows the turn-on of the device to be tightly controlled and sequenced. Fault detection and supply sequencing are possible with the integrated power good circuit.

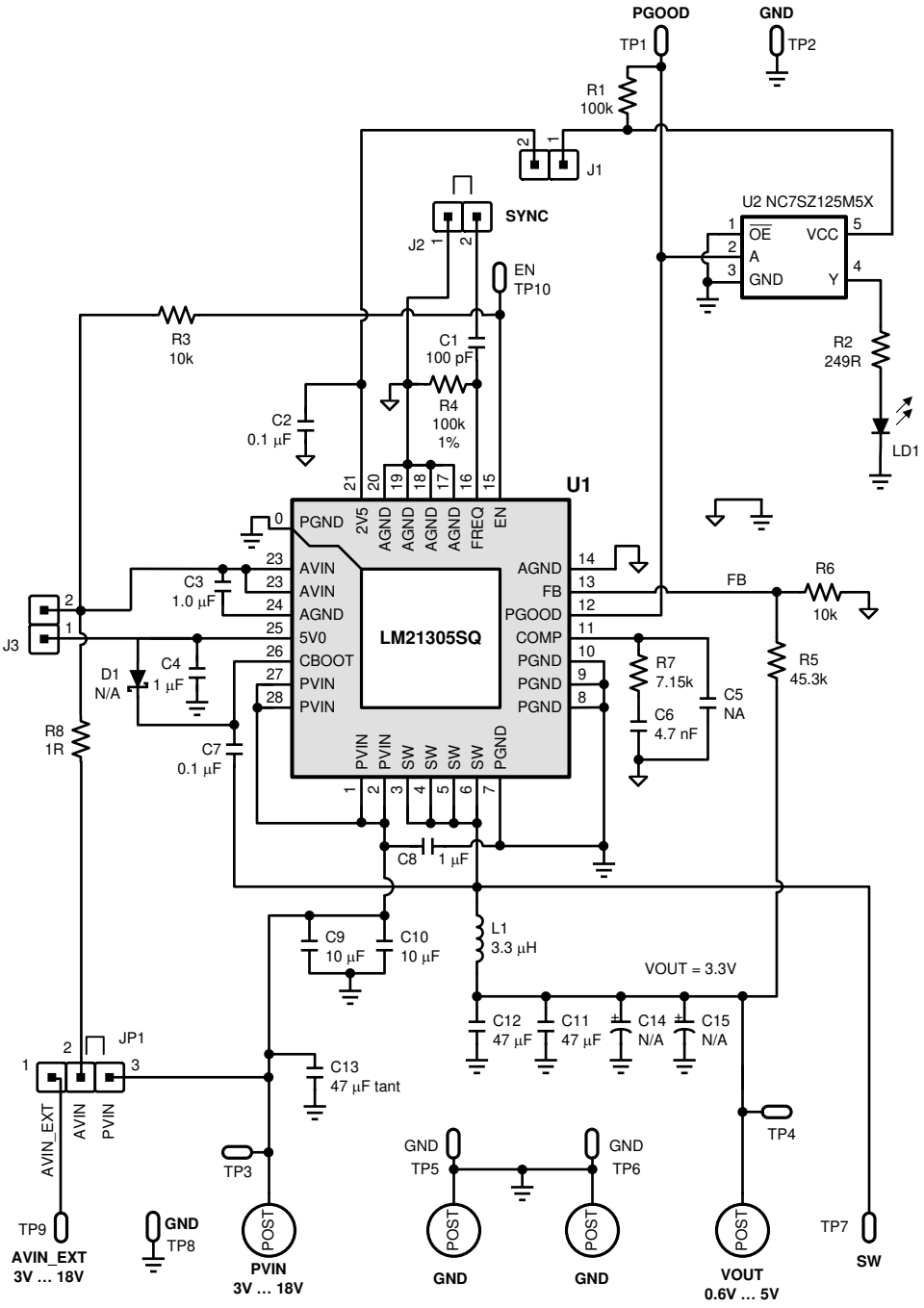
The LM21305 is offered in a WQFN-28 package with an exposed pad for enhanced thermal performance. The LM21305 evaluation board comes ready to operate at the following conditions:

Parameter	Default	Range and Options
PVIN	12 V	External supply 5 V to 18 V
AVIN	=PVIN	Connect to PVIN or to separate supply (3 V to 18 V) selected by JP1
VOUT	3.3 V	0.598 V to 5 V by changing R5, R6, or both
Switching frequency	500 kHz	300 kHz to 1.5 MHz by changing R4
I_{OUT}		0 A to 5 A
Size	2 inches × 1.5 inches	
Number of PCB layers	4	

2 Typical Application Circuit



3 Evaluation Board Schematic



4 Evaluation Board Bill of Materials (BOM)

Table 4-1. Board Bill of Materials (BOM)

Component	Description	Manufacturer	Manufacturer Part Number	Package
C1	CERAMIC 100 pF 25 V NPO	AVX	06033A101KAT2A	0603
C2,C7	CERAMIC 0.1 µF 16 V X7R	TDK	C1608X7R1C104M	0603
C3,C4	CERAMIC 1.0 µF 25 V X7R	TDK	C1608X7R1E105M	0603
C5	N/A	N/A	N/A	N/A
C6	CERAMIC 4.7 nF 50 V X7R	TDK	C1608X7R1H472J	0603
C8	CERAMIC 1.0 µF 25 V X7R	TDK	C3216X7R1E105K	1206
C9, C10	CERAMIC 10 µF 25 V X5R	TDK	C3225X5R1E106K	1210
C11, C12	CERAMIC 47 µF 10 V X5R	TDK	C3225X5R1A476M	1210
C13	TANT 47 µF 25 V	Kemet	T495X476K025ATE150	CASE D
C14, C15	N/A	N/A	N/A	N/A
D1	N/A	N/A	N/A	N/A
L1	3.3 µH 9.0 A SMD	Wurth Electronics	744314330	SMD
LD1	LED GREEN	CML	CMDA5CG7D1Z	0805
R3, R6	10 kΩ 0603 1%	Yageo	RC0603FR-710KL	0603
R2	249Ω 0603 1%	Yageo	RC0603FR-07249RL	0603
R1, R4	100 kΩ 0603 1%	Yageo	RC0603FR-07100KL	0603
R5	45.3 kΩ 0603 1%	Yageo	RC0603FR-0745K3L	0603
R7	7.15 kΩ 0603 1%	Yageo	RC0603FR-077K15RL	0603
R8	1 Ω 0603 1%	Yageo	RC0603FR-071RL	0603
U1	LM21305 Buck Regulator	Texas Instruments	LM21305	WQFN-28
U2	IC BUFF NON-INV	Fairchild	NC7SZ125M5X	SOT23-5

5 Connection Descriptions

Terminal Silkscreen	Description
PVIN	Connect the power supply between this terminal and the GND terminal beside it. The device is rated between 3 V to 18 V. The absolute maximum voltage rating is 20 V.
GND	The GND terminals are meant to provide a close return path to the power and signal terminal beside them. They are all connected together on the board.
SW	The SW terminal is connected to the switch node of the power stage. It can be used to monitor the switch node waveform using an oscilloscope.
VOUT	The VOUT terminal is connected to the output capacitor on the board and should be connected to the load.
AVIN_EXT	The LM21305 evaluation board facilitates using a separate supply voltage to AVIN through JP1 selection and connection to the AVIN_EXT terminal. An AVIN voltage of 5 V will result in optimal efficiency in most cases.
EN	This terminal connects to the EN pin of the device. The EN is pulled up to AVIN through a 10-kΩ resistor on the board. It also can be externally controlled through this terminal. If driven externally, a voltage typically greater than 1.2 V will enable the device.
PGOOD	This terminal connects to the power-good output of the device. There is a 100-kΩ pullup resistor from this pin to the 2V5 bias rail.

6 Jumper Settings

Terminal Silkscreen	Description
JP1	Sets the AVIN of the LM21305. Pins 2 and 3 connected gives AVIN = PVIN. Pins 1 and 2 connected gives AVIN = AVIN_EXT. Default: Pins 2 and 3 connected.
J1	Enables the on-board LED, LD1. When J1 is ON, LD1 will be ON if PGOOD is high. When J1 is OFF, power used to drive LD1 is saved. Default: ON
J2	Synchronizing clock input. When J2 is ON, C1 is connected to ground and switching frequency is set by the on-board resistor R4. When J2 is OFF, the switch node waveform will be synchronized to the clock source connected to J2. Default: ON
J3	Only should be connected when AVIN = 5 V. When AVIN is below 5 V, and especially below 3.3 V, connecting J3 can result in better efficiency. Default: OFF Caution: if AVIN > 5.5 V, connecting J3 can damage the device.

7 Other Design Examples

The LM21305 is designed to fit a wide variety of applications. A design calculator tool for the LM21305 is available to accelerate the design process. Also, the LM21305 is enabled through Texas Instruments WEBENCH® power designer. A few design examples are given here for convenience and only the components that need to be modified are listed below. Design examples are for the following:

- PVIN = 12 V
- f_s = 500 kHz
- $I_{OUT-MAX}$ = 5 A
- V_{OUT} = 1.2V, 1.8 V, 2.5 V, 3.3 V, and 5 V

V_{OUT}	1.2 V	1.8 V	2.5 V	3.3 V	5 V
C6	3300 pF, 25 V	3300 pF, 25 V	4700 pF, 25 V	4700 pF, 25 V	4700 pF, 25 V
L1	1.5 µH, 10 A	2.2 µH, 10 A	2.2 µH, 10 A	3.3 µH, 10 A	3.3 µH, 10 A
R5	10 kΩ, 1%	20 kΩ, 1%	31.6 kΩ, 1%	45.3 kΩ, 1%	73.2 kΩ, 1%
R7	3.32 kΩ, 1%	4.22 kΩ, 1%	5.10 kΩ, 1%	7.15 kΩ, 1%	8.2 kΩ, 1%

8 Typical Performance Characteristics

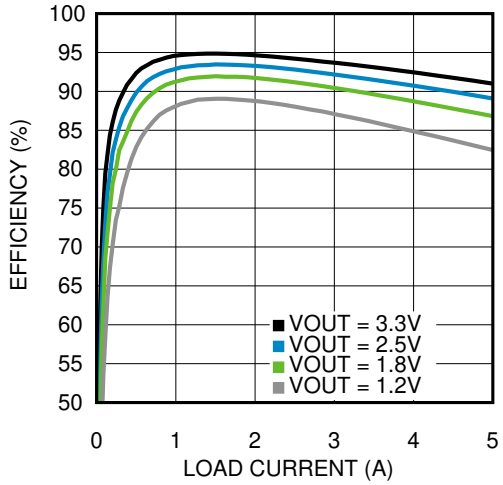


Figure 8-1. Efficiency with PVIN = AVIN = 5 V, f_S = 500 kHz

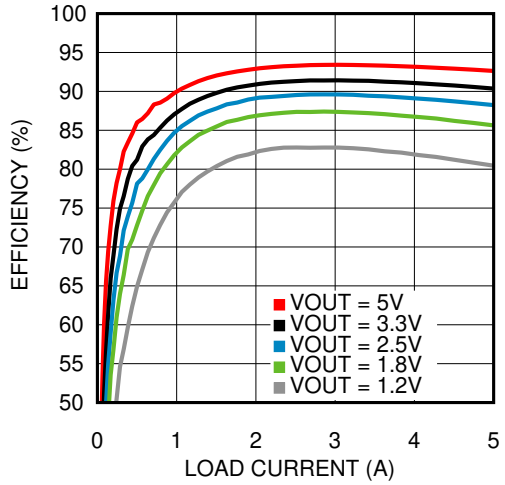


Figure 8-2. Efficiency with PVIN = AVIN = 12V, f_S = 500 kHz

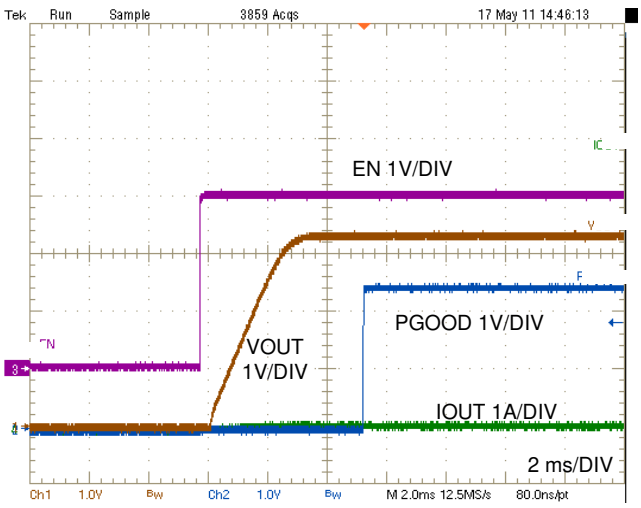


Figure 8-3. Start-Up, No Load

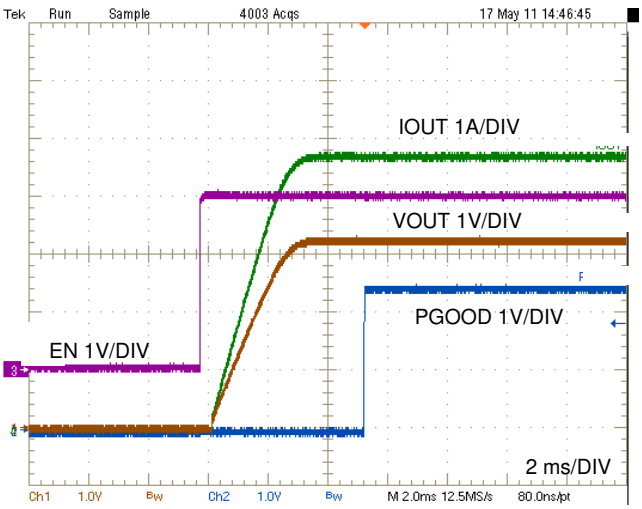


Figure 8-4. Start-Up, 5-A Resistive Load

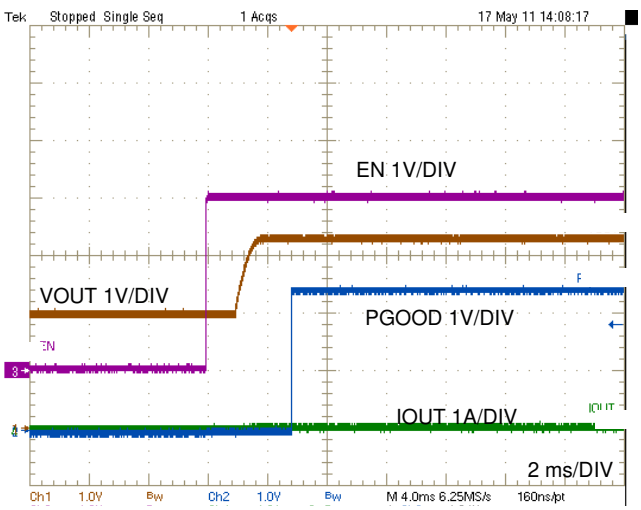


Figure 8-5. Start-Up, Pre-Biased Load

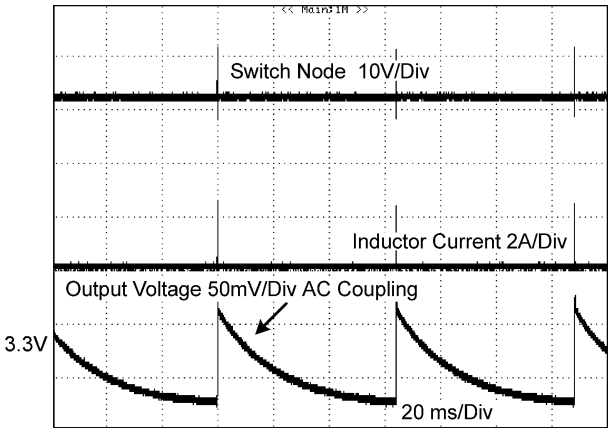


Figure 8-6. Switching Waveform at No Load (DCM Mode)

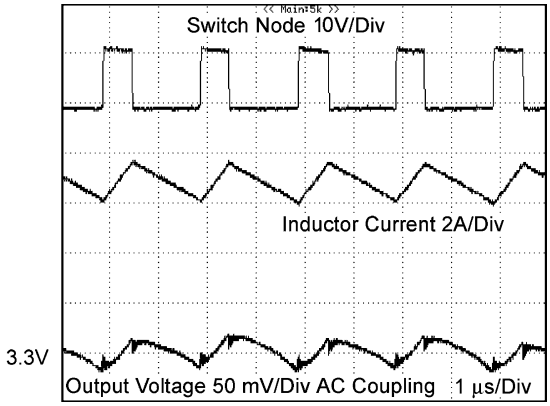


Figure 8-7. Switching Waveform With 5-A Load

9 Component Selection

This section provides a simplified design procedure necessary to select the external components to build a fully functional efficient step-down power supply. As with any DC-DC converter, numerous tradeoffs are possible to optimize the design for efficiency, size, and performance. Unless otherwise indicated, all formulas assume units of the following:

- Amps (A) for current
- Farads (F) for capacitance
- Henries (H) for inductance
- Volts (V) for voltages
- Hertz (Hz) for frequencies

For more details, please refer to the LM21305 data sheet.

9.1 Input Capacitors

PVIN is the supply voltage for the switcher power stage. It is the supply that delivers the output power. The input capacitors supply the large AC switching current drawn by the switching action of the internal MOSFETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle this current. To prevent large voltage transients, a low-ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS\_CIN} = I_{OUT} \sqrt{\frac{V_{OUT} (V_{PVIN} - V_{OUT})}{V_{PVIN}}} \text{ (A)} \quad (1)$$

The power dissipated in the input capacitor is given by:

$P_{D\_CIN} = I_{RMS}{}^2 R_{ESR\_CIN}$

where

- R_{ESR_CIN} is the ESR of the input capacitor.

This equation has a maximum at PVIN = 2 V_{OUT}, where $I_{RMS} \cong I_{OUT} / 2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Several capacitors can also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during load current changes. For optimal high frequency decoupling, a 1-µF ceramic bypass capacitor is also recommended adjacent the IC between the PVIN and PGND pins. Please refer to the PCB layout recommendation section in the LM21305 data sheet for more details. Note that the ESR of an electrolytic capacitor is used in this eval board to damp any oscillations that may occur when the supply lines have parasitic series inductance.

9.2 AVIN Filter

This can be seen on the schematic as components R_F and C_F. There is a practical limit to the size of the resistor R_F as the AVIN pin will draw a short 60-mA burst of current during start-up, and if R_F is too large the resulting voltage drop can trigger the UVLO comparator. For the evaluation board, a 1-Ω resistor is used for R_F ensuring that the UVLO will not be triggered after the part is enabled. A recommended 1-µF C_F capacitor coupled with the 1-Ω resistor provides approximately 10 dB of attenuation at 500-kHz switching frequency.

9.3 Switching Frequency Selection

The LM21305 supports a wide range of switching frequencies: 300 kHz to 1.5 MHz. The choice of switching frequency is usually a compromise between efficiency and size of the circuit. Lower switching frequency usually implies lower switching losses (including gate charge losses, transition losses, etc.) and would typically result in a better efficiency. But higher switching frequency allows the use of smaller LC filters to achieve a more compact design. Lower inductance also helps transient response (faster large-signal slew rate of inductor current) and reduces the conduction loss associated with the inductor DCR. The optimal switching frequency for efficiency needs to be determined on a case by case basis. It is related to the input voltage, the output voltage, the most frequent load level, external component choices, and circuit size requirement. The choice of switching frequency is also limited if an operating condition is possible to trigger $T_{ON\text{-}MIN}$ and $T_{OFF\text{-}MIN}$. The maximum frequency that can be used for a given input and output voltage can be found by:

$$f_{s\text{-}max} = \frac{V_{OUT}}{V_{PVIN\text{-}max}} \times \frac{1}{T_{ON\text{-}MIN}} \tag{2}$$

The following equation should be used to calculate resistor R4 value in order to obtain a desired frequency of operation:

f_s [kHz] = 31000 × $R^{-0.9}$[kΩ]

9.4 Inductor

A general recommendation for the inductor in the LM21305 application is to keep the peak-to-peak ripple current between 20% and 40% of the maximum DC load current (5 A), 30% is desired. The inductor also should have a high enough current rating and a DCR as small as possible.

The peak-to-peak current ripple can be calculated by:

$$\Delta i_{Lp\text{-}p} = \frac{(1 - D) \times V_{OUT}}{f_S \times L} \tag{3}$$

The current ripple is larger with smaller inductance and/or lower switching frequency. In general, with a fixed output voltage, the higher the PVIN, the higher the inductor current ripple. If PVIN is kept constant, inductor current ripple is highest at 50% duty cycle. It is recommended to choose L such that:

$$\frac{(1 - D) \times V_{OUT}}{f_S \times 0.4 \times I_{L(MAX)}} \leq L \leq \frac{(1 - D) \times V_{OUT}}{f_S \times 0.2 \times I_{L(MAX)}} \tag{4}$$

The inductor should be rated to handle the maximum load current plus the ripple current.

$I_{L(MAX)} = I_{LOAD(MAX)} + \Delta i_{L(MAX)} / 2$

An inductor with saturation current higher than the overcurrent protection limit is a safe choice. It is desired to have small inductance in switching power supplies, because it usually means faster transient response, smaller DCR, and smaller size for more compact design. But too low of an inductance will generate too large of an inductor current ripple and it can falsely trigger overcurrent protection at maximum load. It also generates more conduction loss, since the RMS current is slightly higher relative to that with lower ripple current with the same DC load current. Larger inductor current ripple also implies higher output voltage ripple with the same output capacitors. With peak current-mode control, it is recommended not to have too small of an inductor current ripple so that the peak current comparator has enough signal-to-noise ratio.

9.5 Output Capacitor

The LM21305 is designed to be used with a wide variety of LC output filters. It is generally desired to use as little output capacitance as possible to keep cost and size down. The output capacitor or capacitors, C_{OUT}, should be chosen with care since it directly affects the steady state output voltage ripple, loop stability and the voltage overshoot or undershoot during a load transient. The output voltage ripple is composed of two parts. One is related to the inductor current ripple going through the equivalent series resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\text{-}ESR} = \Delta i_{LP\text{-}P} \times ESR$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\text{-}C} = \frac{\Delta i_{Lp\text{-}p}}{8 f_S C_{OUT}} \tag{5}$$

Since the two components in the ripple are not in phase, the actual peak-to-peak ripple is smaller than the sum of the two peaks:

$$\Delta V_{OUT} < \Delta i_{Lp\text{-}p} \times \left(\frac{1}{8 f_S C_{OUT}} + ESR \right) \tag{6}$$

Output capacitance is usually limited by system transient performance specifications, particularly if the system requires tight voltage regulation in the presence of large current steps and fast slew rate. To maintain a small overshoot or undershoot during a load transient, small ESR and large capacitance are desired. But these also come with the penalty of higher cost and size. Clearly, the control loop should also be fast to reduce the voltage droop.

One or more ceramic capacitors are recommended because they have very low ESR and remain capacitive up to high frequencies. The dielectric should be X5R, X7R, or comparable material to maintain proper tolerances. Other types of capacitors also can be used if large capacitance is needed, such as tantalum, POSCAP and OSCON. Such capacitors have lower ESR zero frequency, $1 / (2\pi ESR \times C)$, than ceramic capacitors. The lower ESR zero frequency can affect the control loop if it is close to the crossover frequency. If high switching frequency and high crossover frequency are desired, an all ceramic capacitor design is sometimes more appropriate.

9.6 Compensation Circuit

The LM21305 is designed to achieve high performance in terms of the transient response, audio susceptibility and output impedance, and will typically require only a single resistor R_c and capacitor C_{c1} for compensation. However, depending on the power stage, it could require a second capacitor to create a high frequency pole to cancel the output capacitor ESR.

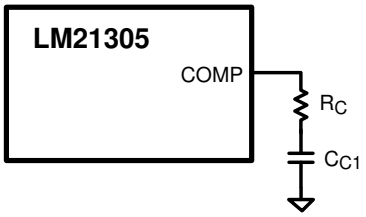


Figure 9-1. LM21305 Compensation Network

To select the compensation components, a desired cross over frequency f_c should be selected first. It is recommended to select f_c equal to or lower than $f_s/6$. A simplified procedure is given below for R_c and C_{c1}, assuming the capacitor ESR zero is at least three times higher than f_c. The compensation resistor can be found by:

$$R_c = \frac{1}{Gain_0} \times \frac{f_c}{f_p} = \frac{V_{OUT}}{V_{FB}} \times 302 \times f_c \times C_{OUT} \quad (7)$$

C_{c1} does not affect the crossover frequency f_c, but it sets the compensator zero f_{Zcomp} and affects the phase margin of the loop. For a fast design, C_{c1} = 4.7 nF gives adequate performance in most LM21305 applications. Larger C_{c1} capacitance gives higher phase margin but at the expese of longer transient response settling time. It is recommended to set the compensation zero no higher than $f_c/3$ to ensure enough phase margin, implying:

$$C_{c1} \geq \frac{3}{2\pi R_c f_c} \quad (8)$$

For more details, see the *LM21305 5A Adjustable Frequency Synchronous Buck Regulator Data Sheet* (SNVS639).

10 PCB Layout

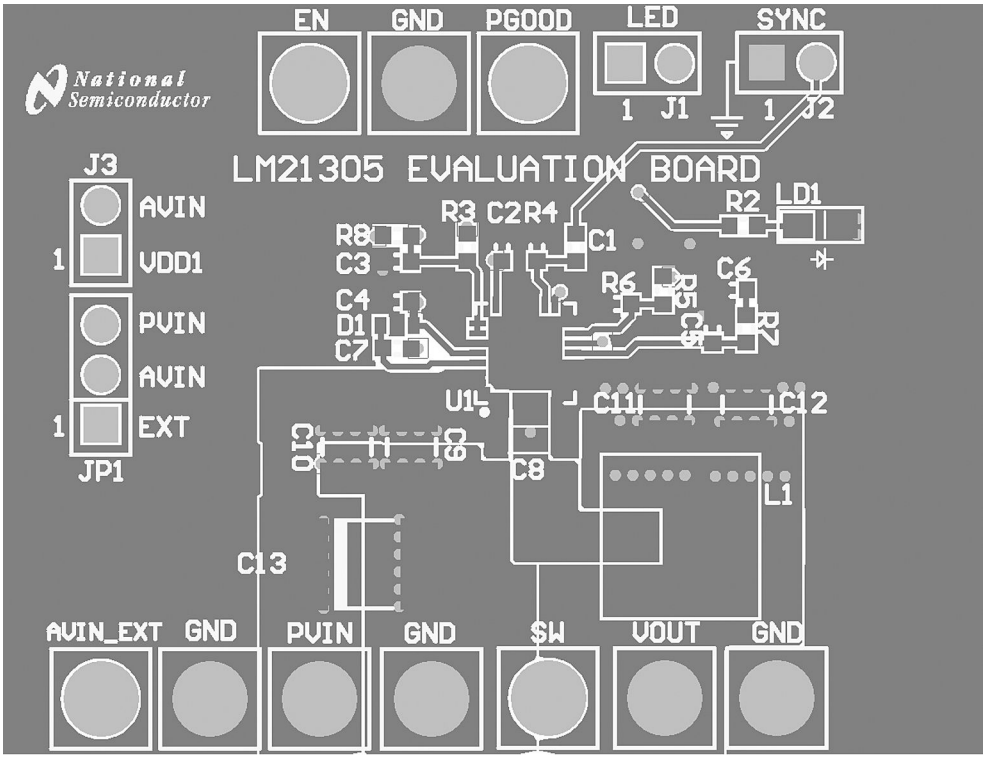


Figure 10-1. PCB Top Layer

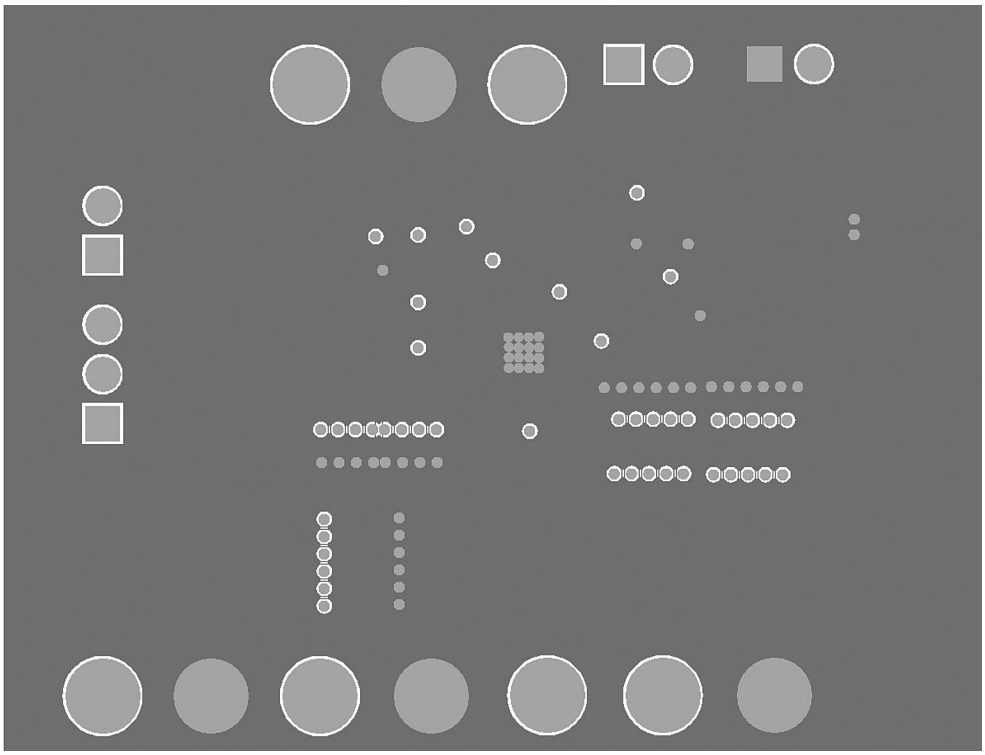


Figure 10-2. PCB Middle Layer 1

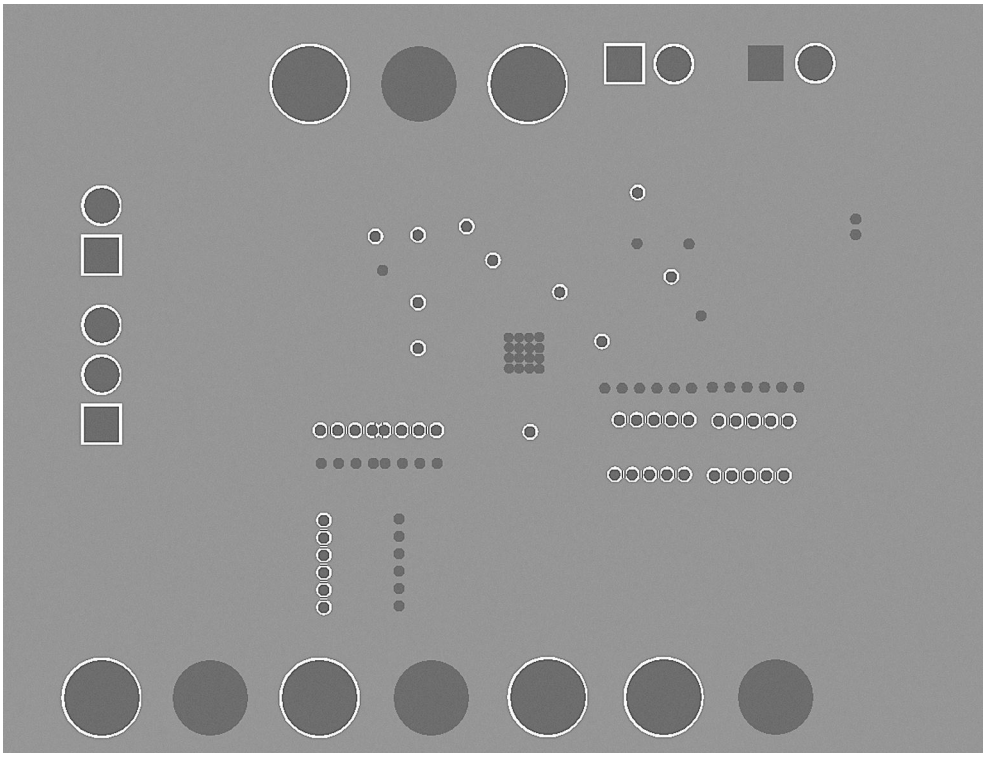


Figure 10-3. PCB Middle Layer 2

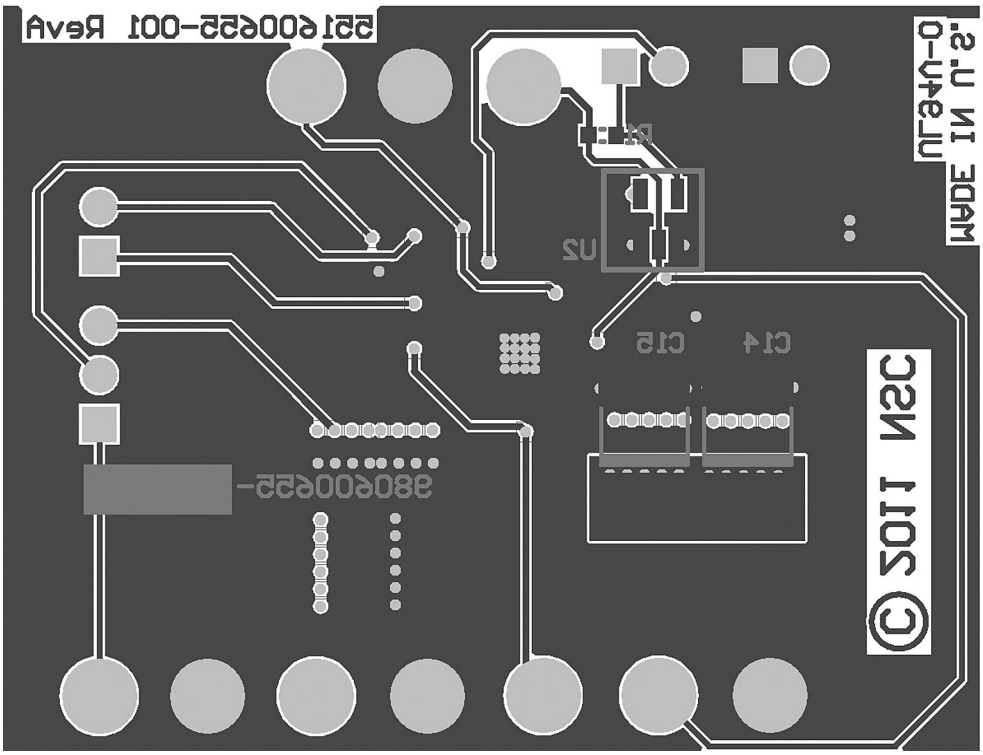


Figure 10-4. PCB Bottom Layer

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D (January 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title.	2

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