Technical Brief
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Performance Analysis of Fast Current Loop (FCL) in Servo Drives Using SFRA on C2000™ Platform

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ABSTRACT

The latest C2000 Delfino™ family of microcontrollers supports fast current loop (FCL) implementation for high bandwidth control of motor drives over a wide speed range in high end multi axes industrial servo control applications. Due to the stringent computational demands of the control algorithm and the demands of interfacing to various position feedback sensors used in these applications, traditionally FPGAs and discrete ADCs have been widely used to implement the core control solution. However, recent C2000 MCUs can cost effectively replace FPGAs and external ADCs in these applications and exceed the functional requirements due to superior features. This technical brief analyses the functional behavior of the servo loops using fast current loop algorithms in terms of bandwidth and phase margin. The test bench consists of a motor-generator set (2MTR-DYNO), an F28379D launch pad (LAUNCHXL-F28379D) and TI's low voltage GaN inverter modules (BOOSTXL-3PHGANINV). The results show a three times improvement in current loop bandwidth for a given phase margin.

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Trademarks

1 Introduction

High performance motor drives in servo control applications are expected to provide high precision and high bandwidth control of current, speed and position loops for superior control of end applications such as robotic arm, CNC machines, and so forth. Since the current loop makes up the inner most control loop, it must have a high bandwidth to enable the outer speed or position loops to be faster. Hence, a high bandwidth FCL is needed in high performance industrial servo control applications. However, the delay due to ADC conversion and algorithm execution limit the current controller bandwidth to about a tenth of the sampling frequency.

The major challenge in digital motor control systems is the influence of the sample and hold (S/H) and transportation delay inside the loop that slows down the system. In a time critical algorithm such as the fast current loop, the latency between feedback sampling and PWM update should be as small as possible. A minimal current loop time not only helps to improve the control bandwidth, but it also enables a higher modulation index (M-I) for the inverter. A higher M-I translates into the higher phase voltage that the inverter can apply on the motor. Higher loop latency will reduce the maximum available voltage and can restrict the rate of current change in the motor, thereby, adversely impacting the controller performance.

In addition to latency considerations, the flexibility to interface various position encoders to the control system can justify the need for FPGAs and external ADCs to implement the fast current loop. However, with the advent of new generation C2000 microcontrollers, it is now possible to replace the functionality of FPGAs and external ADCs. In addition, the MCU can also run speed and position loops with a minimal board space, thereby providing a cost effective solution. This paper outlines the implementation of fast current loop on a C2000 platform running two mechanically coupled motors, and verifies the frequency response of the control loops using TI's Software Frequency Response Analyzer (SFRA) software library. Dynamic frequency response analysis in real-time on a motor drive system is unique among MCU suppliers and is currently capable only on C2000 MCUs.

2 Control System

The speed control block diagram of a field oriented control (FOC) based AC motor control system is shown in Figure 1. The current loop is highlighted because this is the inner most loop and has a higher influence on the bandwidth of the outer speed and position loops. For the outer loop to have a higher bandwidth, the inner loop must have a far higher bandwidth, typically more than 3 times.

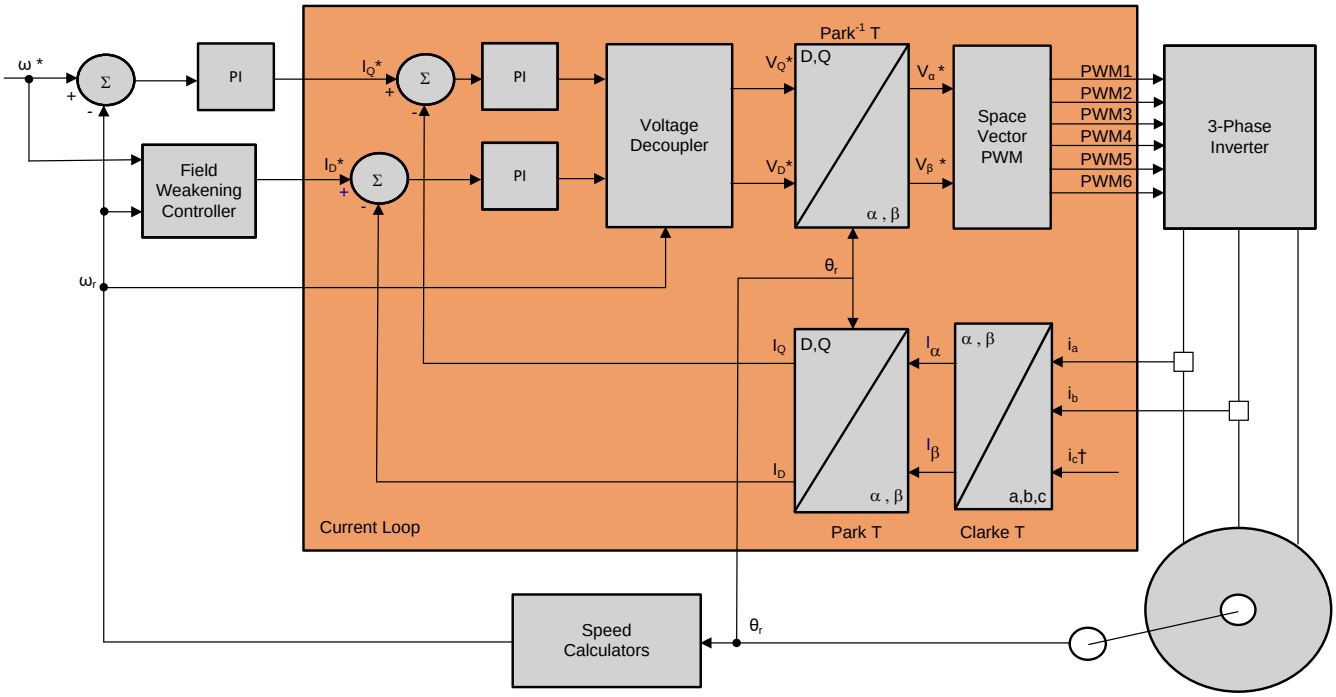

Figure 1. Speed Control Block Diagram of AC Motors

3 PWM Update Latency

The major challenge in implementing the current loop lies in reducing the latencies between feedback sampling and PWM updates. In traditional control schemes, this latency is typically one sampling period thereby delaying the control action. In other words, it leads to one sampling period of inaction to any disturbances in the loop. For a fast current loop, this delay must be as small as possible to improve the loop performance over the wide operating speed range of the motor. Typically, a latency of one microsecond or less is considered acceptable in many applications, and is illustrated in Figure 2. This requires a controller with a fast compute engine, a fast ADC, low latency control peripherals and a superior control algorithm. The TMS320F2837x has the much needed architecture and hardware on-chip to deliver higher performance. The FCL library running on this C2000 MCU, provides the high performance algorithmic support.

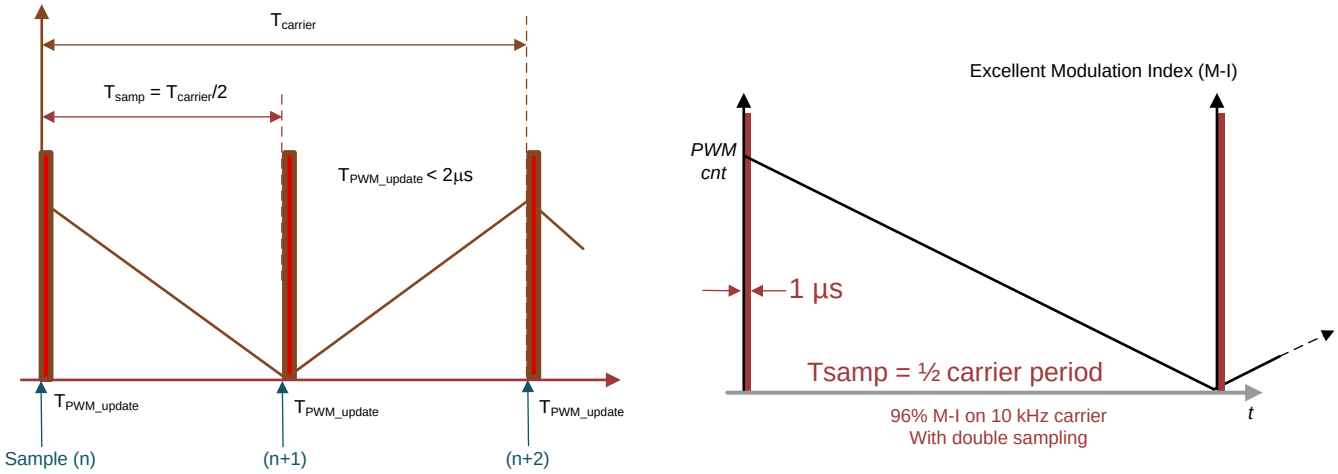

Figure 2. PWM Update Latency

4 FCL Library

TI provides the algorithm for fast current loop as a linkable library that utilizes the following features in the F2837x MCU

- 4 high speed 12-/16-bit ADCs
- Trigonometric and Math Unit (TMU)
- Parallel processing core - Control Law Architecture (CLA)
- Enhanced PWM
- Enhanced QEP or Absolute encoder feedback

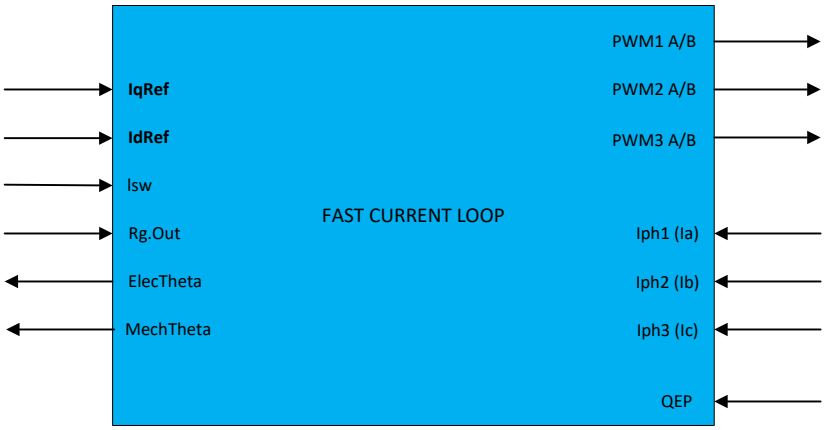

Figure 3. Fast Current Loop (FCL) Library Block Diagram

The block diagram of the FCL library with its inputs and outputs is shown in Figure 3. The earlier version of the FCL library, *Fast Current Loop Library* , partitions the algorithm across CPU, CLA and TMU to bring down the PWM update latency to less than one microsecond. Further optimization is possible if the algorithm is written in assembly. FCL is available as a published example as in C2000 DesignDRIVE application through controlSUITE software. However, in the context of this analysis, the coding process is simplified using only one CPU. The Fast Current Loop(FCL), frequency response analysis (SFRA) and multiple axis control are integrated in this example to facilitate performance evaluation. The entire control algorithm for both motors is run on CPU1 without using the CLA or the second CPU core on the F28379D. The modified FCL library, *Fast Current Loop (C28x) Library* , supports a complex PI controller.

5 SFRA Library

Texas Instruments' Software Frequency Response Analyzer (SFRA) library is designed to enable frequency response analysis on any digitally controlled closed loop system using software only. This enables performing frequency response analysis of the closed loop system with relative ease as no external connections or equipment is required. The optimized library can be used to identify the plant and the open loop characteristics of a closed loop system. In this study, it can be used to get stability information such as the gain margin, phase margin and bandwidth to evaluate the control loop performance.

Consider a digitally controlled closed loop power converter, as shown in Figure 4, where:

- H is the transfer function of the plant that needs to be controlled,
- G is the digital compensator,
- GH is referred to as the open loop transfer function
- r is the instantaneous set point or the reference of the converter,
- Ref is the DC set point reference,
- y the ADC feedback,
- e the instantaneous error,
- d the sensor noise/disturbance,
- u the PWM duty cycle.

The key objectives of the compensator in a closed loop system can be summarized as:

- Ensure system is stable, that is, system tracks the reference asymptotically:

$$e = \lim_{t\to\infty} e(t) = \lim_{t\to\infty} \frac{r}{(1+GH)} \to 0 \tag{1}$$

- System provides disturbance rejection to guarantee robust operation:

$$S = \frac{y}{d} = \frac{1}{1+GH} \to 0 \tag{2}$$

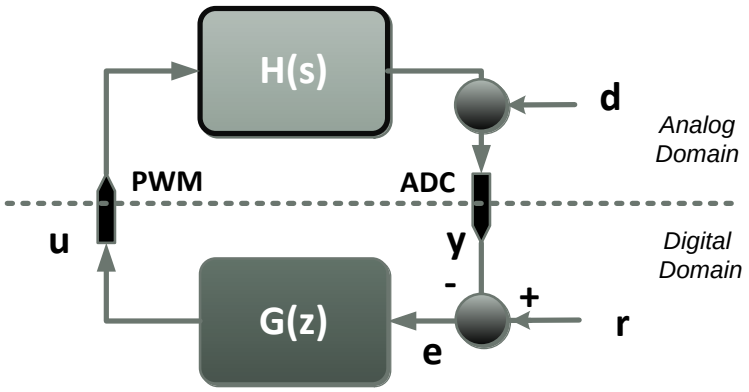

Figure 4. Digitally Controlled Control System

It is clear from Equation 1 and Equation 2 that by knowing the open loop transfer function (GH), one can determine if the system meets the objectives. A Bode plot of the open loop transfer function GH is frequently used for this purpose and quantities such as gain margin(GM), phase margin(PM) and bandwidth (BW) are often used to comment on the stability and robustness of a closed loop system.

SFRA library can enable measurement of the GH and H frequency response by software. This data can be used to:

- Verify the plant model (H) or extract the plant model (H)
- Design a compensator (G) for the closed loop plant
- Verify the close loop performance of the system by plotting the open loop (GH) Bode diagram

As the frequency response of GH and H carry information of the plant, the data can be used to comment on the health of the power stage or control loop by periodically measuring the frequency response.

This library is used to study the current loop performance in motor drive system.

6 Evaluation

The system evaluation consists of two parts:

- Implementing FCL for inner current loop control in two servo drives
- Performance analysis of FCL using SFRA and obtain the loop bandwidth

Implementing FCL consists of integrating the library inside the speed control loop. However, performance analysis and bandwidth determination needs some considerations. In order to study the current loop bandwidth, the back emf component of the loop needs proper decoupling or compensation otherwise it can influence and distort the analysis. At zero speed when there is no back emf, the loop performance can be analyzed using frequency response analysis methods. This can be used as a reference to verify the same at different speeds to see if there is any change in the controller behavior. This helps to ensure the robustness of controller implementation at various speeds. To perform this effectively, a motor generator set, like the 2MTR-DYNO, that can hold zero speed is helpful. The software is built such that two different motors, controlled independently, are coupled together as motor-generator for performing frequency response analysis on the current loop of the generator while the other motor is controlled in constant speed mode. Since the speed is held constant by the drive motor, the generator current loop sees minimal speed jitter, if any. This helps to obtain a frequency analysis report free of speed related jitters. Once the user is comfortable with the test, the same can be repeated on drive side motor too for verification.

The evaluation setup is built using hardware that is readily available from TI and is given in the next section. It consists of an F28379D MCU based LaunchPad, inverter BoosterPack based off GaN+INA240, and a motor-dyno set for load testing the drive motor.

The inverter booster pack provides in-line current sense feedback using the high performance current sense amplifier INA240 that provides the instantaneous motor currents at all times. This allows the FCL algorithm to study several sampling schemes and their impact on loop bandwidth.

6.1 Hardware

The details of the evaluation hardware, all available from TI eStore, and reference to their user guides are given below:

- Controller - LAUNCHXL-F28379D - 1 unit – *LAUNCHXL-F28379D Overview User's Guide*
- Inverter (INV) - BOOSTXL-3PHGANINV - 2 units – *BOOSTXL-3PhGaNInv Evaluation Module User Guide*
- Motor Dyno Set - 2MTR-DYNO - 1 unit (2 motors with mounting hardware)

A lab power supply (variable) rated at 48V/5A will be sufficient to run these experiments. In this document, the inverter is sometimes referred as digital motor control (INV) kit for convenience.

6.1.1 Launch Pad

For immediate reference, the layout of LAUNCHXL-F28379D is given in Figure 5 . For further details, see the *LAUNCHXL-F28379D Overview User's Guide* .

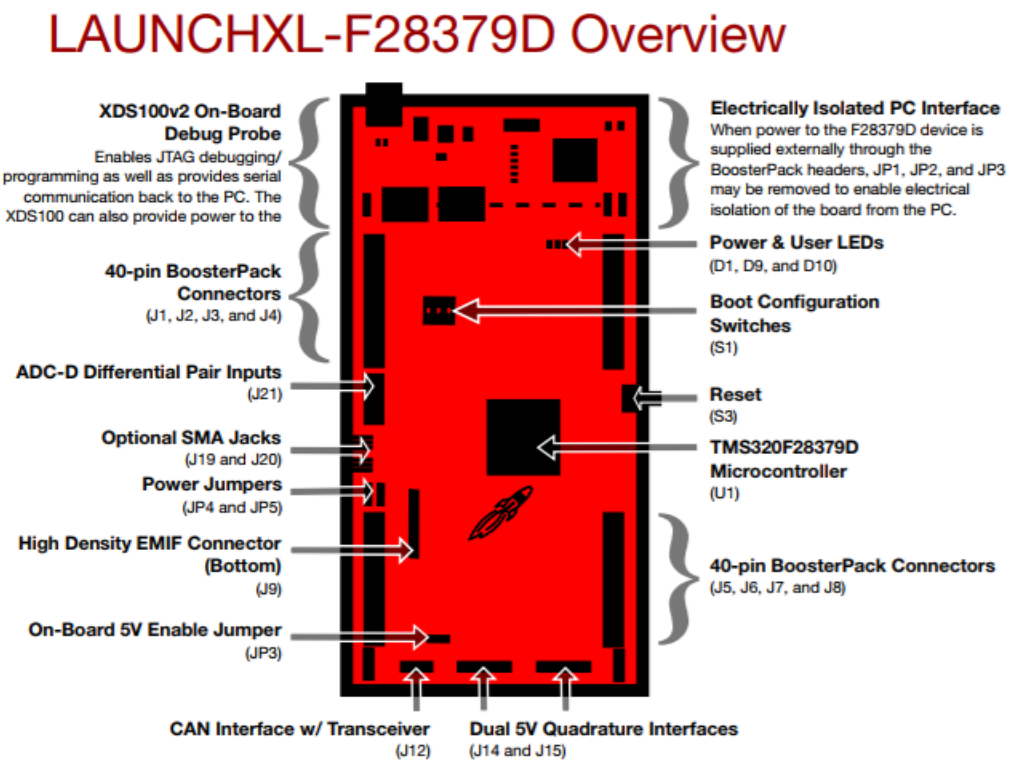

Figure 5. Layout of LAUNCHXL-F28379D

It can support controlling two motors with QEP position feedback. In addition, it has a couple of SPI ports available that can be used to drive SPI configurable inverters. While this board can support external AFE to bring in Absolute encoders signals, this document is currently limited to show the analysis using QEP as the position feedback mechanism

6.1.1.1 PWM DACs

LaunchPad has four PWM-DACs, referenced in this document as PWMDAC1-4. They are available on jumper pins J4-31 and J4-32, and J8-71 and J8-72. PWM-DACs are basically low pass filtered signals that are originally given out as high frequency PWM carrier signals modulating the signal of interest. In the evaluation project, these PWMDACs are used to display intermediate system variables for debug purposes.

6.1.1.2 DACs

LaunchPad also has a couple of DACs available on jumper pins J3-30 and J7-70. Depending on the booster pack in use, they may or may not be available as DAC. With the GaN BoosterPack, this functionality is not available as it is used up by this BoosterPack.

6.1.2 Inverter - BOOSTXL-3PHGANINV

For immediate reference, the functional block diagram of BOOSTXL-3PHGANINV is given in Figure 6 . For more details, see the *BOOSTXL-3PhGaNInv Evaluation Module User Guide* .

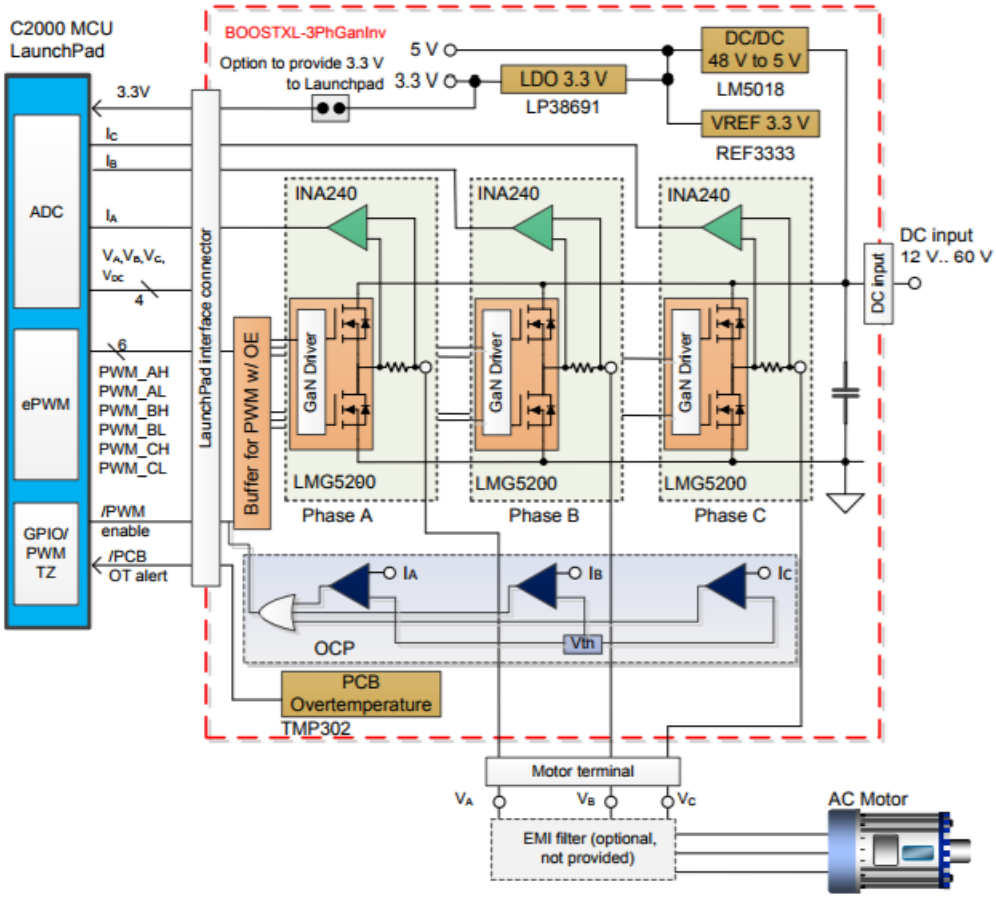

Figure 6. BOOSTXL-3PHGANINV Functional Block Diagram

Because of the dimensions of the GaN + INA240 booster pack (BP), it is not practical to fit two of them on the same side of a launch pad. One of the mounting methods is shown in Figure 7 that uses 2x10 headers for not only extending the signals out but also for providing some spatial clearance between various PCBs giving better clarity. Depending on user convenience, a passive extender board can be designed to bring out a pair of launch pad headers to mount the second booster pack or a short flat 20 pin ribbon cable can be used.

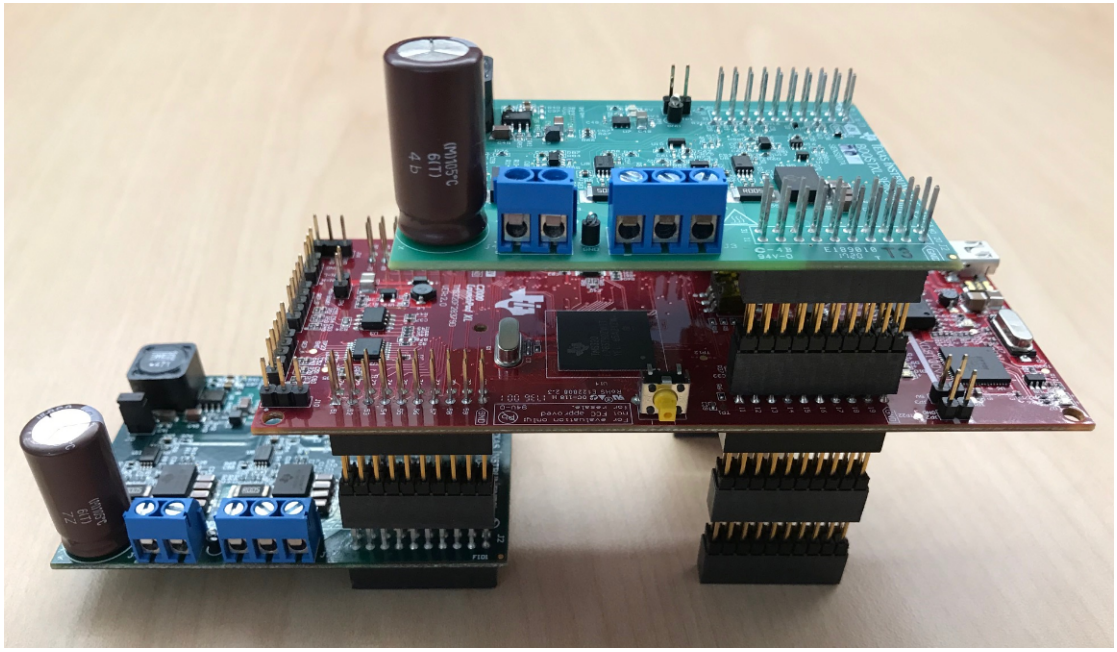

Figure 7. Dual Motor Control Assembly With LAUNCHXL-F28379D and BOOSTXL-3PHGANINV

6.1.3 Two Motor Dyno

The two motor dyno setup helps to perform load test on the drive motor by mechanically coupling it to the other motor that acts as a generator. The kit comes with a coupler, mounting screws and key. The motor-dyno set can be assembled as shown in Figure 8.

Figure 8. Two Motor Dyno Set

6.2 Software

The software is developed based on FCL and SFRA libraries released already in C2000 MCU software environment called controlSUITE. FCL is used to improve the current loop bandwidth and SFRA is used to do frequency response analysis of any control loop. For ease of evaluation, the FCL library is customized toexecute out of CPU1 to control two motors. This solution can adapted using F28379D's dual CPU cores and their CLAs to further speed up the computation, which will facilitate a higher DC bus utilization by the inverter and increase the motor speed range. The software is built such that two different motors can be controlled independently and then coupled together as motor-generator for performing frequency response analysis.

6.2.1 Incremental System Build

The system is incrementally built up like any other projects in controlSUITE. In each build level, a certain operation of the system, be it hardware or software, is verified and integrated incrementally. In the final build level, all operations are integrated to show case the complete system. Software modules are written as either C macros or C callable functions. Table 1 summarizes the functional integration and library integrated in each incremental system build.

Table 1. Testing Modules in Each Incremental System Build

Build Level	Functional Integration	Library
Level 1	PWM generation	
Level 2	Run motor open loop - feedback verification and calibration	
Level 3	Run motor current loops using FCL library	FCL
Level 4	Run motor speed loop with the inner current loop using FCL library	FCL
Level 5	Fun both motors - one as motor and another as generator	FCL
Level 6	Use SFRA GUI to run SFRA on target CPU - CPU using SFRA library	SFRA

FCL implementation is gradually built up through build levels 1 through 4. Frequency response analysis is gradually built up through build levels 5 and 6. Build levels 1 throgh 4 can be done withthe motor shafts coupled together or decoupled, but levels 5 and 6 require the motor shafts be coupled so as to perform load tests as well as frequency response analysis.

6.2.2 QEP Calibration

Both motors in the test set up have QEPs, and they both need to be calibrated before using them for control. Calibration is nothing but knowing the position of QEP index pulse in the circular span of one rotation. Each motor will be spun for a maximum of one rotation until it catches its QEP index pulse. When the motor shafts are disengaged, it is trivial to do the alignment. Motor 1 shaft is brought to alignment followed by spinning it one direction until its QEP index pulse is received. Then the same is repeated on motor 2. However, when the two shafts are connected together, a coordinated sequence is followed. Firstly, the shaft will move to a certain position and hold for a while (alignment by motor 1) before spinning slowly. When QEP1 index pulse is received, motor 1 will stop spinning the shaft and leave it to the control of motor 2. Notice that the shaft will realign to another position for a while (alignment by motor 2), before spinning in opposite direction until QEP2 index pulse is received.

6.2.3 FCL Integration - Build Levels 1-5

By working through build levels 1 through 4 as mentioned in table 1, the control hardware can be calibrated for analog feedbacks, QEP can be verified and FCL library can be integrated into the controller to run two motors independently. The control block diagram of build level 4 is shown in Figure 9. Completion of this build level signifies that FCL integration is successful and that the motors could be independently controlled in speed loop. Once this is established, the motor shafts can be coupled together for verification of motor generator operation by working through build level 5.

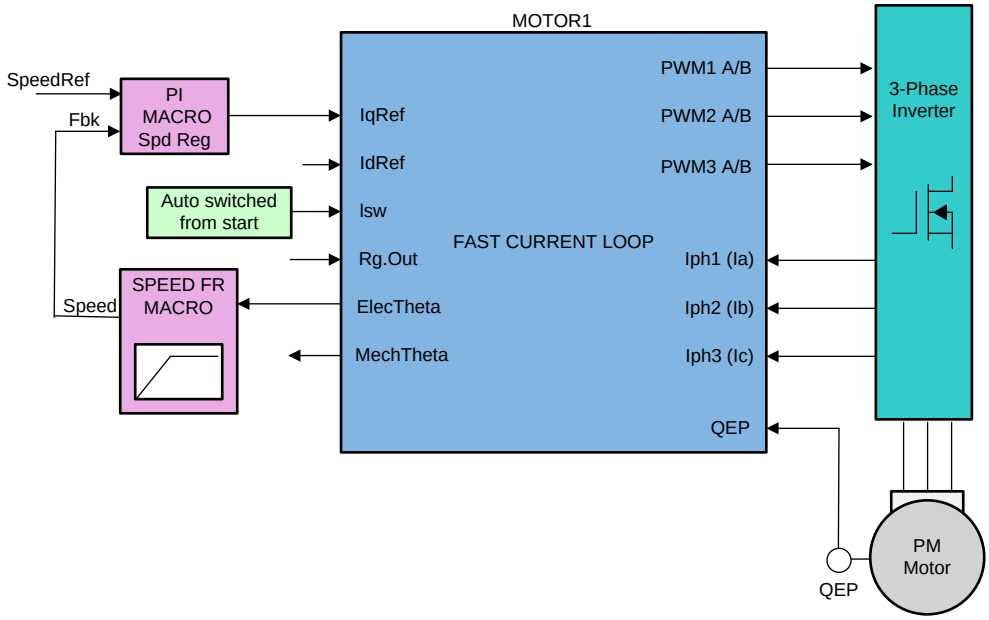

Figure 9. Level 4 Incremental System Build Block Diagram

6.3 SFRA Integration - Build Level 6

Successful completion of build level 5 enables performance analysis of the current loop in build level 6. The control block diagram of the twin motor assembly is shown in Figure 10.

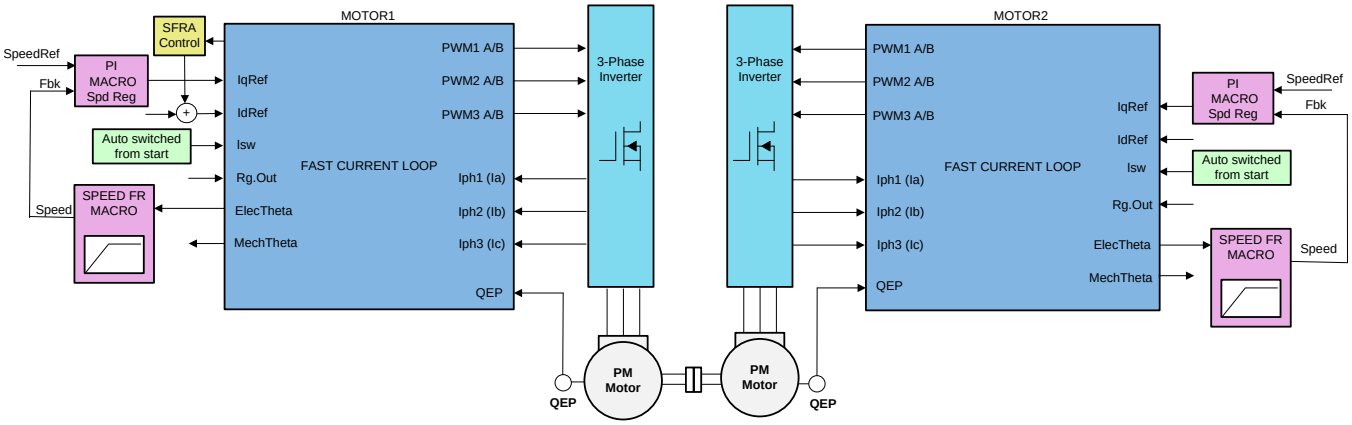

Figure 10. Level 6 Incremental System Build Block Diagram

Build level 6 integrates the SFRA library where it injects a small noise into the control loop under test and monitors the system response and identifies the magnitude and phase response of the loop at various noise frequencies. This information is all stored in the CPU memory as local data. Using a PC based GUI tool for SFRA, this SFRA data is transferred through USB/JTAG and the GUI tool plots the gain response and phase response of the system at the frequencies the loop was tested. A typical plot is shown in Figure 11 and Figure 12. From the gain and phase plots, it identifies the gain margin, phase margin and loop bandwidth and displays them at the bottom.

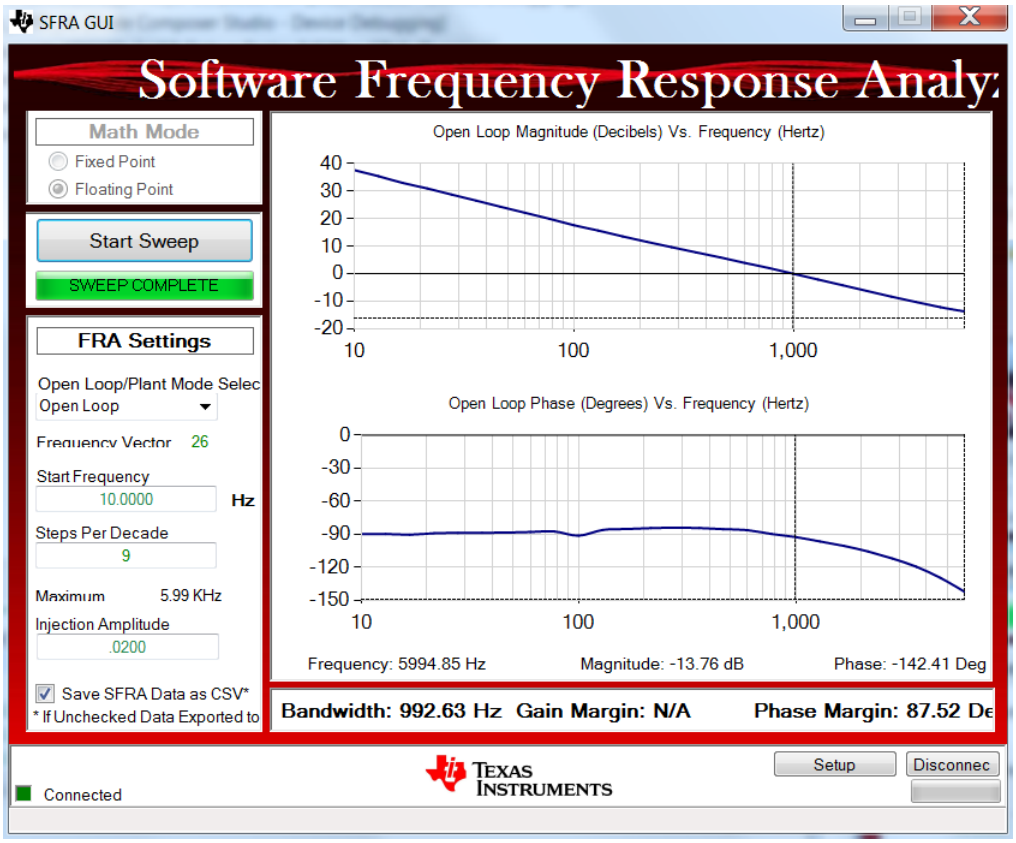

Figure 11. SFRA Plot of Current Loop With Moderate Bandwidth Design

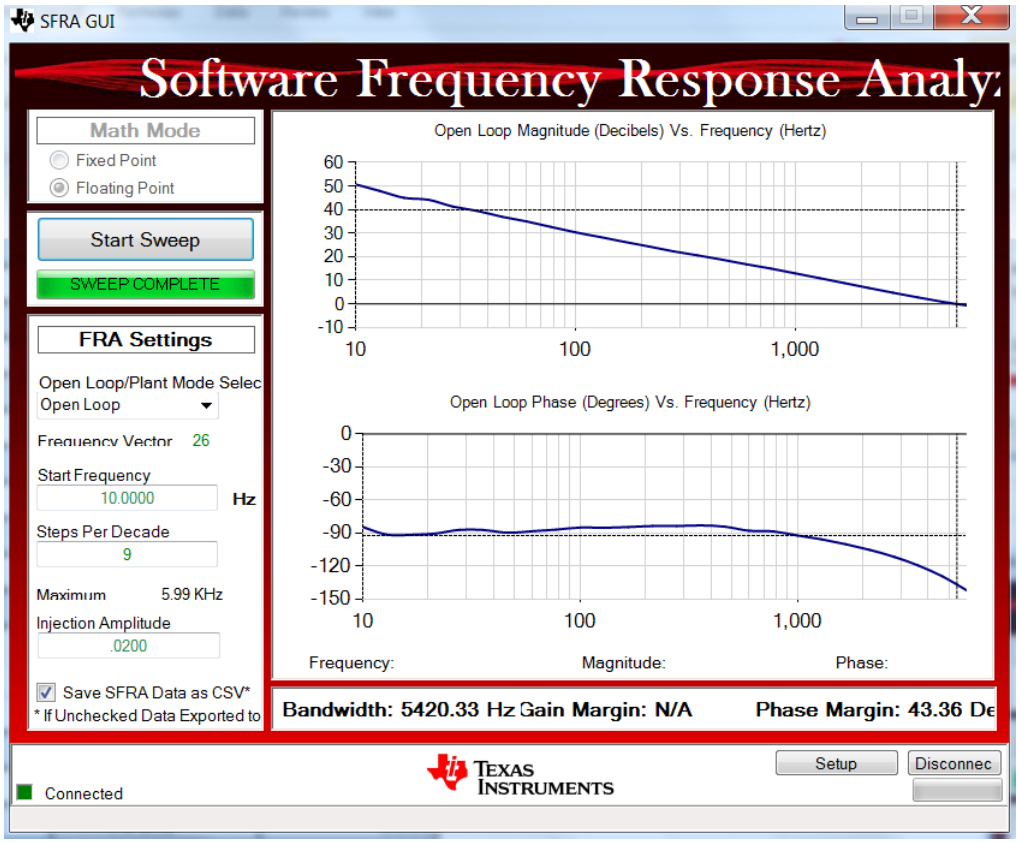

Figure 12. SFRA Plot of Current Loop With Higher Bandwidth Design

These are plots of the D-axis current loop FRA showing a bandwidth of 992Hz and 5420Hz as against the designed 1100 Hz and 5000Hz bandwidths, respectively. As mentioned earlier, the test can be performed at zero speed and obtain the bandwidth, phase margin and gain margin for reference. This test can then be repeated at different speeds and load conditions to verify if there is any change in bandwidth or phase margin from that obtained at zero speed. Any variation in the plot at different speed is indicative of the quality of decoupling in control loops. However, with this test setup, it can be seen that the bandwidth remains nearly the same regardless of running speed. This test can be repeated for Q loop as well, and at different bandwidth settings.

7 Comparison of Current Loops - Classical vs FCL

The test setup enables the users to test the current loop by controlling it using conventional method as well for comparison purposes. Two sets of tests are performed, one with, and the other without, FCL. The bandwidth and phase margin results obtained at different bandwidth design settings are noted down for each set of tests, and the collected data are plotted as shown in Figure 13.

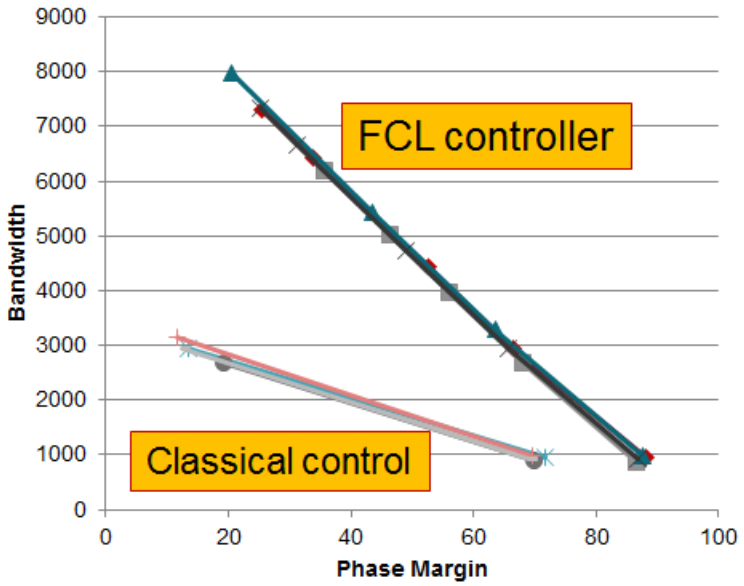

Figure 13. Plot of Gain Margin vs Phase Margin as Experimentally Obtained

The group of plots at the bottom is obtained with conventional control (without using FCL) and the one at the top is obtained with FCL. It is self-revealing that, without FCL, the control bandwidth is too low and that with increasing control bandwidth, the phase margin is decreasing drastically. When FCL is used, the controller can provide a higher bandwidth at a higher phase margin and that the reduction in phase margin for increase in bandwidth is much less. The best performance is found to be when the bandwidth is about 1/6th of the sampling frequency where it almost behaves like deadbeat control. For frequencies beyond that, overshoots may be noticed. In this particular evaluation, the PWM carrier is 10 kHz, the sampling frequency is 20 KHz and the best performance is obtained when the control bandwidth is 3.3 KHz.

8 Summary

This evaluation platform helps to control two different motors, either from one CPU core or two different CPU cores, and with or without FCL technology. When FCL is used, it shows an increase in control bandwidth. The SFRA tool showed the impact of FCL on control bandwidth.

Dynamic frequency response analysis in real-time on a motor drive system is unique among MCU suppliers and is currently capable only on C2000 MCUs. The presence of fast ADC, control law architecture (CLA) and trigonometric math unit (TMU) helps to reduce the latency between feedback sampling and PWM update resulting in higher control bandwidth and increase in maximum modulation index. Higher modulation index helps to improve DC bus utilization by the drive and to increase the control speed range of the motor.

Depending on the control speed range of motors in target applications, the MCU is possible to control multiple motors in multi-axes configurations using FCL based off the dual core F28379D MCU platform. This makes it suitable for high end servo control applications.

9 References

- *Fast Current Loop Library*
- *Fast Current Loop (C28x) Library*
- *LAUNCHXL-F28379D Overview User's Guide*
- *BOOSTXL-3PhGaNInv Evaluation Module User Guide*

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