Technical Reference Manual

AM263Px Register Addendum

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Read This First

About This Register Addendum

This Register Addendum (RA) provides detailed register references for each peripheral and subsystem in the device including:

- Register Address
- Register Name
- Register Types
- Register Reset Values
- Register Descriptions
- Bit-field Descriptions

Register Access Type Codes

Table 1-1. Access Type Codes

Access Type	Description
R	Read
R/W	Read / Write
R/W1TC	Read/Write 1 To Clear
R/W1TS	Read/Write 1 To Set
W	Write

This Register Addendum has been created in order to make the Technical Reference Manual a more effective and size-efficient collateral document.

Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

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Related Documentation From Texas Instruments

For a complete listing of related documentation and development-support tools for the device, visit the Texas Instruments website at www.ti.com.

- AM263Px Data sheet
- AM263Px Errata
- AM263Px Technical Reference Manual
- AM263Px Register Addendum
- AM263Px Flash Selection Guide
- Submit request for AM263Px HSM Addendum here.

AM263Px Software

- Sitara MCU+ Academy for AM26x URL
- MCU-PLUS-SDK-AM263Px

AM263Px Product Folders

- AM263P Product Folder

AM263Px Evaluation Modules

- AM263Px LaunchPad (LP-AM263P)
- AM263Px controlCARD (TMDSCNCD263P)

Note on Register Names

Sub section headers and figure titles show different naming conventions for the registers, but the header and figure are referring to the same register. The different naming conventions help legacy users search for registers. A future revision of this document can align the registers names

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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1 Memory Map

This chapter summarizes the memory map address regions for the device.

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1.1 Device Memory Map

This section describes the device memory map.

Note

The memory locations not shown are either unallocated or reserved and not used.

Accesses to these locations are not recommended and must be avoided.

Table 1-1.

Region Name	Start Address	End Address	Size
Core-specific Internal Memory Map [1]	0x0000 0000	0x1FFF FFFF	537 MB
MCRC0	0x3500 0000	0x3500 03FF	1 KB
STM_STIM0	0x3900 0000	0x39FF FFFF	16 MB
MPU_L2OCRAM_BANK0	0x4002 0000	0x4002 03FF	1 KB
MPU_L2OCRAM_BANK1	0x4004 0000	0x4004 03FF	1 KB
MPU_L2OCRAM_BANK2	0x4006 0000	0x4006 03FF	1 KB
MPU_L2OCRAM_BANK3	0x4008 0000	0x4008 03FF	1 KB
MPU_R5SS0_CORE0_AXIS	0x400A 0000	0x400A 03FF	1 KB
MPU_R5SS0_CORE1_AXIS	0x400C 0000	0x400C 03FF	1 KB
MPU_R5SS1_CORE0_AXIS	0x400E 0000	0x400E 03FF	1 KB
MPU_R5SS1_CORE1_AXIS	0x4010 0000	0x4010 03FF	1 KB
MPU_MBOX_SRAM	0x4014 0000	0x4014 03FF	1 KB
MPU_FSS_DATA	0x4016 0000	0x4016 03FF	1 KB
MPU_SCRM2SCRP0	0x4018 0000	0x4018 03FF	1 KB
MPU_SCRM2SCRP1	0x401A 0000	0x401A 03FF	1 KB
MPU_R5SS0_CORE0_AHB	0x401C 0000	0x401C 03FF	1 KB
MPU_R5SS0_CORE1_AHB	0x401E 0000	0x401E 03FF	1 KB
MPU_R5SS1_CORE0_AHB	0x4020 0000	0x4020 03FF	1 KB
MPU_R5SS1_CORE1_AHB	0x4022 0000	0x4022 03FF	1 KB
MPU_FSS_CONFIG	0x4026 0000	0x4026 03FF	1 KB
MPU_R5SS0	0x4028 0000	0x4028 03FF	1 KB
MPU_R5SS1	0x402A 0000	0x402A 03FF	1 KB
MPU_L2OCRAM_BANK4	0x402C 0000	0x402C 03FF	1 KB
MPU_L2OCRAM_BANK5	0x402E 0000	0x402E 03FF	1 KB
ICSSM0_INTERNAL [1]	0x4800 0000	0x4803 FFFF	256 KB
ICSSM0_ECC_AGGR	0x4810 0000	0x4810 03FF	1 KB
MMC0	0x4830 0000	0x4830 1FFF	8 KB
CONTROLSS_EPWM0_G0	0x5000 0000	0x5000 0FFF	4 KB
CONTROLSS_EPWM1_G0	0x5000 1000	0x5000 1FFF	4 KB
CONTROLSS_EPWM2_G0	0x5000 2000	0x5000 2FFF	4 KB
CONTROLSS_EPWM3_G0	0x5000 3000	0x5000 3FFF	4 KB
CONTROLSS_EPWM4_G0	0x5000 4000	0x5000 4FFF	4 KB
CONTROLSS_EPWM5_G0	0x5000 5000	0x5000 5FFF	4 KB
CONTROLSS_EPWM6_G0	0x5000 6000	0x5000 6FFF	4 KB
CONTROLSS_EPWM7_G0	0x5000 7000	0x5000 7FFF	4 KB
CONTROLSS_EPWM8_G0	0x5000 8000	0x5000 8FFF	4 KB
CONTROLSS_EPWM9_G0	0x5000 9000	0x5000 9FFF	4 KB
CONTROLSS_EPWM10_G0	0x5000 A000	0x5000 AFFF	4 KB
CONTROLSS_EPWM11_G0	0x5000 B000	0x5000 BFFF	4 KB

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Table 1-1. (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_EPWM12_G0	0x5000 C000	0x5000 CFFF	4 KB
CONTROLSS_EPWM13_G0	0x5000 D000	0x5000 DFFF	4 KB
CONTROLSS_EPWM14_G0	0x5000 E000	0x5000 EFFF	4 KB
CONTROLSS_EPWM15_G0	0x5000 F000	0x5000 FFFF	4 KB
CONTROLSS_EPWM16_G0	0x5001 0000	0x5001 0FFF	4 KB
CONTROLSS_EPWM17_G0	0x5001 1000	0x5001 1FFF	4 KB
CONTROLSS_EPWM18_G0	0x5001 2000	0x5001 2FFF	4 KB
CONTROLSS_EPWM19_G0	0x5001 3000	0x5001 3FFF	4 KB
CONTROLSS_EPWM20_G0	0x5001 4000	0x5001 4FFF	4 KB
CONTROLSS_EPWM21_G0	0x5001 5000	0x5001 5FFF	4 KB
CONTROLSS_EPWM22_G0	0x5001 6000	0x5001 6FFF	4 KB
CONTROLSS_EPWM23_G0	0x5001 7000	0x5001 7FFF	4 KB
CONTROLSS_EPWM24_G0	0x5001 8000	0x5001 8FFF	4 KB
CONTROLSS_EPWM25_G0	0x5001 9000	0x5001 9FFF	4 KB
CONTROLSS_EPWM26_G0	0x5001 A000	0x5001 AFFF	4 KB
CONTROLSS_EPWM27_G0	0x5001 B000	0x5001 BFFF	4 KB
CONTROLSS_EPWM28_G0	0x5001 C000	0x5001 CFFF	4 KB
CONTROLSS_EPWM29_G0	0x5001 D000	0x5001 DFFF	4 KB
CONTROLSS_EPWM30_G0	0x5001 E000	0x5001 EFFF	4 KB
CONTROLSS_EPWM31_G0	0x5001 F000	0x5001 FFFF	4 KB
CONTROLSS_EPWM_WLINK_G0	0x5002 0000	0x5002 0FFF	4 KB
CONTROLSS_EPWM0_G1	0x5004 0000	0x5004 0FFF	4 KB
CONTROLSS_EPWM1_G1	0x5004 1000	0x5004 1FFF	4 KB
CONTROLSS_EPWM2_G1	0x5004 2000	0x5004 2FFF	4 KB
CONTROLSS_EPWM3_G1	0x5004 3000	0x5004 3FFF	4 KB
CONTROLSS_EPWM4_G1	0x5004 4000	0x5004 4FFF	4 KB
CONTROLSS_EPWM5_G1	0x5004 5000	0x5004 5FFF	4 KB
CONTROLSS_EPWM6_G1	0x5004 6000	0x5004 6FFF	4 KB
CONTROLSS_EPWM7_G1	0x5004 7000	0x5004 7FFF	4 KB
CONTROLSS_EPWM8_G1	0x5004 8000	0x5004 8FFF	4 KB
CONTROLSS_EPWM9_G1	0x5004 9000	0x5004 9FFF	4 KB
CONTROLSS_EPWM10_G1	0x5004 A000	0x5004 AFFF	4 KB
CONTROLSS_EPWM11_G1	0x5004 B000	0x5004 BFFF	4 KB
CONTROLSS_EPWM12_G1	0x5004 C000	0x5004 CFFF	4 KB
CONTROLSS_EPWM13_G1	0x5004 D000	0x5004 DFFF	4 KB
CONTROLSS_EPWM14_G1	0x5004 E000	0x5004 EFFF	4 KB
CONTROLSS_EPWM15_G1	0x5004 F000	0x5004 FFFF	4 KB
CONTROLSS_EPWM16_G1	0x5005 0000	0x5005 0FFF	4 KB
CONTROLSS_EPWM17_G1	0x5005 1000	0x5005 1FFF	4 KB
CONTROLSS_EPWM18_G1	0x5005 2000	0x5005 2FFF	4 KB
CONTROLSS_EPWM19_G1	0x5005 3000	0x5005 3FFF	4 KB
CONTROLSS_EPWM20_G1	0x5005 4000	0x5005 4FFF	4 KB
CONTROLSS_EPWM21_G1	0x5005 5000	0x5005 5FFF	4 KB
CONTROLSS_EPWM22_G1	0x5005 6000	0x5005 6FFF	4 KB
CONTROLSS_EPWM23_G1	0x5005 7000	0x5005 7FFF	4 KB
CONTROLSS_EPWM24_G1	0x5005 8000	0x5005 8FFF	4 KB
CONTROLSS_EPWM25_G1	0x5005 9000	0x5005 9FFF	4 KB

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Table 1-1. (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_EPWM26_G1	0x5005 A000	0x5005 AFFF	4 KB
CONTROLSS_EPWM27_G1	0x5005 B000	0x5005 BFFF	4 KB
CONTROLSS_EPWM28_G1	0x5005 C000	0x5005 CFFF	4 KB
CONTROLSS_EPWM29_G1	0x5005 D000	0x5005 DFFF	4 KB
CONTROLSS_EPWM30_G1	0x5005 E000	0x5005 EFFF	4 KB
CONTROLSS_EPWM31_G1	0x5005 F000	0x5005 FFFF	4 KB
CONTROLSS_EPWM_WLINK_G1	0x5006 0000	0x5006 0FFF	4 KB
CONTROLSS_EPWM0_G2	0x5008 0000	0x5008 0FFF	4 KB
CONTROLSS_EPWM1_G2	0x5008 1000	0x5008 1FFF	4 KB
CONTROLSS_EPWM2_G2	0x5008 2000	0x5008 2FFF	4 KB
CONTROLSS_EPWM3_G2	0x5008 3000	0x5008 3FFF	4 KB
CONTROLSS_EPWM4_G2	0x5008 4000	0x5008 4FFF	4 KB
CONTROLSS_EPWM5_G2	0x5008 5000	0x5008 5FFF	4 KB
CONTROLSS_EPWM6_G2	0x5008 6000	0x5008 6FFF	4 KB
CONTROLSS_EPWM7_G2	0x5008 7000	0x5008 7FFF	4 KB
CONTROLSS_EPWM8_G2	0x5008 8000	0x5008 8FFF	4 KB
CONTROLSS_EPWM9_G2	0x5008 9000	0x5008 9FFF	4 KB
CONTROLSS_EPWM10_G2	0x5008 A000	0x5008 AFFF	4 KB
CONTROLSS_EPWM11_G2	0x5008 B000	0x5008 BFFF	4 KB
CONTROLSS_EPWM12_G2	0x5008 C000	0x5008 CFFF	4 KB
CONTROLSS_EPWM13_G2	0x5008 D000	0x5008 DFFF	4 KB
CONTROLSS_EPWM14_G2	0x5008 E000	0x5008 EFFF	4 KB
CONTROLSS_EPWM15_G2	0x5008 F000	0x5008 FFFF	4 KB
CONTROLSS_EPWM16_G2	0x5009 0000	0x5009 0FFF	4 KB
CONTROLSS_EPWM17_G2	0x5009 1000	0x5009 1FFF	4 KB
CONTROLSS_EPWM18_G2	0x5009 2000	0x5009 2FFF	4 KB
CONTROLSS_EPWM19_G2	0x5009 3000	0x5009 3FFF	4 KB
CONTROLSS_EPWM20_G2	0x5009 4000	0x5009 4FFF	4 KB
CONTROLSS_EPWM21_G2	0x5009 5000	0x5009 5FFF	4 KB
CONTROLSS_EPWM22_G2	0x5009 6000	0x5009 6FFF	4 KB
CONTROLSS_EPWM23_G2	0x5009 7000	0x5009 7FFF	4 KB
CONTROLSS_EPWM24_G2	0x5009 8000	0x5009 8FFF	4 KB
CONTROLSS_EPWM25_G2	0x5009 9000	0x5009 9FFF	4 KB
CONTROLSS_EPWM26_G2	0x5009 A000	0x5009 AFFF	4 KB
CONTROLSS_EPWM27_G2	0x5009 B000	0x5009 BFFF	4 KB
CONTROLSS_EPWM28_G2	0x5009 C000	0x5009 CFFF	4 KB
CONTROLSS_EPWM29_G2	0x5009 D000	0x5009 DFFF	4 KB
CONTROLSS_EPWM30_G2	0x5009 E000	0x5009 EFFF	4 KB
CONTROLSS_EPWM31_G2	0x5009 F000	0x5009 FFFF	4 KB
CONTROLSS_EPWM_WLINK_G2	0x500A 0000	0x500A 0FFF	4 KB
CONTROLSS_EPWM0_G3	0x500C 0000	0x500C 0FFF	4 KB
CONTROLSS_EPWM1_G3	0x500C 1000	0x500C 1FFF	4 KB
CONTROLSS_EPWM2_G3	0x500C 2000	0x500C 2FFF	4 KB
CONTROLSS_EPWM3_G3	0x500C 3000	0x500C 3FFF	4 KB
CONTROLSS_EPWM4_G3	0x500C 4000	0x500C 4FFF	4 KB
CONTROLSS_EPWM5_G3	0x500C 5000	0x500C 5FFF	4 KB
CONTROLSS_EPWM6_G3	0x500C 6000	0x500C 6FFF	4 KB

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Table 1-1. (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_EPWM7_G3	0x500C 7000	0x500C 7FFF	4 KB
CONTROLSS_EPWM8_G3	0x500C 8000	0x500C 8FFF	4 KB
CONTROLSS_EPWM9_G3	0x500C 9000	0x500C 9FFF	4 KB
CONTROLSS_EPWM10_G3	0x500C A000	0x500C AFFF	4 KB
CONTROLSS_EPWM11_G3	0x500C B000	0x500C BFFF	4 KB
CONTROLSS_EPWM12_G3	0x500C C000	0x500C CFFF	4 KB
CONTROLSS_EPWM13_G3	0x500C D000	0x500C DFFF	4 KB
CONTROLSS_EPWM14_G3	0x500C E000	0x500C EFFF	4 KB
CONTROLSS_EPWM15_G3	0x500C F000	0x500C FFFF	4 KB
CONTROLSS_EPWM16_G3	0x500D 0000	0x500D 0FFF	4 KB
CONTROLSS_EPWM17_G3	0x500D 1000	0x500D 1FFF	4 KB
CONTROLSS_EPWM18_G3	0x500D 2000	0x500D 2FFF	4 KB
CONTROLSS_EPWM19_G3	0x500D 3000	0x500D 3FFF	4 KB
CONTROLSS_EPWM20_G3	0x500D 4000	0x500D 4FFF	4 KB
CONTROLSS_EPWM21_G3	0x500D 5000	0x500D 5FFF	4 KB
CONTROLSS_EPWM22_G3	0x500D 6000	0x500D 6FFF	4 KB
CONTROLSS_EPWM23_G3	0x500D 7000	0x500D 7FFF	4 KB
CONTROLSS_EPWM24_G3	0x500D 8000	0x500D 8FFF	4 KB
CONTROLSS_EPWM25_G3	0x500D 9000	0x500D 9FFF	4 KB
CONTROLSS_EPWM26_G3	0x500D A000	0x500D AFFF	4 KB
CONTROLSS_EPWM27_G3	0x500D B000	0x500D BFFF	4 KB
CONTROLSS_EPWM28_G3	0x500D C000	0x500D CFFF	4 KB
CONTROLSS_EPWM29_G3	0x500D D000	0x500D DFFF	4 KB
CONTROLSS_EPWM30_G3	0x500D E000	0x500D EFFF	4 KB
CONTROLSS_EPWM31_G3	0x500D F000	0x500D FFFF	4 KB
CONTROLSS_EPWM_WLINK_G3	0x500E 0000	0x500E 0FFF	4 KB
CONTROLSS_ADC0_RESULTS	0x5010 0000	0x5010 0FFF	4 KB
CONTROLSS_ADC1_RESULTS	0x5010 1000	0x5010 1FFF	4 KB
CONTROLSS_ADC2_RESULTS	0x5010 2000	0x5010 2FFF	4 KB
CONTROLSS_ADC3_RESULTS	0x5010 3000	0x5010 3FFF	4 KB
CONTROLSS_ADC4_RESULTS	0x5010 4000	0x5010 4FFF	4 KB
CONTROLSS_CMPSSA0	0x5020 0000	0x5020 0FFF	4 KB
CONTROLSS_CMPSSA1	0x5020 1000	0x5020 1FFF	4 KB
CONTROLSS_CMPSSA2	0x5020 2000	0x5020 2FFF	4 KB
CONTROLSS_CMPSSA3	0x5020 3000	0x5020 3FFF	4 KB
CONTROLSS_CMPSSA4	0x5020 4000	0x5020 4FFF	4 KB
CONTROLSS_CMPSSA5	0x5020 5000	0x5020 5FFF	4 KB
CONTROLSS_CMPSSA6	0x5020 6000	0x5020 6FFF	4 KB
CONTROLSS_CMPSSA7	0x5020 7000	0x5020 7FFF	4 KB
CONTROLSS_CMPSSA8	0x5020 8000	0x5020 8FFF	4 KB
CONTROLSS_CMPSSA9	0x5020 9000	0x5020 9FFF	4 KB
CONTROLSS_CMPSSB0	0x5022 0000	0x5022 0FFF	4 KB
CONTROLSS_CMPSSB1	0x5022 1000	0x5022 1FFF	4 KB
CONTROLSS_CMPSSB2	0x5022 2000	0x5022 2FFF	4 KB
CONTROLSS_CMPSSB3	0x5022 3000	0x5022 3FFF	4 KB
CONTROLSS_CMPSSB4	0x5022 4000	0x5022 4FFF	4 KB
CONTROLSS_CMPSSB5	0x5022 5000	0x5022 5FFF	4 KB

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Table 1-1. (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_CMPSSB6	0x5022 6000	0x5022 6FFF	4 KB
CONTROLSS_CMPSSB7	0x5022 7000	0x5022 7FFF	4 KB
CONTROLSS_CMPSSB8	0x5022 8000	0x5022 8FFF	4 KB
CONTROLSS_CMPSSB9	0x5022 9000	0x5022 9FFF	4 KB
CONTROLSS_ECAP0	0x5024 0000	0x5024 0FFF	4 KB
CONTROLSS_ECAP1	0x5024 1000	0x5024 1FFF	4 KB
CONTROLSS_ECAP2	0x5024 2000	0x5024 2FFF	4 KB
CONTROLSS_ECAP3	0x5024 3000	0x5024 3FFF	4 KB
CONTROLSS_ECAP4	0x5024 4000	0x5024 4FFF	4 KB
CONTROLSS_ECAP5	0x5024 5000	0x5024 5FFF	4 KB
CONTROLSS_ECAP6	0x5024 6000	0x5024 6FFF	4 KB
CONTROLSS_ECAP7	0x5024 7000	0x5024 7FFF	4 KB
CONTROLSS_ECAP8	0x5024 8000	0x5024 8FFF	4 KB
CONTROLSS_ECAP9	0x5024 9000	0x5024 9FFF	4 KB
CONTROLSS_ECAP10	0x5024 A000	0x5024 AFFF	4 KB
CONTROLSS_ECAP11	0x5024 B000	0x5024 BFFF	4 KB
CONTROLSS_ECAP12	0x5024 C000	0x5024 CFFF	4 KB
CONTROLSS_ECAP13	0x5024 D000	0x5024 DFFF	4 KB
CONTROLSS_ECAP14	0x5024 E000	0x5024 EFFF	4 KB
CONTROLSS_ECAP15	0x5024 F000	0x5025 FFFF	4 KB
CONTROLSS_DAC0	0x5026 0000	0x5026 0FFF	4 KB
CONTROLSS_SDFM0	0x5026 8000	0x5026 8FFF	4 KB
CONTROLSS_SDFM1	0x5026 9000	0x5026 9FFF	4 KB
CONTROLSS_EQEP0	0x5027 0000	0x5027 0FFF	4 KB
CONTROLSS_EQEP1	0x5027 1000	0x5027 1FFF	4 KB
CONTROLSS_EQEP2	0x5027 2000	0x5027 2FFF	4 KB
CONTROLSS_FSI_TX0	0x5028 0000	0x5028 0FFF	4 KB
CONTROLSS_FSI_TX1	0x5028 1000	0x5028 1FFF	4 KB
CONTROLSS_FSI_RX0	0x5029 0000	0x5029 1FFF	4 KB
CONTROLSS_FSI_RX1	0x5029 1000	0x5029 1FFF	4 KB
CONTROLSS_FSI_TX2	0x502A 0000	0x502A 0FFF	4 KB
CONTROLSS_FSI_TX3	0x502A 1000	0x502A 1FFF	4 KB
CONTROLSS_FSI_RX2	0x502B 0000	0x502B 0FFF	4 KB
CONTROLSS_FSI_RX3	0x502B 1000	0x502B 1FFF	4 KB
CONTROLSS_ADC0_CFG	0x502C 0000	0x502C 0FFF	4 KB
CONTROLSS_ADC1_CFG	0x502C 1000	0x502C 1FFF	4 KB
CONTROLSS_ADC2_CFG	0x502C 2000	0x502C 2FFF	4 KB
CONTROLSS_ADC3_CFG	0x502C 3000	0x502C 3FFF	4 KB
CONTROLSS_ADC4_CFG	0x502C 4000	0x502C FFF	4 KB
CONTROLSS_ADCR0_CFG	0x502C 5000	0x502C 51FF	512 B
CONTROLSS_ADCR0_RESULTS	0x502C 6000	0x502C 60FF	256 B
CONTROLSS_ADCR1_CFG	0x502C 7000	0x502C 71FF	512 B
CONTROLSS_ADCR1_RESULTS	0x502C 8000	0x502C 80FF	256 B
CONTROLSS_RESOLVER0	0x502C B000	0x502C B3FF	1 KB
CONTROLSS_ADCSAFE0	0x502C B400	0x502C B8FF	1 KB
CONTROLSS_ADCSAFE1	0x502C B800	0x502C BBFF	1 KB
CONTROLSS_ADCSAFE2	0x502C BC00	0x502C BFFF	1 KB

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Table 1-1. (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_ADCSAFE3	0x502C C000	0x502C C3FF	1 KB
CONTROLSS_ADCSAFE4	0x502C C400	0x502C C7FF	1 KB
CONTROLSS_ADCSAFE5	0x502C C800	0x502C CBFF	1 KB
CONTROLSS_ADCSAFE6	0x502C CC00	0x502C CFFF	1 KB
CONTROLSS_ADCSAFE7	0x502C D000	0x502C D3FF	1 KB
CONTROLSS_ADCSAFE8	0x502C D400	0x502C D7FF	1 KB
CONTROLSS_ADCSAFE9	0x502C D800	0x502C DBFF	1 KB
CONTROLSS_ADCSAFE10	0x502C DC00	0x502C DFFF	1 KB
CONTROLSS_ADCSAFE11	0x502C E000	0x502C E3FFF	1 KB
CONTROLSS_ADC_SAFETY_AGGR	0x502C EC00	0x502C EFFF	1 KB
CONTROLSS_INPUTXBAR	0x502D 0000	0x502D 0FFF	4 KB
CONTROLSS_PWMXBAR	0x502D 1000	0x502D 1FFF	4 KB
CONTROLSS_PWMSYNCOUTXBAR	0x502D 2000	0x502D 23FF	1 KB
CONTROLSS_MDLXBAR	0x502D 3000	0x502D 37FF	2 KB
CONTROLSS_ICLXBAR	0x502D 4000	0x502D 47FF	2 KB
CONTROLSS_INTXBAR	0x502D 5000	0x502D 5FFF	4 KB
CONTROLSS_DMAXBAR	0x502D 6000	0x502D 67FF	2 KB
CONTROLSS_OUTPUTXBAR	0x502D 8000	0x502D 87FF	2 KB
CONTROLSS_OTTOCAL0	0x502E 0000	0x502E 0FFF	4 KB
CONTROLSS_OTTOCAL1	0x502E 1000	0x502E 1FFF	4 KB
CONTROLSS_OTTOCAL2	0x502E 2000	0x502E 2FFF	4 KB
CONTROLSS_OTTOCAL3	0x502E 3000	0x502E 3FFF	4 KB
CONTROLSS_GLOBAL_CTRL	0x502F 0000	0x502F 1FFF	8 KB
DEBUGSS	0x5080 0000	0x5087 FFFF	512 KB
MSS_CTRL	0x50D0 0000	0x50D1 FFFF	128 KB
TOP_CTRL	0x50D8 0000	0x50D8 1FFF	8 KB
SPINLOCK0	0x50E0 0000	0x50E0 7FFF	32 KB
VIM	0x50F0 0000	0x50F0 3FFF	16 KB
GPIO0	0x5200 0000	0x5200 00FF	256 B
GPIO1	0x5200 1000	0x5200 10FF	256 B
GPIO2	0x5200 2000	0x5200 20FF	256 B
GPIO3	0x5200 3000	0x5200 30FF	256 B
WDT0	0x5210 0000	0x5210 00FF	256 B
WDT1	0x5210 1000	0x5210 10FF	256 B
WDT2	0x5210 2000	0x5210 20FF	256 B
WDT3	0x5210 3000	0x5210 30FF	256 B
RTI0	0x5218 0000	0x5218 00FF	256 B
RTI1	0x5218 1000	0x5218 10FF	256 B
RTI2	0x5218 2000	0x5218 20FF	256 B
RTI3	0x5218 3000	0x5218 30FF	256 B
RTI4	0x5218 4000	0x5218 40FF	256 B
RTI5	0x5218 5000	0x5218 50FF	256 B
RTI6	0x5218 6000	0x5218 60FF	256 B
RTI7	0x5218 7000	0x5218 70FF	256 B
MCSPI0	0x5220 0000	0x5220 03FF	1 KB
MCSPI1	0x5220 1000	0x5220 13FF	1 KB
MCSPI2	0x5220 2000	0x5220 23FF	1 KB

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Table 1-1. (continued)

Region Name	Start Address	End Address	Size
MCSPI3	0x5220 3000	0x5220 33FF	1 KB
MCSPI4	0x5220 4000	0x5220 43FF	1 KB
MCSPI5	0x5220 5000	0x5220 53FF	1 KB
MCSPI6	0x5220 6000	0x5220 63FF	1 KB
MCSPI7	0x5220 7000	0x5220 73FF	1 KB
UART0	0x5230 0000	0x5230 01FF	512 B
UART1	0x5230 1000	0x5230 11FF	512 B
UART2	0x5230 2000	0x5230 21FF	512 B
UART3	0x5230 3000	0x5230 31FF	512 B
UART4	0x5230 4000	0x5230 41FF	512 B
UART5	0x5230 5000	0x5230 51FF	512 B
LIN0	0x5240 0000	0x5240 00FF	256 B
LIN1	0x5240 1000	0x5240 10FF	256 B
LIN2	0x5240 2000	0x5240 20FF	256 B
LIN3	0x5240 3000	0x5240 30FF	256 B
LIN4	0x5240 4000	0x5240 40FF	256 B
I2C0	0x5250 0000	0x5250 007F	128 B
I2C1	0x5250 1000	0x5250 107F	128 B
I2C2	0x5250 2000	0x5250 207F	128 B
I2C3	0x5250 3000	0x5250 307F	128 B
MCAN0_MSG_RAM	0x5260 0000	0x5260 7FFF	32 KB
MCAN0_CFG	0x5260 8000	0x5260 83FF	1 KB
MCAN1_MSG_RAM	0x5261 0000	0x5261 7FFF	32 KB
MCAN1_CFG	0x5261 8000	0x5261 83FF	1 KB
MCAN2_MSG_RAM	0x5262 0000	0x5262 7FFF	32 KB
MCAN2_CFG	0x5262 8000	0x5262 83FF	1 KB
MCAN3_MSG_RAM	0x5263 0000	0x5263 7FFF	32 KB
MCAN3_CFG	0x5263 8000	0x5263 83FF	1 KB
MCAN4_MSG_RAM	0x5264 0000	0x5264 7FFF	32 KB
MCAN4_CFG	0x5264 8000	0x5264 83FF	1 KB
MCAN5_MSG_RAM	0x5265 0000	0x5265 7FFF	32 KB
MCAN5_CFG	0x5265 8000	0x5265 83FF	1 KB
MCAN6_MSG_RAM	0x5266 0000	0x5266 7FFF	32 KB
MCAN6_CFG	0x5266 8000	0x5266 83FF	1 KB
MCAN7_MSG_RAM	0x5267 0000	0x5267 7FFF	32 KB
MCAN7_CFG	0x5267 8000	0x5267 83FF	1 KB
MCAN0_ECC	0x5270 0000	0x5270 03FF	1 KB
MCAN1_ECC	0x5270 1000	0x5270 13FF	1 KB
MCAN2_ECC	0x5270 2000	0x5270 23FF	1 KB
MCAN3_ECC	0x5270 3000	0x5270 33FF	1 KB
MCAN4_ECC	0x5270 4000	0x5270 43FF	1 KB
MCAN5_ECC	0x5270 5000	0x5270 53FF	1 KB
MCAN6_ECC	0x5270 6000	0x5270 63FF	1 KB
MCAN7_ECC	0x5270 7000	0x5270 73FF	1 KB
CPSW0	0x5280 0000	0x529FF FFFF	2 MB
EDMA_TPCC	0x52A0 0000	0x52A0 7FFF	32 KB
EDMA_TPTC0	0x52A4 0000	0x52A4 0FFF	4 KB

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Table 1-1. (continued)

Region Name	Start Address	End Address	Size
EDMA_TPTC1	0x52A6 0000	0x52A6 0FFF	4 KB
DCC0	0x52B0 0000	0x52B0 003F	64 B
DCC1	0x52B0 1000	0x52B0 103F	64 B
DCC2	0x52B0 2000	0x52B0 203F	64 B
DCC3	0x52B0 3000	0x52B0 303F	64 B
TOP_ESM	0x52D0 0000	0x52D0 0FFF	4 KB
SOC_TIMESYNC_XBAR0	0x52E0 0000	0x52E0 03FF	1 KB
EDMA_TRIG_XBAR0	0x52E0 1000	0x52E0 17FF	2 KB
GPIO_INTR_XBAR0	0x52E0 2000	0x52E0 23FF	1 KB
ICSSM_INTR_XBAR0	0x52E0 3000	0x52E0 31FF	512 B
SOC_TIMESYNC_XBAR1	0x52E0 4000	0x52E0 47FF	2 KB
ECC_AGG_R5SS0_CORE0	0x5300 0000	0x5300 03FF	1 KB
ECC_AGG_R5SS0_CORE1	0x5300 3000	0x5300 33FF	1 KB
ECC_AGG_R5SS1_CORE0	0x5300 4000	0x5300 43FF	1 KB
ECC_AGG_R5SS1_CORE1	0x5300 7000	0x5300 73FF	1 KB
ECC_AGG_TOP	0x5301 0000	0x5301 03FF	1 KB
TMU_ROM_R5SS0_CORE0	0x5302 0000	0x5302 1FFF	8 KB
TMU_ROM_R5SS0_CORE1	0x5302 4000	0x5302 5FFF	8 KB
TMU_ROM_R5SS1_CORE0	0x5302 8000	0x5302 9FFF	8 KB
TMU_ROM_R5SS1_CORE1	0x5302 C000	0x5302 DFFF	8 KB
IOMUX	0x5310 0000	0x5310 0FFF	4 KB
TOP_RCM	0x5320 0000	0x5320 0FFF	4 KB
MSS_RCM	0x5320 8000	0x5320 8FFF	4 KB
R5SS0_CCMR	0x5321 0000	0x5321 0FFF	4 KB
R5SS1_CCMR	0x5321 1000	0x5321 1FFF	4 KB
RL2_R5SS0_CORE0	0x5321 2000	0x5321 23FF	1 KB
RL2_R5SS0_CORE1	0x5321 3000	0x5321 33FF	1 KB
RL2_R5SS1_CORE0	0x5321 4000	0x5321 43FF	1 KB
RL2_R5SS1_CORE1	0x5321 5000	0x5321 53FF	1 KB
PBIST0	0x5330 0000	0x5330 01FF	512 B
FSS_TIMEOUT_CFG	0x5340 0000	0x5340 03FF	1 KB
R5SS0_STC	0x5350 0000	0x5350 01FF	512 B
R5SS1_STC	0x5351 0000	0x5351 01FF	512 B
EFUSE0	0x5360 0000	0x5360 03FF	1 KB
FSS_CFG (FLASH_CONFIG_REG0)	0x5380 0000	0x5380 00FF	256 B
FSAS_CFG (FLASH_CONFIG_REG1)	0x5380 1000	0x5380 10FF	256 B
FSAS_OTFA_CFG (FLASH_CONFIG_REG2)	0x5380 2000	0x5380 2FFF	4 KB
OSPI_CFG (FLASH_CONFIG_REG6)	0x5380 6000	0x5380 61FF	512 B
OSPI0_ECC_AGG (FLASH_CONFIG_REG7)	0x5380 7000	0x5380 73FF	1 KB
OSPI0_FLASH_APB (FLASH_CONFIG_REG8)	0x5380 8000	0x5380 80FF	256 B
FOTA_MMR_CFG (FLASH_CONFIG_REG11)	0x5380 B000	0x5380 B0FF	256 B
FOTA_PDMEM_CFG (FLASH_CONFIG_REG12)	0x5380 C000	0x5380 C7FF	2 KB
FOTA_IMEM_CFG (FLASH_CONFIG_REG13)	0x5380 D000	0x5380 D0FF	256 B
FOTA_WBUF_CFG (FLASH_CONFIG_REG14)	0x5380 E000	0x5380 E1FF	512 B
FSAS_ECC_AGGR (FLASH_CONFIG_REG15)	0x5380 F000	0x5380 F3FF	1 KB
FSS_DATA_REG0	0x6000 0000	0x67FF FFFF	128 MB
L2OCRAM_BANK0	0x7000 0000	0x7007 FFFF	512 KB

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Table 1-1. (continued)

Region Name	Start Address	End Address	Size
L2OCRAM_BANK1	0x7008 0000	0x700F FFFF	512 KB
L2OCRAM_BANK2	0x7010 0000	0x7017 FFFF	512 KB
L2OCRAM_BANK3	0x7018 0000	0x701F FFFF	512 KB
L2OCRAM_BANK4	0x7020 0000	0x7027 FFFF	512 KB
L2OCRAM_BANK5	0x7028 0000	0x702F FFFF	512 KB
MBOX_SRAM	0x7200 0000	0x7200 3FFF	16 KB
R5SS0_CORE0_ICACHE [4]	0x7400 0000	0x747F FFFF	16 KB (8 MB) [5]
R5SS0_CORE0_DCACHE [4]	0x7480 0000	0x74FF FFFF	16 KB (8 MB) [5]
R5SS0_CORE1_ICACHE [2,4]	0x7500 0000	0x757F FFFF	16 KB (8 MB) [5]
R5SS0_CORE1_DCACHE [2,4]	0x7580 0000	0x75FF FFFF	16 KB (8 MB) [5]
R5SS1_CORE0_ICACHE [4]	0x7600 0000	0x767F FFFF	16 KB (8 MB) [5]
R5SS1_CORE0_DCACHE [4]	0x7680 0000	0x76FF FFFF	16 KB (8 MB) [5]
R5SS1_CORE1_ICACHE [2,4]	0x7700 0000	0x777F FFFF	16 KB (8 MB) [5]
R5SS1_CORE1_DCACHE [2,4]	0x7780 0000	0x77FF FFFF	16 KB (8 MB) [5]
R5SS0_CORE0_TCMA [3,4]	0x7800 0000	0x7800 7FFF	32 KB
R5SS0_CORE0_TMU_EXT	0x7806 0000	0x7806 03FF	1 KB
R5SS0_CORE0_TCMB [3,4]	0x7810 0000	0x7811 7FFF	96 KB
R5SS0_CORE1_TCMA [2,4]	0x7820 0000	0x7820 7FFF	32 KB
R5SS0_CORE1_TMU_EXT	0x7826 0000	0x7826 03FFF	1 KB
R5SS0_CORE1_TCMB [2,4]	0x7830 0000	0x7831 7FFF	96 KB
R5SS1_CORE0_TCMA [3,4]	0x7840 0000	0x7840 7FFF	32 KB
R5SS1_CORE0_TMU_EXT	0x7846 0000	0x7846 03FF	1 KB
R5SS1_CORE0_TCMB [3,4]	0x7850 0000	0x7851 7FFF	96 KB
R5SS1_CORE1_TCMA [2,4]	0x7860 0000	0x7860 7FFF	32 KB
R5SS1_CORE1_TMU_EXT	0x7866 0000	0x7866 03FF	1 KB
R5SS1_CORE1_TCMB [2,4]	0x7870 0000	0x7871 7FFF	96 KB
FSS_DATA_REG1	0x8000 0000	0x87FF FFFF	128 MB
FSS_DATA_REG3	0x8800 0000	0x88FF FFFF	128 MB

1. See core-specific tables for the internal memory map.
2. In Lockstep mode, the R5FSS*x*_CORE**1** memory region is not accessible.
3. The size of these memories changes based on Dual-Core vs Lockstep operation.
   For more information about Dual-Core and Lockstep modes, see the *R5FSS* chapter.
   For more information about ATCM and BTCM, see the *Tightly-Coupled Memories (TCM)* section within the *R5FSS* chapter.
4. This memory region is used by each CPU core to access the TCM/Cache memory space of other CPU cores.
5. Each R5FSS contains 16 KB i-cache and 16 KB d-cache. However, the system interconnect sees an 8 MB address range at ICACHE/DCACHE. Any core attempting to access more than 16 KB results in a wrap around and accessing the same cache multiple times.

1.2 R5FSS Memory Map

Table 1-2. R5FSS0-0 Memory Map

Region Name	Start Address	End Address	Size
Before ROM to RAM Swap			
R5SS0_CORE0_TCMA_ROM	0x0000 0000	0x0001 FFFF	128 KB
R5SS0_CORE0_TCMA_RAM	0x0002 0000	0x0002 FFFF (Lockstep)	64 KB (Lockstep)
		0x0002 7FFF (Dual Core)	32 KB (Dual Core)

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Table 1-2. R5FSS0-0 Memory Map (continued)

Region Name	Start Address	End Address	Size
R5SS0_CORE0_TMU	0x0006 0000	0x0006 03FF	1 KB
R5SS0_CORE0_TCMB_RAM	0x0008 0000	0x000A FFFF (Lockstep)	192 KB (Lockstep)
		0x0009 7FFF (Dual Core)	96 KB (Dual Core)
R5SS0_CORE0_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS0_CORE0_WWDT (WDT0)	0x5210 0000	0x5210 00FF	256 Bytes
After ROM to RAM Swap			
R5SS0_CORE0_TCMA_ROM	NA	NA	NA
R5SS0_CORE0_TCMA_RAM	0x0000 0000	0x0000 FFFF (Lockstep)	64 KB (Lockstep)
		0x0000 7FFF (Dual Core)	32 KB (Dual Core)
R5SS0_CORE0_TMU	0x0006 0000	0x0006 03FF	1 KB
R5SS0_CORE0_TCMB_RAM	0x0008 0000	0x000A FFFF (Lockstep)	192 KB (Lockstep)
		0x0009 7FFF (Dual Core)	96 KB (Dual Core)
R5SS0_CORE0_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS0_CORE0_WWDT (WDT0)	0x5210 0000	0x5210 00FF	256 Bytes

Table 1-3. R5FSS0-1 Memory Map

Region Name	Start Address	End Address	Size
R5SS0_CORE1_TCMA_RAM	0x0000 0000	0x0000 7FFF	32 KB
R5SS0_CORE1_TCMB_RAM	0x0008 0000	0x0009 7FFF	96 KB
R5SS0_CORE1_TMU	0x0006 0000	0x0006 03FF	1 KB
R5SS0_CORE1_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS0_CORE1_WWDT (WDT1)	0x5210 1000	0x5210 10FF	256 Bytes

Table 1-4. R5FSS1-0 Memory Map

Region Name	Start Address	End Address	Size
R5SS1_CORE0_TCMA_RAM	0x0000 0000	0x0000 FFFF (Lockstep)	64 KB (Lockstep)
		0x0000 7FFF (Dual Core)	32 KB (Dual Core)
R5SS1_CORE0_TMU	0x0006 0000	0x0006 03FF	1 KB
R5SS1_CORE0_TCMB_RAM	0x0008 0000	0x000A FFFF (Lockstep)	192 KB (Lockstep)
		0x0009 7FFF (Dual Core)	96 KB (Dual Core)
R5SS1_CORE0_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS1_CORE0_WWDT (WDT2)	0x5210 2000	0x5210 20FF	256 Bytes

Table 1-5. R5FSS1-1 Memory Map

Region Name	Start Address	End Address	Size
R5SS1_CORE1_TCMA_RAM	0x0000 0000	0x0000 7FFF	32 KB
R5SS1_CORE1_TMU	0x0006 0000	0x0006 03FF	1 KB
R5SS1_CORE1_TCMB_RAM	0x0008 0000	0x0009 7FFF	96 KB
R5SS1_CORE1_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS1_CORE1_WWDT (WDT3)	0x5210 3000	0x5210 30FF	256 Bytes

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1.3 PRU-ICSS Memory Map

Region Name	Start Address	End Address	Size
PRU-ICSS Data RAM0 (DRAM0)	0x0000 0000	0x0000 1FFF	8 KB
PRU-ICSS Data RAM1 (DRAM1)	0x0000 2000	0x0000 3FFF	8 KB
PRU-ICSS Data RAM2 (Shared DRAM2)	0x0001 0000	0x0001 FFFF	64 KB
PRU-ICSS INTC	0x0002 0000	0x0002 1FFF	8 KB
PRU-ICSS PRU0 Control	0x0002 2000	0x0002 23FF	1 KB
PRU-ICSS PRU0 Debug	0x0002 2400	0x0002 3FFF	7 KB
PRU-ICSS PRU1 Control	0x0002 4000	0x0002 43FF	1 KB
PRU-ICSS PRU1 Debug	0x0002 4400	0x0002 5FFF	7 KB
PRU-ICSS CFG	0x0002 6000	0x0002 6FFF	4 KB
PRU-ICSS ECC_CFG	0x0002 7000	0x0002 7FFF	4 KB
PRU-ICSS UART0	0x0002 8000	0x0002 9FFF	8 KB
PRU-ICSS Reserved	0x0002 A000	0x0002 BFFF	8 KB
PRU-ICSS Reserved	0x0002 C000	0x0002 DFFF	8 KB
PRU-ICSS IEP	0x0002 E000	0x0002 EFFF	8 KB
PRU-ICSS ECAP0	0x0003 0000	0x0003 1FFF	8 KB
PRU-ICSS MII_RT_CFG	0x0003 2000	0x0003 23FF	1 KB
PRU-ICSS MII_MDIO	0x0003 2400	0x0003 3FFF	7 KB
PRU-ICSS PRU0 IRAM	0x0003 4000	0x0003 7FFF	16 KB
PRU-ICSS PRU1 IRAM	0x0003 8000	0x0003 BFFF	16 KB

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2 Control Module (CTRLMMR) Registers

The Control module is the main controller for top-level device behavior in various states. Module contains registers for configuration, bootstrap (SOP) signals, I/O terminal pad multiplexing, clock selection, and many others. There are various Control or (CTRLMMR) modules defined in this device:

General SoC Control Modules

- *TOP_CTRL Registers* (CTRLMMR0): SoC-level configuration registers
- *MSS_CTRL Registers* (CTRLMMR1): SoC and Peripheral-level configuration registers
- *CONTROLSS_GLOBAL_CTRL Registers* (CTRLMMR2): CONTROLSS-level configuration registers including general control, reset, and clocking-related functions for the real time control subsystem (CONTROLSS))

Pad Configuration Control Modules

- *MSS_IOMUX Registers* (PADCFG_CTRLMMR0): SoC-level terminal configuration control registers

Reset and Clocking Control Modules

- *MSS_TOPRCM Registers* (RCM_CTRLMMR0): SoC-level Clock and Reset control registers
- *MSS_RCM Registers* (RCM_CTRLMMR1): SoC and Peripheral-level Clock and Reset control registers

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2.1 LOCK_KICK Protection Register Unlock Values

All Control Module MMR have a protection mechanism which prevents spurious writes from changing register values. LOCK0_KICK0 and LOCK0_KICK1 registers are used for this purpose. The sequence to unlock these MMR is as follows:

1. Write exact unlock value (Table 2-1) to <Control Module>LOCK0_KICK0:KEY field
2. Write exact unlock value (Table 2-1) to <Control Module>LOCK0_KICK1:KEY field

The sequence to lock the MMR is as follows:

1. Write zero (or another value other than the unlock value) (Table 2-1) to <Control Module>LOCK0_KICK1:KEY field
2. Write zero (or another value other than the unlock value) (Table 2-1) to <Control Module>LOCK0_KICK0:KEY field

- **Note**

  If the above sequence for locking the IOMUX is not followed, an AHB_WRITE_ERROR interrupt will occur (if enabled).

For example, to unlock Control Module MSS_CTRL the sequence is as below:
1. Write 0x01234567 to MSS_CTRL.LOCK0_KICK0:KEY
2. Write 0xFEDCBA8 to MSS_CTRL.LOCK0_KICK1:KEY

To lock the Control Module MSS_CTRL the sequence is as below:
1. Write 0x0 to MSS_CTRL.LOCK0_KICK1:KEY
2. Write 0x0 to MSS_CTRL.LOCK0_KICK0:KEY

Any writes to locked memory region will result in assertion of the MMR_ACCESS_ERR_WR event by the respective control modules. This assertion can be enabled or disabled by writing the appropriate value to <Control Module>.INTR_ENABLE.KICK_ERR_EN field.

The table below shows the values that must be written to the LOCK0_KICK0 and LOCK0_KICK1 registers to unlock the various Control modules' MMR.

Table 2-1. Kick Protection Register Unlock Values

Protected Register	LockKick Register	Unlock Value
TOP_CTRL	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
MSS_CTRL	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
CONTROLSS_CTRL	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
TOP_RCM	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
MSS_RCM	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
IOMUX	LOCK0_KICK0	0x83E70B13
	LOCK0_KICK1	0x95A4F1E0

Note

To ensure that all registers from a given partition are write protected, software must always re-lock the protection mechanism after completing the register writes.

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The kick protection registers described in this section are an exception and are not write protected by the protection mechanism.

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2.2 TOP_CTRL

TOP_CTRL

2.2.1 TOP_CTRL Summaries

TOP_CTRL Summaries

Table 2-2. TOP_CTRL Registers, Base Address=50D8 0000h, Length=4096

Offset	Length	Register Name	TOP_CTRL Physical Address
10h	32	TOP_CTRL_EFUSE_DIEID0	50D8 0010h
14h	32	TOP_CTRL_EFUSE_DIEID1	50D8 0014h
18h	32	TOP_CTRL_EFUSE_DIEID2	50D8 0018h
1Ch	32	TOP_CTRL_EFUSE_DIEID3	50D8 001Ch
20h	32	TOP_CTRL_EFUSE_UID0	50D8 0020h
24h	32	TOP_CTRL_EFUSE_UID1	50D8 0024h
28h	32	TOP_CTRL_EFUSE_UID2	50D8 0028h
2Ch	32	TOP_CTRL_EFUSE_UID3	50D8 002Ch
30h	32	TOP_CTRL_EFUSE_DEVICE_TYPE	50D8 0030h
34h	32	TOP_CTRL_EFUSE_FROM0_CHECKSUM	50D8 0034h
38h	32	TOP_CTRL_EFUSE_JTAG_USERCODE_ID	50D8 0038h
428h	32	TOP_CTRL_EFUSE1_ROW_12	50D8 0428h
500h	32	TOP_CTRL_MAC_ID0	50D8 0500h
504h	32	TOP_CTRL_MAC_ID1	50D8 0504h
880h	32	TOP_CTRL_EFUSE_OVERRIDE_LDO_TRIM	50D8 0880h
C00h	32	TOP_CTRL_ADC_REFBUF0_CTRL	50D8 0C00h
C04h	32	TOP_CTRL_ADC_REFBUF1_CTRL	50D8 0C04h
C08h	32	TOP_CTRL_ADC_REF_COMP_CTRL	50D8 0C08h
C0Ch	32	TOP_CTRL_ADC_REF_GOOD_STATUS	50D8 0C0Ch
C10h	32	TOP_CTRL_VMON_CTRL	50D8 0C10h
C14h	32	TOP_CTRL_VMON_STAT	50D8 0C14h
C18h	32	TOP_CTRL_PMU_COARSE_STAT	50D8 0C18h
C20h	32	TOP_CTRL_MASK_VMON_ERROR_ESM_H	50D8 0C20h
C24h	32	TOP_CTRL_MASK_VMON_ERROR_ESM_L	50D8 0C24h
C30h	32	TOP_CTRL_MASK_ANA_ISO	50D8 0C30h
C34h	32	TOP_CTRL_VMON_FILTER_CTRL	50D8 0C34h
C40h	32	TOP_CTRL_ADC_RNG_CTRL	50D8 0C40h
C44h	32	TOP_CTRL_ADC0_OSD_CHEN	50D8 0C44h
C48h	32	TOP_CTRL_ADC1_OSD_CHEN	50D8 0C48h
C4Ch	32	TOP_CTRL_ADC2_OSD_CHEN	50D8 0C4Ch
C50h	32	TOP_CTRL_ADC3_OSD_CHEN	50D8 0C50h
C54h	32	TOP_CTRL_ADC4_OSD_CHEN	50D8 0C54h
C58h	32	TOP_CTRL_ADC0_OSD_CTRL	50D8 0C58h
C5Ch	32	TOP_CTRL_ADC1_OSD_CTRL	50D8 0C5Ch
C60h	32	TOP_CTRL_ADC2_OSD_CTRL	50D8 0C60h
C64h	32	TOP_CTRL_ADC3_OSD_CTRL	50D8 0C64h
C68h	32	TOP_CTRL_ADC4_OSD_CTRL	50D8 0C68h
C80h	32	TOP_CTRL_ADC_LOOPBACK_CTRL	50D8 0C80h
C84h	32	TOP_CTRL_CMPSSA_LOOPBACK_CTRL	50D8 0C84h
C88h	32	TOP_CTRL_CMPSSB_LOOPBACK_CTRL	50D8 0C88h

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Table 2-2. TOP_CTRL Registers, Base Address=50D8 0000h, Length=4096 (continued)

Offset	Length	Register Name	TOP_CTRL Physical Address
C8Ch	32	TOP_CTRL_ADCR01_OSD_CHEN	50D8 0C8Ch
C90h	32	TOP_CTRL_ADCR01_OSD_CTRL	50D8 0C90h
C94h	32	TOP_CTRL_ADC_REFBUF2_CTRL	50D8 0C94h
D00h	32	TOP_CTRL_TSENSE_CFG	50D8 0D00h
D04h	32	TOP_CTRL_TSENSE_STATUS	50D8 0D04h
D08h	32	TOP_CTRL_TSENSE_STATUS_RAW	50D8 0D08h
D14h	32	TOP_CTRL_TSENSE0_ALERT	50D8 0D14h
D18h	32	TOP_CTRL_TSENSE0_CNTL	50D8 0D18h
D1Ch	32	TOP_CTRL_TSENSE0_RESULT	50D8 0D1Ch
D20h	32	TOP_CTRL_TSENSE0_DATA0	50D8 0D20h
D24h	32	TOP_CTRL_TSENSE0_DATA1	50D8 0D24h
D28h	32	TOP_CTRL_TSENSE0_DATA2	50D8 0D28h
D2Ch	32	TOP_CTRL_TSENSE0_DATA3	50D8 0D2Ch
D30h	32	TOP_CTRL_TSENSE0_ACCU	50D8 0D30h
D40h	32	TOP_CTRL_TSENSE1_TSHUT	50D8 0D40h
D44h	32	TOP_CTRL_TSENSE1_ALERT	50D8 0D44h
D48h	32	TOP_CTRL_TSENSE1_CNTL	50D8 0D48h
D4Ch	32	TOP_CTRL_TSENSE1_RESULT	50D8 0D4Ch
D50h	32	TOP_CTRL_TSENSE1_DATA0	50D8 0D50h
D54h	32	TOP_CTRL_TSENSE1_DATA1	50D8 0D54h
D58h	32	TOP_CTRL_TSENSE1_DATA2	50D8 0D58h
D5Ch	32	TOP_CTRL_TSENSE1_DATA3	50D8 0D5Ch
D60h	32	TOP_CTRL_TSENSE1_ACCU	50D8 0D60h
D7Ch	32	TOP_CTRL_TSENSE2_RESULT	50D8 0D7Ch
DACh	32	TOP_CTRL_TSENSE3_RESULT	50D8 0DACh
FD0h	32	TOP_CTRL_HW_SPARE_RW0	50D8 0FD0h
FD4h	32	TOP_CTRL_HW_SPARE_RW1	50D8 0FD4h
FD8h	32	TOP_CTRL_HW_SPARE_RW2	50D8 0FD8h
FDCh	32	TOP_CTRL_HW_SPARE_RW3	50D8 0FDCh
FE0h	32	TOP_CTRL_HW_SPARE_RO0	50D8 0FE0h
FE4h	32	TOP_CTRL_HW_SPARE_RO1	50D8 0FE4h
FE8h	32	TOP_CTRL_HW_SPARE_RO2	50D8 0FE8h
FECh	32	TOP_CTRL_HW_SPARE_RO3	50D8 0FECh
FF0h	32	TOP_CTRL_HW_SPARE_WPH	50D8 0FF0h
FF4h	32	TOP_CTRL_HW_SPARE_REC	50D8 0FF4h
1008h	32	TOP_CTRL_LOCK0_KICK0	50D8 1008h
100Ch	32	TOP_CTRL_LOCK0_KICK1	50D8 100Ch
1010h	32	TOP_CTRL_INTR_RAW_STATUS	50D8 1010h
1014h	32	TOP_CTRL_INTR_ENABLED_STATUS_CLEAR	50D8 1014h
1018h	32	TOP_CTRL_INTR_ENABLE	50D8 1018h
101Ch	32	TOP_CTRL_INTR_ENABLE_CLEAR	50D8 101Ch
1020h	32	TOP_CTRL_EOI	50D8 1020h
1024h	32	TOP_CTRL_FAULT_ADDRESS	50D8 1024h
1028h	32	TOP_CTRL_FAULT_TYPE_STATUS	50D8 1028h
102Ch	32	TOP_CTRL_FAULT_ATTR_STATUS	50D8 102Ch
1030h	32	TOP_CTRL_FAULT_CLEAR	50D8 1030h

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2.2.2 TOP_CTRL Registers

TOP_CTRL Registers

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2.2.2.1 TOP_CTRL_EFUSE_DIEID0 Register

2.2.2.1.1 TOP_CTRL_EFUSE_DIEID0 Register (Offset = 10h) [reset = 0h]

EFUSE_DIEID0.

Return to Summary Table

Table 2-3. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0010h

Figure 2-1. TOP_CTRL_EFUSE_DIEID0 Name Register

31	30	29	28	27	26	25	24
EFUSE_DIEID0_VAL							
R							
0h							
23	22	21	20	19	18	17	16
EFUSE_DIEID0_VAL							
R							
0h							
15	14	13	12	11	10	9	8
EFUSE_DIEID0_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_DIEID0_VAL							
R							
0h							

Table 2-4. TOP_CTRL_EFUSE_DIEID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_DIEID0_VAL	R	0h	EFUSE DieID[31:0]

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2.2.2.2 TOP_CTRL_EFUSE_DIEID1 Register

2.2.2.2.1 TOP_CTRL_EFUSE_DIEID1 Register (Offset = 14h) [reset = 0h]

EFUSE_DIEID1.

Return to Summary Table

Table 2-5. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0014h

Figure 2-2. TOP_CTRL_EFUSE_DIEID1 Name Register

31	30	29	28	27	26	25	24
EFUSE_DIEID1_VAL							
R							
0h							
23	22	21	20	19	18	17	16
EFUSE_DIEID1_VAL							
R							
0h							
15	14	13	12	11	10	9	8
EFUSE_DIEID1_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_DIEID1_VAL							
R							
0h							

Table 2-6. TOP_CTRL_EFUSE_DIEID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_DIEID1_VAL	R	0h	EFUSE DieID[63:32]

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2.2.2.3 TOP_CTRL_EFUSE_DIEID2 Register

2.2.2.3.1 TOP_CTRL_EFUSE_DIEID2 Register (Offset = 18h) [reset = 0h]

EFUSE_DIEID2.

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Table 2-7. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0018h

Figure 2-3. TOP_CTRL_EFUSE_DIEID2 Name Register

31	30	29	28	27	26	25	24
EFUSE_DIEID2_VAL							
R							
0h							
23	22	21	20	19	18	17	16
EFUSE_DIEID2_VAL							
R							
0h							
15	14	13	12	11	10	9	8
EFUSE_DIEID2_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_DIEID2_VAL							
R							
0h							

Table 2-8. TOP_CTRL_EFUSE_DIEID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_DIEID2_VAL	R	0h	EFUSE DieID[95:64]

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2.2.2.4 TOP_CTRL_EFUSE_DIEID3 Register

2.2.2.4.1 TOP_CTRL_EFUSE_DIEID3 Register (Offset = 1Ch) [reset = 0h]

EFUSE_DIEID3.

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Table 2-9. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 001Ch

Figure 2-4. TOP_CTRL_EFUSE_DIEID3 Name Register

31	30	29	28	27	26	25	24
EFUSE_DIEID3_VAL							
R							
0h							
23	22	21	20	19	18	17	16
EFUSE_DIEID3_VAL							
R							
0h							
15	14	13	12	11	10	9	8
EFUSE_DIEID3_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_DIEID3_VAL							
R							
0h							

Table 2-10. TOP_CTRL_EFUSE_DIEID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_DIEID3_VAL	R	0h	EFUSE DieID[127:96]

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2.2.2.5 TOP_CTRL_EFUSE_UID0 Register

2.2.2.5.1 TOP_CTRL_EFUSE_UID0 Register (Offset = 20h) [reset = 0h]

EFUSE_UID0.

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Table 2-11. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0020h

Figure 2-5. TOP_CTRL_EFUSE_UID0 Name Register

31	30	29	28	27	26	25	24
EFUSE_UID0_VAL							
R							
0h							
23	22	21	20	19	18	17	16
EFUSE_UID0_VAL							
R							
0h							
15	14	13	12	11	10	9	8
EFUSE_UID0_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_UID0_VAL							
R							
0h							

Table 2-12. TOP_CTRL_EFUSE_UID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_UID0_VAL	R	0h	EFUSE UID[31:0]- Unique ID

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2.2.2.6 TOP_CTRL_EFUSE_UID1 Register

2.2.2.6.1 TOP_CTRL_EFUSE_UID1 Register (Offset = 24h) [reset = 0h]

EFUSE_UID1.

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Table 2-13. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0024h

Figure 2-6. TOP_CTRL_EFUSE_UID1 Name Register

31	30	29	28	27	26	25	24
EFUSE_UID1_VAL							
R							
0h							
23	22	21	20	19	18	17	16
EFUSE_UID1_VAL							
R							
0h							
15	14	13	12	11	10	9	8
EFUSE_UID1_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_UID1_VAL							
R							
0h							

Table 2-14. TOP_CTRL_EFUSE_UID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_UID1_VAL	R	0h	EFUSE UID[63:32]- Unique ID

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2.2.2.7 TOP_CTRL_EFUSE_UID2 Register

2.2.2.7.1 TOP_CTRL_EFUSE_UID2 Register (Offset = 28h) [reset = 0h]

EFUSE_UID2.

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Table 2-15. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0028h

Figure 2-7. TOP_CTRL_EFUSE_UID2 Name Register

31	30	29	28	27	26	25	24
EFUSE_UID2_VAL							
R							
0h							
23	22	21	20	19	18	17	16
EFUSE_UID2_VAL							
R							
0h							
15	14	13	12	11	10	9	8
EFUSE_UID2_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_UID2_VAL							
R							
0h							

Table 2-16. TOP_CTRL_EFUSE_UID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_UID2_VAL	R	0h	EFUSE UID[95:64]- Unique ID

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2.2.2.8 TOP_CTRL_EFUSE_UID3 Register

2.2.2.8.1 TOP_CTRL_EFUSE_UID3 Register (Offset = 2Ch) [reset = 0h]

EFUSE_UID3.

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Table 2-17. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 002Ch

Figure 2-8. TOP_CTRL_EFUSE_UID3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
EFUSE_UID3_VAL							
R							
0h							
15	14	13	12	11	10	9	8
EFUSE_UID3_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_UID3_VAL							
R							
0h							

Table 2-18. TOP_CTRL_EFUSE_UID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	EFUSE_UID3_VAL	R	0h	EFUSE UID[120:96]- Unique ID

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2.2.2.9 TOP_CTRL_EFUSE_DEVICE_TYPE Register

2.2.2.9.1 TOP_CTRL_EFUSE_DEVICE_TYPE Register (Offset = 30h) [reset = 0h]

EFUSE_DEVICE_TYPE.

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Table 2-19. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0030h

Figure 2-9. TOP_CTRL_EFUSE_DEVICE_TYPE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EFUSE_DEVICE_TYPE_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_DEVICE_TYPE_VAL							
R							
0h							

Table 2-20. TOP_CTRL_EFUSE_DEVICE_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EFUSE_DEVICE_TYPE_VAL	R	0h	EFUSE Device Type : 0x5 - Test Device 0x3 - General Purpose Device 0x9 - EMU Device 0xA - High Secure

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2.2.2.10 TOP_CTRL_EFUSE_FROM0_CHECKSUM Register

2.2.2.10.1 TOP_CTRL_EFUSE_FROM0_CHECKSUM Register (Offset = 34h) [reset = 0h]

EFUSE_FROM0_CHECKSUM.

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Table 2-21. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0034h

Figure 2-10. TOP_CTRL_EFUSE_FROM0_CHECKSUM Name Register

31	30	29	28	27	26	25	24
EFUSE_FROM0_CHECKSUM_VAL							
R							
0h							
23	22	21	20	19	18	17	16
EFUSE_FROM0_CHECKSUM_VAL							
R							
0h							
15	14	13	12	11	10	9	8
EFUSE_FROM0_CHECKSUM_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_FROM0_CHECKSUM_VAL							
R							
0h							

Table 2-22. TOP_CTRL_EFUSE_FROM0_CHECKSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_FROM0_CHECKSUM_VAL	R	0h	32 bit FROM0 Checksum

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2.2.2.11 TOP_CTRL_EFUSE_JTAG_USERCODE_ID Register

2.2.2.11.1 TOP_CTRL_EFUSE_JTAG_USERCODE_ID Register (Offset = 38h) [reset = 0h]

EFUSE_JTAG_USERCODE_ID.

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Table 2-23. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0038h

Figure 2-11. TOP_CTRL_EFUSE_JTAG_USERCODE_ID Name Register

31	30	29	28	27	26	25	24
EFUSE_JTAG_USERCODE_ID_VAL							
R							
0h							
23	22	21	20	19	18	17	16
EFUSE_JTAG_USERCODE_ID_VAL							
R							
0h							
15	14	13	12	11	10	9	8
EFUSE_JTAG_USERCODE_ID_VAL							
R							
0h							
7	6	5	4	3	2	1	0
EFUSE_JTAG_USERCODE_ID_VAL							
R							
0h							

Table 2-24. TOP_CTRL_EFUSE_JTAG_USERCODE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EFUSE_JTAG_USERCODE_ID_VAL	R	0h	EFUSE JTAG_USER_CODE_ID[31:0]. Denotes part variant

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2.2.2.12 TOP_CTRL_EFUSE1_ROW_12 Register

2.2.2.12.1 TOP_CTRL_EFUSE1_ROW_12 Register (Offset = 428h) [reset = 0h]

EFUSE Row.

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Table 2-25. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0428h

Figure 2-12. TOP_CTRL_EFUSE1_ROW_12 Name Register

31	30	29	28	27	26	25	24
RESERVED							EFUSE1_ROW_12_EPWM_FEATURE_DISABLE
NONE							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EFUSE1_ROW_12_CANFD_DIS				EFUSE1_ROW_12_PRU_ICSS_HW_DIS			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EFUSE1_ROW_12_PRU_ICSS_HW_DIS				EFUSE1_ROW_12_PRU_ICSS_DIS	EFUSE1_ROW_12_TWOX_CTRL_PERIP_DISABLE	EFUSE1_ROW_12_R5SS_FREQ	EFUSE1_ROW_12_R5SS1_DISABLE
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EFUSE1_ROW_12_R5SS1_DUAL_CORE_DISABLE	EFUSE1_ROW_12_R5SS1_FORCE_DUAL_CORE	EFUSE1_ROW_12_R5SS0_DUAL_CORE_DISABLE	EFUSE1_ROW_12_R5SS0_FORCE_DUAL_CORE	EFUSE1_ROW_12_L2_MEM_SIZE			
R	R	R	R	R			
0h	0h	0h	0h	0h			

Table 2-26. TOP_CTRL_EFUSE1_ROW_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	EFUSE1_ROW_12_EPWM_FEATURE_DISABLE	R	0h	Customer protected features inside PWM IP 1'b0 - All features enabled 1'b1 - Customer defined features are protected
23:20	EFUSE1_ROW_12_CANFD_DIS	R	0h	CANFD disables. Bit positions correspond to CAN instance. 1'b0 - CAN is enabled 1'b1 - CAN is disabled
19:12	EFUSE1_ROW_12_PRU_ICSS_HW_DIS	R	0h	ICSSM IP feature configuration 0x00:EtherCAT is available 0x03:EtherCAT is disabled
11	EFUSE1_ROW_12_PRU_ICSS_DIS	R	0h	ICSSM IP disable 1'b0 - ICSSM enabled 1'b1 - ICSSM disabled

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Table 2-26. TOP_CTRL_EFUSE1_ROW_12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	EFUSE1_ROW_12_TWOX_CTRL_PERIP_DISABLE	R	0h	2x control IPs enabled 1'b0 - 1x control IPs available (Standard Analog Configuration) 1'b1 - (i.e.all) 2x control IPs available (Enhanced Analog Configuration) Refer to device datasheet for more details on the control IP Counts
9	EFUSE1_ROW_12_R5SS_FREQ	R	0h	R5SS Freq 1'b0 - 400 MHz 1'b1 - 200 MHz
8	EFUSE1_ROW_12_R5SS1_DISABLE	R	0h	R5SS1 Disabled
7	EFUSE1_ROW_12_R5SS1_DUAL_CORE_DISABLE	R	0h	Force Lock step
6	EFUSE1_ROW_12_R5SS1_FORCE_DUAL_CORE	R	0h	Force Dual core
5	EFUSE1_ROW_12_R5SS0_DUAL_CORE_DISABLE	R	0h	Force Lock step
4	EFUSE1_ROW_12_R5SS0_FORCE_DUAL_CORE	R	0h	Force Dual core
3:0	EFUSE1_ROW_12_L2_MEM_SIZE	R	0h	Decides memory size 0000L2-3.0 MB 0001L2-2.5 MB 0010L2-2.0 MB 0011L2-1.5 MB 0100L2-1.0 MB 0101L2-0.5 MB Others-Reserved

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2.2.2.13 TOP_CTRL_MAC_ID0 Register

2.2.2.13.1 TOP_CTRL_MAC_ID0 Register (Offset = 500h) [reset = 0h]

Ethernet MAC address lower 32-bits.

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Table 2-27. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0500h

Figure 2-13. TOP_CTRL_MAC_ID0 Name Register

31	30	29	28	27	26	25	24
MAC_ID0_MACID_LO							
R							
0h							
23	22	21	20	19	18	17	16
MAC_ID0_MACID_LO							
R							
0h							
15	14	13	12	11	10	9	8
MAC_ID0_MACID_LO							
R							
0h							
7	6	5	4	3	2	1	0
MAC_ID0_MACID_LO							
R							
0h							

Table 2-28. TOP_CTRL_MAC_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAC_ID0_MACID_LO	R	0h	48-bit Ethernet MAC_ID field [can be used by SW through MMR read] - MAC ID low [32bits]

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2.2.2.14 TOP_CTRL_MAC_ID1 Register

2.2.2.14.1 TOP_CTRL_MAC_ID1 Register (Offset = 504h) [reset = 0h]

Ethernet MAC address upper 16-bits.

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Table 2-29. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0504h

Figure 2-14. TOP_CTRL_MAC_ID1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ID1_MACID_HI							
R							
0h							
7	6	5	4	3	2	1	0
MAC_ID1_MACID_HI							
R							
0h							

Table 2-30. TOP_CTRL_MAC_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAC_ID1_MACID_HI	R	0h	48-bit Ethernet MAC_ID field [can be used by SW through MMR read] - MAC ID high [16bits]

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2.2.2.15 TOP_CTRL_EFUSE_OVERRIDE_LDO_TRIM Register

2.2.2.15.1 TOP_CTRL_EFUSE_OVERRIDE_LDO_TRIM Register (Offset = 880h) [reset = 0h]

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Table 2-31. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0880h

Figure 2-15. TOP_CTRL_EFUSE_OVERRIDE_LDO_TRIM Name Register

31	30	29	28	27	26	25	24
RESERVED		EFUSE_OVERRIDE_LDO_TRIM_LDO_TRIM_OFFSET					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				EFUSE_OVERRIDE_LDO_TRIM_LDO_PROG			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EFUSE_OVERRIDE_LDO_TRIM_OVERRIDE		
NONE					R/W		
0h					0h		

Table 2-32. TOP_CTRL_EFUSE_OVERRIDE_LDO_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:24	EFUSE_OVERRIDE_LDO_TRIM_LDO_TRIM_OFFSET	R/W	0h	LDO Fine trim around program point
23:20	RESERVED	NONE	0h	Reserved
19:16	EFUSE_OVERRIDE_LDO_TRIM_LDO_PROG	R/W	0h	LDO programming controls. Adjusts nominal LDO output voltage
15:3	RESERVED	NONE	0h	Reserved
2:0	EFUSE_OVERRIDE_LDO_TRIM_OVERRIDE	R/W	0h	Override EFUSE Value with SW Value Write 3'b000 : EFUSE Value Write 3'b111 : MMR Value

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2.2.2.16 TOP_CTRL_ADC_REFBUF0_CTRL Register

2.2.2.16.1 TOP_CTRL_ADC_REFBUF0_CTRL Register (Offset = C00h) [reset = 0h]

This register is used to enable or disable ADC Reference buffer 0

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Table 2-33. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C00h

Figure 2-16. TOP_CTRL_ADC_REFBUF0_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_REFBUF0_CTRL_ENABLE		
NONE					R/W		
0h					0h		

Table 2-34. TOP_CTRL_ADC_REFBUF0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_REFBUF0_CTRL_ENABLE	R/W	0h	Enables adc reference 0, mask hhv before enable 000:Disable 111 : Enable

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2.2.2.17 TOP_CTRL_ADC_REFBUF1_CTRL Register

2.2.2.17.1 TOP_CTRL_ADC_REFBUF1_CTRL Register (Offset = C04h) [reset = 0h]

This register is used to enable or disable ADC Reference buffer 1

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Table 2-35. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C04h

Figure 2-17. TOP_CTRL_ADC_REFBUF1_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_REFBUF1_CTRL_ENABLE		
NONE					R/W		
0h					0h		

Table 2-36. TOP_CTRL_ADC_REFBUF1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_REFBUF1_CTRL_ENABLE	R/W	0h	Enables adc reference 0, mask hhv before enable 000:Disable 111 : Enable

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2.2.2.18 TOP_CTRL_ADC_REF_COMP_CTRL Register

2.2.2.18.1 TOP_CTRL_ADC_REF_COMP_CTRL Register (Offset = C08h) [reset = 0h]

This register is used to enable or disable the voltage monitors which measure if the ADC reference voltage is good or not.

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Table 2-37. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C08h

Figure 2-18. TOP_CTRL_ADC_REF_COMP_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	ADC_REF_COMP_CTRL_ADCR01_REFOK_EN			RESERVED	ADC_REF_COMP_CTRL_ADC34_REFOK_EN		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	ADC_REF_COMP_CTRL_ADC12_REFOK_EN			RESERVED	ADC_REF_COMP_CTRL_ADC0_REFOK_EN		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 2-38. TOP_CTRL_ADC_REF_COMP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	ADC_REF_COMP_CTRL_ADCR01_REFOK_EN	R/W	0h	Enables reference comparators [ROK2]. This monitors adc5 & adc6 refernce
11	RESERVED	NONE	0h	Reserved
10:8	ADC_REF_COMP_CTRL_ADC34_REFOK_EN	R/W	0h	Enables reference comparators [ROK1]. This monitors adc3 & adc4 refernc
7	RESERVED	NONE	0h	Reserved
6:4	ADC_REF_COMP_CTRL_ADC12_REFOK_EN	R/W	0h	Enables reference comparators [ROK0B]. This monitors adc1 & adc2 refernce
3	RESERVED	NONE	0h	Reserved
2:0	ADC_REF_COMP_CTRL_ADC0_REFOK_EN	R/W	0h	Enables reference comparators [ROK0]. This monitors adc0 refernce

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2.2.2.19 TOP_CTRL_ADC_REF_GOOD_STATUS Register

2.2.2.19.1 TOP_CTRL_ADC_REF_GOOD_STATUS Register (Offset = C0Ch) [reset = FFh]

This register shows the status of ADC reference voltages as measured by the ADC Reference OK voltage monitors.

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Table 2-39. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C0Ch

Figure 2-19. TOP_CTRL_ADC_REF_GOOD_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ADC_REF_GOOD_STATUS_ADCR01_REF_UV_GOOD	ADC_REF_GOOD_STATUS_ADCR01_REF_OV_GOOD	ADC_REF_GOOD_STATUS_ADC12_REF_UV_GOOD	ADC_REF_GOOD_STATUS_ADC12_REF_OV_GOOD	ADC_REF_GOOD_STATUS_ADC0_REF_UV_GOOD	ADC_REF_GOOD_STATUS_ADC0_REF_OV_GOOD	ADC_REF_GOOD_STATUS_ADC34_REF_UV_GOOD	ADC_REF_GOOD_STATUS_ADC34_REF_OV_GOOD
R	R	R	R	R	R	R	R
1h	1h	1h	1h	1h	1h	1h	1h

Table 2-40. TOP_CTRL_ADC_REF_GOOD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	ADC_REF_GOOD_STATUS_ADCR01_REF_UV_GOOD	R	1h	Under Voltage check OK 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition
6	ADC_REF_GOOD_STATUS_ADCR01_REF_OV_GOOD	R	1h	Over voltage check OK 1'b1 - Comparator output is ok for over voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for over voltage condition
5	ADC_REF_GOOD_STATUS_ADC12_REF_UV_GOOD	R	1h	Under Voltage check OK 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition
4	ADC_REF_GOOD_STATUS_ADC12_REF_OV_GOOD	R	1h	Over voltage check OK 1'b1 - Comparator output is ok for over voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for over voltage condition
3	ADC_REF_GOOD_STATUS_ADC0_REF_UV_GOOD	R	1h	Under Voltage check OK 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition

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Table 2-40. TOP_CTRL_ADC_REF_GOOD_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ADC_REF_GOOD_STATUS_ADC0_REF_OV_GOOD	R	1h	Over voltage check OK 1'b1 - Comparator output is ok for over voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for over voltage condition
1	ADC_REF_GOOD_STATUS_ADC34_REF_UV_GOOD	R	1h	Under Voltage check OK 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition
0	ADC_REF_GOOD_STATUS_ADC34_REF_OV_GOOD	R	1h	Over voltage check OK 1'b1 - Comparator output is ok for over voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for over voltage condition

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2.2.2.20 TOP_CTRL_VMON_CTRL Register

2.2.2.20.1 TOP_CTRL_VMON_CTRL Register (Offset = C10h) [reset = 7777777h]

This register is used to enable or disable the power supply voltage monitors present on the device.

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Table 2-41. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C10h

Figure 2-20. TOP_CTRL_VMON_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED					VMON_CTRL_CMP8_EN		
NONE					R/W		
0h					7h		
23	22	21	20	19	18	17	16
RESERVED	VMON_CTRL_CMP7_EN			RESERVED	VMON_CTRL_CMP5_EN		
NONE	R/W			NONE	R/W		
0h	7h			0h	7h		
15	14	13	12	11	10	9	8
RESERVED	VMON_CTRL_CMP3_EN			RESERVED	VMON_CTRL_CMP2_EN		
NONE	R/W			NONE	R/W		
0h	7h			0h	7h		
7	6	5	4	3	2	1	0
RESERVED	VMON_CTRL_CMP1_EN			RESERVED	VMON_CTRL_CMP0_EN		
NONE	R/W			NONE	R/W		
0h	7h			0h	7h		

Table 2-42. TOP_CTRL_VMON_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	VMON_CTRL_CMP8_EN	R/W	7h	Enable for VMON comparator 8 Configure it to 3'000 to disable it.
23	RESERVED	NONE	0h	Reserved
22:20	VMON_CTRL_CMP7_EN	R/W	7h	Enable for VMON comparator 7 Configure it to 3'000 to disable it.
19	RESERVED	NONE	0h	Reserved
18:16	VMON_CTRL_CMP5_EN	R/W	7h	Enable for VMON comparator 5 Configure it to 3'000 to disable it.
15	RESERVED	NONE	0h	Reserved
14:12	VMON_CTRL_CMP3_EN	R/W	7h	Enable for VMON comparator 3 Configure it to 3'000 to disable it.
11	RESERVED	NONE	0h	Reserved
10:8	VMON_CTRL_CMP2_EN	R/W	7h	Enable for VMON comparator 2 Configure it to 3'000 to disable it.
7	RESERVED	NONE	0h	Reserved
6:4	VMON_CTRL_CMP1_EN	R/W	7h	Enable for VMON comparator 1 Configure it to 3'000 to disable it.
3	RESERVED	NONE	0h	Reserved
2:0	VMON_CTRL_CMP0_EN	R/W	7h	Enable for VMON comparator 0 Configure it to 3'000 to disable it.

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2.2.2.21 TOP_CTRL_VMON_STAT Register

2.2.2.21.1 TOP_CTRL_VMON_STAT Register (Offset = C14h) [reset = 7FFh]

This register shows the status output from the voltage monitors present on the device.

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Table 2-43. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C14h

Figure 2-21. TOP_CTRL_VMON_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					VMON_STAT_CMP8_UV_OK	VMON_STAT_CMP7_UV_OK	VMON_STAT_CMP5_UV_OK
NONE					R	R	R
0h					1h	1h	1h
7	6	5	4	3	2	1	0
VMON_STAT_CMP5_OV_OK	VMON_STAT_CMP3_UV_OK	VMON_STAT_CMP3_OV_OK	VMON_STAT_CMP2_UV_OK	VMON_STAT_CMP2_OV_OK	VMON_STAT_CMP1_UV_OK	VMON_STAT_CMP1_OV_OK	VMON_STAT_CMP0_UV_OK
R	R	R	R	R	R	R	R
1h	1h	1h	1h	1h	1h	1h	1h

Table 2-44. TOP_CTRL_VMON_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	VMON_STAT_CMP8_UV_OK	R	1h	VMON status register for comparator 8. 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition
9	VMON_STAT_CMP7_UV_OK	R	1h	VMON status register for comparator 7. 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition
8	VMON_STAT_CMP5_UV_OK	R	1h	VMON status register for comparator 5. 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition
7	VMON_STAT_CMP5_OV_OK	R	1h	VMON status register for comparator 5.
6	VMON_STAT_CMP3_UV_OK	R	1h	VMON status register for comparator 3. 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition
5	VMON_STAT_CMP3_OV_OK	R	1h	VMON status register for comparator 3. 1'b1 - Comparator output is ok for over voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for over voltage condition

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Table 2-44. TOP_CTRL_VMON_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	VMON_STAT_CMP2_UV_OK	R	1h	VMON status register for comparator 2. 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition
3	VMON_STAT_CMP2_OV_OK	R	1h	VMON status register for comparator 2. 1'b1 - Comparator output is ok for over voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for over voltage condition
2	VMON_STAT_CMP1_UV_OK	R	1h	VMON status register for comparator 1. 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition
1	VMON_STAT_CMP1_OV_OK	R	1h	VMON status register for comparator 1. 1'b1 - Comparator output is ok for over voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for over voltage condition
0	VMON_STAT_CMP0_UV_OK	R	1h	VMON status register for comparator 0. 1'b1 - Comparator output is ok for under voltage condition. 1'b0 - Comparator output is 1'b0 as threshold condition is not meeting for under voltage condition

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2.2.2.22 TOP_CTRL_PMU_COARSE_STAT Register

2.2.2.22.1 TOP_CTRL_PMU_COARSE_STAT Register (Offset = C18h) [reset = Fh]

This register shows the status of coarse voltage monitors present in the device.

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Table 2-45. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C18h

Figure 2-22. TOP_CTRL_PMU_COARSE_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PMU_COARSE_STAT_BG_RDY	PMU_COARSE_STAT_LDO_RDY	PMU_COARSE_STAT_VCORE_RDY	PMU_COARSE_STAT_VSUP18_RDY
NONE				R	R	R	R
0h				1h	1h	1h	1h

Table 2-46. TOP_CTRL_PMU_COARSE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PMU_COARSE_STAT_BG_RDY	R	1h	Bandgap coarse detection status signals.
2	PMU_COARSE_STAT_LDO_RDY	R	1h	LDO coarse detection status signals.
1	PMU_COARSE_STAT_VCORE_RDY	R	1h	vcore coarse detection status signals.
0	PMU_COARSE_STAT_VSUP18_RDY	R	1h	vdda18 coarse detection status signals.

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2.2.2.23 TOP_CTRL_MASK_VMON_ERROR_ESM_H Register

2.2.2.23.1 TOP_CTRL_MASK_VMON_ERROR_ESM_H Register (Offset = C20h) [reset = 7FFFFh]

This register is used to select the voltage monitors whose Error staus should triggering the ESM High Interrupt.

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Table 2-47. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C20h

Figure 2-23. TOP_CTRL_MASK_VMON_ERROR_ESM_H Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					MASK_VMON_ERROR_ESM_H_ADCR01_REF_UV_MASK	MASK_VMON_ERROR_ESM_H_ADCR01_REF_OV_MASK	MASK_VMON_ERROR_ESM_H_ADC12_REF_UV_MASK
NONE					R/W	R/W	R/W
0h					1h	1h	1h
15	14	13	12	11	10	9	8
MASK_VMON_ERROR_ESM_H_ADC12_REF_OV_MASK	MASK_VMON_ERROR_ESM_H_ADC0_REF_UV_MASK	MASK_VMON_ERROR_ESM_H_ADC0_REF_OV_MASK	MASK_VMON_ERROR_ESM_H_ADC34_REF_UV_MASK	MASK_VMON_ERROR_ESM_H_ADC34_REF_OV_MASK	MASK_VMON_ERROR_ESM_H_CMP8_UV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP7_UV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP5_UV_ERR_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
MASK_VMON_ERROR_ESM_H_CMP5_OV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP3_UV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP3_OV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP2_UV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP2_OV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP1_UV_ERR_NASK	MASK_VMON_ERROR_ESM_H_CMP1_OV_ERR_MASK	MASK_VMON_ERROR_ESM_H_CMP0_UV_ERR_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h

Table 2-48. TOP_CTRL_MASK_VMON_ERROR_ESM_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	MASK_VMON_ERROR_ESM_H_ADCR01_REF_UV_MASK	R/W	1h	ADCR01 REF UV VMON Error Mask to ESM Interrupt
17	MASK_VMON_ERROR_ESM_H_ADCR01_REF_OV_MASK	R/W	1h	ADCR01 REF OV VMON Error Mask to ESM Interrupt
16	MASK_VMON_ERROR_ESM_H_ADC12_REF_UV_MASK	R/W	1h	ADC34 REF UV VMON Error Mask to ESM Interrupt
15	MASK_VMON_ERROR_ESM_H_ADC12_REF_OV_MASK	R/W	1h	ADC34 REF OV VMON Error Mask to ESM Interrupt
14	MASK_VMON_ERROR_ESM_H_ADC0_REF_UV_MASK	R/W	1h	ADC12 REF UV VMON Error Mask to ESM Interrupt

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Table 2-48. TOP_CTRL_MASK_VMON_ERROR_ESM_H Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MASK_VMON_ERROR_ESM_H_ADC0_REF_OV_MASK	R/W	1h	ADC12 REF OV VMON Error Mask to ESM Interrupt
12	MASK_VMON_ERROR_ESM_H_ADC34_REF_UV_MASK	R/W	1h	ADC0 REF UV VMON Error Mask to ESM Interrupt
11	MASK_VMON_ERROR_ESM_H_ADC34_REF_OV_MASK	R/W	1h	ADC0 REF OV VMON Error Mask to ESM Interrupt
10	MASK_VMON_ERROR_ESM_H_CMP8_UV_ERR_MASK	R/W	1h	CMP8 UV VMON Error Mask to ESM Interrupt
9	MASK_VMON_ERROR_ESM_H_CMP7_UV_ERR_MASK	R/W	1h	CMP7 UV VMON Error Mask to ESM Interrupt
8	MASK_VMON_ERROR_ESM_H_CMP5_UV_ERR_MASK	R/W	1h	CMP5 UV VMON Error Mask to ESM Interrupt
7	MASK_VMON_ERROR_ESM_H_CMP5_OV_ERR_MASK	R/W	1h	CMP5 OV VMON Error Mask to ESM Interrupt
6	MASK_VMON_ERROR_ESM_H_CMP3_UV_ERR_MASK	R/W	1h	CMP3 UV VMON Error Mask to ESM Interrupt
5	MASK_VMON_ERROR_ESM_H_CMP3_OV_ERR_MASK	R/W	1h	CMP3 OV VMON Error Mask to ESM Interrupt
4	MASK_VMON_ERROR_ESM_H_CMP2_UV_ERR_MASK	R/W	1h	CMP2 UV VMON Error Mask to ESM Interrupt
3	MASK_VMON_ERROR_ESM_H_CMP2_OV_ERR_MASK	R/W	1h	CMP2 OV VMON Error Mask to ESM Interrupt
2	MASK_VMON_ERROR_ESM_H_CMP1_UV_ERR_NASK	R/W	1h	CMP1 UV VMON Error Mask to ESM Interrupt
1	MASK_VMON_ERROR_ESM_H_CMP1_OV_ERR_MASK	R/W	1h	CMP1 OV VMON Error Mask to ESM Interrupt
0	MASK_VMON_ERROR_ESM_H_CMP0_UV_ERR_MASK	R/W	1h	CMP0 UV VMON Error Mask to ESM Interrupt

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2.2.2.24 TOP_CTRL_MASK_VMON_ERROR_ESM_L Register

2.2.2.24.1 TOP_CTRL_MASK_VMON_ERROR_ESM_L Register (Offset = C24h) [reset = 7FFFFh]

This register is used to select the voltage monitors whose Error staus should triggering the ESM Low Interrupt.

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Table 2-49. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C24h

Figure 2-24. TOP_CTRL_MASK_VMON_ERROR_ESM_L Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					MASK_VMON_ERROR_ESM_L_ADCR01_REF_UV_MASK	MASK_VMON_ERROR_ESM_L_ADCR01_REF_OV_MASK	MASK_VMON_ERROR_ESM_L_ADC12_REF_UV_MASK
NONE					R/W	R/W	R/W
0h					1h	1h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MASK_VMON_ERROR_ESM_L_ADC12_REF_OV_MASK	MASK_VMON_ERROR_ESM_L_ADC0_REF_UV_MASK	MASK_VMON_ERROR_ESM_L_ADC0_REF_OV_MASK	MASK_VMON_ERROR_ESM_L_ADC34_REF_UV_MASK	MASK_VMON_ERROR_ESM_L_ADC34_REF_OV_MASK	MASK_VMON_ERROR_ESM_L_CMP8_UV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP7_UV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP5_UV_ERR_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MASK_VMON_ERROR_ESM_L_CMP5_OV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP3_UV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP3_OV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP2_UV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP2_OV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP1_UV_ERR_NASK	MASK_VMON_ERROR_ESM_L_CMP1_OV_ERR_MASK	MASK_VMON_ERROR_ESM_L_CMP0_UV_ERR_MASK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h

Table 2-50. TOP_CTRL_MASK_VMON_ERROR_ESM_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	MASK_VMON_ERROR_ESM_L_ADCR01_REF_UV_MASK	R/W	1h	ADCR01 REF UV VMON Error Mask to ESM Interrupt
17	MASK_VMON_ERROR_ESM_L_ADCR01_REF_OV_MASK	R/W	1h	ADCR01 REF OV VMON Error Mask to ESM Interrupt
16	MASK_VMON_ERROR_ESM_L_ADC12_REF_UV_MASK	R/W	1h	ADC34 REF UV VMON Error Mask to ESM Interrupt
15	MASK_VMON_ERROR_ESM_L_ADC12_REF_OV_MASK	R/W	1h	ADC34 REF OV VMON Error Mask to ESM Interrupt
14	MASK_VMON_ERROR_ESM_L_ADC0_REF_UV_MASK	R/W	1h	ADC12 REF UV VMON Error Mask to ESM Interrupt

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Table 2-50. TOP_CTRL_MASK_VMON_ERROR_ESM_L Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MASK_VMON_ERROR_ESM_L_ADC0_REF_OV_MASK	R/W	1h	ADC12 REF OV VMON Error Mask to ESM Interrupt
12	MASK_VMON_ERROR_ESM_L_ADC34_REF_UV_MASK	R/W	1h	ADC0 REF UV VMON Error Mask to ESM Interrupt
11	MASK_VMON_ERROR_ESM_L_ADC34_REF_OV_MASK	R/W	1h	ADC0 REF OV VMON Error Mask to ESM Interrupt
10	MASK_VMON_ERROR_ESM_L_CMP8_UV_ERR_MASK	R/W	1h	CMP8 UV VMON Error Mask to ESM Interrupt
9	MASK_VMON_ERROR_ESM_L_CMP7_UV_ERR_MASK	R/W	1h	CMP7 UV VMON Error Mask to ESM Interrupt
8	MASK_VMON_ERROR_ESM_L_CMP5_UV_ERR_MASK	R/W	1h	CMP5 UV VMON Error Mask to ESM Interrupt
7	MASK_VMON_ERROR_ESM_L_CMP5_OV_ERR_MASK	R/W	1h	CMP5 OV VMON Error Mask to ESM Interrupt
6	MASK_VMON_ERROR_ESM_L_CMP3_UV_ERR_MASK	R/W	1h	CMP3 UV VMON Error Mask to ESM Interrupt
5	MASK_VMON_ERROR_ESM_L_CMP3_OV_ERR_MASK	R/W	1h	CMP3 OV VMON Error Mask to ESM Interrupt
4	MASK_VMON_ERROR_ESM_L_CMP2_UV_ERR_MASK	R/W	1h	CMP2 UV VMON Error Mask to ESM Interrupt
3	MASK_VMON_ERROR_ESM_L_CMP2_OV_ERR_MASK	R/W	1h	CMP2 OV VMON Error Mask to ESM Interrupt
2	MASK_VMON_ERROR_ESM_L_CMP1_UV_ERR_NASK	R/W	1h	CMP1 UV VMON Error Mask to ESM Interrupt
1	MASK_VMON_ERROR_ESM_L_CMP1_OV_ERR_MASK	R/W	1h	CMP1 OV VMON Error Mask to ESM Interrupt
0	MASK_VMON_ERROR_ESM_L_CMP0_UV_ERR_MASK	R/W	1h	CMP0 UV VMON Error Mask to ESM Interrupt

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2.2.2.25 TOP_CTRL_MASK_ANA_ISO Register

2.2.2.25.1 TOP_CTRL_MASK_ANA_ISO Register (Offset = C30h) [reset = 0h]

This register is used to prevent the Coarse voltage monitor from triggering a faulty SOC reset due to a momentary supply glitch caused when enabling ADC reference buffers.

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Table 2-51. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C30h

Figure 2-25. TOP_CTRL_MASK_ANA_ISO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MASK_ANA_ISO_MASK		
NONE					R/W		
0h					0h		

Table 2-52. TOP_CTRL_MASK_ANA_ISO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MASK_ANA_ISO_MASK	R/W	0h	Mask the Ana ISO generating SOC reset due to a glitch on VDD OK. Used during Trim updates to the analog or during ADC Refbuf enable

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2.2.2.26 TOP_CTRL_VMON_FILTER_CTRL Register

2.2.2.26.1 TOP_CTRL_VMON_FILTER_CTRL Register (Offset = C34h) [reset = 0h]

This register is used to configure the filter present on the Voltage monitor outputs.

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Table 2-53. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C34h

Figure 2-26. TOP_CTRL_VMON_FILTER_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						VMON_FILTER_CTRL_SELECT_VALUE	
NONE						R/W	
0h						0h	

Table 2-54. TOP_CTRL_VMON_FILTER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	VMON_FILTER_CTRL_SELECT_VALUE	R/W	0h	VMON FILTER control select 2'b00 : no filtering [default] 2'b01 : filtering for 4.8us 2'b10 : filtering for 9.6us 2'b11 : filtering for 14.4us **Note: This bit will only be reset by PORz.

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2.2.2.27 TOP_CTRL_ADC_RNG_CTRL Register

2.2.2.27.1 TOP_CTRL_ADC_RNG_CTRL Register (Offset = C40h) [reset = 0h]

ADC range control in single ended mode.

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Table 2-55. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C40h

Figure 2-27. TOP_CTRL_ADC_RNG_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED						ADC_RNG_CTRL_SCALED_MODE	
NONE						R/W	
0h						0h	

7	6	5	4	3	2	1	0
RESERVED	ADC_RNG_CTRL_MODE						
NONE	R/W						
0h	0h						

Table 2-56. TOP_CTRL_ADC_RNG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	ADC_RNG_CTRL_SCALED_MODE	R/W	0h	This bit controls scaled mode for resolver adc's 2'b0 --> Normal output 2'b1 --> scale 0 4223in 0 4095[efectively supporting 0-3.3V in 12 bit space] [in 12bit mode only] bit8 corresponds to adc_r0 bit9 corresponds to adc_r1
7	RESERVED	NONE	0h	Reserved
6:0	ADC_RNG_CTRL_MODE	R/W	0h	Single-Ended Mode, 0 ADC Input supports 0 to Vref*32/1. 0V corresponds to all zero code and 3.2V corresponds to all 1 or code 40951 ADC Input supports Vref*1/18 to Vref*33/18. Vref*1/18 corresponds to all zero code and Vref*32/18 corresponds to all 1 or code 4095 Differential Mode Don't take any effect on the system Default is 0 Vcm=Vref*33/18/2 Vref = ADC reference voltage, typically 1.8V

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2.2.2.28 TOP_CTRL_ADC0_OSD_CHEN Register

2.2.2.28.1 TOP_CTRL_ADC0_OSD_CHEN Register (Offset = C44h) [reset = 0h]

ADC Channel enable for Open Short detection.

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Table 2-57. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C44h

Figure 2-28. TOP_CTRL_ADC0_OSD_CHEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		ADC0_OSD_CHEN_CH_OSD_EN					
NONE		R/W					
0h		0h					

Table 2-58. TOP_CTRL_ADC0_OSD_CHEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	ADC0_OSD_CHEN_CH_OSD_EN	R/W	0h	Controls enabling the channel for ADC when set to 1'b1. Each bit corresponds to the respective ADC channel - Bit 0 - ch0_osd_en Bit 1 - ch1_osd_en Bit 2 - ch2_osd_en Bit 3 - ch3_osd_en Bit 4 - ch4_osd_en Bit 5 - ch5_osd_en

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2.2.2.29 TOP_CTRL_ADC1_OSD_CHEN Register

2.2.2.29.1 TOP_CTRL_ADC1_OSD_CHEN Register (Offset = C48h) [reset = 0h]

ADC Channel enable for Open Short detection.

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Table 2-59. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C48h

Figure 2-29. TOP_CTRL_ADC1_OSD_CHEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ADC1_OSD_CHEN_CH_OSD_EN					
NONE		R/W					
0h		0h					

Table 2-60. TOP_CTRL_ADC1_OSD_CHEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	ADC1_OSD_CHEN_CH_OSD_EN	R/W	0h	Controls enabling the channel for ADC when set to 1'b1. Each bit corresponds to the respective ADC channel - Bit 0 - ch0_osd_en Bit 1 - ch1_osd_en Bit 2 - ch2_osd_en Bit 3 - ch3_osd_en Bit 4 - ch4_osd_en Bit 5 - ch5_osd_en

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2.2.2.30 TOP_CTRL_ADC2_OSD_CHEN Register

2.2.2.30.1 TOP_CTRL_ADC2_OSD_CHEN Register (Offset = C4Ch) [reset = 0h]

ADC Channel enable for Open Short detection.

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Table 2-61. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C4Ch

Figure 2-30. TOP_CTRL_ADC2_OSD_CHEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ADC2_OSD_CHEN_CH_OSD_EN					
NONE		R/W					
0h		0h					

Table 2-62. TOP_CTRL_ADC2_OSD_CHEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	ADC2_OSD_CHEN_CH_OSD_EN	R/W	0h	Controls enabling the channel for ADC when set to 1'b1. Each bit corresponds to the respective ADC channel - Bit 0 - ch0_osd_en Bit 1 - ch1_osd_en Bit 2 - ch2_osd_en Bit 3 - ch3_osd_en Bit 4 - ch4_osd_en Bit 5 - ch5_osd_en

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2.2.2.31 TOP_CTRL_ADC3_OSD_CHEN Register

2.2.2.31.1 TOP_CTRL_ADC3_OSD_CHEN Register (Offset = C50h) [reset = 0h]

ADC Channel enable for Open Short detection.

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Table 2-63. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C50h

Figure 2-31. TOP_CTRL_ADC3_OSD_CHEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ADC3_OSD_CHEN_CH_OSD_EN					
NONE		R/W					
0h		0h					

Table 2-64. TOP_CTRL_ADC3_OSD_CHEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	ADC3_OSD_CHEN_CH_OSD_EN	R/W	0h	Controls enabling the channel for ADC when set to 1'b1. Each bit corresponds to the respective ADC channel - Bit 0 - ch0_osd_en Bit 1 - ch1_osd_en Bit 2 - ch2_osd_en Bit 3 - ch3_osd_en Bit 4 - ch4_osd_en Bit 5 - ch5_osd_en

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2.2.2.32 TOP_CTRL_ADC4_OSD_CHEN Register

2.2.2.32.1 TOP_CTRL_ADC4_OSD_CHEN Register (Offset = C54h) [reset = 0h]

ADC Channel enable for Open Short detection.

Return to Summary Table

Table 2-65. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C54h

Figure 2-32. TOP_CTRL_ADC4_OSD_CHEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ADC4_OSD_CHEN_CH_OSD_EN					
NONE		R/W					
0h		0h					

Table 2-66. TOP_CTRL_ADC4_OSD_CHEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	ADC4_OSD_CHEN_CH_OSD_EN	R/W	0h	Controls enabling the channel for ADC when set to 1'b1. Each bit corresponds to the respective ADC channel - Bit 0 - ch0_osd_en Bit 1 - ch1_osd_en Bit 2 - ch2_osd_en Bit 3 - ch3_osd_en Bit 4 - ch4_osd_en Bit 5 - ch5_osd_en

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2.2.2.33 TOP_CTRL_ADC0_OSD_CTRL Register

2.2.2.33.1 TOP_CTRL_ADC0_OSD_CTRL Register (Offset = C58h) [reset = 0h]

ADC open short function controls.

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Table 2-67. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C58h

Figure 2-33. TOP_CTRL_ADC0_OSD_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC0_OSD_CTRL_FUNCTION		
NONE					R/W		
0h					0h		

Table 2-68. TOP_CTRL_ADC0_OSD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC0_OSD_CTRL_FUNCTION	R/W	0h	Controls the shorting of internal 5K, 11K resistor to the ADC channel for open short detection [Default 0] value function Impedance 5K voltage 7K voltage 3'b000 Zero Scale 5K || 7K vssa vssa 3'b001 Zero Scale 5K vssa open 3'b010 Zero Scale 7K open vssa 3'b011 Full Scale 5K || 7K vdd_3p3v vdd_3p3v 3'b100 Full Scale 5K vdd_3p3v open 3'b101 Full Scale 7K open vdd_3p3v 3'b110 5/12 Scale 5K || 7K vssa vdd_3p3v 3'b111 7/12 Scale K || 7K vdd_3p3v vssa *all resistor values can vary by + 30% **Function is only correct if the external circuits driving the analog port are high impedance. If the port is connected to external circuits the customer will have to calculate the expected output.

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2.2.2.34 TOP_CTRL_ADC1_OSD_CTRL Register

2.2.2.34.1 TOP_CTRL_ADC1_OSD_CTRL Register (Offset = C5Ch) [reset = 0h]

ADC open short function controls.

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Table 2-69. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C5Ch

Figure 2-34. TOP_CTRL_ADC1_OSD_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC1_OSD_CTRL_FUNCTION		
NONE					R/W		
0h					0h		

Table 2-70. TOP_CTRL_ADC1_OSD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC1_OSD_CTRL_FUNCTION	R/W	0h	Controls the shorting of internal 5K, 11K resistor to the ADC channel for open short detection [Default 0] value function Impedance 5K voltage 7K voltage 3'b000 Zero Scale 5K || 7K vssa vssa 3'b001 Zero Scale 5K vssa open 3'b010 Zero Scale 7K open vssa 3'b011 Full Scale 5K || 7K vdd_3p3v vdd_3p3v 3'b100 Full Scale 5K vdd_3p3v open 3'b101 Full Scale 7K open vdd_3p3v 3'b110 5/12 Scale 5K || 7K vssa vdd_3p3v 3'b111 7/12 Scale K || 7K vdd_3p3v vssa *all resistor values can vary by + 30% **Function is only correct if the external circuits driving the analog port are high impedance. If the port is connected to external circuits the customer will have to calculate the expected output.

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2.2.2.35 TOP_CTRL_ADC2_OSD_CTRL Register

2.2.2.35.1 TOP_CTRL_ADC2_OSD_CTRL Register (Offset = C60h) [reset = 0h]

ADC open short function controls.

Return to Summary Table

Table 2-71. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C60h

Figure 2-35. TOP_CTRL_ADC2_OSD_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC2_OSD_CTRL_FUNCTION		
NONE					R/W		
0h					0h		

Table 2-72. TOP_CTRL_ADC2_OSD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC2_OSD_CTRL_FUNCTION	R/W	0h	Controls the shorting of internal 5K, 11K resistor to the ADC channel for open short detection [Default 0] value function Impedance 5K voltage 7K voltage 3'b000 Zero Scale 5K || 7K vssa vssa 3'b001 Zero Scale 5K vssa open 3'b010 Zero Scale 7K open vssa 3'b011 Full Scale 5K || 7K vdd_3p3v vdd_3p3v 3'b100 Full Scale 5K vdd_3p3v open 3'b101 Full Scale 7K open vdd_3p3v 3'b110 5/12 Scale 5K || 7K vssa vdd_3p3v 3'b111 7/12 Scale K || 7K vdd_3p3v vssa *all resistor values can vary by + 30% **Function is only correct if the external circuits driving the analog port are high impedance. If the port is connected to external circuits the customer will have to calculate the expected output.

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2.2.2.36 TOP_CTRL_ADC3_OSD_CTRL Register

2.2.2.36.1 TOP_CTRL_ADC3_OSD_CTRL Register (Offset = C64h) [reset = 0h]

ADC open short function controls.

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Table 2-73. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C64h

Figure 2-36. TOP_CTRL_ADC3_OSD_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC3_OSD_CTRL_FUNCTION		
NONE					R/W		
0h					0h		

Table 2-74. TOP_CTRL_ADC3_OSD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC3_OSD_CTRL_FUNCTION	R/W	0h	Controls the shorting of internal 5K, 11K resistor to the ADC channel for open short detection [Default 0] value function Impedance 5K voltage 7K voltage 3'b000 Zero Scale 5K || 7K vssa vssa 3'b001 Zero Scale 5K vssa open 3'b010 Zero Scale 7K open vssa 3'b011 Full Scale 5K || 7K vdd_3p3v vdd_3p3v 3'b100 Full Scale 5K vdd_3p3v open 3'b101 Full Scale 7K open vdd_3p3v 3'b110 5/12 Scale 5K || 7K vssa vdd_3p3v 3'b111 7/12 Scale K || 7K vdd_3p3v vssa *all resistor values can vary by + 30% **Function is only correct if the external circuits driving the analog port are high impedance. If the port is connected to external circuits the customer will have to calculate the expected output.

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2.2.2.37 TOP_CTRL_ADC4_OSD_CTRL Register

2.2.2.37.1 TOP_CTRL_ADC4_OSD_CTRL Register (Offset = C68h) [reset = 0h]

ADC open short function controls.

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Table 2-75. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C68h

Figure 2-37. TOP_CTRL_ADC4_OSD_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC4_OSD_CTRL_FUNCTION		
NONE					R/W		
0h					0h		

Table 2-76. TOP_CTRL_ADC4_OSD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC4_OSD_CTRL_FUNCTION	R/W	0h	Controls the shorting of internal 5K, 11K resistor to the ADC channel for open short detection [Default 0] value function Impedance 5K voltage 7K voltage 3'b000 Zero Scale 5K || 7K vssa vssa 3'b001 Zero Scale 5K vssa open 3'b010 Zero Scale 7K open vssa 3'b011 Full Scale 5K || 7K vdd_3p3v vdd_3p3v 3'b100 Full Scale 5K vdd_3p3v open 3'b101 Full Scale 7K open vdd_3p3v 3'b110 5/12 Scale 5K || 7K vssa vdd_3p3v 3'b111 7/12 Scale K || 7K vdd_3p3v vssa *all resistor values can vary by + 30% **Function is only correct if the external circuits driving the analog port are high impedance. If the port is connected to external circuits the customer will have to calculate the expected output.

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2.2.2.38 TOP_CTRL_ADC_LOOPBACK_CTRL Register

2.2.2.38.1 TOP_CTRL_ADC_LOOPBACK_CTRL Register (Offset = C80h) [reset = 0h]

Controls loopback safety functionality from DAC output to ADC inputs.

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Table 2-77. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C80h

Figure 2-38. TOP_CTRL_ADC_LOOPBACK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ADC_LOOPBACK_CTRL_ADC_LOOPBACK_EN
NONE							R/W
0h							0h

Table 2-78. TOP_CTRL_ADC_LOOPBACK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ADC_LOOPBACK_CTRL_ADC_LOOPBACK_EN	R/W	0h	Controls ADC loopback 1'b1: loopback enabled, 1'b0: loopback disabled[default]

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2.2.2.39 TOP_CTRL_CMPSSA_LOOPBACK_CTRL Register

2.2.2.39.1 TOP_CTRL_CMPSSA_LOOPBACK_CTRL Register (Offset = C84h) [reset = 0h]

Controls loopback safety functionality from DAC output to ADC inputs.

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Table 2-79. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C84h

Figure 2-39. TOP_CTRL_CMPSSA_LOOPBACK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED						CMPSSA_LOOPBACK_CTRL_CMPSSH9_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSH8_LOOPBACK_EN
NONE						R/W	R/W
0h						0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CMPSSA_LOOPBACK_CTRL_CMPSSH7_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSH6_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSH5_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSH4_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSH3_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSH2_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSH1_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSH0_LOOPBACK_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CMPSSA_LOOPBACK_CTRL_CMPSSL9_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSL8_LOOPBACK_EN
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPSSA_LOOPBACK_CTRL_CMPSSL7_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSL6_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSL5_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSL4_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSL3_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSL2_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSL1_LOOPBACK_EN	CMPSSA_LOOPBACK_CTRL_CMPSSL0_LOOPBACK_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-80. TOP_CTRL_CMPSSA_LOOPBACK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25	CMPSSA_LOOPBACK_CTRL_CMPSSH9_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
24	CMPSSA_LOOPBACK_CTRL_CMPSSH8_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
23	CMPSSA_LOOPBACK_CTRL_CMPSSH7_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
22	CMPSSA_LOOPBACK_CTRL_CMPSSH6_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]

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Table 2-80. TOP_CTRL_CMPSSA_LOOPBACK_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	CMPSSA_LOOPBACK_CTRL_CMPSSH5_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
20	CMPSSA_LOOPBACK_CTRL_CMPSSH4_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
19	CMPSSA_LOOPBACK_CTRL_CMPSSH3_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
18	CMPSSA_LOOPBACK_CTRL_CMPSSH2_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
17	CMPSSA_LOOPBACK_CTRL_CMPSSH1_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
16	CMPSSA_LOOPBACK_CTRL_CMPSSH0_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
15:10	RESERVED	NONE	0h	Reserved
9	CMPSSA_LOOPBACK_CTRL_CMPSSL9_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
8	CMPSSA_LOOPBACK_CTRL_CMPSSL8_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
7	CMPSSA_LOOPBACK_CTRL_CMPSSL7_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
6	CMPSSA_LOOPBACK_CTRL_CMPSSL6_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
5	CMPSSA_LOOPBACK_CTRL_CMPSSL5_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
4	CMPSSA_LOOPBACK_CTRL_CMPSSL4_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
3	CMPSSA_LOOPBACK_CTRL_CMPSSL3_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
2	CMPSSA_LOOPBACK_CTRL_CMPSSL2_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
1	CMPSSA_LOOPBACK_CTRL_CMPSSL1_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
0	CMPSSA_LOOPBACK_CTRL_CMPSSL0_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]

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2.2.2.40 TOP_CTRL_CMPSSB_LOOPBACK_CTRL Register

2.2.2.40.1 TOP_CTRL_CMPSSB_LOOPBACK_CTRL Register (Offset = C88h) [reset = 0h]

Controls loopback safety functionality from DAC output to ADC inputs.

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Table 2-81. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C88h

Figure 2-40. TOP_CTRL_CMPSSB_LOOPBACK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED						CMPSSB_LOOPBACK_CTRL_CMPSSH9_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSH8_LOOPBACK_EN
NONE						R/W	R/W
0h						0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CMPSSB_LOOPBACK_CTRL_CMPSSH7_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSH6_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSH5_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSH4_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSH3_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSH2_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSH1_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSH0_LOOPBACK_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CMPSSB_LOOPBACK_CTRL_CMPSSL9_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSL8_LOOPBACK_EN
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPSSB_LOOPBACK_CTRL_CMPSSL7_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSL6_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSL5_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSL4_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSL3_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSL2_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSL1_LOOPBACK_EN	CMPSSB_LOOPBACK_CTRL_CMPSSL0_LOOPBACK_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-82. TOP_CTRL_CMPSSB_LOOPBACK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25	CMPSSB_LOOPBACK_CTRL_CMPSSH9_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
24	CMPSSB_LOOPBACK_CTRL_CMPSSH8_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
23	CMPSSB_LOOPBACK_CTRL_CMPSSH7_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
22	CMPSSB_LOOPBACK_CTRL_CMPSSH6_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]

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Table 2-82. TOP_CTRL_CMPSSB_LOOPBACK_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	CMPSSB_LOOPBACK_CTRL_CMPSSH5_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
20	CMPSSB_LOOPBACK_CTRL_CMPSSH4_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
19	CMPSSB_LOOPBACK_CTRL_CMPSSH3_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
18	CMPSSB_LOOPBACK_CTRL_CMPSSH2_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
17	CMPSSB_LOOPBACK_CTRL_CMPSSH1_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
16	CMPSSB_LOOPBACK_CTRL_CMPSSH0_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
15:10	RESERVED	NONE	0h	Reserved
9	CMPSSB_LOOPBACK_CTRL_CMPSSL9_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
8	CMPSSB_LOOPBACK_CTRL_CMPSSL8_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
7	CMPSSB_LOOPBACK_CTRL_CMPSSL7_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
6	CMPSSB_LOOPBACK_CTRL_CMPSSL6_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
5	CMPSSB_LOOPBACK_CTRL_CMPSSL5_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
4	CMPSSB_LOOPBACK_CTRL_CMPSSL4_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
3	CMPSSB_LOOPBACK_CTRL_CMPSSL3_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
2	CMPSSB_LOOPBACK_CTRL_CMPSSL2_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
1	CMPSSB_LOOPBACK_CTRL_CMPSSL1_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]
0	CMPSSB_LOOPBACK_CTRL_CMPSSL0_LOOPBACK_EN	R/W	0h	Controls CMPSS loopback enable 1'b1 : loopback enabled, 1'b0 : loopback disabled[default]

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2.2.2.41 TOP_CTRL_ADCR01_OSD_CHEN Register

2.2.2.41.1 TOP_CTRL_ADCR01_OSD_CHEN Register (Offset = C8Ch) [reset = 0h]

ADCR Channel enable for Open Short detection.

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Table 2-83. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C8Ch

Figure 2-41. TOP_CTRL_ADCR01_OSD_CHEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADCR01_OSD_CHEN_CH_OSD_EN							
R/W							
0h							

Table 2-84. TOP_CTRL_ADCR01_OSD_CHEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ADCR01_OSD_CHEN_CH_OSD_EN	R/W	0h	Controls enabling the channel for ADC when set to 1'b1. Each bit corresponds to the respective ADC channel - Bit 0 - ch0_osd_en Bit 1 - ch1_osd_en Bit 2 - ch2_osd_en Bit 3 - ch3_osd_en Bit 4 - ch4_osd_en Bit 5 - ch5_osd_en

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2.2.2.42 TOP_CTRL_ADCR01_OSD_CTRL Register

2.2.2.42.1 TOP_CTRL_ADCR01_OSD_CTRL Register (Offset = C90h) [reset = 0h]

ADCR open short function controls.

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Table 2-85. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C90h

Figure 2-42. TOP_CTRL_ADCR01_OSD_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADCR01_OSD_CTRL_FUNCTION		
NONE					R/W		
0h					0h		

Table 2-86. TOP_CTRL_ADCR01_OSD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADCR01_OSD_CTRL_FUNCTION	R/W	0h	Controls the shorting of internal 5K, 11K resistor to the ADC channel for open short detection [Default 0] value function Impedance 5K voltage 7K voltage 3'b000 Zero Scale 5K || 7K vssa vssa 3'b001 Zero Scale 5K vssa open 3'b010 Zero Scale 7K open vssa 3'b011 Full Scale 5K || 7K vdd_3p3v vdd_3p3v 3'b100 Full Scale 5K vdd_3p3v open 3'b101 Full Scale 7K open vdd_3p3v 3'b110 5/12 Scale 5K || 7K vssa vdd_3p3v 3'b111 7/12 Scale K || 7K vdd_3p3v vssa *all resistor values can vary by + 30% **Function is only correct if the external circuits driving the analog port are high impedance. If the port is connected to external circuits the customer will have to calculate the expected output.

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2.2.2.43 TOP_CTRL_ADC_REFBUF2_CTRL Register

2.2.2.43.1 TOP_CTRL_ADC_REFBUF2_CTRL Register (Offset = C94h) [reset = 0h]

This register is used to enable or disable ADC Reference buffer 2

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Table 2-87. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C94h

Figure 2-43. TOP_CTRL_ADC_REFBUF2_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_REFBUF2_CTRL_ENABLE		
NONE					R/W		
0h					0h		

Table 2-88. TOP_CTRL_ADC_REFBUF2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_REFBUF2_CTRL_ENABLE	R/W	0h	Enables adc reference 0, mask hhv before enable 000:Disable 111 : Enable

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2.2.2.44 TOP_CTRL_TSENSE_CFG Register

2.2.2.44.1 TOP_CTRL_TSENSE_CFG Register (Offset = D00h) [reset = 11110000h]

This register is used to enableand configure the Teperature sensors present in the device .

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Table 2-89. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D00h

Figure 2-44. TOP_CTRL_TSENSE_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED			TSENSE_CFG_TMPSOFF	RESERVED			TSENSE_CFG_BGROFF
NONE			R/W	NONE			R/W
0h			1h	0h			1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TSENSE_CFG_AIPOFF	RESERVED			TSENSE_CFG_SNSR_MX_HIZ
NONE			R/W	NONE			R/W
0h			1h	0h			1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TSENSE_CFG_DELAY					
NONE		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSENSE_CFG_SENSOR_SEL				RESERVED			TSENSE_CFG_ENABLE
R/W				NONE			R/W
0h				0h			0h

Table 2-90. TOP_CTRL_TSENSE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	TSENSE_CFG_TMPSOFF	R/W	1h	BandGap on/off control 1'b1 : off 1'b0 : on **Note: This bit will only be reset by PORz.
27:25	RESERVED	NONE	0h	Reserved
24	TSENSE_CFG_BGROFF	R/W	1h	BandGap on/off control 1'b1 : off 1'b0 : on **Note: This bit will only be reset by PORz.
23:21	RESERVED	NONE	0h	Reserved
20	TSENSE_CFG_AIPOFF	R/W	1h	1'b1 : iddq mode select 1'b0 : normal mode **Note: This bit will only be reset by PORz.
19:17	RESERVED	NONE	0h	Reserved
16	TSENSE_CFG_SNSR_MX_HIZ	R/W	1h	Sensor mux hiz control 1'b0 : normal operation. Mux will select either one of the anlaog sensor 1'b1 : mux will be high impedence **Note: This bit will only be reset by PORz.
15:14	RESERVED	NONE	0h	Reserved

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Table 2-90. TOP_CTRL_TSENSE_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	TSENSE_CFG_DELAY	R/W	0h	Number of wait clock cycles between each TMPS Readout. Configure a Non zero value as delay value since configuring 0 is not allowed **Note: This bit will only be reset by PORz.
7:4	TSENSE_CFG_SENSOR_SEL	R/W	0h	Sensor Selection sensor enable bits for each sensor 1'b0 : sensor disable 1'b1 : sensor enable bit3: temp_sensor3 bit2: temp_sensor2 bit1: temp_sensor1 bit0: temp_sensor0 **Note: This bit will only be reset by PORz.
3:1	RESERVED	NONE	0h	Reserved
0	TSENSE_CFG_ENABLE	R/W	0h	Temperature controller enable **Note: This bit will only be reset by PORz.

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2.2.2.45 TOP_CTRL_TSENSE_STATUS Register

2.2.2.45.1 TOP_CTRL_TSENSE_STATUS Register (Offset = D04h) [reset = 0h]

This register shows the status of Temperature comparator events which are unmasked.

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Table 2-91. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D04h

Figure 2-45. TOP_CTRL_TSENSE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	TSENSE_STATUS_S1_HOT	TSENSE_STATUS_S1_COLD	TSENSE_STATUS_S1_LOW_THRHLD	RESERVED	TSENSE_STATUS_S0_HOT	TSENSE_STATUS_S0_COLD	TSENSE_STATUS_S0_LOW_THRHLD
NONE	R	R	R	NONE	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-92. TOP_CTRL_TSENSE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TSENSE_STATUS_S1_HOT	R	0h	temperature Sensor 1 hot event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz.
5	TSENSE_STATUS_S1_COLD	R	0h	temperature Sensor 1 cold event detect 1'b0 : event not occured 1'b1 : event occurred **Note: This bit will only be reset by PORz.
4	TSENSE_STATUS_S1_LOW_THRHLD	R	0h	temperature Sensor 1 low threshold event detect 1'b0 : event not occured 1'b1 : event occurred **Note: This bit will only be reset by PORz.
3	RESERVED	NONE	0h	Reserved
2	TSENSE_STATUS_S0_HOT	R	0h	temperature Sensor 0 hot event detect 1'b0 : event not occured 1'b1 : event occurred **Note: This bit will only be reset by PORz.
1	TSENSE_STATUS_S0_COLD	R	0h	temperature Sensor 0 cold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz.

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Table 2-92. TOP_CTRL_TSENSE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TSENSE_STATUS_S0_LOW_THRHLD	R	0h	temperature Sensor 0 low threshold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz.

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2.2.2.46 TOP_CTRL_TSENSE_STATUS_RAW Register

2.2.2.46.1 TOP_CTRL_TSENSE_STATUS_RAW Register (Offset = D08h) [reset = 0h]

This register shows the status of all Temperature comparators events including masked events.

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Table 2-93. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D08h

Figure 2-46. TOP_CTRL_TSENSE_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	TSENSE_STATUS_RAW_S1_HOT	TSENSE_STATUS_RAW_S1_COLD	TSENSE_STATUS_RAW_S1_LOW_THRHLD	RESERVED	TSENSE_STATUS_RAW_S0_HOT	TSENSE_STATUS_RAW_S0_COLD	TSENSE_STATUS_RAW_S0_LOW_THRHLD
NONE	R	R	R	NONE	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-94. TOP_CTRL_TSENSE_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TSENSE_STATUS_RAW_S1_HOT	R	0h	temperature Sensor 1 hot event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz.
5	TSENSE_STATUS_RAW_S1_COLD	R	0h	temperature Sensor 1 cold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz.
4	TSENSE_STATUS_RAW_S1_LOW_THRHLD	R	0h	temperature Sensor 1 low threshold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz.
3	RESERVED	NONE	0h	Reserved
2	TSENSE_STATUS_RAW_S0_HOT	R	0h	temperature Sensor 0 hot event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz.
1	TSENSE_STATUS_RAW_S0_COLD	R	0h	temperature Sensor 0 cold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz.

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Table 2-94. TOP_CTRL_TSENSE_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TSENSE_STATUS_RAW_S0_LOW_THRHLD	R	0h	temperature Sensor 0 low threshold event detect 0 : event not occured 1 : event occurred **Note: This bit will only be reset by PORz.

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2.2.2.47 TOP_CTRL_TSENSE0_ALERT Register

2.2.2.47.1 TOP_CTRL_TSENSE0_ALERT Register (Offset = D14h) [reset = 0h]

This register is used to configure the temperature thresholds for Temp Sensor 0 for generating Alert Interrupts.

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Table 2-95. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D14h

Figure 2-47. TOP_CTRL_TSENSE0_ALERT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TSENSE0_ALERT_ALERT_THRHLD_COLD							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TSENSE0_ALERT_ALERT_THRHLD_HOT							
R/W							
0h							

Table 2-96. TOP_CTRL_TSENSE0_ALERT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TSENSE0_ALERT_ALERT_THRHLD_COLD	R/W	0h	cold threshold/low temp threshold **Note: This bit will only be reset by PORz.
15:8	RESERVED	NONE	0h	Reserved
7:0	TSENSE0_ALERT_ALERT_THRHLD_HOT	R/W	0h	Hot threshold/high temp threshold **Note: This bit will only be reset by PORz.

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2.2.2.48 TOP_CTRL_TSENSE0_CNTL Register

2.2.2.48.1 TOP_CTRL_TSENSE0_CNTL Register (Offset = D18h) [reset = 100000h]

This register is used to control and configure Temperature sensor 0

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Table 2-97. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D18h

Figure 2-48. TOP_CTRL_TSENSE0_CNTL Name Register

31	30	29	28	27	26	25	24
RESERVED							TSENSE0_CNTL_MASK_LOW_THRHLD
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			TSENSE0_CNTL_MASK_HOT	RESERVED			TSENSE0_CNTL_MASK_COLD
NONE			R/W	NONE			R/W
0h			1h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TSENSE0_CNTL_ACCU_CLEAR
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TSENSE0_CNTL_FIFO_FREEZE	RESERVED			TSENSE0_CNTL_FIFO_CLEAR
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-98. TOP_CTRL_TSENSE0_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TSENSE0_CNTL_MASK_LOW_THRHLD	R/W	0h	mask low threshold comparator output **Note: This bit will only be reset by PORz.
23:21	RESERVED	NONE	0h	Reserved
20	TSENSE0_CNTL_MASK_HOT	R/W	1h	Mask hot comparator output **Note: This bit will only be reset by PORz.
19:17	RESERVED	NONE	0h	Reserved
16	TSENSE0_CNTL_MASK_COLD	R/W	0h	mask cold comparator output **Note: This bit will only be reset by PORz.
15:9	RESERVED	NONE	0h	Reserved
8	TSENSE0_CNTL_ACCU_CLEAR	R/W	0h	Accumulator clear **Note: This bit will only be reset by PORz.
7:5	RESERVED	NONE	0h	Reserved
4	TSENSE0_CNTL_FIFO_FREEZE	R/W	0h	fifo freeze **Note: This bit will only be reset by PORz.
3:1	RESERVED	NONE	0h	Reserved

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Table 2-98. TOP_CTRL_TSENSE0_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TSENSE0_CNTL_FIFO_CLEAR	R/W	0h	fifo clear **Note: This bit will only be reset by PORz.

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2.2.2.49 TOP_CTRL_TSENSE0_RESULT Register

2.2.2.49.1 TOP_CTRL_TSENSE0_RESULT Register (Offset = D1Ch) [reset = FFh]

This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 0

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Table 2-99. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D1Ch

Figure 2-49. TOP_CTRL_TSENSE0_RESULT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							TSENSE0_RESULT_ECOZ
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSENSE0_RESULT_DTEMP							
R							
FFh							

Table 2-100. TOP_CTRL_TSENSE0_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	TSENSE0_RESULT_ECOZ	R	0h	Conversion in Progress. 1'b1 : Conversion on going 1'b0 : conversion completed **Note: This bit will only be reset by PORz.
15:8	RESERVED	NONE	0h	Reserved
7:0	TSENSE0_RESULT_DTEMP	R	FFh	Temp Code readout **Note: This bit will only be reset by PORz.

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2.2.2.50 TOP_CTRL_TSENSE0_DATA0 Register

2.2.2.50.1 TOP_CTRL_TSENSE0_DATA0 Register (Offset = D20h) [reset = FFh]

Temp Sensor 0 Result FIFO Register 0

Return to Summary Table

Table 2-101. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D20h

Figure 2-50. TOP_CTRL_TSENSE0_DATA0 Name Register

31	30	29	28	27	26	25	24
TSENSE0_DATA0_TAG							
R							
0h							
23	22	21	20	19	18	17	16
TSENSE0_DATA0_TAG							
R							
0h							
15	14	13	12	11	10	9	8
TSENSE0_DATA0_TAG							
R							
0h							
7	6	5	4	3	2	1	0
TSENSE0_DATA0_DATA							
R							
FFh							

Table 2-102. TOP_CTRL_TSENSE0_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE0_DATA0_TAG	R	0h	Tag for temperature sesnor 0 Data 0 measured **Note: This bit will only be reset by PORz.
7:0	TSENSE0_DATA0_DATA	R	FFh	Temperature Sensor0 FIFO data 0 **Note: This bit will only be reset by PORz.

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2.2.2.51 TOP_CTRL_TSENSE0_DATA1 Register

2.2.2.51.1 TOP_CTRL_TSENSE0_DATA1 Register (Offset = D24h) [reset = 0h]

Temp Sensor 0 Result FIFO Register 1

Return to Summary Table

Table 2-103. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D24h

Figure 2-51. TOP_CTRL_TSENSE0_DATA1 Name Register

31	30	29	28	27	26	25	24
TSENSE0_DATA1_TAG							
R							
0h							
23	22	21	20	19	18	17	16
TSENSE0_DATA1_TAG							
R							
0h							
15	14	13	12	11	10	9	8
TSENSE0_DATA1_TAG							
R							
0h							
7	6	5	4	3	2	1	0
TSENSE0_DATA1_DATA							
R							
0h							

Table 2-104. TOP_CTRL_TSENSE0_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE0_DATA1_TAG	R	0h	Tag for temperature sesnor 0 Data 1 measured **Note: This bit will only be reset by PORz.
7:0	TSENSE0_DATA1_DATA	R	0h	Temperature Sensor0 FIFO data 1 **Note: This bit will only be reset by PORz.

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2.2.2.52 TOP_CTRL_TSENSE0_DATA2 Register

2.2.2.52.1 TOP_CTRL_TSENSE0_DATA2 Register (Offset = D28h) [reset = 0h]

Temp Sensor 0 Result FIFO Register 2

Return to Summary Table

Table 2-105. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D28h

Figure 2-52. TOP_CTRL_TSENSE0_DATA2 Name Register

31	30	29	28	27	26	25	24
TSENSE0_DATA2_TAG							
R							
0h							
23	22	21	20	19	18	17	16
TSENSE0_DATA2_TAG							
R							
0h							
15	14	13	12	11	10	9	8
TSENSE0_DATA2_TAG							
R							
0h							
7	6	5	4	3	2	1	0
TSENSE0_DATA2_DATA							
R							
0h							

Table 2-106. TOP_CTRL_TSENSE0_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE0_DATA2_TAG	R	0h	Tag for temperature sesnor 0 Data 2 measured **Note: This bit will only be reset by PORz.
7:0	TSENSE0_DATA2_DATA	R	0h	Temperature Sensor 0 FIFO data 2 **Note: This bit will only be reset by PORz.

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2.2.2.53 TOP_CTRL_TSENSE0_DATA3 Register

2.2.2.53.1 TOP_CTRL_TSENSE0_DATA3 Register (Offset = D2Ch) [reset = 0h]

Temp Sensor 0 Result FIFO Register 3

Return to Summary Table

Table 2-107. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D2Ch

Figure 2-53. TOP_CTRL_TSENSE0_DATA3 Name Register

31	30	29	28	27	26	25	24
TSENSE0_DATA3_TAG							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TSENSE0_DATA3_TAG							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TSENSE0_DATA3_TAG							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSENSE0_DATA3_DATA							
R							
0h							

Table 2-108. TOP_CTRL_TSENSE0_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE0_DATA3_TAG	R	0h	Tag for temperature sesnor 0 Data 3 measured **Note: This bit will only be reset by PORz.
7:0	TSENSE0_DATA3_DATA	R	0h	Temperature Sensor 0 FIFO data 3 **Note: This bit will only be reset by PORz.

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2.2.2.54 TOP_CTRL_TSENSE0_ACCU Register

2.2.2.54.1 TOP_CTRL_TSENSE0_ACCU Register (Offset = D30h) [reset = 0h]

Temp Sensor 0 Result Accumulator Register.

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Table 2-109. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D30h

Figure 2-54. TOP_CTRL_TSENSE0_ACCU Name Register

31	30	29	28	27	26	25	24
TSENSE0_ACCU_CUMUL							
R							
0h							
23	22	21	20	19	18	17	16
TSENSE0_ACCU_CUMUL							
R							
0h							
15	14	13	12	11	10	9	8
TSENSE0_ACCU_CUMUL							
R							
0h							
7	6	5	4	3	2	1	0
TSENSE0_ACCU_CUMUL							
R							
0h							

Table 2-110. TOP_CTRL_TSENSE0_ACCU Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSENSE0_ACCU_CUMUL	R	0h	cumulative sum of past DTEMPs **Note: This bit will only be reset by PORz.

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2.2.2.55 TOP_CTRL_TSENSE1_TSHUT Register

2.2.2.55.1 TOP_CTRL_TSENSE1_TSHUT Register (Offset = D40h) [reset = 0h]

This register is used to override the factory specified Tshut temperature with an application specific Tshut temperature for Temperature sensor 1

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Table 2-111. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D40h

Figure 2-55. TOP_CTRL_TSENSE1_TSHUT Name Register

31	30	29	28	27	26	25	24
TSENSE1_TSHUT_EFUSE_OVERRIDE			RESERVED				
R/W			NONE				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TSENSE1_TSHUT_TSHUT_THRHLD_HOT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSENSE1_TSHUT_TSHUT_THRSHLD_COLD							
R/W							
0h							

Table 2-112. TOP_CTRL_TSENSE1_TSHUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	TSENSE1_TSHUT_EFUSE_OVERRIDE	R/W	0h	Efuse override 3'b000 -- Value from EFUSE is used as tshut hot and tshut cold thresholds 3'b111 - Overide value takes effect **Note: This bit will only be reset by PORz.
28:24	RESERVED	NONE	0h	Reserved
23:16	TSENSE1_TSHUT_TSHUT_THRHLD_HOT	R/W	0h	tshut hot threshold. Reads efuse value untill overwritten with override = 111 **Note: This bit will only be reset by PORz.
15:8	RESERVED	NONE	0h	Reserved
7:0	TSENSE1_TSHUT_TSHUT_THRSHLD_COLD	R/W	0h	tshut cold threshold. Reads efuse value untill overwritten with override = 111 **Note: This bit will only be reset by PORz.

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2.2.2.56 TOP_CTRL_TSENSE1_ALERT Register

2.2.2.56.1 TOP_CTRL_TSENSE1_ALERT Register (Offset = D44h) [reset = 0h]

This register is used to configure the temperature thresholds for Temp Sensor 1 for generating Alert Interrupts.

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Table 2-113. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D44h

Figure 2-56. TOP_CTRL_TSENSE1_ALERT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
TSENSE1_ALERT_ALERT_THRHLD_COLD							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TSENSE1_ALERT_ALERT_THRHLD_HOT							
R/W							
0h							

Table 2-114. TOP_CTRL_TSENSE1_ALERT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TSENSE1_ALERT_ALERT_THRHLD_COLD	R/W	0h	cold threshold/low temp threshold **Note: This bit will only be reset by PORz.
15:8	RESERVED	NONE	0h	Reserved
7:0	TSENSE1_ALERT_ALERT_THRHLD_HOT	R/W	0h	Hot threshold/high temp threshold **Note: This bit will only be reset by PORz.

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2.2.2.57 TOP_CTRL_TSENSE1_CNTL Register

2.2.2.57.1 TOP_CTRL_TSENSE1_CNTL Register (Offset = D48h) [reset = 100000h]

This register is used to control and configure Temperature sensor 1

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Table 2-115. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D48h

Figure 2-57. TOP_CTRL_TSENSE1_CNTL Name Register

31	30	29	28	27	26	25	24
RESERVED							TSENSE1_CNTL_MASK_LOW_THRHLD
NONE							R/W
0h							0h

23	22	21	20	19	18	17	16
RESERVED			TSENSE1_CNTL_MASK_HOT	RESERVED			TSENSE1_CNTL_MASK_COLD
NONE			R/W	NONE			R/W
0h			1h	0h			0h

15	14	13	12	11	10	9	8
RESERVED							TSENSE1_CNTL_ACCU_CLEAR
NONE							R/W
0h							0h

7	6	5	4	3	2	1	0
RESERVED			TSENSE1_CNTL_FIFO_FREEZE	RESERVED			TSENSE1_CNTL_FIFO_CLEAR
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-116. TOP_CTRL_TSENSE1_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TSENSE1_CNTL_MASK_LOW_THRHLD	R/W	0h	mask low threshold comparator output **Note: This bit will only be reset by PORz.
23:21	RESERVED	NONE	0h	Reserved
20	TSENSE1_CNTL_MASK_HOT	R/W	1h	Mask hot comparator output **Note: This bit will only be reset by PORz.
19:17	RESERVED	NONE	0h	Reserved
16	TSENSE1_CNTL_MASK_COLD	R/W	0h	mask cold comparator output **Note: This bit will only be reset by PORz.
15:9	RESERVED	NONE	0h	Reserved
8	TSENSE1_CNTL_ACCU_CLEAR	R/W	0h	Accumulator clear **Note: This bit will only be reset by PORz.
7:5	RESERVED	NONE	0h	Reserved
4	TSENSE1_CNTL_FIFO_FREEZE	R/W	0h	fifo freeze **Note: This bit will only be reset by PORz.
3:1	RESERVED	NONE	0h	Reserved

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Table 2-116. TOP_CTRL_TSENSE1_CNTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TSENSE1_CNTL_FIFO_CLEAR	R/W	0h	fifo clear **Note: This bit will only be reset by PORz.

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2.2.2.58 TOP_CTRL_TSENSE1_RESULT Register

2.2.2.58.1 TOP_CTRL_TSENSE1_RESULT Register (Offset = D4Ch) [reset = FFh]

This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 1

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Table 2-117. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D4Ch

Figure 2-58. TOP_CTRL_TSENSE1_RESULT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							TSENSE1_RESULT_ECOZ
NONE							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TSENSE1_RESULT_DTEMP							
R							
FFh							

Table 2-118. TOP_CTRL_TSENSE1_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	TSENSE1_RESULT_ECOZ	R	0h	Conversion in Progress. 1'b1 : Conversion on going 1'b0 : conversion completed **Note: This bit will only be reset by PORz.
15:8	RESERVED	NONE	0h	Reserved
7:0	TSENSE1_RESULT_DTEMP	R	FFh	Temp Code readout **Note: This bit will only be reset by PORz.

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2.2.2.59 TOP_CTRL_TSENSE1_DATA0 Register

2.2.2.59.1 TOP_CTRL_TSENSE1_DATA0 Register (Offset = D50h) [reset = FFh]

Temp Sensor 1 Result FIFO Register 0

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Table 2-119. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D50h

Figure 2-59. TOP_CTRL_TSENSE1_DATA0 Name Register

31	30	29	28	27	26	25	24
TSENSE1_DATA0_TAG							
R							
0h							
23	22	21	20	19	18	17	16
TSENSE1_DATA0_TAG							
R							
0h							
15	14	13	12	11	10	9	8
TSENSE1_DATA0_TAG							
R							
0h							
7	6	5	4	3	2	1	0
TSENSE1_DATA0_DATA							
R							
FFh							

Table 2-120. TOP_CTRL_TSENSE1_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE1_DATA0_TAG	R	0h	Tag for temperature sesnor 1 Data 0 measured **Note: This bit will only be reset by PORz.
7:0	TSENSE1_DATA0_DATA	R	FFh	Temperature sensor 1 FIFO Data 0 **Note: This bit will only be reset by PORz.

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2.2.2.60 TOP_CTRL_TSENSE1_DATA1 Register

2.2.2.60.1 TOP_CTRL_TSENSE1_DATA1 Register (Offset = D54h) [reset = 0h]

Temp Sensor 1 Result FIFO Register 1

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Table 2-121. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D54h

Figure 2-60. TOP_CTRL_TSENSE1_DATA1 Name Register

31	30	29	28	27	26	25	24
TSENSE1_DATA1_TAG							
R							
0h							
23	22	21	20	19	18	17	16
TSENSE1_DATA1_TAG							
R							
0h							
15	14	13	12	11	10	9	8
TSENSE1_DATA1_TAG							
R							
0h							
7	6	5	4	3	2	1	0
TSENSE1_DATA1_DATA							
R							
0h							

Table 2-122. TOP_CTRL_TSENSE1_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE1_DATA1_TAG	R	0h	Temperature sensor 1 FIFO Data 1 **Note: This bit will only be reset by PORz.
7:0	TSENSE1_DATA1_DATA	R	0h	Temperature sensor 1 FIFO Data 1 **Note: This bit will only be reset by PORz.

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2.2.2.61 TOP_CTRL_TSENSE1_DATA2 Register

2.2.2.61.1 TOP_CTRL_TSENSE1_DATA2 Register (Offset = D58h) [reset = 0h]

Temp Sensor 1 Result FIFO Register 2

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Table 2-123. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D58h

Figure 2-61. TOP_CTRL_TSENSE1_DATA2 Name Register

31	30	29	28	27	26	25	24
TSENSE1_DATA2_TAG							
R							
0h							
23	22	21	20	19	18	17	16
TSENSE1_DATA2_TAG							
R							
0h							
15	14	13	12	11	10	9	8
TSENSE1_DATA2_TAG							
R							
0h							
7	6	5	4	3	2	1	0
TSENSE1_DATA2_DATA							
R							
0h							

Table 2-124. TOP_CTRL_TSENSE1_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE1_DATA2_TAG	R	0h	Temperature sensor 1 FIFO Data 2 **Note: This bit will only be reset by PORz.
7:0	TSENSE1_DATA2_DATA	R	0h	Temperature sensor 1 FIFO Data 2 **Note: This bit will only be reset by PORz.

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2.2.2.62 TOP_CTRL_TSENSE1_DATA3 Register

2.2.2.62.1 TOP_CTRL_TSENSE1_DATA3 Register (Offset = D5Ch) [reset = 0h]

Temp Sensor 1 Result FIFO Register 3

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Table 2-125. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D5Ch

Figure 2-62. TOP_CTRL_TSENSE1_DATA3 Name Register

31	30	29	28	27	26	25	24
TSENSE1_DATA3_TAG							
R							
0h							
23	22	21	20	19	18	17	16
TSENSE1_DATA3_TAG							
R							
0h							
15	14	13	12	11	10	9	8
TSENSE1_DATA3_TAG							
R							
0h							
7	6	5	4	3	2	1	0
TSENSE1_DATA3_DATA							
R							
0h							

Table 2-126. TOP_CTRL_TSENSE1_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	TSENSE1_DATA3_TAG	R	0h	Temperature sensor 1 FIFO Data 3 **Note: This bit will only be reset by PORz.
7:0	TSENSE1_DATA3_DATA	R	0h	Temperature sensor 1 FIFO Data 3 **Note: This bit will only be reset by PORz.

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2.2.2.63 TOP_CTRL_TSENSE1_ACCU Register

2.2.2.63.1 TOP_CTRL_TSENSE1_ACCU Register (Offset = D60h) [reset = 0h]

Temp Sensor 1 Result Accumulator Register.

Return to Summary Table

Table 2-127. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D60h

Figure 2-63. TOP_CTRL_TSENSE1_ACCU Name Register

31	30	29	28	27	26	25	24
TSENSE1_ACCU_CUMUL							
R							
0h							
23	22	21	20	19	18	17	16
TSENSE1_ACCU_CUMUL							
R							
0h							
15	14	13	12	11	10	9	8
TSENSE1_ACCU_CUMUL							
R							
0h							
7	6	5	4	3	2	1	0
TSENSE1_ACCU_CUMUL							
R							
0h							

Table 2-128. TOP_CTRL_TSENSE1_ACCU Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSENSE1_ACCU_CUMUL	R	0h	cumulative sum of past DTEMPs **Note: This bit will only be reset by PORz.

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2.2.2.64 TOP_CTRL_TSENSE2_RESULT Register

2.2.2.64.1 TOP_CTRL_TSENSE2_RESULT Register (Offset = D7Ch) [reset = 0h]

This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 2

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Table 2-129. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D7Ch

Figure 2-64. TOP_CTRL_TSENSE2_RESULT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							TSENSE2_RESULT_ECOZ
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSENSE2_RESULT_DTEMP							
R							
0h							

Table 2-130. TOP_CTRL_TSENSE2_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	TSENSE2_RESULT_ECOZ	R	0h	Conversion in Progress. 1'b1 : Conversion on going 1'b0 : conversion completed **Note: This bit will only be reset by PORz.
15:8	RESERVED	NONE	0h	Reserved
7:0	TSENSE2_RESULT_DTEMP	R	0h	Temp Code readout **Note: This bit will only be reset by PORz.

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2.2.2.65 TOP_CTRL_TSENSE3_RESULT Register

2.2.2.65.1 TOP_CTRL_TSENSE3_RESULT Register (Offset = DACh) [reset = 0h]

This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 3

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Table 2-131. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0DACh

Figure 2-65. TOP_CTRL_TSENSE3_RESULT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							TSENSE3_RESULT_ECOZ
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TSENSE3_RESULT_DTEMP							
R							
0h							

Table 2-132. TOP_CTRL_TSENSE3_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	TSENSE3_RESULT_ECOZ	R	0h	Conversion in Progress. 1'b1 : Conversion on going 1'b0 : conversion completed **Note: This bit will only be reset by PORz.
15:8	RESERVED	NONE	0h	Reserved
7:0	TSENSE3_RESULT_DTEMP	R	0h	Temp Code readout **Note: This bit will only be reset by PORz.

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2.2.2.66 TOP_CTRL_HW_SPARE_RW0 Register

2.2.2.66.1 TOP_CTRL_HW_SPARE_RW0 Register (Offset = FD0h) [reset = 0h]

HW_SPARE_RW0.

Return to Summary Table

Table 2-133. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0FD0h

Figure 2-66. TOP_CTRL_HW_SPARE_RW0 Name Register

31	30	29	28	27	26	25	24
HW_SPARE_RW0_HW_SPARE_RW0							
R/W							
0h							
23	22	21	20	19	18	17	16
HW_SPARE_RW0_HW_SPARE_RW0							
R/W							
0h							
15	14	13	12	11	10	9	8
HW_SPARE_RW0_HW_SPARE_RW0							
R/W							
0h							
7	6	5	4	3	2	1	0
HW_SPARE_RW0_HW_SPARE_RW0							
R/W							
0h							

Table 2-134. TOP_CTRL_HW_SPARE_RW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW0_HW_SPARE_RW0	R/W	0h	Reserved for HW R&D

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2.2.2.67 TOP_CTRL_HW_SPARE_RW1 Register

2.2.2.67.1 TOP_CTRL_HW_SPARE_RW1 Register (Offset = FD4h) [reset = 0h]

HW_SPARE_RW1.

Return to Summary Table

Table 2-135. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0FD4h

Figure 2-67. TOP_CTRL_HW_SPARE_RW1 Name Register

31	30	29	28	27	26	25	24
HW_SPARE_RW1_HW_SPARE_RW1							
R/W							
0h							
23	22	21	20	19	18	17	16
HW_SPARE_RW1_HW_SPARE_RW1							
R/W							
0h							
15	14	13	12	11	10	9	8
HW_SPARE_RW1_HW_SPARE_RW1							
R/W							
0h							
7	6	5	4	3	2	1	0
HW_SPARE_RW1_HW_SPARE_RW1							
R/W							
0h							

Table 2-136. TOP_CTRL_HW_SPARE_RW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW1_HW_SPARE_RW1	R/W	0h	Reserved for HW R&D

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2.2.2.68 TOP_CTRL_HW_SPARE_RW2 Register

2.2.2.68.1 TOP_CTRL_HW_SPARE_RW2 Register (Offset = FD8h) [reset = 0h]

HW_SPARE_RW2.

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Table 2-137. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0FD8h

Figure 2-68. TOP_CTRL_HW_SPARE_RW2 Name Register

31	30	29	28	27	26	25	24
HW_SPARE_RW2_HW_SPARE_RW2							
R/W							
0h							
23	22	21	20	19	18	17	16
HW_SPARE_RW2_HW_SPARE_RW2							
R/W							
0h							
15	14	13	12	11	10	9	8
HW_SPARE_RW2_HW_SPARE_RW2							
R/W							
0h							
7	6	5	4	3	2	1	0
HW_SPARE_RW2_HW_SPARE_RW2							
R/W							
0h							

Table 2-138. TOP_CTRL_HW_SPARE_RW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW2_HW_SPARE_RW2	R/W	0h	Reserved for HW R&D

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2.2.2.69 TOP_CTRL_HW_SPARE_RW3 Register

2.2.2.69.1 TOP_CTRL_HW_SPARE_RW3 Register (Offset = FDCh) [reset = 0h]

HW_SPARE_RW3.

Return to Summary Table

Table 2-139. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0FDCh

Figure 2-69. TOP_CTRL_HW_SPARE_RW3 Name Register

31	30	29	28	27	26	25	24
HW_SPARE_RW3_HW_SPARE_RW3							
R/W							
0h							
23	22	21	20	19	18	17	16
HW_SPARE_RW3_HW_SPARE_RW3							
R/W							
0h							
15	14	13	12	11	10	9	8
HW_SPARE_RW3_HW_SPARE_RW3							
R/W							
0h							
7	6	5	4	3	2	1	0
HW_SPARE_RW3_HW_SPARE_RW3							
R/W							
0h							

Table 2-140. TOP_CTRL_HW_SPARE_RW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RW3_HW_SPARE_RW3	R/W	0h	Reserved for HW R&D

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2.2.2.70 TOP_CTRL_HW_SPARE_RO0 Register

2.2.2.70.1 TOP_CTRL_HW_SPARE_RO0 Register (Offset = FE0h) [reset = 0h]

HW_SPARE_RO0.

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Table 2-141. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0FE0h

Figure 2-70. TOP_CTRL_HW_SPARE_RO0 Name Register

31	30	29	28	27	26	25	24
HW_SPARE_RO0_HW_SPARE_RO0							
R							
0h							
23	22	21	20	19	18	17	16
HW_SPARE_RO0_HW_SPARE_RO0							
R							
0h							
15	14	13	12	11	10	9	8
HW_SPARE_RO0_HW_SPARE_RO0							
R							
0h							
7	6	5	4	3	2	1	0
HW_SPARE_RO0_HW_SPARE_RO0							
R							
0h							

Table 2-142. TOP_CTRL_HW_SPARE_RO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO0_HW_SPARE_RO0	R	0h	Reserved for HW R&D

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2.2.2.71 TOP_CTRL_HW_SPARE_RO1 Register

2.2.2.71.1 TOP_CTRL_HW_SPARE_RO1 Register (Offset = FE4h) [reset = 0h]

HW_SPARE_RO1.

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Table 2-143. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0FE4h

Figure 2-71. TOP_CTRL_HW_SPARE_RO1 Name Register

31	30	29	28	27	26	25	24
HW_SPARE_RO1_HW_SPARE_RO1							
R							
0h							
23	22	21	20	19	18	17	16
HW_SPARE_RO1_HW_SPARE_RO1							
R							
0h							
15	14	13	12	11	10	9	8
HW_SPARE_RO1_HW_SPARE_RO1							
R							
0h							
7	6	5	4	3	2	1	0
HW_SPARE_RO1_HW_SPARE_RO1							
R							
0h							

Table 2-144. TOP_CTRL_HW_SPARE_RO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO1_HW_SPARE_RO1	R	0h	Reserved for HW R&D

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2.2.2.72 TOP_CTRL_HW_SPARE_RO2 Register

2.2.2.72.1 TOP_CTRL_HW_SPARE_RO2 Register (Offset = FE8h) [reset = 0h]

HW_SPARE_RO2.

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Table 2-145. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0FE8h

Figure 2-72. TOP_CTRL_HW_SPARE_RO2 Name Register

31	30	29	28	27	26	25	24
HW_SPARE_RO2_HW_SPARE_RO2							
R							
0h							
23	22	21	20	19	18	17	16
HW_SPARE_RO2_HW_SPARE_RO2							
R							
0h							
15	14	13	12	11	10	9	8
HW_SPARE_RO2_HW_SPARE_RO2							
R							
0h							
7	6	5	4	3	2	1	0
HW_SPARE_RO2_HW_SPARE_RO2							
R							
0h							

Table 2-146. TOP_CTRL_HW_SPARE_RO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO2_HW_SPARE_RO2	R	0h	Reserved for HW R&D

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2.2.2.73 TOP_CTRL_HW_SPARE_RO3 Register

2.2.2.73.1 TOP_CTRL_HW_SPARE_RO3 Register (Offset = FECh) [reset = 0h]

HW_SPARE_RO3.

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Table 2-147. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0FECh

Figure 2-73. TOP_CTRL_HW_SPARE_RO3 Name Register

31	30	29	28	27	26	25	24
HW_SPARE_RO3_HW_SPARE_RO3							
R							
0h							
23	22	21	20	19	18	17	16
HW_SPARE_RO3_HW_SPARE_RO3							
R							
0h							
15	14	13	12	11	10	9	8
HW_SPARE_RO3_HW_SPARE_RO3							
R							
0h							
7	6	5	4	3	2	1	0
HW_SPARE_RO3_HW_SPARE_RO3							
R							
0h							

Table 2-148. TOP_CTRL_HW_SPARE_RO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_RO3_HW_SPARE_RO3	R	0h	Reserved for HW R&D

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2.2.2.74 TOP_CTRL_HW_SPARE_WPH Register

2.2.2.74.1 TOP_CTRL_HW_SPARE_WPH Register (Offset = FF0h) [reset = 0h]

HW_SPARE_WPH.

Return to Summary Table

Table 2-149. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0FF0h

Figure 2-74. TOP_CTRL_HW_SPARE_WPH Name Register

31	30	29	28	27	26	25	24
HW_SPARE_WPH_HW_SPARE_WPH							
R/W							
0h							
23	22	21	20	19	18	17	16
HW_SPARE_WPH_HW_SPARE_WPH							
R/W							
0h							
15	14	13	12	11	10	9	8
HW_SPARE_WPH_HW_SPARE_WPH							
R/W							
0h							
7	6	5	4	3	2	1	0
HW_SPARE_WPH_HW_SPARE_WPH							
R/W							
0h							

Table 2-150. TOP_CTRL_HW_SPARE_WPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HW_SPARE_WPH_HW_SPARE_WPH	R/W	0h	Reserved for HW R&D

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2.2.2.75 TOP_CTRL_HW_SPARE_REC Register

2.2.2.75.1 TOP_CTRL_HW_SPARE_REC Register (Offset = FF4h) [reset = 0h]

HW_SPARE_REC.

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Table 2-151. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0FF4h

Figure 2-75. TOP_CTRL_HW_SPARE_REC Name Register

31	30	29	28	27	26	25	24
HW_SPARE_REC_HW_SPARE_REC31	HW_SPARE_REC_HW_SPARE_REC30	HW_SPARE_REC_HW_SPARE_REC29	HW_SPARE_REC_HW_SPARE_REC28	HW_SPARE_REC_HW_SPARE_REC27	HW_SPARE_REC_HW_SPARE_REC26	HW_SPARE_REC_HW_SPARE_REC25	HW_SPARE_REC_HW_SPARE_REC24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
HW_SPARE_REC_HW_SPARE_REC23	HW_SPARE_REC_HW_SPARE_REC22	HW_SPARE_REC_HW_SPARE_REC21	HW_SPARE_REC_HW_SPARE_REC20	HW_SPARE_REC_HW_SPARE_REC19	HW_SPARE_REC_HW_SPARE_REC18	HW_SPARE_REC_HW_SPARE_REC17	HW_SPARE_REC_HW_SPARE_REC16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
HW_SPARE_REC_HW_SPARE_REC15	HW_SPARE_REC_HW_SPARE_REC14	HW_SPARE_REC_HW_SPARE_REC13	HW_SPARE_REC_HW_SPARE_REC12	HW_SPARE_REC_HW_SPARE_REC11	HW_SPARE_REC_HW_SPARE_REC10	HW_SPARE_REC_HW_SPARE_REC9	HW_SPARE_REC_HW_SPARE_REC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
HW_SPARE_REC_HW_SPARE_REC7	HW_SPARE_REC_HW_SPARE_REC6	HW_SPARE_REC_HW_SPARE_REC5	HW_SPARE_REC_HW_SPARE_REC4	HW_SPARE_REC_HW_SPARE_REC3	HW_SPARE_REC_HW_SPARE_REC2	HW_SPARE_REC_HW_SPARE_REC1	HW_SPARE_REC_HW_SPARE_REC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-152. TOP_CTRL_HW_SPARE_REC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HW_SPARE_REC_HW_SPARE_REC31	R/W	0h	Reserved for HW R&D
30	HW_SPARE_REC_HW_SPARE_REC30	R/W	0h	Reserved for HW R&D
29	HW_SPARE_REC_HW_SPARE_REC29	R/W	0h	Reserved for HW R&D
28	HW_SPARE_REC_HW_SPARE_REC28	R/W	0h	Reserved for HW R&D
27	HW_SPARE_REC_HW_SPARE_REC27	R/W	0h	Reserved for HW R&D
26	HW_SPARE_REC_HW_SPARE_REC26	R/W	0h	Reserved for HW R&D
25	HW_SPARE_REC_HW_SPARE_REC25	R/W	0h	Reserved for HW R&D
24	HW_SPARE_REC_HW_SPARE_REC24	R/W	0h	Reserved for HW R&D

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Table 2-152. TOP_CTRL_HW_SPARE_REC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	HW_SPARE_REC_HW_SPARE_REC23	R/W	0h	Reserved for HW R&D
22	HW_SPARE_REC_HW_SPARE_REC22	R/W	0h	Reserved for HW R&D
21	HW_SPARE_REC_HW_SPARE_REC21	R/W	0h	Reserved for HW R&D
20	HW_SPARE_REC_HW_SPARE_REC20	R/W	0h	Reserved for HW R&D
19	HW_SPARE_REC_HW_SPARE_REC19	R/W	0h	Reserved for HW R&D
18	HW_SPARE_REC_HW_SPARE_REC18	R/W	0h	Reserved for HW R&D
17	HW_SPARE_REC_HW_SPARE_REC17	R/W	0h	Reserved for HW R&D
16	HW_SPARE_REC_HW_SPARE_REC16	R/W	0h	Reserved for HW R&D
15	HW_SPARE_REC_HW_SPARE_REC15	R/W	0h	Reserved for HW R&D
14	HW_SPARE_REC_HW_SPARE_REC14	R/W	0h	Reserved for HW R&D
13	HW_SPARE_REC_HW_SPARE_REC13	R/W	0h	Reserved for HW R&D
12	HW_SPARE_REC_HW_SPARE_REC12	R/W	0h	Reserved for HW R&D
11	HW_SPARE_REC_HW_SPARE_REC11	R/W	0h	Reserved for HW R&D
10	HW_SPARE_REC_HW_SPARE_REC10	R/W	0h	Reserved for HW R&D
9	HW_SPARE_REC_HW_SPARE_REC9	R/W	0h	Reserved for HW R&D
8	HW_SPARE_REC_HW_SPARE_REC8	R/W	0h	Reserved for HW R&D
7	HW_SPARE_REC_HW_SPARE_REC7	R/W	0h	Reserved for HW R&D
6	HW_SPARE_REC_HW_SPARE_REC6	R/W	0h	Reserved for HW R&D
5	HW_SPARE_REC_HW_SPARE_REC5	R/W	0h	Reserved for HW R&D
4	HW_SPARE_REC_HW_SPARE_REC4	R/W	0h	Reserved for HW R&D
3	HW_SPARE_REC_HW_SPARE_REC3	R/W	0h	Reserved for HW R&D
2	HW_SPARE_REC_HW_SPARE_REC2	R/W	0h	Reserved for HW R&D
1	HW_SPARE_REC_HW_SPARE_REC1	R/W	0h	Reserved for HW R&D
0	HW_SPARE_REC_HW_SPARE_REC0	R/W	0h	Reserved for HW R&D

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2.2.2.76 TOP_CTRL_LOCK0_KICK0 Register

2.2.2.76.1 TOP_CTRL_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component.

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Table 2-153. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1008h

Figure 2-76. TOP_CTRL_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 2-154. TOP_CTRL_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component

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2.2.2.77 TOP_CTRL_LOCK0_KICK1 Register

2.2.2.77.1 TOP_CTRL_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component.

Return to Summary Table

Table 2-155. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 100Ch

Figure 2-77. TOP_CTRL_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 2-156. TOP_CTRL_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component

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2.2.2.78 TOP_CTRL_INTR_RAW_STATUS Register

2.2.2.78.1 TOP_CTRL_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register.

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Table 2-157. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1010h

Figure 2-78. TOP_CTRL_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 2-158. TOP_CTRL_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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2.2.2.79 TOP_CTRL_INTR_ENABLED_STATUS_CLEAR Register

2.2.2.79.1 TOP_CTRL_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register.

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Table 2-159. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1014h

Figure 2-79. TOP_CTRL_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 2-160. TOP_CTRL_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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2.2.2.80 TOP_CTRL_INTR_ENABLE Register

2.2.2.80.1 TOP_CTRL_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register.

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Table 2-161. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1018h

Figure 2-80. TOP_CTRL_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 2-162. TOP_CTRL_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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2.2.2.81 TOP_CTRL_INTR_ENABLE_CLEAR Register

2.2.2.81.1 TOP_CTRL_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register.

Return to Summary Table

Table 2-163. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 101Ch

Figure 2-81. TOP_CTRL_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 2-164. TOP_CTRL_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

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2.2.2.82 TOP_CTRL_EOI Register

2.2.2.82.1 TOP_CTRL_EOI Register (Offset = 1020h) [reset = 0h]

EOI register.

Return to Summary Table

Table 2-165. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1020h

Figure 2-82. TOP_CTRL_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 2-166. TOP_CTRL_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip.

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2.2.2.83 TOP_CTRL_FAULT_ADDRESS Register

2.2.2.83.1 TOP_CTRL_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register.

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Table 2-167. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1024h

Figure 2-83. TOP_CTRL_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 2-168. TOP_CTRL_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address.

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2.2.2.84 TOP_CTRL_FAULT_TYPE_STATUS Register

2.2.2.84.1 TOP_CTRL_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register.

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Table 2-169. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1028h

Figure 2-84. TOP_CTRL_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 2-170. TOP_CTRL_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access.
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

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2.2.2.85 TOP_CTRL_FAULT_ATTR_STATUS Register

2.2.2.85.1 TOP_CTRL_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register.

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Table 2-171. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 102Ch

Figure 2-85. TOP_CTRL_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID							
R							
0h							

Table 2-172. TOP_CTRL_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID.
19:8	FAULT_ROUTEID	R	0h	Route ID.
7:0	FAULT_PRIVID	R	0h	Privilege ID.

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2.2.2.86 TOP_CTRL_FAULT_CLEAR Register

2.2.2.86.1 TOP_CTRL_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register.

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Table 2-173. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1030h

Figure 2-86. TOP_CTRL_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 2-174. TOP_CTRL_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

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2.3 MSS_CTRL

MSS_CTRL

2.3.1 MSS_CTRL Summaries

MSS_CTRL Summaries

Table 2-175. MSS_CTRL Registers, Base Address=50D0 0000h, Length=131072

Offset	Length	Register Name	MSS_CTRL Physical Address
20h	32	MSS_CTRL_R5SS0_CONTROL	50D0 0020h
24h	32	MSS_CTRL_R5SS0_CORE0_HALT	50D0 0024h
28h	32	MSS_CTRL_R5SS0_CORE1_HALT	50D0 0028h
2Ch	32	MSS_CTRL_R5SS0_STATUS_REG	50D0 002Ch
30h	32	MSS_CTRL_R5SS0_CORE0_STAT	50D0 0030h
34h	32	MSS_CTRL_R5SS0_CORE1_STAT	50D0 0034h
38h	32	MSS_CTRL_R5SS0_FORCE_WFI	50D0 0038h
40h	32	MSS_CTRL_R5SS1_CONTROL	50D0 0040h
44h	32	MSS_CTRL_R5SS1_CORE0_HALT	50D0 0044h
48h	32	MSS_CTRL_R5SS1_CORE1_HALT	50D0 0048h
4Ch	32	MSS_CTRL_R5SS1_STATUS_REG	50D0 004Ch
50h	32	MSS_CTRL_R5SS1_CORE0_STAT	50D0 0050h
54h	32	MSS_CTRL_R5SS1_CORE1_STAT	50D0 0054h
58h	32	MSS_CTRL_R5SS1_FORCE_WFI	50D0 0058h
80h	32	MSS_CTRL_R5SS0_ROM_ECLIPSE	50D0 0080h
200h	32	MSS_CTRL_R5SS0_ATCM_MEM_INIT	50D0 0200h
204h	32	MSS_CTRL_R5SS0_ATCM_MEM_INIT_DONE	50D0 0204h
208h	32	MSS_CTRL_R5SS0_ATCM_MEM_INIT_STATUS	50D0 0208h
210h	32	MSS_CTRL_R5SS0_BTCM_MEM_INIT	50D0 0210h
214h	32	MSS_CTRL_R5SS0_BTCM_MEM_INIT_DONE	50D0 0214h
218h	32	MSS_CTRL_R5SS0_BTCM_MEM_INIT_STATUS	50D0 0218h
220h	32	MSS_CTRL_R5SS1_ATCM_MEM_INIT	50D0 0220h
224h	32	MSS_CTRL_R5SS1_ATCM_MEM_INIT_DONE	50D0 0224h
228h	32	MSS_CTRL_R5SS1_ATCM_MEM_INIT_STATUS	50D0 0228h
230h	32	MSS_CTRL_R5SS1_BTCM_MEM_INIT	50D0 0230h
234h	32	MSS_CTRL_R5SS1_BTCM_MEM_INIT_DONE	50D0 0234h
238h	32	MSS_CTRL_R5SS1_BTCM_MEM_INIT_STATUS	50D0 0238h
240h	32	MSS_CTRL_L2IOCRAM_MEM_INIT	50D0 0240h
244h	32	MSS_CTRL_L2IOCRAM_MEM_INIT_DONE	50D0 0244h
248h	32	MSS_CTRL_L2IOCRAM_MEM_INIT_STATUS	50D0 0248h
250h	32	MSS_CTRL_MAILBOXRAM_MEM_INIT	50D0 0250h
254h	32	MSS_CTRL_MAILBOXRAM_MEM_INIT_DONE	50D0 0254h
258h	32	MSS_CTRL_MAILBOXRAM_MEM_INIT_STATUS	50D0 0258h
260h	32	MSS_CTRL_TPCC_MEM_INIT	50D0 0260h
264h	32	MSS_CTRL_TPCC_MEM_INIT_DONE	50D0 0264h
268h	32	MSS_CTRL_TPCC_MEMINIT_STATUS	50D0 0268h
300h	32	MSS_CTRL_TOP_PBIST_KEY_RST	50D0 0300h
400h	32	MSS_CTRL_R5SS0_CTI_TRIG_SEL	50D0 0400h
404h	32	MSS_CTRL_R5SS1_CTI_TRIG_SEL	50D0 0404h
408h	32	MSS_CTRL_DBGSS_CTI_TRIG_SEL	50D0 0408h

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Table 2-175. MSS_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)

Offset	Length	Register Name	MSS_CTRL Physical Address
420h	32	MSS_CTRL_MCAN0_HALTEN	50D0 0420h
424h	32	MSS_CTRL_MCAN1_HALTEN	50D0 0424h
428h	32	MSS_CTRL_MCAN2_HALTEN	50D0 0428h
42Ch	32	MSS_CTRL_MCAN3_HALTEN	50D0 042Ch
430h	32	MSS_CTRL_LIN0_HALTEN	50D0 0430h
434h	32	MSS_CTRL_LIN1_HALTEN	50D0 0434h
438h	32	MSS_CTRL_LIN2_HALTEN	50D0 0438h
43Ch	32	MSS_CTRL_LIN3_HALTEN	50D0 043Ch
440h	32	MSS_CTRL_LIN4_HALTEN	50D0 0440h
444h	32	MSS_CTRL_I2C0_HALTEN	50D0 0444h
448h	32	MSS_CTRL_I2C1_HALTEN	50D0 0448h
44Ch	32	MSS_CTRL_I2C2_HALTEN	50D0 044Ch
450h	32	MSS_CTRL_I2C3_HALTEN	50D0 0450h
454h	32	MSS_CTRL_RTI0_HALTEN	50D0 0454h
458h	32	MSS_CTRL_RTI1_HALTEN	50D0 0458h
45Ch	32	MSS_CTRL_RTI2_HALTEN	50D0 045Ch
460h	32	MSS_CTRL_RTI3_HALTEN	50D0 0460h
474h	32	MSS_CTRL_CPSW_HALTEN	50D0 0474h
478h	32	MSS_CTRL_MCRC0_HALTEN	50D0 0478h
47Ch	32	MSS_CTRL_MCAN4_HALTEN	50D0 047Ch
480h	32	MSS_CTRL_MCAN5_HALTEN	50D0 0480h
484h	32	MSS_CTRL_MCAN6_HALTEN	50D0 0484h
488h	32	MSS_CTRL_MCAN7_HALTEN	50D0 0488h
48Ch	32	MSS_CTRL_RTI4_HALTEN	50D0 048Ch
490h	32	MSS_CTRL_RTI5_HALTEN	50D0 0490h
494h	32	MSS_CTRL_RTI6_HALTEN	50D0 0494h
498h	32	MSS_CTRL_RTI7_HALTEN	50D0 0498h
800h	32	MSS_CTRL_TPTC_DBS_CONFIG	50D0 0800h
804h	32	MSS_CTRL_TPTC_BOUNDARY_CFG	50D0 0804h
808h	32	MSS_CTRL_TPTC_XID_REORDER_CFG	50D0 0808h
810h	32	MSS_CTRL_CPSW_CONTROL	50D0 0810h
814h	32	MSS_CTRL_OSPI_CONFIG	50D0 0814h
818h	32	MSS_CTRL_PRU_ICSS_IDLE_CONTROL	50D0 0818h
81Ch	32	MSS_CTRL_PRU_ICSS_PRU0_GPI_SEL	50D0 081Ch
820h	32	MSS_CTRL_PRU_ICSS_PRU1_GPI_SEL	50D0 0820h
824h	32	MSS_CTRL_PRU_ICSS_PRU0_GPIO_OUT_CTRL	50D0 0824h
828h	32	MSS_CTRL_PRU_ICSS_PRU1_GPIO_OUT_CTRL	50D0 0828h
830h	32	MSS_CTRL_TPCC0_INTAGG_MASK	50D0 0830h
834h	32	MSS_CTRL_TPCC0_INTAGG_STATUS	50D0 0834h
838h	32	MSS_CTRL_TPCC0_INTAGG_STATUS_RAW	50D0 0838h
83Ch	32	MSS_CTRL_INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL	50D0 083Ch
840h	32	MSS_CTRL_OSPI_BOOT_CONFIG_MASK	50D0 0840h
844h	32	MSS_CTRL_OSPI_BOOT_CONFIG_SEG	50D0 0844h
848h	32	MSS_CTRL_PRU_ICSS_RX_ERR_COUNTER	50D0 0848h
84Ch	32	MSS_CTRL_PRU_ICSS_RX_ERR_COUNTER_CLR	50D0 084Ch
1008h	32	MSS_CTRL_LOCK0_KICK0	50D0 1008h

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Table 2-175. MSS_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)

Offset	Length	Register Name	MSS_CTRL Physical Address
100Ch	32	MSS_CTRL_LOCK0_KICK1	50D0 100Ch
1010h	32	MSS_CTRL_INTR_RAW_STATUS	50D0 1010h
1014h	32	MSS_CTRL_INTR_ENABLED_STATUS_CLEAR	50D0 1014h
1018h	32	MSS_CTRL_INTR_ENABLE	50D0 1018h
101Ch	32	MSS_CTRL_INTR_ENABLE_CLEAR	50D0 101Ch
1020h	32	MSS_CTRL_EOI	50D0 1020h
1024h	32	MSS_CTRL_FAULT_ADDRESS	50D0 1024h
1028h	32	MSS_CTRL_FAULT_TYPE_STATUS	50D0 1028h
102Ch	32	MSS_CTRL_FAULT_ATTR_STATUS	50D0 102Ch
1030h	32	MSS_CTRL_FAULT_CLEAR	50D0 1030h
4000h	32	MSS_CTRL_R5SS0_CORE0_MBOX_WRITE_DONE	50D0 4000h
4004h	32	MSS_CTRL_R5SS0_CORE0_MBOX_READ_REQ	50D0 4004h
4008h	32	MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE_ACK	50D0 4008h
400Ch	32	MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE	50D0 400Ch
4010h	32	MSS_CTRL_R5SS0_CORE0_SW_INT	50D0 4010h
4020h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_MASK	50D0 4020h
4024h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS	50D0 4024h
4028h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS_RAW	50D0 4028h
4030h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_MASK	50D0 4030h
4034h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS	50D0 4034h
4038h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS_RAW	50D0 4038h
8000h	32	MSS_CTRL_R5SS0_CORE1_MBOX_WRITE_DONE	50D0 8000h
8004h	32	MSS_CTRL_R5SS0_CORE1_MBOX_READ_REQ	50D0 8004h
8008h	32	MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE_ACK	50D0 8008h
800Ch	32	MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE	50D0 800Ch
8010h	32	MSS_CTRL_R5SS0_CORE1_SW_INT	50D0 8010h
8020h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_MASK	50D0 8020h
8024h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS	50D0 8024h
8028h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS_RAW	50D0 8028h
8030h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_MASK	50D0 8030h
8034h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS	50D0 8034h
8038h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS_RAW	50D0 8038h
C000h	32	MSS_CTRL_R5SS1_CORE0_MBOX_WRITE_DONE	50D0 C000h
C004h	32	MSS_CTRL_R5SS1_CORE0_MBOX_READ_REQ	50D0 C004h
C008h	32	MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE_ACK	50D0 C008h
C00Ch	32	MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE	50D0 C00Ch
C010h	32	MSS_CTRL_R5SS1_CORE0_SW_INT	50D0 C010h
C020h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_MASK	50D0 C020h

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Table 2-175. MSS_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)

Offset	Length	Register Name	MSS_CTRL Physical Address
C024h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS	50D0 C024h
C028h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS_RAW	50D0 C028h
C030h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_MASK	50D0 C030h
C034h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS	50D0 C034h
C038h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS_RAW	50D0 C038h
10000h	32	MSS_CTRL_R5SS1_CORE1_MBOX_WRITE_DONE	50D1 0000h
10004h	32	MSS_CTRL_R5SS1_CORE1_MBOX_READ_REQ	50D1 0004h
10008h	32	MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE_ACK	50D1 0008h
1000Ch	32	MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE	50D1 000Ch
10010h	32	MSS_CTRL_R5SS1_CORE1_SW_INT	50D1 0010h
10020h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_MASK	50D1 0020h
10024h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS	50D1 0024h
10028h	32	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS_RAW	50D1 0028h
10030h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_MASK	50D1 0030h
10034h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS	50D1 0034h
10038h	32	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS_RAW	50D1 0038h
14000h	32	MSS_CTRL_PRU_ICSS_PRU0_MBOX_WRITE_DONE	50D1 4000h
14004h	32	MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_REQ	50D1 4004h
14008h	32	MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE_ACK	50D1 4008h
1400Ch	32	MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE	50D1 400Ch
14010h	32	MSS_CTRL_PRU_ICSS_PRU1_MBOX_WRITE_DONE	50D1 4010h
14014h	32	MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_REQ	50D1 4014h
14018h	32	MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE_ACK	50D1 4018h
1401Ch	32	MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE	50D1 401Ch
18000h	32	MSS_CTRL_TPCC0_ERRAGG_MASK	50D1 8000h
18004h	32	MSS_CTRL_TPCC0_ERRAGG_STATUS	50D1 8004h
18008h	32	MSS_CTRL_TPCC0_ERRAGG_STATUS_RAW	50D1 8008h
18010h	32	MSS_CTRL_MMR_ACCESS_ERRAGG_MASK0	50D1 8010h
18014h	32	MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS0	50D1 8014h
18018h	32	MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS_RAW0	50D1 8018h
18080h	32	MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_MASK	50D1 8080h
18084h	32	MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS	50D1 8084h
18088h	32	MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS_RAW	50D1 8088h
18090h	32	MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_MASK	50D1 8090h

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Table 2-175. MSS_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)

Offset	Length	Register Name	MSS_CTRL Physical Address
18094h	32	MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS	50D1 8094h
18098h	32	MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 8098h
180A0h	32	MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_MASK	50D1 80A0h
180A4h	32	MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS	50D1 80A4h
180A8h	32	MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS_RAW	50D1 80A8h
180B0h	32	MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_MASK	50D1 80B0h
180B4h	32	MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS	50D1 80B4h
180B8h	32	MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 80B8h
180C0h	32	MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_MASK	50D1 80C0h
180C4h	32	MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS	50D1 80C4h
180C8h	32	MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS_RAW	50D1 80C8h
180D0h	32	MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_MASK	50D1 80D0h
180D4h	32	MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS	50D1 80D4h
180D8h	32	MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 80D8h
180E0h	32	MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_MASK	50D1 80E0h
180E4h	32	MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS	50D1 80E4h
180E8h	32	MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS_RAW	50D1 80E8h
180F0h	32	MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_MASK	50D1 80F0h
180F4h	32	MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS	50D1 80F4h
180F8h	32	MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 80F8h
18100h	32	MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8100h
18104h	32	MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8104h
18108h	32	MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8108h
18110h	32	MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8110h
18114h	32	MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8114h
18118h	32	MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8118h
18120h	32	MSS_CTRL_R5SS0_TCM_ADDRPARITY_CLR	50D1 8120h
18124h	32	MSS_CTRL_R5SS0_CORE0_ADDRPARITY_ERR_ATCM	50D1 8124h
18128h	32	MSS_CTRL_R5SS0_CORE1_ADDRPARITY_ERR_ATCM	50D1 8128h

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Table 2-175. MSS_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)

Offset	Length	Register Name	MSS_CTRL Physical Address
1812Ch	32	MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B0TCM	50D1 812Ch
18130h	32	MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B0TCM	50D1 8130h
18134h	32	MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B1TCM	50D1 8134h
18138h	32	MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B1TCM	50D1 8138h
1813Ch	32	MSS_CTRL_R5SS0_TCM_ADDRPARITY_ERRFORCE	50D1 813Ch
18140h	32	MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8140h
18144h	32	MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8144h
18148h	32	MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8148h
18150h	32	MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8150h
18154h	32	MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8154h
18158h	32	MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8158h
18160h	32	MSS_CTRL_R5SS1_TCM_ADDRPARITY_CLR	50D1 8160h
18164h	32	MSS_CTRL_R5SS1_CORE0_ADDRPARITY_ERR_ATCM	50D1 8164h
18168h	32	MSS_CTRL_R5SS1_CORE1_ADDRPARITY_ERR_ATCM	50D1 8168h
1816Ch	32	MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B0TCM	50D1 816Ch
18170h	32	MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B0TCM	50D1 8170h
18174h	32	MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B1TCM	50D1 8174h
18178h	32	MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B1TCM	50D1 8178h
1817Ch	32	MSS_CTRL_R5SS1_TCM_ADDRPARITY_ERRFORCE	50D1 817Ch
18180h	32	MSS_CTRL_TPCC0_PARITY_CTRL	50D1 8180h
18184h	32	MSS_CTRL_TPCC0_PARITY_STATUS	50D1 8184h
18188h	32	MSS_CTRL_TMU_R5SS0_CORE0_ROM_PARITY_CTRL	50D1 8188h
1818Ch	32	MSS_CTRL_TMU_R5SS0_CORE0_ROM_PARITY_STATUS	50D1 818Ch
18190h	32	MSS_CTRL_TMU_R5SS0_CORE1_ROM_PARITY_CTRL	50D1 8190h
18194h	32	MSS_CTRL_TMU_R5SS0_CORE1_ROM_PARITY_STATUS	50D1 8194h
18198h	32	MSS_CTRL_TMU_R5SS1_CORE0_ROM_PARITY_CTRL	50D1 8198h
1819Ch	32	MSS_CTRL_TMU_R5SS1_CORE0_ROM_PARITY_STATUS	50D1 819Ch
181A0h	32	MSS_CTRL_TMU_R5SS1_CORE1_ROM_PARITY_CTRL	50D1 81A0h
181A4h	32	MSS_CTRL_TMU_R5SS1_CORE1_ROM_PARITY_STATUS	50D1 81A4h
184A0h	32	MSS_CTRL_OSPI0_BUS_SAFETY_CTRL	50D1 84A0h
184A4h	32	MSS_CTRL_OSPI0_BUS_SAFETY_FI	50D1 84A4h
184A8h	32	MSS_CTRL_OSPI0_BUS_SAFETY_ERR	50D1 84A8h
184ACh	32	MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_DATA0	50D1 84ACh
184B0h	32	MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_CMD	50D1 84B0h
184B4h	32	MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_WRITE	50D1 84B4h
184B8h	32	MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_READ	50D1 84B8h
184BCh	32	MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 84BCh
18880h	32	MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_CTRL	50D1 8880h
18884h	32	MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_FI	50D1 8884h

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Table 2-175. MSS_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)

Offset	Length	Register Name	MSS_CTRL Physical Address
18888h	32	MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR	50D1 8888h
1888Ch	32	MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_DATA0	50D1 888Ch
18890h	32	MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_CMD	50D1 8890h
18894h	32	MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITE	50D1 8894h
18898h	32	MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_READ	50D1 8898h
1889Ch	32	MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 889Ch
188A0h	32	MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_CTRL	50D1 88A0h
188A4h	32	MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_FI	50D1 88A4h
188A8h	32	MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR	50D1 88A8h
188ACh	32	MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_DATA0	50D1 88ACh
188B0h	32	MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_CMD	50D1 88B0h
188B4h	32	MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITE	50D1 88B4h
188B8h	32	MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_READ	50D1 88B8h
188BCh	32	MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITERESP	50D1 88BCh

2.3.2 MSS_CTRL Registers

MSS_CTRL Registers

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2.3.2.1 MSS_CTRL_R5SS0_CONTROL Register

2.3.2.1.1 MSS_CTRL_R5SS0_CONTROL Register (Offset = 20h) [reset = 707h]

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Table 2-176. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0020h

Figure 2-87. MSS_CTRL_R5SS0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED					R5SS0_CONTROL_ROM_WAIT_STATE		
NONE					R/W		
0h					0h		
23	22	21	20	19	18	17	16
RESERVED					R5SS0_CONTROL_RESET_FSM_TRIGGER		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED					R5SS0_CONTROL_LOCK_STEP_SWITCH_WAIT		
NONE					R/W		
0h					7h		
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CONTROL_LOCK_STEP		
NONE					R/W		
0h					7h		

Table 2-177. MSS_CTRL_R5SS0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	R5SS0_CONTROL_ROM_WAIT_STATE	R/W	0h	Writing 3'b111 enables a single cycle wait state with respect to CR5A_clk for rom access. This needs to be set when R5 clock is at 400MHZ and Interconnect-clk is at 200MHZ. [because it is a timing issue in this scenario]
23:19	RESERVED	NONE	0h	Reserved
18:16	R5SS0_CONTROL_RESET_FSM_TRIGGER	R/W	0h	Write pulse bit field: Writing 3'b111 will trigger the reset FSM. Reset FSM ensures reset to R5SS and inturn ensures the latching of lock_step and also mem_swap bit
15:11	RESERVED	NONE	0h	Reserved
10:8	R5SS0_CONTROL_LOCK_STEP_SWITCH_WAIT	R/W	7h	Writing 3'b111 ensures switch happens only after R5SS reset. Orelse it will be a immediate switch.
7:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CONTROL_LOCK_STEP	R/W	7h	Writing 3'b000 ensures R5 to be in Dual-Core mode. Note: The change happens after the R5SS reset assertion if corresponding R5SS_CONTROL_LOCK_STEP_SWITCH_WAIT is set. Or else the switching to Dual-core happens on the fly.

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2.3.2.2 MSS_CTRL_R5SS0_CORE0_HALT Register

2.3.2.2.1 MSS_CTRL_R5SS0_CORE0_HALT Register (Offset = 24h) [reset = 7h]

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Table 2-178. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0024h

Figure 2-88. MSS_CTRL_R5SS0_CORE0_HALT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CORE0_HALT_HALT		
NONE					R/W		
0h					7h		

Table 2-179. MSS_CTRL_R5SS0_CORE0_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CORE0_HALT_HALT	R/W	7h	Writing 3'b000 will unhalt CR5A. This register should be written only once.

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2.3.2.3 MSS_CTRL_R5SS0_CORE1_HALT Register

2.3.2.3.1 MSS_CTRL_R5SS0_CORE1_HALT Register (Offset = 28h) [reset = 7h]

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Table 2-180. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0028h

Figure 2-89. MSS_CTRL_R5SS0_CORE1_HALT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CORE1_HALT_HALT		
NONE					R/W		
0h					7h		

Table 2-181. MSS_CTRL_R5SS0_CORE1_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CORE1_HALT_HALT	R/W	7h	Writing 3'b000 will unhalt for CR5B. This register should be written only once.

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2.3.2.4 MSS_CTRL_R5SS0_STATUS_REG Register

2.3.2.4.1 MSS_CTRL_R5SS0_STATUS_REG Register (Offset = 2Ch) [reset = 0h]

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Table 2-182. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 002Ch

Figure 2-90. MSS_CTRL_R5SS0_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							R5SS0_STATUS_REG_LOCK_STEP
NONE							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED							R5SS0_STATUS_REG_MEMSWAP
NONE							R
0h							0h

Table 2-183. MSS_CTRL_R5SS0_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	R5SS0_STATUS_REG_LOCK_STEP	R	0h	Reading 1:confirms R5SS is in lockstep mode. Reading 0:confirms R5SS is in Dual-core mode.
7:1	RESERVED	NONE	0h	Reserved
0	R5SS0_STATUS_REG_MEMSWAP	R	0h	Reading 1:confirms ROM is Eclipsed from with RAM for R5.

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2.3.2.5 MSS_CTRL_R5SS0_CORE0_STAT Register

2.3.2.5.1 MSS_CTRL_R5SS0_CORE0_STAT Register (Offset = 30h) [reset = 0h]

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Table 2-184. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0030h

Figure 2-91. MSS_CTRL_R5SS0_CORE0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			R5SS0_CORE0_STAT_WFE_STAT	RESERVED			R5SS0_CORE0_STAT_WFI_STAT
NONE			R	NONE			R
0h			0h	0h			0h

Table 2-185. MSS_CTRL_R5SS0_CORE0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CORE0_STAT_WFE_STAT	R	0h	WFE Status
3:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CORE0_STAT_WFI_STAT	R	0h	WFI Status

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2.3.2.6 MSS_CTRL_R5SS0_CORE1_STAT Register

2.3.2.6.1 MSS_CTRL_R5SS0_CORE1_STAT Register (Offset = 34h) [reset = 0h]

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Table 2-186. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0034h

Figure 2-92. MSS_CTRL_R5SS0_CORE1_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS0_CORE1_STAT_WFE_STAT	RESERVED			R5SS0_CORE1_STAT_WFI_STAT
NONE			R	NONE			R
0h			0h	0h			0h

Table 2-187. MSS_CTRL_R5SS0_CORE1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CORE1_STAT_WFE_STAT	R	0h	WFE Status
3:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CORE1_STAT_WFI_STAT	R	0h	WFI Status

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2.3.2.7 MSS_CTRL_R5SS0_FORCE_WFI Register

2.3.2.7.1 MSS_CTRL_R5SS0_FORCE_WFI Register (Offset = 38h) [reset = 0h]

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Table 2-188. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0038h

Figure 2-93. MSS_CTRL_R5SS0_FORCE_WFI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_FORCE_WFI_CR5_WFI_OVERIDE		
NONE					R/W		
0h					0h		

Table 2-189. MSS_CTRL_R5SS0_FORCE_WFI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_FORCE_WFI_CR5_WFI_OVERIDE	R/W	0h	Writing 3'b111 will force the wfi signals of R5SS to 1

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2.3.2.8 MSS_CTRL_R5SS1_CONTROL Register

2.3.2.8.1 MSS_CTRL_R5SS1_CONTROL Register (Offset = 40h) [reset = 707h]

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Table 2-190. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0040h

Figure 2-94. MSS_CTRL_R5SS1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					R5SS1_CONTROL_RESET_FSM_TRIGGER		
NONE					R/W		
0h					0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					R5SS1_CONTROL_LOCK_STEP_SWITCH_WAIT		
NONE					R/W		
0h					7h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS1_CONTROL_LOCK_STEP		
NONE					R/W		
0h					7h		

Table 2-191. MSS_CTRL_R5SS1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	R5SS1_CONTROL_RESET_FSM_TRIGGER	R/W	0h	Write pulse bit field: Writing 3'b111 will trigger the reset FSM. Reset FSM ensures reset to R5SS and inturn ensures the latching of lock_step and also mem_swap bit
15:11	RESERVED	NONE	0h	Reserved
10:8	R5SS1_CONTROL_LOCK_STEP_SWITCH_WAIT	R/W	7h	Writing 3'b111 ensures switch happens only after R5SS reset. Orelse it will be a immediate switch.
7:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CONTROL_LOCK_STEP	R/W	7h	Writing 3'b000 ensures R5 to be in Dual-Core mode. Note: The change happens after the R5SS reset assertion if corresponding R5SS_CONTROL_LOCK_STEP_SWITCH_WAIT is set. Or else the switching to Dual-core happens on the fly.

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2.3.2.9 MSS_CTRL_R5SS1_CORE0_HALT Register

2.3.2.9.1 MSS_CTRL_R5SS1_CORE0_HALT Register (Offset = 44h) [reset = 7h]

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Table 2-192. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0044h

Figure 2-95. MSS_CTRL_R5SS1_CORE0_HALT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CORE0_HALT_HALT		
NONE					R/W		
0h					7h		

Table 2-193. MSS_CTRL_R5SS1_CORE0_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CORE0_HALT_HALT	R/W	7h	Writing 3'b000 will unhalt CR5A. This register should be written only once.

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2.3.2.10 MSS_CTRL_R5SS1_CORE1_HALT Register

2.3.2.10.1 MSS_CTRL_R5SS1_CORE1_HALT Register (Offset = 48h) [reset = 7h]

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Table 2-194. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0048h

Figure 2-96. MSS_CTRL_R5SS1_CORE1_HALT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CORE1_HALT_HALT		
NONE					R/W		
0h					7h		

Table 2-195. MSS_CTRL_R5SS1_CORE1_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CORE1_HALT_HALT	R/W	7h	Writing 3'b000 will unhalt for CR5B. This register should be written only once.

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2.3.2.11 MSS_CTRL_R5SS1_STATUS_REG Register

2.3.2.11.1 MSS_CTRL_R5SS1_STATUS_REG Register (Offset = 4Ch) [reset = 0h]

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Table 2-196. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 004Ch

Figure 2-97. MSS_CTRL_R5SS1_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							R5SS1_STATUS_REG_LOCK_STEP
NONE							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 2-197. MSS_CTRL_R5SS1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	R5SS1_STATUS_REG_LOCK_STEP	R	0h	Reading 1:confirms R5SS is in lockstep mode. Reading 0:confirms R5SS is in Dual-core mode.
7:0	RESERVED	NONE	0h	Reserved

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2.3.2.12 MSS_CTRL_R5SS1_CORE0_STAT Register

2.3.2.12.1 MSS_CTRL_R5SS1_CORE0_STAT Register (Offset = 50h) [reset = 0h]

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Table 2-198. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0050h

Figure 2-98. MSS_CTRL_R5SS1_CORE0_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS1_CORE0_STAT_WFE_STAT	RESERVED			R5SS1_CORE0_STAT_WFI_STAT
NONE			R	NONE			R
0h			0h	0h			0h

Table 2-199. MSS_CTRL_R5SS1_CORE0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CORE0_STAT_WFE_STAT	R	0h	WFE Status
3:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CORE0_STAT_WFI_STAT	R	0h	WFI Status

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2.3.2.13 MSS_CTRL_R5SS1_CORE1_STAT Register

2.3.2.13.1 MSS_CTRL_R5SS1_CORE1_STAT Register (Offset = 54h) [reset = 0h]

Return to Summary Table

Table 2-200. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0054h

Figure 2-99. MSS_CTRL_R5SS1_CORE1_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			R5SS1_CORE1_STAT_WFE_STAT	RESERVED			R5SS1_CORE1_STAT_WFI_STAT
NONE			R	NONE			R
0h			0h	0h			0h

Table 2-201. MSS_CTRL_R5SS1_CORE1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CORE1_STAT_WFE_STAT	R	0h	WFE Status
3:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CORE1_STAT_WFI_STAT	R	0h	WFI Status

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2.3.2.14 MSS_CTRL_R5SS1_FORCE_WFI Register

2.3.2.14.1 MSS_CTRL_R5SS1_FORCE_WFI Register (Offset = 58h) [reset = 0h]

Return to Summary Table

Table 2-202. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0058h

Figure 2-100. MSS_CTRL_R5SS1_FORCE_WFI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_FORCE_WFI_CR5_WFI_OVERIDE		
NONE					R/W		
0h					0h		

Table 2-203. MSS_CTRL_R5SS1_FORCE_WFI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_FORCE_WFI_CR5_WFI_OVERIDE	R/W	0h	Writing 3'b111 will force the wfi signals of R5SS to 1

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2.3.2.15 MSS_CTRL_R5SS0_ROM_ECLIPSE Register

2.3.2.15.1 MSS_CTRL_R5SS0_ROM_ECLIPSE Register (Offset = 80h) [reset = 700h]

Return to Summary Table

Table 2-204. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0080h

Figure 2-101. MSS_CTRL_R5SS0_ROM_ECLIPSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					R5SS0_ROM_ECLIPSE_MEMSWAP_WAIT		
NONE					R/W		
0h					7h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS0_ROM_ECLIPSE_MEMSWAP		
NONE					R/W		
0h					0h		

Table 2-205. MSS_CTRL_R5SS0_ROM_ECLIPSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	R5SS0_ROM_ECLIPSE_MEMSWAP_WAIT	R/W	7h	Writing 3'b111 ensures ROM-Eclipsing happens only after R5SS reset. Or else it will be a immediate change.
7:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_ROM_ECLIPSE_MEMSWAP	R/W	0h	Writing 3'b111 ensures eclipsing of CR5A_ROM immediately if memswap_wait is not set. If memswap_wait is set then ROM is eclipsed after R5SS reset assertion.

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2.3.2.16 MSS_CTRL_R5SS0_ATCM_MEM_INIT Register

2.3.2.16.1 MSS_CTRL_R5SS0_ATCM_MEM_INIT Register (Offset = 200h) [reset = 0h]

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Table 2-206. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0200h

Figure 2-102. MSS_CTRL_R5SS0_ATCM_MEM_INIT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS0_ATCM_MEM_INIT_MEM_INIT
NONE							R/W
0h							0h

Table 2-207. MSS_CTRL_R5SS0_ATCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS0_ATCM_MEM_INIT_MEM_INIT	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the ATCM banks of CR5A/B. Value in each row is initialized to 0x0C_0000_0000

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2.3.2.17 MSS_CTRL_R5SS0_ATCM_MEM_INIT_DONE Register

2.3.2.17.1 MSS_CTRL_R5SS0_ATCM_MEM_INIT_DONE Register (Offset = 204h) [reset = 0h]

Return to Summary Table

Table 2-208. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0204h

Figure 2-103. MSS_CTRL_R5SS0_ATCM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS0_ATCM_MEM_INIT_DONE_MEM_INIT_DONE
NONE							R/W
0h							0h

Table 2-209. MSS_CTRL_R5SS0_ATCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS0_ATCM_MEM_INIT_DONE_MEM_INIT_DONE	R/W	0h	This field will be high once initialization of ATCM banks is finished. Writing '1' would clear the bit.

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2.3.2.18 MSS_CTRL_R5SS0_ATCM_MEM_INIT_STATUS Register

2.3.2.18.1 MSS_CTRL_R5SS0_ATCM_MEM_INIT_STATUS Register (Offset = 208h) [reset = 0h]

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Table 2-210. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0208h

Figure 2-104. MSS_CTRL_R5SS0_ATCM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS0_ATCM_MEM_INIT_STATUS_MEM_STATUS
NONE							R
0h							0h

Table 2-211. MSS_CTRL_R5SS0_ATCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS0_ATCM_MEM_INIT_STATUS_MEM_STATUS	R	0h	1'b0: No initialization is happening for ATCM banks of CR5A/B 1'b1: Initialization is in progress for ATCM banks of CR5A/B

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2.3.2.19 MSS_CTRL_R5SS0_BTCM_MEM_INIT Register

2.3.2.19.1 MSS_CTRL_R5SS0_BTCM_MEM_INIT Register (Offset = 210h) [reset = 0h]

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Table 2-212. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0210h

Figure 2-105. MSS_CTRL_R5SS0_BTCM_MEM_INIT Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>R5SS0_BTCM_MEM_INIT_MEM_INIT</td></tr>
<tr><td colspan="7">NONE</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 2-213. MSS_CTRL_R5SS0_BTCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS0_BTCM_MEM_INIT_MEM_INIT	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the B0/1TCM banks of CR5A/B

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2.3.2.20 MSS_CTRL_R5SS0_BTCM_MEM_INIT_DONE Register

2.3.2.20.1 MSS_CTRL_R5SS0_BTCM_MEM_INIT_DONE Register (Offset = 214h) [reset = 0h]

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Table 2-214. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0214h

Figure 2-106. MSS_CTRL_R5SS0_BTCM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							R5SS0_BTCM_MEM_INIT_DONE_MEM_INIT_DONE
NONE							R/W
0h							0h

Table 2-215. MSS_CTRL_R5SS0_BTCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS0_BTCM_MEM_INIT_DONE_MEM_INIT_DONE	R/W	0h	This field will be high once initialization of B0/1TCM banks is finished. Writing '1' would clear the bit.

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2.3.2.21 MSS_CTRL_R5SS0_BTCM_MEM_INIT_STATUS Register

2.3.2.21.1 MSS_CTRL_R5SS0_BTCM_MEM_INIT_STATUS Register (Offset = 218h) [reset = 0h]

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Table 2-216. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0218h

Figure 2-107. MSS_CTRL_R5SS0_BTCM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS0_BTCM_MEM_INIT_STATUS_MEM_STATUS
NONE							R
0h							0h

Table 2-217. MSS_CTRL_R5SS0_BTCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS0_BTCM_MEM_INIT_STATUS_MEM_STATUS	R	0h	1'b0: No initialization is happening for B0/1TCM banks of CR5A/B 1'b1: Initialization is in progress for B0/1TCM banks of CR5A/B

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2.3.2.22 MSS_CTRL_R5SS1_ATCM_MEM_INIT Register

2.3.2.22.1 MSS_CTRL_R5SS1_ATCM_MEM_INIT Register (Offset = 220h) [reset = 0h]

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Table 2-218. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0220h

Figure 2-108. MSS_CTRL_R5SS1_ATCM_MEM_INIT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS1_ATCM_MEM_INIT_MEM_INIT
NONE							R/W
0h							0h

Table 2-219. MSS_CTRL_R5SS1_ATCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS1_ATCM_MEM_INIT_MEM_INIT	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the ATCM banks of CR5A/B. Value in each row is initialized to 0x0C_0000_0000

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2.3.2.23 MSS_CTRL_R5SS1_ATCM_MEM_INIT_DONE Register

2.3.2.23.1 MSS_CTRL_R5SS1_ATCM_MEM_INIT_DONE Register (Offset = 224h) [reset = 0h]

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Table 2-220. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0224h

Figure 2-109. MSS_CTRL_R5SS1_ATCM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							R5SS1_ATCM_MEM_INIT_DONE_MEM_INIT_DONE
NONE							R/W
0h							0h

Table 2-221. MSS_CTRL_R5SS1_ATCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS1_ATCM_MEM_INIT_DONE_MEM_INIT_DONE	R/W	0h	This field will be high once initialization of ATCM banks is finished. Writing '1' would clear the bit.

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2.3.2.24 MSS_CTRL_R5SS1_ATCM_MEM_INIT_STATUS Register

2.3.2.24.1 MSS_CTRL_R5SS1_ATCM_MEM_INIT_STATUS Register (Offset = 228h) [reset = 0h]

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Table 2-222. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0228h

Figure 2-110. MSS_CTRL_R5SS1_ATCM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS1_ATCM_MEM_INIT_STATUS_MEM_STATUS
NONE							R
0h							0h

Table 2-223. MSS_CTRL_R5SS1_ATCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS1_ATCM_MEM_INIT_STATUS_MEM_STATUS	R	0h	1'b0: No initialization is happening for ATCM banks of CR5A/B 1'b1: Initialization is in progress for ATCM banks of CR5A/B

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2.3.2.25 MSS_CTRL_R5SS1_BTCM_MEM_INIT Register

2.3.2.25.1 MSS_CTRL_R5SS1_BTCM_MEM_INIT Register (Offset = 230h) [reset = 0h]

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Table 2-224. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0230h

Figure 2-111. MSS_CTRL_R5SS1_BTCM_MEM_INIT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							R5SS1_BTCM_MEM_INIT_MEM_INIT
NONE							R/W
0h							0h

Table 2-225. MSS_CTRL_R5SS1_BTCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS1_BTCM_MEM_INIT_MEM_INIT	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the B0/1TCM banks of CR5A/B

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2.3.2.26 MSS_CTRL_R5SS1_BTCM_MEM_INIT_DONE Register

2.3.2.26.1 MSS_CTRL_R5SS1_BTCM_MEM_INIT_DONE Register (Offset = 234h) [reset = 0h]

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Table 2-226. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0234h

Figure 2-112. MSS_CTRL_R5SS1_BTCM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS1_BTCM_MEM_INIT_DONE_MEM_INIT_DONE
NONE							R/W
0h							0h

Table 2-227. MSS_CTRL_R5SS1_BTCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS1_BTCM_MEM_INIT_DONE_MEM_INIT_DONE	R/W	0h	This field will be high once initialization of B0/1TCM banks is finished. Writing '1' would clear the bit.

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2.3.2.27 MSS_CTRL_R5SS1_BTCM_MEM_INIT_STATUS Register

2.3.2.27.1 MSS_CTRL_R5SS1_BTCM_MEM_INIT_STATUS Register (Offset = 238h) [reset = 0h]

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Table 2-228. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0238h

Figure 2-113. MSS_CTRL_R5SS1_BTCM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS1_BTCM_MEM_INIT_STATUS_MEM_STATUS
NONE							R
0h							0h

Table 2-229. MSS_CTRL_R5SS1_BTCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS1_BTCM_MEM_INIT_STATUS_MEM_STATUS	R	0h	1'b0: No initialization is happening for B0/1TCM banks of CR5A/B 1'b1: Initialization is in progress for B0/1TCM banks of CR5A/B

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2.3.2.28 MSS_CTRL_L2IOCRAM_MEM_INIT Register

2.3.2.28.1 MSS_CTRL_L2IOCRAM_MEM_INIT Register (Offset = 240h) [reset = 0h]

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Table 2-230. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0240h

Figure 2-114. MSS_CTRL_L2IOCRAM_MEM_INIT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		L2IOCRAM_MEM_INIT_PARTITION5	L2IOCRAM_MEM_INIT_PARTITION4	L2IOCRAM_MEM_INIT_PARTITION3	L2IOCRAM_MEM_INIT_PARTITION2	L2IOCRAM_MEM_INIT_PARTITION1	L2IOCRAM_MEM_INIT_PARTITION0
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 2-231. MSS_CTRL_L2IOCRAM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	L2IOCRAM_MEM_INIT_PARTITION5	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the L2 Bank5. Value in each row is initialized to 0x0
4	L2IOCRAM_MEM_INIT_PARTITION4	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the L2 Bank4. Value in each row is initialized to 0x0
3	L2IOCRAM_MEM_INIT_PARTITION3	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the L2 Bank3. Value in each row is initialized to 0x0
2	L2IOCRAM_MEM_INIT_PARTITION2	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the L2 Bank2. Value in each row is initialized to 0x0
1	L2IOCRAM_MEM_INIT_PARTITION1	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the L2 Bank1. Value in each row is initialized to 0x0
0	L2IOCRAM_MEM_INIT_PARTITION0	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the L2 Bank0. Value in each row is initialized to 0x0

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2.3.2.29 MSS_CTRL_L2IOCRAM_MEM_INIT_DONE Register

2.3.2.29.1 MSS_CTRL_L2IOCRAM_MEM_INIT_DONE Register (Offset = 244h) [reset = 0h]

Return to Summary Table

Table 2-232. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0244h

Figure 2-115. MSS_CTRL_L2IOCRAM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		L2IOCRAM_MEM_INIT_DONE_PARTITION5	L2IOCRAM_MEM_INIT_DONE_PARTITION4	L2IOCRAM_MEM_INIT_DONE_PARTITION3	L2IOCRAM_MEM_INIT_DONE_PARTITION2	L2IOCRAM_MEM_INIT_DONE_PARTITION1	L2IOCRAM_MEM_INIT_DONE_PARTITION0
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 2-233. MSS_CTRL_L2IOCRAM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	L2IOCRAM_MEM_INIT_DONE_PARTITION5	R/W	0h	This field will be high once intialization of L2 bank5 is finished. Writing '1' would clear the bit
4	L2IOCRAM_MEM_INIT_DONE_PARTITION4	R/W	0h	This field will be high once intialization of L2 bank4 is finished. Writing '1' would clear the bit
3	L2IOCRAM_MEM_INIT_DONE_PARTITION3	R/W	0h	This field will be high once intialization of L2 bank3 is finished. Writing '1' would clear the bit
2	L2IOCRAM_MEM_INIT_DONE_PARTITION2	R/W	0h	This field will be high once intialization of L2 bank2 is finished. Writing '1' would clear the bit
1	L2IOCRAM_MEM_INIT_DONE_PARTITION1	R/W	0h	This field will be high once intialization of L2 bank1 is finished. Writing '1' would clear the bit
0	L2IOCRAM_MEM_INIT_DONE_PARTITION0	R/W	0h	This field will be high once intialization of L2 bank0 is finished. Writing '1' would clear the bit

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2.3.2.30 MSS_CTRL_L2IOCRAM_MEM_INIT_STATUS Register

2.3.2.30.1 MSS_CTRL_L2IOCRAM_MEM_INIT_STATUS Register (Offset = 248h) [reset = 0h]

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Table 2-234. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0248h

Figure 2-116. MSS_CTRL_L2IOCRAM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		L2IOCRAM_MEM_INIT_STATUS_PARTITION5	L2IOCRAM_MEM_INIT_STATUS_PARTITION4	L2IOCRAM_MEM_INIT_STATUS_PARTITION3	L2IOCRAM_MEM_INIT_STATUS_PARTITION2	L2IOCRAM_MEM_INIT_STATUS_PARTITION1	L2IOCRAM_MEM_INIT_STATUS_PARTITION0
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 2-235. MSS_CTRL_L2IOCRAM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	L2IOCRAM_MEM_INIT_STATUS_PARTITION5	R	0h	1'b0: No initialization is happening for L2 bank5 1'b1: Initialization is in progress for L2 bank5
4	L2IOCRAM_MEM_INIT_STATUS_PARTITION4	R	0h	1'b0: No initialization is happening for L2 bank4 1'b1: Initialization is in progress for L2 bank4
3	L2IOCRAM_MEM_INIT_STATUS_PARTITION3	R	0h	1'b0: No initialization is happening for L2 bank3 1'b1: Initialization is in progress for L2 bank3
2	L2IOCRAM_MEM_INIT_STATUS_PARTITION2	R	0h	1'b0: No initialization is happening for L2 bank2 1'b1: Initialization is in progress for L2 bank2
1	L2IOCRAM_MEM_INIT_STATUS_PARTITION1	R	0h	1'b0: No initialization is happening for L2 bank1 1'b1: Initialization is in progress for L2 bank1
0	L2IOCRAM_MEM_INIT_STATUS_PARTITION0	R	0h	1'b0: No initialization is happening for L2 bank0 1'b1: Initialization is in progress for L2 bank0

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2.3.2.31 MSS_CTRL_MAILBOXRAM_MEM_INIT Register

2.3.2.31.1 MSS_CTRL_MAILBOXRAM_MEM_INIT Register (Offset = 250h) [reset = 0h]

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Table 2-236. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0250h

Figure 2-117. MSS_CTRL_MAILBOXRAM_MEM_INIT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MAILBOXRAM_MEM_INIT_MEM0_INIT
NONE							R/W
0h							0h

Table 2-237. MSS_CTRL_MAILBOXRAM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MAILBOXRAM_MEM_INIT_MEM0_INIT	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the MSS_MBOX. Value in each row is initialized to 0x0

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2.3.2.32 MSS_CTRL_MAILBOXRAM_MEM_INIT_DONE Register

2.3.2.32.1 MSS_CTRL_MAILBOXRAM_MEM_INIT_DONE Register (Offset = 254h) [reset = 0h]

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Table 2-238. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0254h

Figure 2-118. MSS_CTRL_MAILBOXRAM_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MAILBOXRAM_MEM_INIT_DONE_MEM0_DONE
NONE							R/W
0h							0h

Table 2-239. MSS_CTRL_MAILBOXRAM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MAILBOXRAM_MEM_INIT_DONE_MEM0_DONE	R/W	0h	This field will be high once intialization of MSS_MBOX is finished. Writing '1' would clear the bit

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2.3.2.33 MSS_CTRL_MAILBOXRAM_MEM_INIT_STATUS Register

2.3.2.33.1 MSS_CTRL_MAILBOXRAM_MEM_INIT_STATUS Register (Offset = 258h) [reset = 0h]

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Table 2-240. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0258h

Figure 2-119. MSS_CTRL_MAILBOXRAM_MEM_INIT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MAILBOXRAM_MEM_INIT_STATUS_MEM0_STATUS
NONE							R
0h							0h

Table 2-241. MSS_CTRL_MAILBOXRAM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MAILBOXRAM_MEM_INIT_STATUS_MEM0_STATUS	R	0h	1'b0: No initialization is happening for MSS_MBOX 1'b1: Initialization is in progress for MSS_MBOX

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2.3.2.34 MSS_CTRL_TPCC_MEM_INIT Register

2.3.2.34.1 MSS_CTRL_TPCC_MEM_INIT Register (Offset = 260h) [reset = 0h]

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Table 2-242. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0260h

Figure 2-120. MSS_CTRL_TPCC_MEM_INIT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TPCC_MEM_INIT_TPCC_A_MEMINIT_START
NONE							R/W
0h							0h

Table 2-243. MSS_CTRL_TPCC_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TPCC_MEM_INIT_TPCC_A_MEMINIT_START	R/W	0h	Write_pulse bit field: Writing 1'b1 will start initializing the MSS_TPCCA

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2.3.2.35 MSS_CTRL_TPCC_MEM_INIT_DONE Register

2.3.2.35.1 MSS_CTRL_TPCC_MEM_INIT_DONE Register (Offset = 264h) [reset = 0h]

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Table 2-244. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0264h

Figure 2-121. MSS_CTRL_TPCC_MEM_INIT_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TPCC_MEM_INIT_DONE_TPCC_A_MEMINIT_DONE
NONE							R/W
0h							0h

Table 2-245. MSS_CTRL_TPCC_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TPCC_MEM_INIT_DONE_TPCC_A_MEMINIT_DONE	R/W	0h	This field will be high once intialization of MSS_TPCCA is finished. Writing '1' would clear the bit

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2.3.2.36 MSS_CTRL_TPCC_MEMINIT_STATUS Register

2.3.2.36.1 MSS_CTRL_TPCC_MEMINIT_STATUS Register (Offset = 268h) [reset = 0h]

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Table 2-246. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0268h

Figure 2-122. MSS_CTRL_TPCC_MEMINIT_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TPCC_MEMINIT_STATUS_TPCC_A_MEMINIT_STATUS
NONE							R
0h							0h

Table 2-247. MSS_CTRL_TPCC_MEMINIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TPCC_MEMINIT_STATUS_TPCC_A_MEMINIT_STATUS	R	0h	1'b0: No initialization is happening for MSS_TPCCA 1'b1: Initialization is in progress for MSS_TPCCB

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2.3.2.37 MSS_CTRL_TOP_PBIST_KEY_RST Register

2.3.2.37.1 MSS_CTRL_TOP_PBIST_KEY_RST Register (Offset = 300h) [reset = 0h]

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Table 2-248. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0300h

Figure 2-123. MSS_CTRL_TOP_PBIST_KEY_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TOP_PBIST_KEY_RST_PBIST_ST_RST				TOP_PBIST_KEY_RST_PBIST_ST_KEY			
R/W				R/W			
0h				0h			

Table 2-249. MSS_CTRL_TOP_PBIST_KEY_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	TOP_PBIST_KEY_RST_PBIST_ST_RST	R/W	0h	MSS PBIST controller will be brought out of reset when value is 0xA
3:0	TOP_PBIST_KEY_RST_PBIST_ST_KEY	R/W	0h	Top PBIST Selftest Key. Valid value is 0x5

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2.3.2.38 MSS_CTRL_R5SS0_CTI_TRIG_SEL Register

2.3.2.38.1 MSS_CTRL_R5SS0_CTI_TRIG_SEL Register (Offset = 400h) [reset = 0h]

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Table 2-250. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0400h

Figure 2-124. MSS_CTRL_R5SS0_CTI_TRIG_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
R5SS0_CTI_TRIG_SEL_TRIG1							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS0_CTI_TRIG_SEL_TRIG0							
R/W							
0h							

Table 2-251. MSS_CTRL_R5SS0_CTI_TRIG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	R5SS0_CTI_TRIG_SEL_TRIG1	R/W	0h	Used for selecting the trigger source for 1st trigger of MSS_R5SS
7:0	R5SS0_CTI_TRIG_SEL_TRIG0	R/W	0h	Used for selecting the trigger source for 0th trigger of MSS_R5SS

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2.3.2.39 MSS_CTRL_R5SS1_CTI_TRIG_SEL Register

2.3.2.39.1 MSS_CTRL_R5SS1_CTI_TRIG_SEL Register (Offset = 404h) [reset = 0h]

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Table 2-252. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0404h

Figure 2-125. MSS_CTRL_R5SS1_CTI_TRIG_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
R5SS1_CTI_TRIG_SEL_TRIG1							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS1_CTI_TRIG_SEL_TRIG0							
R/W							
0h							

Table 2-253. MSS_CTRL_R5SS1_CTI_TRIG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	R5SS1_CTI_TRIG_SEL_TRIG1	R/W	0h	Used for selecting the trigger source for 1st trigger of MSS_R5SS
7:0	R5SS1_CTI_TRIG_SEL_TRIG0	R/W	0h	Used for selecting the trigger source for 0th trigger of MSS_R5SS

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2.3.2.40 MSS_CTRL_DBGSS_CTI_TRIG_SEL Register

2.3.2.40.1 MSS_CTRL_DBGSS_CTI_TRIG_SEL Register (Offset = 408h) [reset = 0h]

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Table 2-254. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0408h

Figure 2-126. MSS_CTRL_DBGSS_CTI_TRIG_SEL Name Register

31	30	29	28	27	26	25	24
DBGSS_CTI_TRIG_SEL_TRIG3							
R/W							
0h							
23	22	21	20	19	18	17	16
DBGSS_CTI_TRIG_SEL_TRIG2							
R/W							
0h							
15	14	13	12	11	10	9	8
DBGSS_CTI_TRIG_SEL_TRIG1							
R/W							
0h							
7	6	5	4	3	2	1	0
DBGSS_CTI_TRIG_SEL_TRIG0							
R/W							
0h							

Table 2-255. MSS_CTRL_DBGSS_CTI_TRIG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DBGSS_CTI_TRIG_SEL_TRIG3	R/W	0h	Used for selecting the trigger source for 3rd trigger of ONE_MCU_CTI
23:16	DBGSS_CTI_TRIG_SEL_TRIG2	R/W	0h	Used for selecting the trigger source for 2nd trigger of ONE_MCU_CTI
15:8	DBGSS_CTI_TRIG_SEL_TRIG1	R/W	0h	Used for selecting the trigger source for 1st trigger of ONE_MCU_CTI
7:0	DBGSS_CTI_TRIG_SEL_TRIG0	R/W	0h	Used for selecting the trigger source for 0th trigger of ONE_MCU_CTI

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2.3.2.41 MSS_CTRL_MCAN0_HALTEN Register

2.3.2.41.1 MSS_CTRL_MCAN0_HALTEN Register (Offset = 420h) [reset = 0h]

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Table 2-256. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0420h

Figure 2-127. MSS_CTRL_MCAN0_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MCAN0_HALTEN_CR5B1_HALTEN	MCAN0_HALTEN_CR5A1_HALTEN	MCAN0_HALTEN_CR5B0_HALTEN	MCAN0_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-257. MSS_CTRL_MCAN0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MCAN0_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	MCAN0_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	MCAN0_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	MCAN0_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.42 MSS_CTRL_MCAN1_HALTEN Register

2.3.2.42.1 MSS_CTRL_MCAN1_HALTEN Register (Offset = 424h) [reset = 0h]

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Table 2-258. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0424h

Figure 2-128. MSS_CTRL_MCAN1_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MCAN1_HALTEN_CR5B1_HALTEN	MCAN1_HALTEN_CR5A1_HALTEN	MCAN1_HALTEN_CR5B0_HALTEN	MCAN1_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-259. MSS_CTRL_MCAN1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MCAN1_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	MCAN1_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	MCAN1_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	MCAN1_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.43 MSS_CTRL_MCAN2_HALTEN Register

2.3.2.43.1 MSS_CTRL_MCAN2_HALTEN Register (Offset = 428h) [reset = 0h]

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Table 2-260. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0428h

Figure 2-129. MSS_CTRL_MCAN2_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MCAN2_HALTEN_CR5B1_HALTEN	MCAN2_HALTEN_CR5A1_HALTEN	MCAN2_HALTEN_CR5B0_HALTEN	MCAN2_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-261. MSS_CTRL_MCAN2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MCAN2_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	MCAN2_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	MCAN2_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	MCAN2_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.44 MSS_CTRL_MCAN3_HALTEN Register

2.3.2.44.1 MSS_CTRL_MCAN3_HALTEN Register (Offset = 42Ch) [reset = 0h]

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Table 2-262. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 042Ch

Figure 2-130. MSS_CTRL_MCAN3_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MCAN3_HALTEN_CR5B1_HALTEN	MCAN3_HALTEN_CR5A1_HALTEN	MCAN3_HALTEN_CR5B0_HALTEN	MCAN3_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-263. MSS_CTRL_MCAN3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MCAN3_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	MCAN3_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	MCAN3_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	MCAN3_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.45 MSS_CTRL_LIN0_HALTEN Register

2.3.2.45.1 MSS_CTRL_LIN0_HALTEN Register (Offset = 430h) [reset = 0h]

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Table 2-264. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0430h

Figure 2-131. MSS_CTRL_LIN0_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				LIN0_HALTEN_CR5B1_HALTEN	LIN0_HALTEN_CR5A1_HALTEN	LIN0_HALTEN_CR5B0_HALTEN	LIN0_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-265. MSS_CTRL_LIN0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	LIN0_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	LIN0_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	LIN0_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	LIN0_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.46 MSS_CTRL_LIN1_HALTEN Register

2.3.2.46.1 MSS_CTRL_LIN1_HALTEN Register (Offset = 434h) [reset = 0h]

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Table 2-266. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0434h

Figure 2-132. MSS_CTRL_LIN1_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				LIN1_HALTEN_CR5B1_HALTEN	LIN1_HALTEN_CR5A1_HALTEN	LIN1_HALTEN_CR5B0_HALTEN	LIN1_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-267. MSS_CTRL_LIN1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	LIN1_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	LIN1_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	LIN1_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	LIN1_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.47 MSS_CTRL_LIN2_HALTEN Register

2.3.2.47.1 MSS_CTRL_LIN2_HALTEN Register (Offset = 438h) [reset = 0h]

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Table 2-268. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0438h

Figure 2-133. MSS_CTRL_LIN2_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				LIN2_HALTEN_CR5B1_HALTEN	LIN2_HALTEN_CR5A1_HALTEN	LIN2_HALTEN_CR5B0_HALTEN	LIN2_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-269. MSS_CTRL_LIN2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	LIN2_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	LIN2_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	LIN2_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	LIN2_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.48 MSS_CTRL_LIN3_HALTEN Register

2.3.2.48.1 MSS_CTRL_LIN3_HALTEN Register (Offset = 43Ch) [reset = 0h]

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Table 2-270. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 043Ch

Figure 2-134. MSS_CTRL_LIN3_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				LIN3_HALTEN_CR5B1_HALTEN	LIN3_HALTEN_CR5A1_HALTEN	LIN3_HALTEN_CR5B0_HALTEN	LIN3_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-271. MSS_CTRL_LIN3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	LIN3_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	LIN3_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	LIN3_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	LIN3_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.49 MSS_CTRL_LIN4_HALTEN Register

2.3.2.49.1 MSS_CTRL_LIN4_HALTEN Register (Offset = 440h) [reset = 0h]

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Table 2-272. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0440h

Figure 2-135. MSS_CTRL_LIN4_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				LIN4_HALTEN_CR5B1_HALTEN	LIN4_HALTEN_CR5A1_HALTEN	LIN4_HALTEN_CR5B0_HALTEN	LIN4_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-273. MSS_CTRL_LIN4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	LIN4_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	LIN4_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	LIN4_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	LIN4_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.50 MSS_CTRL_I2C0_HALTEN Register

2.3.2.50.1 MSS_CTRL_I2C0_HALTEN Register (Offset = 444h) [reset = 0h]

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Table 2-274. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0444h

Figure 2-136. MSS_CTRL_I2C0_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				I2C0_HALTEN_CR5B1_HALTEN	I2C0_HALTEN_CR5A1_HALTEN	I2C0_HALTEN_CR5B0_HALTEN	I2C0_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-275. MSS_CTRL_I2C0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	I2C0_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	I2C0_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	I2C0_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	I2C0_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.51 MSS_CTRL_I2C1_HALTEN Register

2.3.2.51.1 MSS_CTRL_I2C1_HALTEN Register (Offset = 448h) [reset = 0h]

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Table 2-276. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0448h

Figure 2-137. MSS_CTRL_I2C1_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				I2C1_HALTEN_CR5B1_HALTEN	I2C1_HALTEN_CR5A1_HALTEN	I2C1_HALTEN_CR5B0_HALTEN	I2C1_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-277. MSS_CTRL_I2C1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	I2C1_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	I2C1_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	I2C1_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	I2C1_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.52 MSS_CTRL_I2C2_HALTEN Register

2.3.2.52.1 MSS_CTRL_I2C2_HALTEN Register (Offset = 44Ch) [reset = 0h]

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Table 2-278. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 044Ch

Figure 2-138. MSS_CTRL_I2C2_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				I2C2_HALTEN_CR5B1_HALTEN	I2C2_HALTEN_CR5A1_HALTEN	I2C2_HALTEN_CR5B0_HALTEN	I2C2_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-279. MSS_CTRL_I2C2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	I2C2_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	I2C2_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	I2C2_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	I2C2_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.53 MSS_CTRL_I2C3_HALTEN Register

2.3.2.53.1 MSS_CTRL_I2C3_HALTEN Register (Offset = 450h) [reset = 0h]

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Table 2-280. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0450h

Figure 2-139. MSS_CTRL_I2C3_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				I2C3_HALTEN_CR5B1_HALTEN	I2C3_HALTEN_CR5A1_HALTEN	I2C3_HALTEN_CR5B0_HALTEN	I2C3_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-281. MSS_CTRL_I2C3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	I2C3_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	I2C3_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	I2C3_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	I2C3_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.54 MSS_CTRL_RTI0_HALTEN Register

2.3.2.54.1 MSS_CTRL_RTI0_HALTEN Register (Offset = 454h) [reset = 0h]

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Table 2-282. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0454h

Figure 2-140. MSS_CTRL_RTI0_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RTI0_HALTEN_CR5B1_HALTEN	RTI0_HALTEN_CR5A1_HALTEN	RTI0_HALTEN_CR5B0_HALTEN	RTI0_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-283. MSS_CTRL_RTI0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RTI0_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	RTI0_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	RTI0_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	RTI0_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.55 MSS_CTRL_RTI1_HALTEN Register

2.3.2.55.1 MSS_CTRL_RTI1_HALTEN Register (Offset = 458h) [reset = 0h]

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Table 2-284. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0458h

Figure 2-141. MSS_CTRL_RTI1_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RTI1_HALTEN_CR5B1_HALTEN	RTI1_HALTEN_CR5A1_HALTEN	RTI1_HALTEN_CR5B0_HALTEN	RTI1_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-285. MSS_CTRL_RTI1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RTI1_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	RTI1_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	RTI1_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	RTI1_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.56 MSS_CTRL_RTI2_HALTEN Register

2.3.2.56.1 MSS_CTRL_RTI2_HALTEN Register (Offset = 45Ch) [reset = 0h]

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Table 2-286. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 045Ch

Figure 2-142. MSS_CTRL_RTI2_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RTI2_HALTEN_CR5B1_HALTEN	RTI2_HALTEN_CR5A1_HALTEN	RTI2_HALTEN_CR5B0_HALTEN	RTI2_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-287. MSS_CTRL_RTI2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RTI2_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	RTI2_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	RTI2_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	RTI2_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.57 MSS_CTRL_RTI3_HALTEN Register

2.3.2.57.1 MSS_CTRL_RTI3_HALTEN Register (Offset = 460h) [reset = 0h]

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Table 2-288. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0460h

Figure 2-143. MSS_CTRL_RTI3_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RTI3_HALTEN_CR5B1_HALTEN	RTI3_HALTEN_CR5A1_HALTEN	RTI3_HALTEN_CR5B0_HALTEN	RTI3_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-289. MSS_CTRL_RTI3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RTI3_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	RTI3_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	RTI3_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	RTI3_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.58 MSS_CTRL_CPSW_HALTEN Register

2.3.2.58.1 MSS_CTRL_CPSW_HALTEN Register (Offset = 474h) [reset = 0h]

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Table 2-290. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0474h

Figure 2-144. MSS_CTRL_CPSW_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CPSW_HALTEN_CR5B1_HALTEN	CPSW_HALTEN_CR5A1_HALTEN	CPSW_HALTEN_CR5B0_HALTEN	CPSW_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-291. MSS_CTRL_CPSW_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CPSW_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CPSW_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CPSW_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CPSW_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.59 MSS_CTRL_MCRC0_HALTEN Register

2.3.2.59.1 MSS_CTRL_MCRC0_HALTEN Register (Offset = 478h) [reset = 0h]

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Table 2-292. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0478h

Figure 2-145. MSS_CTRL_MCRC0_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MCRC0_HALTEN_CR5B1_HALTEN	MCRC0_HALTEN_CR5A1_HALTEN	MCRC0_HALTEN_CR5B0_HALTEN	MCRC0_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-293. MSS_CTRL_MCRC0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MCRC0_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	MCRC0_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	MCRC0_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	MCRC0_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.60 MSS_CTRL_MCAN4_HALTEN Register

2.3.2.60.1 MSS_CTRL_MCAN4_HALTEN Register (Offset = 47Ch) [reset = 0h]

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Table 2-294. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 047Ch

Figure 2-146. MSS_CTRL_MCAN4_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MCAN4_HALTEN_CR5B1_HALTEN	MCAN4_HALTEN_CR5A1_HALTEN	MCAN4_HALTEN_CR5B0_HALTEN	MCAN4_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-295. MSS_CTRL_MCAN4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MCAN4_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	MCAN4_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	MCAN4_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	MCAN4_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.61 MSS_CTRL_MCAN5_HALTEN Register

2.3.2.61.1 MSS_CTRL_MCAN5_HALTEN Register (Offset = 480h) [reset = 0h]

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Table 2-296. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0480h

Figure 2-147. MSS_CTRL_MCAN5_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MCAN5_HALTEN_CR5B1_HALTEN	MCAN5_HALTEN_CR5A1_HALTEN	MCAN5_HALTEN_CR5B0_HALTEN	MCAN5_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-297. MSS_CTRL_MCAN5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MCAN5_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	MCAN5_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	MCAN5_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	MCAN5_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.62 MSS_CTRL_MCAN6_HALTEN Register

2.3.2.62.1 MSS_CTRL_MCAN6_HALTEN Register (Offset = 484h) [reset = 0h]

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Table 2-298. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0484h

Figure 2-148. MSS_CTRL_MCAN6_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MCAN6_HALTEN_CR5B1_HALTEN	MCAN6_HALTEN_CR5A1_HALTEN	MCAN6_HALTEN_CR5B0_HALTEN	MCAN6_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-299. MSS_CTRL_MCAN6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MCAN6_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	MCAN6_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	MCAN6_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	MCAN6_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.63 MSS_CTRL_MCAN7_HALTEN Register

2.3.2.63.1 MSS_CTRL_MCAN7_HALTEN Register (Offset = 488h) [reset = 0h]

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Table 2-300. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0488h

Figure 2-149. MSS_CTRL_MCAN7_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MCAN7_HALTEN_CR5B1_HALTEN	MCAN7_HALTEN_CR5A1_HALTEN	MCAN7_HALTEN_CR5B0_HALTEN	MCAN7_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-301. MSS_CTRL_MCAN7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MCAN7_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	MCAN7_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	MCAN7_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	MCAN7_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.64 MSS_CTRL_RTI4_HALTEN Register

2.3.2.64.1 MSS_CTRL_RTI4_HALTEN Register (Offset = 48Ch) [reset = 0h]

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Table 2-302. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 048Ch

Figure 2-150. MSS_CTRL_RTI4_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RTI4_HALTEN_CR5B1_HALTEN	RTI4_HALTEN_CR5A1_HALTEN	RTI4_HALTEN_CR5B0_HALTEN	RTI4_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-303. MSS_CTRL_RTI4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RTI4_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	RTI4_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	RTI4_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	RTI4_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.65 MSS_CTRL_RTI5_HALTEN Register

2.3.2.65.1 MSS_CTRL_RTI5_HALTEN Register (Offset = 490h) [reset = 0h]

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Table 2-304. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0490h

Figure 2-151. MSS_CTRL_RTI5_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RTI5_HALTEN_CR5B1_HALTEN	RTI5_HALTEN_CR5A1_HALTEN	RTI5_HALTEN_CR5B0_HALTEN	RTI5_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-305. MSS_CTRL_RTI5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RTI5_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	RTI5_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	RTI5_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	RTI5_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.66 MSS_CTRL_RTI6_HALTEN Register

2.3.2.66.1 MSS_CTRL_RTI6_HALTEN Register (Offset = 494h) [reset = 0h]

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Table 2-306. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0494h

Figure 2-152. MSS_CTRL_RTI6_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RTI6_HALTEN_CR5B1_HALTEN	RTI6_HALTEN_CR5A1_HALTEN	RTI6_HALTEN_CR5B0_HALTEN	RTI6_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-307. MSS_CTRL_RTI6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RTI6_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	RTI6_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	RTI6_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	RTI6_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.67 MSS_CTRL_RTI7_HALTEN Register

2.3.2.67.1 MSS_CTRL_RTI7_HALTEN Register (Offset = 498h) [reset = 0h]

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Table 2-308. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0498h

Figure 2-153. MSS_CTRL_RTI7_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RTI7_HALTEN_CR5B1_HALTEN	RTI7_HALTEN_CR5A1_HALTEN	RTI7_HALTEN_CR5B0_HALTEN	RTI7_HALTEN_CR5A0_HALTEN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-309. MSS_CTRL_RTI7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RTI7_HALTEN_CR5B1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	RTI7_HALTEN_CR5A1_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	RTI7_HALTEN_CR5B0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	RTI7_HALTEN_CR5A0_HALTEN	R/W	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.2.68 MSS_CTRL_TPTC_DBS_CONFIG Register

2.3.2.68.1 MSS_CTRL_TPTC_DBS_CONFIG Register (Offset = 800h) [reset = 11h]

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Table 2-310. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0800h

Figure 2-154. MSS_CTRL_TPTC_DBS_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		TPTC_DBS_CONFIG_TPTC_A1		RESERVED		TPTC_DBS_CONFIG_TPTC_A0	
NONE		R/W		NONE		R/W	
0h		0h		0h		0h	

Table 2-311. MSS_CTRL_TPTC_DBS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:4	TPTC_DBS_CONFIG_TPTC_A1	R/W	0h	DBS [default burst size] tieoff value for TPTC A1. DBS tieoff defines optimally sized cmd.Both the read and write controller will always issue commands that are less than or equal to the DBS tieoff value. This will typically be on the order of 4 or 8 dataphases worth of data. DBS must always be tied off to no larger than half of the Channel FIFO size. Set DBS to - 2'b00 = 16 byte 2'b01 = 32 byte 2'b10 = 64 byte 2'b11 = 128 byte
3:2	RESERVED	NONE	0h	Reserved
1:0	TPTC_DBS_CONFIG_TPTC_A0	R/W	0h	DBS [default burst size] tieoff value for TPTC A0. DBS tieoff defines optimally sized cmd.Both the read and write controller will always issue commands that are less than or equal to the DBS tieoff value. This will typically be on the order of 4 or 8 dataphases worth of data. DBS must always be tied off to no larger than half of the Channel FIFO size. Set DBS to - 2'b00 = 16 byte 2'b01 = 32 byte 2'b10 = 64 byte 2'b11 = 128 byte

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2.3.2.69 MSS_CTRL_TPTC_BOUNDARY_CFG Register

2.3.2.69.1 MSS_CTRL_TPTC_BOUNDARY_CFG Register (Offset = 804h) [reset = 1313h]

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Table 2-312. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0804h

Figure 2-155. MSS_CTRL_TPTC_BOUNDARY_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TPTC_BOUNDARY_CFG_TPTC_A1_SIZE					
NONE		R/W					
0h		13h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		TPTC_BOUNDARY_CFG_TPTC_A0_SIZE					
NONE		R/W					
0h		13h					

Table 2-313. MSS_CTRL_TPTC_BOUNDARY_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:8	TPTC_BOUNDARY_CFG_TPTC_A1_SIZE	R/W	13h	6 bit signal used for deciding the boundary crossing size for CID-RID-SID reordering of MSS_TPTC_A1 Example: Writing 6'd19 decidies boundary to be 2^19 i.e. 512 KB
7:6	RESERVED	NONE	0h	Reserved
5:0	TPTC_BOUNDARY_CFG_TPTC_A0_SIZE	R/W	13h	6 bit signal used for deciding the boundary crossing size for CID-RID-SID reordering of MSS_TPTC_A0 Example: Writing 6'd19 decidies boundary to be 2^19 i.e. 512 KB

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2.3.2.70 MSS_CTRL_TPTC_XID_REORDER_CFG Register

2.3.2.70.1 MSS_CTRL_TPTC_XID_REORDER_CFG Register (Offset = 808h) [reset = 0h]

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Table 2-314. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0808h

Figure 2-156. MSS_CTRL_TPTC_XID_REORDER_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							TPTC_XID_REORDER_CFG_TPTC_A1_DISABLE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							TPTC_XID_REORDER_CFG_TPTC_A0_DISABLE
NONE							R/W
0h							0h

Table 2-315. MSS_CTRL_TPTC_XID_REORDER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	TPTC_XID_REORDER_CFG_TPTC_A1_DISABLE	R/W	0h	Writing 1'b1 will disable the CID-RID-SID reodering feature for MSS_TPTC_A1
7:1	RESERVED	NONE	0h	Reserved
0	TPTC_XID_REORDER_CFG_TPTC_A0_DISABLE	R/W	0h	Writing 1'b1 will disable the CID-RID-SID reodering feature for MSS_TPTC_A0

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2.3.2.71 MSS_CTRL_CPSW_CONTROL Register

2.3.2.71.1 MSS_CTRL_CPSW_CONTROL Register (Offset = 810h) [reset = 1000100h]

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Table 2-316. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0810h

Figure 2-157. MSS_CTRL_CPSW_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							CPSW_CONTROL_RGMII2_ID_MODE
NONE							R/W
0h							1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	CPSW_CONTROL_RMII2_REF_CLK_SEL	RESERVED	CPSW_CONTROL_RMII2_REF_CLK_OE_N	RESERVED	CPSW_CONTROL_PORT2_MODE_SEL		
NONE	R/W	NONE	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							CPSW_CONTROL_RGMII1_ID_MODE
NONE							R/W
0h							1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	CPSW_CONTROL_RMII1_REF_CLK_SEL	RESERVED	CPSW_CONTROL_RMII1_REF_CLK_OE_N	RESERVED	CPSW_CONTROL_PORT1_MODE_SEL		
NONE	R/W	NONE	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		

Table 2-317. MSS_CTRL_CPSW_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	CPSW_CONTROL_RGMII2_ID_MODE	R/W	1h	Internal delay mode for port 2. Only for TX 1'b0 ID mode is disabled 1'b1 ID mode is enabled
23	RESERVED	NONE	0h	Reserved
22	CPSW_CONTROL_RMII2_REF_CLK_SEL	R/W	0h	To select the rmii_ref_clk loopback mux output either from PAD or from MSS_RCM. Write 1'b0 to get clock will be from IO pad[pad loopback]. Write 1'b1 to get clock from internal loopback.
21	RESERVED	NONE	0h	Reserved
20	CPSW_CONTROL_RMII2_REF_CLK_OE_N	R/W	0h	RMII_REF_CLK IO Output enable control 1'b0: Output enable 1'b1: Output Disable
19	RESERVED	NONE	0h	Reserved

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Table 2-317. MSS_CTRL_CPSW_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:16	CPSW_CONTROL_PORT2_MODE_SEL	R/W	0h	Port 2 Interface 3'b000 = MII 3'b001 = RMII 3'b010 = RGMII 011 - 111 = Not Supported
15:9	RESERVED	NONE	0h	Reserved
8	CPSW_CONTROL_RGMII1_ID_MODE	R/W	1h	Internal delay mode for port 1. Only for TX 1'b0 ID mode is disabled 1'b1 ID mode is enabled
7	RESERVED	NONE	0h	Reserved
6	CPSW_CONTROL_RMII1_REF_CLK_SEL	R/W	0h	To select the rmii_ref_clk loopback mux output either from PAD or from MSS_RCM. Write 1'b0 to get clock will be from IO pad[pad loopback]. Write 1'b1 to get clock from internal source
5	RESERVED	NONE	0h	Reserved
4	CPSW_CONTROL_RMII1_REF_CLK_OE_N	R/W	0h	RMII_REF_CLK IO Output enable control 1'b0: Output enable 1'b1: Output Disable
3	RESERVED	NONE	0h	Reserved
2:0	CPSW_CONTROL_PORT1_MODE_SEL	R/W	0h	Port 1 Interface 3'b000 = MII 3'b001 = RMII 3'b010 = RGMII 011 - 111 = Not Supported

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2.3.2.72 MSS_CTRL_OSPI_CONFIG Register

2.3.2.72.1 MSS_CTRL_OSPI_CONFIG Register (Offset = 814h) [reset = 0h]

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Table 2-318. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0814h

Figure 2-158. MSS_CTRL_OSPI_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	OSPI_CONFIG_RTXIP_PENDING			RESERVED			
NONE	R/W			NONE			
0h	0h			0h			
7	6	5	4	3	2	1	0
RESERVED	OSPI_CONFIG_ICLK_SEL			RESERVED	OSPI_CONFIG_EXT_CLK		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 2-319. MSS_CTRL_OSPI_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	OSPI_CONFIG_RTXIP_PENDING	R/W	0h	Real time xip indication for OSPI Write 3'b111 for real time xip is pending Write 3'b000 for real time xip is done configuration changes must be done when FSS is idle/not configured/no transactions
11:7	RESERVED	NONE	0h	Reserved
6:4	OSPI_CONFIG_ICLK_SEL	R/W	0h	Write 3'b111 to switch to loopback clock as OSPI input IO clock Write 3'b000 to switch to OSPI DQS as OSPI input IO clock configuration changes must be done when FSS is idle/not configured/no transactions
3	RESERVED	NONE	0h	Reserved
2:0	OSPI_CONFIG_EXT_CLK	R/W	0h	Write 3'b111 to external clock as OSPI baud clock source - needed for DFT IO char.

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2.3.2.73 MSS_CTRL_PRU_ICSS_IDLE_CONTROL Register

2.3.2.73.1 MSS_CTRL_PRU_ICSS_IDLE_CONTROL Register (Offset = 818h) [reset = 1h]

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Table 2-320. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0818h

Figure 2-159. MSS_CTRL_PRU_ICSS_IDLE_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PRU_ICSS_IDLE_CONTROL_NOGATE
NONE							R/W
0h							1h

Table 2-321. MSS_CTRL_PRU_ICSS_IDLE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PRU_ICSS_IDLE_CONTROL_NOGATE	R/W	1h	Writing 1'b0 will enable local auto-clock gating [lower power] at IP level with increase in access/functional latency. Following IPs are controlled with this signal ICSSM

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2.3.2.74 MSS_CTRL_PRU_ICSS_PRU0_GPI_SEL Register

2.3.2.74.1 MSS_CTRL_PRU_ICSS_PRU0_GPI_SEL Register (Offset = 81Ch) [reset = 0h]

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Table 2-322. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 081Ch

Figure 2-160. MSS_CTRL_PRU_ICSS_PRU0_GPI_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED		PRU_ICSS_PRU0_GPI_SEL_SEL					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PRU_ICSS_PRU0_GPI_SEL_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PRU_ICSS_PRU0_GPI_SEL_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PRU_ICSS_PRU0_GPI_SEL_SEL							
R/W							
0h							

Table 2-323. MSS_CTRL_PRU_ICSS_PRU0_GPI_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PRU_ICSS_PRU0_GPI_SEL_SEL	R/W	0h	GPI or PWMXBAR select for ICSM Port0 3'b000 GPI 3'111 PWMXBAR

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2.3.2.75 MSS_CTRL_PRU_ICSS_PRU1_GPI_SEL Register

2.3.2.75.1 MSS_CTRL_PRU_ICSS_PRU1_GPI_SEL Register (Offset = 820h) [reset = 0h]

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Table 2-324. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0820h

Figure 2-161. MSS_CTRL_PRU_ICSS_PRU1_GPI_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED		PRU_ICSS_PRU1_GPI_SEL_SEL					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU_ICSS_PRU1_GPI_SEL_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU_ICSS_PRU1_GPI_SEL_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU_ICSS_PRU1_GPI_SEL_SEL							
R/W							
0h							

Table 2-325. MSS_CTRL_PRU_ICSS_PRU1_GPI_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PRU_ICSS_PRU1_GPI_SEL_SEL	R/W	0h	GPI or PWMXBAR select for ICSM Port0 3'b000 GPI 3'111 PWMXBAR

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2.3.2.76 MSS_CTRL_PRU_ICSS_PRU0_GPIO_OUT_CTRL Register

2.3.2.76.1 MSS_CTRL_PRU_ICSS_PRU0_GPIO_OUT_CTRL Register (Offset = 824h) [reset = 0h]

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Table 2-326. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0824h

Figure 2-162. MSS_CTRL_PRU_ICSS_PRU0_GPIO_OUT_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED		PRU_ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PRU_ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
PRU_ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
PRU_ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE							
R/W							
0h							

Table 2-327. MSS_CTRL_PRU_ICSS_PRU0_GPIO_OUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PRU_ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE	R/W	0h	GPO output disable for ICSSM Port 0 IO. Disable output for using the pin as input. Each Bit maps to the corresponding bit in the IO 3'b000 Output Enable 3'111 Output Disable

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2.3.2.77 MSS_CTRL_PRU_ICSS_PRU1_GPIO_OUT_CTRL Register

2.3.2.77.1 MSS_CTRL_PRU_ICSS_PRU1_GPIO_OUT_CTRL Register (Offset = 828h) [reset = 0h]

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Table 2-328. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0828h

Figure 2-163. MSS_CTRL_PRU_ICSS_PRU1_GPIO_OUT_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED		PRU_ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE					
NONE		R/W					
0h		0h					
23	22	21	20	19	18	17	16
PRU_ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
PRU_ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
PRU_ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE							
R/W							
0h							

Table 2-329. MSS_CTRL_PRU_ICSS_PRU1_GPIO_OUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PRU_ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE	R/W	0h	GPO output disable for ICSSM Port 1 IO. Disable output for using the pin as input. Each Bit maps to the corresponding bit in the IO 3'b000 Output Enable 3'111 Output Disable

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2.3.2.78 MSS_CTRL_TPCC0_INTAGG_MASK Register

2.3.2.78.1 MSS_CTRL_TPCC0_INTAGG_MASK Register (Offset = 830h) [reset = 0h]

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Table 2-330. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0830h

Figure 2-164. MSS_CTRL_TPCC0_INTAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						TPCC0_INTAGG_MASK_TPTC_A1	TPCC0_INTAGG_MASK_TPTC_A0
NONE						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TPCC0_INTAGG_MASK_TPCC_A_INT7
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TPCC0_INTAGG_MASK_TPCC_A_INT6	TPCC0_INTAGG_MASK_TPCC_A_INT5	TPCC0_INTAGG_MASK_TPCC_A_INT4	TPCC0_INTAGG_MASK_TPCC_A_INT3	TPCC0_INTAGG_MASK_TPCC_A_INT2	TPCC0_INTAGG_MASK_TPCC_A_INT1	TPCC0_INTAGG_MASK_TPCC_A_INT0	TPCC0_INTAGG_MASK_TPCC_A_INTG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-331. MSS_CTRL_TPCC0_INTAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	TPCC0_INTAGG_MASK_TPTC_A1	R/W	0h	Mask Interrupt from TPTC A1 to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
16	TPCC0_INTAGG_MASK_TPTC_A0	R/W	0h	Mask Interrupt from TPTC A0 to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
15:9	RESERVED	NONE	0h	Reserved
8	TPCC0_INTAGG_MASK_TPCC_A_INT7	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
7	TPCC0_INTAGG_MASK_TPCC_A_INT6	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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Table 2-331. MSS_CTRL_TPCC0_INTAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TPCC0_INTAGG_MASK_TPCC_A_INT5	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
5	TPCC0_INTAGG_MASK_TPCC_A_INT4	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
4	TPCC0_INTAGG_MASK_TPCC_A_INT3	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
3	TPCC0_INTAGG_MASK_TPCC_A_INT2	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
2	TPCC0_INTAGG_MASK_TPCC_A_INT1	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
1	TPCC0_INTAGG_MASK_TPCC_A_INT0	R/W	0h	Mask Interrupt from TPCC A to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
0	TPCC0_INTAGG_MASK_TPCC_A_INTG	R/W	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.79 MSS_CTRL_TPCC0_INTAGG_STATUS Register

2.3.2.79.1 MSS_CTRL_TPCC0_INTAGG_STATUS Register (Offset = 834h) [reset = 0h]

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Table 2-332. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0834h

Figure 2-165. MSS_CTRL_TPCC0_INTAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						TPCC0_INTAGG_STATUS_TPTC_A1	TPCC0_INTAGG_STATUS_TPTC_A0
NONE						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED							TPCC0_INTAGG_STATUS_TPCC_A_INT7
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
TPCC0_INTAGG_STATUS_TPCC_A_INT6	TPCC0_INTAGG_STATUS_TPCC_A_INT5	TPCC0_INTAGG_STATUS_TPCC_A_INT4	TPCC0_INTAGG_STATUS_TPCC_A_INT3	TPCC0_INTAGG_STATUS_TPCC_A_INT2	TPCC0_INTAGG_STATUS_TPCC_A_INT1	TPCC0_INTAGG_STATUS_TPCC_A_INT0	TPCC0_INTAGG_STATUS_TPCC_A_INTG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-333. MSS_CTRL_TPCC0_INTAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	TPCC0_INTAGG_STATUS_TPTC_A1	R/W	0h	Status of Interrupt from TPTC A1. Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.
16	TPCC0_INTAGG_STATUS_TPTC_A0	R/W	0h	Status of Interrupt from TPTC A0. Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.
15:9	RESERVED	NONE	0h	Reserved
8	TPCC0_INTAGG_STATUS_TPCC_A_INT7	R/W	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.
7	TPCC0_INTAGG_STATUS_TPCC_A_INT6	R/W	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.
6	TPCC0_INTAGG_STATUS_TPCC_A_INT5	R/W	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.
5	TPCC0_INTAGG_STATUS_TPCC_A_INT4	R/W	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.

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Table 2-333. MSS_CTRL_TPCC0_INTAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TPCC0_INTAGG_STATUS_TPCC_A_INT3	R/W	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.
3	TPCC0_INTAGG_STATUS_TPCC_A_INT2	R/W	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.
2	TPCC0_INTAGG_STATUS_TPCC_A_INT1	R/W	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.
1	TPCC0_INTAGG_STATUS_TPCC_A_INT0	R/W	0h	Status of Interrupt from TPCC A Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.
0	TPCC0_INTAGG_STATUS_TPCC_A_INTG	R/W	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_INTAGG_MASK Wrie 0x1 to clear this interrupt.

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2.3.2.80 MSS_CTRL_TPCC0_INTAGG_STATUS_RAW Register

2.3.2.80.1 MSS_CTRL_TPCC0_INTAGG_STATUS_RAW Register (Offset = 838h) [reset = 0h]

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Table 2-334. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0838h

Figure 2-166. MSS_CTRL_TPCC0_INTAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						TPCC0_INTAGG_STATUS_RAW_TPTC_A1	TPCC0_INTAGG_STATUS_RAW_TPTC_A0
NONE						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED							TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT7
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT6	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT5	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT4	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT3	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT2	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT1	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT0	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INTG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-335. MSS_CTRL_TPCC0_INTAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	TPCC0_INTAGG_STATUS_RAW_TPTC_A1	R/W	0h	Raw Status of Interrupt from TPTC A1. Set irrespective if the Interupt is masked or unmasked in TPCC0_INTAGG_MASK
16	TPCC0_INTAGG_STATUS_RAW_TPTC_A0	R/W	0h	Raw Status of Interrupt from TPTC A0. Set irrespective if the Interupt is masked or unmasked in TPCC0_INTAGG_MASK
15:9	RESERVED	NONE	0h	Reserved
8	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT7	R/W	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
7	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT6	R/W	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
6	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT5	R/W	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK

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Table 2-335. MSS_CTRL_TPCC0_INTAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT4	R/W	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
4	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT3	R/W	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
3	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT2	R/W	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
2	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT1	R/W	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
1	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INT0	R/W	0h	Raw Status of Interrupt from TPCC A. Set irrespective if the Interupt is masked or unmasked in TPCC0_INTAGG_MASK
0	TPCC0_INTAGG_STATUS_RAW_TPCC_A_INTG	R/W	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK

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2.3.2.81 MSS_CTRL_INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL Register

2.3.2.81.1 MSS_CTRL_INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL Register (Offset = 83Ch) [reset = 0h]

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Table 2-336. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 083Ch

Figure 2-167. MSS_CTRL_INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_MISC_PERIPH_DYNAMIC_CLK_GATE_EN			RESERVED	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_MISC_CONFIG1_DYNAMIC_CLK_GATE_EN		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_MISC_CONFIG0_DYNAMIC_CLK_GATE_EN			RESERVED	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_PERI_DYNAMIC_CLK_GATE_EN		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_INFRA_G1_DYNAMIC_CLK_GATE_EN			RESERVED	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_INFRA_G0_DYNAMIC_CLK_GATE_EN		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 2-337. MSS_CTRL_INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:20	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_MISC_PERIPH_DYNAMIC_CLK_GATE_EN	R/W	0h	dynamic clock gate feature enable. Multibit write Write 0x111 to enable Write 0x000 to disable 2 extra clock latency for the first access after the clock is gated and SCRP_PERI is not gated
19	RESERVED	NONE	0h	Reserved
18:16	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_MISC_CONFIG1_DYNAMIC_CLK_GATE_EN	R/W	0h	dynamic clock gate feature enable. Multibit write Write 0x111 to enable Write 0x000 to disable 2 extra clock latency for the first access after the clock is gated and SCRP_PERI is not gated
15	RESERVED	NONE	0h	Reserved
14:12	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_MISC_CONFIG0_DYNAMIC_CLK_GATE_EN	R/W	0h	dynamic clock gate feature enable. Multibit write Write 0x111 to enable Write 0x000 to disable 2 extra clock latency for the first access after the clock is gated and SCRP_PERI is not gated
11	RESERVED	NONE	0h	Reserved

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Table 2-337. MSS_CTRL_INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_PERI_DYNAMIC_CLK_GATE_EN	R/W	0h	dynamic clock gate feature enable. Multibit write Write 0x111 to enable Write 0x000 to disable 2 extra clock latency for the first access after the clock is gated and SCRP_PERI is not gated
7	RESERVED	NONE	0h	Reserved
6:4	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_INFRA_G1_DYNAMIC_CLK_GATE_EN	R/W	0h	dynamic clock gate feature enable. Multibit write Write 0x111 to enable Write 0x000 to disable 2 extra clock latency for the first access after the clock is gated and SCRP_PERI is not gated 4 extra clock latency for the first access after the clock is gated and SCRP_PERI is gated
3	RESERVED	NONE	0h	Reserved
2:0	INTERCONNECT_CLK_GATE_DYNAMIC_CONTROL_INFRA_G0_DYNAMIC_CLK_GATE_EN	R/W	0h	dynamic clock gate feature enable. Multibit write Write 0x111 to enable Write 0x000 to disable 2 extra clock latency for the first access after the clock is gated and SCRP_PERI is not gated 4 extra clock latency for the first access after the clock is gated and SCRP_PERI is gated

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2.3.2.82 MSS_CTRL_OSPI_BOOT_CONFIG_MASK Register

2.3.2.82.1 MSS_CTRL_OSPI_BOOT_CONFIG_MASK Register (Offset = 840h) [reset = 0h]

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Table 2-338. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0840h

Figure 2-168. MSS_CTRL_OSPI_BOOT_CONFIG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OSPI_BOOT_CONFIG_MASK_BOOT_SIZE			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OSPI_BOOT_CONFIG_MASK_BOOT_SIZE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OSPI_BOOT_CONFIG_MASK_BOOT_SIZE							
R/W							
0h							

Table 2-339. MSS_CTRL_OSPI_BOOT_CONFIG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OSPI_BOOT_CONFIG_MASK_BOOT_SIZE	R/W	0h	OSPI boot size register configuration changes must be done when FSS is idle/not configured/no transactions

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2.3.2.83 MSS_CTRL_OSPI_BOOT_CONFIG_SEG Register

2.3.2.83.1 MSS_CTRL_OSPI_BOOT_CONFIG_SEG Register (Offset = 844h) [reset = 0h]

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Table 2-340. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0844h

Figure 2-169. MSS_CTRL_OSPI_BOOT_CONFIG_SEG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OSPI_BOOT_CONFIG_SEG_BOOT_SEG			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OSPI_BOOT_CONFIG_SEG_BOOT_SEG							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OSPI_BOOT_CONFIG_SEG_BOOT_SEG							
R/W							
0h							

Table 2-341. MSS_CTRL_OSPI_BOOT_CONFIG_SEG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OSPI_BOOT_CONFIG_SEG_BOOT_SEG	R/W	0h	OSPI segment selector for programmed boot size configuration changes must be done when FSS is idle/not configured/no transactions

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2.3.2.84 MSS_CTRL_PRU_ICSS_RX_ERR_COUNTER Register

2.3.2.84.1 MSS_CTRL_PRU_ICSS_RX_ERR_COUNTER Register (Offset = 848h) [reset = 0h]

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Table 2-342. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0848h

Figure 2-170. MSS_CTRL_PRU_ICSS_RX_ERR_COUNTER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PRU_ICSS_RX_ERR_COUNTER_MII1_RXERR_CNT							
R							
0h							
7	6	5	4	3	2	1	0
PRU_ICSS_RX_ERR_COUNTER_MII0_RXERR_CNT							
R							
0h							

Table 2-343. MSS_CTRL_PRU_ICSS_RX_ERR_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PRU_ICSS_RX_ERR_COUNTER_MII1_RXERR_CNT	R	0h	Counts the error in MII1_RX_CLK
7:0	PRU_ICSS_RX_ERR_COUNTER_MII0_RXERR_CNT	R	0h	Counts the error in MII0_RX_CLK

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2.3.2.85 MSS_CTRL_PRU_ICSS_RX_ERR_COUNTER_CLR Register

2.3.2.85.1 MSS_CTRL_PRU_ICSS_RX_ERR_COUNTER_CLR Register (Offset = 84Ch) [reset = 0h]

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Table 2-344. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 084Ch

Figure 2-171. MSS_CTRL_PRU_ICSS_RX_ERR_COUNTER_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PRU_ICSS_RX_ERR_COUNTER_CLR_MII1_RXERR_WRT1CLR	PRU_ICSS_RX_ERR_COUNTER_CLR_MII0_RXERR_WRT1CLR
NONE						R/W	R/W
0h						0h	0h

Table 2-345. MSS_CTRL_PRU_ICSS_RX_ERR_COUNTER_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	PRU_ICSS_RX_ERR_COUNTER_CLR_MII1_RXERR_WRT1CLR	R/W	0h	Clears the Counter which counts the error in MII1_RX_CLK 1'b0: Inactive clear 1'b1: Clears the counter
0	PRU_ICSS_RX_ERR_COUNTER_CLR_MII0_RXERR_WRT1CLR	R/W	0h	Clears the Counter which counts the error in MII0_RX_CLK 1'b0: Inactive clear 1'b1: Clears the counter

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2.3.2.86 MSS_CTRL_LOCK0_KICK0 Register

2.3.2.86.1 MSS_CTRL_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component.

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Table 2-346. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1008h

Figure 2-172. MSS_CTRL_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 2-347. MSS_CTRL_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component

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2.3.2.87 MSS_CTRL_LOCK0_KICK1 Register

2.3.2.87.1 MSS_CTRL_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component.

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Table 2-348. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 100Ch

Figure 2-173. MSS_CTRL_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 2-349. MSS_CTRL_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component

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2.3.2.88 MSS_CTRL_INTR_RAW_STATUS Register

2.3.2.88.1 MSS_CTRL_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register.

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Table 2-350. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1010h

Figure 2-174. MSS_CTRL_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 2-351. MSS_CTRL_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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2.3.2.89 MSS_CTRL_INTR_ENABLED_STATUS_CLEAR Register

2.3.2.89.1 MSS_CTRL_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register.

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Table 2-352. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1014h

Figure 2-175. MSS_CTRL_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 2-353. MSS_CTRL_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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2.3.2.90 MSS_CTRL_INTR_ENABLE Register

2.3.2.90.1 MSS_CTRL_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register.

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Table 2-354. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1018h

Figure 2-176. MSS_CTRL_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 2-355. MSS_CTRL_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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2.3.2.91 MSS_CTRL_INTR_ENABLE_CLEAR Register

2.3.2.91.1 MSS_CTRL_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register.

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Table 2-356. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 101Ch

Figure 2-177. MSS_CTRL_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 2-357. MSS_CTRL_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

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2.3.2.92 MSS_CTRL_EOI Register

2.3.2.92.1 MSS_CTRL_EOI Register (Offset = 1020h) [reset = 0h]

EOI register.

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Table 2-358. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1020h

Figure 2-178. MSS_CTRL_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 2-359. MSS_CTRL_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip.

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2.3.2.93 MSS_CTRL_FAULT_ADDRESS Register

2.3.2.93.1 MSS_CTRL_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register.

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Table 2-360. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1024h

Figure 2-179. MSS_CTRL_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 2-361. MSS_CTRL_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address.

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2.3.2.94 MSS_CTRL_FAULT_TYPE_STATUS Register

2.3.2.94.1 MSS_CTRL_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register.

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Table 2-362. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1028h

Figure 2-180. MSS_CTRL_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 2-363. MSS_CTRL_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access.
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

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2.3.2.95 MSS_CTRL_FAULT_ATTR_STATUS Register

2.3.2.95.1 MSS_CTRL_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register.

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Table 2-364. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 102Ch

Figure 2-181. MSS_CTRL_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
FAULT_ROUTEID							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_PRIVID							
R							
0h							

Table 2-365. MSS_CTRL_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID.
19:8	FAULT_ROUTEID	R	0h	Route ID.
7:0	FAULT_PRIVID	R	0h	Privilege ID.

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2.3.2.96 MSS_CTRL_FAULT_CLEAR Register

2.3.2.96.1 MSS_CTRL_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register.

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Table 2-366. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1030h

Figure 2-182. MSS_CTRL_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 2-367. MSS_CTRL_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

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2.3.2.97 MSS_CTRL_R5SS0_CORE0_MBOX_WRITE_DONE Register

2.3.2.97.1 MSS_CTRL_R5SS0_CORE0_MBOX_WRITE_DONE Register (Offset = 4000h) [reset = 0h]

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Table 2-368. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4000h

Figure 2-183. MSS_CTRL_R5SS0_CORE0_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS0_CORE0_MBOX_WRITE_DONE_PROC_7	RESERVED			R5SS0_CORE0_MBOX_WRITE_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R5SS0_CORE0_MBOX_WRITE_DONE_PROC_5	RESERVED			R5SS0_CORE0_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R5SS0_CORE0_MBOX_WRITE_DONE_PROC_3	RESERVED			R5SS0_CORE0_MBOX_WRITE_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS0_CORE0_MBOX_WRITE_DONE_PROC_1	RESERVED			R5SS0_CORE0_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-369. MSS_CTRL_R5SS0_CORE0_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS0_CORE0_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 7
27:25	RESERVED	NONE	0h	Reserved
24	R5SS0_CORE0_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 6
23:21	RESERVED	NONE	0h	Reserved
20	R5SS0_CORE0_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 5
19:17	RESERVED	NONE	0h	Reserved

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Table 2-369. MSS_CTRL_R5SS0_CORE0_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	R5SS0_CORE0_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 4
15:13	RESERVED	NONE	0h	Reserved
12	R5SS0_CORE0_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 3
11:9	RESERVED	NONE	0h	Reserved
8	R5SS0_CORE0_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 2
7:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CORE0_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 1
3:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CORE0_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.2.98 MSS_CTRL_R5SS0_CORE0_MBOX_READ_REQ Register

2.3.2.98.1 MSS_CTRL_R5SS0_CORE0_MBOX_READ_REQ Register (Offset = 4004h) [reset = 0h]

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Table 2-370. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4004h

Figure 2-184. MSS_CTRL_R5SS0_CORE0_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS0_CORE0_MBOX_READ_REQ_PROC_7	RESERVED			R5SS0_CORE0_MBOX_READ_REQ_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R5SS0_CORE0_MBOX_READ_REQ_PROC_5	RESERVED			R5SS0_CORE0_MBOX_READ_REQ_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R5SS0_CORE0_MBOX_READ_REQ_PROC_3	RESERVED			R5SS0_CORE0_MBOX_READ_REQ_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS0_CORE0_MBOX_READ_REQ_PROC_1	RESERVED			R5SS0_CORE0_MBOX_READ_REQ_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-371. MSS_CTRL_R5SS0_CORE0_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS0_CORE0_MBOX_READ_REQ_PROC_7	R/W	0h	This is request from processor 7 to mss_cr5a. Requesting it to read from mailbox.
27:25	RESERVED	NONE	0h	Reserved
24	R5SS0_CORE0_MBOX_READ_REQ_PROC_6	R/W	0h	This is request from processor 6 to mss_cr5a. Requesting it to read from mailbox.
23:21	RESERVED	NONE	0h	Reserved
20	R5SS0_CORE0_MBOX_READ_REQ_PROC_5	R/W	0h	This is request from processor 5 to mss_cr5a. Requesting it to read from mailbox.
19:17	RESERVED	NONE	0h	Reserved
16	R5SS0_CORE0_MBOX_READ_REQ_PROC_4	R/W	0h	This is request from processor 4 to mss_cr5a. Requesting it to read from mailbox.
15:13	RESERVED	NONE	0h	Reserved

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Table 2-371. MSS_CTRL_R5SS0_CORE0_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	R5SS0_CORE0_MBOX_READ_REQ_PROC_3	R/W	0h	This is request from processor 3 to mss_cr5a. Requesting it to read from mailbox.
11:9	RESERVED	NONE	0h	Reserved
8	R5SS0_CORE0_MBOX_READ_REQ_PROC_2	R/W	0h	This is request from processor 2 to mss_cr5a. Requesting it to read from mailbox.
7:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CORE0_MBOX_READ_REQ_PROC_1	R/W	0h	This is request from processor 1 to mss_cr5a. Requesting it to read from mailbox.
3:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CORE0_MBOX_READ_REQ_PROC_0	R/W	0h	This is request from processor 0 to mss_cr5a. Requesting it to read from mailbox.

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2.3.2.99 MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE_ACK Register

2.3.2.99.1 MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE_ACK Register (Offset = 4008h) [reset = 0h]

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Table 2-372. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4008h

Figure 2-185. MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS0_CORE0_MBOX_READ_DONE_ACK_PROC							
R/W							
0h							

Table 2-373. MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	R5SS0_CORE0_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7:Wrting 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5

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2.3.2.100 MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE Register

2.3.2.100.1 MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE Register (Offset = 400Ch) [reset = 0h]

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Table 2-374. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 400Ch

Figure 2-186. MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS0_CORE0_MBOX_READ_DONE_PROC_7	RESERVED			R5SS0_CORE0_MBOX_READ_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R5SS0_CORE0_MBOX_READ_DONE_PROC_5	RESERVED			R5SS0_CORE0_MBOX_READ_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R5SS0_CORE0_MBOX_READ_DONE_PROC_3	RESERVED			R5SS0_CORE0_MBOX_READ_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS0_CORE0_MBOX_READ_DONE_PROC_1	RESERVED			R5SS0_CORE0_MBOX_READ_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-375. MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS0_CORE0_MBOX_READ_DONE_PROC_7	R/W	0h	This register should be written once finishing Reading from proc7's mailbox written by CR5A
27:25	RESERVED	NONE	0h	Reserved
24	R5SS0_CORE0_MBOX_READ_DONE_PROC_6	R/W	0h	This register should be written once finishing Reading from proc6's mailbox written by CR5A
23:21	RESERVED	NONE	0h	Reserved
20	R5SS0_CORE0_MBOX_READ_DONE_PROC_5	R/W	0h	This register should be written once finishing Reading from proc5's mailbox written by CR5A
19:17	RESERVED	NONE	0h	Reserved
16	R5SS0_CORE0_MBOX_READ_DONE_PROC_4	R/W	0h	This register should be written once finishing Reading from proc4's mailbox written by CR5A
15:13	RESERVED	NONE	0h	Reserved

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Table 2-375. MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	R5SS0_CORE0_MBOX_READ_DONE_PROC_3	R/W	0h	This register should be written once finishing Reading from proc3's mailbox written by CR5A
11:9	RESERVED	NONE	0h	Reserved
8	R5SS0_CORE0_MBOX_READ_DONE_PROC_2	R/W	0h	This register should be written once finishing Reading from proc2's mailbox written by CR5A
7:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CORE0_MBOX_READ_DONE_PROC_1	R/W	0h	This register should be written once finishing Reading from proc1's mailbox written by CR5A
3:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CORE0_MBOX_READ_DONE_PROC_0	R/W	0h	This register should be written once finishing Reading from proc0's mailbox written by CR5A

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2.3.2.101 MSS_CTRL_R5SS0_CORE0_SW_INT Register

2.3.2.101.1 MSS_CTRL_R5SS0_CORE0_SW_INT Register (Offset = 4010h) [reset = 0h]

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Table 2-376. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4010h

Figure 2-187. MSS_CTRL_R5SS0_CORE0_SW_INT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS0_CORE0_SW_INT_PULSE
NONE							R/W
0h							0h

Table 2-377. MSS_CTRL_R5SS0_CORE0_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CORE0_SW_INT_PULSE	R/W	0h	Write_pulse bit field: Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B.

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2.3.2.102 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_MASK Register

2.3.2.102.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_MASK Register (Offset = 4020h) [reset = 0h]

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Table 2-378. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4020h

Figure 2-188. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_F_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_E_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_R5SS1_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_R5SS0_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_OPTI_FLASH_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_HSM_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B1_AHB_ADDR_ERR0
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A1_AHB_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B0_AHB_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A0_AHB_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_SCRM2SCRP1_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_SCRM2SCRP0_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_OSPI_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_MBOX_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_DTHE_A_ADDR_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B1_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A1_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B0_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A0_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_D_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_C_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_B_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_A_ADDR_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-379. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_F_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
21	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_E_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-379. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_R5SS1_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
19	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_R5SS0_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
18	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_OPTI_FLASH_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
17	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_HSM_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
16	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B1_AHB_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
15	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A1_AHB_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
14	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B0_AHB_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
13	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A0_AHB_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
12	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_SCRM2SCRP1_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
11	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_SCRM2SCRP0_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
10	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_OSPI_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
9	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_MBOX_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
8	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_DTHE_A_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
7	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B1_AXIS_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
6	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A1_AXIS_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-379. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B0_AXIS_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
4	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A0_AXIS_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
3	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_D_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
2	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_C_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
1	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_B_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
0	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_A_ADDR_ERR0	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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2.3.2.103 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS Register

2.3.2.103.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS Register (Offset = 4024h) [reset = 0h]

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Table 2-380. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4024h

Figure 2-189. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_F_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_E_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_R5SS1_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_R5SS0_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_OPTI_FLASH_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_HSM_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B1_AHB_ADDR_ERR0
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A1_AHB_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B0_AHB_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A0_AHB_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_SCRM2SCRP1_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_SCRM2SCRP0_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_OSPI_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_MBOX_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_DTHE_A_ADDR_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B1_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A1_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B0_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A0_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_D_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_C_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_B_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_A_ADDR_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-381. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_F_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
21	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_E_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-381. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_R5SS1_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
19	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_R5SS0_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
18	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_OPTI_FLASH_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
17	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_HSM_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
16	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B1_AHB_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
15	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A1_AHB_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
14	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B0_AHB_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
13	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A0_AHB_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
12	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_SCRM2SCRP1_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
11	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_SCRM2SCRP0_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
10	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_OSPI_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
9	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_MBOX_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
8	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_DTHE_A_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
7	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B1_AXIS_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
6	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A1_AXIS_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-381. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B0_AXIS_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
4	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A0_AXIS_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
3	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_D_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
2	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_C_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
1	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_B_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_A_ADDR_ERR0	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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2.3.2.104 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS_RAW Register

2.3.2.104.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS_RAW Register (Offset = 4028h) [reset = 0h]

Return to Summary Table

Table 2-382. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4028h

Figure 2-190. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_F_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_E_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_R5SS1_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_R5SS0_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_OPTI_FLASH_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_HSM_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR0
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_OSPI_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_MBOX_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_DTHE_A_ADDR_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-383. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_F_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
21	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_E_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-383. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_R5SS1_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
19	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_R5SS0_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
18	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_OPTI_FLASH_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
17	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_HSM_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
16	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
15	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
14	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
13	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
12	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
11	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
10	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_OSPI_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
9	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_MBOX_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
8	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_DTHE_A_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
7	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
6	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-383. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
4	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
3	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
2	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
1	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
0	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR0	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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2.3.2.105 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_MASK Register

2.3.2.105.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_MASK Register (Offset = 4030h) [reset = 0h]

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Table 2-384. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4030h

Figure 2-191. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_F_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_E_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_R5SS1_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_R5SS0_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_OPTI_FLASH_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_HSM_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B1_AHB_PROT_ERR0
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A1_AHB_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B0_AHB_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A0_AHB_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_SCRM2SCRP1_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_SCRM2SCRP0_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_OSPI_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_MBOX_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_DTHE_A_PROT_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B1_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A1_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B0_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A0_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_D_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_C_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_B_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_A_PROT_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-385. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_F_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
21	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_E_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-385. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_R5SS1_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
19	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_R5SS0_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
18	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_OPTI_FLASH_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
17	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_HSM_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
16	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B1_AHB_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
15	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A1_AHB_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
14	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B0_AHB_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
13	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A0_AHB_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
12	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_SCRM2SCRP1_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
11	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_SCRM2SCRP0_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
10	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_OSPI_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
9	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_MBOX_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
8	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_DTHE_A_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
7	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B1_AXIS_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
6	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A1_AXIS_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-385. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5B0_AXIS_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
4	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_CR5A0_AXIS_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
3	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_D_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
2	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_C_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
1	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_B_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
0	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK_MPU_L2_BANK_A_PROT_ERR0	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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2.3.2.106 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS Register

2.3.2.106.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS Register (Offset = 4034h) [reset = 0h]

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Table 2-386. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4034h

Figure 2-192. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_F_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_E_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_R5SS1_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_R5SS0_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_OPTI_FLASH_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_HSM_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B1_AHB_PROT_ERR0
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A1_AHB_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B0_AHB_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A0_AHB_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_SCRM2SCRP1_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_SCRM2SCRP0_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_OSPI_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_MBOX_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_DTHE_A_PROT_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B1_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A1_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B0_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A0_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_D_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_C_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_B_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_A_PROT_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-387. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_F_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
21	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_E_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-387. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_R5SS1_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
19	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_R5SS0_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
18	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_OPTI_FLASH_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
17	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_HSM_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
16	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B1_AHB_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
15	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A1_AHB_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
14	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B0_AHB_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
13	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A0_AHB_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
12	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_SCRM2SCRP1_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
11	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_SCRM2SCRP0_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
10	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_OSPI_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
9	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_MBOX_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
8	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_DTHE_A_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
7	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B1_AXIS_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
6	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A1_AXIS_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-387. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5B0_AXIS_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
4	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_CR5A0_AXIS_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
3	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_D_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
2	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_C_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
1	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_B_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_MPU_L2_BANK_A_PROT_ERR0	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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2.3.2.107 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS_RAW Register

2.3.2.107.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS_RAW Register (Offset = 4038h) [reset = 0h]

Return to Summary Table

Table 2-388. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4038h

Figure 2-193. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_F_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_E_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_R5SS1_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_R5SS0_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_OPTI_FLASH_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_HSM_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR0
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A1_AHB_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B0_AHB_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A0_AHB_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_OSPI_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_MBOX_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_DTHE_A_PROT_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B1_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A1_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B0_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A0_AXIS_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-389. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_F_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
21	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_E_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-389. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_R5SS1_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
19	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_R5SS0_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
18	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_OPTI_FLASH_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
17	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_HSM_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
16	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
15	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A1_AHB_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
14	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B0_AHB_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
13	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A0_AHB_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
12	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
11	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
10	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_OSPI_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
9	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_MBOX_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
8	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_DTHE_A_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
7	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B1_AXIS_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
6	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A1_AXIS_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-389. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5B0_AXIS_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
4	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_CR5A0_AXIS_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
3	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
2	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
1	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
0	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR0	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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2.3.2.108 MSS_CTRL_R5SS0_CORE1_MBOX_WRITE_DONE Register

2.3.2.108.1 MSS_CTRL_R5SS0_CORE1_MBOX_WRITE_DONE Register (Offset = 8000h) [reset = 0h]

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Table 2-390. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8000h

Figure 2-194. MSS_CTRL_R5SS0_CORE1_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS0_CORE1_MBOX_WRITE_DONE_PROC_7	RESERVED			R5SS0_CORE1_MBOX_WRITE_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	22	21	20	19	18	17	16
RESERVED			R5SS0_CORE1_MBOX_WRITE_DONE_PROC_5	RESERVED			R5SS0_CORE1_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	14	13	12	11	10	9	8
RESERVED			R5SS0_CORE1_MBOX_WRITE_DONE_PROC_3	RESERVED			R5SS0_CORE1_MBOX_WRITE_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED			R5SS0_CORE1_MBOX_WRITE_DONE_PROC_1	RESERVED			R5SS0_CORE1_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-391. MSS_CTRL_R5SS0_CORE1_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS0_CORE1_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 7
27:25	RESERVED	NONE	0h	Reserved
24	R5SS0_CORE1_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 6
23:21	RESERVED	NONE	0h	Reserved
20	R5SS0_CORE1_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 5
19:17	RESERVED	NONE	0h	Reserved

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Table 2-391. MSS_CTRL_R5SS0_CORE1_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	R5SS0_CORE1_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 4
15:13	RESERVED	NONE	0h	Reserved
12	R5SS0_CORE1_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 3
11:9	RESERVED	NONE	0h	Reserved
8	R5SS0_CORE1_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 2
7:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CORE1_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 1
3:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CORE1_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.2.109 MSS_CTRL_R5SS0_CORE1_MBOX_READ_REQ Register

2.3.2.109.1 MSS_CTRL_R5SS0_CORE1_MBOX_READ_REQ Register (Offset = 8004h) [reset = 0h]

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Table 2-392. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8004h

Figure 2-195. MSS_CTRL_R5SS0_CORE1_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS0_CORE1_MBOX_READ_REQ_PROC_7	RESERVED			R5SS0_CORE1_MBOX_READ_REQ_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	22	21	20	19	18	17	16
RESERVED			R5SS0_CORE1_MBOX_READ_REQ_PROC_5	RESERVED			R5SS0_CORE1_MBOX_READ_REQ_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	14	13	12	11	10	9	8
RESERVED			R5SS0_CORE1_MBOX_READ_REQ_PROC_3	RESERVED			R5SS0_CORE1_MBOX_READ_REQ_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED			R5SS0_CORE1_MBOX_READ_REQ_PROC_1	RESERVED			R5SS0_CORE1_MBOX_READ_REQ_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-393. MSS_CTRL_R5SS0_CORE1_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS0_CORE1_MBOX_READ_REQ_PROC_7	R/W	0h	This is request from processor 7 to mss_CR5B. Requesting it to read from mailbox.
27:25	RESERVED	NONE	0h	Reserved
24	R5SS0_CORE1_MBOX_READ_REQ_PROC_6	R/W	0h	This is request from processor 6 to mss_CR5B. Requesting it to read from mailbox.
23:21	RESERVED	NONE	0h	Reserved
20	R5SS0_CORE1_MBOX_READ_REQ_PROC_5	R/W	0h	This is request from processor 5 to mss_CR5B. Requesting it to read from mailbox.
19:17	RESERVED	NONE	0h	Reserved
16	R5SS0_CORE1_MBOX_READ_REQ_PROC_4	R/W	0h	This is request from processor 4 to mss_CR5B. Requesting it to read from mailbox.
15:13	RESERVED	NONE	0h	Reserved

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Table 2-393. MSS_CTRL_R5SS0_CORE1_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	R5SS0_CORE1_MBOX_READ_REQ_PROC_3	R/W	0h	This is request from processor 3 to mss_CR5B. Requesting it to read from mailbox.
11:9	RESERVED	NONE	0h	Reserved
8	R5SS0_CORE1_MBOX_READ_REQ_PROC_2	R/W	0h	This is request from processor 2 to mss_CR5B. Requesting it to read from mailbox.
7:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CORE1_MBOX_READ_REQ_PROC_1	R/W	0h	This is request from processor 1 to mss_CR5B. Requesting it to read from mailbox.
3:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CORE1_MBOX_READ_REQ_PROC_0	R/W	0h	This is request from processor 0 to mss_CR5B. Requesting it to read from mailbox.

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2.3.2.110 MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE_ACK Register

2.3.2.110.1 MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE_ACK Register (Offset = 8008h) [reset = 0h]

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Table 2-394. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8008h

Figure 2-196. MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
R5SS0_CORE1_MBOX_READ_DONE_ACK_PROC							
R/W							
0h							

Table 2-395. MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	R5SS0_CORE1_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7:Wrting 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5

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2.3.2.111 MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE Register

2.3.2.111.1 MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE Register (Offset = 800Ch) [reset = 0h]

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Table 2-396. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 800Ch

Figure 2-197. MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS0_CORE1_MBOX_READ_DONE_PROC_7	RESERVED			R5SS0_CORE1_MBOX_READ_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R5SS0_CORE1_MBOX_READ_DONE_PROC_5	RESERVED			R5SS0_CORE1_MBOX_READ_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R5SS0_CORE1_MBOX_READ_DONE_PROC_3	RESERVED			R5SS0_CORE1_MBOX_READ_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS0_CORE1_MBOX_READ_DONE_PROC_1	RESERVED			R5SS0_CORE1_MBOX_READ_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-397. MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS0_CORE1_MBOX_READ_DONE_PROC_7	R/W	0h	This register should be written once finishing Reading from proc7's mailbox written by CR5B
27:25	RESERVED	NONE	0h	Reserved
24	R5SS0_CORE1_MBOX_READ_DONE_PROC_6	R/W	0h	This register should be written once finishing Reading from proc6's mailbox written by CR5B
23:21	RESERVED	NONE	0h	Reserved
20	R5SS0_CORE1_MBOX_READ_DONE_PROC_5	R/W	0h	This register should be written once finishing Reading from proc5's mailbox written by CR5B
19:17	RESERVED	NONE	0h	Reserved
16	R5SS0_CORE1_MBOX_READ_DONE_PROC_4	R/W	0h	This register should be written once finishing Reading from proc4's mailbox written by CR5B
15:13	RESERVED	NONE	0h	Reserved

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Table 2-397. MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	R5SS0_CORE1_MBOX_READ_DONE_PROC_3	R/W	0h	This register should be written once finishing Reading from proc3's mailbox written by CR5B
11:9	RESERVED	NONE	0h	Reserved
8	R5SS0_CORE1_MBOX_READ_DONE_PROC_2	R/W	0h	This register should be written once finishing Reading from proc2's mailbox written by CR5B
7:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CORE1_MBOX_READ_DONE_PROC_1	R/W	0h	This register should be written once finishing Reading from proc1's mailbox written by CR5B
3:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CORE1_MBOX_READ_DONE_PROC_0	R/W	0h	This register should be written once finishing Reading from proc0's mailbox written by CR5B

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2.3.2.112 MSS_CTRL_R5SS0_CORE1_SW_INT Register

2.3.2.112.1 MSS_CTRL_R5SS0_CORE1_SW_INT Register (Offset = 8010h) [reset = 0h]

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Table 2-398. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8010h

Figure 2-198. MSS_CTRL_R5SS0_CORE1_SW_INT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							R5SS0_CORE1_SW_INT_PULSE
NONE							R/W
0h							0h

Table 2-399. MSS_CTRL_R5SS0_CORE1_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS0_CORE1_SW_INT_PULSE	R/W	0h	Write_pulse bit field: Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B.

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2.3.2.113 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_MASK Register

2.3.2.113.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_MASK Register (Offset = 8020h) [reset = 0h]

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Table 2-400. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8020h

Figure 2-199. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_F_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_E_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_R5SS1_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_R5SS0_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_OPTI_FLASH_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_HSM_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B1_AHB_ADDR_ERR1
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A1_AHB_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B0_AHB_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A0_AHB_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_SCRM2SCRP1_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_SCRM2SCRP0_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_OSPI_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_MBOX_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_DTHE_A_ADDR_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B1_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A1_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B0_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A0_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_D_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_C_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_B_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_A_ADDR_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-401. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_F_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
21	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_E_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-401. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_R5SS1_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
19	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_R5SS0_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
18	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_OPTI_FLASH_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
17	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_HSM_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
16	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B1_AHB_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
15	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A1_AHB_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
14	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B0_AHB_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
13	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A0_AHB_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
12	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_SCRM2SCRP1_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
11	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_SCRM2SCRP0_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
10	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_OSPI_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
9	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_MBOX_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
8	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_DTHE_A_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
7	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B1_AXIS_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
6	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A1_AXIS_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-401. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B0_AXIS_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
4	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A0_AXIS_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
3	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_D_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
2	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_C_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
1	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_B_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
0	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_A_ADDR_ERR1	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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2.3.2.114 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS Register

2.3.2.114.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS Register (Offset = 8024h) [reset = 0h]

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Table 2-402. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8024h

Figure 2-200. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_F_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_E_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_R5SS1_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_R5SS0_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_OPTI_FLASH_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_HSM_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B1_AHB_ADDR_ERR1
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A1_AHB_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B0_AHB_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A0_AHB_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_SCRM2SCRP1_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_SCRM2SCRP0_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_OSPI_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_MBOX_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_DTHE_A_ADDR_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B1_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A1_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B0_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A0_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_D_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_C_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_B_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_A_ADDR_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-403. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_F_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
21	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_E_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-403. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_R5SS1_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
19	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_R5SS0_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
18	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_OPTI_FLASH_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
17	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_HSM_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
16	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B1_AHB_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
15	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A1_AHB_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
14	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B0_AHB_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
13	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A0_AHB_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
12	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_SCRM2SCRP1_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
11	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_SCRM2SCRP0_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
10	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_OSPI_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
9	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_MBOX_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
8	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_DTHE_A_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
7	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B1_AXIS_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
6	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A1_AXIS_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-403. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B0_AXIS_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
4	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A0_AXIS_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
3	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_D_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
2	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_C_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_B_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
0	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_A_ADDR_ERR1	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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2.3.2.115 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS_RAW Register

2.3.2.115.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS_RAW Register (Offset = 8028h) [reset = 0h]

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Table 2-404. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8028h

Figure 2-201. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_F_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_E_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_R5SS1_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_R5SS0_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_OPTI_FLASH_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_HSM_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR1
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_OSPI_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_MBOX_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_DTHE_A_ADDR_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-405. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_F_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
21	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_E_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-405. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_R5SS1_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
19	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_R5SS0_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
18	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_OPTI_FLASH_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
17	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_HSM_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
16	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
15	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
14	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
13	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
12	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
11	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
10	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_OSPI_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
9	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_MBOX_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
8	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_DTHE_A_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
7	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
6	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-405. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CORE1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
4	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
3	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
2	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
1	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
0	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR1	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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2.3.2.116 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_MASK Register

2.3.2.116.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_MASK Register (Offset = 8030h) [reset = 0h]

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Table 2-406. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8030h

Figure 2-202. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_F_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_E_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_R5SS1_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_R5SS0_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_OPTI_FLASH_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_HSM_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B1_AHB_PROT_ERR1
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A1_AHB_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B0_AHB_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A0_AHB_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_SCRM2SCRP1_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_SCRM2SCRP0_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_OSPI_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_MBOX_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_DTHE_A_PROT_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B1_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A1_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B0_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A0_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_D_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_C_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_B_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_A_PROT_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-407. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_F_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
21	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_E_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-407. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_R5SS1_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
19	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_R5SS0_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
18	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_OPTI_FLASH_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
17	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_HSM_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
16	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B1_AHB_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
15	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A1_AHB_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
14	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B0_AHB_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
13	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A0_AHB_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
12	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_SCRM2SCRP1_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
11	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_SCRM2SCRP0_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
10	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_OSPI_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
9	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_MBOX_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
8	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_DTHE_A_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
7	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B1_AXIS_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
6	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A1_AXIS_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-407. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5B0_AXIS_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
4	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_CR5A0_AXIS_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
3	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_D_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
2	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_C_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
1	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_B_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
0	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK_MPU_L2_BANK_A_PROT_ERR1	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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2.3.2.117 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS Register

2.3.2.117.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS Register (Offset = 8034h) [reset = 0h]

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Table 2-408. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8034h

Figure 2-203. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_F_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_E_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_R5SS1_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_R5SS0_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_OPTI_FLASH_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_HSM_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B1_AHB_PROT_ERR1
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A1_AHB_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B0_AHB_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A0_AHB_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_SCRM2SCRP1_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_SCRM2SCRP0_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_OSPI_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_MBOX_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_DTHE_A_PROT_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B1_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A1_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B0_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A0_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_D_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_C_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_B_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_A_PROT_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-409. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_F_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
21	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_E_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-409. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_R5SS1_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
19	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_R5SS0_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
18	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_OPTI_FLASH_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
17	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_HSM_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
16	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B1_AHB_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
15	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A1_AHB_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
14	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B0_AHB_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
13	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A0_AHB_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
12	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_SCRM2SCRP1_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
11	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_SCRM2SCRP0_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
10	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_OSPI_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
9	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_MBOX_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
8	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_DTHE_A_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
7	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B1_AXIS_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
6	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A1_AXIS_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-409. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5B0_AXIS_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
4	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_CR5A0_AXIS_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
3	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_D_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
2	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_C_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_B_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
0	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_MPU_L2_BANK_A_PROT_ERR1	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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2.3.2.118 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS_RAW Register

2.3.2.118.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS_RAW Register (Offset = 8038h) [reset = 0h]

Return to Summary Table

Table 2-410. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8038h

Figure 2-204. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_F_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_E_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_R5SS1_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_R5SS0_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_OPTI_FLASH_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_HSM_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR1
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A1_AHB_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B0_AHB_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A0_AHB_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_OSPI_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_MBOX_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_DTHE_A_PROT_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B1_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A1_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B0_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A0_AXIS_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-411. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_F_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
21	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_E_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-411. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_R5SS1_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
19	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_R5SS0_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
18	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_OPTI_FLASH_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
17	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_HSM_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
16	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
15	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A1_AHB_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
14	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B0_AHB_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
13	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A0_AHB_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
12	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
11	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
10	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_OSPI_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
9	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_MBOX_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
8	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_DTHE_A_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
7	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B1_AXIS_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
6	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A1_AXIS_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-411. MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CORE1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5B0_AXIS_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
4	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_CR5A0_AXIS_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
3	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
2	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
1	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
0	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR1	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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2.3.2.119 MSS_CTRL_R5SS1_CORE0_MBOX_WRITE_DONE Register

2.3.2.119.1 MSS_CTRL_R5SS1_CORE0_MBOX_WRITE_DONE Register (Offset = C000h) [reset = 0h]

Return to Summary Table

Table 2-412. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C000h

Figure 2-205. MSS_CTRL_R5SS1_CORE0_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS1_CORE0_MBOX_WRITE_DONE_PROC_7	RESERVED			R5SS1_CORE0_MBOX_WRITE_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R5SS1_CORE0_MBOX_WRITE_DONE_PROC_5	RESERVED			R5SS1_CORE0_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R5SS1_CORE0_MBOX_WRITE_DONE_PROC_3	RESERVED			R5SS1_CORE0_MBOX_WRITE_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS1_CORE0_MBOX_WRITE_DONE_PROC_1	RESERVED			R5SS1_CORE0_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-413. MSS_CTRL_R5SS1_CORE0_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS1_CORE0_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 7
27:25	RESERVED	NONE	0h	Reserved
24	R5SS1_CORE0_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 6
23:21	RESERVED	NONE	0h	Reserved
20	R5SS1_CORE0_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 5
19:17	RESERVED	NONE	0h	Reserved

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Table 2-413. MSS_CTRL_R5SS1_CORE0_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	R5SS1_CORE0_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 4
15:13	RESERVED	NONE	0h	Reserved
12	R5SS1_CORE0_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 3
11:9	RESERVED	NONE	0h	Reserved
8	R5SS1_CORE0_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 2
7:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CORE0_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 1
3:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CORE0_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.2.120 MSS_CTRL_R5SS1_CORE0_MBOX_READ_REQ Register

2.3.2.120.1 MSS_CTRL_R5SS1_CORE0_MBOX_READ_REQ Register (Offset = C004h) [reset = 0h]

Return to Summary Table

Table 2-414. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C004h

Figure 2-206. MSS_CTRL_R5SS1_CORE0_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS1_CORE0_MBOX_READ_REQ_PROC_7	RESERVED			R5SS1_CORE0_MBOX_READ_REQ_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	22	21	20	19	18	17	16
RESERVED			R5SS1_CORE0_MBOX_READ_REQ_PROC_5	RESERVED			R5SS1_CORE0_MBOX_READ_REQ_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	14	13	12	11	10	9	8
RESERVED			R5SS1_CORE0_MBOX_READ_REQ_PROC_3	RESERVED			R5SS1_CORE0_MBOX_READ_REQ_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED			R5SS1_CORE0_MBOX_READ_REQ_PROC_1	RESERVED			R5SS1_CORE0_MBOX_READ_REQ_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-415. MSS_CTRL_R5SS1_CORE0_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS1_CORE0_MBOX_READ_REQ_PROC_7	R/W	0h	This is request from processor 7 to mss_cr5a. Requesting it to read from mailbox.
27:25	RESERVED	NONE	0h	Reserved
24	R5SS1_CORE0_MBOX_READ_REQ_PROC_6	R/W	0h	This is request from processor 6 to mss_cr5a. Requesting it to read from mailbox.
23:21	RESERVED	NONE	0h	Reserved
20	R5SS1_CORE0_MBOX_READ_REQ_PROC_5	R/W	0h	This is request from processor 5 to mss_cr5a. Requesting it to read from mailbox.
19:17	RESERVED	NONE	0h	Reserved
16	R5SS1_CORE0_MBOX_READ_REQ_PROC_4	R/W	0h	This is request from processor 4 to mss_cr5a. Requesting it to read from mailbox.
15:13	RESERVED	NONE	0h	Reserved

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Table 2-415. MSS_CTRL_R5SS1_CORE0_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	R5SS1_CORE0_MBOX_READ_REQ_PROC_3	R/W	0h	This is request from processor 3 to mss_cr5a. Requesting it to read from mailbox.
11:9	RESERVED	NONE	0h	Reserved
8	R5SS1_CORE0_MBOX_READ_REQ_PROC_2	R/W	0h	This is request from processor 2 to mss_cr5a. Requesting it to read from mailbox.
7:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CORE0_MBOX_READ_REQ_PROC_1	R/W	0h	This is request from processor 1 to mss_cr5a. Requesting it to read from mailbox.
3:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CORE0_MBOX_READ_REQ_PROC_0	R/W	0h	This is request from processor 0 to mss_cr5a. Requesting it to read from mailbox.

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2.3.2.121 MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE_ACK Register

2.3.2.121.1 MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE_ACK Register (Offset = C008h) [reset = 0h]

Return to Summary Table

Table 2-416. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C008h

Figure 2-207. MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
R5SS1_CORE0_MBOX_READ_DONE_ACK_PROC							
R/W							
0h							

Table 2-417. MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	R5SS1_CORE0_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7:Wrting 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5

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2.3.2.122 MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE Register

2.3.2.122.1 MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE Register (Offset = C00Ch) [reset = 0h]

Return to Summary Table

Table 2-418. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C00Ch

Figure 2-208. MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS1_CORE0_MBOX_READ_DONE_PROC_7	RESERVED			R5SS1_CORE0_MBOX_READ_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R5SS1_CORE0_MBOX_READ_DONE_PROC_5	RESERVED			R5SS1_CORE0_MBOX_READ_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R5SS1_CORE0_MBOX_READ_DONE_PROC_3	RESERVED			R5SS1_CORE0_MBOX_READ_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS1_CORE0_MBOX_READ_DONE_PROC_1	RESERVED			R5SS1_CORE0_MBOX_READ_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-419. MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS1_CORE0_MBOX_READ_DONE_PROC_7	R/W	0h	This register should be written once finishing Reading from proc7's mailbox written by CR5A
27:25	RESERVED	NONE	0h	Reserved
24	R5SS1_CORE0_MBOX_READ_DONE_PROC_6	R/W	0h	This register should be written once finishing Reading from proc6's mailbox written by CR5A
23:21	RESERVED	NONE	0h	Reserved
20	R5SS1_CORE0_MBOX_READ_DONE_PROC_5	R/W	0h	This register should be written once finishing Reading from proc5's mailbox written by CR5A
19:17	RESERVED	NONE	0h	Reserved
16	R5SS1_CORE0_MBOX_READ_DONE_PROC_4	R/W	0h	This register should be written once finishing Reading from proc4's mailbox written by CR5A
15:13	RESERVED	NONE	0h	Reserved

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Table 2-419. MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	R5SS1_CORE0_MBOX_READ_DONE_PROC_3	R/W	0h	This register should be written once finishing Reading from proc3's mailbox written by CR5A
11:9	RESERVED	NONE	0h	Reserved
8	R5SS1_CORE0_MBOX_READ_DONE_PROC_2	R/W	0h	This register should be written once finishing Reading from proc2's mailbox written by CR5A
7:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CORE0_MBOX_READ_DONE_PROC_1	R/W	0h	This register should be written once finishing Reading from proc1's mailbox written by CR5A
3:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CORE0_MBOX_READ_DONE_PROC_0	R/W	0h	This register should be written once finishing Reading from proc0's mailbox written by CR5A

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2.3.2.123 MSS_CTRL_R5SS1_CORE0_SW_INT Register

2.3.2.123.1 MSS_CTRL_R5SS1_CORE0_SW_INT Register (Offset = C010h) [reset = 0h]

Return to Summary Table

Table 2-420. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C010h

Figure 2-209. MSS_CTRL_R5SS1_CORE0_SW_INT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS1_CORE0_SW_INT_PULSE
NONE							R/W
0h							0h

Table 2-421. MSS_CTRL_R5SS1_CORE0_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CORE0_SW_INT_PULSE	R/W	0h	Write_pulse bit field: Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B.

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2.3.2.124 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_MASK Register

2.3.2.124.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_MASK Register (Offset = C020h) [reset = 0h]

Return to Summary Table

Table 2-422. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C020h

Figure 2-210. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_F_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_E_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_R5SS1_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_R5SS0_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_OPTI_FLASH_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_HSM_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B1_AHB_ADDR_ERR2
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A1_AHB_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B0_AHB_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A0_AHB_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_SCRM2SCRP1_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_SCRM2SCRP0_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_OSPI_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_MBOX_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_DTHE_A_ADDR_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B1_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A1_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B0_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A0_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_D_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_C_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_B_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_A_ADDR_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-423. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_F_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
21	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_E_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-423. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_R5SS1_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
19	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_R5SS0_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
18	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_OPTI_FLASH_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
17	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_HSM_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
16	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B1_AHB_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
15	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A1_AHB_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
14	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B0_AHB_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
13	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A0_AHB_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
12	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_SCRM2SCRP1_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
11	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_SCRM2SCRP0_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
10	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_OSPI_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
9	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_MBOX_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
8	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_DTHE_A_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
7	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B1_AXIS_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
6	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A1_AXIS_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-423. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B0_AXIS_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
4	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A0_AXIS_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
3	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_D_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
2	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_C_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
1	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_B_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
0	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_A_ADDR_ERR2	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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2.3.2.125 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS Register

2.3.2.125.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS Register (Offset = C024h) [reset = 0h]

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Table 2-424. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C024h

Figure 2-211. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_F_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_E_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_R5SS1_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_R5SS0_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_OPTI_FLASH_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_HSM_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B1_AHB_ADDR_ERR2
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A1_AHB_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B0_AHB_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A0_AHB_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_SCRM2SCRP1_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_SCRM2SCRP0_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_OSPI_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_MBOX_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_DTHE_A_ADDR_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B1_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A1_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B0_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A0_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_D_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_C_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_B_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_A_ADDR_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-425. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_F_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
21	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_E_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-425. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_R5SS1_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
19	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_R5SS0_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
18	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_OPTI_FLASH_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
17	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_HSM_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
16	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B1_AHB_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
15	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A1_AHB_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
14	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B0_AHB_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
13	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A0_AHB_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
12	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_SCRM2SCRP1_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
11	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_SCRM2SCRP0_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
10	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_OSPI_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
9	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_MBOX_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
8	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_DTHE_A_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
7	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B1_AXIS_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
6	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A1_AXIS_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-425. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B0_AXIS_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
4	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A0_AXIS_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
3	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_D_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_C_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
1	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_B_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
0	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_A_ADDR_ERR2	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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2.3.2.126 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS_RAW Register

2.3.2.126.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS_RAW Register (Offset = C028h) [reset = 0h]

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Table 2-426. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C028h

Figure 2-212. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_F_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_E_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_R5SS1_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_R5SS0_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_OPTI_FLASH_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_HSM_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR2
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_OSPI_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_MBOX_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_DTHE_A_ADDR_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-427. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_F_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
21	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_E_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-427. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_R5SS1_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
19	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_R5SS0_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
18	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_OPTI_FLASH_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
17	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_HSM_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
16	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
15	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
14	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
13	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
12	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
11	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
10	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_OSPI_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
9	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_MBOX_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
8	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_DTHE_A_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
7	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
6	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-427. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
4	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
3	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
2	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
1	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
0	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR2	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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2.3.2.127 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_MASK Register

2.3.2.127.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_MASK Register (Offset = C030h) [reset = 0h]

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Table 2-428. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C030h

Figure 2-213. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_F_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_E_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_R5SS1_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_R5SS0_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_OPTI_FLASH_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_HSM_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B1_AHB_PROT_ERR2
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A1_AHB_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B0_AHB_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A0_AHB_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_SCRM2SCRP1_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_SCRM2SCRP0_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_OSPI_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_MBOX_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_DTHE_A_PROT_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B1_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A1_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B0_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A0_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_D_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_C_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_B_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_A_PROT_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-429. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_F_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
21	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_E_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-429. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_R5SS1_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
19	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_R5SS0_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
18	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_OPTI_FLASH_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
17	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_HSM_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
16	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B1_AHB_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
15	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A1_AHB_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
14	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B0_AHB_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
13	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A0_AHB_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
12	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_SCRM2SCRP1_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
11	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_SCRM2SCRP0_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
10	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_OSPI_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
9	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_MBOX_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
8	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_DTHE_A_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
7	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B1_AXIS_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
6	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A1_AXIS_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-429. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5B0_AXIS_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
4	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_CR5A0_AXIS_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
3	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_D_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
2	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_C_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
1	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_B_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
0	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK_MPU_L2_BANK_A_PROT_ERR2	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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2.3.2.128 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS Register

2.3.2.128.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS Register (Offset = C034h) [reset = 0h]

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Table 2-430. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C034h

Figure 2-214. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_F_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_E_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_R5SS1_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_R5SS0_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_OPTI_FLASH_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_HSM_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B1_AHB_PROT_ERR2
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A1_AHB_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B0_AHB_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A0_AHB_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_SCRM2SCRP1_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_SCRM2SCRP0_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_OSPI_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_MBOX_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_DTHE_A_PROT_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B1_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A1_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B0_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A0_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_D_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_C_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_B_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_A_PROT_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-431. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_F_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
21	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_E_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-431. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_R5SS1_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
19	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_R5SS0_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
18	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_OPTI_FLASH_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
17	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_HSM_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
16	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B1_AHB_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
15	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A1_AHB_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
14	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B0_AHB_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
13	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A0_AHB_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
12	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_SCRM2SCRP1_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
11	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_SCRM2SCRP0_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
10	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_OSPI_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
9	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_MBOX_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
8	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_DTHE_A_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
7	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B1_AXIS_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
6	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A1_AXIS_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-431. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5B0_AXIS_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
4	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_CR5A0_AXIS_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
3	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_D_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_C_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
1	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_B_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
0	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_MPU_L2_BANK_A_PROT_ERR2	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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2.3.2.129 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS_RAW Register

2.3.2.129.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS_RAW Register (Offset = C038h) [reset = 0h]

Return to Summary Table

Table 2-432. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C038h

Figure 2-215. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_F_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_E_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_R5SS1_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_R5SS0_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_OPTI_FLASH_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_HSM_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR2
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A1_AHB_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B0_AHB_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A0_AHB_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_OSPI_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_MBOX_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_DTHE_A_PROT_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B1_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A1_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B0_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A0_AXIS_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-433. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_F_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
21	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_E_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-433. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_R5SS1_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
19	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_R5SS0_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
18	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_OPTI_FLASH_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
17	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_HSM_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
16	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
15	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A1_AHB_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
14	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B0_AHB_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
13	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A0_AHB_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
12	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
11	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
10	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_OSPI_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
9	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_MBOX_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
8	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_DTHE_A_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
7	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B1_AXIS_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
6	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A1_AXIS_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-433. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5B0_AXIS_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
4	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_CR5A0_AXIS_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
3	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
2	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
1	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
0	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR2	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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2.3.2.130 MSS_CTRL_R5SS1_CORE1_MBOX_WRITE_DONE Register

2.3.2.130.1 MSS_CTRL_R5SS1_CORE1_MBOX_WRITE_DONE Register (Offset = 10000h) [reset = 0h]

Return to Summary Table

Table 2-434. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0000h

Figure 2-216. MSS_CTRL_R5SS1_CORE1_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS1_CORE1_MBOX_WRITE_DONE_PROC_7	RESERVED			R5SS1_CORE1_MBOX_WRITE_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R5SS1_CORE1_MBOX_WRITE_DONE_PROC_5	RESERVED			R5SS1_CORE1_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R5SS1_CORE1_MBOX_WRITE_DONE_PROC_3	RESERVED			R5SS1_CORE1_MBOX_WRITE_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS1_CORE1_MBOX_WRITE_DONE_PROC_1	RESERVED			R5SS1_CORE1_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-435. MSS_CTRL_R5SS1_CORE1_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS1_CORE1_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 7
27:25	RESERVED	NONE	0h	Reserved
24	R5SS1_CORE1_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 6
23:21	RESERVED	NONE	0h	Reserved
20	R5SS1_CORE1_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 5
19:17	RESERVED	NONE	0h	Reserved

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Table 2-435. MSS_CTRL_R5SS1_CORE1_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	R5SS1_CORE1_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 4
15:13	RESERVED	NONE	0h	Reserved
12	R5SS1_CORE1_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 3
11:9	RESERVED	NONE	0h	Reserved
8	R5SS1_CORE1_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 2
7:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CORE1_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 1
3:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CORE1_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.2.131 MSS_CTRL_R5SS1_CORE1_MBOX_READ_REQ Register

2.3.2.131.1 MSS_CTRL_R5SS1_CORE1_MBOX_READ_REQ Register (Offset = 10004h) [reset = 0h]

Return to Summary Table

Table 2-436. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0004h

Figure 2-217. MSS_CTRL_R5SS1_CORE1_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS1_CORE1_MBOX_READ_REQ_PROC_7	RESERVED			R5SS1_CORE1_MBOX_READ_REQ_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R5SS1_CORE1_MBOX_READ_REQ_PROC_5	RESERVED			R5SS1_CORE1_MBOX_READ_REQ_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R5SS1_CORE1_MBOX_READ_REQ_PROC_3	RESERVED			R5SS1_CORE1_MBOX_READ_REQ_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS1_CORE1_MBOX_READ_REQ_PROC_1	RESERVED			R5SS1_CORE1_MBOX_READ_REQ_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-437. MSS_CTRL_R5SS1_CORE1_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS1_CORE1_MBOX_READ_REQ_PROC_7	R/W	0h	This is request from processor 7 to mss_CR5B. Requesting it to read from mailbox.
27:25	RESERVED	NONE	0h	Reserved
24	R5SS1_CORE1_MBOX_READ_REQ_PROC_6	R/W	0h	This is request from processor 6 to mss_CR5B. Requesting it to read from mailbox.
23:21	RESERVED	NONE	0h	Reserved
20	R5SS1_CORE1_MBOX_READ_REQ_PROC_5	R/W	0h	This is request from processor 5 to mss_CR5B. Requesting it to read from mailbox.
19:17	RESERVED	NONE	0h	Reserved
16	R5SS1_CORE1_MBOX_READ_REQ_PROC_4	R/W	0h	This is request from processor 4 to mss_CR5B. Requesting it to read from mailbox.
15:13	RESERVED	NONE	0h	Reserved

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Table 2-437. MSS_CTRL_R5SS1_CORE1_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	R5SS1_CORE1_MBOX_READ_REQ_PROC_3	R/W	0h	This is request from processor 3 to mss_CR5B. Requesting it to read from mailbox.
11:9	RESERVED	NONE	0h	Reserved
8	R5SS1_CORE1_MBOX_READ_REQ_PROC_2	R/W	0h	This is request from processor 2 to mss_CR5B. Requesting it to read from mailbox.
7:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CORE1_MBOX_READ_REQ_PROC_1	R/W	0h	This is request from processor 1 to mss_CR5B. Requesting it to read from mailbox.
3:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CORE1_MBOX_READ_REQ_PROC_0	R/W	0h	This is request from processor 0 to mss_CR5B. Requesting it to read from mailbox.

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2.3.2.132 MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE_ACK Register

2.3.2.132.1 MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE_ACK Register (Offset = 10008h) [reset = 0h]

Return to Summary Table

Table 2-438. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0008h

Figure 2-218. MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
R5SS1_CORE1_MBOX_READ_DONE_ACK_PROC							
R/W							
0h							

Table 2-439. MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	R5SS1_CORE1_MBOX_ READ_DONE_ACK_PRO C	R/W	0h	Write pulse bit field: For bits 0 to 7:Wrting 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5

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2.3.2.133 MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE Register

2.3.2.133.1 MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE Register (Offset = 1000Ch) [reset = 0h]

Return to Summary Table

Table 2-440. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 000Ch

Figure 2-219. MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			R5SS1_CORE1_MBOX_READ_DONE_PROC_7	RESERVED			R5SS1_CORE1_MBOX_READ_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			R5SS1_CORE1_MBOX_READ_DONE_PROC_5	RESERVED			R5SS1_CORE1_MBOX_READ_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			R5SS1_CORE1_MBOX_READ_DONE_PROC_3	RESERVED			R5SS1_CORE1_MBOX_READ_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS1_CORE1_MBOX_READ_DONE_PROC_1	RESERVED			R5SS1_CORE1_MBOX_READ_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-441. MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	R5SS1_CORE1_MBOX_READ_DONE_PROC_7	R/W	0h	This register should be written once finishing Reading from proc7's mailbox written by CR5B
27:25	RESERVED	NONE	0h	Reserved
24	R5SS1_CORE1_MBOX_READ_DONE_PROC_6	R/W	0h	This register should be written once finishing Reading from proc6's mailbox written by CR5B
23:21	RESERVED	NONE	0h	Reserved
20	R5SS1_CORE1_MBOX_READ_DONE_PROC_5	R/W	0h	This register should be written once finishing Reading from proc5's mailbox written by CR5B
19:17	RESERVED	NONE	0h	Reserved
16	R5SS1_CORE1_MBOX_READ_DONE_PROC_4	R/W	0h	This register should be written once finishing Reading from proc4's mailbox written by CR5B
15:13	RESERVED	NONE	0h	Reserved

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Table 2-441. MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	R5SS1_CORE1_MBOX_READ_DONE_PROC_3	R/W	0h	This register should be written once finishing Reading from proc3's mailbox written by CR5B
11:9	RESERVED	NONE	0h	Reserved
8	R5SS1_CORE1_MBOX_READ_DONE_PROC_2	R/W	0h	This register should be written once finishing Reading from proc2's mailbox written by CR5B
7:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CORE1_MBOX_READ_DONE_PROC_1	R/W	0h	This register should be written once finishing Reading from proc1's mailbox written by CR5B
3:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CORE1_MBOX_READ_DONE_PROC_0	R/W	0h	This register should be written once finishing Reading from proc0's mailbox written by CR5B

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2.3.2.134 MSS_CTRL_R5SS1_CORE1_SW_INT Register

2.3.2.134.1 MSS_CTRL_R5SS1_CORE1_SW_INT Register (Offset = 10010h) [reset = 0h]

Return to Summary Table

Table 2-442. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0010h

Figure 2-220. MSS_CTRL_R5SS1_CORE1_SW_INT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							R5SS1_CORE1_SW_INT_PULSE
NONE							R/W
0h							0h

Table 2-443. MSS_CTRL_R5SS1_CORE1_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	R5SS1_CORE1_SW_INT_PULSE	R/W	0h	Write_pulse bit field: Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B.

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2.3.2.135 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_MASK Register

2.3.2.135.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_MASK Register (Offset = 10020h) [reset = 0h]

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Table 2-444. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0020h

Figure 2-221. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_F_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_E_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_R5SS1_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_R5SS0_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_OPTI_FLASH_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_HSM_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B1_AHB_ADDR_ERR3
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A1_AHB_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B0_AHB_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A0_AHB_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_SCRM2SCRP1_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_SCRM2SCRP0_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_OSPI_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_MBOX_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_DTHE_A_ADDR_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B1_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A1_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B0_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A0_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_D_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_C_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_B_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_A_ADDR_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-445. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_F_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
21	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_E_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-445. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_R5SS1_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
19	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_R5SS0_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
18	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_OPTI_FLASH_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
17	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_HSM_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
16	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B1_AHB_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
15	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A1_AHB_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
14	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B0_AHB_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
13	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A0_AHB_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
12	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_SCRM2SCRP1_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
11	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_SCRM2SCRP0_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
10	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_OSPI_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
9	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_MBOX_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
8	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_DTHE_A_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
7	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B1_AXIS_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
6	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A1_AXIS_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-445. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B0_AXIS_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
4	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A0_AXIS_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
3	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_D_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
2	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_C_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
1	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_B_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
0	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_A_ADDR_ERR3	R/W	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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2.3.2.136 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS Register

2.3.2.136.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS Register (Offset = 10024h) [reset = 0h]

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Table 2-446. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0024h

Figure 2-222. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_F_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_E_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_R5SS1_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_R5SS0_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_OPTI_FLASH_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_HSM_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B1_AHB_ADDR_ERR3
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A1_AHB_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B0_AHB_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A0_AHB_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_SCRM2SCRP1_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_SCRM2SCRP0_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_OSPI_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_MBOX_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_DTHE_A_ADDR_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B1_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A1_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B0_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A0_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_D_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_C_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_B_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_A_ADDR_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-447. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_F_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
21	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_E_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-447. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_R5SS1_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
19	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_R5SS0_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
18	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_OPTI_FLASH_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
17	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_HSM_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
16	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B1_AHB_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
15	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A1_AHB_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
14	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B0_AHB_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
13	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A0_AHB_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
12	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_SCRM2SCRP1_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
11	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_SCRM2SCRP0_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
10	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_OSPI_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
9	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_MBOX_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
8	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_DTHE_A_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
7	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B1_AXIS_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
6	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A1_AXIS_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-447. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B0_AXIS_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
4	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A0_AXIS_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_D_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
2	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_C_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
1	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_B_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
0	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_A_ADDR_ERR3	R/W	0h	Status of Error from MPU_ADDR_INTR. Set only if Interupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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2.3.2.137 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS_RAW Register

2.3.2.137.1 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS_RAW Register (Offset = 10028h) [reset = 0h]

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Table 2-448. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0028h

Figure 2-223. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_F_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_E_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_R5SS1_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_R5SS0_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_OPTI_FLASH_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_HSM_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR3
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_OSPI_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_MBOX_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_DTHE_A_ADDR_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-449. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_F_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
21	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_E_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-449. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_R5SS1_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
19	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_R5SS0_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
18	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_OPTI_FLASH_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
17	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_HSM_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
16	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
15	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
14	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
13	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
12	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_SCRM2SCRP1_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
11	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_SCRM2SCRP0_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
10	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_OSPI_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
9	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_MBOX_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
8	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_DTHE_A_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
7	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
6	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-449. MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CORE1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
4	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
3	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
2	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
1	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
0	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR3	R/W	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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2.3.2.138 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_MASK Register

2.3.2.138.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_MASK Register (Offset = 10030h) [reset = 0h]

Return to Summary Table

Table 2-450. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0030h

Figure 2-224. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_F_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_E_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_R5SS1_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_R5SS0_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_OPTI_FLASH_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_HSM_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B1_AHB_PROT_ERR3
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A1_AHB_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B0_AHB_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A0_AHB_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_SCRM2SCRP1_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_SCRM2SCRP0_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_OSPI_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_MBOX_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_DTHE_A_PROT_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B1_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A1_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B0_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A0_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_D_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_C_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_B_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_A_PROT_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-451. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_F_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
21	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_E_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-451. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_R5SS1_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
19	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_R5SS0_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
18	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_OPTI_FLASH_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
17	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_HSM_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
16	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B1_AHB_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
15	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A1_AHB_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
14	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B0_AHB_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
13	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A0_AHB_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
12	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_SCRM2SCRP1_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
11	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_SCRM2SCRP0_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
10	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_OSPI_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
9	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_MBOX_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
8	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_DTHE_A_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
7	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B1_AXIS_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
6	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A1_AXIS_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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Table 2-451. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5B0_AXIS_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
4	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_CR5A0_AXIS_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
3	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_D_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
2	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_C_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
1	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_B_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
0	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK_MPU_L2_BANK_A_PROT_ERR3	R/W	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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2.3.2.139 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS Register

2.3.2.139.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS Register (Offset = 10034h) [reset = 0h]

Return to Summary Table

Table 2-452. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0034h

Figure 2-225. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_F_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_E_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_R5SS1_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_R5SS0_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_OPTI_FLASH_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_HSM_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B1_AHB_PROT_ERR3
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A1_AHB_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B0_AHB_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A0_AHB_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_SCRM2SCRP1_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_SCRM2SCRP0_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_OSPI_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_MBOX_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_DTHE_A_PROT_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B1_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A1_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B0_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A0_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_D_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_C_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_B_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_A_PROT_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-453. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_F_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
21	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_E_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-453. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_R5SS1_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
19	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_R5SS0_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
18	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_OPTI_FLASH_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
17	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_HSM_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
16	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B1_AHB_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
15	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A1_AHB_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
14	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B0_AHB_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
13	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A0_AHB_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
12	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_SCRM2SCRP1_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
11	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_SCRM2SCRP0_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
10	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_OSPI_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
9	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_MBOX_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
8	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_DTHE_A_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
7	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B1_AXIS_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
6	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A1_AXIS_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-453. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5B0_AXIS_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
4	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_CR5A0_AXIS_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_D_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
2	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_C_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
1	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_B_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.
0	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_MPU_L2_BANK_A_PROT_ERR3	R/W	0h	Status of Error from MPU_PROT_INTR. Set only if Interupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK Wrie 0x1 to clear this Error.

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2.3.2.140 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS_RAW Register

2.3.2.140.1 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS_RAW Register (Offset = 10038h) [reset = 0h]

Return to Summary Table

Table 2-454. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0038h

Figure 2-226. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_F_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_E_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_R5SS1_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_R5SS0_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_OPTI_FLASH_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_HSM_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR3
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A1_AHB_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B0_AHB_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A0_AHB_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_OSPI_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_MBOX_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_DTHE_A_PROT_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B1_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A1_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B0_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A0_AXIS_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-455. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_F_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
21	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_E_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-455. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_R5SS1_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
19	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_R5SS0_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
18	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_OPTI_FLASH_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
17	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_HSM_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
16	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
15	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A1_AHB_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
14	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B0_AHB_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
13	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A0_AHB_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
12	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_SCRM2SCRP1_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
11	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_SCRM2SCRP0_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
10	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_OSPI_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
9	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_MBOX_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
8	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_DTHE_A_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
7	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B1_AXIS_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
6	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A1_AXIS_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-455. MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CORE1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5B0_AXIS_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
4	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_CR5A0_AXIS_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
3	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
2	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
1	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
0	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR3	R/W	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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2.3.2.141 MSS_CTRL_PRU_ICSS_PRU0_MBOX_WRITE_DONE Register

2.3.2.141.1 MSS_CTRL_PRU_ICSS_PRU0_MBOX_WRITE_DONE Register (Offset = 14000h) [reset = 0h]

Return to Summary Table

Table 2-456. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4000h

Figure 2-227. MSS_CTRL_PRU_ICSS_PRU0_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_7	RESERVED			PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_5	RESERVED			PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_3	RESERVED			PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_1	RESERVED			PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-457. MSS_CTRL_PRU_ICSS_PRU0_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 7
27:25	RESERVED	NONE	0h	Reserved
24	PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 6
23:21	RESERVED	NONE	0h	Reserved
20	PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 5
19:17	RESERVED	NONE	0h	Reserved

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Table 2-457. MSS_CTRL_PRU_ICSS_PRU0_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 4
15:13	RESERVED	NONE	0h	Reserved
12	PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 3
11:9	RESERVED	NONE	0h	Reserved
8	PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 2
7:5	RESERVED	NONE	0h	Reserved
4	PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 1
3:1	RESERVED	NONE	0h	Reserved
0	PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.2.142 MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_REQ Register

2.3.2.142.1 MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_REQ Register (Offset = 14004h) [reset = 0h]

Return to Summary Table

Table 2-458. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4004h

Figure 2-228. MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED			PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_7	RESERVED			PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_5	RESERVED			PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_3	RESERVED			PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_1	RESERVED			PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-459. MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_7	R/W	0h	This is request from processor 7 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
27:25	RESERVED	NONE	0h	Reserved
24	PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_6	R/W	0h	This is request from processor 6 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
23:21	RESERVED	NONE	0h	Reserved
20	PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_5	R/W	0h	This is request from processor 5 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
19:17	RESERVED	NONE	0h	Reserved
16	PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_4	R/W	0h	This is request from processor 4 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
15:13	RESERVED	NONE	0h	Reserved

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Table 2-459. MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_3	R/W	0h	This is request from processor 3 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
11:9	RESERVED	NONE	0h	Reserved
8	PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_2	R/W	0h	This is request from processor 2 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
7:5	RESERVED	NONE	0h	Reserved
4	PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_1	R/W	0h	This is request from processor 1 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
3:1	RESERVED	NONE	0h	Reserved
0	PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_0	R/W	0h	This is request from processor 0 to corresponding ICSSM_PRU. Requesting it to read from mailbox.

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2.3.2.143 MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE_ACK Register

2.3.2.143.1 MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE_ACK Register (Offset = 14008h) [reset = 0h]

Return to Summary Table

Table 2-460. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4008h

Figure 2-229. MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRU_ICSS_PRU0_MBOX_READ_DONE_ACK_PROC							
R/W							
0h							

Table 2-461. MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRU_ICSS_PRU0_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7:Wrting 1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU0. For bits 8 to 15:Wrting 1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU1.

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2.3.2.144 MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE Register

2.3.2.144.1 MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE Register (Offset = 1400Ch) [reset = 0h]

Return to Summary Table

Table 2-462. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 400Ch

Figure 2-230. MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_7	RESERVED			PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	22	21	20	19	18	17	16
RESERVED			PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_5	RESERVED			PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	14	13	12	11	10	9	8
RESERVED			PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_3	RESERVED			PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED			PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_1	RESERVED			PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-463. MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_7	R/W	0h	This register should be written once finishing Reading from corresponding proc7's mailbox written by ICSSM_PRU
27:25	RESERVED	NONE	0h	Reserved
24	PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_6	R/W	0h	This register should be written once finishing Reading from corresponding proc6's mailbox written by ICSSM_PRU
23:21	RESERVED	NONE	0h	Reserved
20	PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_5	R/W	0h	This register should be written once finishing Reading from corresponding proc5's mailbox written by ICSSM_PRU
19:17	RESERVED	NONE	0h	Reserved
16	PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_4	R/W	0h	This register should be written once finishing Reading from corresponding proc4's mailbox written by ICSSM_PRU
15:13	RESERVED	NONE	0h	Reserved

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Table 2-463. MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_3	R/W	0h	This register should be written once finishing Reading from corresponding proc3's mailbox written by ICSSM_PRU
11:9	RESERVED	NONE	0h	Reserved
8	PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_2	R/W	0h	This register should be written once finishing Reading from corresponding proc2's mailbox written by ICSSM_PRU
7:5	RESERVED	NONE	0h	Reserved
4	PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_1	R/W	0h	This register should be written once finishing Reading from corresponding proc1's mailbox written by ICSSM_PRU
3:1	RESERVED	NONE	0h	Reserved
0	PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_0	R/W	0h	This register should be written once finishing Reading from corresponding proc0's mailbox written by ICSSM_PRU

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2.3.2.145 MSS_CTRL_PRU_ICSS_PRU1_MBOX_WRITE_DONE Register

2.3.2.145.1 MSS_CTRL_PRU_ICSS_PRU1_MBOX_WRITE_DONE Register (Offset = 14010h) [reset = 0h]

Return to Summary Table

Table 2-464. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4010h

Figure 2-231. MSS_CTRL_PRU_ICSS_PRU1_MBOX_WRITE_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_7	RESERVED			PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	22	21	20	19	18	17	16
RESERVED			PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_5	RESERVED			PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	14	13	12	11	10	9	8
RESERVED			PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_3	RESERVED			PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED			PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_1	RESERVED			PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-465. MSS_CTRL_PRU_ICSS_PRU1_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_7	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 7
27:25	RESERVED	NONE	0h	Reserved
24	PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_6	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 6
23:21	RESERVED	NONE	0h	Reserved
20	PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_5	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 5
19:17	RESERVED	NONE	0h	Reserved

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Table 2-465. MSS_CTRL_PRU_ICSS_PRU1_MBOX_WRITE_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_4	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 4
15:13	RESERVED	NONE	0h	Reserved
12	PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_3	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 3
11:9	RESERVED	NONE	0h	Reserved
8	PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_2	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 2
7:5	RESERVED	NONE	0h	Reserved
4	PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_1	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 1
3:1	RESERVED	NONE	0h	Reserved
0	PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_0	R/W	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.2.146 MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_REQ Register

2.3.2.146.1 MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_REQ Register (Offset = 14014h) [reset = 0h]

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Table 2-466. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4014h

Figure 2-232. MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED			PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_7	RESERVED			PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_5	RESERVED			PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_3	RESERVED			PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_1	RESERVED			PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-467. MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_7	R/W	0h	This is request from processor 7 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
27:25	RESERVED	NONE	0h	Reserved
24	PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_6	R/W	0h	This is request from processor 6 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
23:21	RESERVED	NONE	0h	Reserved
20	PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_5	R/W	0h	This is request from processor 5 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
19:17	RESERVED	NONE	0h	Reserved
16	PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_4	R/W	0h	This is request from processor 4 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
15:13	RESERVED	NONE	0h	Reserved

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Table 2-467. MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_REQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_3	R/W	0h	This is request from processor 3 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
11:9	RESERVED	NONE	0h	Reserved
8	PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_2	R/W	0h	This is request from processor 2 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
7:5	RESERVED	NONE	0h	Reserved
4	PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_1	R/W	0h	This is request from processor 1 to corresponding ICSSM_PRU. Requesting it to read from mailbox.
3:1	RESERVED	NONE	0h	Reserved
0	PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_0	R/W	0h	This is request from processor 0 to corresponding ICSSM_PRU. Requesting it to read from mailbox.

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2.3.2.147 MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE_ACK Register

2.3.2.147.1 MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE_ACK Register (Offset = 14018h) [reset = 0h]

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Table 2-468. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4018h

Figure 2-233. MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE_ACK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PRU_ICSS_PRU1_MBOX_READ_DONE_ACK_PROC							
R/W							
0h							

Table 2-469. MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PRU_ICSS_PRU1_MBOX_READ_DONE_ACK_PROC	R/W	0h	Write pulse bit field: For bits 0 to 7:Wrting 1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU0. For bits 8 to 15:Wrting 1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU1.

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2.3.2.148 MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE Register

2.3.2.148.1 MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE Register (Offset = 1401Ch) [reset = 0h]

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Table 2-470. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 401Ch

Figure 2-234. MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE Name Register

31	30	29	28	27	26	25	24
RESERVED			PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_7	RESERVED			PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_6
NONE			R/W	NONE			R/W
0h			0h	0h			0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_5	RESERVED			PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_4
NONE			R/W	NONE			R/W
0h			0h	0h			0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_3	RESERVED			PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_2
NONE			R/W	NONE			R/W
0h			0h	0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_1	RESERVED			PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_0
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-471. MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_7	R/W	0h	This register should be written once finishing Reading from corresponding proc7's mailbox written by ICSSM_PRU
27:25	RESERVED	NONE	0h	Reserved
24	PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_6	R/W	0h	This register should be written once finishing Reading from corresponding proc6's mailbox written by ICSSM_PRU
23:21	RESERVED	NONE	0h	Reserved
20	PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_5	R/W	0h	This register should be written once finishing Reading from corresponding proc5's mailbox written by ICSSM_PRU
19:17	RESERVED	NONE	0h	Reserved
16	PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_4	R/W	0h	This register should be written once finishing Reading from corresponding proc4's mailbox written by ICSSM_PRU
15:13	RESERVED	NONE	0h	Reserved

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Table 2-471. MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_3	R/W	0h	This register should be written once finishing Reading from corresponding proc3's mailbox written by ICSSM_PRU
11:9	RESERVED	NONE	0h	Reserved
8	PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_2	R/W	0h	This register should be written once finishing Reading from corresponding proc2's mailbox written by ICSSM_PRU
7:5	RESERVED	NONE	0h	Reserved
4	PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_1	R/W	0h	This register should be written once finishing Reading from corresponding proc1's mailbox written by ICSSM_PRU
3:1	RESERVED	NONE	0h	Reserved
0	PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_0	R/W	0h	This register should be written once finishing Reading from corresponding proc0's mailbox written by ICSSM_PRU

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2.3.2.149 MSS_CTRL_TPCC0_ERRAGG_MASK Register

2.3.2.149.1 MSS_CTRL_TPCC0_ERRAGG_MASK Register (Offset = 18000h) [reset = 0h]

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Table 2-472. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8000h

Figure 2-235. MSS_CTRL_TPCC0_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED					TPCC0_ERRAGG_MASK_TPTC_A1_READ_ACCESS_ERROR	TPCC0_ERRAGG_MASK_TPTC_A0_READ_ACCESS_ERROR	TPCC0_ERRAGG_MASK_TPCC_A_READ_ACCESS_ERROR
NONE					R/W	R/W	R/W
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					TPCC0_ERRAGG_MASK_TPTC_A1_WRITE_ACCESS_ERROR	TPCC0_ERRAGG_MASK_TPTC_A0_WRITE_ACCESS_ERROR	TPCC0_ERRAGG_MASK_TPCC_A_WRITE_ACCESS_ERROR
NONE					R/W	R/W	R/W
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TPCC0_ERRAGG_MASK_TPCC_A_PAR_ERR	TPCC0_ERRAGG_MASK_TPTC_A1_ERR	TPCC0_ERRAGG_MASK_TPTC_A0_ERR	TPCC0_ERRAGG_MASK_TPCC_A_MPINT	TPCC0_ERRAGG_MASK_TPCC_A_ERRINT
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-473. MSS_CTRL_TPCC0_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	TPCC0_ERRAGG_MASK_TPTC_A1_READ_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
25	TPCC0_ERRAGG_MASK_TPTC_A0_READ_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
24	TPCC0_ERRAGG_MASK_TPCC_A_READ_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
23:19	RESERVED	NONE	0h	Reserved

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Table 2-473. MSS_CTRL_TPCC0_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	TPCC0_ERRAGG_MASK_TPTC_A1_WRITE_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
17	TPCC0_ERRAGG_MASK_TPTC_A0_WRITE_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
16	TPCC0_ERRAGG_MASK_TPCC_A_WRITE_ACCESS_ERROR	R/W	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
15:5	RESERVED	NONE	0h	Reserved
4	TPCC0_ERRAGG_MASK_TPCC_A_PAR_ERR	R/W	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
3	TPCC0_ERRAGG_MASK_TPTC_A1_ERR	R/W	0h	Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
2	TPCC0_ERRAGG_MASK_TPTC_A0_ERR	R/W	0h	Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
1	TPCC0_ERRAGG_MASK_TPCC_A_MPINT	R/W	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked
0	TPCC0_ERRAGG_MASK_TPCC_A_ERRINT	R/W	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG 1'b1 : Error is Masked 1'b0 : Error is Unmasked

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2.3.2.150 MSS_CTRL_TPCC0_ERRAGG_STATUS Register

2.3.2.150.1 MSS_CTRL_TPCC0_ERRAGG_STATUS Register (Offset = 18004h) [reset = 0h]

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Table 2-474. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8004h

Figure 2-236. MSS_CTRL_TPCC0_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED					TPCC0_ERRAGG_STATUS_TPTC_A1_READ_ACCESS_ERROR	TPCC0_ERRAGG_STATUS_TPTC_A0_READ_ACCESS_ERROR	TPCC0_ERRAGG_STATUS_TPCC_A_READ_ACCESS_ERROR
NONE					R/W	R/W	R/W
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					TPCC0_ERRAGG_STATUS_TPTC_A1_WRITE_ACCESS_ERROR	TPCC0_ERRAGG_STATUS_TPTC_A0_WRITE_ACCESS_ERROR	TPCC0_ERRAGG_STATUS_TPCC_A_WRITE_ACCESS_ERROR
NONE					R/W	R/W	R/W
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TPCC0_ERRAGG_STATUS_TPCC_A_PAR_ERR	TPCC0_ERRAGG_STATUS_TPTC_A1_ERR	TPCC0_ERRAGG_STATUS_TPTC_A0_ERR	TPCC0_ERRAGG_STATUS_TPCC_A_MPINT	TPCC0_ERRAGG_STATUS_TPCC_A_ERRINT
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-475. MSS_CTRL_TPCC0_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	TPCC0_ERRAGG_STATUS_TPTC_A1_READ_ACCESS_ERROR	R/W	0h	Status of Error from MSS_TPTC_A1. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.
25	TPCC0_ERRAGG_STATUS_TPTC_A0_READ_ACCESS_ERROR	R/W	0h	Status of Error from MSS_TPTC_A0. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.
24	TPCC0_ERRAGG_STATUS_TPCC_A_READ_ACCESS_ERROR	R/W	0h	Status of Error from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.
23:19	RESERVED	NONE	0h	Reserved
18	TPCC0_ERRAGG_STATUS_TPTC_A1_WRITE_ACCESS_ERROR	R/W	0h	Status of Error from MSS_TPTC_A1. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.

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Table 2-475. MSS_CTRL_TPCC0_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	TPCC0_ERRAGG_STATUS_TPTC_A0_WRITE_ACCESS_ERROR	R/W	0h	Status of Error from MSS_TPTC_A0. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.
16	TPCC0_ERRAGG_STATUS_TPCC_A_WRITE_ACCESS_ERROR	R/W	0h	Status of Error from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.
15:5	RESERVED	NONE	0h	Reserved
4	TPCC0_ERRAGG_STATUS_TPCC_A_PAR_ERR	R/W	0h	Status of Error from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.
3	TPCC0_ERRAGG_STATUS_TPTC_A1_ERR	R/W	0h	Status of Error from MSS_TPTC_A1. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.
2	TPCC0_ERRAGG_STATUS_TPTC_A0_ERR	R/W	0h	Status of Error from MSS_TPTC_A0. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.
1	TPCC0_ERRAGG_STATUS_TPCC_A_MPINT	R/W	0h	Status of Error from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.
0	TPCC0_ERRAGG_STATUS_TPCC_A_ERRINT	R/W	0h	Status of Error from MSS_TPCC_A. Set only if Interupt is unmasked in TPCC0_ERRAGG_MASK Wrie 0x1 to clear this Error.

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2.3.2.151 MSS_CTRL_TPCC0_ERRAGG_STATUS_RAW Register

2.3.2.151.1 MSS_CTRL_TPCC0_ERRAGG_STATUS_RAW Register (Offset = 18008h) [reset = 0h]

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Table 2-476. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8008h

Figure 2-237. MSS_CTRL_TPCC0_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED					TPCC0_ERRAGG_STATUS_RAW_TPTC_A1_READ_ACCESS_ERROR	TPCC0_ERRAGG_STATUS_RAW_TPTC_A0_READ_ACCESS_ERROR	TPCC0_ERRAGG_STATUS_RAW_TPCC_A_READ_ACCESS_ERROR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

23	22	21	20	19	18	17	16
RESERVED					TPCC0_ERRAGG_STATUS_RAW_TPTC_A1_WRITE_ACCESS_ERROR	TPCC0_ERRAGG_STATUS_RAW_TPTC_A0_WRITE_ACCESS_ERROR	TPCC0_ERRAGG_STATUS_RAW_TPCC_A_WRITE_ACCESS_ERROR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED			TPCC0_ERRAGG_STATUS_RAW_TPCC_A_PAR_ERR	TPCC0_ERRAGG_STATUS_RAW_TPTC_A1_ERR	TPCC0_ERRAGG_STATUS_RAW_TPTC_A0_ERR	TPCC0_ERRAGG_STATUS_RAW_TPCC_A_MPINT	TPCC0_ERRAGG_STATUS_RAW_TPCC_A_ERRINT
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-477. MSS_CTRL_TPCC0_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26	TPCC0_ERRAGG_STATUS_RAW_TPTC_A1_READ_ACCESS_ERROR	R/W	0h	Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK
25	TPCC0_ERRAGG_STATUS_RAW_TPTC_A0_READ_ACCESS_ERROR	R/W	0h	Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK
24	TPCC0_ERRAGG_STATUS_RAW_TPCC_A_READ_ACCESS_ERROR	R/W	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK
23:19	RESERVED	NONE	0h	Reserved
18	TPCC0_ERRAGG_STATUS_RAW_TPTC_A1_WRITE_ACCESS_ERROR	R/W	0h	Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK

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Table 2-477. MSS_CTRL_TPCC0_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	TPCC0_ERRAGG_STATUS_RAW_TPTC_A0_WRITE_ACCESS_ERROR	R/W	0h	Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK
16	TPCC0_ERRAGG_STATUS_RAW_TPCC_A_WRITE_ACCESS_ERROR	R/W	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK
15:5	RESERVED	NONE	0h	Reserved
4	TPCC0_ERRAGG_STATUS_RAW_TPCC_A_PAR_ERR	R/W	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK
3	TPCC0_ERRAGG_STATUS_RAW_TPTC_A1_ERR	R/W	0h	Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK
2	TPCC0_ERRAGG_STATUS_RAW_TPTC_A0_ERR	R/W	0h	Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK
1	TPCC0_ERRAGG_STATUS_RAW_TPCC_A_MPINT	R/W	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK
0	TPCC0_ERRAGG_STATUS_RAW_TPCC_A_ERRINT	R/W	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in TPCC0_ERRAGG_MASK

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2.3.2.152 MSS_CTRL_MMR_ACCESS_ERRAGG_MASK0 Register

2.3.2.152.1 MSS_CTRL_MMR_ACCESS_ERRAGG_MASK0 Register (Offset = 18010h) [reset = 0h]

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Table 2-478. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8010h

Figure 2-238. MSS_CTRL_MMR_ACCESS_ERRAGG_MASK0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MMR_ACCESS_ERRAGG_MASK0_HSM_CTRL_WR	MMR_ACCESS_ERRAGG_MASK0_HSM_CTRL_RD	MMR_ACCESS_ERRAGG_MASK0_HSM_SOC_CTRL_WR	MMR_ACCESS_ERRAGG_MASK0_HSM_SOC_CTRL_RD
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
MMR_ACCESS_ERRAGG_MASK0_TOP_RCM_WR	MMR_ACCESS_ERRAGG_MASK0_TOP_RCM_RD	MMR_ACCESS_ERRAGG_MASK0_TOP_CTRL_WR	MMR_ACCESS_ERRAGG_MASK0_TOP_CTRL_RD	MMR_ACCESS_ERRAGG_MASK0_MSS_RCM_WR	MMR_ACCESS_ERRAGG_MASK0_MSS_RCM_RD	MMR_ACCESS_ERRAGG_MASK0_MSS_CTRL_WR	MMR_ACCESS_ERRAGG_MASK0_MSS_CTRL_RD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-479. MSS_CTRL_MMR_ACCESS_ERRAGG_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	MMR_ACCESS_ERRAGG_MASK0_HSM_CTRL_WR	R/W	0h	Mask Interrupt from HSM_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
10	MMR_ACCESS_ERRAGG_MASK0_HSM_CTRL_RD	R/W	0h	Mask Interrupt from HSM_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
9	MMR_ACCESS_ERRAGG_MASK0_HSM_SOC_CTRL_WR	R/W	0h	Mask Interrupt from HSM_SOC_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
8	MMR_ACCESS_ERRAGG_MASK0_HSM_SOC_CTRL_RD	R/W	0h	Mask Interrupt from HSM_SOC_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
7	MMR_ACCESS_ERRAGG_MASK0_TOP_RCM_WR	R/W	0h	Mask Interrupt from TOP_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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Table 2-479. MSS_CTRL_MMR_ACCESS_ERRAGG_MASK0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	MMR_ACCESS_ERRAG G_MASK0_TOP_RCM_R D	R/W	0h	Mask Interrupt from TOP_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
5	MMR_ACCESS_ERRAG G_MASK0_TOP_CTRL_ WR	R/W	0h	Mask Interrupt from TOP_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
4	MMR_ACCESS_ERRAG G_MASK0_TOP_CTRL_R D	R/W	0h	Mask Interrupt from TOP_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
3	MMR_ACCESS_ERRAG G_MASK0_MSS_RCM_W R	R/W	0h	Mask Interrupt from MSS_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
2	MMR_ACCESS_ERRAG G_MASK0_MSS_RCM_R D	R/W	0h	Mask Interrupt from MSS_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
1	MMR_ACCESS_ERRAG G_MASK0_MSS_CTRL_ WR	R/W	0h	Mask Interrupt from MSS_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
0	MMR_ACCESS_ERRAG G_MASK0_MSS_CTRL_R D	R/W	0h	Mask Interrupt from MSS_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.153 MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS0 Register

2.3.2.153.1 MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS0 Register (Offset = 18014h) [reset = 0h]

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Table 2-480. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8014h

Figure 2-239. MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MMR_ACCESS_ERRAGG_STATUS0_HSM_CTRL_WR	MMR_ACCESS_ERRAGG_STATUS0_HSM_CTRL_RD	MMR_ACCESS_ERRAGG_STATUS0_HSM_SOC_CTRL_WR	MMR_ACCESS_ERRAGG_STATUS0_HSM_SOC_CTRL_RD
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_ACCESS_ERRAGG_STATUS0_TOP_RCM_WR	MMR_ACCESS_ERRAGG_STATUS0_TOP_RCM_RD	MMR_ACCESS_ERRAGG_STATUS0_TOP_CTRL_WR	MMR_ACCESS_ERRAGG_STATUS0_TOP_CTRL_RD	MMR_ACCESS_ERRAGG_STATUS0_MSS_RCM_WR	MMR_ACCESS_ERRAGG_STATUS0_MSS_RCM_RD	MMR_ACCESS_ERRAGG_STATUS0_MSS_CTRL_WR	MMR_ACCESS_ERRAGG_STATUS0_MSS_CTRL_RD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-481. MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	MMR_ACCESS_ERRAGG_STATUS0_HSM_CTRL_WR	R/W	0h	Status of Interrupt from HSM_CTRL Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.
10	MMR_ACCESS_ERRAGG_STATUS0_HSM_CTRL_RD	R/W	0h	Status of Interrupt from HSM_CTRL Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.
9	MMR_ACCESS_ERRAGG_STATUS0_HSM_SOC_CTRL_WR	R/W	0h	Status of Interrupt from HSM_SOC_CTRL Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.
8	MMR_ACCESS_ERRAGG_STATUS0_HSM_SOC_CTRL_RD	R/W	0h	Status of Interrupt from HSM_SOC_CTRL Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.
7	MMR_ACCESS_ERRAGG_STATUS0_TOP_RCM_WR	R/W	0h	Status of Interrupt from TOP_RCM Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.

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Table 2-481. MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	MMR_ACCESS_ERRAGG_STATUS0_TOP_RCM_RD	R/W	0h	Status of Interrupt from TOP_RCM Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.
5	MMR_ACCESS_ERRAGG_STATUS0_TOP_CTRL_WR	R/W	0h	Status of Interrupt from TOP_CTRL Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.
4	MMR_ACCESS_ERRAGG_STATUS0_TOP_CTRL_RD	R/W	0h	Status of Interrupt from TOP_CTRL Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.
3	MMR_ACCESS_ERRAGG_STATUS0_MSS_RCM_WR	R/W	0h	Status of Interrupt from MSS_RCM Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.
2	MMR_ACCESS_ERRAGG_STATUS0_MSS_RCM_RD	R/W	0h	Status of Interrupt from MSS_RCM Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.
1	MMR_ACCESS_ERRAGG_STATUS0_MSS_CTRL_WR	R/W	0h	Status of Interrupt from MSS_CTRL Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.
0	MMR_ACCESS_ERRAGG_STATUS0_MSS_CTRL_RD	R/W	0h	Status of Interrupt from MSS_CTRL Set only if Interupt is unmasked in MMR_ACCESS_ERRAGG_MASK0 Wrie 0x1 to clear this interrupt.

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2.3.2.154 MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS_RAW0 Register

2.3.2.154.1 MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS_RAW0 Register (Offset = 18018h) [reset = 0h]

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Table 2-482. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8018h

Figure 2-240. MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS_RAW0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MMR_ACCESS_ERRAGG_STATUS_RAW0_HSM_CTRL_WR	MMR_ACCESS_ERRAGG_STATUS_RAW0_HSM_CTRL_RD	MMR_ACCESS_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_WR	MMR_ACCESS_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_RD
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MMR_ACCESS_ERRAGG_STATUS_RAW0_TOP_RCM_WR	MMR_ACCESS_ERRAGG_STATUS_RAW0_TOP_RCM_RD	MMR_ACCESS_ERRAGG_STATUS_RAW0_TOP_CTRL_WR	MMR_ACCESS_ERRAGG_STATUS_RAW0_TOP_CTRL_RD	MMR_ACCESS_ERRAGG_STATUS_RAW0_MSS_RCM_WR	MMR_ACCESS_ERRAGG_STATUS_RAW0_MSS_RCM_RD	MMR_ACCESS_ERRAGG_STATUS_RAW0_MSS_CTRL_WR	MMR_ACCESS_ERRAGG_STATUS_RAW0_MSS_CTRL_RD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-483. MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS_RAW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11	MMR_ACCESS_ERRAGG_STATUS_RAW0_HSM_CTRL_WR	R/W	0h	Raw Status of Interrupt from HSM_CTRL. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0
10	MMR_ACCESS_ERRAGG_STATUS_RAW0_HSM_CTRL_RD	R/W	0h	Raw Status of Interrupt from HSM_CTRL. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0
9	MMR_ACCESS_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_WR	R/W	0h	Raw Status of Interrupt from HSM_SOC_CTRL. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0
8	MMR_ACCESS_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_RD	R/W	0h	Raw Status of Interrupt from HSM_SOC_CTRL. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0
7	MMR_ACCESS_ERRAGG_STATUS_RAW0_TOP_RCM_WR	R/W	0h	Raw Status of Interrupt from TOP_RCM. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0
6	MMR_ACCESS_ERRAGG_STATUS_RAW0_TOP_RCM_RD	R/W	0h	Raw Status of Interrupt from TOP_RCM. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0

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Table 2-483. MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS_RAW0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MMR_ACCESS_ERRAGG_STATUS_RAW0_TOP_CTRL_WR	R/W	0h	Raw Status of Interrupt from TOP_CTRL. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0
4	MMR_ACCESS_ERRAGG_STATUS_RAW0_TOP_CTRL_RD	R/W	0h	Raw Status of Interrupt from TOP_CTRL. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0
3	MMR_ACCESS_ERRAGG_STATUS_RAW0_MSS_RCM_WR	R/W	0h	Raw Status of Interrupt from MSS_RCM. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0
2	MMR_ACCESS_ERRAGG_STATUS_RAW0_MSS_RCM_RD	R/W	0h	Raw Status of Interrupt from MSS_RCM. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0
1	MMR_ACCESS_ERRAGG_STATUS_RAW0_MSS_CTRL_WR	R/W	0h	Raw Status of Interrupt from MSS_CTRL. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0
0	MMR_ACCESS_ERRAGG_STATUS_RAW0_MSS_CTRL_RD	R/W	0h	Raw Status of Interrupt from MSS_CTRL. Set irrespective if the Interupt is masked or unmasked in MMR_ACCESS_ERRAGG_MASK0

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2.3.2.155 MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_MASK Register

2.3.2.155.1 MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_MASK Register (Offset = 18080h) [reset = 0h]

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Table 2-484. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8080h

Figure 2-241. MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_IDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ITAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-485. MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_IDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
5	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ITAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
4	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
3	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
2	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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Table 2-485. MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
0	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.156 MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS Register

2.3.2.156.1 MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS Register (Offset = 18084h) [reset = 0h]

Return to Summary Table

Table 2-486. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8084h

Figure 2-242. MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_IDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ITAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-487. MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_IDATA_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
5	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ITAG_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
4	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-487. MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.157 MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS_RAW Register

2.3.2.157.1 MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 18088h) [reset = 0h]

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Table 2-488. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8088h

Figure 2-243. MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_IDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ITAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DDATA_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DTAG_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM_CORR_ERR	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-489. MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_IDATA_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
5	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ITAG_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
4	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DDATA_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DTAG_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-489. MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.158 MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_MASK Register

2.3.2.158.1 MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_MASK Register (Offset = 18090h) [reset = 0h]

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Table 2-490. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8090h

Figure 2-244. MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-491. MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
3	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
2	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
1	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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Table 2-491. MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.159 MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS Register

2.3.2.159.1 MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 18094h) [reset = 0h]

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Table 2-492. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8094h

Figure 2-245. MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-493. MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-493. MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.160 MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW Register

2.3.2.160.1 MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 18098h) [reset = 0h]

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Table 2-494. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8098h

Figure 2-246. MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DDATA_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DTAG_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM_UNCORR_ERR	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-495. MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DDATA_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DTAG_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-495. MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.161 MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_MASK Register

2.3.2.161.1 MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_MASK Register (Offset = 180A0h) [reset = 0h]

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Table 2-496. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80A0h

Figure 2-247. MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_IDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ITAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-497. MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_IDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
5	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ITAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
4	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
3	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
2	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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Table 2-497. MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
0	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.162 MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS Register

2.3.2.162.1 MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS Register (Offset = 180A4h) [reset = 0h]

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Table 2-498. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80A4h

Figure 2-248. MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_IDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ITAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-499. MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_IDATA_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
5	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ITAG_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
4	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-499. MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.163 MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS_RAW Register

2.3.2.163.1 MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 180A8h) [reset = 0h]

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Table 2-500. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80A8h

Figure 2-249. MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_IDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ITAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DDATA_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DTAG_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM_CORR_ERR	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-501. MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_IDATA_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
5	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ITAG_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
4	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DDATA_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DTAG_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-501. MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.164 MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_MASK Register

2.3.2.164.1 MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_MASK Register (Offset = 180B0h) [reset = 0h]

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Table 2-502. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80B0h

Figure 2-250. MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-503. MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
3	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
2	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
1	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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Table 2-503. MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.165 MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS Register

2.3.2.165.1 MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 180B4h) [reset = 0h]

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Table 2-504. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80B4h

Figure 2-251. MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-505. MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-505. MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.166 MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW Register

2.3.2.166.1 MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 180B8h) [reset = 0h]

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Table 2-506. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80B8h

Figure 2-252. MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DDATA_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DTAG_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM_UNCORR_ERR	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-507. MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DDATA_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DTAG_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-507. MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.167 MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_MASK Register

2.3.2.167.1 MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_MASK Register (Offset = 180C0h) [reset = 0h]

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Table 2-508. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80C0h

Figure 2-253. MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_IDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ITAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-509. MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_IDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
5	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ITAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
4	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
3	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
2	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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Table 2-509. MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
0	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.168 MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS Register

2.3.2.168.1 MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS Register (Offset = 180C4h) [reset = 0h]

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Table 2-510. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80C4h

Figure 2-254. MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_IDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ITAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-511. MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_IDATA_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
5	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ITAG_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
4	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-511. MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.169 MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS_RAW Register

2.3.2.169.1 MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 180C8h) [reset = 0h]

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Table 2-512. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80C8h

Figure 2-255. MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_IDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ITAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DTAG_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM_CORR_ERR	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-513. MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_IDATA_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
5	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ITAG_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
4	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DTAG_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-513. MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.170 MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_MASK Register

2.3.2.170.1 MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_MASK Register (Offset = 180D0h) [reset = 0h]

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Table 2-514. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80D0h

Figure 2-256. MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-515. MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
3	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
2	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
1	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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Table 2-515. MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.171 MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS Register

2.3.2.171.1 MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 180D4h) [reset = 0h]

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Table 2-516. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80D4h

Figure 2-257. MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-517. MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-517. MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.172 MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW Register

2.3.2.172.1 MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 180D8h) [reset = 0h]

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Table 2-518. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80D8h

Figure 2-258. MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED			R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DTAG_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM_UNCORR_ERR	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-519. MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DTAG_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-519. MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.173 MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_MASK Register

2.3.2.173.1 MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_MASK Register (Offset = 180E0h) [reset = 0h]

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Table 2-520. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80E0h

Figure 2-259. MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_IDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ITAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-521. MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_IDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
5	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ITAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
4	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
3	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
2	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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Table 2-521. MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
0	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_CORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.174 MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS Register

2.3.2.174.1 MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS Register (Offset = 180E4h) [reset = 0h]

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Table 2-522. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80E4h

Figure 2-260. MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_IDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ITAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-523. MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_IDATA_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
5	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ITAG_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
4	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-523. MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_CORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.175 MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS_RAW Register

2.3.2.175.1 MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 180E8h) [reset = 0h]

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Table 2-524. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80E8h

Figure 2-261. MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_IDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ITAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DTAG_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM_CORR_ERR	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM_CORR_ERR
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 2-525. MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_IDATA_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
5	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ITAG_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
4	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DTAG_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-525. MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM_CORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.176 MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_MASK Register

2.3.2.176.1 MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_MASK Register (Offset = 180F0h) [reset = 0h]

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Table 2-526. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80F0h

Figure 2-262. MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-527. MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
3	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
2	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
1	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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Table 2-527. MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_UNCORR_ERR	R/W	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.177 MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS Register

2.3.2.177.1 MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 180F4h) [reset = 0h]

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Table 2-528. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80F4h

Figure 2-263. MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-529. MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-529. MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_UNCORR_ERR	R/W	0h	Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.178 MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW Register

2.3.2.178.1 MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 180F8h) [reset = 0h]

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Table 2-530. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80F8h

Figure 2-264. MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DTAG_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM_UNCORR_ERR	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM_UNCORR_ERR
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 2-531. MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
3	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DTAG_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
2	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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Table 2-531. MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM_UNCORR_ERR	R/W	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.179 MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_MASK Register

2.3.2.179.1 MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18100h) [reset = 0h]

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Table 2-532. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8100h

Figure 2-265. MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B1TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B0TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_ATCM0_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-533. MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B1TCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
1	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B0TCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
0	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_ATCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.180 MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS Register

2.3.2.180.1 MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18104h) [reset = 0h]

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Table 2-534. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8104h

Figure 2-266. MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED					R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B1TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B0TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_ATCM0_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-535. MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B1TCM0_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B0TCM0_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_ATCM0_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.181 MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register

2.3.2.181.1 MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18108h) [reset = 0h]

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Table 2-536. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8108h

Figure 2-267. MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM0_PARITY_ERR	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM0_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-537. MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM0_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM0_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM0_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.182 MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_MASK Register

2.3.2.182.1 MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18110h) [reset = 0h]

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Table 2-538. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8110h

Figure 2-268. MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM1_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM0_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_ATCM1_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-539. MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM1_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
1	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
0	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_ATCM1_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.183 MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS Register

2.3.2.183.1 MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18114h) [reset = 0h]

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Table 2-540. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8114h

Figure 2-269. MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_B1TCM1_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_B0TCM1_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_ATCM1_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-541. MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_B1TCM1_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_B0TCM1_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_ATCM1_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.184 MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register

2.3.2.184.1 MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18118h) [reset = 0h]

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Table 2-542. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8118h

Figure 2-270. MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM1_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM1_PARITY_ERR	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM1_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-543. MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM1_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM1_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM1_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.185 MSS_CTRL_R5SS0_TCM_ADDRPARITY_CLR Register

2.3.2.185.1 MSS_CTRL_R5SS0_TCM_ADDRPARITY_CLR Register (Offset = 18120h) [reset = 0h]

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Table 2-544. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8120h

Figure 2-271. MSS_CTRL_R5SS0_TCM_ADDRPARITY_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	R5SS0_TCM_ADDRPARITY_CLR_B1TCM1_ERRADDR_CLR			RESERVED	R5SS0_TCM_ADDRPARITY_CLR_B1TCM0_ERRADDR_CLR		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	R5SS0_TCM_ADDRPARITY_CLR_B0CM1_ERRADDR_CLR			RESERVED	R5SS0_TCM_ADDRPARITY_CLR_B0TCM0_ERRADDR_CLR		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	R5SS0_TCM_ADDRPARITY_CLR_ATCM1_ERRADDR_CLR			RESERVED	R5SS0_TCM_ADDRPARITY_CLR_ATCM0_ERRADDR_CLR		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 2-545. MSS_CTRL_R5SS0_TCM_ADDRPARITY_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:20	R5SS0_TCM_ADDRPARITY_CLR_B1TCM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5B
19	RESERVED	NONE	0h	Reserved
18:16	R5SS0_TCM_ADDRPARITY_CLR_B1TCM0_ERRADDR_CLR	R/W	0h	Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5A
15	RESERVED	NONE	0h	Reserved
14:12	R5SS0_TCM_ADDRPARITY_CLR_B0CM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5B
11	RESERVED	NONE	0h	Reserved
10:8	R5SS0_TCM_ADDRPARITY_CLR_B0TCM0_ERRADDR_CLR	R/W	0h	Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5A
7	RESERVED	NONE	0h	Reserved
6:4	R5SS0_TCM_ADDRPARITY_CLR_ATCM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for ATCM of CR5B
3	RESERVED	NONE	0h	Reserved

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Table 2-545. MSS_CTRL_R5SS0_TCM_ADDRPARITY_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	R5SS0_TCM_ADDRPARITY_CLR_ATCM0_ERRADDR_CLR	R/W	0h	Pulse bit-field Writing 3'b111 clears the Address latched after parity error for ATCM of CR5A

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2.3.2.186 MSS_CTRL_R5SS0_CORE0_ADDRPARITY_ERR_ATCM Register

2.3.2.186.1 MSS_CTRL_R5SS0_CORE0_ADDRPARITY_ERR_ATCM Register (Offset = 18124h) [reset = 0h]

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Table 2-546. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8124h

Figure 2-272. MSS_CTRL_R5SS0_CORE0_ADDRPARITY_ERR_ATCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R5SS0_CORE0_ADDRPARITY_ERR_ATCM_ADDR			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
R5SS0_CORE0_ADDRPARITY_ERR_ATCM_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
R5SS0_CORE0_ADDRPARITY_ERR_ATCM_ADDR							
R							
0h							

Table 2-547. MSS_CTRL_R5SS0_CORE0_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS0_CORE0_ADDRPARITY_ERR_ATCM_ADDR	R	0h	Address lathched when parity error is occurred for ATCM of CR5A

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2.3.2.187 MSS_CTRL_R5SS0_CORE1_ADDRPARITY_ERR_ATCM Register

2.3.2.187.1 MSS_CTRL_R5SS0_CORE1_ADDRPARITY_ERR_ATCM Register (Offset = 18128h) [reset = 0h]

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Table 2-548. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8128h

Figure 2-273. MSS_CTRL_R5SS0_CORE1_ADDRPARITY_ERR_ATCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				R5SS0_CORE1_ADDRPARITY_ERR_ATCM_ADDR			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R5SS0_CORE1_ADDRPARITY_ERR_ATCM_ADDR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS0_CORE1_ADDRPARITY_ERR_ATCM_ADDR							
R							
0h							

Table 2-549. MSS_CTRL_R5SS0_CORE1_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS0_CORE1_ADDRPARITY_ERR_ATCM_ADDR	R	0h	Address lathched when parity error is occurred for ATCM of CR5B

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2.3.2.188 MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B0TCM Register

2.3.2.188.1 MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B0TCM Register (Offset = 1812Ch) [reset = 0h]

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Table 2-550. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 812Ch

Figure 2-274. MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B0TCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R5SS0_CORE0_ERR_ADDRPARITY_B0TCM_ADDR			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
R5SS0_CORE0_ERR_ADDRPARITY_B0TCM_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
R5SS0_CORE0_ERR_ADDRPARITY_B0TCM_ADDR							
R							
0h							

Table 2-551. MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS0_CORE0_ERR_ADDRPARITY_B0TCM_ADDR	R	0h	Address lathched when parity error is occurred for B0TCM of CR5A

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2.3.2.189 MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B0TCM Register

2.3.2.189.1 MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B0TCM Register (Offset = 18130h) [reset = 0h]

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Table 2-552. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8130h

Figure 2-275. MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B0TCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				R5SS0_CORE1_ERR_ADDRPARITY_B0TCM_ADDR			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R5SS0_CORE1_ERR_ADDRPARITY_B0TCM_ADDR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS0_CORE1_ERR_ADDRPARITY_B0TCM_ADDR							
R							
0h							

Table 2-553. MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS0_CORE1_ERR_ADDRPARITY_B0TCM_ADDR	R	0h	Address lathched when parity error is occurred for B0TCM of CR5B

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2.3.2.190 MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B1TCM Register

2.3.2.190.1 MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B1TCM Register (Offset = 18134h) [reset = 0h]

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Table 2-554. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8134h

Figure 2-276. MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B1TCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R5SS0_CORE0_ERR_ADDRPARITY_B1TCM_ADDR			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
R5SS0_CORE0_ERR_ADDRPARITY_B1TCM_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
R5SS0_CORE0_ERR_ADDRPARITY_B1TCM_ADDR							
R							
0h							

Table 2-555. MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS0_CORE0_ERR_ADDRPARITY_B1TCM_ADDR	R	0h	Address lathched when parity error is occurred for B1TCM of CR5A

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2.3.2.191 MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B1TCM Register

2.3.2.191.1 MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B1TCM Register (Offset = 18138h) [reset = 0h]

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Table 2-556. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8138h

Figure 2-277. MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B1TCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R5SS0_CORE1_ERR_ADDRPARITY_B1TCM_ADDR			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
R5SS0_CORE1_ERR_ADDRPARITY_B1TCM_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
R5SS0_CORE1_ERR_ADDRPARITY_B1TCM_ADDR							
R							
0h							

Table 2-557. MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS0_CORE1_ERR_ADDRPARITY_B1TCM_ADDR	R	0h	Address lathched when parity error is occurred for B1TCM of CR5B

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2.3.2.192 MSS_CTRL_R5SS0_TCM_ADDRPARITY_ERRFORCE Register

2.3.2.192.1 MSS_CTRL_R5SS0_TCM_ADDRPARITY_ERRFORCE Register (Offset = 1813Ch) [reset = 0h]

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Table 2-558. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 813Ch

Figure 2-278. MSS_CTRL_R5SS0_TCM_ADDRPARITY_ERRFORCE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	R5SS0_TCM_ADDRPARITY_ERRFORCE_B1TCM1			RESERVED	R5SS0_TCM_ADDRPARITY_ERRFORCE_B1TCM0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	R5SS0_TCM_ADDRPARITY_ERRFORCE_B0TCM1			RESERVED	R5SS0_TCM_ADDRPARITY_ERRFORCE_B0TCM0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	R5SS0_TCM_ADDRPARITY_ERRFORCE_ATCM1			RESERVED	R5SS0_TCM_ADDRPARITY_ERRFORCE_ATCM0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 2-559. MSS_CTRL_R5SS0_TCM_ADDRPARITY_ERRFORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:20	R5SS0_TCM_ADDRPARITY_ERRFORCE_B1TCM1	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for B1TCM of CR5B
19	RESERVED	NONE	0h	Reserved
18:16	R5SS0_TCM_ADDRPARITY_ERRFORCE_B1TCM0	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for B1TCM of CR5A
15	RESERVED	NONE	0h	Reserved
14:12	R5SS0_TCM_ADDRPARITY_ERRFORCE_B0TCM1	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for B0TCM of CR5B
11	RESERVED	NONE	0h	Reserved
10:8	R5SS0_TCM_ADDRPARITY_ERRFORCE_B0TCM0	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for B0TCM of CR5A
7	RESERVED	NONE	0h	Reserved
6:4	R5SS0_TCM_ADDRPARITY_ERRFORCE_ATCM1	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for ATCM of CR5B
3	RESERVED	NONE	0h	Reserved

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Table 2-559. MSS_CTRL_R5SS0_TCM_ADDRPARITY_ERRFORCE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	R5SS0_TCM_ADDRPARITY_ERRFORCE_ATCM0	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for ATCM of CR5A

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2.3.2.193 MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_MASK Register

2.3.2.193.1 MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18140h) [reset = 0h]

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Table 2-560. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8140h

Figure 2-279. MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B1TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B0TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_ATCM0_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-561. MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B1TCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
1	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B0TCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
0	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_ATCM0_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.194 MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS Register

2.3.2.194.1 MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18144h) [reset = 0h]

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Table 2-562. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8144h

Figure 2-280. MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_B1TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_B0TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_ATCM0_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-563. MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_B1TCM0_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_B0TCM0_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_ATCM0_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.195 MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register

2.3.2.195.1 MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18148h) [reset = 0h]

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Table 2-564. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8148h

Figure 2-281. MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM0_PARITY_ERR	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM0_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-565. MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM0_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM0_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM0_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.196 MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_MASK Register

2.3.2.196.1 MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18150h) [reset = 0h]

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Table 2-566. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8150h

Figure 2-282. MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED					R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B1TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B0TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_ATCM1_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-567. MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B1TCM1_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
1	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B0TCM1_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked
0	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_ATCM1_PARITY_ERR	R/W	0h	Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU 1'b1 : Interrupt is Masked 1'b0 : Interrupt is Unmasked

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2.3.2.197 MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS Register

2.3.2.197.1 MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18154h) [reset = 0h]

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Table 2-568. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8154h

Figure 2-283. MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_B1TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_B0TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_ATCM1_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-569. MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_B1TCM1_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_B0TCM1_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_ATCM1_PARITY_ERR	R/W	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.198 MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register

2.3.2.198.1 MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18158h) [reset = 0h]

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Table 2-570. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8158h

Figure 2-284. MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM1_PARITY_ERR	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM1_PARITY_ERR
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-571. MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM1_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
1	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM1_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.
0	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM1_PARITY_ERR	R/W	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register Wrie 0x1 to clear this interrupt.

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2.3.2.199 MSS_CTRL_R5SS1_TCM_ADDRPARITY_CLR Register

2.3.2.199.1 MSS_CTRL_R5SS1_TCM_ADDRPARITY_CLR Register (Offset = 18160h) [reset = 0h]

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Table 2-572. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8160h

Figure 2-285. MSS_CTRL_R5SS1_TCM_ADDRPARITY_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	R5SS1_TCM_ADDRPARITY_CLR_B1TCM1_ERRADDR_CLR			RESERVED	R5SS1_TCM_ADDRPARITY_CLR_B1TCM0_ERRADDR_CLR		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	R5SS1_TCM_ADDRPARITY_CLR_B0CM1_ERRADDR_CLR			RESERVED	R5SS1_TCM_ADDRPARITY_CLR_B0TCM0_ERRADDR_CLR		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	R5SS1_TCM_ADDRPARITY_CLR_ATCM1_ERRADDR_CLR			RESERVED	R5SS1_TCM_ADDRPARITY_CLR_ATCM0_ERRADDR_CLR		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 2-573. MSS_CTRL_R5SS1_TCM_ADDRPARITY_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:20	R5SS1_TCM_ADDRPARITY_CLR_B1TCM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5B
19	RESERVED	NONE	0h	Reserved
18:16	R5SS1_TCM_ADDRPARITY_CLR_B1TCM0_ERRADDR_CLR	R/W	0h	Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5A
15	RESERVED	NONE	0h	Reserved
14:12	R5SS1_TCM_ADDRPARITY_CLR_B0CM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5B
11	RESERVED	NONE	0h	Reserved
10:8	R5SS1_TCM_ADDRPARITY_CLR_B0TCM0_ERRADDR_CLR	R/W	0h	Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5A
7	RESERVED	NONE	0h	Reserved
6:4	R5SS1_TCM_ADDRPARITY_CLR_ATCM1_ERRADDR_CLR	R/W	0h	Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for ATCM of CR5B
3	RESERVED	NONE	0h	Reserved

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Table 2-573. MSS_CTRL_R5SS1_TCM_ADDRPARITY_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	R5SS1_TCM_ADDRPARITY_CLR_ATCM0_ERRADDR_CLR	R/W	0h	Pulse bit-field Writing 3'b111 clears the Address latched after parity error for ATCM of CR5A

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2.3.2.200 MSS_CTRL_R5SS1_CORE0_ADDRPARITY_ERR_ATCM Register

2.3.2.200.1 MSS_CTRL_R5SS1_CORE0_ADDRPARITY_ERR_ATCM Register (Offset = 18164h) [reset = 0h]

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Table 2-574. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8164h

Figure 2-286. MSS_CTRL_R5SS1_CORE0_ADDRPARITY_ERR_ATCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R5SS1_CORE0_ADDRPARITY_ERR_ATCM_ADDR			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
R5SS1_CORE0_ADDRPARITY_ERR_ATCM_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
R5SS1_CORE0_ADDRPARITY_ERR_ATCM_ADDR							
R							
0h							

Table 2-575. MSS_CTRL_R5SS1_CORE0_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS1_CORE0_ADDRPARITY_ERR_ATCM_ADDR	R	0h	Address lathched when parity error is occurred for ATCM of CR5A

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2.3.2.201 MSS_CTRL_R5SS1_CORE1_ADDRPARITY_ERR_ATCM Register

2.3.2.201.1 MSS_CTRL_R5SS1_CORE1_ADDRPARITY_ERR_ATCM Register (Offset = 18168h) [reset = 0h]

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Table 2-576. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8168h

Figure 2-287. MSS_CTRL_R5SS1_CORE1_ADDRPARITY_ERR_ATCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R5SS1_CORE1_ADDRPARITY_ERR_ATCM_ADDR			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
R5SS1_CORE1_ADDRPARITY_ERR_ATCM_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
R5SS1_CORE1_ADDRPARITY_ERR_ATCM_ADDR							
R							
0h							

Table 2-577. MSS_CTRL_R5SS1_CORE1_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS1_CORE1_ADDRPARITY_ERR_ATCM_ADDR	R	0h	Address lathched when parity error is occurred for ATCM of CR5B

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2.3.2.202 MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B0TCM Register

2.3.2.202.1 MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B0TCM Register (Offset = 1816Ch) [reset = 0h]

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Table 2-578. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 816Ch

Figure 2-288. MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B0TCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				R5SS1_CORE0_ERR_ADDRPARITY_B0TCM_ADDR			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R5SS1_CORE0_ERR_ADDRPARITY_B0TCM_ADDR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS1_CORE0_ERR_ADDRPARITY_B0TCM_ADDR							
R							
0h							

Table 2-579. MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS1_CORE0_ERR_ADDRPARITY_B0TCM_ADDR	R	0h	Address lathched when parity error is occurred for B0TCM of CR5A

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2.3.2.203 MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B0TCM Register

2.3.2.203.1 MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B0TCM Register (Offset = 18170h) [reset = 0h]

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Table 2-580. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8170h

Figure 2-289. MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B0TCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				R5SS1_CORE1_ERR_ADDRPARITY_B0TCM_ADDR			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R5SS1_CORE1_ERR_ADDRPARITY_B0TCM_ADDR							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS1_CORE1_ERR_ADDRPARITY_B0TCM_ADDR							
R							
0h							

Table 2-581. MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS1_CORE1_ERR_ADDRPARITY_B0TCM_ADDR	R	0h	Address lathched when parity error is occurred for B0TCM of CR5B

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2.3.2.204 MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B1TCM Register

2.3.2.204.1 MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B1TCM Register (Offset = 18174h) [reset = 0h]

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Table 2-582. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8174h

Figure 2-290. MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B1TCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R5SS1_CORE0_ERR_ADDRPARITY_B1TCM_ADDR			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
R5SS1_CORE0_ERR_ADDRPARITY_B1TCM_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
R5SS1_CORE0_ERR_ADDRPARITY_B1TCM_ADDR							
R							
0h							

Table 2-583. MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS1_CORE0_ERR_ADDRPARITY_B1TCM_ADDR	R	0h	Address lathched when parity error is occurred for B1TCM of CR5A

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2.3.2.205 MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B1TCM Register

2.3.2.205.1 MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B1TCM Register (Offset = 18178h) [reset = 0h]

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Table 2-584. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8178h

Figure 2-291. MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B1TCM Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R5SS1_CORE1_ERR_ADDRPARITY_B1TCM_ADDR			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
R5SS1_CORE1_ERR_ADDRPARITY_B1TCM_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
R5SS1_CORE1_ERR_ADDRPARITY_B1TCM_ADDR							
R							
0h							

Table 2-585. MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R5SS1_CORE1_ERR_ADDRPARITY_B1TCM_ADDR	R	0h	Address lathched when parity error is occurred for B1TCM of CR5B

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2.3.2.206 MSS_CTRL_R5SS1_TCM_ADDRPARITY_ERRFORCE Register

2.3.2.206.1 MSS_CTRL_R5SS1_TCM_ADDRPARITY_ERRFORCE Register (Offset = 1817Ch) [reset = 0h]

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Table 2-586. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 817Ch

Figure 2-292. MSS_CTRL_R5SS1_TCM_ADDRPARITY_ERRFORCE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	R5SS1_TCM_ADDRPARITY_ERRFORCE_B1TCM1			RESERVED	R5SS1_TCM_ADDRPARITY_ERRFORCE_B1TCM0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RESERVED	R5SS1_TCM_ADDRPARITY_ERRFORCE_B0TCM1			RESERVED	R5SS1_TCM_ADDRPARITY_ERRFORCE_B0TCM0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RESERVED	R5SS1_TCM_ADDRPARITY_ERRFORCE_ATCM1			RESERVED	R5SS1_TCM_ADDRPARITY_ERRFORCE_ATCM0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 2-587. MSS_CTRL_R5SS1_TCM_ADDRPARITY_ERRFORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:20	R5SS1_TCM_ADDRPARITY_ERRFORCE_B1TCM1	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for B1TCM of CR5B
19	RESERVED	NONE	0h	Reserved
18:16	R5SS1_TCM_ADDRPARITY_ERRFORCE_B1TCM0	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for B1TCM of CR5A
15	RESERVED	NONE	0h	Reserved
14:12	R5SS1_TCM_ADDRPARITY_ERRFORCE_B0TCM1	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for B0TCM of CR5B
11	RESERVED	NONE	0h	Reserved
10:8	R5SS1_TCM_ADDRPARITY_ERRFORCE_B0TCM0	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for B0TCM of CR5A
7	RESERVED	NONE	0h	Reserved
6:4	R5SS1_TCM_ADDRPARITY_ERRFORCE_ATCM1	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for ATCM of CR5B
3	RESERVED	NONE	0h	Reserved

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Table 2-587. MSS_CTRL_R5SS1_TCM_ADDRPARITY_ERRFORCE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	R5SS1_TCM_ADDRPARITY_ERRFORCE_ATCM0	R/W	0h	Write pulse bit field: Writing 3'b111 forces a parity error for ATCM of CR5A

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2.3.2.207 MSS_CTRL_TPCC0_PARITY_CTRL Register

2.3.2.207.1 MSS_CTRL_TPCC0_PARITY_CTRL Register (Offset = 18180h) [reset = 0h]

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Table 2-588. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8180h

Figure 2-293. MSS_CTRL_TPCC0_PARITY_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							TPCC0_PARITY_CTRL_TPCC_A_PARITY_ERR_CLR
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TPCC0_PARITY_CTRL_TPCC_A_PARITY_TESTEN	RESERVED			TPCC0_PARITY_CTRL_TPCC_A_PARITY_EN
NONE			R/W	NONE			R/W
0h			0h	0h			0h

Table 2-589. MSS_CTRL_TPCC0_PARITY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	TPCC0_PARITY_CTRL_TPCC_A_PARITY_ERR_CLR	R/W	0h	Write pulse bit field: parity clear bit. Writing 1'b1 will clear the tpcc_a_parity_addr
15:5	RESERVED	NONE	0h	Reserved
4	TPCC0_PARITY_CTRL_TPCC_A_PARITY_TESTEN	R/W	0h	parity test enable for tpcc a
3:1	RESERVED	NONE	0h	Reserved
0	TPCC0_PARITY_CTRL_TPCC_A_PARITY_EN	R/W	0h	Writing 1'b1 enables parity for TPCC_A

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2.3.2.208 MSS_CTRL_TPCC0_PARITY_STATUS Register

2.3.2.208.1 MSS_CTRL_TPCC0_PARITY_STATUS Register (Offset = 18184h) [reset = 0h]

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Table 2-590. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8184h

Figure 2-294. MSS_CTRL_TPCC0_PARITY_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							TPCC0_PARITY_STATUS_TPCC_A_PARITY_ADDR
NONE							R
0h							0h

7	6	5	4	3	2	1	0
TPCC0_PARITY_STATUS_TPCC_A_PARITY_ADDR							
R							
0h							

Table 2-591. MSS_CTRL_TPCC0_PARITY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:0	TPCC0_PARITY_STATUS_TPCC_A_PARITY_ADDR	R	0h	Address where parity error happened for tpcca

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2.3.2.209 MSS_CTRL_TMU_R5SS0_CORE0_ROM_PARITY_CTRL Register

2.3.2.209.1 MSS_CTRL_TMU_R5SS0_CORE0_ROM_PARITY_CTRL Register (Offset = 18188h) [reset = 0h]

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Table 2-592. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8188h

Figure 2-295. MSS_CTRL_TMU_R5SS0_CORE0_ROM_PARITY_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							TMU_R5SS0_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_ERR_CLR
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED						TMU_R5SS0_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_FORCE_ERR	TMU_R5SS0_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_EN
NONE						R/W	R/W
0h						0h	0h

Table 2-593. MSS_CTRL_TMU_R5SS0_CORE0_ROM_PARITY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	TMU_R5SS0_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_ERR_CLR	R/W	0h	Write pulse bit field: parity clear bit. Writing 1'b1 will clear the tmu0_rom_parity_err_addr
15:2	RESERVED	NONE	0h	Reserved
1	TMU_R5SS0_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_FORCE_ERR	R/W	0h	Force parity error on the read interface
0	TMU_R5SS0_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_EN	R/W	0h	Writing 1'b1 enables parity for TMU0

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2.3.2.210 MSS_CTRL_TMU_R5SS0_CORE0_ROM_PARITY_STATUS Register

2.3.2.210.1 MSS_CTRL_TMU_R5SS0_CORE0_ROM_PARITY_STATUS Register (Offset = 1818Ch) [reset = 0h]

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Table 2-594. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 818Ch

Figure 2-296. MSS_CTRL_TMU_R5SS0_CORE0_ROM_PARITY_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					TMU_R5SS0_CORE0_ROM_PARITY_STATUS_TMU0_ROM_PARITY_ERR_ADDR		
NONE					R		
0h					0h		
7	6	5	4	3	2	1	0
TMU_R5SS0_CORE0_ROM_PARITY_STATUS_TMU0_ROM_PARITY_ERR_ADDR							
R							
0h							

Table 2-595. MSS_CTRL_TMU_R5SS0_CORE0_ROM_PARITY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	TMU_R5SS0_CORE0_ROM_PARITY_STATUS_TMU0_ROM_PARITY_ERR_ADDR	R	0h	Address where parity error happened for tmu0

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2.3.2.211 MSS_CTRL_TMU_R5SS0_CORE1_ROM_PARITY_CTRL Register

2.3.2.211.1 MSS_CTRL_TMU_R5SS0_CORE1_ROM_PARITY_CTRL Register (Offset = 18190h) [reset = 0h]

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Table 2-596. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8190h

Figure 2-297. MSS_CTRL_TMU_R5SS0_CORE1_ROM_PARITY_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							TMU_R5SS0_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_ERR_CLR
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TMU_R5SS0_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_FORCE_ERR	TMU_R5SS0_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_EN
NONE						R/W	R/W
0h						0h	0h

Table 2-597. MSS_CTRL_TMU_R5SS0_CORE1_ROM_PARITY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	TMU_R5SS0_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_ERR_CLR	R/W	0h	Write pulse bit field: parity clear bit. Writing 1'b1 will clear the tmu1_rom_parity_err_addr
15:2	RESERVED	NONE	0h	Reserved
1	TMU_R5SS0_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_FORCE_ERR	R/W	0h	Force parity error on the read interface
0	TMU_R5SS0_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_EN	R/W	0h	Writing 1'b1 enables parity for TMU1

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2.3.2.212 MSS_CTRL_TMU_R5SS0_CORE1_ROM_PARITY_STATUS Register

2.3.2.212.1 MSS_CTRL_TMU_R5SS0_CORE1_ROM_PARITY_STATUS Register (Offset = 18194h) [reset = 0h]

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Table 2-598. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8194h

Figure 2-298. MSS_CTRL_TMU_R5SS0_CORE1_ROM_PARITY_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					TMU_R5SS0_CORE1_ROM_PARITY_STATUS_TMU1_ROM_PARITY_ERR_ADDR		
NONE					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TMU_R5SS0_CORE1_ROM_PARITY_STATUS_TMU1_ROM_PARITY_ERR_ADDR							
R							
0h							

Table 2-599. MSS_CTRL_TMU_R5SS0_CORE1_ROM_PARITY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	TMU_R5SS0_CORE1_ROM_PARITY_STATUS_TMU1_ROM_PARITY_ERR_ADDR	R	0h	Address where parity error happened for tmu1

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2.3.2.213 MSS_CTRL_TMU_R5SS1_CORE0_ROM_PARITY_CTRL Register

2.3.2.213.1 MSS_CTRL_TMU_R5SS1_CORE0_ROM_PARITY_CTRL Register (Offset = 18198h) [reset = 0h]

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Table 2-600. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8198h

Figure 2-299. MSS_CTRL_TMU_R5SS1_CORE0_ROM_PARITY_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							TMU_R5SS1_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_ERR_CLR
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TMU_R5SS1_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_FORCE_ERR	TMU_R5SS1_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_EN
NONE						R/W	R/W
0h						0h	0h

Table 2-601. MSS_CTRL_TMU_R5SS1_CORE0_ROM_PARITY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	TMU_R5SS1_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_ERR_CLR	R/W	0h	Write pulse bit field: parity clear bit. Writing 1'b1 will clear the tmu0_rom_parity_err_addr
15:2	RESERVED	NONE	0h	Reserved
1	TMU_R5SS1_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_FORCE_ERR	R/W	0h	Force parity error on the read interface
0	TMU_R5SS1_CORE0_ROM_PARITY_CTRL_TMU0_ROM_PARITY_EN	R/W	0h	Writing 1'b1 enables parity for TMU0

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2.3.2.214 MSS_CTRL_TMU_R5SS1_CORE0_ROM_PARITY_STATUS Register

2.3.2.214.1 MSS_CTRL_TMU_R5SS1_CORE0_ROM_PARITY_STATUS Register (Offset = 1819Ch) [reset = 0h]

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Table 2-602. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 819Ch

Figure 2-300. MSS_CTRL_TMU_R5SS1_CORE0_ROM_PARITY_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					TMU_R5SS1_CORE0_ROM_PARITY_STATUS_TMU0_ROM_PARITY_ERR_ADDR		
NONE					R		
0h					0h		
7	6	5	4	3	2	1	0
TMU_R5SS1_CORE0_ROM_PARITY_STATUS_TMU0_ROM_PARITY_ERR_ADDR							
R							
0h							

Table 2-603. MSS_CTRL_TMU_R5SS1_CORE0_ROM_PARITY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	TMU_R5SS1_CORE0_ROM_PARITY_STATUS_TMU0_ROM_PARITY_ERR_ADDR	R	0h	Address where parity error happened for tmu0

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2.3.2.215 MSS_CTRL_TMU_R5SS1_CORE1_ROM_PARITY_CTRL Register

2.3.2.215.1 MSS_CTRL_TMU_R5SS1_CORE1_ROM_PARITY_CTRL Register (Offset = 181A0h) [reset = 0h]

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Table 2-604. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 81A0h

Figure 2-301. MSS_CTRL_TMU_R5SS1_CORE1_ROM_PARITY_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							TMU_R5SS1_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_ERR_CLR
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TMU_R5SS1_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_FORCE_ERR	TMU_R5SS1_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_EN
NONE						R/W	R/W
0h						0h	0h

Table 2-605. MSS_CTRL_TMU_R5SS1_CORE1_ROM_PARITY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	TMU_R5SS1_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_ERR_CLR	R/W	0h	Write pulse bit field: parity clear bit. Writing 1'b1 will clear the tmu1_rom_parity_err_addr
15:2	RESERVED	NONE	0h	Reserved
1	TMU_R5SS1_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_FORCE_ERR	R/W	0h	Force parity error on the read interface
0	TMU_R5SS1_CORE1_ROM_PARITY_CTRL_TMU1_ROM_PARITY_EN	R/W	0h	Writing 1'b1 enables parity for TMU1

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2.3.2.216 MSS_CTRL_TMU_R5SS1_CORE1_ROM_PARITY_STATUS Register

2.3.2.216.1 MSS_CTRL_TMU_R5SS1_CORE1_ROM_PARITY_STATUS Register (Offset = 181A4h) [reset = 0h]

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Table 2-606. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 81A4h

Figure 2-302. MSS_CTRL_TMU_R5SS1_CORE1_ROM_PARITY_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					TMU_R5SS1_CORE1_ROM_PARITY_STATUS_TMU1_ROM_PARITY_ERR_ADDR		
NONE					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TMU_R5SS1_CORE1_ROM_PARITY_STATUS_TMU1_ROM_PARITY_ERR_ADDR							
R							
0h							

Table 2-607. MSS_CTRL_TMU_R5SS1_CORE1_ROM_PARITY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	TMU_R5SS1_CORE1_ROM_PARITY_STATUS_TMU1_ROM_PARITY_ERR_ADDR	R	0h	Address where parity error happened for tmu1

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2.3.2.217 MSS_CTRL_OSPI0_BUS_SAFETY_CTRL Register

2.3.2.217.1 MSS_CTRL_OSPI0_BUS_SAFETY_CTRL Register (Offset = 184A0h) [reset = 7h]

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Table 2-608. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 84A0h

Figure 2-303. MSS_CTRL_OSPI0_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OSPI0_BUS_SAFETY_CTRL_TYPE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							OSPI0_BUS_SAFETY_CTRL_ERR_CLEAR
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					OSPI0_BUS_SAFETY_CTRL_ENABLE		
NONE					R/W		
0h					7h		

Table 2-609. MSS_CTRL_OSPI0_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	OSPI0_BUS_SAFETY_CTRL_TYPE	R	0h	This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not. Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0. Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0. Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0. Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0. Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1. Bits 5-7 are set to 3'b000.
15:9	RESERVED	NONE	0h	Reserved
8	OSPI0_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Set this bit to 1'b1 to clear the error status for this port
7:3	RESERVED	NONE	0h	Reserved
2:0	OSPI0_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Set this bit to 3'b111 to enable the safety configuration for this port. Set this bit to 3'b000 to disable the safety configuration for this port.

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2.3.2.218 MSS_CTRL_OSPI0_BUS_SAFETY_FI Register

2.3.2.218.1 MSS_CTRL_OSPI0_BUS_SAFETY_FI Register (Offset = 184A4h) [reset = 0h]

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Table 2-610. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 84A4h

Figure 2-304. MSS_CTRL_OSPI0_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24
OSPI0_BUS_SAFETY_FI_SAFE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OSPI0_BUS_SAFETY_FI_MAIN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OSPI0_BUS_SAFETY_FI_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		OSPI0_BUS_SAFETY_FI_DED	OSPI0_BUS_SAFETY_FI_SEC	OSPI0_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	OSPI0_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	OSPI0_BUS_SAFETY_FI_GLOBAL_SAFE	OSPI0_BUS_SAFETY_FI_GLOBAL_MAIN
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 2-611. MSS_CTRL_OSPI0_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	OSPI0_BUS_SAFETY_FI_SAFE	R/W	0h	This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect. Bit 0 - Set this bit to inject fault on the Command bus. Bit 1 - Set this bit to inject fault on theWrite bus. Bit 2 - Set this bit to inject fault on the Write Status bus. Bit 3 - Set this bit to inject fault on the Read bus. Bit 7- Set this bit to inject fault on the corresponding request bus.
23:16	OSPI0_BUS_SAFETY_FI_MAIN	R/W	0h	This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect. Bit 0 - Set this bit to inject fault on the Command bus. Bit 1 - Set this bit to inject fault on theWrite bus. Bit 2 - Set this bit to inject fault on the Write Status bus. Bit 3 - Set this bit to inject fault on the Read bus. Bit 7- Set this bit to inject fault on the corresponding request bus.
15:8	OSPI0_BUS_SAFETY_FI_DATA	R/W	0h	Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus. Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.
7:6	RESERVED	NONE	0h	Reserved
5	OSPI0_BUS_SAFETY_FI_DED	R/W	0h	Set this bit to 1'b1 inject ded error on data at this port
4	OSPI0_BUS_SAFETY_FI_SEC	R/W	0h	Set this bit to 1'b1 to inject sec error on data at this port
3	OSPI0_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Set this bit 1'b1 to inject fault for request signals on Safe Interconnect.

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Table 2-611. MSS_CTRL_OSPI0_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OSPI0_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Set this bit to 1'b1 to inject fault for request signals on main Interconnect.
1	OSPI0_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.
0	OSPI0_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.

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2.3.2.219 MSS_CTRL_OSPI0_BUS_SAFETY_ERR Register

2.3.2.219.1 MSS_CTRL_OSPI0_BUS_SAFETY_ERR Register (Offset = 184A8h) [reset = 0h]

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Table 2-612. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 84A8h

Figure 2-305. MSS_CTRL_OSPI0_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24
OSPI0_BUS_SAFETY_ERR_DED							
R							
0h							
23	22	21	20	19	18	17	16
OSPI0_BUS_SAFETY_ERR_SEC							
R							
0h							
15	14	13	12	11	10	9	8
OSPI0_BUS_SAFETY_ERR_COMP_CHECK							
R							
0h							
7	6	5	4	3	2	1	0
OSPI0_BUS_SAFETY_ERR_COMP_ERR							
R							
0h							

Table 2-613. MSS_CTRL_OSPI0_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	OSPI0_BUS_SAFETY_ERR_DED	R	0h	This flag signals detection of dual error in Data at this port.Flag is generted for 32 bit segment of Data Bus Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus Bit [7:2] - Unused. Set to 1'b0
23:16	OSPI0_BUS_SAFETY_ERR_SEC	R	0h	This flag signals detection of single error in Data at this port. Flag is generted for 32 bit segment of Data Bus Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus Bit [7:2] - Unused. Set to 1'b0
15:8	OSPI0_BUS_SAFETY_ERR_COMP_CHECK	R	0h	This is used to verify the proper functioning of fault Injection on all the buses.1'b1 indicates error in the corresponding Bus has been injected successfully. Bit 0 - This is a Bitwise AND of error compares of all command bus signals. Bit 1 - This is a Bitwise AND of error compares of all write bus signals. Bit 2 - This is a Bitwise AND of error compares of all write status bus signals. Bit 3 - This is a Bitwise AND of error compares of all read bus signals. Bits [7:4] are unused.

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Table 2-613. MSS_CTRL_OSPI0_BUS_SAFETY_ERR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	OSPI0_BUS_SAFETY_ERR_COMP_ERR	R	0h	1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal Bit 0 - This is a Bitwise OR of error compares of all command bus signals. Bit 1 - This is a Bitwise OR of error compares of all write bus signals. Bit 2 - This is a Bitwise OR of error compares of all write status bus signals. Bit 3 - This is a Bitwise OR of error compares of all read bus signals. Bits [7:4] are unused.

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2.3.2.220 MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_DATA0 Register

2.3.2.220.1 MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 184ACh) [reset = 0h]

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Table 2-614. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 84ACh

Figure 2-306. MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OSPI0_BUS_SAFETY_ERR_STAT_DATA0_D1							
R							
0h							
7	6	5	4	3	2	1	0
OSPI0_BUS_SAFETY_ERR_STAT_DATA0_D0							
R							
0h							

Table 2-615. MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	OSPI0_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC.
7:0	OSPI0_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.

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2.3.2.221 MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_CMD Register

2.3.2.221.1 MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 184B0h) [reset = 0h]

Return to Summary Table

Table 2-616. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 84B0h

Figure 2-307. MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24
OSPI0_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							
23	22	21	20	19	18	17	16
OSPI0_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							
15	14	13	12	11	10	9	8
OSPI0_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							
7	6	5	4	3	2	1	0
OSPI0_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							

Table 2-617. MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OSPI0_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus

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2.3.2.222 MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_WRITE Register

2.3.2.222.1 MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 184B4h) [reset = 0h]

Return to Summary Table

Table 2-618. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 84B4h

Figure 2-308. MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24
OSPI0_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							
23	22	21	20	19	18	17	16
OSPI0_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							
15	14	13	12	11	10	9	8
OSPI0_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							
7	6	5	4	3	2	1	0
OSPI0_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							

Table 2-619. MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OSPI0_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus

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2.3.2.223 MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_READ Register

2.3.2.223.1 MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_READ Register (Offset = 184B8h) [reset = 0h]

Return to Summary Table

Table 2-620. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 84B8h

Figure 2-309. MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24
OSPI0_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							
23	22	21	20	19	18	17	16
OSPI0_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							
15	14	13	12	11	10	9	8
OSPI0_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							
7	6	5	4	3	2	1	0
OSPI0_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							

Table 2-621. MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OSPI0_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus.

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2.3.2.224 MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_WRITERESP Register

2.3.2.224.1 MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 184BCh) [reset = 0h]

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Table 2-622. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 84BCh

Figure 2-310. MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24
OSPI0_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							
23	22	21	20	19	18	17	16
OSPI0_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							
15	14	13	12	11	10	9	8
OSPI0_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							
7	6	5	4	3	2	1	0
OSPI0_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							

Table 2-623. MSS_CTRL_OSPI0_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OSPI0_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Read this bitfield for comparator status for Write response bus for this port. 1'b1 indicates error on Write Rsponse Bus.

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2.3.2.225 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_CTRL Register

2.3.2.225.1 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_CTRL Register (Offset = 18880h) [reset = 7h]

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Table 2-624. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8880h

Figure 2-311. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L2OCRAM_BANK4_BUS_SAFETY_CTRL_TYPE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							L2OCRAM_BANK4_BUS_SAFETY_CTRL_ERR_CLEAR
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					L2OCRAM_BANK4_BUS_SAFETY_CTRL_ENABLE		
NONE					R/W		
0h					7h		

Table 2-625. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	L2OCRAM_BANK4_BUS_SAFETY_CTRL_TYPE	R	0h	This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not. Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0. Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0. Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0. Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0. Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1. Bits 5-7 are set to 3'b000.
15:9	RESERVED	NONE	0h	Reserved
8	L2OCRAM_BANK4_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Set this bit to 1'b1 to clear the error status for this port
7:3	RESERVED	NONE	0h	Reserved
2:0	L2OCRAM_BANK4_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Set this bit to 3'b111 to enable the safety configuration for this port. Set this bit to 3'b000 to disable the safety configuration for this port.

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2.3.2.226 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_FI Register

2.3.2.226.1 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_FI Register (Offset = 18884h) [reset = 0h]

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Table 2-626. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8884h

Figure 2-312. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK4_BUS_SAFETY_FI_SAFE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L2OCRAM_BANK4_BUS_SAFETY_FI_MAIN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
L2OCRAM_BANK4_BUS_SAFETY_FI_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		L2OCRAM_BANK4_BUS_SAFETY_FI_DED	L2OCRAM_BANK4_BUS_SAFETY_FI_SEC	L2OCRAM_BANK4_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	L2OCRAM_BANK4_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	L2OCRAM_BANK4_BUS_SAFETY_FI_GLOBAL_SAFE	L2OCRAM_BANK4_BUS_SAFETY_FI_GLOBAL_MAIN
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 2-627. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	L2OCRAM_BANK4_BUS_SAFETY_FI_SAFE	R/W	0h	This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect. Bit 0 - Set this bit to inject fault on the Command bus. Bit 1 - Set this bit to inject fault on theWrite bus. Bit 2 - Set this bit to inject fault on the Write Status bus. Bit 3 - Set this bit to inject fault on the Read bus. Bit 7- Set this bit to inject fault on the corresponding request bus.
23:16	L2OCRAM_BANK4_BUS_SAFETY_FI_MAIN	R/W	0h	This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect. Bit 0 - Set this bit to inject fault on the Command bus. Bit 1 - Set this bit to inject fault on theWrite bus. Bit 2 - Set this bit to inject fault on the Write Status bus. Bit 3 - Set this bit to inject fault on the Read bus. Bit 7- Set this bit to inject fault on the corresponding request bus.
15:8	L2OCRAM_BANK4_BUS_SAFETY_FI_DATA	R/W	0h	Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus. Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.
7:6	RESERVED	NONE	0h	Reserved
5	L2OCRAM_BANK4_BUS_SAFETY_FI_DED	R/W	0h	Set this bit to 1'b1 inject ded error on data at this port
4	L2OCRAM_BANK4_BUS_SAFETY_FI_SEC	R/W	0h	Set this bit to 1'b1 to inject sec error on data at this port

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Table 2-627. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	L2OCRAM_BANK4_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Set this bit 1'b1 to inject fault for request signals on Safe Interconnect.
2	L2OCRAM_BANK4_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Set this bit to 1'b1 to inject fault for request signals on main Interconnect.
1	L2OCRAM_BANK4_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.
0	L2OCRAM_BANK4_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.

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2.3.2.227 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR Register

2.3.2.227.1 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR Register (Offset = 18888h) [reset = 0h]

Return to Summary Table

Table 2-628. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8888h

Figure 2-313. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK4_BUS_SAFETY_ERR_DED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L2OCRAM_BANK4_BUS_SAFETY_ERR_SEC							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
L2OCRAM_BANK4_BUS_SAFETY_ERR_COMP_CHECK							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
L2OCRAM_BANK4_BUS_SAFETY_ERR_COMP_ERR							
R							
0h							

Table 2-629. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	L2OCRAM_BANK4_BUS_SAFETY_ERR_DED	R	0h	This flag signals detection of dual error in Data at this port.Flag is generted for 32 bit segment of Data Bus Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus Bit [7:2] - Unused. Set to 1'b0
23:16	L2OCRAM_BANK4_BUS_SAFETY_ERR_SEC	R	0h	This flag signals detection of single error in Data at this port. Flag is generted for 32 bit segment of Data Bus Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus Bit [7:2] - Unused. Set to 1'b0
15:8	L2OCRAM_BANK4_BUS_SAFETY_ERR_COMP_CHECK	R	0h	This is used to verify the proper functioning of fault Injection on all the buses.1'b1 indicates error in the corresponding Bus has been injected successfully. Bit 0 - This is a Bitwise AND of error compares of all command bus signals. Bit 1 - This is a Bitwise AND of error compares of all write bus signals. Bit 2 - This is a Bitwise AND of error compares of all write status bus signals. Bit 3 - This is a Bitwise AND of error compares of all read bus signals. Bits [7:4] are unused.

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Table 2-629. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	L2OCRAM_BANK4_BUS_SAFETY_ERR_COMP_ERR	R	0h	1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal Bit 0 - This is a Bitwise OR of error compares of all command bus signals. Bit 1 - This is a Bitwise OR of error compares of all write bus signals. Bit 2 - This is a Bitwise OR of error compares of all write status bus signals. Bit 3 - This is a Bitwise OR of error compares of all read bus signals. Bits [7:4] are unused.

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2.3.2.228 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_DATA0 Register

2.3.2.228.1 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 1888Ch) [reset = 0h]

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Table 2-630. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 888Ch

Figure 2-314. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_DATA0_D1							
R							
0h							
7	6	5	4	3	2	1	0
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_DATA0_D0							
R							
0h							

Table 2-631. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC.
7:0	L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.

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2.3.2.229 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_CMD Register

2.3.2.229.1 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 18890h) [reset = 0h]

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Table 2-632. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8890h

Figure 2-315. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							
23	22	21	20	19	18	17	16
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							
15	14	13	12	11	10	9	8
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							
7	6	5	4	3	2	1	0
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							

Table 2-633. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus

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2.3.2.230 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITE Register

2.3.2.230.1 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 18894h) [reset = 0h]

Return to Summary Table

Table 2-634. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8894h

Figure 2-316. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							
23	22	21	20	19	18	17	16
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							
15	14	13	12	11	10	9	8
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							
7	6	5	4	3	2	1	0
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							

Table 2-635. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus

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2.3.2.231 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_READ Register

2.3.2.231.1 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_READ Register (Offset = 18898h) [reset = 0h]

Return to Summary Table

Table 2-636. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8898h

Figure 2-317. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							
23	22	21	20	19	18	17	16
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							
15	14	13	12	11	10	9	8
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							
7	6	5	4	3	2	1	0
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							

Table 2-637. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus.

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2.3.2.232 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITERESP Register

2.3.2.232.1 MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 1889Ch) [reset = 0h]

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Table 2-638. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 889Ch

Figure 2-318. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							
23	22	21	20	19	18	17	16
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							
15	14	13	12	11	10	9	8
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							
7	6	5	4	3	2	1	0
L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							

Table 2-639. MSS_CTRL_L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	L2OCRAM_BANK4_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Read this bitfield for comparator status for Write response bus for this port. 1'b1 indicates error on Write Rsponse Bus.

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2.3.2.233 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_CTRL Register

2.3.2.233.1 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_CTRL Register (Offset = 188A0h) [reset = 7h]

Return to Summary Table

Table 2-640. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 88A0h

Figure 2-319. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L2OCRAM_BANK5_BUS_SAFETY_CTRL_TYPE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							L2OCRAM_BANK5_BUS_SAFETY_CTRL_ERR_CLEAR
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					L2OCRAM_BANK5_BUS_SAFETY_CTRL_ENABLE		
NONE					R/W		
0h					7h		

Table 2-641. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	L2OCRAM_BANK5_BUS_SAFETY_CTRL_TYPE	R	0h	This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not. Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0. Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0. Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0. Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0. Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1. Bits 5-7 are set to 3'b000.
15:9	RESERVED	NONE	0h	Reserved
8	L2OCRAM_BANK5_BUS_SAFETY_CTRL_ERR_CLEAR	R/W	0h	Set this bit to 1'b1 to clear the error status for this port
7:3	RESERVED	NONE	0h	Reserved
2:0	L2OCRAM_BANK5_BUS_SAFETY_CTRL_ENABLE	R/W	7h	Set this bit to 3'b111 to enable the safety configuration for this port. Set this bit to 3'b000 to disable the safety configuration for this port.

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2.3.2.234 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_FI Register

2.3.2.234.1 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_FI Register (Offset = 188A4h) [reset = 0h]

Return to Summary Table

Table 2-642. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 88A4h

Figure 2-320. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_FI Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK5_BUS_SAFETY_FI_SAFE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L2OCRAM_BANK5_BUS_SAFETY_FI_MAIN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
L2OCRAM_BANK5_BUS_SAFETY_FI_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		L2OCRAM_BANK5_BUS_SAFETY_FI_DED	L2OCRAM_BANK5_BUS_SAFETY_FI_SEC	L2OCRAM_BANK5_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	L2OCRAM_BANK5_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	L2OCRAM_BANK5_BUS_SAFETY_FI_GLOBAL_SAFE	L2OCRAM_BANK5_BUS_SAFETY_FI_GLOBAL_MAIN
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 2-643. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_FI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	L2OCRAM_BANK5_BUS_SAFETY_FI_SAFE	R/W	0h	This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect. Bit 0 - Set this bit to inject fault on the Command bus. Bit 1 - Set this bit to inject fault on theWrite bus. Bit 2 - Set this bit to inject fault on the Write Status bus. Bit 3 - Set this bit to inject fault on the Read bus. Bit 7- Set this bit to inject fault on the corresponding request bus.
23:16	L2OCRAM_BANK5_BUS_SAFETY_FI_MAIN	R/W	0h	This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect. Bit 0 - Set this bit to inject fault on the Command bus. Bit 1 - Set this bit to inject fault on theWrite bus. Bit 2 - Set this bit to inject fault on the Write Status bus. Bit 3 - Set this bit to inject fault on the Read bus. Bit 7- Set this bit to inject fault on the corresponding request bus.
15:8	L2OCRAM_BANK5_BUS_SAFETY_FI_DATA	R/W	0h	Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus. Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.
7:6	RESERVED	NONE	0h	Reserved
5	L2OCRAM_BANK5_BUS_SAFETY_FI_DED	R/W	0h	Set this bit to 1'b1 inject ded error on data at this port
4	L2OCRAM_BANK5_BUS_SAFETY_FI_SEC	R/W	0h	Set this bit to 1'b1 to inject sec error on data at this port

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Table 2-643. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_FI Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	L2OCRAM_BANK5_BUS_SAFETY_FI_GLOBAL_SAFE_REQ	R/W	0h	Set this bit 1'b1 to inject fault for request signals on Safe Interconnect.
2	L2OCRAM_BANK5_BUS_SAFETY_FI_GLOBAL_MAIN_REQ	R/W	0h	Set this bit to 1'b1 to inject fault for request signals on main Interconnect.
1	L2OCRAM_BANK5_BUS_SAFETY_FI_GLOBAL_SAFE	R/W	0h	This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.
0	L2OCRAM_BANK5_BUS_SAFETY_FI_GLOBAL_MAIN	R/W	0h	This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.

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2.3.2.235 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR Register

2.3.2.235.1 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR Register (Offset = 188A8h) [reset = 0h]

Return to Summary Table

Table 2-644. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 88A8h

Figure 2-321. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK5_BUS_SAFETY_ERR_DED							
R							
0h							
23	22	21	20	19	18	17	16
L2OCRAM_BANK5_BUS_SAFETY_ERR_SEC							
R							
0h							
15	14	13	12	11	10	9	8
L2OCRAM_BANK5_BUS_SAFETY_ERR_COMP_CHECK							
R							
0h							
7	6	5	4	3	2	1	0
L2OCRAM_BANK5_BUS_SAFETY_ERR_COMP_ERR							
R							
0h							

Table 2-645. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	L2OCRAM_BANK5_BUS_SAFETY_ERR_DED	R	0h	This flag signals detection of dual error in Data at this port.Flag is generted for 32 bit segment of Data Bus Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus Bit [7:2] - Unused. Set to 1'b0
23:16	L2OCRAM_BANK5_BUS_SAFETY_ERR_SEC	R	0h	This flag signals detection of single error in Data at this port. Flag is generted for 32 bit segment of Data Bus Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus Bit [7:2] - Unused. Set to 1'b0
15:8	L2OCRAM_BANK5_BUS_SAFETY_ERR_COMP_CHECK	R	0h	This is used to verify the proper functioning of fault Injection on all the buses.1'b1 indicates error in the corresponding Bus has been injected successfully. Bit 0 - This is a Bitwise AND of error compares of all command bus signals. Bit 1 - This is a Bitwise AND of error compares of all write bus signals. Bit 2 - This is a Bitwise AND of error compares of all write status bus signals. Bit 3 - This is a Bitwise AND of error compares of all read bus signals. Bits [7:4] are unused.

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Table 2-645. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	L2OCRAM_BANK5_BUS_SAFETY_ERR_COMP_ERR	R	0h	1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal Bit 0 - This is a Bitwise OR of error compares of all command bus signals. Bit 1 - This is a Bitwise OR of error compares of all write bus signals. Bit 2 - This is a Bitwise OR of error compares of all write status bus signals. Bit 3 - This is a Bitwise OR of error compares of all read bus signals. Bits [7:4] are unused.

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2.3.2.236 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_DATA0 Register

2.3.2.236.1 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_DATA0 Register (Offset = 188ACh) [reset = 0h]

Return to Summary Table

Table 2-646. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 88ACh

Figure 2-322. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_DATA0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_DATA0_D1							
R							
0h							
7	6	5	4	3	2	1	0
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_DATA0_D0							
R							
0h							

Table 2-647. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_DATA0_D1	R	0h	Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC.
7:0	L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_DATA0_D0	R	0h	Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.

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2.3.2.237 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_CMD Register

2.3.2.237.1 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_CMD Register (Offset = 188B0h) [reset = 0h]

Return to Summary Table

Table 2-648. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 88B0h

Figure 2-323. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_CMD Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							
23	22	21	20	19	18	17	16
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							
15	14	13	12	11	10	9	8
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							
7	6	5	4	3	2	1	0
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_CMD_STAT							
R							
0h							

Table 2-649. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_CMD_STAT	R	0h	Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus

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2.3.2.238 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITE Register

2.3.2.238.1 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITE Register (Offset = 188B4h) [reset = 0h]

Return to Summary Table

Table 2-650. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 88B4h

Figure 2-324. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITE Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITE_STAT							
R							
0h							

Table 2-651. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITE_STAT	R	0h	Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus

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2.3.2.239 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_READ Register

2.3.2.239.1 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_READ Register (Offset = 188B8h) [reset = 0h]

Return to Summary Table

Table 2-652. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 88B8h

Figure 2-325. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_READ Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							
23	22	21	20	19	18	17	16
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							
15	14	13	12	11	10	9	8
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							
7	6	5	4	3	2	1	0
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_READ_STAT							
R							
0h							

Table 2-653. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_READ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_READ_STAT	R	0h	Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus.

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2.3.2.240 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITERESP Register

2.3.2.240.1 MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITERESP Register (Offset = 188BCh) [reset = 0h]

Return to Summary Table

Table 2-654. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 88BCh

Figure 2-326. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITERESP Name Register

31	30	29	28	27	26	25	24
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							
23	22	21	20	19	18	17	16
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							
15	14	13	12	11	10	9	8
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							
7	6	5	4	3	2	1	0
L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITERESP_STAT							
R							
0h							

Table 2-655. MSS_CTRL_L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITERESP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	L2OCRAM_BANK5_BUS_SAFETY_ERR_STAT_WRITERESP_STAT	R	0h	Read this bitfield for comparator status for Write response bus for this port. 1'b1 indicates error on Write Rsponse Bus.

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2.4 TOP_RCM

TOP_RCM

2.4.1 TOP_RCM Summaries

TOP_RCM Summaries

Table 2-656. TOP_RCM Registers, Base Address=5320 0000h, Length=4096

Offset	Length	Register Name	TOP_RCM Physical Address
4h	32	TOP_RCM_WARM_RESET_CONFIG	5320 0004h
8h	32	TOP_RCM_WARM_RESET_REQ	5320 0008h
Ch	32	TOP_RCM_WARM_RST_CAUSE	5320 000Ch
10h	32	TOP_RCM_WARM_RST_CAUSE_CLR	5320 0010h
14h	32	TOP_RCM_RCOSC32K_CTRL	5320 0014h
18h	32	TOP_RCM_LIMP_MODE_EN	5320 0018h
1Ch	32	TOP_RCM_PLL_REF_CLK_SRC_SEL	5320 001Ch
24h	32	TOP_RCM_SOP_MODE_VALUE	5320 0024h
28h	32	TOP_RCM_CLK_LOSS_STATUS	5320 0028h
30h	32	TOP_RCM_WARM_RSTTIME1	5320 0030h
34h	32	TOP_RCM_WARM_RSTTIME2	5320 0034h
38h	32	TOP_RCM_WARM_RSTTIME3	5320 0038h
3Ch	32	TOP_RCM_WARM_RESET_CONFIG_OV	5320 003Ch
40h	32	TOP_RCM_WARM_RESET_CONFIG_UV	5320 0040h
44h	32	TOP_RCM_WARM_RESET_CONFIG_MISC	5320 0044h
400h	32	TOP_RCM_PLL_CORE_PWRCTRL	5320 0400h
404h	32	TOP_RCM_PLL_CORE_CLKCTRL	5320 0404h
408h	32	TOP_RCM_PLL_CORE_TENABLE	5320 0408h
40Ch	32	TOP_RCM_PLL_CORE_TENABLEDIV	5320 040Ch
410h	32	TOP_RCM_PLL_CORE_M2NDIV	5320 0410h
414h	32	TOP_RCM_PLL_CORE_MN2DIV	5320 0414h
418h	32	TOP_RCM_PLL_CORE_FRACDIV	5320 0418h
41Ch	32	TOP_RCM_PLL_CORE_BWCTRL	5320 041Ch
420h	32	TOP_RCM_PLL_CORE_FRACCTRL	5320 0420h
424h	32	TOP_RCM_PLL_CORE_STATUS	5320 0424h
428h	32	TOP_RCM_PLL_CORE_HSDIVIDER	5320 0428h
42Ch	32	TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT0	5320 042Ch
430h	32	TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT1	5320 0430h
434h	32	TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT2	5320 0434h
438h	32	TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT3	5320 0438h
43Ch	32	TOP_RCM_PLL_CORE_RSTCTRL	5320 043Ch
440h	32	TOP_RCM_PLL_CORE_HSDIVIDER_RSTCTRL	5320 0440h
500h	32	TOP_RCM_R5SS_CLK_SRC_SEL	5320 0500h
504h	32	TOP_RCM_R5SS_CLK_STATUS	5320 0504h
510h	32	TOP_RCM_R5SS0_CLK_DIV_SEL	5320 0510h
514h	32	TOP_RCM_R5SS1_CLK_DIV_SEL	5320 0514h
518h	32	TOP_RCM_R5SS0_CLK_GATE	5320 0518h
51Ch	32	TOP_RCM_R5SS1_CLK_GATE	5320 051Ch
520h	32	TOP_RCM_SYS_CLK_DIV_VAL	5320 0520h
524h	32	TOP_RCM_SYS_CLK_GATE	5320 0524h

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Table 2-656. TOP_RCM Registers, Base Address=5320 0000h, Length=4096 (continued)

Offset	Length	Register Name	TOP_RCM Physical Address
528h	32	TOP_RCM_SYS_CLK_STATUS	5320 0528h
800h	32	TOP_RCM_PLL_PER_PWRCTRL	5320 0800h
804h	32	TOP_RCM_PLL_PER_CLKCTRL	5320 0804h
808h	32	TOP_RCM_PLL_PER_TENABLE	5320 0808h
80Ch	32	TOP_RCM_PLL_PER_TENABLEDIV	5320 080Ch
810h	32	TOP_RCM_PLL_PER_M2NDIV	5320 0810h
814h	32	TOP_RCM_PLL_PER_MN2DIV	5320 0814h
818h	32	TOP_RCM_PLL_PER_FRACDIV	5320 0818h
81Ch	32	TOP_RCM_PLL_PER_BWCTRL	5320 081Ch
820h	32	TOP_RCM_PLL_PER_FRACCTRL	5320 0820h
824h	32	TOP_RCM_PLL_PER_STATUS	5320 0824h
828h	32	TOP_RCM_PLL_PER_HSDIVIDER	5320 0828h
82Ch	32	TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT0	5320 082Ch
830h	32	TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT1	5320 0830h
834h	32	TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT2	5320 0834h
83Ch	32	TOP_RCM_PLL_PER_RSTCTRL	5320 083Ch
840h	32	TOP_RCM_PLL_PER_HSDIVIDER_RSTCTRL	5320 0840h
C00h	32	TOP_RCM_CLKOUT0_CLK_SRC_SEL	5320 0C00h
C04h	32	TOP_RCM_CLKOUT1_CLK_SRC_SEL	5320 0C04h
C08h	32	TOP_RCM_CLKOUT0_DIV_VAL	5320 0C08h
C0Ch	32	TOP_RCM_CLKOUT1_DIV_VAL	5320 0C0Ch
C10h	32	TOP_RCM_CLKOUT0_CLK_GATE	5320 0C10h
C14h	32	TOP_RCM_CLKOUT1_CLK_GATE	5320 0C14h
C18h	32	TOP_RCM_CLKOUT0_CLK_STATUS	5320 0C18h
C1Ch	32	TOP_RCM_CLKOUT1_CLK_STATUS	5320 0C1Ch
C20h	32	TOP_RCM_TRCCLKOUT_CLK_SRC_SEL	5320 0C20h
C24h	32	TOP_RCM_TRCCLKOUT_DIV_VAL	5320 0C24h
C28h	32	TOP_RCM_TRCCLKOUT_CLK_GATE	5320 0C28h
C2Ch	32	TOP_RCM_TRCCLKOUT_CLK_STATUS	5320 0C2Ch
1008h	32	TOP_RCM_LOCK0_KICK0	5320 1008h
100Ch	32	TOP_RCM_LOCK0_KICK1	5320 100Ch
1010h	32	TOP_RCM_INTR_RAW_STATUS	5320 1010h
1014h	32	TOP_RCM_INTR_ENABLED_STATUS_CLEAR	5320 1014h
1018h	32	TOP_RCM_INTR_ENABLE	5320 1018h
101Ch	32	TOP_RCM_INTR_ENABLE_CLEAR	5320 101Ch
1020h	32	TOP_RCM_EOI	5320 1020h
1024h	32	TOP_RCM_FAULT_ADDRESS	5320 1024h
1028h	32	TOP_RCM_FAULT_TYPE_STATUS	5320 1028h
102Ch	32	TOP_RCM_FAULT_ATTR_STATUS	5320 102Ch
1030h	32	TOP_RCM_FAULT_CLEAR	5320 1030h

2.4.2 TOP_RCM Registers

TOP_RCM Registers

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2.4.2.1 TOP_RCM_WARM_RESET_CONFIG Register

2.4.2.1.1 TOP_RCM_WARM_RESET_CONFIG Register (Offset = 4h) [reset = 77770077h]

Warm Reset Config options.

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Table 2-657. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0004h

Figure 2-327. TOP_RCM_WARM_RESET_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED	WARM_RESET_CONFIG_WDOG3_RST_EN			RESERVED	WARM_RESET_CONFIG_WDOG2_RST_EN		
NONE	R/W			NONE	R/W		
0h	7h			0h	7h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	WARM_RESET_CONFIG_WDOG1_RST_EN			RESERVED	WARM_RESET_CONFIG_WDOG0_RST_EN		
NONE	R/W			NONE	R/W		
0h	7h			0h	7h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	WARM_RESET_CONFIG_TSENSE1_RST_EN			RESERVED	WARM_RESET_CONFIG_TSENSE0_RST_EN		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	WARM_RESET_CONFIG_DEBUGSS_RST_EN			RESERVED	WARM_RESET_CONFIG_PAD_BYPASS		
NONE	R/W			NONE	R/W		
0h	7h			0h	7h		

Table 2-658. TOP_RCM_WARM_RESET_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	WARM_RESET_CONFIG_WDOG3_RST_EN	R/W	7h	Enable/Disable WATCHDOG3 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog Write 3'b111 enable corresponding Watchdog
27	RESERVED	NONE	0h	Reserved
26:24	WARM_RESET_CONFIG_WDOG2_RST_EN	R/W	7h	Enable/Disable WATCHDOG2 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog Write 3'b111 enable corresponding Watchdog
23	RESERVED	NONE	0h	Reserved
22:20	WARM_RESET_CONFIG_WDOG1_RST_EN	R/W	7h	Enable/Disable WATCHDOG1 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog Write 3'b111 enable corresponding Watchdog
19	RESERVED	NONE	0h	Reserved
18:16	WARM_RESET_CONFIG_WDOG0_RST_EN	R/W	7h	Enable/Disable WATCHDOG0 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog Write 3'b111 enable corresponding Watchdog
15	RESERVED	NONE	0h	Reserved

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Table 2-658. TOP_RCM_WARM_RESET_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	WARM_RESET_CONFIG_TSENSE1_RST_EN	R/W	0h	Enable/Disable TEMPSENSE1 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable temperature sensor 1 Write 3'b111 to enable temperature sensor 1 **Note: This bit will only be reset by PORz.
11	RESERVED	NONE	0h	Reserved
10:8	WARM_RESET_CONFIG_TSENSE0_RST_EN	R/W	0h	Enable/Disable TEMPSENSE0 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable temperature sensor 0 Write 3'b111 to enable temperature sensor 0 **Note: This bit will only be reset by PORz.
7	RESERVED	NONE	0h	Reserved
6:4	WARM_RESET_CONFIG_DEBUGSS_RST_EN	R/W	7h	Enable/Disable DEBUGSS triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable debugger control on Warm Reset Write 3'b111 enable debugger control on Warm Reset
3	RESERVED	NONE	0h	Reserved
2:0	WARM_RESET_CONFIG_PAD_BYPASS	R/W	7h	Bypass the Warm reset from Pad Input Data should be loaded as multibit. Write 3'b000 : Pad Warm Reset pin has control over warm reset Write 3'b111 : Pad warm reset pin has no control on warm reset **Note: This bit will only be reset by PORz.

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2.4.2.2 TOP_RCM_WARM_RESET_REQ Register

2.4.2.2.1 TOP_RCM_WARM_RESET_REQ Register (Offset = 8h) [reset = 7h]

Warm Reset Config options.

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Table 2-659. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0008h

Figure 2-328. TOP_RCM_WARM_RESET_REQ Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WARM_RESET_REQ_SW_RST		
NONE					R/W		
0h					7h		

Table 2-660. TOP_RCM_WARM_RESET_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WARM_RESET_REQ_SW_RST	R/W	7h	Data should be loaded as multibit. Write 3'b000 to assert warm reset from SW Write 3'b111 to deassert warm reset from SW if this is the only source of warm reset

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2.4.2.3 TOP_RCM_WARM_RST_CAUSE Register

2.4.2.3.1 TOP_RCM_WARM_RST_CAUSE Register (Offset = Ch) [reset = 41h]

Warm Reset Cause Register.

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Table 2-661. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 000Ch

Figure 2-329. TOP_RCM_WARM_RST_CAUSE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WARM_RST_CAUSE_CAUSE							
R							
41h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
WARM_RST_CAUSE_CAUSE							
R							
41h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WARM_RST_CAUSE_CAUSE							
R							
41h							

Table 2-662. TOP_RCM_WARM_RST_CAUSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	WARM_RST_CAUSE_CAUSE	R	41h	Warm Reset Cause register 24'h000041 - POR reset 24'h000042 - Warm reset due to MSS_WDT0 24'h000044 - Warm reset due to MSS_WDT1 24'h000048 - Warm reset due to MSS_WDT2 24'h000050 - Warm reset due to MSS_WDT3 24'h000060 - Warm reset due to TOP_RMC:WARM_RESET_REQ 24'h000040 - External Pad reset 24'h0000C0 - Warm reset due to HSM_WDT 24'h000140 - Warm Reset due to Deugger reset 24'h000240 - Warm Reset due to Temp Sense0 Reset 24'h000440 - Warm Reset due to Temp Sense1 Reset 24'h000840 - Warm Reset due to vmon_cmp1_ov 24'h001040 - Warm Reset due to vmon_cmp2_ov 24'h002040 - Warm Reset due to vmon_cmp3_ov 24'h004040 - Warm Reset due to vmon_cmp5_ov 24'h008040 - Warm Reset due to vmon_cmp0_uv 24'h010040 - Warm Reset due to vmon_cmp1_uv 24'h020040 - Warm Reset due to vmon_cmp2_uv 24'h040040 - Warm Reset due to vmon_cmp3_uv 24'h080040 - Warm Reset due to vmon_cmp5_uv 24'h100040 - Warm Reset due to vmon_cmp7_uv 24'h200040 - Warm Reset due to vmon_cmp8_uv 24'h400040 - Warm Reset due to esm 24'h800040 - Warm Reset due to clk_loss on sys_clk

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2.4.2.4 TOP_RCM_WARM_RST_CAUSE_CLR Register

2.4.2.4.1 TOP_RCM_WARM_RST_CAUSE_CLR Register (Offset = 10h) [reset = 0h]

Warm Reset Cause Register Clear.

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Table 2-663. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0010h

Figure 2-330. TOP_RCM_WARM_RST_CAUSE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WARM_RST_CAUSE_CLR_CLEAR		
NONE					R/W		
0h					0h		

Table 2-664. TOP_RCM_WARM_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WARM_RST_CAUSE_CLR_CLEAR	R/W	0h	Write pulse bit field to 3'b111: Data should be loaded as multibit. Warm Reset Cause register Clear

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2.4.2.5 TOP_RCM_RCOSC32K_CTRL Register

2.4.2.5.1 TOP_RCM_RCOSC32K_CTRL Register (Offset = 14h) [reset = 0h]

RC OSC 32KHz clock control.

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Table 2-665. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0014h

Figure 2-331. TOP_RCM_RCOSC32K_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RCOSC32K_CTRL_STOPOSC		
NONE					R/W		
0h					0h		

Table 2-666. TOP_RCM_RCOSC32K_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RCOSC32K_CTRL_STOPOSC	R/W	0h	Stop 32KHz RCOSC. Write 3'b111 to stop clock

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2.4.2.6 TOP_RCM_LIMP_MODE_EN Register

2.4.2.6.1 TOP_RCM_LIMP_MODE_EN Register (Offset = 18h) [reset = 0h]

Control to enabled limp mode.

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Table 2-667. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0018h

Figure 2-332. TOP_RCM_LIMP_MODE_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					LIMP_MODE_EN_COREPLL_LOSS_EN		
NONE					R/W		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED	LIMP_MODE_EN_XTALCLK_LOSS_EN			RESERVED	LIMP_MODE_EN_DCC0_ERROR_EN		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 2-668. TOP_RCM_LIMP_MODE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	LIMP_MODE_EN_COREPLL_LOSS_EN	R/W	0h	Enable for core pll phase lock loss to generate Limp mode 3'b000: will not generate Limp mode [multibit 000] 3'b111 : will generate Limp mode [multibit 111]
7	RESERVED	NONE	0h	Reserved
6:4	LIMP_MODE_EN_XTALCLK_LOSS_EN	R/W	0h	Enable for crystal_clock_loss to generate Limp mode 3'b000: will not generate Limp mode [multibit 000] 3'b111 : will generate Limp mode [multibit 111]
3	RESERVED	NONE	0h	Reserved
2:0	LIMP_MODE_EN_DCC0_ERROR_EN	R/W	0h	Enable DCC0 Error to generate Limp mode 3'b000: DCC0 Error will not generate Limp mode [multibit 000] 3'b111 : DCC0 Error will generate Limp mode [multibit 111]

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2.4.2.7 TOP_RCM_PLL_REF_CLK_SRC_SEL Register

2.4.2.7.1 TOP_RCM_PLL_REF_CLK_SRC_SEL Register (Offset = 1Ch) [reset = 0h]

CORE PLL and PERI PLL reference clock select.

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Table 2-669. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 001Ch

Figure 2-333. TOP_RCM_PLL_REF_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PLL_REF_CLK_SRC_SEL_PLL_PERI_REF_CLK_SRC_SEL			RESERVED	PLL_REF_CLK_SRC_SEL_PLL_CORE_REF_CLK_SRC_SEL		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 2-670. TOP_RCM_PLL_REF_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:4	PLL_REF_CLK_SRC_SEL_PLL_PERI_REF_CLK_SRC_SEL	R/W	0h	Mux selct for PERI PLL REF clock Write 3'b111 : to select external reference clock as PLL reference clock Write 3'b000 : to select on-die clock as PLL reference clock
3	RESERVED	NONE	0h	Reserved
2:0	PLL_REF_CLK_SRC_SEL_PLL_CORE_REF_CLK_SRC_SEL	R/W	0h	Mux selct for CORE PLL REF clock Write 3'b111 : to select external reference clock as PLL reference clock Write 3'b000 : to select on-die clock as PLL reference clock

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2.4.2.8 TOP_RCM_SOP_MODE_VALUE Register

2.4.2.8.1 TOP_RCM_SOP_MODE_VALUE Register (Offset = 24h) [reset = 0h]

Sense on Power mode value.

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Table 2-671. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0024h

Figure 2-334. TOP_RCM_SOP_MODE_VALUE Name Register

31	30	29	28	27	26	25	24
SOP_MODE_VALUE_VAL							
R							
0h							
23	22	21	20	19	18	17	16
SOP_MODE_VALUE_VAL							
R							
0h							
15	14	13	12	11	10	9	8
SOP_MODE_VALUE_VAL							
R							
0h							
7	6	5	4	3	2	1	0
SOP_MODE_VALUE_VAL							
R							
0h							

Table 2-672. TOP_RCM_SOP_MODE_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SOP_MODE_VALUE_VAL	R	0h	Bootmode (SOP_MODE) values and their corresponding mapping SOP3 SOP2 SOP1 SOP0 Bootmode 0 0 0 0 OSPI Functional Mode[4S] 0 0 0 1 UART Functional Mode 0 0 1 0 OSPI Functional Mode[1S] 0 0 1 1 OSPI Functional Mode[8S] 1 0 1 1 Devboot mode 1 1 0 0 xSPI 8D (SFDP) mode Any undefined values are reserved for future use. Note: Reset value of MMR is 0, but true SOP pin values will latch immediately after PORz reset is released. CPU reads to the MMR will only reflect the SOP mode values latched at reset.

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2.4.2.9 TOP_RCM_CLK_LOSS_STATUS Register

2.4.2.9.1 TOP_RCM_CLK_LOSS_STATUS Register (Offset = 28h) [reset = 100h]

Coarse detection clock loss status for RC and Crystal.

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Table 2-673. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0028h

Figure 2-335. TOP_RCM_CLK_LOSS_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							CLK_LOSS_STATUS_RC_GOOD_BOOT
NONE							R
0h							1h
7	6	5	4	3	2	1	0
RESERVED			CLK_LOSS_STATUS_RC_CLOCK_LOSS	RESERVED			CLK_LOSS_STATUS_CRYSTAL_CLOCK_LOSS
NONE			R	NONE			R
0h			0h	0h			0h

Table 2-674. TOP_RCM_CLK_LOSS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CLK_LOSS_STATUS_RC_GOOD_BOOT	R	1h	Clock status of RC clock at boot. Reset value will reflect the actual status 1 --> clock present at boot 0 --> clock not present at boot
7:5	RESERVED	NONE	0h	Reserved
4	CLK_LOSS_STATUS_RC_CLOCK_LOSS	R	0h	Coarse detection clock loss status for RC clock. Reset value will reflect the actual status 1 --> clock lost 0 --> clock good
3:1	RESERVED	NONE	0h	Reserved
0	CLK_LOSS_STATUS_CRYSTAL_CLOCK_LOSS	R	0h	Coarse detection clock loss status for Crystal clock. Reset value will reflect the actual status 1 --> clock lost 0 --> clock good

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2.4.2.10 TOP_RCM_WARM_RSTTIME1 Register

2.4.2.10.1 TOP_RCM_WARM_RSTTIME1 Register (Offset = 30h) [reset = 888h]

programing Output delay: time between internal warm reset source assert to warm reset pad deassert.

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Table 2-675. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0030h

Figure 2-336. TOP_RCM_WARM_RSTTIME1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WARM_RSTTIME1_DELAY			
NONE				R/W			
0h				888h			
7	6	5	4	3	2	1	0
WARM_RSTTIME1_DELAY							
R/W							
888h							

Table 2-676. TOP_RCM_WARM_RSTTIME1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WARM_RSTTIME1_DELAY	R/W	888h	Program sufficient delay using this bitfield to keep the WARMRSTn pad active for any external devices relying on the reset signal. Refer to Reset Details Section in TRM for more details. Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register. **Note: This bit will only be reset by PORz.

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2.4.2.11 TOP_RCM_WARM_RSTTIME2 Register

2.4.2.11.1 TOP_RCM_WARM_RSTTIME2 Register (Offset = 34h) [reset = 888h]

programing input Rise delay : time between warm reset pad deassert to chip warm reset deassert.

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Table 2-677. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0034h

Figure 2-337. TOP_RCM_WARM_RSTTIME2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WARM_RSTTIME2_DELAY			
NONE				R/W			
0h				888h			
7	6	5	4	3	2	1	0
WARM_RSTTIME2_DELAY							
R/W							
888h							

Table 2-678. TOP_RCM_WARM_RSTTIME2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WARM_RSTTIME2_DELAY	R/W	888h	Program the deassertion delay with this bitfield to control internal system reset deassertion which is relative to the deassertion of WARMRSTn pad. Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register. **Note: This bit will only be reset by PORz.

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2.4.2.12 TOP_RCM_WARM_RSTTIME3 Register

2.4.2.12.1 TOP_RCM_WARM_RSTTIME3 Register (Offset = 38h) [reset = 111h]

programing Input Fall delay : time between warm reset pad assert to chip warm reset assert.

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Table 2-679. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0038h

Figure 2-338. TOP_RCM_WARM_RSTTIME3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WARM_RSTTIME3_DELAY			
NONE				R/W			
0h				111h			
7	6	5	4	3	2	1	0
WARM_RSTTIME3_DELAY							
R/W							
111h							

Table 2-680. TOP_RCM_WARM_RSTTIME3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WARM_RSTTIME3_DELAY	R/W	111h	The glitch filter logic will filter any input pad signal which is LOW for any time less than the delay programmed with this bit.This parameter also programmes the delay from external Warmrestn assertion to Internal system warm resetn assertion. Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register. **Note: This bit will only be reset by PORz.

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2.4.2.13 TOP_RCM_WARM_RESET_CONFIG_OV Register

2.4.2.13.1 TOP_RCM_WARM_RESET_CONFIG_OV Register (Offset = 3Ch) [reset = 0h]

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Table 2-681. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 003Ch

Figure 2-339. TOP_RCM_WARM_RESET_CONFIG_OV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				WARM_RESET_CONFIG_OV_VMON_CMP5_OV_RST_EN			WARM_RESET_CONFIG_OV_VMON_CMP3_OV_RST_EN
NONE				R/W			R/W
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WARM_RESET_CONFIG_OV_VMON_CMP3_OV_RST_EN		WARM_RESET_CONFIG_OV_VMON_CMP2_OV_RST_EN			WARM_RESET_CONFIG_OV_VMON_CMP1_OV_RST_EN		
R/W		R/W			R/W		
0h		0h			0h		

Table 2-682. TOP_RCM_WARM_RESET_CONFIG_OV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:9	WARM_RESET_CONFIG_OV_VMON_CMP5_OV_RST_EN	R/W	0h	Enable/Disable VMON Overvoltage CMP5 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_ov rst_en Write 3'b111 to enable vmon_ov rst_en **Note: This bit will only be reset by PORz.
8:6	WARM_RESET_CONFIG_OV_VMON_CMP3_OV_RST_EN	R/W	0h	Enable/Disable VMON Overvoltage CMP3 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_ov rst_en Write 3'b111 to enable vmon_ov rst_en **Note: This bit will only be reset by PORz.
5:3	WARM_RESET_CONFIG_OV_VMON_CMP2_OV_RST_EN	R/W	0h	Enable/Disable VMON Overvoltage CMP2 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_ov rst_en Write 3'b111 to enable vmon_ov rst_en **Note: This bit will only be reset by PORz.
2:0	WARM_RESET_CONFIG_OV_VMON_CMP1_OV_RST_EN	R/W	0h	Enable/Disable VMON Overvoltage CMP1 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_ov rst_en Write 3'b111 to enable vmon_ov rst_en **Note: This bit will only be reset by PORz.

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2.4.2.14 TOP_RCM_WARM_RESET_CONFIG_UV Register

2.4.2.14.1 TOP_RCM_WARM_RESET_CONFIG_UV Register (Offset = 40h) [reset = 0h]

Return to Summary Table

Table 2-683. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0040h

Figure 2-340. TOP_RCM_WARM_RESET_CONFIG_UV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED			WARM_RESET_CONFIG_UV_VMON_CMP8_UV_RST_EN			WARM_RESET_CONFIG_UV_VMON_CMP7_UV_RST_EN	
NONE			R/W			R/W	
0h			0h			0h	

15	14	13	12	11	10	9	8
WARM_RESET_CONFIG_UV_VMON_CMP7_UV_RST_EN	WARM_RESET_CONFIG_UV_VMON_CMP5_UV_RST_EN			WARM_RESET_CONFIG_UV_VMON_CMP3_UV_RST_EN			WARM_RESET_CONFIG_UV_VMON_CMP2_UV_RST_EN
R/W	R/W			R/W			R/W
0h	0h			0h			0h

7	6	5	4	3	2	1	0
WARM_RESET_CONFIG_UV_VMON_CMP2_UV_RST_EN		WARM_RESET_CONFIG_UV_VMON_CMP1_UV_RST_EN			WARM_RESET_CONFIG_UV_VMON_CMP0_UV_RST_EN		
R/W		R/W			R/W		
0h		0h			0h		

Table 2-684. TOP_RCM_WARM_RESET_CONFIG_UV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:21	RESERVED	NONE	0h	Reserved
20:18	WARM_RESET_CONFIG_UV_VMON_CMP8_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP8 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_uv rst_en Write 3'b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz.
17:15	WARM_RESET_CONFIG_UV_VMON_CMP7_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP7 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_uv rst_en Write 3'b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz.
14:12	WARM_RESET_CONFIG_UV_VMON_CMP5_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP5 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_uv rst_en Write 3'b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz.
11:9	WARM_RESET_CONFIG_UV_VMON_CMP3_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP3 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_uv rst_en Write 3'b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz.

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Table 2-684. TOP_RCM_WARM_RESET_CONFIG_UV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:6	WARM_RESET_CONFIG_UV_VMON_CMP2_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP2 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_uv rst_en Write 3'b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz.
5:3	WARM_RESET_CONFIG_UV_VMON_CMP1_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP1 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_uv rst_en Write 3'b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz.
2:0	WARM_RESET_CONFIG_UV_VMON_CMP0_UV_RST_EN	R/W	0h	Enable/Disable VMON Undervoltage CMP0 triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable vmon_uv rst_en Write 3'b111 to enable vmon_uv rst_en **Note: This bit will only be reset by PORz.

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2.4.2.15 TOP_RCM_WARM_RESET_CONFIG_MISC Register

2.4.2.15.1 TOP_RCM_WARM_RESET_CONFIG_MISC Register (Offset = 44h) [reset = 0h]

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Table 2-685. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0044h

Figure 2-341. TOP_RCM_WARM_RESET_CONFIG_MISC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		WARM_RESET_CONFIG_MISC_CLK_LOSS_SYS_CLK_RST_EN			WARM_RESET_CONFIG_MISC_ESM_RST_EN		
NONE		R/W			R/W		
0h		0h			0h		

Table 2-686. TOP_RCM_WARM_RESET_CONFIG_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:3	WARM_RESET_CONFIG_MISC_CLK_LOSS_SYS_CLK_RST_EN	R/W	0h	Enable/Disable Clock loss on SYS_CLK triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable clk_loss on sys_clk rst_en Write 3'b111 to enable clk_loss on sys_clk rst_en
2:0	WARM_RESET_CONFIG_MISC_ESM_RST_EN	R/W	0h	Enable/Disable ESM triggering Warm Reset Data should be loaded as multibit. Write 3'b000 to disable esm rst_en Write 3'b111 to enable esm rst_en

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2.4.2.16 TOP_RCM_PLL_CORE_PWRCTRL Register

2.4.2.16.1 TOP_RCM_PLL_CORE_PWRCTRL Register (Offset = 400h) [reset = 30h]

Power control for Core PLL.

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Table 2-687. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0400h

Figure 2-342. TOP_RCM_PLL_CORE_PWRCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PLL_CORE_PWRCTRL_PONIN	PLL_CORE_PWRCTRL_PGOODIN	PLL_CORE_PWRCTRL_RET	PLL_CORE_PWRCTRL_ISORET	PLL_CORE_PWRCTRL_ISOSCAN	PLL_CORE_PWRCTRL_OFFMODE
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		1h	1h	0h	0h	0h	0h

Table 2-688. TOP_RCM_PLL_CORE_PWRCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	PLL_CORE_PWRCTRL_PONIN	R/W	1h	ON/OFF control of the weak power switch digital. For functional mode it should be 1'b1
4	PLL_CORE_PWRCTRL_PGOODIN	R/W	1h	ON/OFF control of the strong power switch digital. For functional mode it should be 1'b1
3	PLL_CORE_PWRCTRL_RET	R/W	0h	Save/Restore control for Retention mode. For functional mode it should be 1'b0
2	PLL_CORE_PWRCTRL_ISORET	R/W	0h	Save/Restore control for Isolation of output pins For functional mode it should be 1'b0
1	PLL_CORE_PWRCTRL_ISOSCAN	R/W	0h	Save/Restore control for Isolation of the Scanout pins. For functional mode it should be 1'b0
0	PLL_CORE_PWRCTRL_OFFMODE	R/W	0h	Used to switch OFF the logic on VDDA. For functional mode it should be 1'b0

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2.4.2.17 TOP_RCM_PLL_CORE_CLKCTRL Register

2.4.2.17.1 TOP_RCM_PLL_CORE_CLKCTRL Register (Offset = 404h) [reset = 895000h]

Clock control for Core PLL.

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Table 2-689. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0404h

Figure 2-343. TOP_RCM_PLL_CORE_CLKCTRL Name Register

31	30	29	28	27	26	25	24
PLL_CORE_CLKCTRL_CYCLESLIPEN	PLL_CORE_CLKCTRL_ENSSC	PLL_CORE_CLKCTRL_CLKDCOLDOEN	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PLL_CORE_CLKCTRL_IDLE	PLL_CORE_CLKCTRL_BYPASSACKZ	PLL_CORE_CLKCTRL_STBYRET	PLL_CORE_CLKCTRL_CLKOUTEN	PLL_CORE_CLKCTRL_CLKOUTLDOEN	PLL_CORE_CLKCTRL_ULOWCLKEN	PLL_CORE_CLKCTRL_CLKDCOLDOPWDNZ	PLL_CORE_CLKCTRL_M2PWDNZ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	1h	0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PLL_CORE_CLKCTRL_STOPMODE	RESERVED	PLL_CORE_CLKCTRL_SELFREQDCO			RESERVED	PLL_CORE_CLKCTRL_RELAXED_LOCK
NONE	R/W	NONE	R/W			NONE	R/W
0h	1h	0h	4h			0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PLL_CORE_CLKCTRL_SSCTYPE	PLL_CORE_CLKCTRL_TINTZ
NONE						R/W	R/W
0h						0h	0h

Table 2-690. TOP_RCM_PLL_CORE_CLKCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_CORE_CLKCTRL_CYCLESLIPEN	R/W	0h	FailSafe enable to trigger re-calibration in case CycleSlip occurs between REFCLK and FBCLK. Cycleslip could be caused if loop is not able to track input clock. Default = 1'b0 recommended
30	PLL_CORE_CLKCTRL_ENSSC	R/W	0h	Controls Clock SpReading. SSC is not supported. Should be set to 0x0 to disable clock spReading.
29	PLL_CORE_CLKCTRL_CLKDCOLDOEN	R/W	0h	Synchronously enables/disables CLKDCOLDO 0x0 : synchronously disables CLKDCOLDO 0x1 : synchronously enables CLKDCOLDO
28:24	RESERVED	NONE	0h	Reserved
23	PLL_CORE_CLKCTRL_IDLE	R/W	1h	Sets PLL to Idle mode 0x0 : When SYSRESET = 0 and TINITZ = 1 IDLE = 0 PLL will go to Active and Locked 0x1 : When SYSRESET = 0 and TINITZ = 1 IDLE = 1 PLL will go to Idle Bypass low powe

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Table 2-690. TOP_RCM_PLL_CORE_CLKCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	PLL_CORE_CLKCTRL_BYPASSACKZ	R/W	0h	BYPASSACKZ is a special purpose input to the module. In general this input is expected to be tied to static low. For the output clocks of the module that do not have an internal bypass mux viz. CLKDCOLDO and CLKOUTLDO, a bypass mux could be implemented external to the module.
21	PLL_CORE_CLKCTRL_STBYRET	R/W	0h	Standby retention control 0x0 : prepares ADPLLLJ for relock when out of retention by removing the gating on all internal clocks. 0x1 : prepares ADPLLLJ for retention by gating all the internal clocks.
20	PLL_CORE_CLKCTRL_CLKOUTEN	R/W	0h	CLKOUT enable or disable 0x0 : synchronously disables CLKOUT 0x1 : synchronously enables CLKOUT
19	PLL_CORE_CLKCTRL_CLKOUTLDOEN	R/W	1h	Synchronously enables/disables CLKOUTLDO 0x0 : synchronously disables CLKOUTLDO 0x1 : synchronously enables CLKOUTLDO
18	PLL_CORE_CLKCTRL_ULOWCLKEN	R/W	0h	Select CLKOUT source in bypass 0x0: When ADPLLLJ in bypass mode, CLKOUT = CLKINP/[N2+1] 0x1: When ADPLLLJ in bypass mode, CLKOUT = CLKINPULOW.
17	PLL_CORE_CLKCTRL_CLKDCOLDOPWDNZ	R/W	0h	0 Asynchronous power down for CLKDCOLDO o/p.
16	PLL_CORE_CLKCTRL_M2PWDNZ	R/W	1h	M2 divider power down mode 0x0: Asynchronous power down for M2 divider 0x1 : M2 divider is functional
15	RESERVED	NONE	0h	Reserved
14	PLL_CORE_CLKCTRL_STOPMODE	R/W	1h	When in Lossclk/Stbyret 0x0 : Limp mode 0x1 : Stopmode
13	RESERVED	NONE	0h	Reserved
12:10	PLL_CORE_CLKCTRL_SELFREQDCO	R/W	4h	DCO Clock [DCOCLK = CLKINP * [M/[N+1]]] frequency range selector. 0x0: Reserved 0x2: HS2 : DCOCLK range is from 500 MHz to 1000MHz 0x3: Reserved 0x4: HS1: DCOCLK range is from 1000MHz to 2000MHz 0x5: Reserved
9	RESERVED	NONE	0h	Reserved
8	PLL_CORE_CLKCTRL_RELAXED_LOCK	R/W	0h	Decides when FREQLOCK asserted 0x0: FREQLOCK asserted when DC frequency error less than 1% 0x1: FREQLOCK asserted when DC frequency error less than 2%
7:2	RESERVED	NONE	0h	Reserved
1	PLL_CORE_CLKCTRL_SSCTYPE	R/W	0h	SSC Type - This should be configured as 1'b0. The module supports spread spectrum clocking [SSC] on its output clocks.
0	PLL_CORE_CLKCTRL_TINTZ	R/W	0h	PLL core soft reset. TINITZ activation [Low] gives softreset to ADPLLLJ. TINITZ does not reset the entire digital control logic; it forces the FSM into RESET State so that ADPLLLJ could restart.

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2.4.2.18 TOP_RCM_PLL_CORE_TENABLE Register

2.4.2.18.1 TOP_RCM_PLL_CORE_TENABLE Register (Offset = 408h) [reset = 0h]

Trigger enable for core PLL.

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Table 2-691. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0408h

Figure 2-344. TOP_RCM_PLL_CORE_TENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PLL_CORE_TENABLE_TENABLE
NONE							R/W
0h							0h

Table 2-692. TOP_RCM_PLL_CORE_TENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PLL_CORE_TENABLE_TENABLE	R/W	0h	Signal TENABLE loads REGM, REGN, REGSD and SELFREQDCO data. M, N. SD and SELFREQDCO latch [active rise edge]

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2.4.2.19 TOP_RCM_PLL_CORE_TENABLEDIV Register

2.4.2.19.1 TOP_RCM_PLL_CORE_TENABLEDIV Register (Offset = 40Ch) [reset = 0h]

Load Trigger for divider control value for Core PLL.

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Table 2-693. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 040Ch

Figure 2-345. TOP_RCM_PLL_CORE_TENABLEDIV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PLL_CORE_TENABLEDIV_TENABLEDIV
NONE							R/W
0h							0h

Table 2-694. TOP_RCM_PLL_CORE_TENABLEDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PLL_CORE_TENABLEDIV_TENABLEDIV	R/W	0h	TENABLEDIV rising edge loads the values of M2REG and N2REG into ADPLLLJ register. TENABLEDIV could be activated anytime when the DPLL digital is in power-up condition. M2 and N2 latch [active rise edge]

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2.4.2.20 TOP_RCM_PLL_CORE_M2NDIV Register

2.4.2.20.1 TOP_RCM_PLL_CORE_M2NDIV Register (Offset = 410h) [reset = 13h]

M2N config register for core PLL.

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Table 2-695. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0410h

Figure 2-346. TOP_RCM_PLL_CORE_M2NDIV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PLL_CORE_M2NDIV_M2						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_CORE_M2NDIV_N							
R/W							
13h							

Table 2-696. TOP_RCM_PLL_CORE_M2NDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	PLL_CORE_M2NDIV_M2	R/W	0h	Post-divider is REGM2
15:8	RESERVED	NONE	0h	Reserved
7:0	PLL_CORE_M2NDIV_N	R/W	13h	Pre-divider is REGN+1

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2.4.2.21 TOP_RCM_PLL_CORE_MN2DIV Register

2.4.2.21.1 TOP_RCM_PLL_CORE_MN2DIV Register (Offset = 414h) [reset = 640h]

MN2 config register for core PLL.

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Table 2-697. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0414h

Figure 2-347. TOP_RCM_PLL_CORE_MN2DIV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PLL_CORE_MN2DIV_N2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PLL_CORE_MN2DIV_M			
NONE				R/W			
0h				640h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_CORE_MN2DIV_M							
R/W							
640h							

Table 2-698. TOP_RCM_PLL_CORE_MN2DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PLL_CORE_MN2DIV_N2	R/W	0h	Bypass divider is REGN2+1
15:12	RESERVED	NONE	0h	Reserved
11:0	PLL_CORE_MN2DIV_M	R/W	640h	Feedback Multiplier is REGM

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2.4.2.22 TOP_RCM_PLL_CORE_FRACDIV Register

2.4.2.22.1 TOP_RCM_PLL_CORE_FRACDIV Register (Offset = 418h) [reset = 8000000h]

Fractionsl divider and Sigma Delta config register for Core PLL.

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Table 2-699. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0418h

Figure 2-348. TOP_RCM_PLL_CORE_FRACDIV Name Register

31	30	29	28	27	26	25	24
PLL_CORE_FRACDIV_REGSD							
R/W							
8h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PLL_CORE_FRACDIV_FRACTIONALM	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_CORE_FRACDIV_FRACTIONALM							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_CORE_FRACDIV_FRACTIONALM							
R/W							
0h							

Table 2-700. TOP_RCM_PLL_CORE_FRACDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PLL_CORE_FRACDIV_REGSD	R/W	8h	Sigma-Delta Divider Should be set by s/w to provide optimum jitter performance. DPLL_SD_DIV = CEILING [[DPLL_MULT/[DPLL_DIV+1]] * CLKINP/250], where CLKINP is the input clock of the DPLL in MHz
23:18	RESERVED	NONE	0h	Reserved
17:0	PLL_CORE_FRACDIV_FRACTIONALM	R/W	0h	Fractional part of the M divider.The 18bit FractionalM value is loaded into DPLL on the rising edge of TENABLE signal .To enable Integer only division FractionalM should be set to 18'b0.

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2.4.2.23 TOP_RCM_PLL_CORE_BWCTRL Register

2.4.2.23.1 TOP_RCM_PLL_CORE_BWCTRL Register (Offset = 41Ch) [reset = 0h]

Loop bandwidth control for Core PLL.

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Table 2-701. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 041Ch

Figure 2-349. TOP_RCM_PLL_CORE_BWCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PLL_CORE_BWCTRL_BWCONTROL		PLL_CORE_BWCTRL_BW_INCR_DECRZ
NONE					R/W		R/W
0h					0h		0h

Table 2-702. TOP_RCM_PLL_CORE_BWCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:1	PLL_CORE_BWCTRL_BWCONTROL	R/W	0h	Change Loop Bandwidth
0	PLL_CORE_BWCTRL_BW_INCR_DECRZ	R/W	0h	Direction of Loop Bandwidth 0x0 : decrease BW 0x1 : increase BW

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2.4.2.24 TOP_RCM_PLL_CORE_FRACCTRL Register

2.4.2.24.1 TOP_RCM_PLL_CORE_FRACCTRL Register (Offset = 420h) [reset = 0h]

Spread Specturm control for Core PLL - Not Supported.

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Table 2-703. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0420h

Figure 2-350. TOP_RCM_PLL_CORE_FRACCTRL Name Register

31	30	29	28	27	26	25	24
PLL_CORE_FRACCTRL_DOWNSPREAD	PLL_CORE_FRACCTRL_MODFREQDIVIDEREXPONENT			PLL_CORE_FRACCTRL_MODFREQDIVIDERMANTISSA			
R/W	R/W			R/W			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PLL_CORE_FRACCTRL_MODFREQDIVIDERMANTISSA			PLL_CORE_FRACCTRL_DELTAMSTEPINTEGER			PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION	
R/W			R/W			R/W	
0h			0h			0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION							
R/W							
0h							

Table 2-704. TOP_RCM_PLL_CORE_FRACCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_CORE_FRACCTRL_DOWNSPREAD	R/W	0h	Controls frequency spread 0x0 : enables both side frequency spread about the programmed frequency. 0x1 : enables low frequency spread only
30:28	PLL_CORE_FRACCTRL_MODFREQDIVIDEREXPONENT	R/W	0h	Exponent of the REFCLK divider to define the modulation frequency.
27:21	PLL_CORE_FRACCTRL_MODFREQDIVIDERMANTISSA	R/W	0h	Mantissa of the REFCLK divider to define the modulation frequency
20:18	PLL_CORE_FRACCTRL_DELTAMSTEPINTEGER	R/W	0h	Integer part of Frequency Spread control
17:0	PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION	R/W	0h	The fraction part of Frequency Spread control

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2.4.2.25 TOP_RCM_PLL_CORE_STATUS Register

2.4.2.25.1 TOP_RCM_PLL_CORE_STATUS Register (Offset = 424h) [reset = E0001141h]

Core PLL status regiser.

Return to Summary Table

Table 2-705. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0424h

Figure 2-351. TOP_RCM_PLL_CORE_STATUS Name Register

31	30	29	28	27	26	25	24
PLL_CORE_STATUS_PONOUT	PLL_CORE_STATUS_PGOODOUT	PLL_CORE_STATUS_LDOPWDN	PLL_CORE_STATUS_RECAL_BSTATUS3	PLL_CORE_STATUS_RECAL_OPPIN	RESERVED		
R	R	R	R	R	NONE		
1h	1h	1h	0h	0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PLL_CORE_STATUS_CLKOUTLDOENACK	PLL_CORE_STATUS_CLKDCOLDOACK	PLL_CORE_STATUS_PHASELOCK	PLL_CORE_STATUS_FREQLOCK	PLL_CORE_STATUS_BYPASSACK
NONE			R	R	R	R	R
0h			1h	0h	0h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_CORE_STATUS_STBYRETACK	PLL_CORE_STATUS_LOSSREF	PLL_CORE_STATUS_CLKOUTENACK	PLL_CORE_STATUS_LOCK2	PLL_CORE_STATUS_M2CHANGEACK	PLL_CORE_STATUS_SSCACK	PLL_CORE_STATUS_HIGHJITTER	PLL_CORE_STATUS_BYPASS
R	R	R	R	R	R	R	R
0h	1h	0h	0h	0h	0h	0h	1h

Table 2-706. TOP_RCM_PLL_CORE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_CORE_STATUS_PONOUT	R	1h	Status of the weak power-switch 0x0 : indicates the/OFF status of the weak power-switch in digital to SOC. 0x1 : ndicates the ON status of the weak power-switch in digital to SOC.
30	PLL_CORE_STATUS_PGOODOUT	R	1h	Status of the strong power-switch 0x0 : indicates the/OFF status of the strong power-switch in digital to SOC. 0x1 : ndicates the ON status of the strong power-switch in digital to SOC.
29	PLL_CORE_STATUS_LDOPWDN	R	1h	1'b1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT will be un-defined in this condition
28	PLL_CORE_STATUS_RECAL_BSTATUS3	R	0h	Recalibration status flag. 1'b1 ADPLLLJ requires recalibration
27	PLL_CORE_STATUS_RECAL_OPPIN	R	0h	Recalibration status flag. 1'b1 ADPLLLJ requires recalibration
26:13	RESERVED	NONE	0h	Reserved

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Table 2-706. TOP_RCM_PLL_CORE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PLL_CORE_STATUS_CLKOUTLDOENACK	R	1h	Indicates the enable/disable condition of CLKOUTLDOEN 0x0 = CLKOUTLDO gating completed 0x1 = CLKOUTLDO enabling completed
11	PLL_CORE_STATUS_CLKDCOLDOACK	R	0h	Indicates the enable/disable condition of CLKDCOLDOEN 0x0 = CLKDCOLDO gating completed 0x1 = CLKDCOLOD enabling completed
10	PLL_CORE_STATUS_PHASELOCK	R	0h	Status on PHASELOCK output pin
9	PLL_CORE_STATUS_FREQLOCK	R	0h	Status on FREQLOCK output pin
8	PLL_CORE_STATUS_BYPASSACK	R	1h	Status of BYPASSACK output pin
7	PLL_CORE_STATUS_STBYRETACK	R	0h	Standby and retention status 0x0: indicates to SOC that all internal clocks in ADPLLLJ are active and it is starting the relock process. 0x1: indicates to SOC that all internal clocks in ADPLLLJ are gated and it is ready for retention.
6	PLL_CORE_STATUS_LOSSREF	R	1h	Reference input loss is indicated by 1'b0.
5	PLL_CORE_STATUS_CLKOUTENACK	R	0h	Indicates the enable/disable condition of CLKOUTEN 0x0 = CLKOUT gating completed 0x1 = CLKOUT enabling completed
4	PLL_CORE_STATUS_LOCK2	R	0h	ADPLL internal loop lock status
3	PLL_CORE_STATUS_M2CHANGEACK	R	0h	Acknowledge for change to M2 divider. Toggles from 1-0 or 0-1 [depending on current value] once CLKOUT frequency change has completed.
2	PLL_CORE_STATUS_SSCACK	R	0h	Spread Spectrum status 0x0 : Spread-spectrum Clocking is disabled on output clocks 0x1 : Spread-spectrum Clocking is enabled on output clocks
1	PLL_CORE_STATUS_HIGHJITTER	R	0h	1'b1 indicates jitter. After PHASELOCK is asserted high, the HIGHJITTER flag is asserted high if phase error between REFCLK and FBCLK greater than 24%.
0	PLL_CORE_STATUS_BYPASS	R	1h	Bypass status signal. 1 CLKOUT in bypass

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2.4.2.26 TOP_RCM_PLL_CORE_HSDIVIDER Register

2.4.2.26.1 TOP_RCM_PLL_CORE_HSDIVIDER Register (Offset = 428h) [reset = 0h]

Core PLL high speed divider config.

Return to Summary Table

Table 2-707. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0428h

Figure 2-352. TOP_RCM_PLL_CORE_HSDIVIDER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PLL_CORE_HSDIVIDER_LDOPWDNACK	PLL_CORE_HSDIVIDER_BYPASSACKZ
NONE						R	R
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PLL_CORE_HSDIVIDER_TENABLEDIV	PLL_CORE_HSDIVIDER_LDOPWDN	PLL_CORE_HSDIVIDER_BYPASS
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-708. TOP_RCM_PLL_CORE_HSDIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	PLL_CORE_HSDIVIDER_LDOPWDNACK	R	0h	LDO Power Down Ack
16	PLL_CORE_HSDIVIDER_BYPASSACKZ	R	0h	HSDIVIDER Bypass Ack
15:3	RESERVED	NONE	0h	Reserved
2	PLL_CORE_HSDIVIDER_TENABLEDIV	R/W	0h	TENABLEDIV rising edge loads the values of M2REG and N2REG into ADPLLLJ register. TENABLEDIV could be activated anytime when the DPLL digital is in power-up condition. M2 and N2 latch [active rise edge]
1	PLL_CORE_HSDIVIDER_LDOPWDN	R/W	0h	1'b1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT will be un-defined in this condition
0	PLL_CORE_HSDIVIDER_BYPASS	R/W	0h	HSDIVIDER Bypass. Set it to 1'b1 to bypass the HSDIVIDER.

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2.4.2.27 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT0 Register

2.4.2.27.1 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT0 Register (Offset = 42Ch) [reset = 4h]

Core PLL high speed divider clock 0 control.

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Table 2-709. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 042Ch

Figure 2-353. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PLL_CORE_HSDIVIDER_CLKOUT0_PWDN	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT0_STATUS	PLL_CORE_HSDIVIDER_CLKOUT0_GATE_CTRL
NONE			R/W	NONE		R	R/W
0h			0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PLL_CORE_HSDIVIDER_CLKOUT0_DIVCHACK	PLL_CORE_HSDIVIDER_CLKOUT0_DIV				
NONE		R	R/W				
0h		0h	4h				

Table 2-710. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	PLL_CORE_HSDIVIDER_CLKOUT0_PWDN	R/W	0h	Power down for HSDIVIDER CLKOUT0 divider and hence CLKOUT0 output 0h[R/W] = CLKOUT0 divider active 1h[R/W] = CLKOUT0 divider is powered down
11:10	RESERVED	NONE	0h	Reserved
9	PLL_CORE_HSDIVIDER_CLKOUT0_STATUS	R	0h	HSDIVIDER CLKOUT0 status 0h[R] = The clock output is gated 1h[R] = The clock output is enabled
8	PLL_CORE_HSDIVIDER_CLKOUT0_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT0 0h[R/W] = Automatically gate this clock when there is no dependency for it 1h[R/W] = Force this clock to stay enabled even if there is no request
7:6	RESERVED	NONE	0h	Reserved
5	PLL_CORE_HSDIVIDER_CLKOUT0_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT0_DIV indicates that the change in divider value has taken effect

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Table 2-710. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	PLL_CORE_HSDIVIDER_CLKOUT0_DIV	R/W	4h	DPLL post-divider factor, HSDIVIDER CLKOUT0, for internal clock generation. Divide values from 1 to 31. 0h[R/W] = Reserved

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2.4.2.28 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT1 Register

2.4.2.28.1 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT1 Register (Offset = 430h) [reset = 3h]

Core PLL high speed divider clock 1 control.

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Table 2-711. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0430h

Figure 2-354. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PLL_CORE_HSDIVIDER_CLKOUT1_PWDN	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT1_STATUS	PLL_CORE_HSDIVIDER_CLKOUT1_GATE_CTRL
NONE			R/W	NONE		R	R/W
0h			0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PLL_CORE_HSDIVIDER_CLKOUT1_DIVCHACK	PLL_CORE_HSDIVIDER_CLKOUT1_DIV				
NONE		R	R/W				
0h		0h	3h				

Table 2-712. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	PLL_CORE_HSDIVIDER_CLKOUT1_PWDN	R/W	0h	Power down for HSDIVIDER CLKOUT1 divider and hence CLKOUT1 output 0h[R/W] = CLKOUT1 divider active 1h[R/W] = CLKOUT1 divider is powered down
11:10	RESERVED	NONE	0h	Reserved
9	PLL_CORE_HSDIVIDER_CLKOUT1_STATUS	R	0h	HSDIVIDER CLKOUT1 status 0h[R] = The clock output is gated 1h[R] = The clock output is enabled
8	PLL_CORE_HSDIVIDER_CLKOUT1_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT1 0h[R/W] = Automatically gate this clock when there is no dependency for it 1h[R/W] = Force this clock to stay enabled even if there is no request
7:6	RESERVED	NONE	0h	Reserved
5	PLL_CORE_HSDIVIDER_CLKOUT1_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect

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Table 2-712. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	PLL_CORE_HSDIVIDER_CLKOUT1_DIV	R/W	3h	DPLL post-divider factor, HSDIVIDER CLKOUT1, for internal clock generation. Divide values from 1 to 31. 0h[R/W] = Reserved

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2.4.2.29 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT2 Register

2.4.2.29.1 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT2 Register (Offset = 434h) [reset = 4h]

Core PLL high speed divider clock 2 control.

Return to Summary Table

Table 2-713. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0434h

Figure 2-355. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PLL_CORE_HSDIVIDER_CLKOUT2_PWDN	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT2_STATUS	PLL_CORE_HSDIVIDER_CLKOUT2_GATE_CTRL
NONE			R/W	NONE		R	R/W
0h			0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PLL_CORE_HSDIVIDER_CLKOUT2_DIVCHACK	PLL_CORE_HSDIVIDER_CLKOUT2_DIV				
NONE		R	R/W				
0h		0h	4h				

Table 2-714. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	PLL_CORE_HSDIVIDER_CLKOUT2_PWDN	R/W	0h	Power down for HSDIVIDER CLKOUT2 divider and hence CLKOUT2 output 0h[R/W] = CLKOUT2 divider active 1h[R/W] = CLKOUT2 divider is powered down
11:10	RESERVED	NONE	0h	Reserved
9	PLL_CORE_HSDIVIDER_CLKOUT2_STATUS	R	0h	HSDIVIDER CLKOUT2 status 0h[R] = The clock output is gated 1h[R] = The clock output is enabled
8	PLL_CORE_HSDIVIDER_CLKOUT2_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT2 0h[R/W] = Automatically gate this clock when there is no dependency for it 1h[R/W] = Force this clock to stay enabled even if there is no request
7:6	RESERVED	NONE	0h	Reserved
5	PLL_CORE_HSDIVIDER_CLKOUT2_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect

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Table 2-714. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	PLL_CORE_HSDIVIDER_CLKOUT2_DIV	R/W	4h	DPLL post-divider factor, HSDIVIDER CLKOUT2, for internal clock generation. Divide values from 1 to 31. 0h[R/W] = Reserved

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2.4.2.30 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT3 Register

2.4.2.30.1 TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT3 Register (Offset = 438h) [reset = 9h]

Core PLL high speed divider clock 3 control.

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Table 2-715. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0438h

Figure 2-356. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			PLL_CORE_HSDIVIDER_CLKOUT3_PWDN	RESERVED		PLL_CORE_HSDIVIDER_CLKOUT3_STATUS	PLL_CORE_HSDIVIDER_CLKOUT3_GATE_CTRL
NONE			R/W	NONE		R	R/W
0h			0h	0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED		PLL_CORE_HSDIVIDER_CLKOUT3_DIVCHACK	PLL_CORE_HSDIVIDER_CLKOUT3_DIV				
NONE		R	R/W				
0h		0h	9h				

Table 2-716. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	PLL_CORE_HSDIVIDER_CLKOUT3_PWDN	R/W	0h	Power down for HSDIVIDER CLKOUT3 divider and hence CLKOUT3 output 0h[R/W] = CLKOUT3 divider active 1h[R/W] = CLKOUT3 divider is powered down
11:10	RESERVED	NONE	0h	Reserved
9	PLL_CORE_HSDIVIDER_CLKOUT3_STATUS	R	0h	HSDIVIDER CLKOUT3 status 0h[R] = The clock output is gated 1h[R] = The clock output is enabled
8	PLL_CORE_HSDIVIDER_CLKOUT3_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT3 0h[R/W] = Automatically gate this clock when there is no dependency for it 1h[R/W] = Force this clock to stay enabled even if there is no request
7:6	RESERVED	NONE	0h	Reserved
5	PLL_CORE_HSDIVIDER_CLKOUT3_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT3_DIV indicates that the change in divider value has taken effect

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Table 2-716. TOP_RCM_PLL_CORE_HSDIVIDER_CLKOUT3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	PLL_CORE_HSDIVIDER_ CLKOUT3_DIV	R/W	9h	DPLL post-divider factor, HSDIVIDER CLKOUT3, for internal clock generation. Divide values from 1 to 31. 0h[R/W] = Reserved

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2.4.2.31 TOP_RCM_PLL_CORE_RSTCTRL Register

2.4.2.31.1 TOP_RCM_PLL_CORE_RSTCTRL Register (Offset = 43Ch) [reset = 0h]

Core PLL reset control.

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Table 2-717. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 043Ch

Figure 2-357. TOP_RCM_PLL_CORE_RSTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PLL_CORE_RSTCTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-718. TOP_RCM_PLL_CORE_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PLL_CORE_RSTCTRL_ASSERT	R/W	0h	SW Reset override for the PLL Write 3'b111 : Override is enabled and Reset is asserted

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2.4.2.32 TOP_RCM_PLL_CORE_HSDIVIDER_RSTCTRL Register

2.4.2.32.1 TOP_RCM_PLL_CORE_HSDIVIDER_RSTCTRL Register (Offset = 440h) [reset = 0h]

Core PLL high speed divider reset control.

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Table 2-719. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0440h

Figure 2-358. TOP_RCM_PLL_CORE_HSDIVIDER_RSTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PLL_CORE_HSDIVIDER_RSTCTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-720. TOP_RCM_PLL_CORE_HSDIVIDER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PLL_CORE_HSDIVIDER_RSTCTRL_ASSERT	R/W	0h	SW Reset override for the HSDIVIDER Write 3'b111 : Override is enabled and Reset is asserted

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2.4.2.33 TOP_RCM_R5SS_CLK_SRC_SEL Register

2.4.2.33.1 TOP_RCM_R5SS_CLK_SRC_SEL Register (Offset = 500h) [reset = 0h]

Clock Source select register for MSS CortexR5 clock.

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Table 2-721. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0500h

Figure 2-359. TOP_RCM_R5SS_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				R5SS_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
R5SS_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-722. TOP_RCM_R5SS_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	R5SS_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for MSS Coretex R5 and System bus Clock. Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - DPLL_CORE_HSDIV0_CLKOUT0 0x333 - RCCLK10M 0x444 - RCCLK10M 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.4.2.34 TOP_RCM_R5SS_CLK_STATUS Register

2.4.2.34.1 TOP_RCM_R5SS_CLK_STATUS Register (Offset = 504h) [reset = 1h]

Clock Status register for MSS Root clock for CortexR5 and SYS clock.

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Table 2-723. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0504h

Figure 2-360. TOP_RCM_R5SS_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
R5SS_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-724. TOP_RCM_R5SS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	R5SS_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Root clock for CortexR5 and Sysclk

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2.4.2.35 TOP_RCM_R5SS0_CLK_DIV_SEL Register

2.4.2.35.1 TOP_RCM_R5SS0_CLK_DIV_SEL Register (Offset = 510h) [reset = 0h]

Clock Divider register for Respective R5SS clock .

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Table 2-725. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0510h

Figure 2-361. TOP_RCM_R5SS0_CLK_DIV_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CLK_DIV_SEL_CLKSRCSEL		
NONE					R/W		
0h					0h		

Table 2-726. TOP_RCM_R5SS0_CLK_DIV_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CLK_DIV_SEL_CLKSRCSEL	R/W	0h	Writing 3'b000 Sets R5 clock = R5SS Root clock Writing 3'b111 Sets R5 Clock = SYSCLK

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2.4.2.36 TOP_RCM_R5SS1_CLK_DIV_SEL Register

2.4.2.36.1 TOP_RCM_R5SS1_CLK_DIV_SEL Register (Offset = 514h) [reset = 0h]

Clock Divider register for Respective R5SS clock .

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Table 2-727. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0514h

Figure 2-362. TOP_RCM_R5SS1_CLK_DIV_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS1_CLK_DIV_SEL_CLKSRCSEL		
NONE					R/W		
0h					0h		

Table 2-728. TOP_RCM_R5SS1_CLK_DIV_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CLK_DIV_SEL_CLKSRCSEL	R/W	0h	Writing 3'b000 Sets R5 clock = R5SS Root clock Writing 3'b111 Sets R5 Clock = SYSCLK

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2.4.2.37 TOP_RCM_R5SS0_CLK_GATE Register

2.4.2.37.1 TOP_RCM_R5SS0_CLK_GATE Register (Offset = 518h) [reset = 0h]

Clock Gating register for Respective R5SS clock.

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Table 2-729. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0518h

Figure 2-363. TOP_RCM_R5SS0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-730. TOP_RCM_R5SS0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CLK_GATE_GATED	R/W	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS Coretex R5. Data should be loaded as multibit. Write 3'b000 : Clock is ungated [multibit 000] Write 3'b111 : Clock is gated [multibit 111]

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2.4.2.38 TOP_RCM_R5SS1_CLK_GATE Register

2.4.2.38.1 TOP_RCM_R5SS1_CLK_GATE Register (Offset = 51Ch) [reset = 0h]

Clock Gating register for Respective R5SS clock.

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Table 2-731. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 051Ch

Figure 2-364. TOP_RCM_R5SS1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-732. TOP_RCM_R5SS1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CLK_GATE_GATED	R/W	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS Coretex R5. Data should be loaded as multibit. Write 3'b000 : Clock is ungated [multibit 000] Write 3'b111 : Clock is gated [multibit 111]

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2.4.2.39 TOP_RCM_SYS_CLK_DIV_VAL Register

2.4.2.39.1 TOP_RCM_SYS_CLK_DIV_VAL Register (Offset = 520h) [reset = 0h]

Clock Divider register for System Clock.

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Table 2-733. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0520h

Figure 2-365. TOP_RCM_SYS_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				SYS_CLK_DIV_VAL_CLKDIV			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
SYS_CLK_DIV_VAL_CLKDIV							
R/W							
0h							

Table 2-734. TOP_RCM_SYS_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	SYS_CLK_DIV_VAL_CLKDIV	R/W	0h	Divider value for CLKOUT selected clock..To set the divider value of [n+1] configure the register to '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.4.2.40 TOP_RCM_SYS_CLK_GATE Register

2.4.2.40.1 TOP_RCM_SYS_CLK_GATE Register (Offset = 524h) [reset = 0h]

Clock Gating register for System Clock.

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Table 2-735. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0524h

Figure 2-366. TOP_RCM_SYS_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					SYS_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-736. TOP_RCM_SYS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	SYS_CLK_GATE_GATED	R/W	0h	Only for debug- Functionality not guaranteed Clock gating config for System Clock Data should be loaded as multibit. Write 3'b000 : Clock is ungated [multibit 000] Write 3'b111 : Clock is gated [multibit 111]

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2.4.2.41 TOP_RCM_SYS_CLK_STATUS Register

2.4.2.41.1 TOP_RCM_SYS_CLK_STATUS Register (Offset = 528h) [reset = 0h]

Clock Status register for System Clock.

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Table 2-737. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0528h

Figure 2-367. TOP_RCM_SYS_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SYS_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 2-738. TOP_RCM_SYS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	SYS_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Sys Clock
7:0	RESERVED	NONE	0h	Reserved

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2.4.2.42 TOP_RCM_PLL_PER_PWRCTRL Register

2.4.2.42.1 TOP_RCM_PLL_PER_PWRCTRL Register (Offset = 800h) [reset = 30h]

Power control for peripheral PLL.

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Table 2-739. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0800h

Figure 2-368. TOP_RCM_PLL_PER_PWRCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PLL_PER_PWRCTRL_PONIN	PLL_PER_PWRCTRL_PGOODIN	PLL_PER_PWRCTRL_RET	PLL_PER_PWRCTRL_ISORET	PLL_PER_PWRCTRL_ISOSCAN	PLL_PER_PWRCTRL_OFFMODE
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		1h	1h	0h	0h	0h	0h

Table 2-740. TOP_RCM_PLL_PER_PWRCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	PLL_PER_PWRCTRL_PONIN	R/W	1h	ON/OFF control of the weak power switch digital. For functional mode it should be 1
4	PLL_PER_PWRCTRL_PGOODIN	R/W	1h	ON/OFF control of the strong power switch digital. For functional mode it should be 1
3	PLL_PER_PWRCTRL_RET	R/W	0h	Save/Restore control for Retention mode. For functional mode it should be 0
2	PLL_PER_PWRCTRL_ISORET	R/W	0h	Save/Restore control for Isolation of output pins For functional mode it should be 1'b0
1	PLL_PER_PWRCTRL_ISOSCAN	R/W	0h	Save/Restore control for Isolation of the Scanout pins. For functional mode it should be 1'b0
0	PLL_PER_PWRCTRL_OFFMODE	R/W	0h	Used to switch OFF the logic on VDDA. For functional mode it should be 0

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2.4.2.43 TOP_RCM_PLL_PER_CLKCTRL Register

2.4.2.43.1 TOP_RCM_PLL_PER_CLKCTRL Register (Offset = 804h) [reset = 895000h]

Clock control for Peripheral PLL.

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Table 2-741. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0804h

Figure 2-369. TOP_RCM_PLL_PER_CLKCTRL Name Register

31	30	29	28	27	26	25	24
PLL_PER_CLKCTRL_CYCLESLIPEN	PLL_PER_CLKCTRL_ENSSC	PLL_PER_CLKCTRL_CLKDCOLDOEN	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PLL_PER_CLKCTRL_IDLE	PLL_PER_CLKCTRL_BYPASSACKZ	PLL_PER_CLKCTRL_STBYRET	PLL_PER_CLKCTRL_CLKOUTEN	PLL_PER_CLKCTRL_CLKOUTLDOEN	PLL_PER_CLKCTRL_ULOWCLKEN	PLL_PER_CLKCTRL_CLKDCOLDOPWDNZ	PLL_PER_CLKCTRL_M2PWDNZ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	1h	0h	0h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PLL_PER_CLKCTRL_STOPMODE	RESERVED	PLL_PER_CLKCTRL_SELFREQDCO			RESERVED	PLL_PER_CLKCTRL_RELAXED_LOCK
NONE	R/W	NONE	R/W			NONE	R/W
0h	1h	0h	4h			0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						PLL_PER_CLKCTRL_SSCTYPE	PLL_PER_CLKCTRL_TINTZ
NONE						R/W	R/W
0h						0h	0h

Table 2-742. TOP_RCM_PLL_PER_CLKCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_PER_CLKCTRL_CYCLESLIPEN	R/W	0h	FailSafe enable to trigger re-calibration in case CycleSlip occurs between REFCLK and FBCLK. Cycleslip could be caused if loop is not able to track input clock. Default = 1'b0 recommended
30	PLL_PER_CLKCTRL_ENSSC	R/W	0h	Controls Clock SpReading. SSC is not supported. Should be set to 0x0 to disable clock spReading.
29	PLL_PER_CLKCTRL_CLKDCOLDOEN	R/W	0h	Synchronously enables/disables CLKDCOLDO 0x0 : synchronously disables CLKDCOLDO 0x1 : synchronously enables CLKDCOLDO
28:24	RESERVED	NONE	0h	Reserved
23	PLL_PER_CLKCTRL_IDLE	R/W	1h	Sets PLL to Idle mode 0x0 : When SYSRESET = 0 and TINITZ = 1 IDLE = 0 PLL will go to Active and Locked 0x1 : When SYSRESET = 0 and TINITZ = 1 IDLE = 1 PLL will go to Idle Bypass low powe

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Table 2-742. TOP_RCM_PLL_PER_CLKCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	PLL_PER_CLKCTRL_BYPASSACKZ	R/W	0h	BYPASSACKZ is a special purpose input to the module. In general this input is expected to be tied to static low. For the output clocks of the module that do not have an internal bypass mux viz. CLKDCOLDO and CLKOUTLDO, a bypass mux could be implemented external to the module.
21	PLL_PER_CLKCTRL_STBYRET	R/W	0h	Standby retention control 0x0 : prepares ADPLLLJ for relock when out of retention by removing the gating on all internal clocks. 0x1 : prepares ADPLLLJ for retention by gating all the internal clocks.
20	PLL_PER_CLKCTRL_CLKOUTEN	R/W	0h	CLKOUT enable or disable 0x0 : synchronously disables CLKOUT 0x1 : synchronously enables CLKOUT
19	PLL_PER_CLKCTRL_CLKOUTLDOEN	R/W	1h	Synchronously enables/disables CLKOUTLDO 0x0 : synchronously disables CLKOUTLDO 0x1 : synchronously enables CLKOUTLDO
18	PLL_PER_CLKCTRL_ULOWCLKEN	R/W	0h	Select CLKOUT source in bypass 0x0: When ADPLLLJ in bypass mode, CLKOUT = CLKINP/[N2+1] 0x1: When ADPLLLJ in bypass mode, CLKOUT = CLKINPULOW.
17	PLL_PER_CLKCTRL_CLKDCOLDOPWDNZ	R/W	0h	0 Asynchronous power down for CLKDCOLDO o/p.
16	PLL_PER_CLKCTRL_M2PWDNZ	R/W	1h	M2 divider power down mode 0x0: Asynchronous power down for M2 divider 0x1 : M2 divider is functional
15	RESERVED	NONE	0h	Reserved
14	PLL_PER_CLKCTRL_STOPMODE	R/W	1h	When in Lossclk/Stbyret 0x0 : Limp mode 0x1 : Stopmode
13	RESERVED	NONE	0h	Reserved
12:10	PLL_PER_CLKCTRL_SELFREQDCO	R/W	4h	DCO Clock [DCOCLK = CLKINP * [M/[N+1]]] frequency range selector. 0x0: Reserved 0x2: HS2 : DCOCLK range is from 500 MHz to 1000MHz 0x3: Reserved 0x4: HS1: DCOCLK range is from 1000MHz to 2000MHz 0x5: Reserved
9	RESERVED	NONE	0h	Reserved
8	PLL_PER_CLKCTRL_RELAXED_LOCK	R/W	0h	Decides when FREQLOCK asserted 0x0: FREQLOCK asserted when DC frequency error less than 1% 0x1: FREQLOCK asserted when DC frequency error less than 2%
7:2	RESERVED	NONE	0h	Reserved
1	PLL_PER_CLKCTRL_SSCTYPE	R/W	0h	SSC Type - This should be configured as 1'b0. The module supports spread spectrum clocking [SSC] on its output clocks.
0	PLL_PER_CLKCTRL_TINTZ	R/W	0h	PLL core soft reset. TINITZ activation [Low] gives softreset to ADPLLLJ. TINITZ does not reset the entire digital control logic; it forces the FSM into RESET State so that ADPLLLJ could restart.

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2.4.2.44 TOP_RCM_PLL_PER_TENABLE Register

2.4.2.44.1 TOP_RCM_PLL_PER_TENABLE Register (Offset = 808h) [reset = 0h]

Trigger enable for Peripheral PLL.

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Table 2-743. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0808h

Figure 2-370. TOP_RCM_PLL_PER_TENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PLL_PER_TENABLE_TENABLE
NONE							R/W
0h							0h

Table 2-744. TOP_RCM_PLL_PER_TENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PLL_PER_TENABLE_TENABLE	R/W	0h	Signal TENABLE loads REGM, REGN, REGSD and SELFREQDCO data. M, N. SD and SELFREQDCO latch [active rise edge]

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2.4.2.45 TOP_RCM_PLL_PER_TENABLEDIV Register

2.4.2.45.1 TOP_RCM_PLL_PER_TENABLEDIV Register (Offset = 80Ch) [reset = 0h]

Load Trigger for divider control value for peripheral PLL.

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Table 2-745. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 080Ch

Figure 2-371. TOP_RCM_PLL_PER_TENABLEDIV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PLL_PER_TENABLEDIV_TENABLEDIV
NONE							R/W
0h							0h

Table 2-746. TOP_RCM_PLL_PER_TENABLEDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PLL_PER_TENABLEDIV_TENABLEDIV	R/W	0h	TENABLEDIV rising edge loads the values of M2REG and N2REG into ADPLLLJ register. TENABLEDIV could be activated anytime when the DPLL digital is in power-up condition. M2 and N2 latch [active rise edge]

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2.4.2.46 TOP_RCM_PLL_PER_M2NDIV Register

2.4.2.46.1 TOP_RCM_PLL_PER_M2NDIV Register (Offset = 810h) [reset = 13h]

M2N config register for peripheral PLL.

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Table 2-747. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0810h

Figure 2-372. TOP_RCM_PLL_PER_M2NDIV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PLL_PER_M2NDIV_M2						
NONE	R/W						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PLL_PER_M2NDIV_N							
R/W							
13h							

Table 2-748. TOP_RCM_PLL_PER_M2NDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:16	PLL_PER_M2NDIV_M2	R/W	0h	Post-divider is REGM2
15:8	RESERVED	NONE	0h	Reserved
7:0	PLL_PER_M2NDIV_N	R/W	13h	Pre-divider is REGN+1

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2.4.2.47 TOP_RCM_PLL_PER_MN2DIV Register

2.4.2.47.1 TOP_RCM_PLL_PER_MN2DIV Register (Offset = 814h) [reset = 600h]

MN2 config register for peripheral PLL.

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Table 2-749. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0814h

Figure 2-373. TOP_RCM_PLL_PER_MN2DIV Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PLL_PER_MN2DIV_N2			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				PLL_PER_MN2DIV_M			
NONE				R/W			
0h				600h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_PER_MN2DIV_M							
R/W							
600h							

Table 2-750. TOP_RCM_PLL_PER_MN2DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:16	PLL_PER_MN2DIV_N2	R/W	0h	Bypass divider is REGN2+1
15:12	RESERVED	NONE	0h	Reserved
11:0	PLL_PER_MN2DIV_M	R/W	600h	Feedback Multiplier is REGM

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2.4.2.48 TOP_RCM_PLL_PER_FRACDIV Register

2.4.2.48.1 TOP_RCM_PLL_PER_FRACDIV Register (Offset = 818h) [reset = 8000000h]

Fractionsl divider and Sigma Delta config register for peripheral PLL.

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Table 2-751. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0818h

Figure 2-374. TOP_RCM_PLL_PER_FRACDIV Name Register

31	30	29	28	27	26	25	24
PLL_PER_FRACDIV_REGSD							
R/W							
8h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						PLL_PER_FRACDIV_FRACTIONALM	
NONE						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_PER_FRACDIV_FRACTIONALM							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_PER_FRACDIV_FRACTIONALM							
R/W							
0h							

Table 2-752. TOP_RCM_PLL_PER_FRACDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PLL_PER_FRACDIV_REGSD	R/W	8h	Sigma-Delta Divider Should be set by s/w to provide optimum jitter performance. DPLL_SD_DIV = CEILING [[DPLL_MULT/[DPLL_DIV+1]] * CLKINP/250], where CLKINP is the input clock of the DPLL in MHz
23:18	RESERVED	NONE	0h	Reserved
17:0	PLL_PER_FRACDIV_FRACTIONALM	R/W	0h	Fractional part of the M divider.The 18bit FractionalM value is loaded into DPLL on the rising edge of TENABLE signal .To enable Integer only division FractionalM should be set to 18'b0.

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2.4.2.49 TOP_RCM_PLL_PER_BWCTRL Register

2.4.2.49.1 TOP_RCM_PLL_PER_BWCTRL Register (Offset = 81Ch) [reset = 0h]

Loop bandwidth control for peripheral PLL.

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Table 2-753. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 081Ch

Figure 2-375. TOP_RCM_PLL_PER_BWCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PLL_PER_BWCTRL_BWCONTROL		PLL_PER_BWCTRL_BW_INCR_DECRZ
NONE					R/W		R/W
0h					0h		0h

Table 2-754. TOP_RCM_PLL_PER_BWCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:1	PLL_PER_BWCTRL_BWCONTROL	R/W	0h	Change Loop Bandwidth
0	PLL_PER_BWCTRL_BW_INCR_DECRZ	R/W	0h	Direction of Loop Bandwidth 0x0 : decrease BW 0x1 : increase BW

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2.4.2.50 TOP_RCM_PLL_PER_FRACCTRL Register

2.4.2.50.1 TOP_RCM_PLL_PER_FRACCTRL Register (Offset = 820h) [reset = 0h]

Spread Specturm control for peripheral PLL - Not Supported.

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Table 2-755. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0820h

Figure 2-376. TOP_RCM_PLL_PER_FRACCTRL Name Register

31	30	29	28	27	26	25	24
PLL_PER_FRACCTRL_DOWNSPREAD	PLL_PER_FRACCTRL_MODFREQDIVIDEREXPONENT			PLL_PER_FRACCTRL_MODFREQDIVIDERMANTISSA			
R/W	R/W			R/W			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PLL_PER_FRACCTRL_MODFREQDIVIDERMANTISSA			PLL_PER_FRACCTRL_DELTAMSTEPINTEGER			PLL_PER_FRACCTRL_DELTAMSTEPFRACTION	
R/W			R/W			R/W	
0h			0h			0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_PER_FRACCTRL_DELTAMSTEPFRACTION							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_PER_FRACCTRL_DELTAMSTEPFRACTION							
R/W							
0h							

Table 2-756. TOP_RCM_PLL_PER_FRACCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_PER_FRACCTRL_DOWNSPREAD	R/W	0h	Controls frequency spread 0x0 : enables both side frequency spread about the programmed frequency. 0x1 : enables low frequency spread only
30:28	PLL_PER_FRACCTRL_MODFREQDIVIDEREXPONENT	R/W	0h	Exponent of the REFCLK divider to define the modulation frequency.
27:21	PLL_PER_FRACCTRL_MODFREQDIVIDERMANTISSA	R/W	0h	Mantissa of the REFCLK divider to define the modulation frequency
20:18	PLL_PER_FRACCTRL_DELTAMSTEPINTEGER	R/W	0h	Integer part of Frequency Spread control
17:0	PLL_PER_FRACCTRL_DELTAMSTEPFRACTION	R/W	0h	The fraction part of Frequency Spread control

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2.4.2.51 TOP_RCM_PLL_PER_STATUS Register

2.4.2.51.1 TOP_RCM_PLL_PER_STATUS Register (Offset = 824h) [reset = E0001141h]

Peripheral PLL status regiser.

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Table 2-757. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0824h

Figure 2-377. TOP_RCM_PLL_PER_STATUS Name Register

31	30	29	28	27	26	25	24
PLL_PER_STATUS_PONOUT	PLL_PER_STATUS_PGOODOUT	PLL_PER_STATUS_LDOPWDN	PLL_PER_STATUS_RECAL_BSTATUS3	PLL_PER_STATUS_RECAL_OPPIN	RESERVED		
R	R	R	R	R	NONE		
1h	1h	1h	0h	0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PLL_PER_STATUS_CLKOUTLDOENACK	PLL_PER_STATUS_CLKDCOLDOACK	PLL_PER_STATUS_PHASELOCK	PLL_PER_STATUS_FREQLOCK	PLL_PER_STATUS_BYPASSACK
NONE			R	R	R	R	R
0h			1h	0h	0h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLL_PER_STATUS_STBYRETACK	PLL_PER_STATUS_LOSSREF	PLL_PER_STATUS_CLKOUTENACK	PLL_PER_STATUS_LOCK2	PLL_PER_STATUS_M2CHANGEACK	PLL_PER_STATUS_SSCACK	PLL_PER_STATUS_HIGHJITTER	PLL_PER_STATUS_BYPASS
R	R	R	R	R	R	R	R
0h	1h	0h	0h	0h	0h	0h	1h

Table 2-758. TOP_RCM_PLL_PER_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PLL_PER_STATUS_PONOUT	R	1h	Status of the weak power-switch 0x0 : indicates the/OFF status of the weak power-switch in digital to SOC. 0x1 : ndicates the ON status of the weak power-switch in digital to SOC.
30	PLL_PER_STATUS_PGOODOUT	R	1h	Status of the strong power-switch 0x0 : indicates the/OFF status of the strong power-switch in digital to SOC. 0x1 : ndicates the ON status of the strong power-switch in digital to SOC.
29	PLL_PER_STATUS_LDOPWDN	R	1h	1'b1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT will be un-defined in this condition
28	PLL_PER_STATUS_RECAL_BSTATUS3	R	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration
27	PLL_PER_STATUS_RECAL_OPPIN	R	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration
26:13	RESERVED	NONE	0h	Reserved

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Table 2-758. TOP_RCM_PLL_PER_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PLL_PER_STATUS_CLKOUTLDOENACK	R	1h	Indicates the enable/disable condition of CLKOUTLDOEN 0x0 = CLKOUTLDO gating completed 0x1 = CLKOUTLDO enabling completed
11	PLL_PER_STATUS_CLKDCOLDOACK	R	0h	Indicates the enable/disable condition of CLKDCOLDOEN 0x0 = CLKDCOLDO gating completed 0x1 = CLKDCOLDO enabling completed
10	PLL_PER_STATUS_PHASELOCK	R	0h	Status on PHASELOCK output pin
9	PLL_PER_STATUS_FREQLOCK	R	0h	Status on FREQLOCK output pin
8	PLL_PER_STATUS_BYPASSACK	R	1h	Status of BYPASSACK output pin
7	PLL_PER_STATUS_STBYRETACK	R	0h	Standby and retention status 0x0: indicates to SOC that all internal clocks in ADPLLLJ are active and it is starting the relock process. 0x1: indicates to SOC that all internal clocks in ADPLLLJ are gated and it is ready for retention.
6	PLL_PER_STATUS_LOSSREF	R	1h	Reference input loss is indicated by 1'b0.
5	PLL_PER_STATUS_CLKOUTENACK	R	0h	Indicates the enable/disable condition of CLKOUTEN 0x0 = CLKOUT gating completed 0x1 = CLKOUT enabling completed
4	PLL_PER_STATUS_LOCK2	R	0h	ADPLL internal loop lock status
3	PLL_PER_STATUS_M2CHANGEACK	R	0h	Acknowledge for change to M2 divider. Toggles from 1-0 or 0-1 [depending on current value] once CLKOUT frequency change has completed.
2	PLL_PER_STATUS_SSCACK	R	0h	Spread Spectrum status 0x0 : Spread-spectrum Clocking is disabled on output clocks 0x1 : Spread-spectrum Clocking is enabled on output clocks
1	PLL_PER_STATUS_HIGHJITTER	R	0h	1'b1 indicates jitter. After PHASELOCK is asserted high, the HIGHJITTER flag is asserted high if phase error between REFCLK and FBCLK greater than 24%.
0	PLL_PER_STATUS_BYPASS	R	1h	Bypass status signal. 1 CLKOUT in bypass

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2.4.2.52 TOP_RCM_PLL_PER_HSDIVIDER Register

2.4.2.52.1 TOP_RCM_PLL_PER_HSDIVIDER Register (Offset = 828h) [reset = 0h]

Peripheral PLL high speed divider config.

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Table 2-759. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0828h

Figure 2-378. TOP_RCM_PLL_PER_HSDIVIDER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PLL_PER_HSDIVIDER_LDOPWDNACK	PLL_PER_HSDIVIDER_BYPASSACKZ
NONE						R	R
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PLL_PER_HSDIVIDER_TENABLEDIV	PLL_PER_HSDIVIDER_LDOPWDN	PLL_PER_HSDIVIDER_BYPASS
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 2-760. TOP_RCM_PLL_PER_HSDIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	PLL_PER_HSDIVIDER_LDOPWDNACK	R	0h	LDO Power Down Ack
16	PLL_PER_HSDIVIDER_BYPASSACKZ	R	0h	HSDIVIDER Bypass Ack
15:3	RESERVED	NONE	0h	Reserved
2	PLL_PER_HSDIVIDER_TENABLEDIV	R/W	0h	TENABLEDIV rising edge loads the values of M2REG and N2REG into ADPLLLJ register. TENABLEDIV could be activated anytime when the DPLL digital is in power-up condition. M2 and N2 latch [active rise edge]
1	PLL_PER_HSDIVIDER_LDOPWDN	R/W	0h	1'b1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT will be un-defined in this condition
0	PLL_PER_HSDIVIDER_BYPASS	R/W	0h	HSDIVIDER Bypass

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2.4.2.53 TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT0 Register

2.4.2.53.1 TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT0 Register (Offset = 82Ch) [reset = Bh]

Peripheral PLL high speed divider clock 0 control.

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Table 2-761. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 082Ch

Figure 2-379. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PLL_PER_HSDIVIDER_CLKOUT0_PWDN	RESERVED		PLL_PER_HSDIVIDER_CLKOUT0_STATUS	PLL_PER_HSDIVIDER_CLKOUT0_GATE_CTRL
NONE			R/W	NONE		R	R/W
0h			0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PLL_PER_HSDIVIDER_CLKOUT0_DIVCHACK	PLL_PER_HSDIVIDER_CLKOUT0_DIV				
NONE		R	R/W				
0h		0h	Bh				

Table 2-762. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	PLL_PER_HSDIVIDER_CLKOUT0_PWDN	R/W	0h	Power down for HSDIVIDER CLKOUT0 divider and hence CLKOUT0 output 0h[R/W] = CLKOUT0 divider active 1h[R/W] = CLKOUT0 divider is powered down
11:10	RESERVED	NONE	0h	Reserved
9	PLL_PER_HSDIVIDER_CLKOUT0_STATUS	R	0h	HSDIVIDER CLKOUT0 status 0h[R] = The clock output is gated 1h[R] = The clock output is enabled
8	PLL_PER_HSDIVIDER_CLKOUT0_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT0 0h[R/W] = Automatically gate this clock when there is no dependency for it 1h[R/W] = Force this clock to stay enabled even if there is no request
7:6	RESERVED	NONE	0h	Reserved
5	PLL_PER_HSDIVIDER_CLKOUT0_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT0_DIV indicates that the change in divider value has taken effect

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Table 2-762. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	PLL_PER_HSDIVIDER_CLKOUT0_DIV	R/W	Bh	DPLL post-divider factor, HSDIVIDER CLKOUT0, for internal clock generation. Divide values from 1 to 31. 0h[R/W] = Reserved

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2.4.2.54 TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT1 Register

2.4.2.54.1 TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT1 Register (Offset = 830h) [reset = 9h]

Peripheral PLL high speed divider clock 1 control.

Return to Summary Table

Table 2-763. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0830h

Figure 2-380. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td>PLL_PER_HSDIVIDER_CLKOUT1_PWDN</td><td colspan="2">RESERVED</td><td>PLL_PER_HSDIVIDER_CLKOUT1_STATUS</td><td>PLL_PER_HSDIVIDER_CLKOUT1_GATE_CTRL</td></tr>
<tr><td colspan="3">NONE</td><td>R/W</td><td colspan="2">NONE</td><td>R</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>PLL_PER_HSDIVIDER_CLKOUT1_DIVCHACK</td><td colspan="5">PLL_PER_HSDIVIDER_CLKOUT1_DIV</td></tr>
<tr><td colspan="2">NONE</td><td>R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="5">9h</td></tr>
</table>

Table 2-764. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	PLL_PER_HSDIVIDER_CLKOUT1_PWDN	R/W	0h	Power down for HSDIVIDER CLKOUT1 divider and hence CLKOUT1 output 0h[R/W] = CLKOUT1 divider active 1h[R/W] = CLKOUT1 divider is powered down
11:10	RESERVED	NONE	0h	Reserved
9	PLL_PER_HSDIVIDER_CLKOUT1_STATUS	R	0h	HSDIVIDER CLKOUT1 status 0h[R] = The clock output is gated 1h[R] = The clock output is enabled
8	PLL_PER_HSDIVIDER_CLKOUT1_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT1 0h[R/W] = Automatically gate this clock when there is no dependency for it 1h[R/W] = Force this clock to stay enabled even if there is no request
7:6	RESERVED	NONE	0h	Reserved
5	PLL_PER_HSDIVIDER_CLKOUT1_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect

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Table 2-764. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	PLL_PER_HSDIVIDER_CLKOUT1_DIV	R/W	9h	DPLL post-divider factor, HSDIVIDER CLKOUT1, for internal clock generation. Divide values from 1 to 31. 0h[R/W] = Reserved

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2.4.2.55 TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT2 Register

2.4.2.55.1 TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT2 Register (Offset = 834h) [reset = Bh]

Peripheral PLL high speed divider clock 2 control.

Return to Summary Table

Table 2-765. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0834h

Figure 2-381. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PLL_PER_HSDIVIDER_CLKOUT2_PWDN	RESERVED		PLL_PER_HSDIVIDER_CLKOUT2_STATUS	PLL_PER_HSDIVIDER_CLKOUT2_GATE_CTRL
NONE			R/W	NONE		R	R/W
0h			0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PLL_PER_HSDIVIDER_CLKOUT2_DIVCHACK	PLL_PER_HSDIVIDER_CLKOUT2_DIV				
NONE		R	R/W				
0h		0h	Bh				

Table 2-766. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12	PLL_PER_HSDIVIDER_CLKOUT2_PWDN	R/W	0h	Power down for HSDIVIDER CLKOUT2 divider and hence CLKOUT2 output 0h[R/W] = CLKOUT2 divider active 1h[R/W] = CLKOUT2 divider is powered down
11:10	RESERVED	NONE	0h	Reserved
9	PLL_PER_HSDIVIDER_CLKOUT2_STATUS	R	0h	HSDIVIDER CLKOUT2 status 0h[R] = The clock output is gated 1h[R] = The clock output is enabled
8	PLL_PER_HSDIVIDER_CLKOUT2_GATE_CTRL	R/W	0h	Control gating of HSDIVIDER CLKOUT2 0h[R/W] = Automatically gate this clock when there is no dependency for it 1h[R/W] = Force this clock to stay enabled even if there is no request
7:6	RESERVED	NONE	0h	Reserved
5	PLL_PER_HSDIVIDER_CLKOUT2_DIVCHACK	R	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect

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Table 2-766. TOP_RCM_PLL_PER_HSDIVIDER_CLKOUT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	PLL_PER_HSDIVIDER_CLKOUT2_DIV	R/W	Bh	DPLL post-divider factor, HSDIVIDER CLKOUT2, for internal clock generation. Divide values from 1 to 31. 0h[R/W] = Reserved

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2.4.2.56 TOP_RCM_PLL_PER_RSTCTRL Register

2.4.2.56.1 TOP_RCM_PLL_PER_RSTCTRL Register (Offset = 83Ch) [reset = 0h]

Peripheral PLL reset control.

Return to Summary Table

Table 2-767. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 083Ch

Figure 2-382. TOP_RCM_PLL_PER_RSTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PLL_PER_RSTCTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-768. TOP_RCM_PLL_PER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PLL_PER_RSTCTRL_ASSERT	R/W	0h	SW Reset override for the PLL Write 3'b111 : Override is enabled and Reset is asserted

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2.4.2.57 TOP_RCM_PLL_PER_HSDIVIDER_RSTCTRL Register

2.4.2.57.1 TOP_RCM_PLL_PER_HSDIVIDER_RSTCTRL Register (Offset = 840h) [reset = 0h]

Peripheral PLL high speed divider reset control.

Return to Summary Table

Table 2-769. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0840h

Figure 2-383. TOP_RCM_PLL_PER_HSDIVIDER_RSTCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PLL_PER_HSDIVIDER_RSTCTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-770. TOP_RCM_PLL_PER_HSDIVIDER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PLL_PER_HSDIVIDER_RSTCTRL_ASSERT	R/W	0h	SW Reset override for the HSDIVIDER Write 3'b111 : Override is enabled and Reset is asserted

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2.4.2.58 TOP_RCM_CLKOUT0_CLK_SRC_SEL Register

2.4.2.58.1 TOP_RCM_CLKOUT0_CLK_SRC_SEL Register (Offset = C00h) [reset = 0h]

Clock Source select register for CLKOUT clock.

Return to Summary Table

Table 2-771. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C00h

Figure 2-384. TOP_RCM_CLKOUT0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				CLKOUT0_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CLKOUT0_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-772. TOP_RCM_CLKOUT0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	CLKOUT0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for MSS CLKOUT . Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - DPLL_CORE_HSDIV0_CLKOUT0 0x222 - DPLL_CORE_HSDIV0_CLKOUT1 0x333 - DPLL_PER_HSDIV0_CLKOUT0 0x444 - DPLL_PER_HSDIV0_CLKOUT1 0x555 - RCCLK10M 0x666 - RCCLK32K 0x777 - CTPS_GENF0

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2.4.2.59 TOP_RCM_CLKOUT1_CLK_SRC_SEL Register

2.4.2.59.1 TOP_RCM_CLKOUT1_CLK_SRC_SEL Register (Offset = C04h) [reset = 0h]

Clock Source select register for CLKOUT clock.

Return to Summary Table

Table 2-773. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C04h

Figure 2-385. TOP_RCM_CLKOUT1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				CLKOUT1_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CLKOUT1_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-774. TOP_RCM_CLKOUT1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	CLKOUT1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for MSS CLKOUT . Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - DPLL_CORE_HSDIV0_CLKOUT0 0x222 - DPLL_CORE_HSDIV0_CLKOUT1 0x333 - DPLL_PER_HSDIV0_CLKOUT0 0x444 - DPLL_PER_HSDIV0_CLKOUT1 0x555 - RCCLK10M 0x666 - RCCLK32K 0x777 - CTPS_GENF0

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2.4.2.60 TOP_RCM_CLKOUT0_DIV_VAL Register

2.4.2.60.1 TOP_RCM_CLKOUT0_DIV_VAL Register (Offset = C08h) [reset = 0h]

Clock Divider register for CLKOUT clock.

Return to Summary Table

Table 2-775. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C08h

Figure 2-386. TOP_RCM_CLKOUT0_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				CLKOUT0_DIV_VAL_CLKDIV			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CLKOUT0_DIV_VAL_CLKDIV							
R/W							
0h							

Table 2-776. TOP_RCM_CLKOUT0_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	CLKOUT0_DIV_VAL_CLKDIV	R/W	0h	Divider value for CLKOUT selected clock..To set the divider value of [n+1] configure the register to '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.4.2.61 TOP_RCM_CLKOUT1_DIV_VAL Register

2.4.2.61.1 TOP_RCM_CLKOUT1_DIV_VAL Register (Offset = C0Ch) [reset = 0h]

Clock Divider register for CLKOUT clock.

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Table 2-777. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C0Ch

Figure 2-387. TOP_RCM_CLKOUT1_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				CLKOUT1_DIV_VAL_CLKDIV			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CLKOUT1_DIV_VAL_CLKDIV							
R/W							
0h							

Table 2-778. TOP_RCM_CLKOUT1_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	CLKOUT1_DIV_VAL_CLKDIV	R/W	0h	Divider value for CLKOUT selected clock..To set the divider value of [n+1] configure the register to '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.4.2.62 TOP_RCM_CLKOUT0_CLK_GATE Register

2.4.2.62.1 TOP_RCM_CLKOUT0_CLK_GATE Register (Offset = C10h) [reset = 0h]

Clock Gating register for CLKOUT clock.

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Table 2-779. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C10h

Figure 2-388. TOP_RCM_CLKOUT0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CLKOUT0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-780. TOP_RCM_CLKOUT0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CLKOUT0_CLK_GATE_GATED	R/W	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS CLKOUT Data should be loaded as multibit. Write 3'b000 : Clock is ungated [multibit 000] Write 3'b111 : Clock is gated [multibit 111]

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2.4.2.63 TOP_RCM_CLKOUT1_CLK_GATE Register

2.4.2.63.1 TOP_RCM_CLKOUT1_CLK_GATE Register (Offset = C14h) [reset = 0h]

Clock Gating register for CLKOUT clock.

Return to Summary Table

Table 2-781. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C14h

Figure 2-389. TOP_RCM_CLKOUT1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CLKOUT1_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-782. TOP_RCM_CLKOUT1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CLKOUT1_CLK_GATE_GATED	R/W	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS CLKOUT Data should be loaded as multibit. Write 3'b000 : Clock is ungated [multibit 000] Write 3'b111 : Clock is gated [multibit 111]

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2.4.2.64 TOP_RCM_CLKOUT0_CLK_STATUS Register

2.4.2.64.1 TOP_RCM_CLKOUT0_CLK_STATUS Register (Offset = C18h) [reset = 1h]

Clock Status register for CLKOUT clock.

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Table 2-783. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C18h

Figure 2-390. TOP_RCM_CLKOUT0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT0_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
CLKOUT0_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-784. TOP_RCM_CLKOUT0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	CLKOUT0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for CLKOUT Clock
7:0	CLKOUT0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for CLKOUT Clock

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2.4.2.65 TOP_RCM_CLKOUT1_CLK_STATUS Register

2.4.2.65.1 TOP_RCM_CLKOUT1_CLK_STATUS Register (Offset = C1Ch) [reset = 1h]

Clock Status register for CLKOUT clock.

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Table 2-785. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C1Ch

Figure 2-391. TOP_RCM_CLKOUT1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLKOUT1_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
CLKOUT1_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-786. TOP_RCM_CLKOUT1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	CLKOUT1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for CLKOUT Clock
7:0	CLKOUT1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for CLKOUT Clock

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2.4.2.66 TOP_RCM_TRCCLKOUT_CLK_SRC_SEL Register

2.4.2.66.1 TOP_RCM_TRCCLKOUT_CLK_SRC_SEL Register (Offset = C20h) [reset = 0h]

Clock Source select register for TRC clkout.

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Table 2-787. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C20h

Figure 2-392. TOP_RCM_TRCCLKOUT_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				TRCCLKOUT_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
TRCCLKOUT_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-788. TOP_RCM_TRCCLKOUT_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	TRCCLKOUT_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for TRC Clkout Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - DPLL_CORE_HSDIV0_CLKOUT0 0x222 - DPLL_CORE_HSDIV0_CLKOUT1 0x333 - DPLL_PER_HSDIV0_CLKOUT0 0x444 - DPLL_PER_HSDIV0_CLKOUT1 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.4.2.67 TOP_RCM_TRCCLKOUT_DIV_VAL Register

2.4.2.67.1 TOP_RCM_TRCCLKOUT_DIV_VAL Register (Offset = C24h) [reset = 0h]

Clock Divider register for TRC clkout.

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Table 2-789. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C24h

Figure 2-393. TOP_RCM_TRCCLKOUT_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				TRCCLKOUT_DIV_VAL_CLKDIV			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
TRCCLKOUT_DIV_VAL_CLKDIV							
R/W							
0h							

Table 2-790. TOP_RCM_TRCCLKOUT_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	TRCCLKOUT_DIV_VAL_CLKDIV	R/W	0h	Divider value for CLKOUT selected clock..To set the divider value of [n+1] configure the register to '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.4.2.68 TOP_RCM_TRCCLKOUT_CLK_GATE Register

2.4.2.68.1 TOP_RCM_TRCCLKOUT_CLK_GATE Register (Offset = C28h) [reset = 0h]

Clock Gating register for TRC clkout.

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Table 2-791. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C28h

Figure 2-394. TOP_RCM_TRCCLKOUT_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TRCCLKOUT_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-792. TOP_RCM_TRCCLKOUT_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TRCCLKOUT_CLK_GATE_GATED	R/W	0h	Clock gatring config for TRC Clkout Data should be loaded as multibit. Write 3'b000 : Clock is ungated [multibit 000] Write 3'b111 : Clock is gated [multibit 111]

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2.4.2.69 TOP_RCM_TRCCLKOUT_CLK_STATUS Register

2.4.2.69.1 TOP_RCM_TRCCLKOUT_CLK_STATUS Register (Offset = C2Ch) [reset = 1h]

Clock Status register for TRC clkout.

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Table 2-793. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C2Ch

Figure 2-395. TOP_RCM_TRCCLKOUT_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TRCCLKOUT_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
TRCCLKOUT_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-794. TOP_RCM_TRCCLKOUT_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TRCCLKOUT_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for PMIC Clkout Clock
7:0	TRCCLKOUT_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for PMIC Clkout Clock

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2.4.2.70 TOP_RCM_LOCK0_KICK0 Register

2.4.2.70.1 TOP_RCM_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component.

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Table 2-795. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1008h

Figure 2-396. TOP_RCM_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 2-796. TOP_RCM_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component

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2.4.2.71 TOP_RCM_LOCK0_KICK1 Register

2.4.2.71.1 TOP_RCM_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component.

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Table 2-797. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 100Ch

Figure 2-397. TOP_RCM_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 2-798. TOP_RCM_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component

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2.4.2.72 TOP_RCM_INTR_RAW_STATUS Register

2.4.2.72.1 TOP_RCM_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register.

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Table 2-799. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1010h

Figure 2-398. TOP_RCM_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 2-800. TOP_RCM_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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2.4.2.73 TOP_RCM_INTR_ENABLED_STATUS_CLEAR Register

2.4.2.73.1 TOP_RCM_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register.

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Table 2-801. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1014h

Figure 2-399. TOP_RCM_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 2-802. TOP_RCM_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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2.4.2.74 TOP_RCM_INTR_ENABLE Register

2.4.2.74.1 TOP_RCM_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register.

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Table 2-803. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1018h

Figure 2-400. TOP_RCM_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 2-804. TOP_RCM_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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2.4.2.75 TOP_RCM_INTR_ENABLE_CLEAR Register

2.4.2.75.1 TOP_RCM_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register.

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Table 2-805. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 101Ch

Figure 2-401. TOP_RCM_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 2-806. TOP_RCM_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

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2.4.2.76 TOP_RCM_EOI Register

2.4.2.76.1 TOP_RCM_EOI Register (Offset = 1020h) [reset = 0h]

EOI register.

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Table 2-807. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1020h

Figure 2-402. TOP_RCM_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 2-808. TOP_RCM_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip.

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2.4.2.77 TOP_RCM_FAULT_ADDRESS Register

2.4.2.77.1 TOP_RCM_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register.

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Table 2-809. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1024h

Figure 2-403. TOP_RCM_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 2-810. TOP_RCM_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address.

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2.4.2.78 TOP_RCM_FAULT_TYPE_STATUS Register

2.4.2.78.1 TOP_RCM_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register.

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Table 2-811. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1028h

Figure 2-404. TOP_RCM_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 2-812. TOP_RCM_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access.
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

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2.4.2.79 TOP_RCM_FAULT_ATTR_STATUS Register

2.4.2.79.1 TOP_RCM_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register.

Return to Summary Table

Table 2-813. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 102Ch

Figure 2-405. TOP_RCM_FAULT_ATTR_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">FAULT_XID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">FAULT_XID</td><td colspan="4">FAULT_ROUTEID</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FAULT_ROUTEID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FAULT_PRIVID</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 2-814. TOP_RCM_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID.
19:8	FAULT_ROUTEID	R	0h	Route ID.
7:0	FAULT_PRIVID	R	0h	Privilege ID.

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2.4.2.80 TOP_RCM_FAULT_CLEAR Register

2.4.2.80.1 TOP_RCM_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register.

Return to Summary Table

Table 2-815. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1030h

Figure 2-406. TOP_RCM_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 2-816. TOP_RCM_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

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2.5 MSS_RCM

MSS_RCM

2.5.1 MSS_RCM Summaries

MSS_RCM Summaries

Table 2-817. MSS_RCM Registers, Base Address=5320 8000h, Length=4096

Offset	Length	Register Name	MSS_RCM Physical Address
10h	32	MSS_RCM_R5SS0_RST_STATUS	5320 8010h
14h	32	MSS_RCM_R5SS0_RST_CAUSE_CLR	5320 8014h
18h	32	MSS_RCM_R5SS0_DBG_RST_EN	5320 8018h
1Ch	32	MSS_RCM_R5SS0_RST_ASSERDLY	5320 801Ch
20h	32	MSS_RCM_R5SS0_RST2ASSERTDLY	5320 8020h
24h	32	MSS_RCM_R5SS0_RST_WFICHECK	5320 8024h
30h	32	MSS_RCM_R5SS1_RST_STATUS	5320 8030h
34h	32	MSS_RCM_R5SS1_RST_CAUSE_CLR	5320 8034h
38h	32	MSS_RCM_R5SS1_DBG_RST_EN	5320 8038h
3Ch	32	MSS_RCM_R5SS1_RST_ASSERDLY	5320 803Ch
40h	32	MSS_RCM_R5SS1_RST2ASSERTDLY	5320 8040h
44h	32	MSS_RCM_R5SS1_RST_WFICHECK	5320 8044h
80h	32	MSS_RCM_CPSW_5_50_250_CLK_MUX_CTRL	5320 8080h
100h	32	MSS_RCM_MCAN0_CLK_SRC_SEL	5320 8100h
104h	32	MSS_RCM_MCAN1_CLK_SRC_SEL	5320 8104h
108h	32	MSS_RCM_MCAN2_CLK_SRC_SEL	5320 8108h
10Ch	32	MSS_RCM_MCAN3_CLK_SRC_SEL	5320 810Ch
110h	32	MSS_RCM_OSPI0_CLK_SRC_SEL	5320 8110h
114h	32	MSS_RCM_RTI0_CLK_SRC_SEL	5320 8114h
118h	32	MSS_RCM_RTI1_CLK_SRC_SEL	5320 8118h
11Ch	32	MSS_RCM_RTI2_CLK_SRC_SEL	5320 811Ch
120h	32	MSS_RCM_RTI3_CLK_SRC_SEL	5320 8120h
128h	32	MSS_RCM_WDT0_CLK_SRC_SEL	5320 8128h
12Ch	32	MSS_RCM_WDT1_CLK_SRC_SEL	5320 812Ch
130h	32	MSS_RCM_WDT2_CLK_SRC_SEL	5320 8130h
134h	32	MSS_RCM_WDT3_CLK_SRC_SEL	5320 8134h
13Ch	32	MSS_RCM_MCSPI0_CLK_SRC_SEL	5320 813Ch
140h	32	MSS_RCM_MCSPI1_CLK_SRC_SEL	5320 8140h
144h	32	MSS_RCM_MCSPI2_CLK_SRC_SEL	5320 8144h
148h	32	MSS_RCM_MCSPI3_CLK_SRC_SEL	5320 8148h
14Ch	32	MSS_RCM_MCSPI4_CLK_SRC_SEL	5320 814Ch
150h	32	MSS_RCM_MMC0_CLK_SRC_SEL	5320 8150h
154h	32	MSS_RCM_PRU_ICSS0_UART0_CLK_SRC_SEL	5320 8154h
158h	32	MSS_RCM_CPTS_CLK_SRC_SEL	5320 8158h
160h	32	MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL	5320 8160h
164h	32	MSS_RCM_I2C_CLK_SRC_SEL	5320 8164h
174h	32	MSS_RCM_LIN0_UART0_CLK_SRC_SEL	5320 8174h
178h	32	MSS_RCM_LIN1_UART1_CLK_SRC_SEL	5320 8178h
17Ch	32	MSS_RCM_LIN2_UART2_CLK_SRC_SEL	5320 817Ch
180h	32	MSS_RCM_LIN3_UART3_CLK_SRC_SEL	5320 8180h

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Table 2-817. MSS_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)

Offset	Length	Register Name	MSS_RCM Physical Address
184h	32	MSS_RCM_LIN4_UART4_CLK_SRC_SEL	5320 8184h
188h	32	MSS_RCM_LIN5_UART5_CLK_SRC_SEL	5320 8188h
18Ch	32	MSS_RCM_MCAN4_CLK_SRC_SEL	5320 818Ch
190h	32	MSS_RCM_MCAN5_CLK_SRC_SEL	5320 8190h
194h	32	MSS_RCM_MCAN6_CLK_SRC_SEL	5320 8194h
198h	32	MSS_RCM_MCAN7_CLK_SRC_SEL	5320 8198h
19Ch	32	MSS_RCM_RTI4_CLK_SRC_SEL	5320 819Ch
1A0h	32	MSS_RCM_RTI5_CLK_SRC_SEL	5320 81A0h
1A4h	32	MSS_RCM_RTI6_CLK_SRC_SEL	5320 81A4h
1A8h	32	MSS_RCM_RTI7_CLK_SRC_SEL	5320 81A8h
1ACh	32	MSS_RCM_MCSPI5_CLK_SRC_SEL	5320 81ACh
1B0h	32	MSS_RCM_MCSPI6_CLK_SRC_SEL	5320 81B0h
1B4h	32	MSS_RCM_MCSPI7_CLK_SRC_SEL	5320 81B4h
200h	32	MSS_RCM_MCAN0_CLK_DIV_VAL	5320 8200h
204h	32	MSS_RCM_MCAN1_CLK_DIV_VAL	5320 8204h
208h	32	MSS_RCM_MCAN2_CLK_DIV_VAL	5320 8208h
20Ch	32	MSS_RCM_MCAN3_CLK_DIV_VAL	5320 820Ch
210h	32	MSS_RCM_OSPI0_CLK_DIV_VAL	5320 8210h
214h	32	MSS_RCM_RTI0_CLK_DIV_VAL	5320 8214h
218h	32	MSS_RCM_RTI1_CLK_DIV_VAL	5320 8218h
21Ch	32	MSS_RCM_RTI2_CLK_DIV_VAL	5320 821Ch
220h	32	MSS_RCM_RTI3_CLK_DIV_VAL	5320 8220h
228h	32	MSS_RCM_WDT0_CLK_DIV_VAL	5320 8228h
22Ch	32	MSS_RCM_WDT1_CLK_DIV_VAL	5320 822Ch
230h	32	MSS_RCM_WDT2_CLK_DIV_VAL	5320 8230h
234h	32	MSS_RCM_WDT3_CLK_DIV_VAL	5320 8234h
23Ch	32	MSS_RCM_MCSPI0_CLK_DIV_VAL	5320 823Ch
240h	32	MSS_RCM_MCSPI1_CLK_DIV_VAL	5320 8240h
244h	32	MSS_RCM_MCSPI2_CLK_DIV_VAL	5320 8244h
248h	32	MSS_RCM_MCSPI3_CLK_DIV_VAL	5320 8248h
24Ch	32	MSS_RCM_MCSPI4_CLK_DIV_VAL	5320 824Ch
250h	32	MSS_RCM_MMC0_CLK_DIV_VAL	5320 8250h
254h	32	MSS_RCM_PRU_ICSS0_UART_CLK_DIV_VAL	5320 8254h
258h	32	MSS_RCM_CPTS_CLK_DIV_VAL	5320 8258h
260h	32	MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL	5320 8260h
264h	32	MSS_RCM_I2C_CLK_DIV_VAL	5320 8264h
274h	32	MSS_RCM_LIN0_UART0_CLK_DIV_VAL	5320 8274h
278h	32	MSS_RCM_LIN1_UART1_CLK_DIV_VAL	5320 8278h
27Ch	32	MSS_RCM_LIN2_UART2_CLK_DIV_VAL	5320 827Ch
280h	32	MSS_RCM_LIN3_UART3_CLK_DIV_VAL	5320 8280h
284h	32	MSS_RCM_LIN4_UART4_CLK_DIV_VAL	5320 8284h
288h	32	MSS_RCM_LIN5_UART5_CLK_DIV_VAL	5320 8288h
28Ch	32	MSS_RCM_RGMII_250_CLK_DIV_VAL	5320 828Ch
290h	32	MSS_RCM_RGMII_50_CLK_DIV_VAL	5320 8290h
294h	32	MSS_RCM_RGMII_5_CLK_DIV_VAL	5320 8294h
298h	32	MSS_RCM_XTAL_MMC_32K_CLK_DIV_VAL	5320 8298h
29Ch	32	MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL	5320 829Ch

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Table 2-817. MSS_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)

Offset	Length	Register Name	MSS_RCM Physical Address
2A4h	32	MSS_RCM_MCAN4_CLK_DIV_VAL	5320 82A4h
2A8h	32	MSS_RCM_MCAN5_CLK_DIV_VAL	5320 82A8h
2ACh	32	MSS_RCM_MCAN6_CLK_DIV_VAL	5320 82ACh
2B0h	32	MSS_RCM_MCAN7_CLK_DIV_VAL	5320 82B0h
2B4h	32	MSS_RCM_RTI4_CLK_DIV_VAL	5320 82B4h
2B8h	32	MSS_RCM_RTI5_CLK_DIV_VAL	5320 82B8h
2BCh	32	MSS_RCM_RTI6_CLK_DIV_VAL	5320 82BCh
2C0h	32	MSS_RCM_RTI7_CLK_DIV_VAL	5320 82C0h
2C4h	32	MSS_RCM_MCSPI5_CLK_DIV_VAL	5320 82C4h
2C8h	32	MSS_RCM_MCSPI6_CLK_DIV_VAL	5320 82C8h
2CCh	32	MSS_RCM_MCSPI7_CLK_DIV_VAL	5320 82CCh
300h	32	MSS_RCM_MCAN0_CLK_GATE	5320 8300h
304h	32	MSS_RCM_MCAN1_CLK_GATE	5320 8304h
308h	32	MSS_RCM_MCAN2_CLK_GATE	5320 8308h
30Ch	32	MSS_RCM_MCAN3_CLK_GATE	5320 830Ch
310h	32	MSS_RCM_OSPI0_CLK_GATE	5320 8310h
314h	32	MSS_RCM_RTI0_CLK_GATE	5320 8314h
318h	32	MSS_RCM_RTI1_CLK_GATE	5320 8318h
31Ch	32	MSS_RCM_RTI2_CLK_GATE	5320 831Ch
320h	32	MSS_RCM_RTI3_CLK_GATE	5320 8320h
328h	32	MSS_RCM_WDT0_CLK_GATE	5320 8328h
32Ch	32	MSS_RCM_WDT1_CLK_GATE	5320 832Ch
330h	32	MSS_RCM_WDT2_CLK_GATE	5320 8330h
334h	32	MSS_RCM_WDT3_CLK_GATE	5320 8334h
33Ch	32	MSS_RCM_MCSPI0_CLK_GATE	5320 833Ch
340h	32	MSS_RCM_MCSPI1_CLK_GATE	5320 8340h
344h	32	MSS_RCM_MCSPI2_CLK_GATE	5320 8344h
348h	32	MSS_RCM_MCSPI3_CLK_GATE	5320 8348h
34Ch	32	MSS_RCM_MCSPI4_CLK_GATE	5320 834Ch
350h	32	MSS_RCM_MMC0_CLK_GATE	5320 8350h
354h	32	MSS_RCM_PRU_ICSS0_UART_CLK_GATE	5320 8354h
358h	32	MSS_RCM_CPTS_CLK_GATE	5320 8358h
360h	32	MSS_RCM_CONTROLSS_PLL_CLK_GATE	5320 8360h
364h	32	MSS_RCM_I2C0_CLK_GATE	5320 8364h
368h	32	MSS_RCM_I2C1_CLK_GATE	5320 8368h
36Ch	32	MSS_RCM_I2C2_CLK_GATE	5320 836Ch
370h	32	MSS_RCM_I2C3_CLK_GATE	5320 8370h
374h	32	MSS_RCM_LIN0_CLK_GATE	5320 8374h
378h	32	MSS_RCM_LIN1_CLK_GATE	5320 8378h
37Ch	32	MSS_RCM_LIN2_CLK_GATE	5320 837Ch
380h	32	MSS_RCM_LIN3_CLK_GATE	5320 8380h
384h	32	MSS_RCM_LIN4_CLK_GATE	5320 8384h
38Ch	32	MSS_RCM_UART0_CLK_GATE	5320 838Ch
390h	32	MSS_RCM_UART1_CLK_GATE	5320 8390h
394h	32	MSS_RCM_UART2_CLK_GATE	5320 8394h
398h	32	MSS_RCM_UART3_CLK_GATE	5320 8398h
39Ch	32	MSS_RCM_UART4_CLK_GATE	5320 839Ch

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Table 2-817. MSS_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)

Offset	Length	Register Name	MSS_RCM Physical Address
3A0h	32	MSS_RCM_UART5_CLK_GATE	5320 83A0h
3A4h	32	MSS_RCM_RGMII_250_CLK_GATE	5320 83A4h
3A8h	32	MSS_RCM_RGMII_50_CLK_GATE	5320 83A8h
3ACh	32	MSS_RCM_RGMII_5_CLK_GATE	5320 83ACh
3B0h	32	MSS_RCM_MMC0_32K_CLK_GATE	5320 83B0h
3B4h	32	MSS_RCM_TEMPSENSE_32K_CLK_GATE	5320 83B4h
3B8h	32	MSS_RCM_CPSW_CLK_GATE	5320 83B8h
3BCh	32	MSS_RCM_PRU_ICSS0_IEP_CLK_GATE	5320 83BCh
3C0h	32	MSS_RCM_PRU_ICSS0_CORE_CLK_GATE	5320 83C0h
3C4h	32	MSS_RCM_MSS_PRU_ICSS_SYS_CLK_GATE	5320 83C4h
3CCh	32	MSS_RCM_R5SS0_CORE0_GATE	5320 83CCh
3D0h	32	MSS_RCM_R5SS1_CORE0_GATE	5320 83D0h
3D4h	32	MSS_RCM_R5SS0_CORE1_GATE	5320 83D4h
3D8h	32	MSS_RCM_R5SS1_CORE1_GATE	5320 83D8h
3DCh	32	MSS_RCM_MSS_MCAN4_CLK_GATE	5320 83DCh
3E0h	32	MSS_RCM_MSS_MCAN5_CLK_GATE	5320 83E0h
3E4h	32	MSS_RCM_MSS_MCAN6_CLK_GATE	5320 83E4h
3E8h	32	MSS_RCM_MSS_MCAN7_CLK_GATE	5320 83E8h
3ECh	32	MSS_RCM_RTI4_CLK_GATE	5320 83ECh
3F0h	32	MSS_RCM_RTI5_CLK_GATE	5320 83F0h
3F4h	32	MSS_RCM_RTI6_CLK_GATE	5320 83F4h
3F8h	32	MSS_RCM_RTI7_CLK_GATE	5320 83F8h
400h	32	MSS_RCM_MCAN0_CLK_STATUS	5320 8400h
404h	32	MSS_RCM_MCAN1_CLK_STATUS	5320 8404h
408h	32	MSS_RCM_MCAN2_CLK_STATUS	5320 8408h
40Ch	32	MSS_RCM_MCAN3_CLK_STATUS	5320 840Ch
410h	32	MSS_RCM_OSPI0_CLK_STATUS	5320 8410h
414h	32	MSS_RCM_RTI0_CLK_STATUS	5320 8414h
418h	32	MSS_RCM_RTI1_CLK_STATUS	5320 8418h
41Ch	32	MSS_RCM_RTI2_CLK_STATUS	5320 841Ch
420h	32	MSS_RCM_RTI3_CLK_STATUS	5320 8420h
428h	32	MSS_RCM_WDT0_CLK_STATUS	5320 8428h
42Ch	32	MSS_RCM_WDT1_CLK_STATUS	5320 842Ch
430h	32	MSS_RCM_WDT2_CLK_STATUS	5320 8430h
434h	32	MSS_RCM_WDT3_CLK_STATUS	5320 8434h
43Ch	32	MSS_RCM_MCSPI0_CLK_STATUS	5320 843Ch
440h	32	MSS_RCM_MCSPI1_CLK_STATUS	5320 8440h
444h	32	MSS_RCM_MCSPI2_CLK_STATUS	5320 8444h
448h	32	MSS_RCM_MCSPI3_CLK_STATUS	5320 8448h
44Ch	32	MSS_RCM_MCSPI4_CLK_STATUS	5320 844Ch
450h	32	MSS_RCM_MMC0_CLK_STATUS	5320 8450h
454h	32	MSS_RCM_PRU_ICSS0_UART_CLK_STATUS	5320 8454h
458h	32	MSS_RCM_CPTS_CLK_STATUS	5320 8458h
460h	32	MSS_RCM_CONTROLSS_PLL_CLK_STATUS	5320 8460h
464h	32	MSS_RCM_I2C_CLK_STATUS	5320 8464h
474h	32	MSS_RCM_LIN0_UART0_CLK_STATUS	5320 8474h
478h	32	MSS_RCM_LIN1_UART1_CLK_STATUS	5320 8478h

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Table 2-817. MSS_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)

Offset	Length	Register Name	MSS_RCM Physical Address
47Ch	32	MSS_RCM_LIN2_UART2_CLK_STATUS	5320 847Ch
480h	32	MSS_RCM_LIN3_UART3_CLK_STATUS	5320 8480h
484h	32	MSS_RCM_LIN4_UART4_CLK_STATUS	5320 8484h
488h	32	MSS_RCM_LIN5_UART5_CLK_STATUS	5320 8488h
48Ch	32	MSS_RCM_RGMII_250_CLK_STATUS	5320 848Ch
490h	32	MSS_RCM_RGMII_50_CLK_STATUS	5320 8490h
494h	32	MSS_RCM_RGMII_5_CLK_STATUS	5320 8494h
49Ch	32	MSS_RCM_MMC0_32K_CLK_STATUS	5320 849Ch
4A0h	32	MSS_RCM_TEMPSENSE_32K_CLK_STATUS	5320 84A0h
4A8h	32	MSS_RCM_MCAN4_CLK_STATUS	5320 84A8h
4ACh	32	MSS_RCM_MCAN5_CLK_STATUS	5320 84ACh
4B0h	32	MSS_RCM_MCAN6_CLK_STATUS	5320 84B0h
4B4h	32	MSS_RCM_MCAN7_CLK_STATUS	5320 84B4h
4B8h	32	MSS_RCM_RTI4_CLK_STATUS	5320 84B8h
4BCh	32	MSS_RCM_RTI5_CLK_STATUS	5320 84BCh
4C0h	32	MSS_RCM_RTI6_CLK_STATUS	5320 84C0h
4C4h	32	MSS_RCM_RTI7_CLK_STATUS	5320 84C4h
4C8h	32	MSS_RCM_MCSPI5_CLK_STATUS	5320 84C8h
4CCh	32	MSS_RCM_MCSPI6_CLK_STATUS	5320 84CCh
4D0h	32	MSS_RCM_MCSPI7_CLK_STATUS	5320 84D0h
500h	32	MSS_RCM_R5SS0_POR_RST_CTRL	5320 8500h
504h	32	MSS_RCM_R5SS1_POR_RST_CTRL	5320 8504h
508h	32	MSS_RCM_R5SS0_CORE0_GRST_CTRL	5320 8508h
50Ch	32	MSS_RCM_R5SS1_CORE0_GRST_CTRL	5320 850Ch
510h	32	MSS_RCM_R5SS0_CORE1_GRST_CTRL	5320 8510h
514h	32	MSS_RCM_R5SS1_CORE1_GRST_CTRL	5320 8514h
518h	32	MSS_RCM_R5SS0_CORE0_LRST_CTRL	5320 8518h
51Ch	32	MSS_RCM_R5SS1_CORE0_LRST_CTRL	5320 851Ch
520h	32	MSS_RCM_R5SS0_CORE1_LRST_CTRL	5320 8520h
524h	32	MSS_RCM_R5SS1_CORE1_LRST_CTRL	5320 8524h
528h	32	MSS_RCM_R5SS0_VIM0_RST_CTRL	5320 8528h
52Ch	32	MSS_RCM_R5SS1_VIM0_RST_CTRL	5320 852Ch
530h	32	MSS_RCM_R5SS0_VIM1_RST_CTRL	5320 8530h
534h	32	MSS_RCM_R5SS1_VIM1_RST_CTRL	5320 8534h
538h	32	MSS_RCM_MCRC0_RST_CTRL	5320 8538h
53Ch	32	MSS_RCM_RTI0_RST_CTRL	5320 853Ch
540h	32	MSS_RCM_RTI1_RST_CTRL	5320 8540h
544h	32	MSS_RCM_RTI2_RST_CTRL	5320 8544h
548h	32	MSS_RCM_RTI3_RST_CTRL	5320 8548h
54Ch	32	MSS_RCM_WDT0_RST_CTRL	5320 854Ch
550h	32	MSS_RCM_WDT1_RST_CTRL	5320 8550h
554h	32	MSS_RCM_WDT2_RST_CTRL	5320 8554h
558h	32	MSS_RCM_WDT3_RST_CTRL	5320 8558h
55Ch	32	MSS_RCM_TOP_ESM_RST_CTRL	5320 855Ch
560h	32	MSS_RCM_DCC0_RST_CTRL	5320 8560h
564h	32	MSS_RCM_DCC1_RST_CTRL	5320 8564h
568h	32	MSS_RCM_DCC2_RST_CTRL	5320 8568h

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Table 2-817. MSS_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)

Offset	Length	Register Name	MSS_RCM Physical Address
56Ch	32	MSS_RCM_DCC3_RST_CTRL	5320 856Ch
570h	32	MSS_RCM_MCSPI0_RST_CTRL	5320 8570h
574h	32	MSS_RCM_MCSPI1_RST_CTRL	5320 8574h
578h	32	MSS_RCM_MCSPI2_RST_CTRL	5320 8578h
57Ch	32	MSS_RCM_MCSPI3_RST_CTRL	5320 857Ch
580h	32	MSS_RCM_MCSPI4_RST_CTRL	5320 8580h
584h	32	MSS_RCM_OSPI0_RST_CTRL	5320 8584h
588h	32	MSS_RCM_MCAN0_RST_CTRL	5320 8588h
58Ch	32	MSS_RCM_MCAN1_RST_CTRL	5320 858Ch
590h	32	MSS_RCM_MCAN2_RST_CTRL	5320 8590h
594h	32	MSS_RCM_MCAN3_RST_CTRL	5320 8594h
598h	32	MSS_RCM_I2C0_RST_CTRL	5320 8598h
59Ch	32	MSS_RCM_I2C1_RST_CTRL	5320 859Ch
5A0h	32	MSS_RCM_I2C2_RST_CTRL	5320 85A0h
5A4h	32	MSS_RCM_I2C3_RST_CTRL	5320 85A4h
5A8h	32	MSS_RCM_UART0_RST_CTRL	5320 85A8h
5ACh	32	MSS_RCM_UART1_RST_CTRL	5320 85ACh
5B0h	32	MSS_RCM_UART2_RST_CTRL	5320 85B0h
5B4h	32	MSS_RCM_UART3_RST_CTRL	5320 85B4h
5B8h	32	MSS_RCM_UART4_RST_CTRL	5320 85B8h
5BCh	32	MSS_RCM_UART5_RST_CTRL	5320 85BCh
5C0h	32	MSS_RCM_LIN0_RST_CTRL	5320 85C0h
5C4h	32	MSS_RCM_LIN1_RST_CTRL	5320 85C4h
5C8h	32	MSS_RCM_LIN2_RST_CTRL	5320 85C8h
5CCh	32	MSS_RCM_LIN3_RST_CTRL	5320 85CCh
5D0h	32	MSS_RCM_LIN4_RST_CTRL	5320 85D0h
5D8h	32	MSS_RCM_EDMA_RST_CTRL	5320 85D8h
5DCh	32	MSS_RCM_INFRA_RST_CTRL	5320 85DCh
5E0h	32	MSS_RCM_CPSW_RST_CTRL	5320 85E0h
5E4h	32	MSS_RCM_PRU_ICSS0_RST_CTRL	5320 85E4h
5E8h	32	MSS_RCM_MMC0_RST_CTRL	5320 85E8h
5ECh	32	MSS_RCM_GPIO0_RST_CTRL	5320 85ECh
5F0h	32	MSS_RCM_GPIO1_RST_CTRL	5320 85F0h
5F4h	32	MSS_RCM_GPIO2_RST_CTRL	5320 85F4h
5F8h	32	MSS_RCM_GPIO3_RST_CTRL	5320 85F8h
5FCh	32	MSS_RCM_SPINLOCK0_RST_CTRL	5320 85FCh
604h	32	MSS_RCM_TEMPSENSE_32K_RST_CTRL	5320 8604h
60Ch	32	MSS_RCM_MCAN4_RST_CTRL	5320 860Ch
610h	32	MSS_RCM_MCAN5_RST_CTRL	5320 8610h
614h	32	MSS_RCM_MCAN6_RST_CTRL	5320 8614h
618h	32	MSS_RCM_MCAN7_RST_CTRL	5320 8618h
61Ch	32	MSS_RCM_RTI4_RST_CTRL	5320 861Ch
620h	32	MSS_RCM_RTI5_RST_CTRL	5320 8620h
624h	32	MSS_RCM_RTI6_RST_CTRL	5320 8624h
628h	32	MSS_RCM_RTI7_RST_CTRL	5320 8628h
62Ch	32	MSS_RCM_MCSPI5_RST_CTRL	5320 862Ch
630h	32	MSS_RCM_MCSPI6_RST_CTRL	5320 8630h

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Table 2-817. MSS_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)

Offset	Length	Register Name	MSS_RCM Physical Address
634h	32	MSS_RCM_MCSPI7_RST_CTRL	5320 8634h
700h	32	MSS_RCM_MSS_L2_BANK0_PD_CTRL	5320 8700h
704h	32	MSS_RCM_MSS_L2_BANK1_PD_CTRL	5320 8704h
708h	32	MSS_RCM_MSS_L2_BANK2_PD_CTRL	5320 8708h
70Ch	32	MSS_RCM_MSS_L2_BANK3_PD_CTRL	5320 870Ch
710h	32	MSS_RCM_MSS_L2_BANK0_PD_STATUS	5320 8710h
714h	32	MSS_RCM_MSS_L2_BANK1_PD_STATUS	5320 8714h
718h	32	MSS_RCM_MSS_L2_BANK2_PD_STATUS	5320 8718h
71Ch	32	MSS_RCM_MSS_L2_BANK3_PD_STATUS	5320 871Ch
730h	32	MSS_RCM_L2OCRAM_BANK4_PD_CTRL	5320 8730h
734h	32	MSS_RCM_L2OCRAM_BANK5_PD_CTRL	5320 8734h
738h	32	MSS_RCM_L2OCRAM_BANK4_PD_STATUS	5320 8738h
73Ch	32	MSS_RCM_L2OCRAM_BANK5_PD_STATUS	5320 873Ch
800h	32	MSS_RCM_HSM_RTIA_CLK_SRC_SEL	5320 8800h
804h	32	MSS_RCM_HSM_WDT_CLK_SRC_SEL	5320 8804h
808h	32	MSS_RCM_HSM_RTC_CLK_SRC_SEL	5320 8808h
80Ch	32	MSS_RCM_HSM_DMTA_CLK_SRC_SEL	5320 880Ch
810h	32	MSS_RCM_HSM_DMTB_CLK_SRC_SEL	5320 8810h
814h	32	MSS_RCM_HSM_RTI_CLK_DIV_VAL	5320 8814h
818h	32	MSS_RCM_HSM_WDT_CLK_DIV_VAL	5320 8818h
81Ch	32	MSS_RCM_HSM_RTC_CLK_DIV_VAL	5320 881Ch
820h	32	MSS_RCM_HSM_DMTA_CLK_DIV_VAL	5320 8820h
824h	32	MSS_RCM_HSM_DMTB_CLK_DIV_VAL	5320 8824h
828h	32	MSS_RCM_HSM_RTI_CLK_GATE	5320 8828h
82Ch	32	MSS_RCM_HSM_WDT_CLK_GATE	5320 882Ch
830h	32	MSS_RCM_HSM_RTC_CLK_GATE	5320 8830h
834h	32	MSS_RCM_HSM_DMTA_CLK_GATE	5320 8834h
838h	32	MSS_RCM_HSM_DMTB_CLK_GATE	5320 8838h
83Ch	32	MSS_RCM_HSM_RTI_CLK_STATUS	5320 883Ch
840h	32	MSS_RCM_HSM_WDT_CLK_STATUS	5320 8840h
844h	32	MSS_RCM_HSM_RTC_CLK_STATUS	5320 8844h
848h	32	MSS_RCM_HSM_DMTA_CLK_STATUS	5320 8848h
84Ch	32	MSS_RCM_HSM_DMTB_CLK_STATUS	5320 884Ch
900h	32	MSS_RCM_MCSPI5_CLK_GATE	5320 8900h
904h	32	MSS_RCM_MCSPI6_CLK_GATE	5320 8904h
908h	32	MSS_RCM_MCSPI7_CLK_GATE	5320 8908h
1008h	32	MSS_RCM_LOCK0_KICK0	5320 9008h
100Ch	32	MSS_RCM_LOCK0_KICK1	5320 900Ch
1010h	32	MSS_RCM_INTR_RAW_STATUS	5320 9010h
1014h	32	MSS_RCM_INTR_ENABLED_STATUS_CLEAR	5320 9014h
1018h	32	MSS_RCM_INTR_ENABLE	5320 9018h
101Ch	32	MSS_RCM_INTR_ENABLE_CLEAR	5320 901Ch
1020h	32	MSS_RCM_EOI	5320 9020h
1024h	32	MSS_RCM_FAULT_ADDRESS	5320 9024h
1028h	32	MSS_RCM_FAULT_TYPE_STATUS	5320 9028h
102Ch	32	MSS_RCM_FAULT_ATTR_STATUS	5320 902Ch

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Table 2-817. MSS_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)

Offset	Length	Register Name	MSS_RCM Physical Address
1030h	32	MSS_RCM_FAULT_CLEAR	5320 9030h

2.5.2 MSS_RCM Registers

MSS_RCM Registers

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2.5.2.1 MSS_RCM_R5SS0_RST_STATUS Register

2.5.2.1.1 MSS_RCM_R5SS0_RST_STATUS Register (Offset = 10h) [reset = 3h]

R5SS Reset Cause Status register of corresponding R5SS.

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Table 2-818. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8010h

Figure 2-407. MSS_RCM_R5SS0_RST_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					R5SS0_RST_STATUS_CAUSE		
NONE					R		
0h					3h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R5SS0_RST_STATUS_CAUSE							
R							
3h							

Table 2-819. MSS_RCM_R5SS0_RST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	R5SS0_RST_STATUS_CAUSE	R	3h	Has the status because of which reset has happened. Bit0: POR Reset Bit1: Warm Reset [ALso set during POR Reset] Bit2: CR5SS0 STC Reset Bit3 Reset for CORE0 and MSS_CORE00_VIM using MSS_RCM::MSS_CR5SSA0_RST_CTRL Bit4: Reset for CORE1 and MSS_CORE10_VIM using MSS_RCM::MSS_CR5SSB0_RST_CTRL Bit5: Reset for CORE0 only using MSS_RCM::MSS_CORE00_RST_CTRL Bit6: Reset for CORE1 only using using MSS_RCM::MSS_CORE10_RST_CTRL Bit7: Reset for CORE0 and MSS_CORE00_VIM caused because of reset request by debugger in CORE00 Bit8: Reset for CORE10 and MSS_CORE10_VIM caused because of reset request by debugger in CORE10 Bit9: Reset for CR5SS0 by the RESET FSM using MSS_CTRL::R5SS0_CONTROL_RESET_FSM_TRIGGER Bit 10 : Reset for CR5SS0 using MSS_RCM.R5SS0_POR_RST_CTRL

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2.5.2.2 MSS_RCM_R5SS0_RST_CAUSE_CLR Register

2.5.2.2.1 MSS_RCM_R5SS0_RST_CAUSE_CLR Register (Offset = 14h) [reset = 0h]

R5SS Reset Cause Clear register of corresponding R5SS.

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Table 2-820. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8014h

Figure 2-408. MSS_RCM_R5SS0_RST_CAUSE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_RST_CAUSE_CLR_CLR		
NONE					R/W		
0h					0h		

Table 2-821. MSS_RCM_R5SS0_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_RST_CAUSE_CLR_CLR	R/W	0h	Write pulse bit field: Clear bit for rst cause register [Writing 3'b111 will clear the rst cause register]

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2.5.2.3 MSS_RCM_R5SS0_DBG_RST_EN Register

2.5.2.3.1 MSS_RCM_R5SS0_DBG_RST_EN Register (Offset = 18h) [reset = 0h]

This register enables Core debug reset request to propogate to RCM.

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Table 2-822. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8018h

Figure 2-409. MSS_RCM_R5SS0_DBG_RST_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED					R5SS0_DBG_RST_EN_EN_CORE1		
NONE					R/W		
0h					0h		

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED					R5SS0_DBG_RST_EN_EN_CORE0		
NONE					R/W		
0h					0h		

Table 2-823. MSS_RCM_R5SS0_DBG_RST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	R5SS0_DBG_RST_EN_EN_CORE1	R/W	0h	Writing 3'b111 will block debug reset request from CORE1 toggling reset for CORE1 of respective R5SS
15:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_DBG_RST_EN_EN_CORE0	R/W	0h	Writing 3'b111 will block debug reset request from CORE0 toggling reset for CORE0 of respective R5SS

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2.5.2.4 MSS_RCM_R5SS0_RST_ASSERDLY Register

2.5.2.4.1 MSS_RCM_R5SS0_RST_ASSERDLY Register (Offset = 1Ch) [reset = Fh]

This register controls the reset duration of the corrseponding R5SS.

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Table 2-824. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 801Ch

Figure 2-410. MSS_RCM_R5SS0_RST_ASSERDLY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
R5SS0_RST_ASSERDLY_COMMON							
R/W							
Fh							

Table 2-825. MSS_RCM_R5SS0_RST_ASSERDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	R5SS0_RST_ASSERDLY_COMMON	R/W	Fh	Value decides number of cycles reset should be kept asserted for CR5SS related resets. Programming a value of 0xFF will keep the reset asserted untill a new value other than 0xFF is written to this register The actual duration is count + 2 cycles. S/W Recommended value for this is 0x0F The COUNT is applicable to both CPU cores

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2.5.2.5 MSS_RCM_R5SS0_RST2ASSERTDLY Register

2.5.2.5.1 MSS_RCM_R5SS0_RST2ASSERTDLY Register (Offset = 20h) [reset = 0h]

This register controls the delay of Reset assertion to the corresponding R5SS.

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Table 2-826. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8020h

Figure 2-411. MSS_RCM_R5SS0_RST2ASSERTDLY Name Register

31	30	29	28	27	26	25	24
R5SS0_RST2ASSERTDLY_R5_CORE1_COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS0_RST2ASSERTDLY_R5_CORE0_COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS0_RST2ASSERTDLY_R5SS_CORE1_COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS0_RST2ASSERTDLY_R5SS_CORE0_COUNT							
R/W							
0h							

Table 2-827. MSS_RCM_R5SS0_RST2ASSERTDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	R5SS0_RST2ASSERTDLY_R5_CORE1_COUNT	R/W	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE1
23:16	R5SS0_RST2ASSERTDLY_R5_CORE0_COUNT	R/W	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE0.
15:8	R5SS0_RST2ASSERTDLY_R5SS_CORE1_COUNT	R/W	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE1
7:0	R5SS0_RST2ASSERTDLY_R5SS_CORE0_COUNT	R/W	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE0.

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2.5.2.6 MSS_RCM_R5SS0_RST_WFICHECK Register

2.5.2.6.1 MSS_RCM_R5SS0_RST_WFICHECK Register (Offset = 24h) [reset = 7070707h]

Enable WFI ceck before R5 Reset is asserted.

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Table 2-828. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8024h

Figure 2-412. MSS_RCM_R5SS0_RST_WFICHECK Name Register

31	30	29	28	27	26	25	24
RESERVED					R5SS0_RST_WFICHECK_EN_R5_CORE1		
NONE					R/W		
0h					7h		
23	22	21	20	19	18	17	16
RESERVED					R5SS0_RST_WFICHECK_R5A		
NONE					R/W		
0h					7h		
15	14	13	12	11	10	9	8
RESERVED					R5SS0_RST_WFICHECK_EN_R5SS_CORE1		
NONE					R/W		
0h					7h		
7	6	5	4	3	2	1	0
RESERVED					R5SS0_RST_WFICHECK_EN_R5SS_CORE0		
NONE					R/W		
0h					7h		

Table 2-829. MSS_RCM_R5SS0_RST_WFICHECK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	R5SS0_RST_WFICHECK_EN_R5_CORE1	R/W	7h	Writing 3'b000 will disable check for WFI before local reset assertion of CORE0
23:19	RESERVED	NONE	0h	Reserved
18:16	R5SS0_RST_WFICHECK_R5A	R/W	7h	Writing 3'b000 will disable check for WFI before local reset assertion of CORE0
15:11	RESERVED	NONE	0h	Reserved
10:8	R5SS0_RST_WFICHECK_EN_R5SS_CORE1	R/W	7h	Writing 3'b000 will disable check for WFI before global reset assertion of CORE1
7:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_RST_WFICHECK_EN_R5SS_CORE0	R/W	7h	Writing 3'b000 will disable check for WFI before global reset assertion of CORE0

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2.5.2.7 MSS_RCM_R5SS1_RST_STATUS Register

2.5.2.7.1 MSS_RCM_R5SS1_RST_STATUS Register (Offset = 30h) [reset = 3h]

R5SS Reset Cause Status register of corresponding R5SS.

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Table 2-830. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8030h

Figure 2-413. MSS_RCM_R5SS1_RST_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					R5SS1_RST_STATUS_CAUSE		
NONE					R		
0h					3h		
7	6	5	4	3	2	1	0
R5SS1_RST_STATUS_CAUSE							
R							
3h							

Table 2-831. MSS_RCM_R5SS1_RST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	R5SS1_RST_STATUS_CAUSE	R	3h	Has the status because of which reset has happened. Bit0: POR Reset Bit1: Warm Reset [ALso set during POR Reset] Bit2: CR5SS1 STC Reset Bit3 Reset for CORE0 and MSS_CORE00_VIM using MSS_RCM::MSS_CR5SSA0_RST_CTRL Bit4: Reset for CORE1 and MSS_CORE10_VIM using MSS_RCM::MSS_CR5SSB0_RST_CTRL Bit5: Reset for CORE0 only using MSS_RCM::MSS_CORE00_RST_CTRL Bit6: Reset for CORE1 only using using MSS_RCM::MSS_CORE10_RST_CTRL Bit7: Reset for CORE0 and MSS_CORE00_VIM caused because of reset request by debugger in CORE00 Bit8: Reset for CORE10 and MSS_CORE10_VIM caused because of reset request by debugger in CORE10 Bit9: Reset for CR5SS0 by the RESET FSM using MSS_CTRL::R5SS0_CONTROL_RESET_FSM_TRIGGER Bit 10 : Reset for CR5SS1 using MSS_RCM.R5SS0_POR_RST_CTRL

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2.5.2.8 MSS_RCM_R5SS1_RST_CAUSE_CLR Register

2.5.2.8.1 MSS_RCM_R5SS1_RST_CAUSE_CLR Register (Offset = 34h) [reset = 0h]

R5SS Reset Cause Clear register of corresponding R5SS.

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Table 2-832. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8034h

Figure 2-414. MSS_RCM_R5SS1_RST_CAUSE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS1_RST_CAUSE_CLR_CLR		
NONE					R/W		
0h					0h		

Table 2-833. MSS_RCM_R5SS1_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_RST_CAUSE_CLR_CLR	R/W	0h	Write pulse bit field: Clear bit for rst cause register [Writing 3'b111 will clear the rst cause register]

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2.5.2.9 MSS_RCM_R5SS1_DBG_RST_EN Register

2.5.2.9.1 MSS_RCM_R5SS1_DBG_RST_EN Register (Offset = 38h) [reset = 0h]

This register enables Core debug reset request to propogate to RCM.

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Table 2-834. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8038h

Figure 2-415. MSS_RCM_R5SS1_DBG_RST_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					R5SS1_DBG_RST_EN_EN_CORE1		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_DBG_RST_EN_EN_CORE0		
NONE					R/W		
0h					0h		

Table 2-835. MSS_RCM_R5SS1_DBG_RST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:16	R5SS1_DBG_RST_EN_EN_CORE1	R/W	0h	Writing 3'b111 will block debug reset request from CORE1 toggling reset for CORE1 of respective R5SS
15:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_DBG_RST_EN_EN_CORE0	R/W	0h	Writing 3'b111 will block debug reset request from CORE0 toggling reset for CORE0 of respective R5SS

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2.5.2.10 MSS_RCM_R5SS1_RST_ASSERDLY Register

2.5.2.10.1 MSS_RCM_R5SS1_RST_ASSERDLY Register (Offset = 3Ch) [reset = Fh]

This register controls the reset duration of the corrseponding R5SS.

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Table 2-836. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 803Ch

Figure 2-416. MSS_RCM_R5SS1_RST_ASSERDLY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
R5SS1_RST_ASSERDLY_COMMON							
R/W							
Fh							

Table 2-837. MSS_RCM_R5SS1_RST_ASSERDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	R5SS1_RST_ASSERDLY_COMMON	R/W	Fh	Value decides number of cycles reset should be kept asserted for CR5SS related resets. Programming a value of 0xFF will keep the reset asserted untill a new value other than 0xFF is written to this register The actual duration is count + 2 cycles. S/W Recommended value for this is 0x0F The COUNT is applicable to both CPU cores

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2.5.2.11 MSS_RCM_R5SS1_RST2ASSERTDLY Register

2.5.2.11.1 MSS_RCM_R5SS1_RST2ASSERTDLY Register (Offset = 40h) [reset = 0h]

This register controls the delay of Reset assertion to the corresponding R5SS.

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Table 2-838. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8040h

Figure 2-417. MSS_RCM_R5SS1_RST2ASSERTDLY Name Register

31	30	29	28	27	26	25	24
R5SS1_RST2ASSERTDLY_R5_CORE1_COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
R5SS1_RST2ASSERTDLY_R5_CORE0_COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
R5SS1_RST2ASSERTDLY_R5SS_CORE1_COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
R5SS1_RST2ASSERTDLY_R5SS_CORE0_COUNT							
R/W							
0h							

Table 2-839. MSS_RCM_R5SS1_RST2ASSERTDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	R5SS1_RST2ASSERTDLY_R5_CORE1_COUNT	R/W	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE1
23:16	R5SS1_RST2ASSERTDLY_R5_CORE0_COUNT	R/W	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE0.
15:8	R5SS1_RST2ASSERTDLY_R5SS_CORE1_COUNT	R/W	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE1
7:0	R5SS1_RST2ASSERTDLY_R5SS_CORE0_COUNT	R/W	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE0.

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2.5.2.12 MSS_RCM_R5SS1_RST_WFICHECK Register

2.5.2.12.1 MSS_RCM_R5SS1_RST_WFICHECK Register (Offset = 44h) [reset = 7070707h]

Enable WFI ceck before R5 Reset is asserted.

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Table 2-840. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8044h

Figure 2-418. MSS_RCM_R5SS1_RST_WFICHECK Name Register

31	30	29	28	27	26	25	24
RESERVED					R5SS1_RST_WFICHECK_EN_R5_CORE1		
NONE					R/W		
0h					7h		
23	22	21	20	19	18	17	16
RESERVED					R5SS1_RST_WFICHECK_R5A		
NONE					R/W		
0h					7h		
15	14	13	12	11	10	9	8
RESERVED					R5SS1_RST_WFICHECK_EN_R5SS_CORE1		
NONE					R/W		
0h					7h		
7	6	5	4	3	2	1	0
RESERVED					R5SS1_RST_WFICHECK_EN_R5SS_CORE0		
NONE					R/W		
0h					7h		

Table 2-841. MSS_RCM_R5SS1_RST_WFICHECK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:24	R5SS1_RST_WFICHECK_EN_R5_CORE1	R/W	7h	Writing 3'b000 will disable check for WFI before local reset assertion of CORE0
23:19	RESERVED	NONE	0h	Reserved
18:16	R5SS1_RST_WFICHECK_R5A	R/W	7h	Writing 3'b000 will disable check for WFI before local reset assertion of CORE0
15:11	RESERVED	NONE	0h	Reserved
10:8	R5SS1_RST_WFICHECK_EN_R5SS_CORE1	R/W	7h	Writing 3'b000 will disable check for WFI before global reset assertion of CORE1
7:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_RST_WFICHECK_EN_R5SS_CORE0	R/W	7h	Writing 3'b000 will disable check for WFI before global reset assertion of CORE0

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2.5.2.13 MSS_RCM_CPSW_5_50_250_CLK_MUX_CTRL Register

2.5.2.13.1 MSS_RCM_CPSW_5_50_250_CLK_MUX_CTRL Register (Offset = 80h) [reset = 0h]

CPSW CLK MUX CTRL to select DPLL_PER_HSDIV0_CLKOUT1 or DPLL_CORE_HSDIV0_CLKOUT1.

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Table 2-842. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8080h

Figure 2-419. MSS_RCM_CPSW_5_50_250_CLK_MUX_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CPSW_5_50_250_CLK_MUX_CTRL_CLKSRCSEL		
NONE					R/W		
0h					0h		

Table 2-843. MSS_RCM_CPSW_5_50_250_CLK_MUX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CPSW_5_50_250_CLK_MUX_CTRL_CLKSRCSEL	R/W	0h	CPSW CLK MUX CTRL to select DPLL_PER_HSDIV0_CLKOUT1 or DPLL_CORE_HSDIV0_CLKOUT1 3'b000: DPLL_CORE_HSDIV0_CLKOUT1 [default] 3'b111: DPLL_PER_HSDIV0_CLKOUT1 **Note: The input clocks to the mux should be disabled when the mux select toggles.

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2.5.2.14 MSS_RCM_MCAN0_CLK_SRC_SEL Register

2.5.2.14.1 MSS_RCM_MCAN0_CLK_SRC_SEL Register (Offset = 100h) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

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Table 2-844. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8100h

Figure 2-420. MSS_RCM_MCAN0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN0_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN0_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-845. MSS_RCM_MCAN0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values for selecting clock source- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.15 MSS_RCM_MCAN1_CLK_SRC_SEL Register

2.5.2.15.1 MSS_RCM_MCAN1_CLK_SRC_SEL Register (Offset = 104h) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

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Table 2-846. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8104h

Figure 2-421. MSS_RCM_MCAN1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MCAN1_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCAN1_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-847. MSS_RCM_MCAN1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values for selecting clock source- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.16 MSS_RCM_MCAN2_CLK_SRC_SEL Register

2.5.2.16.1 MSS_RCM_MCAN2_CLK_SRC_SEL Register (Offset = 108h) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

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Table 2-848. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8108h

Figure 2-422. MSS_RCM_MCAN2_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN2_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN2_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-849. MSS_RCM_MCAN2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN2_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values for selecting clock source- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.17 MSS_RCM_MCAN3_CLK_SRC_SEL Register

2.5.2.17.1 MSS_RCM_MCAN3_CLK_SRC_SEL Register (Offset = 10Ch) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

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Table 2-850. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 810Ch

Figure 2-423. MSS_RCM_MCAN3_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN3_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN3_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-851. MSS_RCM_MCAN3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN3_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values for selecting clock source- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.18 MSS_RCM_OSPI0_CLK_SRC_SEL Register

2.5.2.18.1 MSS_RCM_OSPI0_CLK_SRC_SEL Register (Offset = 110h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-852. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8110h

Figure 2-424. MSS_RCM_OSPI0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				OSPI0_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
OSPI0_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-853. MSS_RCM_OSPI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	OSPI0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for OSPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - DPLL_CORE_HSDIV0_CLKOUT3 0x777 - DPLL_PER_HSDIV0_CLKOUT2

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2.5.2.19 MSS_RCM_RTI0_CLK_SRC_SEL Register

2.5.2.19.1 MSS_RCM_RTI0_CLK_SRC_SEL Register (Offset = 114h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-854. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8114h

Figure 2-425. MSS_RCM_RTI0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				RTI0_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RTI0_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-855. MSS_RCM_RTI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - CTPS_GENF0

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2.5.2.20 MSS_RCM_RTI1_CLK_SRC_SEL Register

2.5.2.20.1 MSS_RCM_RTI1_CLK_SRC_SEL Register (Offset = 118h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-856. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8118h

Figure 2-426. MSS_RCM_RTI1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI1_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI1_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-857. MSS_RCM_RTI1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - CTPS_GENF0

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2.5.2.21 MSS_RCM_RTI2_CLK_SRC_SEL Register

2.5.2.21.1 MSS_RCM_RTI2_CLK_SRC_SEL Register (Offset = 11Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-858. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 811Ch

Figure 2-427. MSS_RCM_RTI2_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				RTI2_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RTI2_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-859. MSS_RCM_RTI2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI2_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - CTPS_GENF0

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2.5.2.22 MSS_RCM_RTI3_CLK_SRC_SEL Register

2.5.2.22.1 MSS_RCM_RTI3_CLK_SRC_SEL Register (Offset = 120h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-860. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8120h

Figure 2-428. MSS_RCM_RTI3_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI3_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI3_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-861. MSS_RCM_RTI3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI3_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - CTPS_GENF0

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2.5.2.23 MSS_RCM_WDT0_CLK_SRC_SEL Register

2.5.2.23.1 MSS_RCM_WDT0_CLK_SRC_SEL Register (Offset = 128h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-862. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8128h

Figure 2-429. MSS_RCM_WDT0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WDT0_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
WDT0_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-863. MSS_RCM_WDT0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WDT0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - RCCLK10M 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK32K

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2.5.2.24 MSS_RCM_WDT1_CLK_SRC_SEL Register

2.5.2.24.1 MSS_RCM_WDT1_CLK_SRC_SEL Register (Offset = 12Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-864. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 812Ch

Figure 2-430. MSS_RCM_WDT1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WDT1_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
WDT1_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-865. MSS_RCM_WDT1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WDT1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - RCCLK10M 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK32K

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2.5.2.25 MSS_RCM_WDT2_CLK_SRC_SEL Register

2.5.2.25.1 MSS_RCM_WDT2_CLK_SRC_SEL Register (Offset = 130h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-866. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8130h

Figure 2-431. MSS_RCM_WDT2_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WDT2_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
WDT2_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-867. MSS_RCM_WDT2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WDT2_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - RCCLK10M 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK32K

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2.5.2.26 MSS_RCM_WDT3_CLK_SRC_SEL Register

2.5.2.26.1 MSS_RCM_WDT3_CLK_SRC_SEL Register (Offset = 134h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-868. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8134h

Figure 2-432. MSS_RCM_WDT3_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WDT3_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
WDT3_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-869. MSS_RCM_WDT3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WDT3_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - RCCLK10M 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK32K

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2.5.2.27 MSS_RCM_MCSPI0_CLK_SRC_SEL Register

2.5.2.27.1 MSS_RCM_MCSPI0_CLK_SRC_SEL Register (Offset = 13Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-870. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 813Ch

Figure 2-433. MSS_RCM_MCSPI0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI0_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI0_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-871. MSS_RCM_MCSPI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.28 MSS_RCM_MCSPI1_CLK_SRC_SEL Register

2.5.2.28.1 MSS_RCM_MCSPI1_CLK_SRC_SEL Register (Offset = 140h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-872. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8140h

Figure 2-434. MSS_RCM_MCSPI1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI1_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI1_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-873. MSS_RCM_MCSPI1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.29 MSS_RCM_MCSPI2_CLK_SRC_SEL Register

2.5.2.29.1 MSS_RCM_MCSPI2_CLK_SRC_SEL Register (Offset = 144h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-874. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8144h

Figure 2-435. MSS_RCM_MCSPI2_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI2_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI2_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-875. MSS_RCM_MCSPI2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI2_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.30 MSS_RCM_MCSPI3_CLK_SRC_SEL Register

2.5.2.30.1 MSS_RCM_MCSPI3_CLK_SRC_SEL Register (Offset = 148h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-876. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8148h

Figure 2-436. MSS_RCM_MCSPI3_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MCSPI3_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCSPI3_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-877. MSS_RCM_MCSPI3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI3_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.31 MSS_RCM_MCSPI4_CLK_SRC_SEL Register

2.5.2.31.1 MSS_RCM_MCSPI4_CLK_SRC_SEL Register (Offset = 14Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-878. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 814Ch

Figure 2-437. MSS_RCM_MCSPI4_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI4_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI4_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-879. MSS_RCM_MCSPI4_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI4_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.32 MSS_RCM_MMC0_CLK_SRC_SEL Register

2.5.2.32.1 MSS_RCM_MMC0_CLK_SRC_SEL Register (Offset = 150h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-880. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8150h

Figure 2-438. MSS_RCM_MMC0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MMC0_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MMC0_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-881. MSS_RCM_MMC0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MMC0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for MMCSD.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.33 MSS_RCM_PRU_ICSS0_UART0_CLK_SRC_SEL Register

2.5.2.33.1 MSS_RCM_PRU_ICSS0_UART0_CLK_SRC_SEL Register (Offset = 154h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-882. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8154h

Figure 2-439. MSS_RCM_PRU_ICSS0_UART0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				PRU_ICSS0_UART0_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PRU_ICSS0_UART0_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-883. MSS_RCM_PRU_ICSS0_UART0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	PRU_ICSS0_UART0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for ICSSM_UCLK.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - DPLL_PER_HSDIV0_CLKOUT0

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2.5.2.34 MSS_RCM_CPTS_CLK_SRC_SEL Register

2.5.2.34.1 MSS_RCM_CPTS_CLK_SRC_SEL Register (Offset = 158h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-884. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8158h

Figure 2-440. MSS_RCM_CPTS_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				CPTS_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CPTS_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-885. MSS_RCM_CPTS_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	CPTS_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for CPTS.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.35 MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL Register

2.5.2.35.1 MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL Register (Offset = 160h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-886. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8160h

Figure 2-441. MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				CONTROLSS_PLL_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CONTROLSS_PLL_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-887. MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	CONTROLSS_PLL_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for CONTROLSS_PLL.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - DPLL_CORE_HSDIV0_CLKOUT2 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.36 MSS_RCM_I2C_CLK_SRC_SEL Register

2.5.2.36.1 MSS_RCM_I2C_CLK_SRC_SEL Register (Offset = 164h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-888. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8164h

Figure 2-442. MSS_RCM_I2C_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				I2C_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
I2C_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-889. MSS_RCM_I2C_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	I2C_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for I2C.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.37 MSS_RCM_LIN0_UART0_CLK_SRC_SEL Register

2.5.2.37.1 MSS_RCM_LIN0_UART0_CLK_SRC_SEL Register (Offset = 174h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-890. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8174h

Figure 2-443. MSS_RCM_LIN0_UART0_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				LIN0_UART0_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LIN0_UART0_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-891. MSS_RCM_LIN0_UART0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN0_UART0_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - DPLL_PER_HSDIV0_CLKOUT0

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2.5.2.38 MSS_RCM_LIN1_UART1_CLK_SRC_SEL Register

2.5.2.38.1 MSS_RCM_LIN1_UART1_CLK_SRC_SEL Register (Offset = 178h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-892. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8178h

Figure 2-444. MSS_RCM_LIN1_UART1_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				LIN1_UART1_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LIN1_UART1_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-893. MSS_RCM_LIN1_UART1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN1_UART1_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - DPLL_PER_HSDIV0_CLKOUT0

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2.5.2.39 MSS_RCM_LIN2_UART2_CLK_SRC_SEL Register

2.5.2.39.1 MSS_RCM_LIN2_UART2_CLK_SRC_SEL Register (Offset = 17Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-894. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 817Ch

Figure 2-445. MSS_RCM_LIN2_UART2_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				LIN2_UART2_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIN2_UART2_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-895. MSS_RCM_LIN2_UART2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN2_UART2_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - DPLL_PER_HSDIV0_CLKOUT0

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2.5.2.40 MSS_RCM_LIN3_UART3_CLK_SRC_SEL Register

2.5.2.40.1 MSS_RCM_LIN3_UART3_CLK_SRC_SEL Register (Offset = 180h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to Summary Table

Table 2-896. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8180h

Figure 2-446. MSS_RCM_LIN3_UART3_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				LIN3_UART3_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LIN3_UART3_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-897. MSS_RCM_LIN3_UART3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN3_UART3_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - DPLL_PER_HSDIV0_CLKOUT0

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2.5.2.41 MSS_RCM_LIN4_UART4_CLK_SRC_SEL Register

2.5.2.41.1 MSS_RCM_LIN4_UART4_CLK_SRC_SEL Register (Offset = 184h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-898. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8184h

Figure 2-447. MSS_RCM_LIN4_UART4_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				LIN4_UART4_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LIN4_UART4_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-899. MSS_RCM_LIN4_UART4_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN4_UART4_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - DPLL_PER_HSDIV0_CLKOUT0

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2.5.2.42 MSS_RCM_LIN5_UART5_CLK_SRC_SEL Register

2.5.2.42.1 MSS_RCM_LIN5_UART5_CLK_SRC_SEL Register (Offset = 188h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-900. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8188h

Figure 2-448. MSS_RCM_LIN5_UART5_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				LIN5_UART5_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIN5_UART5_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-901. MSS_RCM_LIN5_UART5_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN5_UART5_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - DPLL_PER_HSDIV0_CLKOUT0

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2.5.2.43 MSS_RCM_MCAN4_CLK_SRC_SEL Register

2.5.2.43.1 MSS_RCM_MCAN4_CLK_SRC_SEL Register (Offset = 18Ch) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

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Table 2-902. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 818Ch

Figure 2-449. MSS_RCM_MCAN4_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN4_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN4_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-903. MSS_RCM_MCAN4_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN4_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values for selecting clock source- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.44 MSS_RCM_MCAN5_CLK_SRC_SEL Register

2.5.2.44.1 MSS_RCM_MCAN5_CLK_SRC_SEL Register (Offset = 190h) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

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Table 2-904. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8190h

Figure 2-450. MSS_RCM_MCAN5_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN5_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN5_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-905. MSS_RCM_MCAN5_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN5_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values for selecting clock source- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.45 MSS_RCM_MCAN6_CLK_SRC_SEL Register

2.5.2.45.1 MSS_RCM_MCAN6_CLK_SRC_SEL Register (Offset = 194h) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

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Table 2-906. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8194h

Figure 2-451. MSS_RCM_MCAN6_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN6_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN6_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-907. MSS_RCM_MCAN6_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN6_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values for selecting clock source- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.46 MSS_RCM_MCAN7_CLK_SRC_SEL Register

2.5.2.46.1 MSS_RCM_MCAN7_CLK_SRC_SEL Register (Offset = 198h) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

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Table 2-908. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8198h

Figure 2-452. MSS_RCM_MCAN7_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN7_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN7_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-909. MSS_RCM_MCAN7_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN7_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values for selecting clock source- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.47 MSS_RCM_RTI4_CLK_SRC_SEL Register

2.5.2.47.1 MSS_RCM_RTI4_CLK_SRC_SEL Register (Offset = 19Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-910. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 819Ch

Figure 2-453. MSS_RCM_RTI4_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI4_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI4_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-911. MSS_RCM_RTI4_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI4_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - CTPS_GENF0

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2.5.2.48 MSS_RCM_RTI5_CLK_SRC_SEL Register

2.5.2.48.1 MSS_RCM_RTI5_CLK_SRC_SEL Register (Offset = 1A0h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-912. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 81A0h

Figure 2-454. MSS_RCM_RTI5_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI5_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI5_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-913. MSS_RCM_RTI5_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI5_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - CTPS_GENF0

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2.5.2.49 MSS_RCM_RTI6_CLK_SRC_SEL Register

2.5.2.49.1 MSS_RCM_RTI6_CLK_SRC_SEL Register (Offset = 1A4h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-914. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 81A4h

Figure 2-455. MSS_RCM_RTI6_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI6_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI6_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-915. MSS_RCM_RTI6_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI6_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - CTPS_GENF0

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2.5.2.50 MSS_RCM_RTI7_CLK_SRC_SEL Register

2.5.2.50.1 MSS_RCM_RTI7_CLK_SRC_SEL Register (Offset = 1A8h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-916. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 81A8h

Figure 2-456. MSS_RCM_RTI7_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI7_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI7_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-917. MSS_RCM_RTI7_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI7_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - CTPS_GENF0

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2.5.2.51 MSS_RCM_MCSPI5_CLK_SRC_SEL Register

2.5.2.51.1 MSS_RCM_MCSPI5_CLK_SRC_SEL Register (Offset = 1ACh) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-918. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 81ACh

Figure 2-457. MSS_RCM_MCSPI5_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI5_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI5_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-919. MSS_RCM_MCSPI5_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI5_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.52 MSS_RCM_MCSPI6_CLK_SRC_SEL Register

2.5.2.52.1 MSS_RCM_MCSPI6_CLK_SRC_SEL Register (Offset = 1B0h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-920. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 81B0h

Figure 2-458. MSS_RCM_MCSPI6_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MCSPI6_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCSPI6_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-921. MSS_RCM_MCSPI6_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI6_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.53 MSS_RCM_MCSPI7_CLK_SRC_SEL Register

2.5.2.53.1 MSS_RCM_MCSPI7_CLK_SRC_SEL Register (Offset = 1B4h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-922. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 81B4h

Figure 2-459. MSS_RCM_MCSPI7_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI7_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI7_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-923. MSS_RCM_MCSPI7_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI7_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - EXT_REFCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - DPLL_CORE_HSDIV0_CLKOUT0 0x555 - RCCLK10M 0x666 - XTALCLK 0x777 - RCCLK10M

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2.5.2.54 MSS_RCM_MCAN0_CLK_DIV_VAL Register

2.5.2.54.1 MSS_RCM_MCAN0_CLK_DIV_VAL Register (Offset = 200h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-924. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8200h

Figure 2-460. MSS_RCM_MCAN0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MCAN0_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCAN0_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-925. MSS_RCM_MCAN0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.55 MSS_RCM_MCAN1_CLK_DIV_VAL Register

2.5.2.55.1 MSS_RCM_MCAN1_CLK_DIV_VAL Register (Offset = 204h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-926. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8204h

Figure 2-461. MSS_RCM_MCAN1_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN1_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN1_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-927. MSS_RCM_MCAN1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN1_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.56 MSS_RCM_MCAN2_CLK_DIV_VAL Register

2.5.2.56.1 MSS_RCM_MCAN2_CLK_DIV_VAL Register (Offset = 208h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-928. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8208h

Figure 2-462. MSS_RCM_MCAN2_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN2_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN2_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-929. MSS_RCM_MCAN2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN2_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.57 MSS_RCM_MCAN3_CLK_DIV_VAL Register

2.5.2.57.1 MSS_RCM_MCAN3_CLK_DIV_VAL Register (Offset = 20Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-930. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 820Ch

Figure 2-463. MSS_RCM_MCAN3_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN3_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN3_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-931. MSS_RCM_MCAN3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN3_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.58 MSS_RCM_OSPI0_CLK_DIV_VAL Register

2.5.2.58.1 MSS_RCM_OSPI0_CLK_DIV_VAL Register (Offset = 210h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-932. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8210h

Figure 2-464. MSS_RCM_OSPI0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				OSPI0_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
OSPI0_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-933. MSS_RCM_OSPI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	OSPI0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value OSPI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.59 MSS_RCM_RTI0_CLK_DIV_VAL Register

2.5.2.59.1 MSS_RCM_RTI0_CLK_DIV_VAL Register (Offset = 214h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-934. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8214h

Figure 2-465. MSS_RCM_RTI0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI0_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI0_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-935. MSS_RCM_RTI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.60 MSS_RCM_RTI1_CLK_DIV_VAL Register

2.5.2.60.1 MSS_RCM_RTI1_CLK_DIV_VAL Register (Offset = 218h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-936. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8218h

Figure 2-466. MSS_RCM_RTI1_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI1_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI1_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-937. MSS_RCM_RTI1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI1_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.61 MSS_RCM_RTI2_CLK_DIV_VAL Register

2.5.2.61.1 MSS_RCM_RTI2_CLK_DIV_VAL Register (Offset = 21Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-938. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 821Ch

Figure 2-467. MSS_RCM_RTI2_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI2_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI2_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-939. MSS_RCM_RTI2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI2_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.62 MSS_RCM_RTI3_CLK_DIV_VAL Register

2.5.2.62.1 MSS_RCM_RTI3_CLK_DIV_VAL Register (Offset = 220h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-940. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8220h

Figure 2-468. MSS_RCM_RTI3_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI3_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI3_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-941. MSS_RCM_RTI3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI3_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.63 MSS_RCM_WDT0_CLK_DIV_VAL Register

2.5.2.63.1 MSS_RCM_WDT0_CLK_DIV_VAL Register (Offset = 228h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-942. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8228h

Figure 2-469. MSS_RCM_WDT0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WDT0_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
WDT0_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-943. MSS_RCM_WDT0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WDT0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value WDT selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.64 MSS_RCM_WDT1_CLK_DIV_VAL Register

2.5.2.64.1 MSS_RCM_WDT1_CLK_DIV_VAL Register (Offset = 22Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-944. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 822Ch

Figure 2-470. MSS_RCM_WDT1_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WDT1_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
WDT1_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-945. MSS_RCM_WDT1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WDT1_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value WDT selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.65 MSS_RCM_WDT2_CLK_DIV_VAL Register

2.5.2.65.1 MSS_RCM_WDT2_CLK_DIV_VAL Register (Offset = 230h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-946. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8230h

Figure 2-471. MSS_RCM_WDT2_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WDT2_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
WDT2_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-947. MSS_RCM_WDT2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WDT2_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value WDT selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.66 MSS_RCM_WDT3_CLK_DIV_VAL Register

2.5.2.66.1 MSS_RCM_WDT3_CLK_DIV_VAL Register (Offset = 234h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-948. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8234h

Figure 2-472. MSS_RCM_WDT3_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				WDT3_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
WDT3_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-949. MSS_RCM_WDT3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	WDT3_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value WDT selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.67 MSS_RCM_MCSPI0_CLK_DIV_VAL Register

2.5.2.67.1 MSS_RCM_MCSPI0_CLK_DIV_VAL Register (Offset = 23Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-950. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 823Ch

Figure 2-473. MSS_RCM_MCSPI0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI0_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI0_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-951. MSS_RCM_MCSPI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.68 MSS_RCM_MCSPI1_CLK_DIV_VAL Register

2.5.2.68.1 MSS_RCM_MCSPI1_CLK_DIV_VAL Register (Offset = 240h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-952. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8240h

Figure 2-474. MSS_RCM_MCSPI1_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MCSPI1_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCSPI1_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-953. MSS_RCM_MCSPI1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI1_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.69 MSS_RCM_MCSPI2_CLK_DIV_VAL Register

2.5.2.69.1 MSS_RCM_MCSPI2_CLK_DIV_VAL Register (Offset = 244h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-954. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8244h

Figure 2-475. MSS_RCM_MCSPI2_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI2_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI2_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-955. MSS_RCM_MCSPI2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI2_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.70 MSS_RCM_MCSPI3_CLK_DIV_VAL Register

2.5.2.70.1 MSS_RCM_MCSPI3_CLK_DIV_VAL Register (Offset = 248h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-956. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8248h

Figure 2-476. MSS_RCM_MCSPI3_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI3_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI3_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-957. MSS_RCM_MCSPI3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI3_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.71 MSS_RCM_MCSPI4_CLK_DIV_VAL Register

2.5.2.71.1 MSS_RCM_MCSPI4_CLK_DIV_VAL Register (Offset = 24Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-958. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 824Ch

Figure 2-477. MSS_RCM_MCSPI4_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI4_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI4_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-959. MSS_RCM_MCSPI4_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI4_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.72 MSS_RCM_MMC0_CLK_DIV_VAL Register

2.5.2.72.1 MSS_RCM_MMC0_CLK_DIV_VAL Register (Offset = 250h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-960. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8250h

Figure 2-478. MSS_RCM_MMC0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MMC0_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MMC0_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-961. MSS_RCM_MMC0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MMC0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value MMCSD selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.73 MSS_RCM_PRU_ICSS0_UART_CLK_DIV_VAL Register

2.5.2.73.1 MSS_RCM_PRU_ICSS0_UART_CLK_DIV_VAL Register (Offset = 254h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-962. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8254h

Figure 2-479. MSS_RCM_PRU_ICSS0_UART_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				PRU_ICSS0_UART_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PRU_ICSS0_UART_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-963. MSS_RCM_PRU_ICSS0_UART_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	PRU_ICSS0_UART_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value ICSSM_UCLK selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.74 MSS_RCM_CPTS_CLK_DIV_VAL Register

2.5.2.74.1 MSS_RCM_CPTS_CLK_DIV_VAL Register (Offset = 258h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-964. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8258h

Figure 2-480. MSS_RCM_CPTS_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				CPTS_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CPTS_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-965. MSS_RCM_CPTS_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	CPTS_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value CPTS selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.75 MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL Register

2.5.2.75.1 MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL Register (Offset = 260h) [reset = 0h]

CONTROLSS_PLL_CLK Divider Value for Control subsystem.

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Table 2-966. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8260h

Figure 2-481. MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				CONTROLSS_PLL_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
CONTROLSS_PLL_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-967. MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	CONTROLSS_PLL_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value CONTROLSS_PLL selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.76 MSS_RCM_I2C_CLK_DIV_VAL Register

2.5.2.76.1 MSS_RCM_I2C_CLK_DIV_VAL Register (Offset = 264h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-968. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8264h

Figure 2-482. MSS_RCM_I2C_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				I2C_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
I2C_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-969. MSS_RCM_I2C_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	I2C_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value I2C selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.77 MSS_RCM_LIN0_UART0_CLK_DIV_VAL Register

2.5.2.77.1 MSS_RCM_LIN0_UART0_CLK_DIV_VAL Register (Offset = 274h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-970. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8274h

Figure 2-483. MSS_RCM_LIN0_UART0_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				LIN0_UART0_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LIN0_UART0_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-971. MSS_RCM_LIN0_UART0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN0_UART0_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.78 MSS_RCM_LIN1_UART1_CLK_DIV_VAL Register

2.5.2.78.1 MSS_RCM_LIN1_UART1_CLK_DIV_VAL Register (Offset = 278h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-972. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8278h

Figure 2-484. MSS_RCM_LIN1_UART1_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				LIN1_UART1_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LIN1_UART1_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-973. MSS_RCM_LIN1_UART1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN1_UART1_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.79 MSS_RCM_LIN2_UART2_CLK_DIV_VAL Register

2.5.2.79.1 MSS_RCM_LIN2_UART2_CLK_DIV_VAL Register (Offset = 27Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-974. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 827Ch

Figure 2-485. MSS_RCM_LIN2_UART2_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				LIN2_UART2_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LIN2_UART2_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-975. MSS_RCM_LIN2_UART2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN2_UART2_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.80 MSS_RCM_LIN3_UART3_CLK_DIV_VAL Register

2.5.2.80.1 MSS_RCM_LIN3_UART3_CLK_DIV_VAL Register (Offset = 280h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-976. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8280h

Figure 2-486. MSS_RCM_LIN3_UART3_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				LIN3_UART3_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LIN3_UART3_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-977. MSS_RCM_LIN3_UART3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN3_UART3_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.81 MSS_RCM_LIN4_UART4_CLK_DIV_VAL Register

2.5.2.81.1 MSS_RCM_LIN4_UART4_CLK_DIV_VAL Register (Offset = 284h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-978. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8284h

Figure 2-487. MSS_RCM_LIN4_UART4_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				LIN4_UART4_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LIN4_UART4_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-979. MSS_RCM_LIN4_UART4_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN4_UART4_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.82 MSS_RCM_LIN5_UART5_CLK_DIV_VAL Register

2.5.2.82.1 MSS_RCM_LIN5_UART5_CLK_DIV_VAL Register (Offset = 288h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-980. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8288h

Figure 2-488. MSS_RCM_LIN5_UART5_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				LIN5_UART5_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
LIN5_UART5_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-981. MSS_RCM_LIN5_UART5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	LIN5_UART5_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value for corresponding UART and LIN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.83 MSS_RCM_RGMII_250_CLK_DIV_VAL Register

2.5.2.83.1 MSS_RCM_RGMII_250_CLK_DIV_VAL Register (Offset = 28Ch) [reset = 111h]

RGMII 250 CLK Divider Value.

Return to Summary Table

Table 2-982. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 828Ch

Figure 2-489. MSS_RCM_RGMII_250_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RGMII_250_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				111h			
7	6	5	4	3	2	1	0
RGMII_250_CLK_DIV_VAL_CLKDIVR							
R/W							
111h							

Table 2-983. MSS_RCM_RGMII_250_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RGMII_250_CLK_DIV_VAL_CLKDIVR	R/W	111h	Divider value RGMII selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.84 MSS_RCM_RGMII_50_CLK_DIV_VAL Register

2.5.2.84.1 MSS_RCM_RGMII_50_CLK_DIV_VAL Register (Offset = 290h) [reset = 999h]

RGMII 50 CLK Divider Value.

Return to Summary Table

Table 2-984. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8290h

Figure 2-490. MSS_RCM_RGMII_50_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RGMII_50_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				999h			
7	6	5	4	3	2	1	0
RGMII_50_CLK_DIV_VAL_CLKDIVR							
R/W							
999h							

Table 2-985. MSS_RCM_RGMII_50_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RGMII_50_CLK_DIV_VAL_CLKDIVR	R/W	999h	Divider value MII100 selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.85 MSS_RCM_RGMII_5_CLK_DIV_VAL Register

2.5.2.85.1 MSS_RCM_RGMII_5_CLK_DIV_VAL Register (Offset = 294h) [reset = 636363h]

RGMII 5 CLK Divider Value.

Return to Summary Table

Table 2-986. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8294h

Figure 2-491. MSS_RCM_RGMII_5_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RGMII_5_CLK_DIV_VAL_CLKDIVR							
R/W							
636363h							
15	14	13	12	11	10	9	8
RGMII_5_CLK_DIV_VAL_CLKDIVR							
R/W							
636363h							
7	6	5	4	3	2	1	0
RGMII_5_CLK_DIV_VAL_CLKDIVR							
R/W							
636363h							

Table 2-987. MSS_RCM_RGMII_5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	RGMII_5_CLK_DIV_VAL_CLKDIVR	R/W	636363h	Divider value MII10 selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x15' is required then '0x151515' should be configured to the register.

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2.5.2.86 MSS_RCM_XTAL_MMC_32K_CLK_DIV_VAL Register

2.5.2.86.1 MSS_RCM_XTAL_MMC_32K_CLK_DIV_VAL Register (Offset = 298h) [reset = 30CC330Ch]

XTAL 32K CLK Divider Value for MMC.

Return to Summary Table

Table 2-988. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8298h

Figure 2-492. MSS_RCM_XTAL_MMC_32K_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED		XTAL_MMC_32K_CLK_DIV_VAL_CLKDIVR					
NONE		R/W					
0h		30CC330Ch					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XTAL_MMC_32K_CLK_DIV_VAL_CLKDIVR							
R/W							
30CC330Ch							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XTAL_MMC_32K_CLK_DIV_VAL_CLKDIVR							
R/W							
30CC330Ch							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XTAL_MMC_32K_CLK_DIV_VAL_CLKDIVR							
R/W							
30CC330Ch							

Table 2-989. MSS_RCM_XTAL_MMC_32K_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	XTAL_MMC_32K_CLK_DIV_VAL_CLKDIVR	R/W	30CC330Ch	Divider value for XTAL_32K clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x30C' is required then register should be configured as follows - bits[9:0] = 0x30C bits[19:10] = 0x30C bits[29:20] = 0x30C This configures the register to 0x30CC330C

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2.5.2.87 MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL Register

2.5.2.87.1 MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL Register (Offset = 29Ch) [reset = 30CC330Ch]

XTAL 32K CLK Divider Value for Temp Sensor.

Return to Summary Table

Table 2-990. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 829Ch

Figure 2-493. MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED		XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR					
NONE		R/W					
0h		30CC330Ch					
23	22	21	20	19	18	17	16
XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR							
R/W							
30CC330Ch							
15	14	13	12	11	10	9	8
XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR							
R/W							
30CC330Ch							
7	6	5	4	3	2	1	0
XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR							
R/W							
30CC330Ch							

Table 2-991. MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR	R/W	30CC330Ch	Divider value for XTAL_32K clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x30C' is required then register should be configured as follows - bits[9:0] = 0x30C bits[19:10] = 0x30C bits[29:20] = 0x30C This configures the register to 0x30CC330C

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2.5.2.88 MSS_RCM_MCAN4_CLK_DIV_VAL Register

2.5.2.88.1 MSS_RCM_MCAN4_CLK_DIV_VAL Register (Offset = 2A4h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-992. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82A4h

Figure 2-494. MSS_RCM_MCAN4_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN4_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN4_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-993. MSS_RCM_MCAN4_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN4_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.89 MSS_RCM_MCAN5_CLK_DIV_VAL Register

2.5.2.89.1 MSS_RCM_MCAN5_CLK_DIV_VAL Register (Offset = 2A8h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-994. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82A8h

Figure 2-495. MSS_RCM_MCAN5_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCAN5_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCAN5_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-995. MSS_RCM_MCAN5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN5_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.90 MSS_RCM_MCAN6_CLK_DIV_VAL Register

2.5.2.90.1 MSS_RCM_MCAN6_CLK_DIV_VAL Register (Offset = 2ACh) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-996. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82ACh

Figure 2-496. MSS_RCM_MCAN6_CLK_DIV_VAL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">MCAN6_CLK_DIV_VAL_CLKDIVR</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">MCAN6_CLK_DIV_VAL_CLKDIVR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 2-997. MSS_RCM_MCAN6_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN6_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.91 MSS_RCM_MCAN7_CLK_DIV_VAL Register

2.5.2.91.1 MSS_RCM_MCAN7_CLK_DIV_VAL Register (Offset = 2B0h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-998. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82B0h

Figure 2-497. MSS_RCM_MCAN7_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MCAN7_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCAN7_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-999. MSS_RCM_MCAN7_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCAN7_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value corresponding MCAN selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.92 MSS_RCM_RTI4_CLK_DIV_VAL Register

2.5.2.92.1 MSS_RCM_RTI4_CLK_DIV_VAL Register (Offset = 2B4h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-1000. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82B4h

Figure 2-498. MSS_RCM_RTI4_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI4_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI4_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1001. MSS_RCM_RTI4_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI4_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.93 MSS_RCM_RTI5_CLK_DIV_VAL Register

2.5.2.93.1 MSS_RCM_RTI5_CLK_DIV_VAL Register (Offset = 2B8h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-1002. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82B8h

Figure 2-499. MSS_RCM_RTI5_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI5_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI5_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1003. MSS_RCM_RTI5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI5_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.94 MSS_RCM_RTI6_CLK_DIV_VAL Register

2.5.2.94.1 MSS_RCM_RTI6_CLK_DIV_VAL Register (Offset = 2BCh) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-1004. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82BCh

Figure 2-500. MSS_RCM_RTI6_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI6_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI6_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1005. MSS_RCM_RTI6_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI6_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.95 MSS_RCM_RTI7_CLK_DIV_VAL Register

2.5.2.95.1 MSS_RCM_RTI7_CLK_DIV_VAL Register (Offset = 2C0h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-1006. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82C0h

Figure 2-501. MSS_RCM_RTI7_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				RTI7_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RTI7_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1007. MSS_RCM_RTI7_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	RTI7_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding RTI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.96 MSS_RCM_MCSPI5_CLK_DIV_VAL Register

2.5.2.96.1 MSS_RCM_MCSPI5_CLK_DIV_VAL Register (Offset = 2C4h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-1008. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82C4h

Figure 2-502. MSS_RCM_MCSPI5_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI5_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI5_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1009. MSS_RCM_MCSPI5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI5_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.97 MSS_RCM_MCSPI6_CLK_DIV_VAL Register

2.5.2.97.1 MSS_RCM_MCSPI6_CLK_DIV_VAL Register (Offset = 2C8h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to Summary Table

Table 2-1010. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82C8h

Figure 2-503. MSS_RCM_MCSPI6_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				MCSPI6_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MCSPI6_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1011. MSS_RCM_MCSPI6_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI6_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.98 MSS_RCM_MCSPI7_CLK_DIV_VAL Register

2.5.2.98.1 MSS_RCM_MCSPI7_CLK_DIV_VAL Register (Offset = 2CCh) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-1012. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82CCh

Figure 2-504. MSS_RCM_MCSPI7_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				MCSPI7_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
MCSPI7_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1013. MSS_RCM_MCSPI7_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	MCSPI7_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value Corresponding SPI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.99 MSS_RCM_MCAN0_CLK_GATE Register

2.5.2.99.1 MSS_RCM_MCAN0_CLK_GATE Register (Offset = 300h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1014. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8300h

Figure 2-505. MSS_RCM_MCAN0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCAN0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1015. MSS_RCM_MCAN0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN0_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.5.2.100 MSS_RCM_MCAN1_CLK_GATE Register

2.5.2.100.1 MSS_RCM_MCAN1_CLK_GATE Register (Offset = 304h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1016. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8304h

Figure 2-506. MSS_RCM_MCAN1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCAN1_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1017. MSS_RCM_MCAN1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN1_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.5.2.101 MSS_RCM_MCAN2_CLK_GATE Register

2.5.2.101.1 MSS_RCM_MCAN2_CLK_GATE Register (Offset = 308h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1018. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8308h

Figure 2-507. MSS_RCM_MCAN2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MCAN2_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1019. MSS_RCM_MCAN2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN2_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.5.2.102 MSS_RCM_MCAN3_CLK_GATE Register

2.5.2.102.1 MSS_RCM_MCAN3_CLK_GATE Register (Offset = 30Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to Summary Table

Table 2-1020. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 830Ch

Figure 2-508. MSS_RCM_MCAN3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCAN3_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1021. MSS_RCM_MCAN3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN3_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.5.2.103 MSS_RCM_OSPI0_CLK_GATE Register

2.5.2.103.1 MSS_RCM_OSPI0_CLK_GATE Register (Offset = 310h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1022. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8310h

Figure 2-509. MSS_RCM_OSPI0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OSPI0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1023. MSS_RCM_OSPI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OSPI0_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for OSPI

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2.5.2.104 MSS_RCM_RTI0_CLK_GATE Register

2.5.2.104.1 MSS_RCM_RTI0_CLK_GATE Register (Offset = 314h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1024. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8314h

Figure 2-510. MSS_RCM_RTI0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1025. MSS_RCM_RTI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI0_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.5.2.105 MSS_RCM_RTI1_CLK_GATE Register

2.5.2.105.1 MSS_RCM_RTI1_CLK_GATE Register (Offset = 318h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1026. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8318h

Figure 2-511. MSS_RCM_RTI1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI1_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1027. MSS_RCM_RTI1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI1_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.5.2.106 MSS_RCM_RTI2_CLK_GATE Register

2.5.2.106.1 MSS_RCM_RTI2_CLK_GATE Register (Offset = 31Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to Summary Table

Table 2-1028. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 831Ch

Figure 2-512. MSS_RCM_RTI2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI2_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1029. MSS_RCM_RTI2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI2_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.5.2.107 MSS_RCM_RTI3_CLK_GATE Register

2.5.2.107.1 MSS_RCM_RTI3_CLK_GATE Register (Offset = 320h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1030. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8320h

Figure 2-513. MSS_RCM_RTI3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI3_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1031. MSS_RCM_RTI3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI3_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.5.2.108 MSS_RCM_WDT0_CLK_GATE Register

2.5.2.108.1 MSS_RCM_WDT0_CLK_GATE Register (Offset = 328h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1032. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8328h

Figure 2-514. MSS_RCM_WDT0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					WDT0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1033. MSS_RCM_WDT0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WDT0_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for WDT

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2.5.2.109 MSS_RCM_WDT1_CLK_GATE Register

2.5.2.109.1 MSS_RCM_WDT1_CLK_GATE Register (Offset = 32Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1034. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 832Ch

Figure 2-515. MSS_RCM_WDT1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WDT1_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1035. MSS_RCM_WDT1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WDT1_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for WDT

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2.5.2.110 MSS_RCM_WDT2_CLK_GATE Register

2.5.2.110.1 MSS_RCM_WDT2_CLK_GATE Register (Offset = 330h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1036. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8330h

Figure 2-516. MSS_RCM_WDT2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WDT2_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1037. MSS_RCM_WDT2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WDT2_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for WDT

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2.5.2.111 MSS_RCM_WDT3_CLK_GATE Register

2.5.2.111.1 MSS_RCM_WDT3_CLK_GATE Register (Offset = 334h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1038. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8334h

Figure 2-517. MSS_RCM_WDT3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					WDT3_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1039. MSS_RCM_WDT3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WDT3_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for WDT

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2.5.2.112 MSS_RCM_MCSPI0_CLK_GATE Register

2.5.2.112.1 MSS_RCM_MCSPI0_CLK_GATE Register (Offset = 33Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1040. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 833Ch

Figure 2-518. MSS_RCM_MCSPI0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MCSPI0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1041. MSS_RCM_MCSPI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI0_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.5.2.113 MSS_RCM_MCSPI1_CLK_GATE Register

2.5.2.113.1 MSS_RCM_MCSPI1_CLK_GATE Register (Offset = 340h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1042. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8340h

Figure 2-519. MSS_RCM_MCSPI1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI1_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1043. MSS_RCM_MCSPI1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI1_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.5.2.114 MSS_RCM_MCSPI2_CLK_GATE Register

2.5.2.114.1 MSS_RCM_MCSPI2_CLK_GATE Register (Offset = 344h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1044. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8344h

Figure 2-520. MSS_RCM_MCSPI2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI2_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1045. MSS_RCM_MCSPI2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI2_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.5.2.115 MSS_RCM_MCSPI3_CLK_GATE Register

2.5.2.115.1 MSS_RCM_MCSPI3_CLK_GATE Register (Offset = 348h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1046. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8348h

Figure 2-521. MSS_RCM_MCSPI3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MCSPI3_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1047. MSS_RCM_MCSPI3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI3_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.5.2.116 MSS_RCM_MCSPI4_CLK_GATE Register

2.5.2.116.1 MSS_RCM_MCSPI4_CLK_GATE Register (Offset = 34Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1048. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 834Ch

Figure 2-522. MSS_RCM_MCSPI4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI4_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1049. MSS_RCM_MCSPI4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI4_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.5.2.117 MSS_RCM_MMC0_CLK_GATE Register

2.5.2.117.1 MSS_RCM_MMC0_CLK_GATE Register (Offset = 350h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1050. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8350h

Figure 2-523. MSS_RCM_MMC0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MMC0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1051. MSS_RCM_MMC0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MMC0_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for MMCSD

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2.5.2.118 MSS_RCM_PRU_ICSS0_UART_CLK_GATE Register

2.5.2.118.1 MSS_RCM_PRU_ICSS0_UART_CLK_GATE Register (Offset = 354h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1052. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8354h

Figure 2-524. MSS_RCM_PRU_ICSS0_UART_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PRU_ICSS0_UART_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1053. MSS_RCM_PRU_ICSS0_UART_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PRU_ICSS0_UART_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for ICSSM_UCLK

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2.5.2.119 MSS_RCM_CPTS_CLK_GATE Register

2.5.2.119.1 MSS_RCM_CPTS_CLK_GATE Register (Offset = 358h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1054. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8358h

Figure 2-525. MSS_RCM_CPTS_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CPTS_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1055. MSS_RCM_CPTS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CPTS_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for CPTS

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2.5.2.120 MSS_RCM_CONTROLSS_PLL_CLK_GATE Register

2.5.2.120.1 MSS_RCM_CONTROLSS_PLL_CLK_GATE Register (Offset = 360h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1056. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8360h

Figure 2-526. MSS_RCM_CONTROLSS_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CONTROLSS_PLL_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1057. MSS_RCM_CONTROLSS_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CONTROLSS_PLL_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for CONTROLSS_PLL

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2.5.2.121 MSS_RCM_I2C0_CLK_GATE Register

2.5.2.121.1 MSS_RCM_I2C0_CLK_GATE Register (Offset = 364h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1058. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8364h

Figure 2-527. MSS_RCM_I2C0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					I2C0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1059. MSS_RCM_I2C0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	I2C0_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for I2C

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2.5.2.122 MSS_RCM_I2C1_CLK_GATE Register

2.5.2.122.1 MSS_RCM_I2C1_CLK_GATE Register (Offset = 368h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1060. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8368h

Figure 2-528. MSS_RCM_I2C1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					I2C1_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1061. MSS_RCM_I2C1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	I2C1_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for I2C

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2.5.2.123 MSS_RCM_I2C2_CLK_GATE Register

2.5.2.123.1 MSS_RCM_I2C2_CLK_GATE Register (Offset = 36Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1062. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 836Ch

Figure 2-529. MSS_RCM_I2C2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					I2C2_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1063. MSS_RCM_I2C2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	I2C2_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for I2C

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2.5.2.124 MSS_RCM_I2C3_CLK_GATE Register

2.5.2.124.1 MSS_RCM_I2C3_CLK_GATE Register (Offset = 370h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1064. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8370h

Figure 2-530. MSS_RCM_I2C3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					I2C3_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1065. MSS_RCM_I2C3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	I2C3_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for I2C

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2.5.2.125 MSS_RCM_LIN0_CLK_GATE Register

2.5.2.125.1 MSS_RCM_LIN0_CLK_GATE Register (Offset = 374h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1066. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8374h

Figure 2-531. MSS_RCM_LIN0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LIN0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1067. MSS_RCM_LIN0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	LIN0_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for SPIB

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2.5.2.126 MSS_RCM_LIN1_CLK_GATE Register

2.5.2.126.1 MSS_RCM_LIN1_CLK_GATE Register (Offset = 378h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1068. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8378h

Figure 2-532. MSS_RCM_LIN1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LIN1_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1069. MSS_RCM_LIN1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	LIN1_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for SPIB

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2.5.2.127 MSS_RCM_LIN2_CLK_GATE Register

2.5.2.127.1 MSS_RCM_LIN2_CLK_GATE Register (Offset = 37Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1070. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 837Ch

Figure 2-533. MSS_RCM_LIN2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LIN2_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1071. MSS_RCM_LIN2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	LIN2_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for SPIB

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2.5.2.128 MSS_RCM_LIN3_CLK_GATE Register

2.5.2.128.1 MSS_RCM_LIN3_CLK_GATE Register (Offset = 380h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1072. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8380h

Figure 2-534. MSS_RCM_LIN3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LIN3_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1073. MSS_RCM_LIN3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	LIN3_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for SPIB

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2.5.2.129 MSS_RCM_LIN4_CLK_GATE Register

2.5.2.129.1 MSS_RCM_LIN4_CLK_GATE Register (Offset = 384h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1074. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8384h

Figure 2-535. MSS_RCM_LIN4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LIN4_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1075. MSS_RCM_LIN4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	LIN4_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for SPIB

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2.5.2.130 MSS_RCM_UART0_CLK_GATE Register

2.5.2.130.1 MSS_RCM_UART0_CLK_GATE Register (Offset = 38Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1076. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 838Ch

Figure 2-536. MSS_RCM_UART0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UART0_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1077. MSS_RCM_UART0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART0_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding UART

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2.5.2.131 MSS_RCM_UART1_CLK_GATE Register

2.5.2.131.1 MSS_RCM_UART1_CLK_GATE Register (Offset = 390h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1078. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8390h

Figure 2-537. MSS_RCM_UART1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					UART1_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1079. MSS_RCM_UART1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART1_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding UART

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2.5.2.132 MSS_RCM_UART2_CLK_GATE Register

2.5.2.132.1 MSS_RCM_UART2_CLK_GATE Register (Offset = 394h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1080. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8394h

Figure 2-538. MSS_RCM_UART2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UART2_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1081. MSS_RCM_UART2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART2_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding UART

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2.5.2.133 MSS_RCM_UART3_CLK_GATE Register

2.5.2.133.1 MSS_RCM_UART3_CLK_GATE Register (Offset = 398h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1082. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8398h

Figure 2-539. MSS_RCM_UART3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UART3_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1083. MSS_RCM_UART3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART3_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding UART

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2.5.2.134 MSS_RCM_UART4_CLK_GATE Register

2.5.2.134.1 MSS_RCM_UART4_CLK_GATE Register (Offset = 39Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1084. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 839Ch

Figure 2-540. MSS_RCM_UART4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UART4_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1085. MSS_RCM_UART4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART4_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding UART

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2.5.2.135 MSS_RCM_UART5_CLK_GATE Register

2.5.2.135.1 MSS_RCM_UART5_CLK_GATE Register (Offset = 3A0h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1086. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83A0h

Figure 2-541. MSS_RCM_UART5_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UART5_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1087. MSS_RCM_UART5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART5_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding UART

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2.5.2.136 MSS_RCM_RGMII_250_CLK_GATE Register

2.5.2.136.1 MSS_RCM_RGMII_250_CLK_GATE Register (Offset = 3A4h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1088. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83A4h

Figure 2-542. MSS_RCM_RGMII_250_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RGMII_250_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1089. MSS_RCM_RGMII_250_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RGMII_250_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for RGMII

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2.5.2.137 MSS_RCM_RGMII_50_CLK_GATE Register

2.5.2.137.1 MSS_RCM_RGMII_50_CLK_GATE Register (Offset = 3A8h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1090. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83A8h

Figure 2-543. MSS_RCM_RGMII_50_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RGMII_50_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1091. MSS_RCM_RGMII_50_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RGMII_50_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for MII100

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2.5.2.138 MSS_RCM_RGMII_5_CLK_GATE Register

2.5.2.138.1 MSS_RCM_RGMII_5_CLK_GATE Register (Offset = 3ACh) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1092. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83ACh

Figure 2-544. MSS_RCM_RGMII_5_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RGMII_5_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1093. MSS_RCM_RGMII_5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RGMII_5_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for MII10

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2.5.2.139 MSS_RCM_MMC0_32K_CLK_GATE Register

2.5.2.139.1 MSS_RCM_MMC0_32K_CLK_GATE Register (Offset = 3B0h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1094. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83B0h

Figure 2-545. MSS_RCM_MMC0_32K_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MMC0_32K_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1095. MSS_RCM_MMC0_32K_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MMC0_32K_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for MMCSD_32K

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2.5.2.140 MSS_RCM_TEMPSENSE_32K_CLK_GATE Register

2.5.2.140.1 MSS_RCM_TEMPSENSE_32K_CLK_GATE Register (Offset = 3B4h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1096. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83B4h

Figure 2-546. MSS_RCM_TEMPSENSE_32K_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TEMPSENSE_32K_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1097. MSS_RCM_TEMPSENSE_32K_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TEMPSENSE_32K_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for TEMPSENSE_32K

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2.5.2.141 MSS_RCM_CPSW_CLK_GATE Register

2.5.2.141.1 MSS_RCM_CPSW_CLK_GATE Register (Offset = 3B8h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1098. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83B8h

Figure 2-547. MSS_RCM_CPSW_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CPSW_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1099. MSS_RCM_CPSW_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CPSW_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for CPSW CPPI

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2.5.2.142 MSS_RCM_PRU_ICSS0_IEP_CLK_GATE Register

2.5.2.142.1 MSS_RCM_PRU_ICSS0_IEP_CLK_GATE Register (Offset = 3BCh) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1100. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83BCh

Figure 2-548. MSS_RCM_PRU_ICSS0_IEP_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					PRU_ICSS0_IEP_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1101. MSS_RCM_PRU_ICSS0_IEP_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PRU_ICSS0_IEP_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for ICSSM_IEP

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2.5.2.143 MSS_RCM_PRU_ICSS0_CORE_CLK_GATE Register

2.5.2.143.1 MSS_RCM_PRU_ICSS0_CORE_CLK_GATE Register (Offset = 3C0h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1102. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83C0h

Figure 2-549. MSS_RCM_PRU_ICSS0_CORE_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PRU_ICSS0_CORE_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1103. MSS_RCM_PRU_ICSS0_CORE_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PRU_ICSS0_CORE_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for ICSSM_CORE

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2.5.2.144 MSS_RCM_MSS_PRU_ICSS_SYS_CLK_GATE Register

2.5.2.144.1 MSS_RCM_MSS_PRU_ICSS_SYS_CLK_GATE Register (Offset = 3C4h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1104. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83C4h

Figure 2-550. MSS_RCM_MSS_PRU_ICSS_SYS_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSS_PRU_ICSS_SYS_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1105. MSS_RCM_MSS_PRU_ICSS_SYS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSS_PRU_ICSS_SYS_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for ICSSM_SYS

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2.5.2.145 MSS_RCM_R5SS0_CORE0_GATE Register

2.5.2.145.1 MSS_RCM_R5SS0_CORE0_GATE Register (Offset = 3CCh) [reset = 0h]

Clock gating for individual CPU core.

Return to Summary Table

Table 2-1106. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83CCh

Figure 2-551. MSS_RCM_R5SS0_CORE0_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CORE0_GATE_CLKGATE		
NONE					R/W		
0h					0h		

Table 2-1107. MSS_RCM_R5SS0_CORE0_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CORE0_GATE_CLKGATE	R/W	0h	Writing 3'b111 will gate clock to CORE0 related peripherals inside Cortexr5ss

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2.5.2.146 MSS_RCM_R5SS1_CORE0_GATE Register

2.5.2.146.1 MSS_RCM_R5SS1_CORE0_GATE Register (Offset = 3D0h) [reset = 0h]

Clock gating for individual CPU core.

Return to Summary Table

Table 2-1108. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83D0h

Figure 2-552. MSS_RCM_R5SS1_CORE0_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CORE0_GATE_CLKGATE		
NONE					R/W		
0h					0h		

Table 2-1109. MSS_RCM_R5SS1_CORE0_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CORE0_GATE_CLKGATE	R/W	0h	Writing 3'b111 will gate clock to CORE0 related peripherals inside Cortexr5ss

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2.5.2.147 MSS_RCM_R5SS0_CORE1_GATE Register

2.5.2.147.1 MSS_RCM_R5SS0_CORE1_GATE Register (Offset = 3D4h) [reset = 0h]

Clock gating for individual CPU core.

Return to Summary Table

Table 2-1110. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83D4h

Figure 2-553. MSS_RCM_R5SS0_CORE1_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CORE1_GATE_CLKGATE		
NONE					R/W		
0h					0h		

Table 2-1111. MSS_RCM_R5SS0_CORE1_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CORE1_GATE_CLKGATE	R/W	0h	Writing 3'b111 will gate clock to CORE1 related peripherals inside Cortexr5ss

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2.5.2.148 MSS_RCM_R5SS1_CORE1_GATE Register

2.5.2.148.1 MSS_RCM_R5SS1_CORE1_GATE Register (Offset = 3D8h) [reset = 0h]

Clock gating for individual CPU core.

Return to Summary Table

Table 2-1112. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83D8h

Figure 2-554. MSS_RCM_R5SS1_CORE1_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CORE1_GATE_CLKGATE		
NONE					R/W		
0h					0h		

Table 2-1113. MSS_RCM_R5SS1_CORE1_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CORE1_GATE_CLKGATE	R/W	0h	Writing 3'b111 will gate clock to CORE1 related peripherals inside Cortexr5ss

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2.5.2.149 MSS_RCM_MSS_MCAN4_CLK_GATE Register

2.5.2.149.1 MSS_RCM_MSS_MCAN4_CLK_GATE Register (Offset = 3DCh) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to Summary Table

Table 2-1114. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83DCh

Figure 2-555. MSS_RCM_MSS_MCAN4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSS_MCAN4_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1115. MSS_RCM_MSS_MCAN4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSS_MCAN4_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.5.2.150 MSS_RCM_MSS_MCAN5_CLK_GATE Register

2.5.2.150.1 MSS_RCM_MSS_MCAN5_CLK_GATE Register (Offset = 3E0h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to Summary Table

Table 2-1116. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83E0h

Figure 2-556. MSS_RCM_MSS_MCAN5_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MSS_MCAN5_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1117. MSS_RCM_MSS_MCAN5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSS_MCAN5_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.5.2.151 MSS_RCM_MSS_MCAN6_CLK_GATE Register

2.5.2.151.1 MSS_RCM_MSS_MCAN6_CLK_GATE Register (Offset = 3E4h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to Summary Table

Table 2-1118. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83E4h

Figure 2-557. MSS_RCM_MSS_MCAN6_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSS_MCAN6_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1119. MSS_RCM_MSS_MCAN6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSS_MCAN6_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.5.2.152 MSS_RCM_MSS_MCAN7_CLK_GATE Register

2.5.2.152.1 MSS_RCM_MSS_MCAN7_CLK_GATE Register (Offset = 3E8h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to Summary Table

Table 2-1120. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83E8h

Figure 2-558. MSS_RCM_MSS_MCAN7_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MSS_MCAN7_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1121. MSS_RCM_MSS_MCAN7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MSS_MCAN7_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.5.2.153 MSS_RCM_RTI4_CLK_GATE Register

2.5.2.153.1 MSS_RCM_RTI4_CLK_GATE Register (Offset = 3ECh) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to Summary Table

Table 2-1122. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83ECh

Figure 2-559. MSS_RCM_RTI4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI4_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1123. MSS_RCM_RTI4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI4_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.5.2.154 MSS_RCM_RTI5_CLK_GATE Register

2.5.2.154.1 MSS_RCM_RTI5_CLK_GATE Register (Offset = 3F0h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to Summary Table

Table 2-1124. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83F0h

Figure 2-560. MSS_RCM_RTI5_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI5_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1125. MSS_RCM_RTI5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI5_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.5.2.155 MSS_RCM_RTI6_CLK_GATE Register

2.5.2.155.1 MSS_RCM_RTI6_CLK_GATE Register (Offset = 3F4h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to Summary Table

Table 2-1126. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83F4h

Figure 2-561. MSS_RCM_RTI6_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI6_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1127. MSS_RCM_RTI6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI6_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.5.2.156 MSS_RCM_RTI7_CLK_GATE Register

2.5.2.156.1 MSS_RCM_RTI7_CLK_GATE Register (Offset = 3F8h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1128. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83F8h

Figure 2-562. MSS_RCM_RTI7_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI7_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1129. MSS_RCM_RTI7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI7_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.5.2.157 MSS_RCM_MCAN0_CLK_STATUS Register

2.5.2.157.1 MSS_RCM_MCAN0_CLK_STATUS Register (Offset = 400h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1130. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8400h

Figure 2-563. MSS_RCM_MCAN0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCAN0_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCAN0_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1131. MSS_RCM_MCAN0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCAN0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN
7:0	MCAN0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN based on one hot encoding technique.

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2.5.2.158 MSS_RCM_MCAN1_CLK_STATUS Register

2.5.2.158.1 MSS_RCM_MCAN1_CLK_STATUS Register (Offset = 404h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1132. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8404h

Figure 2-564. MSS_RCM_MCAN1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCAN1_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCAN1_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1133. MSS_RCM_MCAN1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCAN1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN
7:0	MCAN1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN based on one hot encoding technique.

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2.5.2.159 MSS_RCM_MCAN2_CLK_STATUS Register

2.5.2.159.1 MSS_RCM_MCAN2_CLK_STATUS Register (Offset = 408h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1134. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8408h

Figure 2-565. MSS_RCM_MCAN2_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCAN2_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCAN2_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1135. MSS_RCM_MCAN2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCAN2_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN
7:0	MCAN2_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN based on one hot encoding technique.

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2.5.2.160 MSS_RCM_MCAN3_CLK_STATUS Register

2.5.2.160.1 MSS_RCM_MCAN3_CLK_STATUS Register (Offset = 40Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1136. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 840Ch

Figure 2-566. MSS_RCM_MCAN3_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCAN3_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCAN3_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1137. MSS_RCM_MCAN3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCAN3_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN
7:0	MCAN3_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN based on one hot encoding technique.

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2.5.2.161 MSS_RCM_OSPI0_CLK_STATUS Register

2.5.2.161.1 MSS_RCM_OSPI0_CLK_STATUS Register (Offset = 410h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1138. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8410h

Figure 2-567. MSS_RCM_OSPI0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OSPI0_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
OSPI0_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1139. MSS_RCM_OSPI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	OSPI0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for OSPI
7:0	OSPI0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for OSPI based on one hot encoding technique.

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2.5.2.162 MSS_RCM_RTI0_CLK_STATUS Register

2.5.2.162.1 MSS_RCM_RTI0_CLK_STATUS Register (Offset = 414h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1140. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8414h

Figure 2-568. MSS_RCM_RTI0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RTI0_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
RTI0_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1141. MSS_RCM_RTI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RTI0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI
7:0	RTI0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI based on one hot encoding technique.

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2.5.2.163 MSS_RCM_RTI1_CLK_STATUS Register

2.5.2.163.1 MSS_RCM_RTI1_CLK_STATUS Register (Offset = 418h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

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Table 2-1142. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8418h

Figure 2-569. MSS_RCM_RTI1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RTI1_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
RTI1_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1143. MSS_RCM_RTI1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RTI1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI
7:0	RTI1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI based on one hot encoding technique.

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2.5.2.164 MSS_RCM_RTI2_CLK_STATUS Register

2.5.2.164.1 MSS_RCM_RTI2_CLK_STATUS Register (Offset = 41Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1144. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 841Ch

Figure 2-570. MSS_RCM_RTI2_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RTI2_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
RTI2_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1145. MSS_RCM_RTI2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RTI2_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI
7:0	RTI2_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI based on one hot encoding technique.

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2.5.2.165 MSS_RCM_RTI3_CLK_STATUS Register

2.5.2.165.1 MSS_RCM_RTI3_CLK_STATUS Register (Offset = 420h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1146. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8420h

Figure 2-571. MSS_RCM_RTI3_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RTI3_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
RTI3_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1147. MSS_RCM_RTI3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RTI3_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI
7:0	RTI3_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI based on one hot encoding technique.

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2.5.2.166 MSS_RCM_WDT0_CLK_STATUS Register

2.5.2.166.1 MSS_RCM_WDT0_CLK_STATUS Register (Offset = 428h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1148. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8428h

Figure 2-572. MSS_RCM_WDT0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
WDT0_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
WDT0_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1149. MSS_RCM_WDT0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	WDT0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for WDT
7:0	WDT0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for WDT based on one hot encoding technique.

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2.5.2.167 MSS_RCM_WDT1_CLK_STATUS Register

2.5.2.167.1 MSS_RCM_WDT1_CLK_STATUS Register (Offset = 42Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1150. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 842Ch

Figure 2-573. MSS_RCM_WDT1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
WDT1_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
WDT1_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1151. MSS_RCM_WDT1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	WDT1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for WDT
7:0	WDT1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for WDT based on one hot encoding technique.

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2.5.2.168 MSS_RCM_WDT2_CLK_STATUS Register

2.5.2.168.1 MSS_RCM_WDT2_CLK_STATUS Register (Offset = 430h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1152. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8430h

Figure 2-574. MSS_RCM_WDT2_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
WDT2_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
WDT2_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1153. MSS_RCM_WDT2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	WDT2_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for WDT
7:0	WDT2_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for WDT based on one hot encoding technique.

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2.5.2.169 MSS_RCM_WDT3_CLK_STATUS Register

2.5.2.169.1 MSS_RCM_WDT3_CLK_STATUS Register (Offset = 434h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1154. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8434h

Figure 2-575. MSS_RCM_WDT3_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
WDT3_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
WDT3_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1155. MSS_RCM_WDT3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	WDT3_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for WDT
7:0	WDT3_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for WDT based on one hot encoding technique.

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2.5.2.170 MSS_RCM_MCSPI0_CLK_STATUS Register

2.5.2.170.1 MSS_RCM_MCSPI0_CLK_STATUS Register (Offset = 43Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1156. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 843Ch

Figure 2-576. MSS_RCM_MCSPI0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCSPI0_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCSPI0_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1157. MSS_RCM_MCSPI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCSPI0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI
7:0	MCSPI0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI based on one hot encoding technique.

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2.5.2.171 MSS_RCM_MCSPI1_CLK_STATUS Register

2.5.2.171.1 MSS_RCM_MCSPI1_CLK_STATUS Register (Offset = 440h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1158. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8440h

Figure 2-577. MSS_RCM_MCSPI1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCSPI1_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCSPI1_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1159. MSS_RCM_MCSPI1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCSPI1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI
7:0	MCSPI1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI based on one hot encoding technique.

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2.5.2.172 MSS_RCM_MCSPI2_CLK_STATUS Register

2.5.2.172.1 MSS_RCM_MCSPI2_CLK_STATUS Register (Offset = 444h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1160. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8444h

Figure 2-578. MSS_RCM_MCSPI2_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCSPI2_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCSPI2_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1161. MSS_RCM_MCSPI2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCSPI2_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI
7:0	MCSPI2_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI based on one hot encoding technique.

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2.5.2.173 MSS_RCM_MCSPI3_CLK_STATUS Register

2.5.2.173.1 MSS_RCM_MCSPI3_CLK_STATUS Register (Offset = 448h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1162. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8448h

Figure 2-579. MSS_RCM_MCSPI3_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCSPI3_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCSPI3_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1163. MSS_RCM_MCSPI3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCSPI3_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI
7:0	MCSPI3_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI based on one hot encoding technique.

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2.5.2.174 MSS_RCM_MCSPI4_CLK_STATUS Register

2.5.2.174.1 MSS_RCM_MCSPI4_CLK_STATUS Register (Offset = 44Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1164. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 844Ch

Figure 2-580. MSS_RCM_MCSPI4_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCSPI4_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCSPI4_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1165. MSS_RCM_MCSPI4_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCSPI4_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI
7:0	MCSPI4_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI based on one hot encoding technique.

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2.5.2.175 MSS_RCM_MMC0_CLK_STATUS Register

2.5.2.175.1 MSS_RCM_MMC0_CLK_STATUS Register (Offset = 450h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1166. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8450h

Figure 2-581. MSS_RCM_MMC0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MMC0_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MMC0_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1167. MSS_RCM_MMC0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MMC0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for MMCSD
7:0	MMC0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for MMCSD based on one hot encoding technique.

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2.5.2.176 MSS_RCM_PRU_ICSS0_UART_CLK_STATUS Register

2.5.2.176.1 MSS_RCM_PRU_ICSS0_UART_CLK_STATUS Register (Offset = 454h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1168. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8454h

Figure 2-582. MSS_RCM_PRU_ICSS0_UART_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PRU_ICSS0_UART_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
PRU_ICSS0_UART_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1169. MSS_RCM_PRU_ICSS0_UART_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PRU_ICSS0_UART_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for ICSSM_UCLK
7:0	PRU_ICSS0_UART_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for ICSSM_UCLK based on one hot encoding technique.

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2.5.2.177 MSS_RCM_CPTS_CLK_STATUS Register

2.5.2.177.1 MSS_RCM_CPTS_CLK_STATUS Register (Offset = 458h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1170. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8458h

Figure 2-583. MSS_RCM_CPTS_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CPTS_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
CPTS_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1171. MSS_RCM_CPTS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	CPTS_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for CPTS
7:0	CPTS_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for CPTS based on one hot encoding technique.

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2.5.2.178 MSS_RCM_CONTROLSS_PLL_CLK_STATUS Register

2.5.2.178.1 MSS_RCM_CONTROLSS_PLL_CLK_STATUS Register (Offset = 460h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1172. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8460h

Figure 2-584. MSS_RCM_CONTROLSS_PLL_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CONTROLSS_PLL_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CONTROLSS_PLL_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1173. MSS_RCM_CONTROLSS_PLL_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	CONTROLSS_PLL_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for CONTROLSS_PLL
7:0	CONTROLSS_PLL_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for CONTROLSS_PLL based on one hot encoding technique.

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2.5.2.179 MSS_RCM_I2C_CLK_STATUS Register

2.5.2.179.1 MSS_RCM_I2C_CLK_STATUS Register (Offset = 464h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1174. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8464h

Figure 2-585. MSS_RCM_I2C_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
I2C_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1175. MSS_RCM_I2C_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	I2C_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for I2C
7:0	I2C_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for I2C based on one hot encoding technique.

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2.5.2.180 MSS_RCM_LIN0_UART0_CLK_STATUS Register

2.5.2.180.1 MSS_RCM_LIN0_UART0_CLK_STATUS Register (Offset = 474h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1176. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8474h

Figure 2-586. MSS_RCM_LIN0_UART0_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
LIN0_UART0_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
LIN0_UART0_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1177. MSS_RCM_LIN0_UART0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	LIN0_UART0_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN
7:0	LIN0_UART0_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN based on one hot encoding technique.

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2.5.2.181 MSS_RCM_LIN1_UART1_CLK_STATUS Register

2.5.2.181.1 MSS_RCM_LIN1_UART1_CLK_STATUS Register (Offset = 478h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1178. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8478h

Figure 2-587. MSS_RCM_LIN1_UART1_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
LIN1_UART1_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
LIN1_UART1_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1179. MSS_RCM_LIN1_UART1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	LIN1_UART1_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN
7:0	LIN1_UART1_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN based on one hot encoding technique.

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2.5.2.182 MSS_RCM_LIN2_UART2_CLK_STATUS Register

2.5.2.182.1 MSS_RCM_LIN2_UART2_CLK_STATUS Register (Offset = 47Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1180. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 847Ch

Figure 2-588. MSS_RCM_LIN2_UART2_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
LIN2_UART2_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
LIN2_UART2_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1181. MSS_RCM_LIN2_UART2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	LIN2_UART2_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN
7:0	LIN2_UART2_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN based on one hot encoding technique.

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2.5.2.183 MSS_RCM_LIN3_UART3_CLK_STATUS Register

2.5.2.183.1 MSS_RCM_LIN3_UART3_CLK_STATUS Register (Offset = 480h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1182. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8480h

Figure 2-589. MSS_RCM_LIN3_UART3_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
LIN3_UART3_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
LIN3_UART3_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1183. MSS_RCM_LIN3_UART3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	LIN3_UART3_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN
7:0	LIN3_UART3_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN based on one hot encoding technique.

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2.5.2.184 MSS_RCM_LIN4_UART4_CLK_STATUS Register

2.5.2.184.1 MSS_RCM_LIN4_UART4_CLK_STATUS Register (Offset = 484h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1184. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8484h

Figure 2-590. MSS_RCM_LIN4_UART4_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
LIN4_UART4_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
LIN4_UART4_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1185. MSS_RCM_LIN4_UART4_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	LIN4_UART4_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN
7:0	LIN4_UART4_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN based on one hot encoding technique.

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2.5.2.185 MSS_RCM_LIN5_UART5_CLK_STATUS Register

2.5.2.185.1 MSS_RCM_LIN5_UART5_CLK_STATUS Register (Offset = 488h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1186. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8488h

Figure 2-591. MSS_RCM_LIN5_UART5_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
LIN5_UART5_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
LIN5_UART5_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1187. MSS_RCM_LIN5_UART5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	LIN5_UART5_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding UART and LIN
7:0	LIN5_UART5_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding UART and LIN based on one hot encoding technique.

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2.5.2.186 MSS_RCM_RGMII_250_CLK_STATUS Register

2.5.2.186.1 MSS_RCM_RGMII_250_CLK_STATUS Register (Offset = 48Ch) [reset = 100h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1188. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 848Ch

Figure 2-592. MSS_RCM_RGMII_250_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RGMII_250_CLK_STATUS_CURRDIVIDER							
R							
1h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 2-1189. MSS_RCM_RGMII_250_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RGMII_250_CLK_STATUS_CURRDIVIDER	R	1h	Status shows the current divider value choosen for RGMII
7:0	RESERVED	NONE	0h	Reserved

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2.5.2.187 MSS_RCM_RGMII_50_CLK_STATUS Register

2.5.2.187.1 MSS_RCM_RGMII_50_CLK_STATUS Register (Offset = 490h) [reset = 900h]

RGMII_50_CLK_STATUS.

Return to Summary Table

Table 2-1190. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8490h

Figure 2-593. MSS_RCM_RGMII_50_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RGMII_50_CLK_STATUS_CURRDIVIDER							
R							
9h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 2-1191. MSS_RCM_RGMII_50_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RGMII_50_CLK_STATUS_CURRDIVIDER	R	9h	Status shows the current divider value choosen for MII100
7:0	RESERVED	NONE	0h	Reserved

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2.5.2.188 MSS_RCM_RGMII_5_CLK_STATUS Register

2.5.2.188.1 MSS_RCM_RGMII_5_CLK_STATUS Register (Offset = 494h) [reset = 6300h]

RGMII_5_CLK_STATUS.

Return to Summary Table

Table 2-1192. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8494h

Figure 2-594. MSS_RCM_RGMII_5_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RGMII_5_CLK_STATUS_CURRDIVIDER							
R							
63h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 2-1193. MSS_RCM_RGMII_5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RGMII_5_CLK_STATUS_CURRDIVIDER	R	63h	Status shows the current divider value choosen for MII10
7:0	RESERVED	NONE	0h	Reserved

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2.5.2.189 MSS_RCM_MMC0_32K_CLK_STATUS Register

2.5.2.189.1 MSS_RCM_MMC0_32K_CLK_STATUS Register (Offset = 49Ch) [reset = 30C00h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1194. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 849Ch

Figure 2-595. MSS_RCM_MMC0_32K_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						MMC0_32K_CLK_STATUS_CURRDIVIDER	
NONE						R	
0h						30Ch	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MMC0_32K_CLK_STATUS_CURRDIVIDER							
R							
30Ch							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 2-1195. MSS_RCM_MMC0_32K_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	MMC0_32K_CLK_STATUS_CURRDIVIDER	R	30Ch	Status shows the current divider value choosen for XTAL_32K
7:0	RESERVED	NONE	0h	Reserved

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2.5.2.190 MSS_RCM_TEMPSENSE_32K_CLK_STATUS Register

2.5.2.190.1 MSS_RCM_TEMPSENSE_32K_CLK_STATUS Register (Offset = 4A0h) [reset = 30C00h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1196. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84A0h

Figure 2-596. MSS_RCM_TEMPSENSE_32K_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						TEMPSENSE_32K_CLK_STATUS_CURRDIVIDER	
NONE						R	
0h						30Ch	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TEMPSENSE_32K_CLK_STATUS_CURRDIVIDER							
R							
30Ch							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 2-1197. MSS_RCM_TEMPSENSE_32K_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	TEMPSENSE_32K_CLK_STATUS_CURRDIVIDER	R	30Ch	Status shows the current divider value choosen for XTAL_32K
7:0	RESERVED	NONE	0h	Reserved

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2.5.2.191 MSS_RCM_MCAN4_CLK_STATUS Register

2.5.2.191.1 MSS_RCM_MCAN4_CLK_STATUS Register (Offset = 4A8h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1198. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84A8h

Figure 2-597. MSS_RCM_MCAN4_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCAN4_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCAN4_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1199. MSS_RCM_MCAN4_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCAN4_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN
7:0	MCAN4_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN based on one hot encoding technique.

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2.5.2.192 MSS_RCM_MCAN5_CLK_STATUS Register

2.5.2.192.1 MSS_RCM_MCAN5_CLK_STATUS Register (Offset = 4ACh) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1200. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84ACh

Figure 2-598. MSS_RCM_MCAN5_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCAN5_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCAN5_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1201. MSS_RCM_MCAN5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCAN5_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN
7:0	MCAN5_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN based on one hot encoding technique.

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2.5.2.193 MSS_RCM_MCAN6_CLK_STATUS Register

2.5.2.193.1 MSS_RCM_MCAN6_CLK_STATUS Register (Offset = 4B0h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1202. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84B0h

Figure 2-599. MSS_RCM_MCAN6_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCAN6_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCAN6_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1203. MSS_RCM_MCAN6_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCAN6_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN
7:0	MCAN6_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN based on one hot encoding technique.

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2.5.2.194 MSS_RCM_MCAN7_CLK_STATUS Register

2.5.2.194.1 MSS_RCM_MCAN7_CLK_STATUS Register (Offset = 4B4h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1204. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84B4h

Figure 2-600. MSS_RCM_MCAN7_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCAN7_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCAN7_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1205. MSS_RCM_MCAN7_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCAN7_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for corresponding MCAN
7:0	MCAN7_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for corresponding MCAN based on one hot encoding technique.

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2.5.2.195 MSS_RCM_RTI4_CLK_STATUS Register

2.5.2.195.1 MSS_RCM_RTI4_CLK_STATUS Register (Offset = 4B8h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1206. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84B8h

Figure 2-601. MSS_RCM_RTI4_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RTI4_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
RTI4_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1207. MSS_RCM_RTI4_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RTI4_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI
7:0	RTI4_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI based on one hot encoding technique.

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2.5.2.196 MSS_RCM_RTI5_CLK_STATUS Register

2.5.2.196.1 MSS_RCM_RTI5_CLK_STATUS Register (Offset = 4BCh) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1208. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84BCh

Figure 2-602. MSS_RCM_RTI5_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RTI5_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
RTI5_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1209. MSS_RCM_RTI5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RTI5_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI
7:0	RTI5_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI based on one hot encoding technique.

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2.5.2.197 MSS_RCM_RTI6_CLK_STATUS Register

2.5.2.197.1 MSS_RCM_RTI6_CLK_STATUS Register (Offset = 4C0h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1210. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84C0h

Figure 2-603. MSS_RCM_RTI6_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RTI6_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
RTI6_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1211. MSS_RCM_RTI6_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RTI6_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI
7:0	RTI6_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI based on one hot encoding technique.

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2.5.2.198 MSS_RCM_RTI7_CLK_STATUS Register

2.5.2.198.1 MSS_RCM_RTI7_CLK_STATUS Register (Offset = 4C4h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1212. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84C4h

Figure 2-604. MSS_RCM_RTI7_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RTI7_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
RTI7_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1213. MSS_RCM_RTI7_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	RTI7_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding RTI
7:0	RTI7_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding RTI based on one hot encoding technique.

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2.5.2.199 MSS_RCM_MCSPI5_CLK_STATUS Register

2.5.2.199.1 MSS_RCM_MCSPI5_CLK_STATUS Register (Offset = 4C8h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1214. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84C8h

Figure 2-605. MSS_RCM_MCSPI5_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCSPI5_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCSPI5_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1215. MSS_RCM_MCSPI5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCSPI5_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI
7:0	MCSPI5_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI based on one hot encoding technique.

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2.5.2.200 MSS_RCM_MCSPI6_CLK_STATUS Register

2.5.2.200.1 MSS_RCM_MCSPI6_CLK_STATUS Register (Offset = 4CCh) [reset = 1h]

Clock source selection and Divider Value of respective clock.

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Table 2-1216. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84CCh

Figure 2-606. MSS_RCM_MCSPI6_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCSPI6_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCSPI6_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1217. MSS_RCM_MCSPI6_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCSPI6_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI
7:0	MCSPI6_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI based on one hot encoding technique.

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2.5.2.201 MSS_RCM_MCSPI7_CLK_STATUS Register

2.5.2.201.1 MSS_RCM_MCSPI7_CLK_STATUS Register (Offset = 4D0h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to Summary Table

Table 2-1218. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84D0h

Figure 2-607. MSS_RCM_MCSPI7_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MCSPI7_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
MCSPI7_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1219. MSS_RCM_MCSPI7_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MCSPI7_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for Corresponding SPI
7:0	MCSPI7_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for Corresponding SPI based on one hot encoding technique.

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2.5.2.202 MSS_RCM_R5SS0_POR_RST_CTRL Register

2.5.2.202.1 MSS_RCM_R5SS0_POR_RST_CTRL Register (Offset = 500h) [reset = 0h]

R5SS POR Reset.

Return to Summary Table

Table 2-1220. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8500h

Figure 2-608. MSS_RCM_R5SS0_POR_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_POR_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1221. MSS_RCM_R5SS0_POR_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_POR_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: Writing 3'b111 will assert por reset to R5SS Read is always 000

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2.5.2.203 MSS_RCM_R5SS1_POR_RST_CTRL Register

2.5.2.203.1 MSS_RCM_R5SS1_POR_RST_CTRL Register (Offset = 504h) [reset = 0h]

R5SS POR Reset.

Return to Summary Table

Table 2-1222. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8504h

Figure 2-609. MSS_RCM_R5SS1_POR_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_POR_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1223. MSS_RCM_R5SS1_POR_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_POR_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: Writing 3'b111 will assert por reset to R5SS Read is always 000

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2.5.2.204 MSS_RCM_R5SS0_CORE0_GRST_CTRL Register

2.5.2.204.1 MSS_RCM_R5SS0_CORE0_GRST_CTRL Register (Offset = 508h) [reset = 0h]

Core 0 Global Reset.

Return to Summary Table

Table 2-1224. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8508h

Figure 2-610. MSS_RCM_R5SS0_CORE0_GRST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CORE0_GRST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1225. MSS_RCM_R5SS0_CORE0_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CORE0_GRST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: Writing 3'b111 will reset CORE0 and MSS_CORE0_VIM

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2.5.2.205 MSS_RCM_R5SS1_CORE0_GRST_CTRL Register

2.5.2.205.1 MSS_RCM_R5SS1_CORE0_GRST_CTRL Register (Offset = 50Ch) [reset = 0h]

Core 0 Global Reset.

Return to Summary Table

Table 2-1226. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 850Ch

Figure 2-611. MSS_RCM_R5SS1_CORE0_GRST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CORE0_GRST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1227. MSS_RCM_R5SS1_CORE0_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CORE0_GRST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: Writing 3'b111 will reset CORE0 and MSS_CORE0_VIM

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2.5.2.206 MSS_RCM_R5SS0_CORE1_GRST_CTRL Register

2.5.2.206.1 MSS_RCM_R5SS0_CORE1_GRST_CTRL Register (Offset = 510h) [reset = 0h]

Core 1 Global Reset.

Return to Summary Table

Table 2-1228. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8510h

Figure 2-612. MSS_RCM_R5SS0_CORE1_GRST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CORE1_GRST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1229. MSS_RCM_R5SS0_CORE1_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CORE1_GRST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: Writing 3'b111 will reset CORE1 and MSS_CORE1_VIM

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2.5.2.207 MSS_RCM_R5SS1_CORE1_GRST_CTRL Register

2.5.2.207.1 MSS_RCM_R5SS1_CORE1_GRST_CTRL Register (Offset = 514h) [reset = 0h]

Core 1 Global Reset.

Return to Summary Table

Table 2-1230. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8514h

Figure 2-613. MSS_RCM_R5SS1_CORE1_GRST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CORE1_GRST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1231. MSS_RCM_R5SS1_CORE1_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CORE1_GRST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: Writing 3'b111 will reset CORE1 and MSS_CORE1_VIM

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2.5.2.208 MSS_RCM_R5SS0_CORE0_LRST_CTRL Register

2.5.2.208.1 MSS_RCM_R5SS0_CORE0_LRST_CTRL Register (Offset = 518h) [reset = 0h]

Core 0 Local Reset.

Return to Summary Table

Table 2-1232. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8518h

Figure 2-614. MSS_RCM_R5SS0_CORE0_LRST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_CORE0_LRST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1233. MSS_RCM_R5SS0_CORE0_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CORE0_LRST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: Writing 3'b111 will reset CORE0 only

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2.5.2.209 MSS_RCM_R5SS1_CORE0_LRST_CTRL Register

2.5.2.209.1 MSS_RCM_R5SS1_CORE0_LRST_CTRL Register (Offset = 51Ch) [reset = 0h]

Core 0 Local Reset.

Return to Summary Table

Table 2-1234. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 851Ch

Figure 2-615. MSS_RCM_R5SS1_CORE0_LRST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CORE0_LRST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1235. MSS_RCM_R5SS1_CORE0_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CORE0_LRST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: Writing 3'b111 will reset CORE0 only

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2.5.2.210 MSS_RCM_R5SS0_CORE1_LRST_CTRL Register

2.5.2.210.1 MSS_RCM_R5SS0_CORE1_LRST_CTRL Register (Offset = 520h) [reset = 0h]

Core 1 Local Reset.

Return to Summary Table

Table 2-1236. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8520h

Figure 2-616. MSS_RCM_R5SS0_CORE1_LRST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS0_CORE1_LRST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1237. MSS_RCM_R5SS0_CORE1_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_CORE1_LRST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: Writing 3'b111 will reset CORE1 only

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2.5.2.211 MSS_RCM_R5SS1_CORE1_LRST_CTRL Register

2.5.2.211.1 MSS_RCM_R5SS1_CORE1_LRST_CTRL Register (Offset = 524h) [reset = 0h]

Core 1 Local Reset.

Return to Summary Table

Table 2-1238. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8524h

Figure 2-617. MSS_RCM_R5SS1_CORE1_LRST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_CORE1_LRST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1239. MSS_RCM_R5SS1_CORE1_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_CORE1_LRST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. write pulse bit field: Writing 3'b111 will reset CORE1 only

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2.5.2.212 MSS_RCM_R5SS0_VIM0_RST_CTRL Register

2.5.2.212.1 MSS_RCM_R5SS0_VIM0_RST_CTRL Register (Offset = 528h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1240. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8528h

Figure 2-618. MSS_RCM_R5SS0_VIM0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS0_VIM0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1241. MSS_RCM_R5SS0_VIM0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_VIM0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE0_VIM Writing 3'b000 will deassert the reset

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2.5.2.213 MSS_RCM_R5SS1_VIM0_RST_CTRL Register

2.5.2.213.1 MSS_RCM_R5SS1_VIM0_RST_CTRL Register (Offset = 52Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1242. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 852Ch

Figure 2-619. MSS_RCM_R5SS1_VIM0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					R5SS1_VIM0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1243. MSS_RCM_R5SS1_VIM0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_VIM0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE0_VIM Writing 3'b000 will deassert the reset

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2.5.2.214 MSS_RCM_R5SS0_VIM1_RST_CTRL Register

2.5.2.214.1 MSS_RCM_R5SS0_VIM1_RST_CTRL Register (Offset = 530h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1244. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8530h

Figure 2-620. MSS_RCM_R5SS0_VIM1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS0_VIM1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1245. MSS_RCM_R5SS0_VIM1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS0_VIM1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE1_VIM

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2.5.2.215 MSS_RCM_R5SS1_VIM1_RST_CTRL Register

2.5.2.215.1 MSS_RCM_R5SS1_VIM1_RST_CTRL Register (Offset = 534h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1246. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8534h

Figure 2-621. MSS_RCM_R5SS1_VIM1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					R5SS1_VIM1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1247. MSS_RCM_R5SS1_VIM1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	R5SS1_VIM1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE1_VIM

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2.5.2.216 MSS_RCM_MCRC0_RST_CTRL Register

2.5.2.216.1 MSS_RCM_MCRC0_RST_CTRL Register (Offset = 538h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1248. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8538h

Figure 2-622. MSS_RCM_MCRC0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCRC0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1249. MSS_RCM_MCRC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCRC0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MCRC

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2.5.2.217 MSS_RCM_RTI0_RST_CTRL Register

2.5.2.217.1 MSS_RCM_RTI0_RST_CTRL Register (Offset = 53Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1250. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 853Ch

Figure 2-623. MSS_RCM_RTI0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					RTI0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1251. MSS_RCM_RTI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.5.2.218 MSS_RCM_RTI1_RST_CTRL Register

2.5.2.218.1 MSS_RCM_RTI1_RST_CTRL Register (Offset = 540h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1252. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8540h

Figure 2-624. MSS_RCM_RTI1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1253. MSS_RCM_RTI1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.5.2.219 MSS_RCM_RTI2_RST_CTRL Register

2.5.2.219.1 MSS_RCM_RTI2_RST_CTRL Register (Offset = 544h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1254. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8544h

Figure 2-625. MSS_RCM_RTI2_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI2_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1255. MSS_RCM_RTI2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.5.2.220 MSS_RCM_RTI3_RST_CTRL Register

2.5.2.220.1 MSS_RCM_RTI3_RST_CTRL Register (Offset = 548h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1256. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8548h

Figure 2-626. MSS_RCM_RTI3_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI3_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1257. MSS_RCM_RTI3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.5.2.221 MSS_RCM_WDT0_RST_CTRL Register

2.5.2.221.1 MSS_RCM_WDT0_RST_CTRL Register (Offset = 54Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1258. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 854Ch

Figure 2-627. MSS_RCM_WDT0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					WDT0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1259. MSS_RCM_WDT0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WDT0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset WDT

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2.5.2.222 MSS_RCM_WDT1_RST_CTRL Register

2.5.2.222.1 MSS_RCM_WDT1_RST_CTRL Register (Offset = 550h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1260. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8550h

Figure 2-628. MSS_RCM_WDT1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WDT1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1261. MSS_RCM_WDT1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WDT1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset WDT

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2.5.2.223 MSS_RCM_WDT2_RST_CTRL Register

2.5.2.223.1 MSS_RCM_WDT2_RST_CTRL Register (Offset = 554h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1262. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8554h

Figure 2-629. MSS_RCM_WDT2_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WDT2_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1263. MSS_RCM_WDT2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WDT2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset WDT

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2.5.2.224 MSS_RCM_WDT3_RST_CTRL Register

2.5.2.224.1 MSS_RCM_WDT3_RST_CTRL Register (Offset = 558h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1264. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8558h

Figure 2-630. MSS_RCM_WDT3_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					WDT3_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1265. MSS_RCM_WDT3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	WDT3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset WDT

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2.5.2.225 MSS_RCM_TOP_ESM_RST_CTRL Register

2.5.2.225.1 MSS_RCM_TOP_ESM_RST_CTRL Register (Offset = 55Ch) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1266. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 855Ch

Figure 2-631. MSS_RCM_TOP_ESM_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TOP_ESM_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1267. MSS_RCM_TOP_ESM_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TOP_ESM_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset ESM

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2.5.2.226 MSS_RCM_DCC0_RST_CTRL Register

2.5.2.226.1 MSS_RCM_DCC0_RST_CTRL Register (Offset = 560h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1268. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8560h

Figure 2-632. MSS_RCM_DCC0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DCC0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1269. MSS_RCM_DCC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DCC0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCC0

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2.5.2.227 MSS_RCM_DCC1_RST_CTRL Register

2.5.2.227.1 MSS_RCM_DCC1_RST_CTRL Register (Offset = 564h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1270. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8564h

Figure 2-633. MSS_RCM_DCC1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DCC1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1271. MSS_RCM_DCC1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DCC1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCC1

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2.5.2.228 MSS_RCM_DCC2_RST_CTRL Register

2.5.2.228.1 MSS_RCM_DCC2_RST_CTRL Register (Offset = 568h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1272. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8568h

Figure 2-634. MSS_RCM_DCC2_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DCC2_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1273. MSS_RCM_DCC2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DCC2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCC2

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2.5.2.229 MSS_RCM_DCC3_RST_CTRL Register

2.5.2.229.1 MSS_RCM_DCC3_RST_CTRL Register (Offset = 56Ch) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1274. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 856Ch

Figure 2-635. MSS_RCM_DCC3_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DCC3_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1275. MSS_RCM_DCC3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DCC3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCC3

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2.5.2.230 MSS_RCM_MCSPI0_RST_CTRL Register

2.5.2.230.1 MSS_RCM_MCSPI0_RST_CTRL Register (Offset = 570h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1276. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8570h

Figure 2-636. MSS_RCM_MCSPI0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1277. MSS_RCM_MCSPI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.5.2.231 MSS_RCM_MCSPI1_RST_CTRL Register

2.5.2.231.1 MSS_RCM_MCSPI1_RST_CTRL Register (Offset = 574h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1278. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8574h

Figure 2-637. MSS_RCM_MCSPI1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1279. MSS_RCM_MCSPI1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.5.2.232 MSS_RCM_MCSPI2_RST_CTRL Register

2.5.2.232.1 MSS_RCM_MCSPI2_RST_CTRL Register (Offset = 578h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1280. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8578h

Figure 2-638. MSS_RCM_MCSPI2_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI2_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1281. MSS_RCM_MCSPI2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.5.2.233 MSS_RCM_MCSPI3_RST_CTRL Register

2.5.2.233.1 MSS_RCM_MCSPI3_RST_CTRL Register (Offset = 57Ch) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1282. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 857Ch

Figure 2-639. MSS_RCM_MCSPI3_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI3_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1283. MSS_RCM_MCSPI3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.5.2.234 MSS_RCM_MCSPI4_RST_CTRL Register

2.5.2.234.1 MSS_RCM_MCSPI4_RST_CTRL Register (Offset = 580h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1284. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8580h

Figure 2-640. MSS_RCM_MCSPI4_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI4_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1285. MSS_RCM_MCSPI4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI4_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.5.2.235 MSS_RCM_OSPI0_RST_CTRL Register

2.5.2.235.1 MSS_RCM_OSPI0_RST_CTRL Register (Offset = 584h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1286. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8584h

Figure 2-641. MSS_RCM_OSPI0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OSPI0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1287. MSS_RCM_OSPI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OSPI0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset OSPI

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2.5.2.236 MSS_RCM_MCAN0_RST_CTRL Register

2.5.2.236.1 MSS_RCM_MCAN0_RST_CTRL Register (Offset = 588h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1288. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8588h

Figure 2-642. MSS_RCM_MCAN0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCAN0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1289. MSS_RCM_MCAN0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.5.2.237 MSS_RCM_MCAN1_RST_CTRL Register

2.5.2.237.1 MSS_RCM_MCAN1_RST_CTRL Register (Offset = 58Ch) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1290. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 858Ch

Figure 2-643. MSS_RCM_MCAN1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCAN1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1291. MSS_RCM_MCAN1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.5.2.238 MSS_RCM_MCAN2_RST_CTRL Register

2.5.2.238.1 MSS_RCM_MCAN2_RST_CTRL Register (Offset = 590h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1292. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8590h

Figure 2-644. MSS_RCM_MCAN2_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCAN2_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1293. MSS_RCM_MCAN2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.5.2.239 MSS_RCM_MCAN3_RST_CTRL Register

2.5.2.239.1 MSS_RCM_MCAN3_RST_CTRL Register (Offset = 594h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1294. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8594h

Figure 2-645. MSS_RCM_MCAN3_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCAN3_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1295. MSS_RCM_MCAN3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.5.2.240 MSS_RCM_I2C0_RST_CTRL Register

2.5.2.240.1 MSS_RCM_I2C0_RST_CTRL Register (Offset = 598h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1296. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8598h

Figure 2-646. MSS_RCM_I2C0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					I2C0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1297. MSS_RCM_I2C0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	I2C0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C

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2.5.2.241 MSS_RCM_I2C1_RST_CTRL Register

2.5.2.241.1 MSS_RCM_I2C1_RST_CTRL Register (Offset = 59Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1298. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 859Ch

Figure 2-647. MSS_RCM_I2C1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					I2C1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1299. MSS_RCM_I2C1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	I2C1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C

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2.5.2.242 MSS_RCM_I2C2_RST_CTRL Register

2.5.2.242.1 MSS_RCM_I2C2_RST_CTRL Register (Offset = 5A0h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1300. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85A0h

Figure 2-648. MSS_RCM_I2C2_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					I2C2_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1301. MSS_RCM_I2C2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	I2C2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C

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2.5.2.243 MSS_RCM_I2C3_RST_CTRL Register

2.5.2.243.1 MSS_RCM_I2C3_RST_CTRL Register (Offset = 5A4h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1302. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85A4h

Figure 2-649. MSS_RCM_I2C3_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					I2C3_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1303. MSS_RCM_I2C3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	I2C3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C

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2.5.2.244 MSS_RCM_UART0_RST_CTRL Register

2.5.2.244.1 MSS_RCM_UART0_RST_CTRL Register (Offset = 5A8h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1304. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85A8h

Figure 2-650. MSS_RCM_UART0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					UART0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1305. MSS_RCM_UART0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.5.2.245 MSS_RCM_UART1_RST_CTRL Register

2.5.2.245.1 MSS_RCM_UART1_RST_CTRL Register (Offset = 5ACh) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1306. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85ACh

Figure 2-651. MSS_RCM_UART1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UART1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1307. MSS_RCM_UART1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.5.2.246 MSS_RCM_UART2_RST_CTRL Register

2.5.2.246.1 MSS_RCM_UART2_RST_CTRL Register (Offset = 5B0h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1308. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85B0h

Figure 2-652. MSS_RCM_UART2_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					UART2_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1309. MSS_RCM_UART2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.5.2.247 MSS_RCM_UART3_RST_CTRL Register

2.5.2.247.1 MSS_RCM_UART3_RST_CTRL Register (Offset = 5B4h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1310. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85B4h

Figure 2-653. MSS_RCM_UART3_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					UART3_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1311. MSS_RCM_UART3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.5.2.248 MSS_RCM_UART4_RST_CTRL Register

2.5.2.248.1 MSS_RCM_UART4_RST_CTRL Register (Offset = 5B8h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1312. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85B8h

Figure 2-654. MSS_RCM_UART4_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					UART4_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1313. MSS_RCM_UART4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART4_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.5.2.249 MSS_RCM_UART5_RST_CTRL Register

2.5.2.249.1 MSS_RCM_UART5_RST_CTRL Register (Offset = 5BCh) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1314. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85BCh

Figure 2-655. MSS_RCM_UART5_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UART5_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1315. MSS_RCM_UART5_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UART5_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.5.2.250 MSS_RCM_LIN0_RST_CTRL Register

2.5.2.250.1 MSS_RCM_LIN0_RST_CTRL Register (Offset = 5C0h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1316. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85C0h

Figure 2-656. MSS_RCM_LIN0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LIN0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1317. MSS_RCM_LIN0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	LIN0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset LIN

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2.5.2.251 MSS_RCM_LIN1_RST_CTRL Register

2.5.2.251.1 MSS_RCM_LIN1_RST_CTRL Register (Offset = 5C4h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1318. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85C4h

Figure 2-657. MSS_RCM_LIN1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LIN1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1319. MSS_RCM_LIN1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	LIN1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset LIN

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2.5.2.252 MSS_RCM_LIN2_RST_CTRL Register

2.5.2.252.1 MSS_RCM_LIN2_RST_CTRL Register (Offset = 5C8h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1320. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85C8h

Figure 2-658. MSS_RCM_LIN2_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LIN2_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1321. MSS_RCM_LIN2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	LIN2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset LIN

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2.5.2.253 MSS_RCM_LIN3_RST_CTRL Register

2.5.2.253.1 MSS_RCM_LIN3_RST_CTRL Register (Offset = 5CCh) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1322. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85CCh

Figure 2-659. MSS_RCM_LIN3_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					LIN3_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1323. MSS_RCM_LIN3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	LIN3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset LIN

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2.5.2.254 MSS_RCM_LIN4_RST_CTRL Register

2.5.2.254.1 MSS_RCM_LIN4_RST_CTRL Register (Offset = 5D0h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1324. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85D0h

Figure 2-660. MSS_RCM_LIN4_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					LIN4_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1325. MSS_RCM_LIN4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	LIN4_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset LIN

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2.5.2.255 MSS_RCM_EDMA_RST_CTRL Register

2.5.2.255.1 MSS_RCM_EDMA_RST_CTRL Register (Offset = 5D8h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1326. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85D8h

Figure 2-661. MSS_RCM_EDMA_RST_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="3">EDMA_RST_CTRL_TPTCA1_ASSERT</td><td>RESERVED</td><td colspan="3">EDMA_RST_CTRL_TPTCA0_ASSERT</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="3">EDMA_RST_CTRL_TPCCA_ASSERT</td><td>RESERVED</td><td colspan="3">EDMA_RST_CTRL_ASSERT</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 2-1327. MSS_RCM_EDMA_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED	NONE	0h	Reserved
14:12	EDMA_RST_CTRL_TPTCA1_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_TPTCA1
11	RESERVED	NONE	0h	Reserved
10:8	EDMA_RST_CTRL_TPTCA0_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_TPTCA0
7	RESERVED	NONE	0h	Reserved
6:4	EDMA_RST_CTRL_TPCCA_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_TPCCA
3	RESERVED	NONE	0h	Reserved
2:0	EDMA_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset EDMA

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2.5.2.256 MSS_RCM_INFRA_RST_CTRL Register

2.5.2.256.1 MSS_RCM_INFRA_RST_CTRL Register (Offset = 5DCh) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1328. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85DCh

Figure 2-662. MSS_RCM_INFRA_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INFRA_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1329. MSS_RCM_INFRA_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INFRA_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS INFRA

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2.5.2.257 MSS_RCM_CPSW_RST_CTRL Register

2.5.2.257.1 MSS_RCM_CPSW_RST_CTRL Register (Offset = 5E0h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1330. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85E0h

Figure 2-663. MSS_RCM_CPSW_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CPSW_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1331. MSS_RCM_CPSW_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CPSW_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS CPSW

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2.5.2.258 MSS_RCM_PRU_ICSS0_RST_CTRL Register

2.5.2.258.1 MSS_RCM_PRU_ICSS0_RST_CTRL Register (Offset = 5E4h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1332. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85E4h

Figure 2-664. MSS_RCM_PRU_ICSS0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					PRU_ICSS0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1333. MSS_RCM_PRU_ICSS0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	PRU_ICSS0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS ICSSM

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2.5.2.259 MSS_RCM_MMC0_RST_CTRL Register

2.5.2.259.1 MSS_RCM_MMC0_RST_CTRL Register (Offset = 5E8h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1334. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85E8h

Figure 2-665. MSS_RCM_MMC0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MMC0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1335. MSS_RCM_MMC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MMC0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MMCSD

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2.5.2.260 MSS_RCM_GPIO0_RST_CTRL Register

2.5.2.260.1 MSS_RCM_GPIO0_RST_CTRL Register (Offset = 5ECh) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1336. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85ECh

Figure 2-666. MSS_RCM_GPIO0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					GPIO0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1337. MSS_RCM_GPIO0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	GPIO0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO

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2.5.2.261 MSS_RCM_GPIO1_RST_CTRL Register

2.5.2.261.1 MSS_RCM_GPIO1_RST_CTRL Register (Offset = 5F0h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1338. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85F0h

Figure 2-667. MSS_RCM_GPIO1_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					GPIO1_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1339. MSS_RCM_GPIO1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	GPIO1_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO

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2.5.2.262 MSS_RCM_GPIO2_RST_CTRL Register

2.5.2.262.1 MSS_RCM_GPIO2_RST_CTRL Register (Offset = 5F4h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1340. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85F4h

Figure 2-668. MSS_RCM_GPIO2_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					GPIO2_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1341. MSS_RCM_GPIO2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	GPIO2_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO

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2.5.2.263 MSS_RCM_GPIO3_RST_CTRL Register

2.5.2.263.1 MSS_RCM_GPIO3_RST_CTRL Register (Offset = 5F8h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1342. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85F8h

Figure 2-669. MSS_RCM_GPIO3_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					GPIO3_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1343. MSS_RCM_GPIO3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	GPIO3_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO

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2.5.2.264 MSS_RCM_SPINLOCK0_RST_CTRL Register

2.5.2.264.1 MSS_RCM_SPINLOCK0_RST_CTRL Register (Offset = 5FCh) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1344. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85FCh

Figure 2-670. MSS_RCM_SPINLOCK0_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					SPINLOCK0_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1345. MSS_RCM_SPINLOCK0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	SPINLOCK0_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset SPINLOCK

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2.5.2.265 MSS_RCM_TEMPSENSE_32K_RST_CTRL Register

2.5.2.265.1 MSS_RCM_TEMPSENSE_32K_RST_CTRL Register (Offset = 604h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1346. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8604h

Figure 2-671. MSS_RCM_TEMPSENSE_32K_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TEMPSENSE_32K_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1347. MSS_RCM_TEMPSENSE_32K_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TEMPSENSE_32K_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset TEMPSENSE **Note: This bit will only be reset by PORz.

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2.5.2.266 MSS_RCM_MCAN4_RST_CTRL Register

2.5.2.266.1 MSS_RCM_MCAN4_RST_CTRL Register (Offset = 60Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1348. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 860Ch

Figure 2-672. MSS_RCM_MCAN4_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCAN4_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1349. MSS_RCM_MCAN4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN4_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.5.2.267 MSS_RCM_MCAN5_RST_CTRL Register

2.5.2.267.1 MSS_RCM_MCAN5_RST_CTRL Register (Offset = 610h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1350. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8610h

Figure 2-673. MSS_RCM_MCAN5_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCAN5_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1351. MSS_RCM_MCAN5_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN5_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.5.2.268 MSS_RCM_MCAN6_RST_CTRL Register

2.5.2.268.1 MSS_RCM_MCAN6_RST_CTRL Register (Offset = 614h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1352. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8614h

Figure 2-674. MSS_RCM_MCAN6_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MCAN6_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1353. MSS_RCM_MCAN6_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN6_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.5.2.269 MSS_RCM_MCAN7_RST_CTRL Register

2.5.2.269.1 MSS_RCM_MCAN7_RST_CTRL Register (Offset = 618h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1354. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8618h

Figure 2-675. MSS_RCM_MCAN7_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCAN7_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1355. MSS_RCM_MCAN7_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCAN7_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.5.2.270 MSS_RCM_RTI4_RST_CTRL Register

2.5.2.270.1 MSS_RCM_RTI4_RST_CTRL Register (Offset = 61Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1356. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 861Ch

Figure 2-676. MSS_RCM_RTI4_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI4_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1357. MSS_RCM_RTI4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI4_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.5.2.271 MSS_RCM_RTI5_RST_CTRL Register

2.5.2.271.1 MSS_RCM_RTI5_RST_CTRL Register (Offset = 620h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1358. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8620h

Figure 2-677. MSS_RCM_RTI5_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI5_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1359. MSS_RCM_RTI5_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI5_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.5.2.272 MSS_RCM_RTI6_RST_CTRL Register

2.5.2.272.1 MSS_RCM_RTI6_RST_CTRL Register (Offset = 624h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1360. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8624h

Figure 2-678. MSS_RCM_RTI6_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI6_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1361. MSS_RCM_RTI6_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI6_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.5.2.273 MSS_RCM_RTI7_RST_CTRL Register

2.5.2.273.1 MSS_RCM_RTI7_RST_CTRL Register (Offset = 628h) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1362. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8628h

Figure 2-679. MSS_RCM_RTI7_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RTI7_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1363. MSS_RCM_RTI7_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RTI7_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.5.2.274 MSS_RCM_MCSPI5_RST_CTRL Register

2.5.2.274.1 MSS_RCM_MCSPI5_RST_CTRL Register (Offset = 62Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to Summary Table

Table 2-1364. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 862Ch

Figure 2-680. MSS_RCM_MCSPI5_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI5_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1365. MSS_RCM_MCSPI5_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI5_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.5.2.275 MSS_RCM_MCSPI6_RST_CTRL Register

2.5.2.275.1 MSS_RCM_MCSPI6_RST_CTRL Register (Offset = 630h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1366. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8630h

Figure 2-681. MSS_RCM_MCSPI6_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI6_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1367. MSS_RCM_MCSPI6_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI6_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.5.2.276 MSS_RCM_MCSPI7_RST_CTRL Register

2.5.2.276.1 MSS_RCM_MCSPI7_RST_CTRL Register (Offset = 634h) [reset = 0h]

This register is used to Reset respective IP.

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Table 2-1368. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8634h

Figure 2-682. MSS_RCM_MCSPI7_RST_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI7_RST_CTRL_ASSERT		
NONE					R/W		
0h					0h		

Table 2-1369. MSS_RCM_MCSPI7_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI7_RST_CTRL_ASSERT	R/W	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.5.2.277 MSS_RCM_MSS_L2_BANK0_PD_CTRL Register

2.5.2.277.1 MSS_RCM_MSS_L2_BANK0_PD_CTRL Register (Offset = 700h) [reset = 770h]

S/W control to Powers down the L2 Bank 0 and disconnect from Interconnect. AON AGOOD 0 or ISO =1 causes bus disconnect.

Return to Summary Table

Table 2-1370. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8700h

Figure 2-683. MSS_RCM_MSS_L2_BANK0_PD_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					MSS_L2_BANK0_PD_CTRL_AGOODIN		
NONE					R/W		
0h					7h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	MSS_L2_BANK0_PD_CTRL_AONIN			RESERVED	MSS_L2_BANK0_PD_CTRL_ISO		
NONE	R/W			NONE	R/W		
0h	7h			0h	0h		

Table 2-1371. MSS_RCM_MSS_L2_BANK0_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	MSS_L2_BANK0_PD_CTRL_AGOODIN	R/W	7h	SW control for power signal 'AGOODIN' for MSS_L2_BANK0
7	RESERVED	NONE	0h	Reserved
6:4	MSS_L2_BANK0_PD_CTRL_AONIN	R/W	7h	SW control for power signal 'AONIN' for MSS_L2_BANK0
3	RESERVED	NONE	0h	Reserved
2:0	MSS_L2_BANK0_PD_CTRL_ISO	R/W	0h	SW control for power signal 'ISO' for MSS_L2_BANK0.

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2.5.2.278 MSS_RCM_MSS_L2_BANK1_PD_CTRL Register

2.5.2.278.1 MSS_RCM_MSS_L2_BANK1_PD_CTRL Register (Offset = 704h) [reset = 770h]

S/W control to Powers down the L2 Bank 1 and disconnect from Interconnect.

Return to Summary Table

Table 2-1372. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8704h

Figure 2-684. MSS_RCM_MSS_L2_BANK1_PD_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					MSS_L2_BANK1_PD_CTRL_AGOODIN		
NONE					R/W		
0h					7h		
7	6	5	4	3	2	1	0
RESERVED	MSS_L2_BANK1_PD_CTRL_AONIN			RESERVED	MSS_L2_BANK1_PD_CTRL_ISO		
NONE	R/W			NONE	R/W		
0h	7h			0h	0h		

Table 2-1373. MSS_RCM_MSS_L2_BANK1_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	MSS_L2_BANK1_PD_CTRL_AGOODIN	R/W	7h	SW control for power signal 'AGOODIN' for MSS_L2_BANK1
7	RESERVED	NONE	0h	Reserved
6:4	MSS_L2_BANK1_PD_CTRL_AONIN	R/W	7h	SW control for power signal 'AONIN' for MSS_L2_BANK1
3	RESERVED	NONE	0h	Reserved
2:0	MSS_L2_BANK1_PD_CTRL_ISO	R/W	0h	SW control for power signal 'ISO' for MSS_L2_BANK1

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2.5.2.279 MSS_RCM_MSS_L2_BANK2_PD_CTRL Register

2.5.2.279.1 MSS_RCM_MSS_L2_BANK2_PD_CTRL Register (Offset = 708h) [reset = 770h]

S/W control to Powers down the L2 Bank 2 and disconnect from Interconnect.

Return to Summary Table

Table 2-1374. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8708h

Figure 2-685. MSS_RCM_MSS_L2_BANK2_PD_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					MSS_L2_BANK2_PD_CTRL_AGOODIN		
NONE					R/W		
0h					7h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	MSS_L2_BANK2_PD_CTRL_AONIN			RESERVED	MSS_L2_BANK2_PD_CTRL_ISO		
NONE	R/W			NONE	R/W		
0h	7h			0h	0h		

Table 2-1375. MSS_RCM_MSS_L2_BANK2_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	MSS_L2_BANK2_PD_CTRL_AGOODIN	R/W	7h	SW control for power signal 'AGOODIN' for MSS_L2_BANK2
7	RESERVED	NONE	0h	Reserved
6:4	MSS_L2_BANK2_PD_CTRL_AONIN	R/W	7h	SW control for power signal 'AONIN' for MSS_L2_BANK2
3	RESERVED	NONE	0h	Reserved
2:0	MSS_L2_BANK2_PD_CTRL_ISO	R/W	0h	SW control for power signal 'ISO' for MSS_L2_BANK2

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2.5.2.280 MSS_RCM_MSS_L2_BANK3_PD_CTRL Register

2.5.2.280.1 MSS_RCM_MSS_L2_BANK3_PD_CTRL Register (Offset = 70Ch) [reset = 770h]

S/W control to Powers down the L2 Bank 3 and disconnect from Interconnect.

Return to Summary Table

Table 2-1376. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 870Ch

Figure 2-686. MSS_RCM_MSS_L2_BANK3_PD_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">MSS_L2_BANK3_PD_CTRL_AGOODIN</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">7h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="3">MSS_L2_BANK3_PD_CTRL_AONIN</td><td>RESERVED</td><td colspan="3">MSS_L2_BANK3_PD_CTRL_ISO</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 2-1377. MSS_RCM_MSS_L2_BANK3_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	MSS_L2_BANK3_PD_CTRL_AGOODIN	R/W	7h	SW control for power signal 'AGOODIN' for MSS_L2_BANK3
7	RESERVED	NONE	0h	Reserved
6:4	MSS_L2_BANK3_PD_CTRL_AONIN	R/W	7h	SW control for power signal 'AONIN' for MSS_L2_BANK3
3	RESERVED	NONE	0h	Reserved
2:0	MSS_L2_BANK3_PD_CTRL_ISO	R/W	0h	SW control for power signal 'ISO' for MSS_L2_BANK3

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2.5.2.281 MSS_RCM_MSS_L2_BANK0_PD_STATUS Register

2.5.2.281.1 MSS_RCM_MSS_L2_BANK0_PD_STATUS Register (Offset = 710h) [reset = 3h]

L2 Bank PD status. Pgood out observation.

Return to Summary Table

Table 2-1378. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8710h

Figure 2-687. MSS_RCM_MSS_L2_BANK0_PD_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MSS_L2_BANK0_PD_STATUS_AGOODOUT	MSS_L2_BANK0_PD_STATUS_AONOUT
NONE						R	R
0h						1h	1h

Table 2-1379. MSS_RCM_MSS_L2_BANK0_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MSS_L2_BANK0_PD_STATUS_AGOODOUT	R	1h	SW status indicating the 'pgoodin' of MSS_L2_BANK0
0	MSS_L2_BANK0_PD_STATUS_AONOUT	R	1h	SW status indicating the 'ponin' of MSS_L2_BANK0

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2.5.2.282 MSS_RCM_MSS_L2_BANK1_PD_STATUS Register

2.5.2.282.1 MSS_RCM_MSS_L2_BANK1_PD_STATUS Register (Offset = 714h) [reset = 3h]

L2 Bank PD status. Pgood out observation.

Return to Summary Table

Table 2-1380. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8714h

Figure 2-688. MSS_RCM_MSS_L2_BANK1_PD_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MSS_L2_BANK1_PD_STATUS_AGOODOUT	MSS_L2_BANK1_PD_STATUS_AONOUT
NONE						R	R
0h						1h	1h

Table 2-1381. MSS_RCM_MSS_L2_BANK1_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MSS_L2_BANK1_PD_STATUS_AGOODOUT	R	1h	SW status indicating the 'pgoodin' of MSS_L2_BANK1
0	MSS_L2_BANK1_PD_STATUS_AONOUT	R	1h	SW status indicating the 'ponin' of MSS_L2_BANK1

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2.5.2.283 MSS_RCM_MSS_L2_BANK2_PD_STATUS Register

2.5.2.283.1 MSS_RCM_MSS_L2_BANK2_PD_STATUS Register (Offset = 718h) [reset = 3h]

L2 Bank PD status. Pgood out observation.

Return to Summary Table

Table 2-1382. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8718h

Figure 2-689. MSS_RCM_MSS_L2_BANK2_PD_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						MSS_L2_BANK2_PD_STATUS_AGOODOUT	MSS_L2_BANK2_PD_STATUS_AONOUT
NONE						R	R
0h						1h	1h

Table 2-1383. MSS_RCM_MSS_L2_BANK2_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MSS_L2_BANK2_PD_STATUS_AGOODOUT	R	1h	SW status indicating the 'pgoodin' of MSS_L2_BANK2
0	MSS_L2_BANK2_PD_STATUS_AONOUT	R	1h	SW status indicating the 'ponin' of MSS_L2_BANK2

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2.5.2.284 MSS_RCM_MSS_L2_BANK3_PD_STATUS Register

2.5.2.284.1 MSS_RCM_MSS_L2_BANK3_PD_STATUS Register (Offset = 71Ch) [reset = 3h]

L2 Bank PD status. Pgood out observation.

Return to Summary Table

Table 2-1384. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 871Ch

Figure 2-690. MSS_RCM_MSS_L2_BANK3_PD_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						MSS_L2_BANK3_PD_STATUS_AGOODOUT	MSS_L2_BANK3_PD_STATUS_AONOUT
NONE						R	R
0h						1h	1h

Table 2-1385. MSS_RCM_MSS_L2_BANK3_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MSS_L2_BANK3_PD_STATUS_AGOODOUT	R	1h	SW status indicating the 'pgoodin' of MSS_L2_BANK3
0	MSS_L2_BANK3_PD_STATUS_AONOUT	R	1h	SW status indicating the 'ponin' of MSS_L2_BANK3

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2.5.2.285 MSS_RCM_L2OCRAM_BANK4_PD_CTRL Register

2.5.2.285.1 MSS_RCM_L2OCRAM_BANK4_PD_CTRL Register (Offset = 730h) [reset = 770h]

S/W control to Powers down the L2 Bank 4 and disconnect from Interconnect.

Return to Summary Table

Table 2-1386. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8730h

Figure 2-691. MSS_RCM_L2OCRAM_BANK4_PD_CTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">L2OCRAM_BANK4_PD_CTRL_AGOODIN</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">7h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="3">L2OCRAM_BANK4_PD_CTRL_AONIN</td><td>RESERVED</td><td colspan="3">L2OCRAM_BANK4_PD_CTRL_ISO</td></tr>
<tr><td>NONE</td><td colspan="3">R/W</td><td>NONE</td><td colspan="3">R/W</td></tr>
<tr><td>0h</td><td colspan="3">7h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 2-1387. MSS_RCM_L2OCRAM_BANK4_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	L2OCRAM_BANK4_PD_CTRL_AGOODIN	R/W	7h	SW control for power signal 'AGOODIN' for MSS_L2_BANKE
7	RESERVED	NONE	0h	Reserved
6:4	L2OCRAM_BANK4_PD_CTRL_AONIN	R/W	7h	SW control for power signal 'AONIN' for MSS_L2_BANKE
3	RESERVED	NONE	0h	Reserved
2:0	L2OCRAM_BANK4_PD_CTRL_ISO	R/W	0h	SW control for power signal 'ISO' for MSS_L2_BANKE

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2.5.2.286 MSS_RCM_L2OCRAM_BANK5_PD_CTRL Register

2.5.2.286.1 MSS_RCM_L2OCRAM_BANK5_PD_CTRL Register (Offset = 734h) [reset = 770h]

S/W control to Powers down the L2 Bank 5 and disconnect from Interconnect.

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Table 2-1388. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8734h

Figure 2-692. MSS_RCM_L2OCRAM_BANK5_PD_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					L2OCRAM_BANK5_PD_CTRL_AGOODIN		
NONE					R/W		
0h					7h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	L2OCRAM_BANK5_PD_CTRL_AONIN			RESERVED	L2OCRAM_BANK5_PD_CTRL_ISO		
NONE	R/W			NONE	R/W		
0h	7h			0h	0h		

Table 2-1389. MSS_RCM_L2OCRAM_BANK5_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:8	L2OCRAM_BANK5_PD_CTRL_AGOODIN	R/W	7h	SW control for power signal 'AGOODIN' for MSS_L2_BANKF
7	RESERVED	NONE	0h	Reserved
6:4	L2OCRAM_BANK5_PD_CTRL_AONIN	R/W	7h	SW control for power signal 'AONIN' for MSS_L2_BANKF
3	RESERVED	NONE	0h	Reserved
2:0	L2OCRAM_BANK5_PD_CTRL_ISO	R/W	0h	SW control for power signal 'ISO' for MSS_L2_BANKF

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2.5.2.287 MSS_RCM_L2OCRAM_BANK4_PD_STATUS Register

2.5.2.287.1 MSS_RCM_L2OCRAM_BANK4_PD_STATUS Register (Offset = 738h) [reset = 3h]

L2 Bank PD status. Pgood out observation.

Return to Summary Table

Table 2-1390. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8738h

Figure 2-693. MSS_RCM_L2OCRAM_BANK4_PD_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						L2OCRAM_BANK4_PD_STATUS_AGOODOUT	L2OCRAM_BANK4_PD_STATUS_AONOUT
NONE						R	R
0h						1h	1h

Table 2-1391. MSS_RCM_L2OCRAM_BANK4_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	L2OCRAM_BANK4_PD_STATUS_AGOODOUT	R	1h	SW status indicating the 'pgoodin' of MSS_L2_BANKE
0	L2OCRAM_BANK4_PD_STATUS_AONOUT	R	1h	SW status indicating the 'ponin' of MSS_L2_BANKE

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2.5.2.288 MSS_RCM_L2OCRAM_BANK5_PD_STATUS Register

2.5.2.288.1 MSS_RCM_L2OCRAM_BANK5_PD_STATUS Register (Offset = 73Ch) [reset = 3h]

L2 Bank PD status. Pgood out observation.

Return to Summary Table

Table 2-1392. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 873Ch

Figure 2-694. MSS_RCM_L2OCRAM_BANK5_PD_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						L2OCRAM_BANK5_PD_STATUS_AGOODOUT	L2OCRAM_BANK5_PD_STATUS_AONOUT
NONE						R	R
0h						1h	1h

Table 2-1393. MSS_RCM_L2OCRAM_BANK5_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	L2OCRAM_BANK5_PD_STATUS_AGOODOUT	R	1h	SW status indicating the 'pgoodin' of MSS_L2_BANKF
0	L2OCRAM_BANK5_PD_STATUS_AONOUT	R	1h	SW status indicating the 'ponin' of MSS_L2_BANKF

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2.5.2.289 MSS_RCM_HSM_RTIA_CLK_SRC_SEL Register

2.5.2.289.1 MSS_RCM_HSM_RTIA_CLK_SRC_SEL Register (Offset = 800h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to Summary Table

Table 2-1394. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8800h

Figure 2-695. MSS_RCM_HSM_RTIA_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				HSM_RTIA_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HSM_RTIA_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-1395. MSS_RCM_HSM_RTIA_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	HSM_RTIA_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for HSM_Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - XTALCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - RCCLK10M 0x555 - RCCLK10M 0x666 - EXT_REFCLK 0x777 - RCCLK32K

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2.5.2.290 MSS_RCM_HSM_WDT_CLK_SRC_SEL Register

2.5.2.290.1 MSS_RCM_HSM_WDT_CLK_SRC_SEL Register (Offset = 804h) [reset = 555h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-1396. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8804h

Figure 2-696. MSS_RCM_HSM_WDT_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				HSM_WDT_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				555h			
7	6	5	4	3	2	1	0
HSM_WDT_CLK_SRC_SEL_CLKSRCSEL							
R/W							
555h							

Table 2-1397. MSS_RCM_HSM_WDT_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	HSM_WDT_CLK_SRC_SEL_CLKSRCSEL	R/W	555h	Select line for selecting source clock for HSM_WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - XTALCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - RCCLK10M 0x555 - RCCLK10M 0x666 - EXT_REFCLK 0x777 - RCCLK32K

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2.5.2.291 MSS_RCM_HSM_RTC_CLK_SRC_SEL Register

2.5.2.291.1 MSS_RCM_HSM_RTC_CLK_SRC_SEL Register (Offset = 808h) [reset = 777h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-1398. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8808h

Figure 2-697. MSS_RCM_HSM_RTC_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				HSM_RTC_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				777h			
7	6	5	4	3	2	1	0
HSM_RTC_CLK_SRC_SEL_CLKSRCSEL							
R/W							
777h							

Table 2-1399. MSS_RCM_HSM_RTC_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	HSM_RTC_CLK_SRC_SEL_CLKSRCSEL	R/W	777h	Select line for selecting source clock for HSM_RTC.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - XTALCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - RCCLK10M 0x555 - RCCLK10M 0x666 - EXT_REFCLK 0x777 - RCCLK32K

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2.5.2.292 MSS_RCM_HSM_DMTA_CLK_SRC_SEL Register

2.5.2.292.1 MSS_RCM_HSM_DMTA_CLK_SRC_SEL Register (Offset = 80Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-1400. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 880Ch

Figure 2-698. MSS_RCM_HSM_DMTA_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				HSM_DMTA_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
HSM_DMTA_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-1401. MSS_RCM_HSM_DMTA_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	HSM_DMTA_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for HSM_DMTA.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - XTALCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - RCCLK10M 0x555 - RCCLK10M 0x666 - EXT_REFCLK 0x777 - RCCLK32K

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2.5.2.293 MSS_RCM_HSM_DMTB_CLK_SRC_SEL Register

2.5.2.293.1 MSS_RCM_HSM_DMTB_CLK_SRC_SEL Register (Offset = 810h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

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Table 2-1402. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8810h

Figure 2-699. MSS_RCM_HSM_DMTB_CLK_SRC_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				HSM_DMTB_CLK_SRC_SEL_CLKSRCSEL			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
HSM_DMTB_CLK_SRC_SEL_CLKSRCSEL							
R/W							
0h							

Table 2-1403. MSS_RCM_HSM_DMTB_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	HSM_DMTB_CLK_SRC_SEL_CLKSRCSEL	R/W	0h	Select line for selecting source clock for HSM_DMTB.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src- 0x000 - WUCPUCLK 0x111 - XTALCLK 0x222 - SYS_CLK 0x333 - DPLL_PER_HSDIV0_CLKOUT1 0x444 - RCCLK10M 0x555 - RCCLK10M 0x666 - EXT_REFCLK 0x777 - RCCLK32K

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2.5.2.294 MSS_RCM_HSM_RTI_CLK_DIV_VAL Register

2.5.2.294.1 MSS_RCM_HSM_RTI_CLK_DIV_VAL Register (Offset = 814h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-1404. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8814h

Figure 2-700. MSS_RCM_HSM_RTI_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				HSM_RTI_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
HSM_RTI_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1405. MSS_RCM_HSM_RTI_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	HSM_RTI_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value HSM RTI selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.295 MSS_RCM_HSM_WDT_CLK_DIV_VAL Register

2.5.2.295.1 MSS_RCM_HSM_WDT_CLK_DIV_VAL Register (Offset = 818h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-1406. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8818h

Figure 2-701. MSS_RCM_HSM_WDT_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				HSM_WDT_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
HSM_WDT_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1407. MSS_RCM_HSM_WDT_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	HSM_WDT_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value HSM WDT selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.296 MSS_RCM_HSM_RTC_CLK_DIV_VAL Register

2.5.2.296.1 MSS_RCM_HSM_RTC_CLK_DIV_VAL Register (Offset = 81Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-1408. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 881Ch

Figure 2-702. MSS_RCM_HSM_RTC_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				HSM_RTC_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
HSM_RTC_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1409. MSS_RCM_HSM_RTC_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	HSM_RTC_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value HSM RTC selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.297 MSS_RCM_HSM_DMTA_CLK_DIV_VAL Register

2.5.2.297.1 MSS_RCM_HSM_DMTA_CLK_DIV_VAL Register (Offset = 820h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-1410. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8820h

Figure 2-703. MSS_RCM_HSM_DMTA_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				HSM_DMTA_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HSM_DMTA_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1411. MSS_RCM_HSM_DMTA_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	HSM_DMTA_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value HSM DMTA selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.298 MSS_RCM_HSM_DMTB_CLK_DIV_VAL Register

2.5.2.298.1 MSS_RCM_HSM_DMTB_CLK_DIV_VAL Register (Offset = 824h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

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Table 2-1412. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8824h

Figure 2-704. MSS_RCM_HSM_DMTB_CLK_DIV_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				HSM_DMTB_CLK_DIV_VAL_CLKDIVR			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
HSM_DMTB_CLK_DIV_VAL_CLKDIVR							
R/W							
0h							

Table 2-1413. MSS_RCM_HSM_DMTB_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	HSM_DMTB_CLK_DIV_VAL_CLKDIVR	R/W	0h	Divider value HSM DMTB selected clock.To set the divider value of [n+1] configure the register to value of '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register.

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2.5.2.299 MSS_RCM_HSM_RTI_CLK_GATE Register

2.5.2.299.1 MSS_RCM_HSM_RTI_CLK_GATE Register (Offset = 828h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1414. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8828h

Figure 2-705. MSS_RCM_HSM_RTI_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					HSM_RTI_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1415. MSS_RCM_HSM_RTI_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	HSM_RTI_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for HSM RTI

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2.5.2.300 MSS_RCM_HSM_WDT_CLK_GATE Register

2.5.2.300.1 MSS_RCM_HSM_WDT_CLK_GATE Register (Offset = 82Ch) [reset = 7h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1416. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 882Ch

Figure 2-706. MSS_RCM_HSM_WDT_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					HSM_WDT_CLK_GATE_GATED		
NONE					R/W		
0h					7h		

Table 2-1417. MSS_RCM_HSM_WDT_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	HSM_WDT_CLK_GATE_GATED	R/W	7h	Writing 3'b111 will gate clock for HSM WDT

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2.5.2.301 MSS_RCM_HSM_RTC_CLK_GATE Register

2.5.2.301.1 MSS_RCM_HSM_RTC_CLK_GATE Register (Offset = 830h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1418. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8830h

Figure 2-707. MSS_RCM_HSM_RTC_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					HSM_RTC_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1419. MSS_RCM_HSM_RTC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	HSM_RTC_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for HSM RTC

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2.5.2.302 MSS_RCM_HSM_DMTA_CLK_GATE Register

2.5.2.302.1 MSS_RCM_HSM_DMTA_CLK_GATE Register (Offset = 834h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1420. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8834h

Figure 2-708. MSS_RCM_HSM_DMTA_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					HSM_DMTA_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1421. MSS_RCM_HSM_DMTA_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	HSM_DMTA_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for HSM DMTA

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2.5.2.303 MSS_RCM_HSM_DMTB_CLK_GATE Register

2.5.2.303.1 MSS_RCM_HSM_DMTB_CLK_GATE Register (Offset = 838h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1422. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8838h

Figure 2-709. MSS_RCM_HSM_DMTB_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					HSM_DMTB_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1423. MSS_RCM_HSM_DMTB_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	HSM_DMTB_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for HSM DMTB

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2.5.2.304 MSS_RCM_HSM_RTI_CLK_STATUS Register

2.5.2.304.1 MSS_RCM_HSM_RTI_CLK_STATUS Register (Offset = 83Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

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Table 2-1424. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 883Ch

Figure 2-710. MSS_RCM_HSM_RTI_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HSM_RTI_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
HSM_RTI_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1425. MSS_RCM_HSM_RTI_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	HSM_RTI_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for HSM_RTI
7:0	HSM_RTI_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for HSM_RTI based on one hot encoding technique.

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2.5.2.305 MSS_RCM_HSM_WDT_CLK_STATUS Register

2.5.2.305.1 MSS_RCM_HSM_WDT_CLK_STATUS Register (Offset = 840h) [reset = 20h]

Clock source selection and Divider Value of respective clock.

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Table 2-1426. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8840h

Figure 2-711. MSS_RCM_HSM_WDT_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HSM_WDT_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
HSM_WDT_CLK_STATUS_CLKINUSE							
R							
20h							

Table 2-1427. MSS_RCM_HSM_WDT_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	HSM_WDT_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for HSM_WDT
7:0	HSM_WDT_CLK_STATUS_CLKINUSE	R	20h	Status shows the source clock slected for HSM_WDT based on one hot encoding technique.

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2.5.2.306 MSS_RCM_HSM_RTC_CLK_STATUS Register

2.5.2.306.1 MSS_RCM_HSM_RTC_CLK_STATUS Register (Offset = 844h) [reset = 80h]

Clock source selection and Divider Value of respective clock.

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Table 2-1428. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8844h

Figure 2-712. MSS_RCM_HSM_RTC_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HSM_RTC_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
HSM_RTC_CLK_STATUS_CLKINUSE							
R							
80h							

Table 2-1429. MSS_RCM_HSM_RTC_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	HSM_RTC_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for HSM_RTC
7:0	HSM_RTC_CLK_STATUS_CLKINUSE	R	80h	Status shows the source clock slected for HSM_RTC based on one hot encoding technique.

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2.5.2.307 MSS_RCM_HSM_DMTA_CLK_STATUS Register

2.5.2.307.1 MSS_RCM_HSM_DMTA_CLK_STATUS Register (Offset = 848h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

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Table 2-1430. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8848h

Figure 2-713. MSS_RCM_HSM_DMTA_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HSM_DMTA_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
HSM_DMTA_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1431. MSS_RCM_HSM_DMTA_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	HSM_DMTA_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for HSM_DMTA
7:0	HSM_DMTA_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for HSM_DMTA based on one hot encoding technique.

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2.5.2.308 MSS_RCM_HSM_DMTB_CLK_STATUS Register

2.5.2.308.1 MSS_RCM_HSM_DMTB_CLK_STATUS Register (Offset = 84Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

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Table 2-1432. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 884Ch

Figure 2-714. MSS_RCM_HSM_DMTB_CLK_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
HSM_DMTB_CLK_STATUS_CURRDIVIDER							
R							
0h							
7	6	5	4	3	2	1	0
HSM_DMTB_CLK_STATUS_CLKINUSE							
R							
1h							

Table 2-1433. MSS_RCM_HSM_DMTB_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	HSM_DMTB_CLK_STATUS_CURRDIVIDER	R	0h	Status shows the current divider value choosen for HSM_DMTB
7:0	HSM_DMTB_CLK_STATUS_CLKINUSE	R	1h	Status shows the source clock slected for HSM_DMTB based on one hot encoding technique.

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2.5.2.309 MSS_RCM_MCSPI5_CLK_GATE Register

2.5.2.309.1 MSS_RCM_MCSPI5_CLK_GATE Register (Offset = 900h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1434. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8900h

Figure 2-715. MSS_RCM_MCSPI5_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI5_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1435. MSS_RCM_MCSPI5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI5_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.5.2.310 MSS_RCM_MCSPI6_CLK_GATE Register

2.5.2.310.1 MSS_RCM_MCSPI6_CLK_GATE Register (Offset = 904h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1436. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8904h

Figure 2-716. MSS_RCM_MCSPI6_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI6_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1437. MSS_RCM_MCSPI6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI6_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.5.2.311 MSS_RCM_MCSPI7_CLK_GATE Register

2.5.2.311.1 MSS_RCM_MCSPI7_CLK_GATE Register (Offset = 908h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

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Table 2-1438. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8908h

Figure 2-717. MSS_RCM_MCSPI7_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MCSPI7_CLK_GATE_GATED		
NONE					R/W		
0h					0h		

Table 2-1439. MSS_RCM_MCSPI7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	MCSPI7_CLK_GATE_GATED	R/W	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.5.2.312 MSS_RCM_LOCK0_KICK0 Register

2.5.2.312.1 MSS_RCM_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component.

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Table 2-1440. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9008h

Figure 2-718. MSS_RCM_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 2-1441. MSS_RCM_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component

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2.5.2.313 MSS_RCM_LOCK0_KICK1 Register

2.5.2.313.1 MSS_RCM_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component.

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Table 2-1442. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 900Ch

Figure 2-719. MSS_RCM_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 2-1443. MSS_RCM_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component

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2.5.2.314 MSS_RCM_INTR_RAW_STATUS Register

2.5.2.314.1 MSS_RCM_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register.

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Table 2-1444. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9010h

Figure 2-720. MSS_RCM_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 2-1445. MSS_RCM_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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2.5.2.315 MSS_RCM_INTR_ENABLED_STATUS_CLEAR Register

2.5.2.315.1 MSS_RCM_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register.

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Table 2-1446. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9014h

Figure 2-721. MSS_RCM_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 2-1447. MSS_RCM_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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2.5.2.316 MSS_RCM_INTR_ENABLE Register

2.5.2.316.1 MSS_RCM_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register.

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Table 2-1448. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9018h

Figure 2-722. MSS_RCM_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 2-1449. MSS_RCM_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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2.5.2.317 MSS_RCM_INTR_ENABLE_CLEAR Register

2.5.2.317.1 MSS_RCM_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register.

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Table 2-1450. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 901Ch

Figure 2-723. MSS_RCM_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 2-1451. MSS_RCM_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

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2.5.2.318 MSS_RCM_EOI Register

2.5.2.318.1 MSS_RCM_EOI Register (Offset = 1020h) [reset = 0h]

EOI register.

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Table 2-1452. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9020h

Figure 2-724. MSS_RCM_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 2-1453. MSS_RCM_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip.

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2.5.2.319 MSS_RCM_FAULT_ADDRESS Register

2.5.2.319.1 MSS_RCM_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register.

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Table 2-1454. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9024h

Figure 2-725. MSS_RCM_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 2-1455. MSS_RCM_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address.

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2.5.2.320 MSS_RCM_FAULT_TYPE_STATUS Register

2.5.2.320.1 MSS_RCM_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register.

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Table 2-1456. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9028h

Figure 2-726. MSS_RCM_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 2-1457. MSS_RCM_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access.
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

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2.5.2.321 MSS_RCM_FAULT_ATTR_STATUS Register

2.5.2.321.1 MSS_RCM_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register.

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Table 2-1458. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 902Ch

Figure 2-727. MSS_RCM_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FAULT_ROUTEID							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FAULT_PRIVID							
R							
0h							

Table 2-1459. MSS_RCM_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID.
19:8	FAULT_ROUTEID	R	0h	Route ID.
7:0	FAULT_PRIVID	R	0h	Privilege ID.

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2.5.2.322 MSS_RCM_FAULT_CLEAR Register

2.5.2.322.1 MSS_RCM_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register.

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Table 2-1460. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9030h

Figure 2-728. MSS_RCM_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 2-1461. MSS_RCM_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

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2.6 CONTROLSS_GLOBAL_CTRL

CONTROLSS_GLOBAL_CTRL

2.6.1 CONTROLSS_GLOBAL_CTRL Summaries

CONTROLSS_GLOBAL_CTRL Summaries

Table 2-1462. CONTROLSS_CTRL Registers, Base Address=502F 0000h, Length=4096

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
4h	32	CONTROLSS_CTRL_EPWM_STATICXBAR_SEL0	502F 0004h
8h	32	CONTROLSS_CTRL_EPWM_STATICXBAR_SEL1	502F 0008h
10h	32	CONTROLSS_CTRL_EPWM_CLKSYNC	502F 0010h
18h	32	CONTROLSS_CTRL_SDFM1_CLK0_SEL	502F 0018h
20h	32	CONTROLSS_CTRL_EMUSTOPN_MASK	502F 0020h
28h	32	CONTROLSS_CTRL_CLB_AQ_EN0	502F 0028h
30h	32	CONTROLSS_CTRL_CLB_AQ_EN1	502F 0030h
38h	32	CONTROLSS_CTRL_CLB_DB_EN0	502F 0038h
40h	32	CONTROLSS_CTRL_CLB_DB_EN1	502F 0040h
44h	32	CONTROLSS_CTRL_ADCSOCFRCGBSEL	502F 0044h
48h	32	CONTROLSS_CTRL_ADCSOCFRCGB	502F 0048h
4Ch	32	CONTROLSS_CTRL_ADC_EXTCH_DLY_SEL	502F 004Ch
50h	32	CONTROLSS_CTRL_XBAR_LOOPBACK_CTRL	502F 0050h
60h	32	CONTROLSS_CTRL_EPWM_SOCA_SEL	502F 0060h
64h	32	CONTROLSS_CTRL_EPWM_SOCB_SEL	502F 0064h
70h	32	CONTROLSS_CTRL_ADCEXTCHXBAR0_G0_SEL	502F 0070h
74h	32	CONTROLSS_CTRL_ADCEXTCHXBAR1_G0_SEL	502F 0074h
78h	32	CONTROLSS_CTRL_ADCEXTCHXBAR2_G0_SEL	502F 0078h
7Ch	32	CONTROLSS_CTRL_ADCEXTCHXBAR3_G0_SEL	502F 007Ch
80h	32	CONTROLSS_CTRL_ADCEXTCHXBAR4_G0_SEL	502F 0080h
84h	32	CONTROLSS_CTRL_ADCEXTCHXBAR5_G0_SEL	502F 0084h
88h	32	CONTROLSS_CTRL_ADCEXTCHXBAR6_G0_SEL	502F 0088h
8Ch	32	CONTROLSS_CTRL_ADCEXTCHXBAR7_G0_SEL	502F 008Ch
90h	32	CONTROLSS_CTRL_ADCEXTCHXBAR8_G0_SEL	502F 0090h
94h	32	CONTROLSS_CTRL_ADCEXTCHXBAR9_G0_SEL	502F 0094h
B0h	32	CONTROLSS_CTRL_SDFM0_CLK0_OUT_SEL	502F 00B0h
B4h	32	CONTROLSS_CTRL_SDFM0_CLK1_OUT_SEL	502F 00B4h
B8h	32	CONTROLSS_CTRL_SDFM0_CLK2_OUT_SEL	502F 00B8h
BCh	32	CONTROLSS_CTRL_SDFM0_CLK3_OUT_SEL	502F 00BCh
C0h	32	CONTROLSS_CTRL_SDFM1_CLK0_OUT_SEL	502F 00C0h
C4h	32	CONTROLSS_CTRL_SDFM1_CLK1_OUT_SEL	502F 00C4h
C8h	32	CONTROLSS_CTRL_SDFM1_CLK2_OUT_SEL	502F 00C8h
CCh	32	CONTROLSS_CTRL_SDFM1_CLK3_OUT_SEL	502F 00CCh
E0h	32	CONTROLSS_CTRL_CONTROLSS_G0_EPWM_WLINK	502F 00E0h
E4h	32	CONTROLSS_CTRL_CONTROLSS_G1_EPWM_WLINK	502F 00E4h
E8h	32	CONTROLSS_CTRL_CONTROLSS_G2_EPWM_WLINK	502F 00E8h
ECh	32	CONTROLSS_CTRL_CONTROLSS_G3_EPWM_WLINK	502F 00ECh
100h	32	CONTROLSS_CTRL_EPWM0_CLK_GATE	502F 0100h
104h	32	CONTROLSS_CTRL_EPWM1_CLK_GATE	502F 0104h

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Table 2-1462. CONTROLSS_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
108h	32	CONTROLSS_CTRL_EPWM2_CLK_GATE	502F 0108h
10Ch	32	CONTROLSS_CTRL_EPWM3_CLK_GATE	502F 010Ch
110h	32	CONTROLSS_CTRL_EPWM4_CLK_GATE	502F 0110h
114h	32	CONTROLSS_CTRL_EPWM5_CLK_GATE	502F 0114h
118h	32	CONTROLSS_CTRL_EPWM6_CLK_GATE	502F 0118h
11Ch	32	CONTROLSS_CTRL_EPWM7_CLK_GATE	502F 011Ch
120h	32	CONTROLSS_CTRL_EPWM8_CLK_GATE	502F 0120h
124h	32	CONTROLSS_CTRL_EPWM9_CLK_GATE	502F 0124h
128h	32	CONTROLSS_CTRL_EPWM10_CLK_GATE	502F 0128h
12Ch	32	CONTROLSS_CTRL_EPWM11_CLK_GATE	502F 012Ch
130h	32	CONTROLSS_CTRL_EPWM12_CLK_GATE	502F 0130h
134h	32	CONTROLSS_CTRL_EPWM13_CLK_GATE	502F 0134h
138h	32	CONTROLSS_CTRL_EPWM14_CLK_GATE	502F 0138h
13Ch	32	CONTROLSS_CTRL_EPWM15_CLK_GATE	502F 013Ch
140h	32	CONTROLSS_CTRL_EPWM16_CLK_GATE	502F 0140h
144h	32	CONTROLSS_CTRL_EPWM17_CLK_GATE	502F 0144h
148h	32	CONTROLSS_CTRL_EPWM18_CLK_GATE	502F 0148h
14Ch	32	CONTROLSS_CTRL_EPWM19_CLK_GATE	502F 014Ch
150h	32	CONTROLSS_CTRL_EPWM20_CLK_GATE	502F 0150h
154h	32	CONTROLSS_CTRL_EPWM21_CLK_GATE	502F 0154h
158h	32	CONTROLSS_CTRL_EPWM22_CLK_GATE	502F 0158h
15Ch	32	CONTROLSS_CTRL_EPWM23_CLK_GATE	502F 015Ch
160h	32	CONTROLSS_CTRL_EPWM24_CLK_GATE	502F 0160h
164h	32	CONTROLSS_CTRL_EPWM25_CLK_GATE	502F 0164h
168h	32	CONTROLSS_CTRL_EPWM26_CLK_GATE	502F 0168h
16Ch	32	CONTROLSS_CTRL_EPWM27_CLK_GATE	502F 016Ch
170h	32	CONTROLSS_CTRL_EPWM28_CLK_GATE	502F 0170h
174h	32	CONTROLSS_CTRL_EPWM29_CLK_GATE	502F 0174h
178h	32	CONTROLSS_CTRL_EPWM30_CLK_GATE	502F 0178h
17Ch	32	CONTROLSS_CTRL_EPWM31_CLK_GATE	502F 017Ch
180h	32	CONTROLSS_CTRL_FSI_TX0_CLK_GATE	502F 0180h
184h	32	CONTROLSS_CTRL_FSI_TX1_CLK_GATE	502F 0184h
188h	32	CONTROLSS_CTRL_FSI_TX2_CLK_GATE	502F 0188h
18Ch	32	CONTROLSS_CTRL_FSI_TX3_CLK_GATE	502F 018Ch
190h	32	CONTROLSS_CTRL_FSI_RX0_CLK_GATE	502F 0190h
194h	32	CONTROLSS_CTRL_FSI_RX1_CLK_GATE	502F 0194h
198h	32	CONTROLSS_CTRL_FSI_RX2_CLK_GATE	502F 0198h
19Ch	32	CONTROLSS_CTRL_FSI_RX3_CLK_GATE	502F 019Ch
1A0h	32	CONTROLSS_CTRL_CMPSSA0_CLK_GATE	502F 01A0h
1A4h	32	CONTROLSS_CTRL_CMPSSA1_CLK_GATE	502F 01A4h
1A8h	32	CONTROLSS_CTRL_CMPSSA2_CLK_GATE	502F 01A8h
1ACh	32	CONTROLSS_CTRL_CMPSSA3_CLK_GATE	502F 01ACh
1B0h	32	CONTROLSS_CTRL_CMPSSA4_CLK_GATE	502F 01B0h
1B4h	32	CONTROLSS_CTRL_CMPSSA5_CLK_GATE	502F 01B4h
1B8h	32	CONTROLSS_CTRL_CMPSSA6_CLK_GATE	502F 01B8h
1BCh	32	CONTROLSS_CTRL_CMPSSA7_CLK_GATE	502F 01BCh

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Table 2-1462. CONTROLSS_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
1C0h	32	CONTROLSS_CTRL_CMPSSA8_CLK_GATE	502F 01C0h
1C4h	32	CONTROLSS_CTRL_CMPSSA9_CLK_GATE	502F 01C4h
1D0h	32	CONTROLSS_CTRL_CMPSSB0_CLK_GATE	502F 01D0h
1D4h	32	CONTROLSS_CTRL_CMPSSB1_CLK_GATE	502F 01D4h
1D8h	32	CONTROLSS_CTRL_CMPSSB2_CLK_GATE	502F 01D8h
1DCh	32	CONTROLSS_CTRL_CMPSSB3_CLK_GATE	502F 01DCh
1E0h	32	CONTROLSS_CTRL_CMPSSB4_CLK_GATE	502F 01E0h
1E4h	32	CONTROLSS_CTRL_CMPSSB5_CLK_GATE	502F 01E4h
1E8h	32	CONTROLSS_CTRL_CMPSSB6_CLK_GATE	502F 01E8h
1ECh	32	CONTROLSS_CTRL_CMPSSB7_CLK_GATE	502F 01ECh
1F0h	32	CONTROLSS_CTRL_CMPSSB8_CLK_GATE	502F 01F0h
1F4h	32	CONTROLSS_CTRL_CMPSSB9_CLK_GATE	502F 01F4h
200h	32	CONTROLSS_CTRL_ECAP0_CLK_GATE	502F 0200h
204h	32	CONTROLSS_CTRL_ECAP1_CLK_GATE	502F 0204h
208h	32	CONTROLSS_CTRL_ECAP2_CLK_GATE	502F 0208h
20Ch	32	CONTROLSS_CTRL_ECAP3_CLK_GATE	502F 020Ch
210h	32	CONTROLSS_CTRL_ECAP4_CLK_GATE	502F 0210h
214h	32	CONTROLSS_CTRL_ECAP5_CLK_GATE	502F 0214h
218h	32	CONTROLSS_CTRL_ECAP6_CLK_GATE	502F 0218h
21Ch	32	CONTROLSS_CTRL_ECAP7_CLK_GATE	502F 021Ch
220h	32	CONTROLSS_CTRL_ECAP8_CLK_GATE	502F 0220h
224h	32	CONTROLSS_CTRL_ECAP9_CLK_GATE	502F 0224h
228h	32	CONTROLSS_CTRL_ECAP10_CLK_GATE	502F 0228h
22Ch	32	CONTROLSS_CTRL_ECAP11_CLK_GATE	502F 022Ch
230h	32	CONTROLSS_CTRL_ECAP12_CLK_GATE	502F 0230h
234h	32	CONTROLSS_CTRL_ECAP13_CLK_GATE	502F 0234h
238h	32	CONTROLSS_CTRL_ECAP14_CLK_GATE	502F 0238h
23Ch	32	CONTROLSS_CTRL_ECAP15_CLK_GATE	502F 023Ch
240h	32	CONTROLSS_CTRL_EQEP0_CLK_GATE	502F 0240h
244h	32	CONTROLSS_CTRL_EQEP1_CLK_GATE	502F 0244h
248h	32	CONTROLSS_CTRL_EQEP2_CLK_GATE	502F 0248h
250h	32	CONTROLSS_CTRL_SDFM0_CLK_GATE	502F 0250h
254h	32	CONTROLSS_CTRL_SDFM1_CLK_GATE	502F 0254h
258h	32	CONTROLSS_CTRL_DAC_CLK_GATE	502F 0258h
25Ch	32	CONTROLSS_CTRL_ADC0_CLK_GATE	502F 025Ch
260h	32	CONTROLSS_CTRL_ADC1_CLK_GATE	502F 0260h
264h	32	CONTROLSS_CTRL_ADC2_CLK_GATE	502F 0264h
268h	32	CONTROLSS_CTRL_ADC3_CLK_GATE	502F 0268h
26Ch	32	CONTROLSS_CTRL_ADC4_CLK_GATE	502F 026Ch
270h	32	CONTROLSS_CTRL_OTTO0_CLK_GATE	502F 0270h
274h	32	CONTROLSS_CTRL_OTTO1_CLK_GATE	502F 0274h
278h	32	CONTROLSS_CTRL_OTTO2_CLK_GATE	502F 0278h
27Ch	32	CONTROLSS_CTRL_OTTO3_CLK_GATE	502F 027Ch
280h	32	CONTROLSS_CTRL_SDFM0_PLL_CLK_GATE	502F 0280h
284h	32	CONTROLSS_CTRL_SDFM1_PLL_CLK_GATE	502F 0284h
288h	32	CONTROLSS_CTRL_FSI_TX0_PLL_CLK_GATE	502F 0288h

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Table 2-1462. CONTROLSS_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
28Ch	32	CONTROLSS_CTRL_FSI_TX1_PLL_CLK_GATE	502F 028Ch
290h	32	CONTROLSS_CTRL_FSI_TX2_PLL_CLK_GATE	502F 0290h
294h	32	CONTROLSS_CTRL_FSI_TX3_PLL_CLK_GATE	502F 0294h
298h	32	CONTROLSS_CTRL_HW_RESOLVER_CLK_GATE	502F 0298h
29Ch	32	CONTROLSS_CTRL_ADC_SCTILE0_CLK_GATE	502F 029Ch
2A0h	32	CONTROLSS_CTRL_ADC_SCTILE1_CLK_GATE	502F 02A0h
2A4h	32	CONTROLSS_CTRL_ADC_SCTILE2_CLK_GATE	502F 02A4h
2A8h	32	CONTROLSS_CTRL_ADC_SCTILE3_CLK_GATE	502F 02A8h
2ACh	32	CONTROLSS_CTRL_ADC_SCTILE4_CLK_GATE	502F 02ACh
2B0h	32	CONTROLSS_CTRL_ADC_SCTILE5_CLK_GATE	502F 02B0h
2B4h	32	CONTROLSS_CTRL_ADC_SCTILE6_CLK_GATE	502F 02B4h
2B8h	32	CONTROLSS_CTRL_ADC_SCTILE7_CLK_GATE	502F 02B8h
2BCh	32	CONTROLSS_CTRL_ADC_SCTILE8_CLK_GATE	502F 02BCh
2C0h	32	CONTROLSS_CTRL_ADC_SCTILE9_CLK_GATE	502F 02C0h
2C4h	32	CONTROLSS_CTRL_ADC_SCTILE10_CLK_GATE	502F 02C4h
2C8h	32	CONTROLSS_CTRL_ADC_SCTILE11_CLK_GATE	502F 02C8h
2DCh	32	CONTROLSS_CTRL_ADC_AGG0_CLK_GATE	502F 02DCh
2E0h	32	CONTROLSS_CTRL_CONTROLSS_XBAR_CLK_GATE	502F 02E0h
2E4h	32	CONTROLSS_CTRL_ADCR0_CLK_GATE	502F 02E4h
2E8h	32	CONTROLSS_CTRL_ADCR1_CLK_GATE	502F 02E8h
300h	32	CONTROLSS_CTRL_EPWM0_RST	502F 0300h
304h	32	CONTROLSS_CTRL_EPWM1_RST	502F 0304h
308h	32	CONTROLSS_CTRL_EPWM2_RST	502F 0308h
30Ch	32	CONTROLSS_CTRL_EPWM3_RST	502F 030Ch
310h	32	CONTROLSS_CTRL_EPWM4_RST	502F 0310h
314h	32	CONTROLSS_CTRL_EPWM5_RST	502F 0314h
318h	32	CONTROLSS_CTRL_EPWM6_RST	502F 0318h
31Ch	32	CONTROLSS_CTRL_EPWM7_RST	502F 031Ch
320h	32	CONTROLSS_CTRL_EPWM8_RST	502F 0320h
324h	32	CONTROLSS_CTRL_EPWM9_RST	502F 0324h
328h	32	CONTROLSS_CTRL_EPWM10_RST	502F 0328h
32Ch	32	CONTROLSS_CTRL_EPWM11_RST	502F 032Ch
330h	32	CONTROLSS_CTRL_EPWM12_RST	502F 0330h
334h	32	CONTROLSS_CTRL_EPWM13_RST	502F 0334h
338h	32	CONTROLSS_CTRL_EPWM14_RST	502F 0338h
33Ch	32	CONTROLSS_CTRL_EPWM15_RST	502F 033Ch
340h	32	CONTROLSS_CTRL_EPWM16_RST	502F 0340h
344h	32	CONTROLSS_CTRL_EPWM17_RST	502F 0344h
348h	32	CONTROLSS_CTRL_EPWM18_RST	502F 0348h
34Ch	32	CONTROLSS_CTRL_EPWM19_RST	502F 034Ch
350h	32	CONTROLSS_CTRL_EPWM20_RST	502F 0350h
354h	32	CONTROLSS_CTRL_EPWM21_RST	502F 0354h
358h	32	CONTROLSS_CTRL_EPWM22_RST	502F 0358h
35Ch	32	CONTROLSS_CTRL_EPWM23_RST	502F 035Ch
360h	32	CONTROLSS_CTRL_EPWM24_RST	502F 0360h
364h	32	CONTROLSS_CTRL_EPWM25_RST	502F 0364h

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Table 2-1462. CONTROLSS_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
368h	32	CONTROLSS_CTRL_EPWM26_RST	502F 0368h
36Ch	32	CONTROLSS_CTRL_EPWM27_RST	502F 036Ch
370h	32	CONTROLSS_CTRL_EPWM28_RST	502F 0370h
374h	32	CONTROLSS_CTRL_EPWM29_RST	502F 0374h
378h	32	CONTROLSS_CTRL_EPWM30_RST	502F 0378h
37Ch	32	CONTROLSS_CTRL_EPWM31_RST	502F 037Ch
380h	32	CONTROLSS_CTRL_FSI_TX0_RST	502F 0380h
384h	32	CONTROLSS_CTRL_FSI_TX1_RST	502F 0384h
388h	32	CONTROLSS_CTRL_FSI_TX2_RST	502F 0388h
38Ch	32	CONTROLSS_CTRL_FSI_TX3_RST	502F 038Ch
390h	32	CONTROLSS_CTRL_FSI_RX0_RST	502F 0390h
394h	32	CONTROLSS_CTRL_FSI_RX1_RST	502F 0394h
398h	32	CONTROLSS_CTRL_FSI_RX2_RST	502F 0398h
39Ch	32	CONTROLSS_CTRL_FSI_RX3_RST	502F 039Ch
3A0h	32	CONTROLSS_CTRL_CMPSSA0_RST	502F 03A0h
3A4h	32	CONTROLSS_CTRL_CMPSSA1_RST	502F 03A4h
3A8h	32	CONTROLSS_CTRL_CMPSSA2_RST	502F 03A8h
3ACh	32	CONTROLSS_CTRL_CMPSSA3_RST	502F 03ACh
3B0h	32	CONTROLSS_CTRL_CMPSSA4_RST	502F 03B0h
3B4h	32	CONTROLSS_CTRL_CMPSSA5_RST	502F 03B4h
3B8h	32	CONTROLSS_CTRL_CMPSSA6_RST	502F 03B8h
3BCh	32	CONTROLSS_CTRL_CMPSSA7_RST	502F 03BCh
3C0h	32	CONTROLSS_CTRL_CMPSSA8_RST	502F 03C0h
3C4h	32	CONTROLSS_CTRL_CMPSSA9_RST	502F 03C4h
3D0h	32	CONTROLSS_CTRL_CMPSSB0_RST	502F 03D0h
3D4h	32	CONTROLSS_CTRL_CMPSSB1_RST	502F 03D4h
3D8h	32	CONTROLSS_CTRL_CMPSSB2_RST	502F 03D8h
3DCh	32	CONTROLSS_CTRL_CMPSSB3_RST	502F 03DCh
3E0h	32	CONTROLSS_CTRL_CMPSSB4_RST	502F 03E0h
3E4h	32	CONTROLSS_CTRL_CMPSSB5_RST	502F 03E4h
3E8h	32	CONTROLSS_CTRL_CMPSSB6_RST	502F 03E8h
3ECh	32	CONTROLSS_CTRL_CMPSSB7_RST	502F 03ECh
3F0h	32	CONTROLSS_CTRL_CMPSSB8_RST	502F 03F0h
3F4h	32	CONTROLSS_CTRL_CMPSSB9_RST	502F 03F4h
400h	32	CONTROLSS_CTRL_ECAP0_RST	502F 0400h
404h	32	CONTROLSS_CTRL_ECAP1_RST	502F 0404h
408h	32	CONTROLSS_CTRL_ECAP2_RST	502F 0408h
40Ch	32	CONTROLSS_CTRL_ECAP3_RST	502F 040Ch
410h	32	CONTROLSS_CTRL_ECAP4_RST	502F 0410h
414h	32	CONTROLSS_CTRL_ECAP5_RST	502F 0414h
418h	32	CONTROLSS_CTRL_ECAP6_RST	502F 0418h
41Ch	32	CONTROLSS_CTRL_ECAP7_RST	502F 041Ch
420h	32	CONTROLSS_CTRL_ECAP8_RST	502F 0420h
424h	32	CONTROLSS_CTRL_ECAP9_RST	502F 0424h
428h	32	CONTROLSS_CTRL_ECAP10_RST	502F 0428h
42Ch	32	CONTROLSS_CTRL_ECAP11_RST	502F 042Ch

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Table 2-1462. CONTROLSS_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
430h	32	CONTROLSS_CTRL_ECAP12_RST	502F 0430h
434h	32	CONTROLSS_CTRL_ECAP13_RST	502F 0434h
438h	32	CONTROLSS_CTRL_ECAP14_RST	502F 0438h
43Ch	32	CONTROLSS_CTRL_ECAP15_RST	502F 043Ch
440h	32	CONTROLSS_CTRL_EQEP0_RST	502F 0440h
444h	32	CONTROLSS_CTRL_EQEP1_RST	502F 0444h
448h	32	CONTROLSS_CTRL_EQEP2_RST	502F 0448h
450h	32	CONTROLSS_CTRL_SDFM0_RST	502F 0450h
454h	32	CONTROLSS_CTRL_SDFM1_RST	502F 0454h
458h	32	CONTROLSS_CTRL_DAC_RST	502F 0458h
45Ch	32	CONTROLSS_CTRL_ADC0_RST	502F 045Ch
460h	32	CONTROLSS_CTRL_ADC1_RST	502F 0460h
464h	32	CONTROLSS_CTRL_ADC2_RST	502F 0464h
468h	32	CONTROLSS_CTRL_ADC3_RST	502F 0468h
46Ch	32	CONTROLSS_CTRL_ADC4_RST	502F 046Ch
470h	32	CONTROLSS_CTRL_OTTO0_RST	502F 0470h
474h	32	CONTROLSS_CTRL_OTTO1_RST	502F 0474h
478h	32	CONTROLSS_CTRL_OTTO2_RST	502F 0478h
47Ch	32	CONTROLSS_CTRL_OTTO3_RST	502F 047Ch
480h	32	CONTROLSS_CTRL_HW_RESOLVER_RST	502F 0480h
484h	32	CONTROLSS_CTRL_ADC_SCTILE0_RST	502F 0484h
488h	32	CONTROLSS_CTRL_ADC_SCTILE1_RST	502F 0488h
48Ch	32	CONTROLSS_CTRL_ADC_SCTILE2_RST	502F 048Ch
490h	32	CONTROLSS_CTRL_ADC_SCTILE3_RST	502F 0490h
494h	32	CONTROLSS_CTRL_ADC_SCTILE4_RST	502F 0494h
498h	32	CONTROLSS_CTRL_ADC_SCTILE5_RST	502F 0498h
49Ch	32	CONTROLSS_CTRL_ADC_SCTILE6_RST	502F 049Ch
4A0h	32	CONTROLSS_CTRL_ADC_SCTILE7_RST	502F 04A0h
4A4h	32	CONTROLSS_CTRL_ADC_SCTILE8_RST	502F 04A4h
4A8h	32	CONTROLSS_CTRL_ADC_SCTILE9_RST	502F 04A8h
4ACh	32	CONTROLSS_CTRL_ADC_SCTILE10_RST	502F 04ACh
4B0h	32	CONTROLSS_CTRL_ADC_SCTILE11_RST	502F 04B0h
4C4h	32	CONTROLSS_CTRL_ADC_AGG0_RST	502F 04C4h
4C8h	32	CONTROLSS_CTRL_ADCR0_RST	502F 04C8h
4CCh	32	CONTROLSS_CTRL_ADCR1_RST	502F 04CCh
500h	32	CONTROLSS_CTRL_EPWM0_HALTEN	502F 0500h
504h	32	CONTROLSS_CTRL_EPWM1_HALTEN	502F 0504h
508h	32	CONTROLSS_CTRL_EPWM2_HALTEN	502F 0508h
50Ch	32	CONTROLSS_CTRL_EPWM3_HALTEN	502F 050Ch
510h	32	CONTROLSS_CTRL_EPWM4_HALTEN	502F 0510h
514h	32	CONTROLSS_CTRL_EPWM5_HALTEN	502F 0514h
518h	32	CONTROLSS_CTRL_EPWM6_HALTEN	502F 0518h
51Ch	32	CONTROLSS_CTRL_EPWM7_HALTEN	502F 051Ch
520h	32	CONTROLSS_CTRL_EPWM8_HALTEN	502F 0520h
524h	32	CONTROLSS_CTRL_EPWM9_HALTEN	502F 0524h
528h	32	CONTROLSS_CTRL_EPWM10_HALTEN	502F 0528h

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Table 2-1462. CONTROLSS_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
52Ch	32	CONTROLSS_CTRL_EPWM11_HALTEN	502F 052Ch
530h	32	CONTROLSS_CTRL_EPWM12_HALTEN	502F 0530h
534h	32	CONTROLSS_CTRL_EPWM13_HALTEN	502F 0534h
538h	32	CONTROLSS_CTRL_EPWM14_HALTEN	502F 0538h
53Ch	32	CONTROLSS_CTRL_EPWM15_HALTEN	502F 053Ch
540h	32	CONTROLSS_CTRL_EPWM16_HALTEN	502F 0540h
544h	32	CONTROLSS_CTRL_EPWM17_HALTEN	502F 0544h
548h	32	CONTROLSS_CTRL_EPWM18_HALTEN	502F 0548h
54Ch	32	CONTROLSS_CTRL_EPWM19_HALTEN	502F 054Ch
550h	32	CONTROLSS_CTRL_EPWM20_HALTEN	502F 0550h
554h	32	CONTROLSS_CTRL_EPWM21_HALTEN	502F 0554h
558h	32	CONTROLSS_CTRL_EPWM22_HALTEN	502F 0558h
55Ch	32	CONTROLSS_CTRL_EPWM23_HALTEN	502F 055Ch
560h	32	CONTROLSS_CTRL_EPWM24_HALTEN	502F 0560h
564h	32	CONTROLSS_CTRL_EPWM25_HALTEN	502F 0564h
568h	32	CONTROLSS_CTRL_EPWM26_HALTEN	502F 0568h
56Ch	32	CONTROLSS_CTRL_EPWM27_HALTEN	502F 056Ch
570h	32	CONTROLSS_CTRL_EPWM28_HALTEN	502F 0570h
574h	32	CONTROLSS_CTRL_EPWM29_HALTEN	502F 0574h
578h	32	CONTROLSS_CTRL_EPWM30_HALTEN	502F 0578h
57Ch	32	CONTROLSS_CTRL_EPWM31_HALTEN	502F 057Ch
580h	32	CONTROLSS_CTRL_CMPSSA0_HALTEN	502F 0580h
584h	32	CONTROLSS_CTRL_CMPSSA1_HALTEN	502F 0584h
588h	32	CONTROLSS_CTRL_CMPSSA2_HALTEN	502F 0588h
58Ch	32	CONTROLSS_CTRL_CMPSSA3_HALTEN	502F 058Ch
590h	32	CONTROLSS_CTRL_CMPSSA4_HALTEN	502F 0590h
594h	32	CONTROLSS_CTRL_CMPSSA5_HALTEN	502F 0594h
598h	32	CONTROLSS_CTRL_CMPSSA6_HALTEN	502F 0598h
59Ch	32	CONTROLSS_CTRL_CMPSSA7_HALTEN	502F 059Ch
5A0h	32	CONTROLSS_CTRL_CMPSSA8_HALTEN	502F 05A0h
5A4h	32	CONTROLSS_CTRL_CMPSSA9_HALTEN	502F 05A4h
5A8h	32	CONTROLSS_CTRL_CMPSSB0_HALTEN	502F 05A8h
5ACh	32	CONTROLSS_CTRL_CMPSSB1_HALTEN	502F 05ACh
5B0h	32	CONTROLSS_CTRL_CMPSSB2_HALTEN	502F 05B0h
5B4h	32	CONTROLSS_CTRL_CMPSSB3_HALTEN	502F 05B4h
5B8h	32	CONTROLSS_CTRL_CMPSSB4_HALTEN	502F 05B8h
5BCh	32	CONTROLSS_CTRL_CMPSSB5_HALTEN	502F 05BCh
5C0h	32	CONTROLSS_CTRL_CMPSSB6_HALTEN	502F 05C0h
5C4h	32	CONTROLSS_CTRL_CMPSSB7_HALTEN	502F 05C4h
5C8h	32	CONTROLSS_CTRL_CMPSSB8_HALTEN	502F 05C8h
5CCh	32	CONTROLSS_CTRL_CMPSSB9_HALTEN	502F 05CCh
5D0h	32	CONTROLSS_CTRL_ECAP0_HALTEN	502F 05D0h
5D4h	32	CONTROLSS_CTRL_ECAP1_HALTEN	502F 05D4h
5D8h	32	CONTROLSS_CTRL_ECAP2_HALTEN	502F 05D8h
5DCh	32	CONTROLSS_CTRL_ECAP3_HALTEN	502F 05DCh
5E0h	32	CONTROLSS_CTRL_ECAP4_HALTEN	502F 05E0h

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Table 2-1462. CONTROLSS_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
5E4h	32	CONTROLSS_CTRL_ECAP5_HALTEN	502F 05E4h
5E8h	32	CONTROLSS_CTRL_ECAP6_HALTEN	502F 05E8h
5ECh	32	CONTROLSS_CTRL_ECAP7_HALTEN	502F 05ECh
5F0h	32	CONTROLSS_CTRL_ECAP8_HALTEN	502F 05F0h
5F4h	32	CONTROLSS_CTRL_ECAP9_HALTEN	502F 05F4h
5F8h	32	CONTROLSS_CTRL_EQEP0_HALTEN	502F 05F8h
5FCh	32	CONTROLSS_CTRL_EQEP1_HALTEN	502F 05FCh
600h	32	CONTROLSS_CTRL_EQEP2_HALTEN	502F 0600h
604h	32	CONTROLSS_CTRL_ECAP10_HALTEN	502F 0604h
608h	32	CONTROLSS_CTRL_ECAP11_HALTEN	502F 0608h
60Ch	32	CONTROLSS_CTRL_ECAP12_HALTEN	502F 060Ch
610h	32	CONTROLSS_CTRL_ECAP13_HALTEN	502F 0610h
614h	32	CONTROLSS_CTRL_ECAP14_HALTEN	502F 0614h
618h	32	CONTROLSS_CTRL_ECAP15_HALTEN	502F 0618h
1008h	32	CONTROLSS_CTRL_LOCK0_KICK0	502F 1008h
100Ch	32	CONTROLSS_CTRL_LOCK0_KICK1	502F 100Ch
1010h	32	CONTROLSS_CTRL_INTR_RAW_STATUS	502F 1010h
1014h	32	CONTROLSS_CTRL_INTR_ENABLED_STATUS_CLEAR	502F 1014h
1018h	32	CONTROLSS_CTRL_INTR_ENABLE	502F 1018h
101Ch	32	CONTROLSS_CTRL_INTR_ENABLE_CLEAR	502F 101Ch
1020h	32	CONTROLSS_CTRL_EOI	502F 1020h
1024h	32	CONTROLSS_CTRL_FAULT_ADDRESS	502F 1024h
1028h	32	CONTROLSS_CTRL_FAULT_TYPE_STATUS	502F 1028h
102Ch	32	CONTROLSS_CTRL_FAULT_ATTR_STATUS	502F 102Ch
1030h	32	CONTROLSS_CTRL_FAULT_CLEAR	502F 1030h

2.6.2 CONTROLSS_GLOBAL_CTRL Registers

CONTROLSS_GLOBAL_CTRL Registers

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2.6.2.1 CONTROLSS_CTRL_EPWM_STATICXBAR_SEL0 Register

2.6.2.1.1 CONTROLSS_CTRL_EPWM_STATICXBAR_SEL0 Register (Offset = 4h) [reset = 0h]

Static crossbar for epwm select.

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Table 2-1463. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0004h

Figure 2-729. CONTROLSS_CTRL_EPWM_STATICXBAR_SEL0 Name Register

31 30	29 28	27 26	25 24
EPWM_STATICXBAR_SEL0_EPWM15	EPWM_STATICXBAR_SEL0_EPWM14	EPWM_STATICXBAR_SEL0_EPWM13	EPWM_STATICXBAR_SEL0_EPWM12
R/W	R/W	R/W	R/W
0h	0h	0h	0h
23 22	**21 20**	**19 18**	**17 16**
EPWM_STATICXBAR_SEL0_EPWM11	EPWM_STATICXBAR_SEL0_EPWM10	EPWM_STATICXBAR_SEL0_EPWM9	EPWM_STATICXBAR_SEL0_EPWM8
R/W	R/W	R/W	R/W
0h	0h	0h	0h
15 14	**13 12**	**11 10**	**9 8**
EPWM_STATICXBAR_SEL0_EPWM7	EPWM_STATICXBAR_SEL0_EPWM6	EPWM_STATICXBAR_SEL0_EPWM5	EPWM_STATICXBAR_SEL0_EPWM4
R/W	R/W	R/W	R/W
0h	0h	0h	0h
7 6	**5 4**	**3 2**	**1 0**
EPWM_STATICXBAR_SEL0_EPWM3	EPWM_STATICXBAR_SEL0_EPWM2	EPWM_STATICXBAR_SEL0_EPWM1	EPWM_STATICXBAR_SEL0_EPWM0
R/W	R/W	R/W	R/W
0h	0h	0h	0h

Table 2-1464. CONTROLSS_CTRL_EPWM_STATICXBAR_SEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	EPWM_STATICXBAR_SEL0_EPWM15	R/W	0h	EPWM15 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
29:28	EPWM_STATICXBAR_SEL0_EPWM14	R/W	0h	EPWM14 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
27:26	EPWM_STATICXBAR_SEL0_EPWM13	R/W	0h	EPWM13 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
25:24	EPWM_STATICXBAR_SEL0_EPWM12	R/W	0h	EPWM12 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
23:22	EPWM_STATICXBAR_SEL0_EPWM11	R/W	0h	EPWM11 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
21:20	EPWM_STATICXBAR_SEL0_EPWM10	R/W	0h	EPWM10 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
19:18	EPWM_STATICXBAR_SEL0_EPWM9	R/W	0h	EPWM9 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
17:16	EPWM_STATICXBAR_SEL0_EPWM8	R/W	0h	EPWM8 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
15:14	EPWM_STATICXBAR_SEL0_EPWM7	R/W	0h	EPWM7 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
13:12	EPWM_STATICXBAR_SEL0_EPWM6	R/W	0h	EPWM6 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3

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Table 2-1464. CONTROLSS_CTRL_EPWM_STATICXBAR_SEL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	EPWM_STATICXBAR_SEL0_EPWM5	R/W	0h	EPWM5 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
9:8	EPWM_STATICXBAR_SEL0_EPWM4	R/W	0h	EPWM4 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
7:6	EPWM_STATICXBAR_SEL0_EPWM3	R/W	0h	EPWM3 access from PCR grouping. Write the following value to access groups - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
5:4	EPWM_STATICXBAR_SEL0_EPWM2	R/W	0h	EPWM2 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
3:2	EPWM_STATICXBAR_SEL0_EPWM1	R/W	0h	EPWM1 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
1:0	EPWM_STATICXBAR_SEL0_EPWM0	R/W	0h	EPWM0 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3

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2.6.2.2 CONTROLSS_CTRL_EPWM_STATICXBAR_SEL1 Register

2.6.2.2.1 CONTROLSS_CTRL_EPWM_STATICXBAR_SEL1 Register (Offset = 8h) [reset = 0h]

Static crossbar for epwm select.

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Table 2-1465. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0008h

Figure 2-730. CONTROLSS_CTRL_EPWM_STATICXBAR_SEL1 Name Register

31 30	29 28	27 26	25 24
EPWM_STATICXBAR_SEL1_EPWM31	EPWM_STATICXBAR_SEL1_EPWM30	EPWM_STATICXBAR_SEL1_EPWM29	EPWM_STATICXBAR_SEL1_EPWM28
R/W	R/W	R/W	R/W
0h	0h	0h	0h
23 22	21 20	19 18	17 16
EPWM_STATICXBAR_SEL1_EPWM27	EPWM_STATICXBAR_SEL1_EPWM26	EPWM_STATICXBAR_SEL1_EPWM25	EPWM_STATICXBAR_SEL1_EPWM24
R/W	R/W	R/W	R/W
0h	0h	0h	0h
15 14	13 12	11 10	9 8
EPWM_STATICXBAR_SEL1_EPWM23	EPWM_STATICXBAR_SEL1_EPWM22	EPWM_STATICXBAR_SEL1_EPWM21	EPWM_STATICXBAR_SEL1_EPWM20
R/W	R/W	R/W	R/W
0h	0h	0h	0h
7 6	5 4	3 2	1 0
EPWM_STATICXBAR_SEL1_EPWM19	EPWM_STATICXBAR_SEL1_EPWM18	EPWM_STATICXBAR_SEL1_EPWM17	EPWM_STATICXBAR_SEL1_EPWM16
R/W	R/W	R/W	R/W
0h	0h	0h	0h

Table 2-1466. CONTROLSS_CTRL_EPWM_STATICXBAR_SEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	EPWM_STATICXBAR_SEL1_EPWM31	R/W	0h	EPWM31 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
29:28	EPWM_STATICXBAR_SEL1_EPWM30	R/W	0h	EPWM30 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
27:26	EPWM_STATICXBAR_SEL1_EPWM29	R/W	0h	EPWM29 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
25:24	EPWM_STATICXBAR_SEL1_EPWM28	R/W	0h	EPWM28 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
23:22	EPWM_STATICXBAR_SEL1_EPWM27	R/W	0h	EPWM27 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
21:20	EPWM_STATICXBAR_SEL1_EPWM26	R/W	0h	EPWM26 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
19:18	EPWM_STATICXBAR_SEL1_EPWM25	R/W	0h	EPWM25 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
17:16	EPWM_STATICXBAR_SEL1_EPWM24	R/W	0h	EPWM24 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
15:14	EPWM_STATICXBAR_SEL1_EPWM23	R/W	0h	EPWM23 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
13:12	EPWM_STATICXBAR_SEL1_EPWM22	R/W	0h	EPWM22 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3

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Table 2-1466. CONTROLSS_CTRL_EPWM_STATICXBAR_SEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	EPWM_STATICXBAR_SEL1_EPWM21	R/W	0h	EPWM21 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
9:8	EPWM_STATICXBAR_SEL1_EPWM20	R/W	0h	EPWM20 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
7:6	EPWM_STATICXBAR_SEL1_EPWM19	R/W	0h	EPWM19 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
5:4	EPWM_STATICXBAR_SEL1_EPWM18	R/W	0h	EPWM18 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
3:2	EPWM_STATICXBAR_SEL1_EPWM17	R/W	0h	EPWM17 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3
1:0	EPWM_STATICXBAR_SEL1_EPWM16	R/W	0h	EPWM16 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3

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2.6.2.3 CONTROLSS_CTRL_EPWM_CLKSYNC Register

2.6.2.3.1 CONTROLSS_CTRL_EPWM_CLKSYNC Register (Offset = 10h) [reset = 0h]

Epwm clock sync.

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Table 2-1467. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0010h

Figure 2-731. CONTROLSS_CTRL_EPWM_CLKSYNC Name Register

31	30	29	28	27	26	25	24
EPWM_CLKSYNC_BIT							
R/W							
0h							
23	22	21	20	19	18	17	16
EPWM_CLKSYNC_BIT							
R/W							
0h							
15	14	13	12	11	10	9	8
EPWM_CLKSYNC_BIT							
R/W							
0h							
7	6	5	4	3	2	1	0
EPWM_CLKSYNC_BIT							
R/W							
0h							

Table 2-1468. CONTROLSS_CTRL_EPWM_CLKSYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPWM_CLKSYNC_BIT	R/W	0h	EPWM clock sync for each EPWM instance. Set the bit corresponding to the instance number to enable that EPWM instance. When set, all enabled EPWM module clocks are started with the first rising edge of TBCLK aligned.Refer to TRM for more details. Writing 1'b1 will allow to enable corresponding EPWM instance Writing 1'b0 will disable corresponding EPWM instance.

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2.6.2.4 CONTROLSS_CTRL_SDFM1_CLK0_SEL Register

2.6.2.4.1 CONTROLSS_CTRL_SDFM1_CLK0_SEL Register (Offset = 18h) [reset = 0h]

Sdfm1 clock select.

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Table 2-1469. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0018h

Figure 2-732. CONTROLSS_CTRL_SDFM1_CLK0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SDFM1_CLK0_SEL_SEL
NONE							R/W
0h							0h

Table 2-1470. CONTROLSS_CTRL_SDFM1_CLK0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SDFM1_CLK0_SEL_SEL	R/W	0h	SDFM1 clock CK0 select Write 1'b0: source is SDFM1 CK0 from Pinmux Write 1'b1: source is SDFM0 CK0 from Pinmux

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2.6.2.5 CONTROLSS_CTRL_EMUSTOPN_MASK Register

2.6.2.5.1 CONTROLSS_CTRL_EMUSTOPN_MASK Register (Offset = 20h) [reset = 0h]

Bit-mask for debug suspend cpu cores to EPWM.

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Table 2-1471. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0020h

Figure 2-733. CONTROLSS_CTRL_EMUSTOPN_MASK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EMUSTOPN_MASK_CR5B1	EMUSTOPN_MASK_CR5A1	EMUSTOPN_MASK_CR5B0	EMUSTOPN_MASK_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1472. CONTROLSS_CTRL_EMUSTOPN_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EMUSTOPN_MASK_CR5B1	R/W	0h	Bit-mask for debug suspend cpu cores to EPWM 1'b0 : R5FSS1_CORE1 enabled to control EMUSTOPn 1'b1 : R5FSS1_CORE1 disabled to control EMUSTOPn
2	EMUSTOPN_MASK_CR5A1	R/W	0h	Bit-mask for debug suspend cpu cores to EPWM 1'b0 : R5FSS1_CORE0 enabled to control EMUSTOPn 1'b1 : R5FSS1_CORE0 disabled to control EMUSTOPn
1	EMUSTOPN_MASK_CR5B0	R/W	0h	Bit-mask for debug suspend cpu cores to EPWM 1'b0 : R5FSS0_CORE1 enabled to control EMUSTOPn 1'b1 : R5FSS0_CORE1 disabled to control EMUSTOPn
0	EMUSTOPN_MASK_CR5A0	R/W	0h	Bit-mask for debug suspend cpu cores to EPWM 1'b0 : R5FSS0_CORE0 enabled to control EMUSTOPn 1'b1 : R5FSS0_CORE0 disabled to control EMUSTOPn

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2.6.2.6 CONTROLSS_CTRL_CLB_AQ_EN0 Register

2.6.2.6.1 CONTROLSS_CTRL_CLB_AQ_EN0 Register (Offset = 28h) [reset = 0h]

clb_aq_en0.

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Table 2-1473. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0028h

Figure 2-734. CONTROLSS_CTRL_CLB_AQ_EN0 Name Register

31	30	29	28	27	26	25	24
CLB_AQ_EN0_ENABLE							
R/W							
0h							
23	22	21	20	19	18	17	16
CLB_AQ_EN0_ENABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
CLB_AQ_EN0_ENABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
CLB_AQ_EN0_ENABLE							
R/W							
0h							

Table 2-1474. CONTROLSS_CTRL_CLB_AQ_EN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLB_AQ_EN0_ENABLE	R/W	0h	Enable ICCS control to CLB_AQ signal of PWM[15:0]. Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 0-15.

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2.6.2.7 CONTROLSS_CTRL_CLB_AQ_EN1 Register

2.6.2.7.1 CONTROLSS_CTRL_CLB_AQ_EN1 Register (Offset = 30h) [reset = 0h]

clb_aq_en1.

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Table 2-1475. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0030h

Figure 2-735. CONTROLSS_CTRL_CLB_AQ_EN1 Name Register

31	30	29	28	27	26	25	24
CLB_AQ_EN1_ENABLE							
R/W							
0h							
23	22	21	20	19	18	17	16
CLB_AQ_EN1_ENABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
CLB_AQ_EN1_ENABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
CLB_AQ_EN1_ENABLE							
R/W							
0h							

Table 2-1476. CONTROLSS_CTRL_CLB_AQ_EN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLB_AQ_EN1_ENABLE	R/W	0h	Enable ICCS control to CLB_AQ signal of PWM[31:16].Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 16-31.

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2.6.2.8 CONTROLSS_CTRL_CLB_DB_EN0 Register

2.6.2.8.1 CONTROLSS_CTRL_CLB_DB_EN0 Register (Offset = 38h) [reset = 0h]

clb_db_en0.

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Table 2-1477. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0038h

Figure 2-736. CONTROLSS_CTRL_CLB_DB_EN0 Name Register

31	30	29	28	27	26	25	24
CLB_DB_EN0_ENABLE							
R/W							
0h							
23	22	21	20	19	18	17	16
CLB_DB_EN0_ENABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
CLB_DB_EN0_ENABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
CLB_DB_EN0_ENABLE							
R/W							
0h							

Table 2-1478. CONTROLSS_CTRL_CLB_DB_EN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLB_DB_EN0_ENABLE	R/W	0h	Enable ICCS control to CLB_DB signal of PWM[15:0]. Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 0-15.

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2.6.2.9 CONTROLSS_CTRL_CLB_DB_EN1 Register

2.6.2.9.1 CONTROLSS_CTRL_CLB_DB_EN1 Register (Offset = 40h) [reset = 0h]

clb_db_en1.

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Table 2-1479. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0040h

Figure 2-737. CONTROLSS_CTRL_CLB_DB_EN1 Name Register

31	30	29	28	27	26	25	24
CLB_DB_EN1_ENABLE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLB_DB_EN1_ENABLE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLB_DB_EN1_ENABLE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLB_DB_EN1_ENABLE							
R/W							
0h							

Table 2-1480. CONTROLSS_CTRL_CLB_DB_EN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLB_DB_EN1_ENABLE	R/W	0h	Enable ICCS control to CLB_DB signal of PWM[31:16].Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 16-31.

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2.6.2.10 CONTROLSS_CTRL_ADCSOCFRCGBSEL Register

2.6.2.10.1 CONTROLSS_CTRL_ADCSOCFRCGBSEL Register (Offset = 44h) [reset = 0h]

ADC Global SoC Force select.

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Table 2-1481. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0044h

Figure 2-738. CONTROLSS_CTRL_ADCSOCFRCGBSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	ADCSOCFRCGBSEL_ENABLE						
NONE	R/W						
0h	0h						

Table 2-1482. CONTROLSS_CTRL_ADCSOCFRCGBSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	ADCSOCFRCGBSEL_ENABLE	R/W	0h	ADCSOCFRCGBSEL has one bit for each ADC BIT FIELD Description bitx ADCx Indicate if ADCx selected for global SW trigger 1'b0 : Not selected for Global SW Trigger 1'b1 : Selected for Global SW TriggerReset Reset type: SYSRSn Note: x represents 0-4

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2.6.2.11 CONTROLSS_CTRL_ADCSOCFRCGB Register

2.6.2.11.1 CONTROLSS_CTRL_ADCSOCFRCGB Register (Offset = 48h) [reset = 0h]

ADC Global SOC Force.

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Table 2-1483. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0048h

Figure 2-739. CONTROLSS_CTRL_ADCSOCFRCGB Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADCSOCFRCGB_TRIG							
R/W							
0h							
7	6	5	4	3	2	1	0
ADCSOCFRCGB_TRIG							
R/W							
0h							

Table 2-1484. CONTROLSS_CTRL_ADCSOCFRCGB Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADCSOCFRCGB_TRIG	R/W	0h	ADCSOCFRCGB has one bit for each SOC[Start of conversion] BIT FIELD Description bitxx SOCxx Indicate if SOCxx selected for global SW trigger 1'b0 : Not selected for Global SW Trigger 1'b1 : Selected for Global SW Trigger Reset type: SYSRSn Note: xx represents 0-15

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2.6.2.12 CONTROLSS_CTRL_ADC_EXTCH_DLY_SEL Register

2.6.2.12.1 CONTROLSS_CTRL_ADC_EXTCH_DLY_SEL Register (Offset = 4Ch) [reset = 0h]

Mux select to choose delay for adc_extchsel.

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Table 2-1485. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 004Ch

Figure 2-740. CONTROLSS_CTRL_ADC_EXTCH_DLY_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ADC_EXTCH_DLY_SEL_SEL
NONE							R/W
0h							0h

Table 2-1486. CONTROLSS_CTRL_ADC_EXTCH_DLY_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ADC_EXTCH_DLY_SEL_SEL	R/W	0h	MUX select to choose delay Write 1'b0: 3 cycle delay[default] Write 1'b1: 6 cycle delay

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2.6.2.13 CONTROLSS_CTRL_XBAR_LOOPBACK_CTRL Register

2.6.2.13.1 CONTROLSS_CTRL_XBAR_LOOPBACK_CTRL Register (Offset = 50h) [reset = 0h]

Mux select to enable Loopback for corresponding outputXBAR.

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Table 2-1487. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0050h

Figure 2-741. CONTROLSS_CTRL_XBAR_LOOPBACK_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
XBAR_LOOPBACK_CTRL_ENABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
XBAR_LOOPBACK_CTRL_ENABLE							
R/W							
0h							

Table 2-1488. CONTROLSS_CTRL_XBAR_LOOPBACK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	XBAR_LOOPBACK_CTRL_ENABLE	R/W	0h	Mux select to enable Loopback for corresponding outputXBAR signal to the inputXBAR Write 1'b0: Loopback disabled [default] Write 1'b1: Loopback enable **Note: Each Mux select bit corresponds to the corresponding XBAR_LOOPBACK_CTRL_MUX

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2.6.2.14 CONTROLSS_CTRL_EPWM_SOCA_SEL Register

2.6.2.14.1 CONTROLSS_CTRL_EPWM_SOCA_SEL Register (Offset = 60h) [reset = 0h]

Select line to choose EPWM SOC A to EQEPx.SOCA and PWMBAR.

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Table 2-1489. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0060h

Figure 2-742. CONTROLSS_CTRL_EPWM_SOCA_SEL Name Register

31	30	29	28	27	26	25	24
EPWM_SOCA_SEL_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
EPWM_SOCA_SEL_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
EPWM_SOCA_SEL_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
EPWM_SOCA_SEL_SEL							
R/W							
0h							

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Table 2-1490. CONTROLSS_CTRL_EPWM_SOCA_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPWM_SOCA_SEL_SEL	R/W	0h	MUX select to choose EPWM SOC A to EQEPx.SOCA and PWMBAR. Each bit in SOC_A_SEL corresponds to each input EPWM_SOCA_SEL_0:pwm_soca_0 EPWM_SOCA_SEL_1:pwm_soca_1 EPWM_SOCA_SEL_2:pwm_soca_2 EPWM_SOCA_SEL_3:pwm_soca_3 EPWM_SOCA_SEL_4:pwm_soca_4 EPWM_SOCA_SEL_5:pwm_soca_5 EPWM_SOCA_SEL_6:pwm_soca_6 EPWM_SOCA_SEL_7:pwm_soca_7 EPWM_SOCA_SEL_8:pwm_soca_8 EPWM_SOCA_SEL_9:pwm_soca_9 EPWM_SOCA_SEL_10:pwm_soca_10 EPWM_SOCA_SEL_11:pwm_soca_11 EPWM_SOCA_SEL_12:pwm_soca_12 EPWM_SOCA_SEL_13:pwm_soca_13 EPWM_SOCA_SEL_14:pwm_soca_14 EPWM_SOCA_SEL_15:pwm_soca_15 EPWM_SOCA_SEL_16:pwm_soca_16 EPWM_SOCA_SEL_17:pwm_soca_17 EPWM_SOCA_SEL_18:pwm_soca_18 EPWM_SOCA_SEL_19:pwm_soca_19 EPWM_SOCA_SEL_20:pwm_soca_20 EPWM_SOCA_SEL_21:pwm_soca_21 EPWM_SOCA_SEL_22:pwm_soca_22 EPWM_SOCA_SEL_23:pwm_soca_23 EPWM_SOCA_SEL_24:pwm_soca_24 EPWM_SOCA_SEL_25:pwm_soca_25 EPWM_SOCA_SEL_26:pwm_soca_26 EPWM_SOCA_SEL_27:pwm_soca_27 EPWM_SOCA_SEL_28:pwm_soca_28 EPWM_SOCA_SEL_29:pwm_soca_29 EPWM_SOCA_SEL_30:pwm_soca_30 EPWM_SOCA_SEL_31:pwm_soca_31

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2.6.2.15 CONTROLSS_CTRL_EPWM_SOCB_SEL Register

2.6.2.15.1 CONTROLSS_CTRL_EPWM_SOCB_SEL Register (Offset = 64h) [reset = 0h]

Select line to choose EPWM SOC B to EQEPx.SOCB and PWMBAR.

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Table 2-1491. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0064h

Figure 2-743. CONTROLSS_CTRL_EPWM_SOCB_SEL Name Register

31	30	29	28	27	26	25	24
EPWM_SOCB_SEL_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
EPWM_SOCB_SEL_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
EPWM_SOCB_SEL_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
EPWM_SOCB_SEL_SEL							
R/W							
0h							

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Table 2-1492. CONTROLSS_CTRL_EPWM_SOCB_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	EPWM_SOCB_SEL_SEL	R/W	0h	MUX select to choose EPWM SOC B to EQEPx.SOCB and PWMBAR. Each bit in SOC_B_SEL corresponds to each input EPWM_SOCB_SEL_0:pwm_socb_0 EPWM_SOCB_SEL_1:pwm_socb_1 EPWM_SOCB_SEL_2:pwm_socb_2 EPWM_SOCB_SEL_3:pwm_socb_3 EPWM_SOCB_SEL_4:pwm_socb_4 EPWM_SOCB_SEL_5:pwm_socb_5 EPWM_SOCB_SEL_6:pwm_socb_6 EPWM_SOCB_SEL_7:pwm_socb_7 EPWM_SOCB_SEL_8:pwm_socb_8 EPWM_SOCB_SEL_9:pwm_socb_9 EPWM_SOCB_SEL_10:pwm_socb_10 EPWM_SOCB_SEL_11:pwm_socb_11 EPWM_SOCB_SEL_12:pwm_socb_12 EPWM_SOCB_SEL_13:pwm_socb_13 EPWM_SOCB_SEL_14:pwm_socb_14 EPWM_SOCB_SEL_15:pwm_socb_15 EPWM_SOCB_SEL_16:pwm_socb_16 EPWM_SOCB_SEL_17:pwm_socb_17 EPWM_SOCB_SEL_18:pwm_socb_18 EPWM_SOCB_SEL_19:pwm_socb_19 EPWM_SOCB_SEL_20:pwm_socb_20 EPWM_SOCB_SEL_21:pwm_socb_21 EPWM_SOCB_SEL_22:pwm_socb_22 EPWM_SOCB_SEL_23:pwm_socb_23 EPWM_SOCB_SEL_24:pwm_socb_24 EPWM_SOCB_SEL_25:pwm_socb_25 EPWM_SOCB_SEL_26:pwm_socb_26 EPWM_SOCB_SEL_27:pwm_socb_27 EPWM_SOCB_SEL_28:pwm_socb_28 EPWM_SOCB_SEL_29:pwm_socb_29 EPWM_SOCB_SEL_30:pwm_socb_30 EPWM_SOCB_SEL_31:pwm_socb_31

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2.6.2.16 CONTROLSS_CTRL_ADCEXTCHXBAR0_G0_SEL Register

2.6.2.16.1 CONTROLSS_CTRL_ADCEXTCHXBAR0_G0_SEL Register (Offset = 70h) [reset = 0h]

ADC EXTCH XBAR [x] Input Select.

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Table 2-1493. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0070h

Figure 2-744. CONTROLSS_CTRL_ADCEXTCHXBAR0_G0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADCEXTCHXBAR0_G0_SEL_SEL			
NONE				R/W			
0h				0h			

Table 2-1494. CONTROLSS_CTRL_ADCEXTCHXBAR0_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ADCEXTCHXBAR0_G0_SEL_SEL	R/W	0h	ADC EXTCH XBAR 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: ADC_R0_EXTCHSEL_BIT0 4'b1011: ADC_R0_EXTCHSEL_BIT1 4'b1100: ADC_R1_EXTCHSEL_BIT0 4'b1101: ADC_R1_EXTCHSEL_BIT1 Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBAR3.G0.SEL set to 4'b0100

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2.6.2.17 CONTROLSS_CTRL_ADCEXTCHXBAR1_G0_SEL Register

2.6.2.17.1 CONTROLSS_CTRL_ADCEXTCHXBAR1_G0_SEL Register (Offset = 74h) [reset = 0h]

ADC EXTCH XBAR [x] Input Select.

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Table 2-1495. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0074h

Figure 2-745. CONTROLSS_CTRL_ADCEXTCHXBAR1_G0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADCEXTCHXBAR1_G0_SEL_SEL			
NONE				R/W			
0h				0h			

Table 2-1496. CONTROLSS_CTRL_ADCEXTCHXBAR1_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ADCEXTCHXBAR1_G0_SEL_SEL	R/W	0h	ADC EXTCH XBAR 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: ADC_R0_EXTCHSEL_BIT0 4'b1011: ADC_R0_EXTCHSEL_BIT1 4'b1100: ADC_R1_EXTCHSEL_BIT0 4'b1101: ADC_R1_EXTCHSEL_BIT1 Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBAR3.G0.SEL set to 4'b0100

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2.6.2.18 CONTROLSS_CTRL_ADCEXTCHXBAR2_G0_SEL Register

2.6.2.18.1 CONTROLSS_CTRL_ADCEXTCHXBAR2_G0_SEL Register (Offset = 78h) [reset = 0h]

ADC EXTCH XBAR [x] Input Select.

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Table 2-1497. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0078h

Figure 2-746. CONTROLSS_CTRL_ADCEXTCHXBAR2_G0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADCEXTCHXBAR2_G0_SEL_SEL			
NONE				R/W			
0h				0h			

Table 2-1498. CONTROLSS_CTRL_ADCEXTCHXBAR2_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ADCEXTCHXBAR2_G0_SEL_SEL	R/W	0h	ADC EXTCH XBAR 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: ADC_R0_EXTCHSEL_BIT0 4'b1011: ADC_R0_EXTCHSEL_BIT1 4'b1100: ADC_R1_EXTCHSEL_BIT0 4'b1101: ADC_R1_EXTCHSEL_BIT1 Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBAR3.G0.SEL set to 4'b0100

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2.6.2.19 CONTROLSS_CTRL_ADCEXTCHXBAR3_G0_SEL Register

2.6.2.19.1 CONTROLSS_CTRL_ADCEXTCHXBAR3_G0_SEL Register (Offset = 7Ch) [reset = 0h]

ADC EXTCH XBAR [x] Input Select.

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Table 2-1499. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 007Ch

Figure 2-747. CONTROLSS_CTRL_ADCEXTCHXBAR3_G0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADCEXTCHXBAR3_G0_SEL_SEL			
NONE				R/W			
0h				0h			

Table 2-1500. CONTROLSS_CTRL_ADCEXTCHXBAR3_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ADCEXTCHXBAR3_G0_SEL_SEL	R/W	0h	ADC EXTCH XBAR 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: ADC_R0_EXTCHSEL_BIT0 4'b1011: ADC_R0_EXTCHSEL_BIT1 4'b1100: ADC_R1_EXTCHSEL_BIT0 4'b1101: ADC_R1_EXTCHSEL_BIT1 Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBAR3.G0.SEL set to 4'b0100

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2.6.2.20 CONTROLSS_CTRL_ADCEXTCHXBAR4_G0_SEL Register

2.6.2.20.1 CONTROLSS_CTRL_ADCEXTCHXBAR4_G0_SEL Register (Offset = 80h) [reset = 0h]

ADC EXTCH XBAR [x] Input Select.

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Table 2-1501. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0080h

Figure 2-748. CONTROLSS_CTRL_ADCEXTCHXBAR4_G0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ADCEXTCHXBAR4_G0_SEL_SEL			
NONE				R/W			
0h				0h			

Table 2-1502. CONTROLSS_CTRL_ADCEXTCHXBAR4_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ADCEXTCHXBAR4_G0_SEL_SEL	R/W	0h	ADC EXTCH XBAR 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: ADC_R0_EXTCHSEL_BIT0 4'b1011: ADC_R0_EXTCHSEL_BIT1 4'b1100: ADC_R1_EXTCHSEL_BIT0 4'b1101: ADC_R1_EXTCHSEL_BIT1 Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBAR3.G0.SEL set to 4'b0100

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2.6.2.21 CONTROLSS_CTRL_ADCEXTCHXBAR5_G0_SEL Register

2.6.2.21.1 CONTROLSS_CTRL_ADCEXTCHXBAR5_G0_SEL Register (Offset = 84h) [reset = 0h]

ADC EXTCH XBAR [x] Input Select.

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Table 2-1503. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0084h

Figure 2-749. CONTROLSS_CTRL_ADCEXTCHXBAR5_G0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADCEXTCHXBAR5_G0_SEL_SEL			
NONE				R/W			
0h				0h			

Table 2-1504. CONTROLSS_CTRL_ADCEXTCHXBAR5_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ADCEXTCHXBAR5_G0_SEL_SEL	R/W	0h	ADC EXTCH XBAR 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: ADC_R0_EXTCHSEL_BIT0 4'b1011: ADC_R0_EXTCHSEL_BIT1 4'b1100: ADC_R1_EXTCHSEL_BIT0 4'b1101: ADC_R1_EXTCHSEL_BIT1 Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBAR3.G0.SEL set to 4'b0100

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2.6.2.22 CONTROLSS_CTRL_ADCEXTCHXBAR6_G0_SEL Register

2.6.2.22.1 CONTROLSS_CTRL_ADCEXTCHXBAR6_G0_SEL Register (Offset = 88h) [reset = 0h]

ADC EXTCH XBAR [x] Input Select.

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Table 2-1505. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0088h

Figure 2-750. CONTROLSS_CTRL_ADCEXTCHXBAR6_G0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADCEXTCHXBAR6_G0_SEL_SEL			
NONE				R/W			
0h				0h			

Table 2-1506. CONTROLSS_CTRL_ADCEXTCHXBAR6_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ADCEXTCHXBAR6_G0_SEL_SEL	R/W	0h	ADC EXTCH XBAR 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: ADC_R0_EXTCHSEL_BIT0 4'b1011: ADC_R0_EXTCHSEL_BIT1 4'b1100: ADC_R1_EXTCHSEL_BIT0 4'b1101: ADC_R1_EXTCHSEL_BIT1 Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBAR3.G0.SEL set to 4'b0100

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2.6.2.23 CONTROLSS_CTRL_ADCEXTCHXBAR7_G0_SEL Register

2.6.2.23.1 CONTROLSS_CTRL_ADCEXTCHXBAR7_G0_SEL Register (Offset = 8Ch) [reset = 0h]

ADC EXTCH XBAR [x] Input Select.

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Table 2-1507. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 008Ch

Figure 2-751. CONTROLSS_CTRL_ADCEXTCHXBAR7_G0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADCEXTCHXBAR7_G0_SEL_SEL			
NONE				R/W			
0h				0h			

Table 2-1508. CONTROLSS_CTRL_ADCEXTCHXBAR7_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ADCEXTCHXBAR7_G0_SEL_SEL	R/W	0h	ADC EXTCH XBAR 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: ADC_R0_EXTCHSEL_BIT0 4'b1011: ADC_R0_EXTCHSEL_BIT1 4'b1100: ADC_R1_EXTCHSEL_BIT0 4'b1101: ADC_R1_EXTCHSEL_BIT1 Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBAR3.G0.SEL set to 4'b0100

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2.6.2.24 CONTROLSS_CTRL_ADCEXTCHXBAR8_G0_SEL Register

2.6.2.24.1 CONTROLSS_CTRL_ADCEXTCHXBAR8_G0_SEL Register (Offset = 90h) [reset = 0h]

ADC EXTCH XBAR [x] Input Select.

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Table 2-1509. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0090h

Figure 2-752. CONTROLSS_CTRL_ADCEXTCHXBAR8_G0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADCEXTCHXBAR8_G0_SEL_SEL			
NONE				R/W			
0h				0h			

Table 2-1510. CONTROLSS_CTRL_ADCEXTCHXBAR8_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ADCEXTCHXBAR8_G0_SEL_SEL	R/W	0h	ADC EXTCH XBAR 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: ADC_R0_EXTCHSEL_BIT0 4'b1011: ADC_R0_EXTCHSEL_BIT1 4'b1100: ADC_R1_EXTCHSEL_BIT0 4'b1101: ADC_R1_EXTCHSEL_BIT1 Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBAR3.G0.SEL set to 4'b0100

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2.6.2.25 CONTROLSS_CTRL_ADCEXTCHXBAR9_G0_SEL Register

2.6.2.25.1 CONTROLSS_CTRL_ADCEXTCHXBAR9_G0_SEL Register (Offset = 94h) [reset = 0h]

ADC EXTCH XBAR [x] Input Select.

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Table 2-1511. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0094h

Figure 2-753. CONTROLSS_CTRL_ADCEXTCHXBAR9_G0_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ADCEXTCHXBAR9_G0_SEL_SEL			
NONE				R/W			
0h				0h			

Table 2-1512. CONTROLSS_CTRL_ADCEXTCHXBAR9_G0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	ADCEXTCHXBAR9_G0_SEL_SEL	R/W	0h	ADC EXTCH XBAR 0 Input Select 4'b0000: ADC0EXTCHSEL_BIT0 4'b0001: ADC0EXTCHSEL_BIT1 4'b0010: ADC1EXTCHSEL_BIT0 4'b0011: ADC1EXTCHSEL_BIT1 4'b0100: ADC2EXTCHSEL_BIT0 4'b0101: ADC2EXTCHSEL_BIT1 4'b0110: ADC3EXTCHSEL_BIT0 4'b0111: ADC3EXTCHSEL_BIT1 4'b1000: ADC4EXTCHSEL_BIT0 4'b1001: ADC4EXTCHSEL_BIT1 4'b1010: ADC_R0_EXTCHSEL_BIT0 4'b1011: ADC_R0_EXTCHSEL_BIT1 4'b1100: ADC_R1_EXTCHSEL_BIT0 4'b1101: ADC_R1_EXTCHSEL_BIT1 Example: ADC2EXTCHSEL_BIT0 needs to be connect to ADC_EXTCH_XBAROUT3, then ADCEXTCHXBAR3.G0.SEL set to 4'b0100

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2.6.2.26 CONTROLSS_CTRL_SDFM0_CLK0_OUT_SEL Register

2.6.2.26.1 CONTROLSS_CTRL_SDFM0_CLK0_OUT_SEL Register (Offset = B0h) [reset = 0h]

SDFM0_CLK[x]_OUT Input Select.

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Table 2-1513. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00B0h

Figure 2-754. CONTROLSS_CTRL_SDFM0_CLK0_OUT_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SDFM0_CLK0_OUT_SEL_SEL
NONE							R/W
0h							0h

Table 2-1514. CONTROLSS_CTRL_SDFM0_CLK0_OUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SDFM0_CLK0_OUT_SEL_SEL	R/W	0h	SDFM0_CLK0_OUT Input select Write 1'b0: ECAP4_OUT [default] Write 1'b1: ECAP12_OUT

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2.6.2.27 CONTROLSS_CTRL_SDFM0_CLK1_OUT_SEL Register

2.6.2.27.1 CONTROLSS_CTRL_SDFM0_CLK1_OUT_SEL Register (Offset = B4h) [reset = 0h]

SDFM0_CLK[x]_OUT Input Select.

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Table 2-1515. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00B4h

Figure 2-755. CONTROLSS_CTRL_SDFM0_CLK1_OUT_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SDFM0_CLK1_OUT_SEL_SEL
NONE							R/W
0h							0h

Table 2-1516. CONTROLSS_CTRL_SDFM0_CLK1_OUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SDFM0_CLK1_OUT_SEL_SEL	R/W	0h	SDFM0_CLK1_OUT Input select Write 1'b0: ECAP5_OUT [default] Write 1'b1: ECAP13_OUT

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2.6.2.28 CONTROLSS_CTRL_SDFM0_CLK2_OUT_SEL Register

2.6.2.28.1 CONTROLSS_CTRL_SDFM0_CLK2_OUT_SEL Register (Offset = B8h) [reset = 0h]

SDFM0_CLK[x]_OUT Input Select.

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Table 2-1517. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00B8h

Figure 2-756. CONTROLSS_CTRL_SDFM0_CLK2_OUT_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SDFM0_CLK2_OUT_SEL_SEL
NONE							R/W
0h							0h

Table 2-1518. CONTROLSS_CTRL_SDFM0_CLK2_OUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SDFM0_CLK2_OUT_SEL_SEL	R/W	0h	SDFM0_CLK2_OUT Input select Write 1'b0: ECAP6_OUT [default] Write 1'b1: ECAP14_OUT

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2.6.2.29 CONTROLSS_CTRL_SDFM0_CLK3_OUT_SEL Register

2.6.2.29.1 CONTROLSS_CTRL_SDFM0_CLK3_OUT_SEL Register (Offset = BCh) [reset = 0h]

SDFM0_CLK[x]_OUT Input Select.

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Table 2-1519. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00BCh

Figure 2-757. CONTROLSS_CTRL_SDFM0_CLK3_OUT_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SDFM0_CLK3_OUT_SEL_SEL
NONE							R/W
0h							0h

Table 2-1520. CONTROLSS_CTRL_SDFM0_CLK3_OUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SDFM0_CLK3_OUT_SEL_SEL	R/W	0h	SDFM0_CLK3_OUT Input select Write 1'b0: ECAP7_OUT [default] Write 1'b1: ECAP15_OUT

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2.6.2.30 CONTROLSS_CTRL_SDFM1_CLK0_OUT_SEL Register

2.6.2.30.1 CONTROLSS_CTRL_SDFM1_CLK0_OUT_SEL Register (Offset = C0h) [reset = 0h]

SDFM1_CLK[x]_OUT Input Select.

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Table 2-1521. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00C0h

Figure 2-758. CONTROLSS_CTRL_SDFM1_CLK0_OUT_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SDFM1_CLK0_OUT_SEL_SEL
NONE							R/W
0h							0h

Table 2-1522. CONTROLSS_CTRL_SDFM1_CLK0_OUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SDFM1_CLK0_OUT_SEL_SEL	R/W	0h	SDFM1_CLK0_OUT Input select Write 1'b0: ECAP7_OUT [default] Write 1'b1: ECAP15_OUT

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2.6.2.31 CONTROLSS_CTRL_SDFM1_CLK1_OUT_SEL Register

2.6.2.31.1 CONTROLSS_CTRL_SDFM1_CLK1_OUT_SEL Register (Offset = C4h) [reset = 0h]

SDFM1_CLK[x]_OUT Input Select.

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Table 2-1523. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00C4h

Figure 2-759. CONTROLSS_CTRL_SDFM1_CLK1_OUT_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SDFM1_CLK1_OUT_SEL_SEL
NONE							R/W
0h							0h

Table 2-1524. CONTROLSS_CTRL_SDFM1_CLK1_OUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SDFM1_CLK1_OUT_SEL_SEL	R/W	0h	SDFM1_CLK1_OUT Input select Write 1'b0: ECAP6_OUT [default] Write 1'b1: ECAP14_OUT

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2.6.2.32 CONTROLSS_CTRL_SDFM1_CLK2_OUT_SEL Register

2.6.2.32.1 CONTROLSS_CTRL_SDFM1_CLK2_OUT_SEL Register (Offset = C8h) [reset = 0h]

SDFM1_CLK[x]_OUT Input Select.

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Table 2-1525. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00C8h

Figure 2-760. CONTROLSS_CTRL_SDFM1_CLK2_OUT_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SDFM1_CLK2_OUT_SEL_SEL
NONE							R/W
0h							0h

Table 2-1526. CONTROLSS_CTRL_SDFM1_CLK2_OUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SDFM1_CLK2_OUT_SEL_SEL	R/W	0h	SDFM1_CLK2_OUT Input select Write 1'b0: ECAP5_OUT [default] Write 1'b1: ECAP13_OUT

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2.6.2.33 CONTROLSS_CTRL_SDFM1_CLK3_OUT_SEL Register

2.6.2.33.1 CONTROLSS_CTRL_SDFM1_CLK3_OUT_SEL Register (Offset = CCh) [reset = 0h]

SDFM1_CLK[x]_OUT Input Select.

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Table 2-1527. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00CCh

Figure 2-761. CONTROLSS_CTRL_SDFM1_CLK3_OUT_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SDFM1_CLK3_OUT_SEL_SEL
NONE							R/W
0h							0h

Table 2-1528. CONTROLSS_CTRL_SDFM1_CLK3_OUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SDFM1_CLK3_OUT_SEL_SEL	R/W	0h	SDFM1_CLK3_OUT Input select Write 1'b0: ECAP4_OUT [default] Write 1'b1: ECAP12_OUT

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2.6.2.34 CONTROLSS_CTRL_CONTROLSS_G0_EPWM_WLINK Register

2.6.2.34.1 CONTROLSS_CTRL_CONTROLSS_G0_EPWM_WLINK Register (Offset = E0h) [reset = 0h]

Enable for WLINK of EPWM groups.

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Table 2-1529. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00E0h

Figure 2-762. CONTROLSS_CTRL_CONTROLSS_G0_EPWM_WLINK Name Register

31	30	29	28	27	26	25	24
CONTROLSS_G0_EPWM_WLINK_ENABLE							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTROLSS_G0_EPWM_WLINK_ENABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTROLSS_G0_EPWM_WLINK_ENABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTROLSS_G0_EPWM_WLINK_ENABLE							
R/W							
0h							

Table 2-1530. CONTROLSS_CTRL_CONTROLSS_G0_EPWM_WLINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTROLSS_G0_EPWM_WLINK_ENABLE	R/W	0h	Writing 1'b1 to the bit enables the corresponding EPWM instance for WLINK feature

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2.6.2.35 CONTROLSS_CTRL_CONTROLSS_G1_EPWM_WLINK Register

2.6.2.35.1 CONTROLSS_CTRL_CONTROLSS_G1_EPWM_WLINK Register (Offset = E4h) [reset = 0h]

Enable for WLINK of EPWM groups.

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Table 2-1531. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00E4h

Figure 2-763. CONTROLSS_CTRL_CONTROLSS_G1_EPWM_WLINK Name Register

31	30	29	28	27	26	25	24
CONTROLSS_G1_EPWM_WLINK_ENABLE							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTROLSS_G1_EPWM_WLINK_ENABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTROLSS_G1_EPWM_WLINK_ENABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTROLSS_G1_EPWM_WLINK_ENABLE							
R/W							
0h							

Table 2-1532. CONTROLSS_CTRL_CONTROLSS_G1_EPWM_WLINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTROLSS_G1_EPWM_WLINK_ENABLE	R/W	0h	Writing 1'b1 to the bit enables the corresponding EPWM instance for WLINK feature

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2.6.2.36 CONTROLSS_CTRL_CONTROLSS_G2_EPWM_WLINK Register

2.6.2.36.1 CONTROLSS_CTRL_CONTROLSS_G2_EPWM_WLINK Register (Offset = E8h) [reset = 0h]

Enable for WLINK of EPWM groups.

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Table 2-1533. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00E8h

Figure 2-764. CONTROLSS_CTRL_CONTROLSS_G2_EPWM_WLINK Name Register

31	30	29	28	27	26	25	24
CONTROLSS_G2_EPWM_WLINK_ENABLE							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTROLSS_G2_EPWM_WLINK_ENABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTROLSS_G2_EPWM_WLINK_ENABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTROLSS_G2_EPWM_WLINK_ENABLE							
R/W							
0h							

Table 2-1534. CONTROLSS_CTRL_CONTROLSS_G2_EPWM_WLINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTROLSS_G2_EPWM_WLINK_ENABLE	R/W	0h	Writing 1'b1 to the bit enables the corresponding EPWM instance for WLINK feature

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2.6.2.37 CONTROLSS_CTRL_CONTROLSS_G3_EPWM_WLINK Register

2.6.2.37.1 CONTROLSS_CTRL_CONTROLSS_G3_EPWM_WLINK Register (Offset = ECh) [reset = 0h]

Enable for WLINK of EPWM groups.

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Table 2-1535. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 00ECh

Figure 2-765. CONTROLSS_CTRL_CONTROLSS_G3_EPWM_WLINK Name Register

31	30	29	28	27	26	25	24
CONTROLSS_G3_EPWM_WLINK_ENABLE							
R/W							
0h							
23	22	21	20	19	18	17	16
CONTROLSS_G3_EPWM_WLINK_ENABLE							
R/W							
0h							
15	14	13	12	11	10	9	8
CONTROLSS_G3_EPWM_WLINK_ENABLE							
R/W							
0h							
7	6	5	4	3	2	1	0
CONTROLSS_G3_EPWM_WLINK_ENABLE							
R/W							
0h							

Table 2-1536. CONTROLSS_CTRL_CONTROLSS_G3_EPWM_WLINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CONTROLSS_G3_EPWM_WLINK_ENABLE	R/W	0h	Writing 1'b1 to the bit enables the corresponding EPWM instance for WLINK feature

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2.6.2.38 CONTROLSS_CTRL_EPWM0_CLK_GATE Register

2.6.2.38.1 CONTROLSS_CTRL_EPWM0_CLK_GATE Register (Offset = 100h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1537. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0100h

Figure 2-766. CONTROLSS_CTRL_EPWM0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1538. CONTROLSS_CTRL_EPWM0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.39 CONTROLSS_CTRL_EPWM1_CLK_GATE Register

2.6.2.39.1 CONTROLSS_CTRL_EPWM1_CLK_GATE Register (Offset = 104h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1539. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0104h

Figure 2-767. CONTROLSS_CTRL_EPWM1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1540. CONTROLSS_CTRL_EPWM1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.40 CONTROLSS_CTRL_EPWM2_CLK_GATE Register

2.6.2.40.1 CONTROLSS_CTRL_EPWM2_CLK_GATE Register (Offset = 108h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1541. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0108h

Figure 2-768. CONTROLSS_CTRL_EPWM2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM2_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1542. CONTROLSS_CTRL_EPWM2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM2_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.41 CONTROLSS_CTRL_EPWM3_CLK_GATE Register

2.6.2.41.1 CONTROLSS_CTRL_EPWM3_CLK_GATE Register (Offset = 10Ch) [reset = 0h]

To clock gate epwm[x].

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Table 2-1543. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 010Ch

Figure 2-769. CONTROLSS_CTRL_EPWM3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM3_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1544. CONTROLSS_CTRL_EPWM3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM3_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.42 CONTROLSS_CTRL_EPWM4_CLK_GATE Register

2.6.2.42.1 CONTROLSS_CTRL_EPWM4_CLK_GATE Register (Offset = 110h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1545. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0110h

Figure 2-770. CONTROLSS_CTRL_EPWM4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM4_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1546. CONTROLSS_CTRL_EPWM4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM4_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.43 CONTROLSS_CTRL_EPWM5_CLK_GATE Register

2.6.2.43.1 CONTROLSS_CTRL_EPWM5_CLK_GATE Register (Offset = 114h) [reset = 0h]

To clock gate epwm[x].

Return to Summary Table

Table 2-1547. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0114h

Figure 2-771. CONTROLSS_CTRL_EPWM5_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM5_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1548. CONTROLSS_CTRL_EPWM5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM5_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.44 CONTROLSS_CTRL_EPWM6_CLK_GATE Register

2.6.2.44.1 CONTROLSS_CTRL_EPWM6_CLK_GATE Register (Offset = 118h) [reset = 0h]

To clock gate epwm[x].

Return to Summary Table

Table 2-1549. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0118h

Figure 2-772. CONTROLSS_CTRL_EPWM6_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM6_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1550. CONTROLSS_CTRL_EPWM6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM6_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.45 CONTROLSS_CTRL_EPWM7_CLK_GATE Register

2.6.2.45.1 CONTROLSS_CTRL_EPWM7_CLK_GATE Register (Offset = 11Ch) [reset = 0h]

To clock gate epwm[x].

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Table 2-1551. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 011Ch

Figure 2-773. CONTROLSS_CTRL_EPWM7_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM7_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1552. CONTROLSS_CTRL_EPWM7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM7_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.46 CONTROLSS_CTRL_EPWM8_CLK_GATE Register

2.6.2.46.1 CONTROLSS_CTRL_EPWM8_CLK_GATE Register (Offset = 120h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1553. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0120h

Figure 2-774. CONTROLSS_CTRL_EPWM8_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM8_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1554. CONTROLSS_CTRL_EPWM8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM8_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.47 CONTROLSS_CTRL_EPWM9_CLK_GATE Register

2.6.2.47.1 CONTROLSS_CTRL_EPWM9_CLK_GATE Register (Offset = 124h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1555. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0124h

Figure 2-775. CONTROLSS_CTRL_EPWM9_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM9_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1556. CONTROLSS_CTRL_EPWM9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM9_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.48 CONTROLSS_CTRL_EPWM10_CLK_GATE Register

2.6.2.48.1 CONTROLSS_CTRL_EPWM10_CLK_GATE Register (Offset = 128h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1557. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0128h

Figure 2-776. CONTROLSS_CTRL_EPWM10_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM10_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1558. CONTROLSS_CTRL_EPWM10_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM10_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.49 CONTROLSS_CTRL_EPWM11_CLK_GATE Register

2.6.2.49.1 CONTROLSS_CTRL_EPWM11_CLK_GATE Register (Offset = 12Ch) [reset = 0h]

To clock gate epwm[x].

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Table 2-1559. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 012Ch

Figure 2-777. CONTROLSS_CTRL_EPWM11_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM11_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1560. CONTROLSS_CTRL_EPWM11_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM11_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.50 CONTROLSS_CTRL_EPWM12_CLK_GATE Register

2.6.2.50.1 CONTROLSS_CTRL_EPWM12_CLK_GATE Register (Offset = 130h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1561. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0130h

Figure 2-778. CONTROLSS_CTRL_EPWM12_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM12_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1562. CONTROLSS_CTRL_EPWM12_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM12_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.51 CONTROLSS_CTRL_EPWM13_CLK_GATE Register

2.6.2.51.1 CONTROLSS_CTRL_EPWM13_CLK_GATE Register (Offset = 134h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1563. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0134h

Figure 2-779. CONTROLSS_CTRL_EPWM13_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM13_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1564. CONTROLSS_CTRL_EPWM13_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM13_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.52 CONTROLSS_CTRL_EPWM14_CLK_GATE Register

2.6.2.52.1 CONTROLSS_CTRL_EPWM14_CLK_GATE Register (Offset = 138h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1565. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0138h

Figure 2-780. CONTROLSS_CTRL_EPWM14_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM14_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1566. CONTROLSS_CTRL_EPWM14_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM14_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.53 CONTROLSS_CTRL_EPWM15_CLK_GATE Register

2.6.2.53.1 CONTROLSS_CTRL_EPWM15_CLK_GATE Register (Offset = 13Ch) [reset = 0h]

To clock gate epwm[x].

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Table 2-1567. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 013Ch

Figure 2-781. CONTROLSS_CTRL_EPWM15_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM15_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1568. CONTROLSS_CTRL_EPWM15_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM15_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.54 CONTROLSS_CTRL_EPWM16_CLK_GATE Register

2.6.2.54.1 CONTROLSS_CTRL_EPWM16_CLK_GATE Register (Offset = 140h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1569. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0140h

Figure 2-782. CONTROLSS_CTRL_EPWM16_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM16_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1570. CONTROLSS_CTRL_EPWM16_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM16_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.55 CONTROLSS_CTRL_EPWM17_CLK_GATE Register

2.6.2.55.1 CONTROLSS_CTRL_EPWM17_CLK_GATE Register (Offset = 144h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1571. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0144h

Figure 2-783. CONTROLSS_CTRL_EPWM17_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EPWM17_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1572. CONTROLSS_CTRL_EPWM17_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM17_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.56 CONTROLSS_CTRL_EPWM18_CLK_GATE Register

2.6.2.56.1 CONTROLSS_CTRL_EPWM18_CLK_GATE Register (Offset = 148h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1573. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0148h

Figure 2-784. CONTROLSS_CTRL_EPWM18_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM18_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1574. CONTROLSS_CTRL_EPWM18_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM18_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.57 CONTROLSS_CTRL_EPWM19_CLK_GATE Register

2.6.2.57.1 CONTROLSS_CTRL_EPWM19_CLK_GATE Register (Offset = 14Ch) [reset = 0h]

To clock gate epwm[x].

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Table 2-1575. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 014Ch

Figure 2-785. CONTROLSS_CTRL_EPWM19_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM19_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1576. CONTROLSS_CTRL_EPWM19_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM19_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.58 CONTROLSS_CTRL_EPWM20_CLK_GATE Register

2.6.2.58.1 CONTROLSS_CTRL_EPWM20_CLK_GATE Register (Offset = 150h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1577. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0150h

Figure 2-786. CONTROLSS_CTRL_EPWM20_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM20_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1578. CONTROLSS_CTRL_EPWM20_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM20_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.59 CONTROLSS_CTRL_EPWM21_CLK_GATE Register

2.6.2.59.1 CONTROLSS_CTRL_EPWM21_CLK_GATE Register (Offset = 154h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1579. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0154h

Figure 2-787. CONTROLSS_CTRL_EPWM21_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM21_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1580. CONTROLSS_CTRL_EPWM21_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM21_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.60 CONTROLSS_CTRL_EPWM22_CLK_GATE Register

2.6.2.60.1 CONTROLSS_CTRL_EPWM22_CLK_GATE Register (Offset = 158h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1581. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0158h

Figure 2-788. CONTROLSS_CTRL_EPWM22_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM22_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1582. CONTROLSS_CTRL_EPWM22_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM22_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.61 CONTROLSS_CTRL_EPWM23_CLK_GATE Register

2.6.2.61.1 CONTROLSS_CTRL_EPWM23_CLK_GATE Register (Offset = 15Ch) [reset = 0h]

To clock gate epwm[x].

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Table 2-1583. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 015Ch

Figure 2-789. CONTROLSS_CTRL_EPWM23_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM23_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1584. CONTROLSS_CTRL_EPWM23_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM23_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.62 CONTROLSS_CTRL_EPWM24_CLK_GATE Register

2.6.2.62.1 CONTROLSS_CTRL_EPWM24_CLK_GATE Register (Offset = 160h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1585. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0160h

Figure 2-790. CONTROLSS_CTRL_EPWM24_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM24_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1586. CONTROLSS_CTRL_EPWM24_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM24_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.63 CONTROLSS_CTRL_EPWM25_CLK_GATE Register

2.6.2.63.1 CONTROLSS_CTRL_EPWM25_CLK_GATE Register (Offset = 164h) [reset = 0h]

To clock gate epwm[x].

Return to Summary Table

Table 2-1587. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0164h

Figure 2-791. CONTROLSS_CTRL_EPWM25_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM25_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1588. CONTROLSS_CTRL_EPWM25_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM25_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.64 CONTROLSS_CTRL_EPWM26_CLK_GATE Register

2.6.2.64.1 CONTROLSS_CTRL_EPWM26_CLK_GATE Register (Offset = 168h) [reset = 0h]

To clock gate epwm[x].

Return to Summary Table

Table 2-1589. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0168h

Figure 2-792. CONTROLSS_CTRL_EPWM26_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM26_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1590. CONTROLSS_CTRL_EPWM26_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM26_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.65 CONTROLSS_CTRL_EPWM27_CLK_GATE Register

2.6.2.65.1 CONTROLSS_CTRL_EPWM27_CLK_GATE Register (Offset = 16Ch) [reset = 0h]

To clock gate epwm[x].

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Table 2-1591. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 016Ch

Figure 2-793. CONTROLSS_CTRL_EPWM27_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM27_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1592. CONTROLSS_CTRL_EPWM27_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM27_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.66 CONTROLSS_CTRL_EPWM28_CLK_GATE Register

2.6.2.66.1 CONTROLSS_CTRL_EPWM28_CLK_GATE Register (Offset = 170h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1593. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0170h

Figure 2-794. CONTROLSS_CTRL_EPWM28_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM28_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1594. CONTROLSS_CTRL_EPWM28_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM28_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.67 CONTROLSS_CTRL_EPWM29_CLK_GATE Register

2.6.2.67.1 CONTROLSS_CTRL_EPWM29_CLK_GATE Register (Offset = 174h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1595. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0174h

Figure 2-795. CONTROLSS_CTRL_EPWM29_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM29_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1596. CONTROLSS_CTRL_EPWM29_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM29_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.68 CONTROLSS_CTRL_EPWM30_CLK_GATE Register

2.6.2.68.1 CONTROLSS_CTRL_EPWM30_CLK_GATE Register (Offset = 178h) [reset = 0h]

To clock gate epwm[x].

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Table 2-1597. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0178h

Figure 2-796. CONTROLSS_CTRL_EPWM30_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM30_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1598. CONTROLSS_CTRL_EPWM30_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM30_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.69 CONTROLSS_CTRL_EPWM31_CLK_GATE Register

2.6.2.69.1 CONTROLSS_CTRL_EPWM31_CLK_GATE Register (Offset = 17Ch) [reset = 0h]

To clock gate epwm[x].

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Table 2-1599. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 017Ch

Figure 2-797. CONTROLSS_CTRL_EPWM31_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM31_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1600. CONTROLSS_CTRL_EPWM31_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM31_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding epwm

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2.6.2.70 CONTROLSS_CTRL_FSI_TX0_CLK_GATE Register

2.6.2.70.1 CONTROLSS_CTRL_FSI_TX0_CLK_GATE Register (Offset = 180h) [reset = 0h]

fsi_tx[x] clock gate.

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Table 2-1601. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0180h

Figure 2-798. CONTROLSS_CTRL_FSI_TX0_CLK_GATE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">FSI_TX0_CLK_GATE_CLK_GATE</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 2-1602. CONTROLSS_CTRL_FSI_TX0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi_tx

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2.6.2.71 CONTROLSS_CTRL_FSI_TX1_CLK_GATE Register

2.6.2.71.1 CONTROLSS_CTRL_FSI_TX1_CLK_GATE Register (Offset = 184h) [reset = 0h]

fsi_tx[x] clock gate.

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Table 2-1603. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0184h

Figure 2-799. CONTROLSS_CTRL_FSI_TX1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_TX1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1604. CONTROLSS_CTRL_FSI_TX1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi_tx

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2.6.2.72 CONTROLSS_CTRL_FSI_TX2_CLK_GATE Register

2.6.2.72.1 CONTROLSS_CTRL_FSI_TX2_CLK_GATE Register (Offset = 188h) [reset = 0h]

fsi_tx[x] clock gate.

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Table 2-1605. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0188h

Figure 2-800. CONTROLSS_CTRL_FSI_TX2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_TX2_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1606. CONTROLSS_CTRL_FSI_TX2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX2_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi_tx

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2.6.2.73 CONTROLSS_CTRL_FSI_TX3_CLK_GATE Register

2.6.2.73.1 CONTROLSS_CTRL_FSI_TX3_CLK_GATE Register (Offset = 18Ch) [reset = 0h]

fsi_tx[x] clock gate.

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Table 2-1607. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 018Ch

Figure 2-801. CONTROLSS_CTRL_FSI_TX3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_TX3_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1608. CONTROLSS_CTRL_FSI_TX3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX3_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi_tx

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2.6.2.74 CONTROLSS_CTRL_FSI_RX0_CLK_GATE Register

2.6.2.74.1 CONTROLSS_CTRL_FSI_RX0_CLK_GATE Register (Offset = 190h) [reset = 0h]

fsi_rx[x] clock gate.

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Table 2-1609. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0190h

Figure 2-802. CONTROLSS_CTRL_FSI_RX0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_RX0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1610. CONTROLSS_CTRL_FSI_RX0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_RX0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi_rx

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2.6.2.75 CONTROLSS_CTRL_FSI_RX1_CLK_GATE Register

2.6.2.75.1 CONTROLSS_CTRL_FSI_RX1_CLK_GATE Register (Offset = 194h) [reset = 0h]

fsi_rx[x] clock gate.

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Table 2-1611. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0194h

Figure 2-803. CONTROLSS_CTRL_FSI_RX1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_RX1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1612. CONTROLSS_CTRL_FSI_RX1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_RX1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi_rx

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2.6.2.76 CONTROLSS_CTRL_FSI_RX2_CLK_GATE Register

2.6.2.76.1 CONTROLSS_CTRL_FSI_RX2_CLK_GATE Register (Offset = 198h) [reset = 0h]

fsi_rx[x] clock gate.

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Table 2-1613. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0198h

Figure 2-804. CONTROLSS_CTRL_FSI_RX2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_RX2_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1614. CONTROLSS_CTRL_FSI_RX2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_RX2_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi_rx

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2.6.2.77 CONTROLSS_CTRL_FSI_RX3_CLK_GATE Register

2.6.2.77.1 CONTROLSS_CTRL_FSI_RX3_CLK_GATE Register (Offset = 19Ch) [reset = 0h]

fsi_rx[x] clock gate.

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Table 2-1615. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 019Ch

Figure 2-805. CONTROLSS_CTRL_FSI_RX3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_RX3_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1616. CONTROLSS_CTRL_FSI_RX3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_RX3_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi_rx

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2.6.2.78 CONTROLSS_CTRL_CMPSSA0_CLK_GATE Register

2.6.2.78.1 CONTROLSS_CTRL_CMPSSA0_CLK_GATE Register (Offset = 1A0h) [reset = 0h]

cmpssa[x] clock gate.

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Table 2-1617. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01A0h

Figure 2-806. CONTROLSS_CTRL_CMPSSA0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1618. CONTROLSS_CTRL_CMPSSA0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssa

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2.6.2.79 CONTROLSS_CTRL_CMPSSA1_CLK_GATE Register

2.6.2.79.1 CONTROLSS_CTRL_CMPSSA1_CLK_GATE Register (Offset = 1A4h) [reset = 0h]

cmpssa[x] clock gate.

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Table 2-1619. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01A4h

Figure 2-807. CONTROLSS_CTRL_CMPSSA1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1620. CONTROLSS_CTRL_CMPSSA1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssa

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2.6.2.80 CONTROLSS_CTRL_CMPSSA2_CLK_GATE Register

2.6.2.80.1 CONTROLSS_CTRL_CMPSSA2_CLK_GATE Register (Offset = 1A8h) [reset = 0h]

cmpssa[x] clock gate.

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Table 2-1621. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01A8h

Figure 2-808. CONTROLSS_CTRL_CMPSSA2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA2_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1622. CONTROLSS_CTRL_CMPSSA2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA2_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssa

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2.6.2.81 CONTROLSS_CTRL_CMPSSA3_CLK_GATE Register

2.6.2.81.1 CONTROLSS_CTRL_CMPSSA3_CLK_GATE Register (Offset = 1ACh) [reset = 0h]

cmpssa[x] clock gate.

Return to Summary Table

Table 2-1623. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01ACh

Figure 2-809. CONTROLSS_CTRL_CMPSSA3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSA3_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1624. CONTROLSS_CTRL_CMPSSA3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA3_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssa

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2.6.2.82 CONTROLSS_CTRL_CMPSSA4_CLK_GATE Register

2.6.2.82.1 CONTROLSS_CTRL_CMPSSA4_CLK_GATE Register (Offset = 1B0h) [reset = 0h]

cmpssa[x] clock gate.

Return to Summary Table

Table 2-1625. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01B0h

Figure 2-810. CONTROLSS_CTRL_CMPSSA4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA4_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1626. CONTROLSS_CTRL_CMPSSA4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA4_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssa

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2.6.2.83 CONTROLSS_CTRL_CMPSSA5_CLK_GATE Register

2.6.2.83.1 CONTROLSS_CTRL_CMPSSA5_CLK_GATE Register (Offset = 1B4h) [reset = 0h]

cmpssa[x] clock gate.

Return to Summary Table

Table 2-1627. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01B4h

Figure 2-811. CONTROLSS_CTRL_CMPSSA5_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA5_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1628. CONTROLSS_CTRL_CMPSSA5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA5_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssa

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2.6.2.84 CONTROLSS_CTRL_CMPSSA6_CLK_GATE Register

2.6.2.84.1 CONTROLSS_CTRL_CMPSSA6_CLK_GATE Register (Offset = 1B8h) [reset = 0h]

cmpssa[x] clock gate.

Return to Summary Table

Table 2-1629. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01B8h

Figure 2-812. CONTROLSS_CTRL_CMPSSA6_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA6_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1630. CONTROLSS_CTRL_CMPSSA6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA6_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssa

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2.6.2.85 CONTROLSS_CTRL_CMPSSA7_CLK_GATE Register

2.6.2.85.1 CONTROLSS_CTRL_CMPSSA7_CLK_GATE Register (Offset = 1BCh) [reset = 0h]

cmpssa[x] clock gate.

Return to Summary Table

Table 2-1631. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01BCh

Figure 2-813. CONTROLSS_CTRL_CMPSSA7_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA7_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1632. CONTROLSS_CTRL_CMPSSA7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA7_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssa

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2.6.2.86 CONTROLSS_CTRL_CMPSSA8_CLK_GATE Register

2.6.2.86.1 CONTROLSS_CTRL_CMPSSA8_CLK_GATE Register (Offset = 1C0h) [reset = 0h]

cmpssa[x] clock gate.

Return to Summary Table

Table 2-1633. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01C0h

Figure 2-814. CONTROLSS_CTRL_CMPSSA8_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA8_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1634. CONTROLSS_CTRL_CMPSSA8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA8_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssa

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2.6.2.87 CONTROLSS_CTRL_CMPSSA9_CLK_GATE Register

2.6.2.87.1 CONTROLSS_CTRL_CMPSSA9_CLK_GATE Register (Offset = 1C4h) [reset = 0h]

cmpssa[x] clock gate.

Return to Summary Table

Table 2-1635. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01C4h

Figure 2-815. CONTROLSS_CTRL_CMPSSA9_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA9_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1636. CONTROLSS_CTRL_CMPSSA9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA9_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssa

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2.6.2.88 CONTROLSS_CTRL_CMPSSB0_CLK_GATE Register

2.6.2.88.1 CONTROLSS_CTRL_CMPSSB0_CLK_GATE Register (Offset = 1D0h) [reset = 0h]

cmpssb[x] clock gate.

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Table 2-1637. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01D0h

Figure 2-816. CONTROLSS_CTRL_CMPSSB0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1638. CONTROLSS_CTRL_CMPSSB0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssb

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2.6.2.89 CONTROLSS_CTRL_CMPSSB1_CLK_GATE Register

2.6.2.89.1 CONTROLSS_CTRL_CMPSSB1_CLK_GATE Register (Offset = 1D4h) [reset = 0h]

cmpssb[x] clock gate.

Return to Summary Table

Table 2-1639. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01D4h

Figure 2-817. CONTROLSS_CTRL_CMPSSB1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1640. CONTROLSS_CTRL_CMPSSB1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssb

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2.6.2.90 CONTROLSS_CTRL_CMPSSB2_CLK_GATE Register

2.6.2.90.1 CONTROLSS_CTRL_CMPSSB2_CLK_GATE Register (Offset = 1D8h) [reset = 0h]

cmpssb[x] clock gate.

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Table 2-1641. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01D8h

Figure 2-818. CONTROLSS_CTRL_CMPSSB2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB2_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1642. CONTROLSS_CTRL_CMPSSB2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB2_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssb

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2.6.2.91 CONTROLSS_CTRL_CMPSSB3_CLK_GATE Register

2.6.2.91.1 CONTROLSS_CTRL_CMPSSB3_CLK_GATE Register (Offset = 1DCh) [reset = 0h]

cmpssb[x] clock gate.

Return to Summary Table

Table 2-1643. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01DCh

Figure 2-819. CONTROLSS_CTRL_CMPSSB3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB3_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1644. CONTROLSS_CTRL_CMPSSB3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB3_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssb

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2.6.2.92 CONTROLSS_CTRL_CMPSSB4_CLK_GATE Register

2.6.2.92.1 CONTROLSS_CTRL_CMPSSB4_CLK_GATE Register (Offset = 1E0h) [reset = 0h]

cmpssb[x] clock gate.

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Table 2-1645. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01E0h

Figure 2-820. CONTROLSS_CTRL_CMPSSB4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB4_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1646. CONTROLSS_CTRL_CMPSSB4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB4_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssb

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2.6.2.93 CONTROLSS_CTRL_CMPSSB5_CLK_GATE Register

2.6.2.93.1 CONTROLSS_CTRL_CMPSSB5_CLK_GATE Register (Offset = 1E4h) [reset = 0h]

cmpssb[x] clock gate.

Return to Summary Table

Table 2-1647. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01E4h

Figure 2-821. CONTROLSS_CTRL_CMPSSB5_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB5_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1648. CONTROLSS_CTRL_CMPSSB5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB5_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssb

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2.6.2.94 CONTROLSS_CTRL_CMPSSB6_CLK_GATE Register

2.6.2.94.1 CONTROLSS_CTRL_CMPSSB6_CLK_GATE Register (Offset = 1E8h) [reset = 0h]

cmpssb[x] clock gate.

Return to Summary Table

Table 2-1649. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01E8h

Figure 2-822. CONTROLSS_CTRL_CMPSSB6_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSB6_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1650. CONTROLSS_CTRL_CMPSSB6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB6_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssb

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2.6.2.95 CONTROLSS_CTRL_CMPSSB7_CLK_GATE Register

2.6.2.95.1 CONTROLSS_CTRL_CMPSSB7_CLK_GATE Register (Offset = 1ECh) [reset = 0h]

cmpssb[x] clock gate.

Return to Summary Table

Table 2-1651. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01ECh

Figure 2-823. CONTROLSS_CTRL_CMPSSB7_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB7_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1652. CONTROLSS_CTRL_CMPSSB7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB7_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssb

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2.6.2.96 CONTROLSS_CTRL_CMPSSB8_CLK_GATE Register

2.6.2.96.1 CONTROLSS_CTRL_CMPSSB8_CLK_GATE Register (Offset = 1F0h) [reset = 0h]

cmpssb[x] clock gate.

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Table 2-1653. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01F0h

Figure 2-824. CONTROLSS_CTRL_CMPSSB8_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB8_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1654. CONTROLSS_CTRL_CMPSSB8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB8_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssb

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2.6.2.97 CONTROLSS_CTRL_CMPSSB9_CLK_GATE Register

2.6.2.97.1 CONTROLSS_CTRL_CMPSSB9_CLK_GATE Register (Offset = 1F4h) [reset = 0h]

cmpssb[x] clock gate.

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Table 2-1655. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 01F4h

Figure 2-825. CONTROLSS_CTRL_CMPSSB9_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB9_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1656. CONTROLSS_CTRL_CMPSSB9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB9_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding cmpssb

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2.6.2.98 CONTROLSS_CTRL_ECAP0_CLK_GATE Register

2.6.2.98.1 CONTROLSS_CTRL_ECAP0_CLK_GATE Register (Offset = 200h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1657. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0200h

Figure 2-826. CONTROLSS_CTRL_ECAP0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1658. CONTROLSS_CTRL_ECAP0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.99 CONTROLSS_CTRL_ECAP1_CLK_GATE Register

2.6.2.99.1 CONTROLSS_CTRL_ECAP1_CLK_GATE Register (Offset = 204h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1659. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0204h

Figure 2-827. CONTROLSS_CTRL_ECAP1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1660. CONTROLSS_CTRL_ECAP1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.100 CONTROLSS_CTRL_ECAP2_CLK_GATE Register

2.6.2.100.1 CONTROLSS_CTRL_ECAP2_CLK_GATE Register (Offset = 208h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1661. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0208h

Figure 2-828. CONTROLSS_CTRL_ECAP2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP2_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1662. CONTROLSS_CTRL_ECAP2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP2_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.101 CONTROLSS_CTRL_ECAP3_CLK_GATE Register

2.6.2.101.1 CONTROLSS_CTRL_ECAP3_CLK_GATE Register (Offset = 20Ch) [reset = 0h]

Ecap[x] clock gate.

Return to Summary Table

Table 2-1663. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 020Ch

Figure 2-829. CONTROLSS_CTRL_ECAP3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP3_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1664. CONTROLSS_CTRL_ECAP3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP3_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.102 CONTROLSS_CTRL_ECAP4_CLK_GATE Register

2.6.2.102.1 CONTROLSS_CTRL_ECAP4_CLK_GATE Register (Offset = 210h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1665. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0210h

Figure 2-830. CONTROLSS_CTRL_ECAP4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP4_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1666. CONTROLSS_CTRL_ECAP4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP4_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.103 CONTROLSS_CTRL_ECAP5_CLK_GATE Register

2.6.2.103.1 CONTROLSS_CTRL_ECAP5_CLK_GATE Register (Offset = 214h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1667. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0214h

Figure 2-831. CONTROLSS_CTRL_ECAP5_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP5_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1668. CONTROLSS_CTRL_ECAP5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP5_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.104 CONTROLSS_CTRL_ECAP6_CLK_GATE Register

2.6.2.104.1 CONTROLSS_CTRL_ECAP6_CLK_GATE Register (Offset = 218h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1669. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0218h

Figure 2-832. CONTROLSS_CTRL_ECAP6_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP6_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1670. CONTROLSS_CTRL_ECAP6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP6_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.105 CONTROLSS_CTRL_ECAP7_CLK_GATE Register

2.6.2.105.1 CONTROLSS_CTRL_ECAP7_CLK_GATE Register (Offset = 21Ch) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1671. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 021Ch

Figure 2-833. CONTROLSS_CTRL_ECAP7_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP7_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1672. CONTROLSS_CTRL_ECAP7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP7_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.106 CONTROLSS_CTRL_ECAP8_CLK_GATE Register

2.6.2.106.1 CONTROLSS_CTRL_ECAP8_CLK_GATE Register (Offset = 220h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1673. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0220h

Figure 2-834. CONTROLSS_CTRL_ECAP8_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP8_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1674. CONTROLSS_CTRL_ECAP8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP8_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.107 CONTROLSS_CTRL_ECAP9_CLK_GATE Register

2.6.2.107.1 CONTROLSS_CTRL_ECAP9_CLK_GATE Register (Offset = 224h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1675. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0224h

Figure 2-835. CONTROLSS_CTRL_ECAP9_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP9_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1676. CONTROLSS_CTRL_ECAP9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP9_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.108 CONTROLSS_CTRL_ECAP10_CLK_GATE Register

2.6.2.108.1 CONTROLSS_CTRL_ECAP10_CLK_GATE Register (Offset = 228h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1677. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0228h

Figure 2-836. CONTROLSS_CTRL_ECAP10_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP10_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1678. CONTROLSS_CTRL_ECAP10_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP10_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.109 CONTROLSS_CTRL_ECAP11_CLK_GATE Register

2.6.2.109.1 CONTROLSS_CTRL_ECAP11_CLK_GATE Register (Offset = 22Ch) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1679. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 022Ch

Figure 2-837. CONTROLSS_CTRL_ECAP11_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP11_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1680. CONTROLSS_CTRL_ECAP11_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP11_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.110 CONTROLSS_CTRL_ECAP12_CLK_GATE Register

2.6.2.110.1 CONTROLSS_CTRL_ECAP12_CLK_GATE Register (Offset = 230h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1681. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0230h

Figure 2-838. CONTROLSS_CTRL_ECAP12_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP12_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1682. CONTROLSS_CTRL_ECAP12_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP12_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.111 CONTROLSS_CTRL_ECAP13_CLK_GATE Register

2.6.2.111.1 CONTROLSS_CTRL_ECAP13_CLK_GATE Register (Offset = 234h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1683. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0234h

Figure 2-839. CONTROLSS_CTRL_ECAP13_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP13_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1684. CONTROLSS_CTRL_ECAP13_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP13_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.112 CONTROLSS_CTRL_ECAP14_CLK_GATE Register

2.6.2.112.1 CONTROLSS_CTRL_ECAP14_CLK_GATE Register (Offset = 238h) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1685. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0238h

Figure 2-840. CONTROLSS_CTRL_ECAP14_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP14_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1686. CONTROLSS_CTRL_ECAP14_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP14_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.113 CONTROLSS_CTRL_ECAP15_CLK_GATE Register

2.6.2.113.1 CONTROLSS_CTRL_ECAP15_CLK_GATE Register (Offset = 23Ch) [reset = 0h]

Ecap[x] clock gate.

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Table 2-1687. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 023Ch

Figure 2-841. CONTROLSS_CTRL_ECAP15_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ECAP15_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1688. CONTROLSS_CTRL_ECAP15_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP15_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding ecap

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2.6.2.114 CONTROLSS_CTRL_EQEP0_CLK_GATE Register

2.6.2.114.1 CONTROLSS_CTRL_EQEP0_CLK_GATE Register (Offset = 240h) [reset = 0h]

Eqep[x] clock gate.

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Table 2-1689. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0240h

Figure 2-842. CONTROLSS_CTRL_EQEP0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EQEP0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1690. CONTROLSS_CTRL_EQEP0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EQEP0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding eqep

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2.6.2.115 CONTROLSS_CTRL_EQEP1_CLK_GATE Register

2.6.2.115.1 CONTROLSS_CTRL_EQEP1_CLK_GATE Register (Offset = 244h) [reset = 0h]

Eqep[x] clock gate.

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Table 2-1691. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0244h

Figure 2-843. CONTROLSS_CTRL_EQEP1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EQEP1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1692. CONTROLSS_CTRL_EQEP1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EQEP1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding eqep

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2.6.2.116 CONTROLSS_CTRL_EQEP2_CLK_GATE Register

2.6.2.116.1 CONTROLSS_CTRL_EQEP2_CLK_GATE Register (Offset = 248h) [reset = 0h]

Eqep[x] clock gate.

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Table 2-1693. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0248h

Figure 2-844. CONTROLSS_CTRL_EQEP2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EQEP2_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1694. CONTROLSS_CTRL_EQEP2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EQEP2_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding eqep

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2.6.2.117 CONTROLSS_CTRL_SDFM0_CLK_GATE Register

2.6.2.117.1 CONTROLSS_CTRL_SDFM0_CLK_GATE Register (Offset = 250h) [reset = 0h]

Sdfm[x] clock gate.

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Table 2-1695. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0250h

Figure 2-845. CONTROLSS_CTRL_SDFM0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					SDFM0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1696. CONTROLSS_CTRL_SDFM0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	SDFM0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding sdfm

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2.6.2.118 CONTROLSS_CTRL_SDFM1_CLK_GATE Register

2.6.2.118.1 CONTROLSS_CTRL_SDFM1_CLK_GATE Register (Offset = 254h) [reset = 0h]

Sdfm[x] clock gate.

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Table 2-1697. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0254h

Figure 2-846. CONTROLSS_CTRL_SDFM1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					SDFM1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1698. CONTROLSS_CTRL_SDFM1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	SDFM1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding sdfm

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2.6.2.119 CONTROLSS_CTRL_DAC_CLK_GATE Register

2.6.2.119.1 CONTROLSS_CTRL_DAC_CLK_GATE Register (Offset = 258h) [reset = 0h]

dac clock gate.

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Table 2-1699. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0258h

Figure 2-847. CONTROLSS_CTRL_DAC_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DAC_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1700. CONTROLSS_CTRL_DAC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DAC_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for dac

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2.6.2.120 CONTROLSS_CTRL_ADC0_CLK_GATE Register

2.6.2.120.1 CONTROLSS_CTRL_ADC0_CLK_GATE Register (Offset = 25Ch) [reset = 0h]

Adc[x] clock gate.

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Table 2-1701. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 025Ch

Figure 2-848. CONTROLSS_CTRL_ADC0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1702. CONTROLSS_CTRL_ADC0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc

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2.6.2.121 CONTROLSS_CTRL_ADC1_CLK_GATE Register

2.6.2.121.1 CONTROLSS_CTRL_ADC1_CLK_GATE Register (Offset = 260h) [reset = 0h]

Adc[x] clock gate.

Return to Summary Table

Table 2-1703. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0260h

Figure 2-849. CONTROLSS_CTRL_ADC1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1704. CONTROLSS_CTRL_ADC1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc

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2.6.2.122 CONTROLSS_CTRL_ADC2_CLK_GATE Register

2.6.2.122.1 CONTROLSS_CTRL_ADC2_CLK_GATE Register (Offset = 264h) [reset = 0h]

Adc[x] clock gate.

Return to Summary Table

Table 2-1705. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0264h

Figure 2-850. CONTROLSS_CTRL_ADC2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC2_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1706. CONTROLSS_CTRL_ADC2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC2_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc

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2.6.2.123 CONTROLSS_CTRL_ADC3_CLK_GATE Register

2.6.2.123.1 CONTROLSS_CTRL_ADC3_CLK_GATE Register (Offset = 268h) [reset = 0h]

Adc[x] clock gate.

Return to Summary Table

Table 2-1707. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0268h

Figure 2-851. CONTROLSS_CTRL_ADC3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC3_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1708. CONTROLSS_CTRL_ADC3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC3_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc

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2.6.2.124 CONTROLSS_CTRL_ADC4_CLK_GATE Register

2.6.2.124.1 CONTROLSS_CTRL_ADC4_CLK_GATE Register (Offset = 26Ch) [reset = 0h]

Adc[x] clock gate.

Return to Summary Table

Table 2-1709. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 026Ch

Figure 2-852. CONTROLSS_CTRL_ADC4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC4_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1710. CONTROLSS_CTRL_ADC4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC4_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc

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2.6.2.125 CONTROLSS_CTRL_OTTO0_CLK_GATE Register

2.6.2.125.1 CONTROLSS_CTRL_OTTO0_CLK_GATE Register (Offset = 270h) [reset = 0h]

Otto[x] clock gate.

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Table 2-1711. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0270h

Figure 2-853. CONTROLSS_CTRL_OTTO0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OTTO0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1712. CONTROLSS_CTRL_OTTO0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OTTO0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding otto

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2.6.2.126 CONTROLSS_CTRL_OTTO1_CLK_GATE Register

2.6.2.126.1 CONTROLSS_CTRL_OTTO1_CLK_GATE Register (Offset = 274h) [reset = 0h]

Otto[x] clock gate.

Return to Summary Table

Table 2-1713. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0274h

Figure 2-854. CONTROLSS_CTRL_OTTO1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OTTO1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1714. CONTROLSS_CTRL_OTTO1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OTTO1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding otto

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2.6.2.127 CONTROLSS_CTRL_OTTO2_CLK_GATE Register

2.6.2.127.1 CONTROLSS_CTRL_OTTO2_CLK_GATE Register (Offset = 278h) [reset = 0h]

Otto[x] clock gate.

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Table 2-1715. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0278h

Figure 2-855. CONTROLSS_CTRL_OTTO2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OTTO2_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1716. CONTROLSS_CTRL_OTTO2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OTTO2_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding otto

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2.6.2.128 CONTROLSS_CTRL_OTTO3_CLK_GATE Register

2.6.2.128.1 CONTROLSS_CTRL_OTTO3_CLK_GATE Register (Offset = 27Ch) [reset = 0h]

Otto[x] clock gate.

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Table 2-1717. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 027Ch

Figure 2-856. CONTROLSS_CTRL_OTTO3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					OTTO3_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1718. CONTROLSS_CTRL_OTTO3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OTTO3_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding otto

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2.6.2.129 CONTROLSS_CTRL_SDFM0_PLL_CLK_GATE Register

2.6.2.129.1 CONTROLSS_CTRL_SDFM0_PLL_CLK_GATE Register (Offset = 280h) [reset = 0h]

Sdfm[x]_pll clock gate.

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Table 2-1719. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0280h

Figure 2-857. CONTROLSS_CTRL_SDFM0_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					SDFM0_PLL_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1720. CONTROLSS_CTRL_SDFM0_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	SDFM0_PLL_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding sdfm pll clock

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2.6.2.130 CONTROLSS_CTRL_SDFM1_PLL_CLK_GATE Register

2.6.2.130.1 CONTROLSS_CTRL_SDFM1_PLL_CLK_GATE Register (Offset = 284h) [reset = 0h]

Sdfm[x]_pll clock gate.

Return to Summary Table

Table 2-1721. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0284h

Figure 2-858. CONTROLSS_CTRL_SDFM1_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					SDFM1_PLL_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1722. CONTROLSS_CTRL_SDFM1_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	SDFM1_PLL_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding sdfm pll clock

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2.6.2.131 CONTROLSS_CTRL_FSI_TX0_PLL_CLK_GATE Register

2.6.2.131.1 CONTROLSS_CTRL_FSI_TX0_PLL_CLK_GATE Register (Offset = 288h) [reset = 0h]

fsi_tx[x]_pll clock gate.

Return to Summary Table

Table 2-1723. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0288h

Figure 2-859. CONTROLSS_CTRL_FSI_TX0_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					FSI_TX0_PLL_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1724. CONTROLSS_CTRL_FSI_TX0_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX0_PLL_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi rx pll clock

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2.6.2.132 CONTROLSS_CTRL_FSI_TX1_PLL_CLK_GATE Register

2.6.2.132.1 CONTROLSS_CTRL_FSI_TX1_PLL_CLK_GATE Register (Offset = 28Ch) [reset = 0h]

fsi_tx[x]_pll clock gate.

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Table 2-1725. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 028Ch

Figure 2-860. CONTROLSS_CTRL_FSI_TX1_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_TX1_PLL_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1726. CONTROLSS_CTRL_FSI_TX1_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX1_PLL_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi rx pll clock

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2.6.2.133 CONTROLSS_CTRL_FSI_TX2_PLL_CLK_GATE Register

2.6.2.133.1 CONTROLSS_CTRL_FSI_TX2_PLL_CLK_GATE Register (Offset = 290h) [reset = 0h]

fsi_tx[x]_pll clock gate.

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Table 2-1727. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0290h

Figure 2-861. CONTROLSS_CTRL_FSI_TX2_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_TX2_PLL_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1728. CONTROLSS_CTRL_FSI_TX2_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX2_PLL_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi rx pll clock

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2.6.2.134 CONTROLSS_CTRL_FSI_TX3_PLL_CLK_GATE Register

2.6.2.134.1 CONTROLSS_CTRL_FSI_TX3_PLL_CLK_GATE Register (Offset = 294h) [reset = 0h]

fsi_tx[x]_pll clock gate.

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Table 2-1729. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0294h

Figure 2-862. CONTROLSS_CTRL_FSI_TX3_PLL_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_TX3_PLL_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1730. CONTROLSS_CTRL_FSI_TX3_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX3_PLL_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding fsi rx pll clock

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2.6.2.135 CONTROLSS_CTRL_HW_RESOLVER_CLK_GATE Register

2.6.2.135.1 CONTROLSS_CTRL_HW_RESOLVER_CLK_GATE Register (Offset = 298h) [reset = 0h]

Hardware resolver clock gate.

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Table 2-1731. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0298h

Figure 2-863. CONTROLSS_CTRL_HW_RESOLVER_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					HW_RESOLVER_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1732. CONTROLSS_CTRL_HW_RESOLVER_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	HW_RESOLVER_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding hw_resolver

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2.6.2.136 CONTROLSS_CTRL_ADC_SCTILE0_CLK_GATE Register

2.6.2.136.1 CONTROLSS_CTRL_ADC_SCTILE0_CLK_GATE Register (Offset = 29Ch) [reset = 0h]

ADC Safecheck tiles clock gate.

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Table 2-1733. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 029Ch

Figure 2-864. CONTROLSS_CTRL_ADC_SCTILE0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ADC_SCTILE0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1734. CONTROLSS_CTRL_ADC_SCTILE0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.137 CONTROLSS_CTRL_ADC_SCTILE1_CLK_GATE Register

2.6.2.137.1 CONTROLSS_CTRL_ADC_SCTILE1_CLK_GATE Register (Offset = 2A0h) [reset = 0h]

ADC Safecheck tiles clock gate.

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Table 2-1735. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02A0h

Figure 2-865. CONTROLSS_CTRL_ADC_SCTILE1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ADC_SCTILE1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1736. CONTROLSS_CTRL_ADC_SCTILE1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.138 CONTROLSS_CTRL_ADC_SCTILE2_CLK_GATE Register

2.6.2.138.1 CONTROLSS_CTRL_ADC_SCTILE2_CLK_GATE Register (Offset = 2A4h) [reset = 0h]

ADC Safecheck tiles clock gate.

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Table 2-1737. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02A4h

Figure 2-866. CONTROLSS_CTRL_ADC_SCTILE2_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE2_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1738. CONTROLSS_CTRL_ADC_SCTILE2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE2_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.139 CONTROLSS_CTRL_ADC_SCTILE3_CLK_GATE Register

2.6.2.139.1 CONTROLSS_CTRL_ADC_SCTILE3_CLK_GATE Register (Offset = 2A8h) [reset = 0h]

ADC Safecheck tiles clock gate.

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Table 2-1739. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02A8h

Figure 2-867. CONTROLSS_CTRL_ADC_SCTILE3_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE3_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1740. CONTROLSS_CTRL_ADC_SCTILE3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE3_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.140 CONTROLSS_CTRL_ADC_SCTILE4_CLK_GATE Register

2.6.2.140.1 CONTROLSS_CTRL_ADC_SCTILE4_CLK_GATE Register (Offset = 2ACh) [reset = 0h]

ADC Safecheck tiles clock gate.

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Table 2-1741. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02ACh

Figure 2-868. CONTROLSS_CTRL_ADC_SCTILE4_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE4_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1742. CONTROLSS_CTRL_ADC_SCTILE4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE4_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.141 CONTROLSS_CTRL_ADC_SCTILE5_CLK_GATE Register

2.6.2.141.1 CONTROLSS_CTRL_ADC_SCTILE5_CLK_GATE Register (Offset = 2B0h) [reset = 0h]

ADC Safecheck tiles clock gate.

Return to Summary Table

Table 2-1743. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02B0h

Figure 2-869. CONTROLSS_CTRL_ADC_SCTILE5_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE5_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1744. CONTROLSS_CTRL_ADC_SCTILE5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE5_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.142 CONTROLSS_CTRL_ADC_SCTILE6_CLK_GATE Register

2.6.2.142.1 CONTROLSS_CTRL_ADC_SCTILE6_CLK_GATE Register (Offset = 2B4h) [reset = 0h]

ADC Safecheck tiles clock gate.

Return to Summary Table

Table 2-1745. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02B4h

Figure 2-870. CONTROLSS_CTRL_ADC_SCTILE6_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE6_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1746. CONTROLSS_CTRL_ADC_SCTILE6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE6_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.143 CONTROLSS_CTRL_ADC_SCTILE7_CLK_GATE Register

2.6.2.143.1 CONTROLSS_CTRL_ADC_SCTILE7_CLK_GATE Register (Offset = 2B8h) [reset = 0h]

ADC Safecheck tiles clock gate.

Return to Summary Table

Table 2-1747. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02B8h

Figure 2-871. CONTROLSS_CTRL_ADC_SCTILE7_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE7_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1748. CONTROLSS_CTRL_ADC_SCTILE7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE7_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.144 CONTROLSS_CTRL_ADC_SCTILE8_CLK_GATE Register

2.6.2.144.1 CONTROLSS_CTRL_ADC_SCTILE8_CLK_GATE Register (Offset = 2BCh) [reset = 0h]

ADC Safecheck tiles clock gate.

Return to Summary Table

Table 2-1749. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02BCh

Figure 2-872. CONTROLSS_CTRL_ADC_SCTILE8_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE8_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1750. CONTROLSS_CTRL_ADC_SCTILE8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE8_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.145 CONTROLSS_CTRL_ADC_SCTILE9_CLK_GATE Register

2.6.2.145.1 CONTROLSS_CTRL_ADC_SCTILE9_CLK_GATE Register (Offset = 2C0h) [reset = 0h]

ADC Safecheck tiles clock gate.

Return to Summary Table

Table 2-1751. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02C0h

Figure 2-873. CONTROLSS_CTRL_ADC_SCTILE9_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE9_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1752. CONTROLSS_CTRL_ADC_SCTILE9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE9_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.146 CONTROLSS_CTRL_ADC_SCTILE10_CLK_GATE Register

2.6.2.146.1 CONTROLSS_CTRL_ADC_SCTILE10_CLK_GATE Register (Offset = 2C4h) [reset = 0h]

ADC Safecheck tiles clock gate.

Return to Summary Table

Table 2-1753. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02C4h

Figure 2-874. CONTROLSS_CTRL_ADC_SCTILE10_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE10_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1754. CONTROLSS_CTRL_ADC_SCTILE10_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE10_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.147 CONTROLSS_CTRL_ADC_SCTILE11_CLK_GATE Register

2.6.2.147.1 CONTROLSS_CTRL_ADC_SCTILE11_CLK_GATE Register (Offset = 2C8h) [reset = 0h]

ADC Safecheck tiles clock gate.

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Table 2-1755. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02C8h

Figure 2-875. CONTROLSS_CTRL_ADC_SCTILE11_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE11_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1756. CONTROLSS_CTRL_ADC_SCTILE11_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE11_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc safety tiles

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2.6.2.148 CONTROLSS_CTRL_ADC_AGG0_CLK_GATE Register

2.6.2.148.1 CONTROLSS_CTRL_ADC_AGG0_CLK_GATE Register (Offset = 2DCh) [reset = 0h]

ADC Aggregator clock gate.

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Table 2-1757. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02DCh

Figure 2-876. CONTROLSS_CTRL_ADC_AGG0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_AGG0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1758. CONTROLSS_CTRL_ADC_AGG0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_AGG0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc aggregator

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2.6.2.149 CONTROLSS_CTRL_CONTROLSS_XBAR_CLK_GATE Register

2.6.2.149.1 CONTROLSS_CTRL_CONTROLSS_XBAR_CLK_GATE Register (Offset = 2E0h) [reset = 0h]

clock gate for eight XBARs.

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Table 2-1759. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02E0h

Figure 2-877. CONTROLSS_CTRL_CONTROLSS_XBAR_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED	CONTROLSS_XBAR_CLK_GATE_PWMSYNCOUTXBAR			RESERVED	CONTROLSS_XBAR_CLK_GATE_OUTPUTXBAR		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	CONTROLSS_XBAR_CLK_GATE_DMAXBAR			RESERVED	CONTROLSS_XBAR_CLK_GATE_INTXBAR		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	CONTROLSS_XBAR_CLK_GATE_ICLXBAR			RESERVED	CONTROLSS_XBAR_CLK_GATE_MDLXBAR		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	CONTROLSS_XBAR_CLK_GATE_PWMXBAR			RESERVED	CONTROLSS_XBAR_CLK_GATE_INPUTXBAR		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 2-1760. CONTROLSS_CTRL_CONTROLSS_XBAR_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	CONTROLSS_XBAR_CLK_GATE_PWMSYNCOUTXBAR	R/W	0h	Writing 3'b111 to register will clock gate the corresponding XBAR
27	RESERVED	NONE	0h	Reserved
26:24	CONTROLSS_XBAR_CLK_GATE_OUTPUTXBAR	R/W	0h	Writing 3'b111 to register will clock gate the corresponding XBAR
23	RESERVED	NONE	0h	Reserved
22:20	CONTROLSS_XBAR_CLK_GATE_DMAXBAR	R/W	0h	Writing 3'b111 to register will clock gate the corresponding XBAR
19	RESERVED	NONE	0h	Reserved
18:16	CONTROLSS_XBAR_CLK_GATE_INTXBAR	R/W	0h	Writing 3'b111 to register will clock gate the corresponding XBAR
15	RESERVED	NONE	0h	Reserved
14:12	CONTROLSS_XBAR_CLK_GATE_ICLXBAR	R/W	0h	Writing 3'b111 to register will clock gate the corresponding XBAR
11	RESERVED	NONE	0h	Reserved
10:8	CONTROLSS_XBAR_CLK_GATE_MDLXBAR	R/W	0h	Writing 3'b111 to register will clock gate the corresponding XBAR
7	RESERVED	NONE	0h	Reserved

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Table 2-1760. CONTROLSS_CTRL_CONTROLSS_XBAR_CLK_GATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	CONTROLSS_XBAR_CLK_GATE_PWMXBAR	R/W	0h	Writing 3'b111 to register will clock gate the corresponding XBAR
3	RESERVED	NONE	0h	Reserved
2:0	CONTROLSS_XBAR_CLK_GATE_INPUTXBAR	R/W	0h	Writing 3'b111 to register will clock gate the corresponding XBAR

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2.6.2.150 CONTROLSS_CTRL_ADCR0_CLK_GATE Register

2.6.2.150.1 CONTROLSS_CTRL_ADCR0_CLK_GATE Register (Offset = 2E4h) [reset = 0h]

Adcr[x] clock gate.

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Table 2-1761. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02E4h

Figure 2-878. CONTROLSS_CTRL_ADCR0_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ADCR0_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1762. CONTROLSS_CTRL_ADCR0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADCR0_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc

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2.6.2.151 CONTROLSS_CTRL_ADCR1_CLK_GATE Register

2.6.2.151.1 CONTROLSS_CTRL_ADCR1_CLK_GATE Register (Offset = 2E8h) [reset = 0h]

Adcr[x] clock gate.

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Table 2-1763. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 02E8h

Figure 2-879. CONTROLSS_CTRL_ADCR1_CLK_GATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADCR1_CLK_GATE_CLK_GATE		
NONE					R/W		
0h					0h		

Table 2-1764. CONTROLSS_CTRL_ADCR1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADCR1_CLK_GATE_CLK_GATE	R/W	0h	Writing 3'b111 will gate clock for corresponding adc

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2.6.2.152 CONTROLSS_CTRL_EPWM0_RST Register

2.6.2.152.1 CONTROLSS_CTRL_EPWM0_RST Register (Offset = 300h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1765. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0300h

Figure 2-880. CONTROLSS_CTRL_EPWM0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1766. CONTROLSS_CTRL_EPWM0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.153 CONTROLSS_CTRL_EPWM1_RST Register

2.6.2.153.1 CONTROLSS_CTRL_EPWM1_RST Register (Offset = 304h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1767. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0304h

Figure 2-881. CONTROLSS_CTRL_EPWM1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1768. CONTROLSS_CTRL_EPWM1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.154 CONTROLSS_CTRL_EPWM2_RST Register

2.6.2.154.1 CONTROLSS_CTRL_EPWM2_RST Register (Offset = 308h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1769. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0308h

Figure 2-882. CONTROLSS_CTRL_EPWM2_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EPWM2_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1770. CONTROLSS_CTRL_EPWM2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM2_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.155 CONTROLSS_CTRL_EPWM3_RST Register

2.6.2.155.1 CONTROLSS_CTRL_EPWM3_RST Register (Offset = 30Ch) [reset = 0h]

Epwm[x]_reset.

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Table 2-1771. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 030Ch

Figure 2-883. CONTROLSS_CTRL_EPWM3_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EPWM3_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1772. CONTROLSS_CTRL_EPWM3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM3_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.156 CONTROLSS_CTRL_EPWM4_RST Register

2.6.2.156.1 CONTROLSS_CTRL_EPWM4_RST Register (Offset = 310h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1773. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0310h

Figure 2-884. CONTROLSS_CTRL_EPWM4_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM4_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1774. CONTROLSS_CTRL_EPWM4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM4_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.157 CONTROLSS_CTRL_EPWM5_RST Register

2.6.2.157.1 CONTROLSS_CTRL_EPWM5_RST Register (Offset = 314h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1775. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0314h

Figure 2-885. CONTROLSS_CTRL_EPWM5_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM5_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1776. CONTROLSS_CTRL_EPWM5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM5_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.158 CONTROLSS_CTRL_EPWM6_RST Register

2.6.2.158.1 CONTROLSS_CTRL_EPWM6_RST Register (Offset = 318h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1777. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0318h

Figure 2-886. CONTROLSS_CTRL_EPWM6_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EPWM6_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1778. CONTROLSS_CTRL_EPWM6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM6_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.159 CONTROLSS_CTRL_EPWM7_RST Register

2.6.2.159.1 CONTROLSS_CTRL_EPWM7_RST Register (Offset = 31Ch) [reset = 0h]

Epwm[x]_reset.

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Table 2-1779. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 031Ch

Figure 2-887. CONTROLSS_CTRL_EPWM7_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM7_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1780. CONTROLSS_CTRL_EPWM7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM7_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.160 CONTROLSS_CTRL_EPWM8_RST Register

2.6.2.160.1 CONTROLSS_CTRL_EPWM8_RST Register (Offset = 320h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1781. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0320h

Figure 2-888. CONTROLSS_CTRL_EPWM8_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM8_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1782. CONTROLSS_CTRL_EPWM8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM8_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.161 CONTROLSS_CTRL_EPWM9_RST Register

2.6.2.161.1 CONTROLSS_CTRL_EPWM9_RST Register (Offset = 324h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1783. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0324h

Figure 2-889. CONTROLSS_CTRL_EPWM9_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EPWM9_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1784. CONTROLSS_CTRL_EPWM9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM9_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.162 CONTROLSS_CTRL_EPWM10_RST Register

2.6.2.162.1 CONTROLSS_CTRL_EPWM10_RST Register (Offset = 328h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1785. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0328h

Figure 2-890. CONTROLSS_CTRL_EPWM10_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM10_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1786. CONTROLSS_CTRL_EPWM10_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM10_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.163 CONTROLSS_CTRL_EPWM11_RST Register

2.6.2.163.1 CONTROLSS_CTRL_EPWM11_RST Register (Offset = 32Ch) [reset = 0h]

Epwm[x]_reset.

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Table 2-1787. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 032Ch

Figure 2-891. CONTROLSS_CTRL_EPWM11_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM11_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1788. CONTROLSS_CTRL_EPWM11_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM11_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.164 CONTROLSS_CTRL_EPWM12_RST Register

2.6.2.164.1 CONTROLSS_CTRL_EPWM12_RST Register (Offset = 330h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1789. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0330h

Figure 2-892. CONTROLSS_CTRL_EPWM12_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM12_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1790. CONTROLSS_CTRL_EPWM12_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM12_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.165 CONTROLSS_CTRL_EPWM13_RST Register

2.6.2.165.1 CONTROLSS_CTRL_EPWM13_RST Register (Offset = 334h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1791. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0334h

Figure 2-893. CONTROLSS_CTRL_EPWM13_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM13_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1792. CONTROLSS_CTRL_EPWM13_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM13_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.166 CONTROLSS_CTRL_EPWM14_RST Register

2.6.2.166.1 CONTROLSS_CTRL_EPWM14_RST Register (Offset = 338h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1793. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0338h

Figure 2-894. CONTROLSS_CTRL_EPWM14_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM14_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1794. CONTROLSS_CTRL_EPWM14_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM14_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.167 CONTROLSS_CTRL_EPWM15_RST Register

2.6.2.167.1 CONTROLSS_CTRL_EPWM15_RST Register (Offset = 33Ch) [reset = 0h]

Epwm[x]_reset.

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Table 2-1795. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 033Ch

Figure 2-895. CONTROLSS_CTRL_EPWM15_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM15_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1796. CONTROLSS_CTRL_EPWM15_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM15_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.168 CONTROLSS_CTRL_EPWM16_RST Register

2.6.2.168.1 CONTROLSS_CTRL_EPWM16_RST Register (Offset = 340h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1797. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0340h

Figure 2-896. CONTROLSS_CTRL_EPWM16_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM16_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1798. CONTROLSS_CTRL_EPWM16_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM16_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.169 CONTROLSS_CTRL_EPWM17_RST Register

2.6.2.169.1 CONTROLSS_CTRL_EPWM17_RST Register (Offset = 344h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1799. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0344h

Figure 2-897. CONTROLSS_CTRL_EPWM17_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM17_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1800. CONTROLSS_CTRL_EPWM17_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM17_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.170 CONTROLSS_CTRL_EPWM18_RST Register

2.6.2.170.1 CONTROLSS_CTRL_EPWM18_RST Register (Offset = 348h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1801. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0348h

Figure 2-898. CONTROLSS_CTRL_EPWM18_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM18_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1802. CONTROLSS_CTRL_EPWM18_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM18_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.171 CONTROLSS_CTRL_EPWM19_RST Register

2.6.2.171.1 CONTROLSS_CTRL_EPWM19_RST Register (Offset = 34Ch) [reset = 0h]

Epwm[x]_reset.

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Table 2-1803. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 034Ch

Figure 2-899. CONTROLSS_CTRL_EPWM19_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM19_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1804. CONTROLSS_CTRL_EPWM19_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM19_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.172 CONTROLSS_CTRL_EPWM20_RST Register

2.6.2.172.1 CONTROLSS_CTRL_EPWM20_RST Register (Offset = 350h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1805. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0350h

Figure 2-900. CONTROLSS_CTRL_EPWM20_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM20_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1806. CONTROLSS_CTRL_EPWM20_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM20_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.173 CONTROLSS_CTRL_EPWM21_RST Register

2.6.2.173.1 CONTROLSS_CTRL_EPWM21_RST Register (Offset = 354h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1807. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0354h

Figure 2-901. CONTROLSS_CTRL_EPWM21_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM21_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1808. CONTROLSS_CTRL_EPWM21_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM21_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.174 CONTROLSS_CTRL_EPWM22_RST Register

2.6.2.174.1 CONTROLSS_CTRL_EPWM22_RST Register (Offset = 358h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1809. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0358h

Figure 2-902. CONTROLSS_CTRL_EPWM22_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM22_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1810. CONTROLSS_CTRL_EPWM22_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM22_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.175 CONTROLSS_CTRL_EPWM23_RST Register

2.6.2.175.1 CONTROLSS_CTRL_EPWM23_RST Register (Offset = 35Ch) [reset = 0h]

Epwm[x]_reset.

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Table 2-1811. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 035Ch

Figure 2-903. CONTROLSS_CTRL_EPWM23_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EPWM23_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1812. CONTROLSS_CTRL_EPWM23_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM23_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.176 CONTROLSS_CTRL_EPWM24_RST Register

2.6.2.176.1 CONTROLSS_CTRL_EPWM24_RST Register (Offset = 360h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1813. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0360h

Figure 2-904. CONTROLSS_CTRL_EPWM24_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EPWM24_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1814. CONTROLSS_CTRL_EPWM24_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM24_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.177 CONTROLSS_CTRL_EPWM25_RST Register

2.6.2.177.1 CONTROLSS_CTRL_EPWM25_RST Register (Offset = 364h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1815. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0364h

Figure 2-905. CONTROLSS_CTRL_EPWM25_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EPWM25_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1816. CONTROLSS_CTRL_EPWM25_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM25_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.178 CONTROLSS_CTRL_EPWM26_RST Register

2.6.2.178.1 CONTROLSS_CTRL_EPWM26_RST Register (Offset = 368h) [reset = 0h]

Epwm[x]_reset.

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Table 2-1817. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0368h

Figure 2-906. CONTROLSS_CTRL_EPWM26_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM26_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1818. CONTROLSS_CTRL_EPWM26_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM26_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.179 CONTROLSS_CTRL_EPWM27_RST Register

2.6.2.179.1 CONTROLSS_CTRL_EPWM27_RST Register (Offset = 36Ch) [reset = 0h]

Epwm[x]_reset.

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Table 2-1819. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 036Ch

Figure 2-907. CONTROLSS_CTRL_EPWM27_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM27_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1820. CONTROLSS_CTRL_EPWM27_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM27_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.180 CONTROLSS_CTRL_EPWM28_RST Register

2.6.2.180.1 CONTROLSS_CTRL_EPWM28_RST Register (Offset = 370h) [reset = 0h]

Epwm[x]_reset.

Return to Summary Table

Table 2-1821. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0370h

Figure 2-908. CONTROLSS_CTRL_EPWM28_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM28_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1822. CONTROLSS_CTRL_EPWM28_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM28_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.181 CONTROLSS_CTRL_EPWM29_RST Register

2.6.2.181.1 CONTROLSS_CTRL_EPWM29_RST Register (Offset = 374h) [reset = 0h]

Epwm[x]_reset.

Return to Summary Table

Table 2-1823. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0374h

Figure 2-909. CONTROLSS_CTRL_EPWM29_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM29_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1824. CONTROLSS_CTRL_EPWM29_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM29_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.182 CONTROLSS_CTRL_EPWM30_RST Register

2.6.2.182.1 CONTROLSS_CTRL_EPWM30_RST Register (Offset = 378h) [reset = 0h]

Epwm[x]_reset.

Return to Summary Table

Table 2-1825. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0378h

Figure 2-910. CONTROLSS_CTRL_EPWM30_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM30_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1826. CONTROLSS_CTRL_EPWM30_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM30_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.183 CONTROLSS_CTRL_EPWM31_RST Register

2.6.2.183.1 CONTROLSS_CTRL_EPWM31_RST Register (Offset = 37Ch) [reset = 0h]

Epwm[x]_reset.

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Table 2-1827. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 037Ch

Figure 2-911. CONTROLSS_CTRL_EPWM31_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					EPWM31_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1828. CONTROLSS_CTRL_EPWM31_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EPWM31_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding epwm

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2.6.2.184 CONTROLSS_CTRL_FSI_TX0_RST Register

2.6.2.184.1 CONTROLSS_CTRL_FSI_TX0_RST Register (Offset = 380h) [reset = 0h]

fsi_tx[x]_reset.

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Table 2-1829. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0380h

Figure 2-912. CONTROLSS_CTRL_FSI_TX0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_TX0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1830. CONTROLSS_CTRL_FSI_TX0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding fsi_tx

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2.6.2.185 CONTROLSS_CTRL_FSI_TX1_RST Register

2.6.2.185.1 CONTROLSS_CTRL_FSI_TX1_RST Register (Offset = 384h) [reset = 0h]

fsi_tx[x]_reset.

Return to Summary Table

Table 2-1831. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0384h

Figure 2-913. CONTROLSS_CTRL_FSI_TX1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_TX1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1832. CONTROLSS_CTRL_FSI_TX1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding fsi_tx

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2.6.2.186 CONTROLSS_CTRL_FSI_TX2_RST Register

2.6.2.186.1 CONTROLSS_CTRL_FSI_TX2_RST Register (Offset = 388h) [reset = 0h]

fsi_tx[x]_reset.

Return to Summary Table

Table 2-1833. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0388h

Figure 2-914. CONTROLSS_CTRL_FSI_TX2_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					FSI_TX2_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1834. CONTROLSS_CTRL_FSI_TX2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX2_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding fsi_tx

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2.6.2.187 CONTROLSS_CTRL_FSI_TX3_RST Register

2.6.2.187.1 CONTROLSS_CTRL_FSI_TX3_RST Register (Offset = 38Ch) [reset = 0h]

fsi_tx[x]_reset.

Return to Summary Table

Table 2-1835. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 038Ch

Figure 2-915. CONTROLSS_CTRL_FSI_TX3_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_TX3_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1836. CONTROLSS_CTRL_FSI_TX3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_TX3_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding fsi_tx

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2.6.2.188 CONTROLSS_CTRL_FSI_RX0_RST Register

2.6.2.188.1 CONTROLSS_CTRL_FSI_RX0_RST Register (Offset = 390h) [reset = 0h]

fsi_rx[x]_reset.

Return to Summary Table

Table 2-1837. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0390h

Figure 2-916. CONTROLSS_CTRL_FSI_RX0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_RX0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1838. CONTROLSS_CTRL_FSI_RX0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_RX0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding fsi_rx

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2.6.2.189 CONTROLSS_CTRL_FSI_RX1_RST Register

2.6.2.189.1 CONTROLSS_CTRL_FSI_RX1_RST Register (Offset = 394h) [reset = 0h]

fsi_rx[x]_reset.

Return to Summary Table

Table 2-1839. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0394h

Figure 2-917. CONTROLSS_CTRL_FSI_RX1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_RX1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1840. CONTROLSS_CTRL_FSI_RX1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_RX1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding fsi_rx

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2.6.2.190 CONTROLSS_CTRL_FSI_RX2_RST Register

2.6.2.190.1 CONTROLSS_CTRL_FSI_RX2_RST Register (Offset = 398h) [reset = 0h]

fsi_rx[x]_reset.

Return to Summary Table

Table 2-1841. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0398h

Figure 2-918. CONTROLSS_CTRL_FSI_RX2_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					FSI_RX2_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1842. CONTROLSS_CTRL_FSI_RX2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_RX2_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding fsi_rx

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2.6.2.191 CONTROLSS_CTRL_FSI_RX3_RST Register

2.6.2.191.1 CONTROLSS_CTRL_FSI_RX3_RST Register (Offset = 39Ch) [reset = 0h]

fsi_rx[x]_reset.

Return to Summary Table

Table 2-1843. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 039Ch

Figure 2-919. CONTROLSS_CTRL_FSI_RX3_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					FSI_RX3_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1844. CONTROLSS_CTRL_FSI_RX3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FSI_RX3_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding fsi_rx

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2.6.2.192 CONTROLSS_CTRL_CMPSSA0_RST Register

2.6.2.192.1 CONTROLSS_CTRL_CMPSSA0_RST Register (Offset = 3A0h) [reset = 0h]

cmpssa[x]_reset.

Return to Summary Table

Table 2-1845. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03A0h

Figure 2-920. CONTROLSS_CTRL_CMPSSA0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSA0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1846. CONTROLSS_CTRL_CMPSSA0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssa

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2.6.2.193 CONTROLSS_CTRL_CMPSSA1_RST Register

2.6.2.193.1 CONTROLSS_CTRL_CMPSSA1_RST Register (Offset = 3A4h) [reset = 0h]

cmpssa[x]_reset.

Return to Summary Table

Table 2-1847. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03A4h

Figure 2-921. CONTROLSS_CTRL_CMPSSA1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1848. CONTROLSS_CTRL_CMPSSA1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssa

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2.6.2.194 CONTROLSS_CTRL_CMPSSA2_RST Register

2.6.2.194.1 CONTROLSS_CTRL_CMPSSA2_RST Register (Offset = 3A8h) [reset = 0h]

cmpssa[x]_reset.

Return to Summary Table

Table 2-1849. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03A8h

Figure 2-922. CONTROLSS_CTRL_CMPSSA2_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSA2_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1850. CONTROLSS_CTRL_CMPSSA2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA2_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssa

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2.6.2.195 CONTROLSS_CTRL_CMPSSA3_RST Register

2.6.2.195.1 CONTROLSS_CTRL_CMPSSA3_RST Register (Offset = 3ACh) [reset = 0h]

cmpssa[x]_reset.

Return to Summary Table

Table 2-1851. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03ACh

Figure 2-923. CONTROLSS_CTRL_CMPSSA3_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSA3_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1852. CONTROLSS_CTRL_CMPSSA3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA3_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssa

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2.6.2.196 CONTROLSS_CTRL_CMPSSA4_RST Register

2.6.2.196.1 CONTROLSS_CTRL_CMPSSA4_RST Register (Offset = 3B0h) [reset = 0h]

cmpssa[x]_reset.

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Table 2-1853. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03B0h

Figure 2-924. CONTROLSS_CTRL_CMPSSA4_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA4_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1854. CONTROLSS_CTRL_CMPSSA4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA4_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssa

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2.6.2.197 CONTROLSS_CTRL_CMPSSA5_RST Register

2.6.2.197.1 CONTROLSS_CTRL_CMPSSA5_RST Register (Offset = 3B4h) [reset = 0h]

cmpssa[x]_reset.

Return to Summary Table

Table 2-1855. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03B4h

Figure 2-925. CONTROLSS_CTRL_CMPSSA5_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSA5_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1856. CONTROLSS_CTRL_CMPSSA5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA5_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssa

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2.6.2.198 CONTROLSS_CTRL_CMPSSA6_RST Register

2.6.2.198.1 CONTROLSS_CTRL_CMPSSA6_RST Register (Offset = 3B8h) [reset = 0h]

cmpssa[x]_reset.

Return to Summary Table

Table 2-1857. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03B8h

Figure 2-926. CONTROLSS_CTRL_CMPSSA6_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSA6_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1858. CONTROLSS_CTRL_CMPSSA6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA6_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssa

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2.6.2.199 CONTROLSS_CTRL_CMPSSA7_RST Register

2.6.2.199.1 CONTROLSS_CTRL_CMPSSA7_RST Register (Offset = 3BCh) [reset = 0h]

cmpssa[x]_reset.

Return to Summary Table

Table 2-1859. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03BCh

Figure 2-927. CONTROLSS_CTRL_CMPSSA7_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSA7_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1860. CONTROLSS_CTRL_CMPSSA7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA7_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssa

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2.6.2.200 CONTROLSS_CTRL_CMPSSA8_RST Register

2.6.2.200.1 CONTROLSS_CTRL_CMPSSA8_RST Register (Offset = 3C0h) [reset = 0h]

cmpssa[x]_reset.

Return to Summary Table

Table 2-1861. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03C0h

Figure 2-928. CONTROLSS_CTRL_CMPSSA8_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSA8_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1862. CONTROLSS_CTRL_CMPSSA8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA8_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssa

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2.6.2.201 CONTROLSS_CTRL_CMPSSA9_RST Register

2.6.2.201.1 CONTROLSS_CTRL_CMPSSA9_RST Register (Offset = 3C4h) [reset = 0h]

cmpssa[x]_reset.

Return to Summary Table

Table 2-1863. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03C4h

Figure 2-929. CONTROLSS_CTRL_CMPSSA9_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSA9_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1864. CONTROLSS_CTRL_CMPSSA9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSA9_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssa

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2.6.2.202 CONTROLSS_CTRL_CMPSSB0_RST Register

2.6.2.202.1 CONTROLSS_CTRL_CMPSSB0_RST Register (Offset = 3D0h) [reset = 0h]

cmpssb[x]_reset.

Return to Summary Table

Table 2-1865. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03D0h

Figure 2-930. CONTROLSS_CTRL_CMPSSB0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSB0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1866. CONTROLSS_CTRL_CMPSSB0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssb

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2.6.2.203 CONTROLSS_CTRL_CMPSSB1_RST Register

2.6.2.203.1 CONTROLSS_CTRL_CMPSSB1_RST Register (Offset = 3D4h) [reset = 0h]

cmpssb[x]_reset.

Return to Summary Table

Table 2-1867. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03D4h

Figure 2-931. CONTROLSS_CTRL_CMPSSB1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1868. CONTROLSS_CTRL_CMPSSB1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssb

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2.6.2.204 CONTROLSS_CTRL_CMPSSB2_RST Register

2.6.2.204.1 CONTROLSS_CTRL_CMPSSB2_RST Register (Offset = 3D8h) [reset = 0h]

cmpssb[x]_reset.

Return to Summary Table

Table 2-1869. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03D8h

Figure 2-932. CONTROLSS_CTRL_CMPSSB2_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB2_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1870. CONTROLSS_CTRL_CMPSSB2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB2_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssb

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2.6.2.205 CONTROLSS_CTRL_CMPSSB3_RST Register

2.6.2.205.1 CONTROLSS_CTRL_CMPSSB3_RST Register (Offset = 3DCh) [reset = 0h]

cmpssb[x]_reset.

Return to Summary Table

Table 2-1871. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03DCh

Figure 2-933. CONTROLSS_CTRL_CMPSSB3_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB3_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1872. CONTROLSS_CTRL_CMPSSB3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB3_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssb

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2.6.2.206 CONTROLSS_CTRL_CMPSSB4_RST Register

2.6.2.206.1 CONTROLSS_CTRL_CMPSSB4_RST Register (Offset = 3E0h) [reset = 0h]

cmpssb[x]_reset.

Return to Summary Table

Table 2-1873. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03E0h

Figure 2-934. CONTROLSS_CTRL_CMPSSB4_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB4_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1874. CONTROLSS_CTRL_CMPSSB4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB4_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssb

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2.6.2.207 CONTROLSS_CTRL_CMPSSB5_RST Register

2.6.2.207.1 CONTROLSS_CTRL_CMPSSB5_RST Register (Offset = 3E4h) [reset = 0h]

cmpssb[x]_reset.

Return to Summary Table

Table 2-1875. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03E4h

Figure 2-935. CONTROLSS_CTRL_CMPSSB5_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB5_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1876. CONTROLSS_CTRL_CMPSSB5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB5_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssb

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2.6.2.208 CONTROLSS_CTRL_CMPSSB6_RST Register

2.6.2.208.1 CONTROLSS_CTRL_CMPSSB6_RST Register (Offset = 3E8h) [reset = 0h]

cmpssb[x]_reset.

Return to Summary Table

Table 2-1877. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03E8h

Figure 2-936. CONTROLSS_CTRL_CMPSSB6_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB6_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1878. CONTROLSS_CTRL_CMPSSB6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB6_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssb

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2.6.2.209 CONTROLSS_CTRL_CMPSSB7_RST Register

2.6.2.209.1 CONTROLSS_CTRL_CMPSSB7_RST Register (Offset = 3ECh) [reset = 0h]

cmpssb[x]_reset.

Return to Summary Table

Table 2-1879. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03ECh

Figure 2-937. CONTROLSS_CTRL_CMPSSB7_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB7_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1880. CONTROLSS_CTRL_CMPSSB7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB7_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssb

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2.6.2.210 CONTROLSS_CTRL_CMPSSB8_RST Register

2.6.2.210.1 CONTROLSS_CTRL_CMPSSB8_RST Register (Offset = 3F0h) [reset = 0h]

cmpssb[x]_reset.

Return to Summary Table

Table 2-1881. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03F0h

Figure 2-938. CONTROLSS_CTRL_CMPSSB8_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMPSSB8_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1882. CONTROLSS_CTRL_CMPSSB8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB8_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssb

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2.6.2.211 CONTROLSS_CTRL_CMPSSB9_RST Register

2.6.2.211.1 CONTROLSS_CTRL_CMPSSB9_RST Register (Offset = 3F4h) [reset = 0h]

cmpssb[x]_reset.

Return to Summary Table

Table 2-1883. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 03F4h

Figure 2-939. CONTROLSS_CTRL_CMPSSB9_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMPSSB9_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1884. CONTROLSS_CTRL_CMPSSB9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	CMPSSB9_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding cmpssb

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2.6.2.212 CONTROLSS_CTRL_ECAP0_RST Register

2.6.2.212.1 CONTROLSS_CTRL_ECAP0_RST Register (Offset = 400h) [reset = 0h]

Ecap[x]_reset.

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Table 2-1885. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0400h

Figure 2-940. CONTROLSS_CTRL_ECAP0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1886. CONTROLSS_CTRL_ECAP0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.213 CONTROLSS_CTRL_ECAP1_RST Register

2.6.2.213.1 CONTROLSS_CTRL_ECAP1_RST Register (Offset = 404h) [reset = 0h]

Ecap[x]_reset.

Return to Summary Table

Table 2-1887. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0404h

Figure 2-941. CONTROLSS_CTRL_ECAP1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1888. CONTROLSS_CTRL_ECAP1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.214 CONTROLSS_CTRL_ECAP2_RST Register

2.6.2.214.1 CONTROLSS_CTRL_ECAP2_RST Register (Offset = 408h) [reset = 0h]

Ecap[x]_reset.

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Table 2-1889. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0408h

Figure 2-942. CONTROLSS_CTRL_ECAP2_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP2_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1890. CONTROLSS_CTRL_ECAP2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP2_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.215 CONTROLSS_CTRL_ECAP3_RST Register

2.6.2.215.1 CONTROLSS_CTRL_ECAP3_RST Register (Offset = 40Ch) [reset = 0h]

Ecap[x]_reset.

Return to Summary Table

Table 2-1891. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 040Ch

Figure 2-943. CONTROLSS_CTRL_ECAP3_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ECAP3_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1892. CONTROLSS_CTRL_ECAP3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP3_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.216 CONTROLSS_CTRL_ECAP4_RST Register

2.6.2.216.1 CONTROLSS_CTRL_ECAP4_RST Register (Offset = 410h) [reset = 0h]

Ecap[x]_reset.

Return to Summary Table

Table 2-1893. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0410h

Figure 2-944. CONTROLSS_CTRL_ECAP4_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP4_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1894. CONTROLSS_CTRL_ECAP4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP4_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.217 CONTROLSS_CTRL_ECAP5_RST Register

2.6.2.217.1 CONTROLSS_CTRL_ECAP5_RST Register (Offset = 414h) [reset = 0h]

Ecap[x]_reset.

Return to Summary Table

Table 2-1895. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0414h

Figure 2-945. CONTROLSS_CTRL_ECAP5_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP5_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1896. CONTROLSS_CTRL_ECAP5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP5_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.218 CONTROLSS_CTRL_ECAP6_RST Register

2.6.2.218.1 CONTROLSS_CTRL_ECAP6_RST Register (Offset = 418h) [reset = 0h]

Ecap[x]_reset.

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Table 2-1897. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0418h

Figure 2-946. CONTROLSS_CTRL_ECAP6_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP6_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1898. CONTROLSS_CTRL_ECAP6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP6_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.219 CONTROLSS_CTRL_ECAP7_RST Register

2.6.2.219.1 CONTROLSS_CTRL_ECAP7_RST Register (Offset = 41Ch) [reset = 0h]

Ecap[x]_reset.

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Table 2-1899. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 041Ch

Figure 2-947. CONTROLSS_CTRL_ECAP7_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ECAP7_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1900. CONTROLSS_CTRL_ECAP7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP7_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.220 CONTROLSS_CTRL_ECAP8_RST Register

2.6.2.220.1 CONTROLSS_CTRL_ECAP8_RST Register (Offset = 420h) [reset = 0h]

Ecap[x]_reset.

Return to Summary Table

Table 2-1901. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0420h

Figure 2-948. CONTROLSS_CTRL_ECAP8_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ECAP8_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1902. CONTROLSS_CTRL_ECAP8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP8_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.221 CONTROLSS_CTRL_ECAP9_RST Register

2.6.2.221.1 CONTROLSS_CTRL_ECAP9_RST Register (Offset = 424h) [reset = 0h]

Ecap[x]_reset.

Return to Summary Table

Table 2-1903. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0424h

Figure 2-949. CONTROLSS_CTRL_ECAP9_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP9_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1904. CONTROLSS_CTRL_ECAP9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP9_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.222 CONTROLSS_CTRL_ECAP10_RST Register

2.6.2.222.1 CONTROLSS_CTRL_ECAP10_RST Register (Offset = 428h) [reset = 0h]

Ecap[x]_reset.

Return to Summary Table

Table 2-1905. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0428h

Figure 2-950. CONTROLSS_CTRL_ECAP10_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP10_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1906. CONTROLSS_CTRL_ECAP10_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP10_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.223 CONTROLSS_CTRL_ECAP11_RST Register

2.6.2.223.1 CONTROLSS_CTRL_ECAP11_RST Register (Offset = 42Ch) [reset = 0h]

Ecap[x]_reset.

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Table 2-1907. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 042Ch

Figure 2-951. CONTROLSS_CTRL_ECAP11_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP11_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1908. CONTROLSS_CTRL_ECAP11_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP11_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.224 CONTROLSS_CTRL_ECAP12_RST Register

2.6.2.224.1 CONTROLSS_CTRL_ECAP12_RST Register (Offset = 430h) [reset = 0h]

Ecap[x]_reset.

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Table 2-1909. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0430h

Figure 2-952. CONTROLSS_CTRL_ECAP12_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP12_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1910. CONTROLSS_CTRL_ECAP12_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP12_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.225 CONTROLSS_CTRL_ECAP13_RST Register

2.6.2.225.1 CONTROLSS_CTRL_ECAP13_RST Register (Offset = 434h) [reset = 0h]

Ecap[x]_reset.

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Table 2-1911. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0434h

Figure 2-953. CONTROLSS_CTRL_ECAP13_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP13_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1912. CONTROLSS_CTRL_ECAP13_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP13_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.226 CONTROLSS_CTRL_ECAP14_RST Register

2.6.2.226.1 CONTROLSS_CTRL_ECAP14_RST Register (Offset = 438h) [reset = 0h]

Ecap[x]_reset.

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Table 2-1913. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0438h

Figure 2-954. CONTROLSS_CTRL_ECAP14_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP14_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1914. CONTROLSS_CTRL_ECAP14_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP14_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.227 CONTROLSS_CTRL_ECAP15_RST Register

2.6.2.227.1 CONTROLSS_CTRL_ECAP15_RST Register (Offset = 43Ch) [reset = 0h]

Ecap[x]_reset.

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Table 2-1915. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 043Ch

Figure 2-955. CONTROLSS_CTRL_ECAP15_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ECAP15_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1916. CONTROLSS_CTRL_ECAP15_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ECAP15_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding ecap

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2.6.2.228 CONTROLSS_CTRL_EQEP0_RST Register

2.6.2.228.1 CONTROLSS_CTRL_EQEP0_RST Register (Offset = 440h) [reset = 0h]

Eqep[x]_reset.

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Table 2-1917. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0440h

Figure 2-956. CONTROLSS_CTRL_EQEP0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EQEP0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1918. CONTROLSS_CTRL_EQEP0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EQEP0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding eqep

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2.6.2.229 CONTROLSS_CTRL_EQEP1_RST Register

2.6.2.229.1 CONTROLSS_CTRL_EQEP1_RST Register (Offset = 444h) [reset = 0h]

Eqep[x]_reset.

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Table 2-1919. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0444h

Figure 2-957. CONTROLSS_CTRL_EQEP1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EQEP1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1920. CONTROLSS_CTRL_EQEP1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EQEP1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding eqep

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2.6.2.230 CONTROLSS_CTRL_EQEP2_RST Register

2.6.2.230.1 CONTROLSS_CTRL_EQEP2_RST Register (Offset = 448h) [reset = 0h]

Eqep[x]_reset.

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Table 2-1921. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0448h

Figure 2-958. CONTROLSS_CTRL_EQEP2_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					EQEP2_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1922. CONTROLSS_CTRL_EQEP2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	EQEP2_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding eqep

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2.6.2.231 CONTROLSS_CTRL_SDFM0_RST Register

2.6.2.231.1 CONTROLSS_CTRL_SDFM0_RST Register (Offset = 450h) [reset = 0h]

Sdfm[x]_reset.

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Table 2-1923. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0450h

Figure 2-959. CONTROLSS_CTRL_SDFM0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					SDFM0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1924. CONTROLSS_CTRL_SDFM0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	SDFM0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding sdfm

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2.6.2.232 CONTROLSS_CTRL_SDFM1_RST Register

2.6.2.232.1 CONTROLSS_CTRL_SDFM1_RST Register (Offset = 454h) [reset = 0h]

Sdfm[x]_reset.

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Table 2-1925. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0454h

Figure 2-960. CONTROLSS_CTRL_SDFM1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					SDFM1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1926. CONTROLSS_CTRL_SDFM1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	SDFM1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding sdfm

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2.6.2.233 CONTROLSS_CTRL_DAC_RST Register

2.6.2.233.1 CONTROLSS_CTRL_DAC_RST Register (Offset = 458h) [reset = 0h]

dac_reset.

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Table 2-1927. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0458h

Figure 2-961. CONTROLSS_CTRL_DAC_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DAC_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1928. CONTROLSS_CTRL_DAC_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DAC_RST_RST	R/W	0h	Writing 3'b111 will generate reset for dac

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2.6.2.234 CONTROLSS_CTRL_ADC0_RST Register

2.6.2.234.1 CONTROLSS_CTRL_ADC0_RST Register (Offset = 45Ch) [reset = 0h]

Adc[x]_reset.

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Table 2-1929. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 045Ch

Figure 2-962. CONTROLSS_CTRL_ADC0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ADC0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1930. CONTROLSS_CTRL_ADC0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc

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2.6.2.235 CONTROLSS_CTRL_ADC1_RST Register

2.6.2.235.1 CONTROLSS_CTRL_ADC1_RST Register (Offset = 460h) [reset = 0h]

Adc[x]_reset.

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Table 2-1931. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0460h

Figure 2-963. CONTROLSS_CTRL_ADC1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ADC1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1932. CONTROLSS_CTRL_ADC1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc

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2.6.2.236 CONTROLSS_CTRL_ADC2_RST Register

2.6.2.236.1 CONTROLSS_CTRL_ADC2_RST Register (Offset = 464h) [reset = 0h]

Adc[x]_reset.

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Table 2-1933. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0464h

Figure 2-964. CONTROLSS_CTRL_ADC2_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC2_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1934. CONTROLSS_CTRL_ADC2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC2_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc

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2.6.2.237 CONTROLSS_CTRL_ADC3_RST Register

2.6.2.237.1 CONTROLSS_CTRL_ADC3_RST Register (Offset = 468h) [reset = 0h]

Adc[x]_reset.

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Table 2-1935. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0468h

Figure 2-965. CONTROLSS_CTRL_ADC3_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC3_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1936. CONTROLSS_CTRL_ADC3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC3_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc

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2.6.2.238 CONTROLSS_CTRL_ADC4_RST Register

2.6.2.238.1 CONTROLSS_CTRL_ADC4_RST Register (Offset = 46Ch) [reset = 0h]

Adc[x]_reset.

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Table 2-1937. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 046Ch

Figure 2-966. CONTROLSS_CTRL_ADC4_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC4_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1938. CONTROLSS_CTRL_ADC4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC4_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc

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2.6.2.239 CONTROLSS_CTRL_OTTO0_RST Register

2.6.2.239.1 CONTROLSS_CTRL_OTTO0_RST Register (Offset = 470h) [reset = 0h]

Otto[x]_reset.

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Table 2-1939. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0470h

Figure 2-967. CONTROLSS_CTRL_OTTO0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OTTO0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1940. CONTROLSS_CTRL_OTTO0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OTTO0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding otto

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2.6.2.240 CONTROLSS_CTRL_OTTO1_RST Register

2.6.2.240.1 CONTROLSS_CTRL_OTTO1_RST Register (Offset = 474h) [reset = 0h]

Otto[x]_reset.

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Table 2-1941. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0474h

Figure 2-968. CONTROLSS_CTRL_OTTO1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OTTO1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1942. CONTROLSS_CTRL_OTTO1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OTTO1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding otto

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2.6.2.241 CONTROLSS_CTRL_OTTO2_RST Register

2.6.2.241.1 CONTROLSS_CTRL_OTTO2_RST Register (Offset = 478h) [reset = 0h]

Otto[x]_reset.

Return to Summary Table

Table 2-1943. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0478h

Figure 2-969. CONTROLSS_CTRL_OTTO2_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OTTO2_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1944. CONTROLSS_CTRL_OTTO2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OTTO2_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding otto

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2.6.2.242 CONTROLSS_CTRL_OTTO3_RST Register

2.6.2.242.1 CONTROLSS_CTRL_OTTO3_RST Register (Offset = 47Ch) [reset = 0h]

Otto[x]_reset.

Return to Summary Table

Table 2-1945. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 047Ch

Figure 2-970. CONTROLSS_CTRL_OTTO3_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					OTTO3_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1946. CONTROLSS_CTRL_OTTO3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OTTO3_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding otto

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2.6.2.243 CONTROLSS_CTRL_HW_RESOLVER_RST Register

2.6.2.243.1 CONTROLSS_CTRL_HW_RESOLVER_RST Register (Offset = 480h) [reset = 0h]

Hardware resolver reset.

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Table 2-1947. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0480h

Figure 2-971. CONTROLSS_CTRL_HW_RESOLVER_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					HW_RESOLVER_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1948. CONTROLSS_CTRL_HW_RESOLVER_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	HW_RESOLVER_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding hw_resolver

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2.6.2.244 CONTROLSS_CTRL_ADC_SCTILE0_RST Register

2.6.2.244.1 CONTROLSS_CTRL_ADC_SCTILE0_RST Register (Offset = 484h) [reset = 0h]

ADC Safecheck tiles Reset.

Return to Summary Table

Table 2-1949. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0484h

Figure 2-972. CONTROLSS_CTRL_ADC_SCTILE0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ADC_SCTILE0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1950. CONTROLSS_CTRL_ADC_SCTILE0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.245 CONTROLSS_CTRL_ADC_SCTILE1_RST Register

2.6.2.245.1 CONTROLSS_CTRL_ADC_SCTILE1_RST Register (Offset = 488h) [reset = 0h]

ADC Safecheck tiles Reset.

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Table 2-1951. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0488h

Figure 2-973. CONTROLSS_CTRL_ADC_SCTILE1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1952. CONTROLSS_CTRL_ADC_SCTILE1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.246 CONTROLSS_CTRL_ADC_SCTILE2_RST Register

2.6.2.246.1 CONTROLSS_CTRL_ADC_SCTILE2_RST Register (Offset = 48Ch) [reset = 0h]

ADC Safecheck tiles Reset.

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Table 2-1953. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 048Ch

Figure 2-974. CONTROLSS_CTRL_ADC_SCTILE2_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ADC_SCTILE2_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1954. CONTROLSS_CTRL_ADC_SCTILE2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE2_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.247 CONTROLSS_CTRL_ADC_SCTILE3_RST Register

2.6.2.247.1 CONTROLSS_CTRL_ADC_SCTILE3_RST Register (Offset = 490h) [reset = 0h]

ADC Safecheck tiles Reset.

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Table 2-1955. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0490h

Figure 2-975. CONTROLSS_CTRL_ADC_SCTILE3_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE3_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1956. CONTROLSS_CTRL_ADC_SCTILE3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE3_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.248 CONTROLSS_CTRL_ADC_SCTILE4_RST Register

2.6.2.248.1 CONTROLSS_CTRL_ADC_SCTILE4_RST Register (Offset = 494h) [reset = 0h]

ADC Safecheck tiles Reset.

Return to Summary Table

Table 2-1957. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0494h

Figure 2-976. CONTROLSS_CTRL_ADC_SCTILE4_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE4_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1958. CONTROLSS_CTRL_ADC_SCTILE4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE4_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.249 CONTROLSS_CTRL_ADC_SCTILE5_RST Register

2.6.2.249.1 CONTROLSS_CTRL_ADC_SCTILE5_RST Register (Offset = 498h) [reset = 0h]

ADC Safecheck tiles Reset.

Return to Summary Table

Table 2-1959. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0498h

Figure 2-977. CONTROLSS_CTRL_ADC_SCTILE5_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE5_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1960. CONTROLSS_CTRL_ADC_SCTILE5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE5_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.250 CONTROLSS_CTRL_ADC_SCTILE6_RST Register

2.6.2.250.1 CONTROLSS_CTRL_ADC_SCTILE6_RST Register (Offset = 49Ch) [reset = 0h]

ADC Safecheck tiles Reset.

Return to Summary Table

Table 2-1961. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 049Ch

Figure 2-978. CONTROLSS_CTRL_ADC_SCTILE6_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ADC_SCTILE6_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1962. CONTROLSS_CTRL_ADC_SCTILE6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE6_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.251 CONTROLSS_CTRL_ADC_SCTILE7_RST Register

2.6.2.251.1 CONTROLSS_CTRL_ADC_SCTILE7_RST Register (Offset = 4A0h) [reset = 0h]

ADC Safecheck tiles Reset.

Return to Summary Table

Table 2-1963. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 04A0h

Figure 2-979. CONTROLSS_CTRL_ADC_SCTILE7_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE7_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1964. CONTROLSS_CTRL_ADC_SCTILE7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE7_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.252 CONTROLSS_CTRL_ADC_SCTILE8_RST Register

2.6.2.252.1 CONTROLSS_CTRL_ADC_SCTILE8_RST Register (Offset = 4A4h) [reset = 0h]

ADC Safecheck tiles Reset.

Return to Summary Table

Table 2-1965. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 04A4h

Figure 2-980. CONTROLSS_CTRL_ADC_SCTILE8_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					ADC_SCTILE8_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1966. CONTROLSS_CTRL_ADC_SCTILE8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE8_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.253 CONTROLSS_CTRL_ADC_SCTILE9_RST Register

2.6.2.253.1 CONTROLSS_CTRL_ADC_SCTILE9_RST Register (Offset = 4A8h) [reset = 0h]

ADC Safecheck tiles Reset.

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Table 2-1967. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 04A8h

Figure 2-981. CONTROLSS_CTRL_ADC_SCTILE9_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE9_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1968. CONTROLSS_CTRL_ADC_SCTILE9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE9_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.254 CONTROLSS_CTRL_ADC_SCTILE10_RST Register

2.6.2.254.1 CONTROLSS_CTRL_ADC_SCTILE10_RST Register (Offset = 4ACh) [reset = 0h]

ADC Safecheck tiles Reset.

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Table 2-1969. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 04ACh

Figure 2-982. CONTROLSS_CTRL_ADC_SCTILE10_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE10_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1970. CONTROLSS_CTRL_ADC_SCTILE10_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE10_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.255 CONTROLSS_CTRL_ADC_SCTILE11_RST Register

2.6.2.255.1 CONTROLSS_CTRL_ADC_SCTILE11_RST Register (Offset = 4B0h) [reset = 0h]

ADC Safecheck tiles Reset.

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Table 2-1971. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 04B0h

Figure 2-983. CONTROLSS_CTRL_ADC_SCTILE11_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_SCTILE11_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1972. CONTROLSS_CTRL_ADC_SCTILE11_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_SCTILE11_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc safety tiles

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2.6.2.256 CONTROLSS_CTRL_ADC_AGG0_RST Register

2.6.2.256.1 CONTROLSS_CTRL_ADC_AGG0_RST Register (Offset = 4C4h) [reset = 0h]

ADC Aggregator Reset.

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Table 2-1973. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 04C4h

Figure 2-984. CONTROLSS_CTRL_ADC_AGG0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADC_AGG0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1974. CONTROLSS_CTRL_ADC_AGG0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADC_AGG0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc aggregator

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2.6.2.257 CONTROLSS_CTRL_ADCR0_RST Register

2.6.2.257.1 CONTROLSS_CTRL_ADCR0_RST Register (Offset = 4C8h) [reset = 0h]

Adcr[x] reset.

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Table 2-1975. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 04C8h

Figure 2-985. CONTROLSS_CTRL_ADCR0_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADCR0_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1976. CONTROLSS_CTRL_ADCR0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADCR0_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc

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2.6.2.258 CONTROLSS_CTRL_ADCR1_RST Register

2.6.2.258.1 CONTROLSS_CTRL_ADCR1_RST Register (Offset = 4CCh) [reset = 0h]

Adcr[x] reset.

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Table 2-1977. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 04CCh

Figure 2-986. CONTROLSS_CTRL_ADCR1_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADCR1_RST_RST		
NONE					R/W		
0h					0h		

Table 2-1978. CONTROLSS_CTRL_ADCR1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADCR1_RST_RST	R/W	0h	Writing 3'b111 will generate reset for corresponding adc

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2.6.2.259 CONTROLSS_CTRL_EPWM0_HALTEN Register

2.6.2.259.1 CONTROLSS_CTRL_EPWM0_HALTEN Register (Offset = 500h) [reset = 0h]

Epwm halt enable.

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Table 2-1979. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0500h

Figure 2-987. CONTROLSS_CTRL_EPWM0_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM0_HALTEN_CR5B1	EPWM0_HALTEN_CR5A1	EPWM0_HALTEN_CR5B0	EPWM0_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1980. CONTROLSS_CTRL_EPWM0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM0_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM0_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM0_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM0_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.260 CONTROLSS_CTRL_EPWM1_HALTEN Register

2.6.2.260.1 CONTROLSS_CTRL_EPWM1_HALTEN Register (Offset = 504h) [reset = 0h]

Epwm halt enable.

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Table 2-1981. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0504h

Figure 2-988. CONTROLSS_CTRL_EPWM1_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EPWM1_HALTEN_CR5B1	EPWM1_HALTEN_CR5A1	EPWM1_HALTEN_CR5B0	EPWM1_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1982. CONTROLSS_CTRL_EPWM1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM1_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM1_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM1_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM1_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.261 CONTROLSS_CTRL_EPWM2_HALTEN Register

2.6.2.261.1 CONTROLSS_CTRL_EPWM2_HALTEN Register (Offset = 508h) [reset = 0h]

Epwm halt enable.

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Table 2-1983. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0508h

Figure 2-989. CONTROLSS_CTRL_EPWM2_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM2_HALTEN_CR5B1	EPWM2_HALTEN_CR5A1	EPWM2_HALTEN_CR5B0	EPWM2_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1984. CONTROLSS_CTRL_EPWM2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM2_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM2_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM2_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM2_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.262 CONTROLSS_CTRL_EPWM3_HALTEN Register

2.6.2.262.1 CONTROLSS_CTRL_EPWM3_HALTEN Register (Offset = 50Ch) [reset = 0h]

Epwm halt enable.

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Table 2-1985. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 050Ch

Figure 2-990. CONTROLSS_CTRL_EPWM3_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM3_HALTEN_CR5B1	EPWM3_HALTEN_CR5A1	EPWM3_HALTEN_CR5B0	EPWM3_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1986. CONTROLSS_CTRL_EPWM3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM3_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM3_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM3_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM3_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.263 CONTROLSS_CTRL_EPWM4_HALTEN Register

2.6.2.263.1 CONTROLSS_CTRL_EPWM4_HALTEN Register (Offset = 510h) [reset = 0h]

Epwm halt enable.

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Table 2-1987. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0510h

Figure 2-991. CONTROLSS_CTRL_EPWM4_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM4_HALTEN_CR5B1	EPWM4_HALTEN_CR5A1	EPWM4_HALTEN_CR5B0	EPWM4_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1988. CONTROLSS_CTRL_EPWM4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM4_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM4_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM4_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM4_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.264 CONTROLSS_CTRL_EPWM5_HALTEN Register

2.6.2.264.1 CONTROLSS_CTRL_EPWM5_HALTEN Register (Offset = 514h) [reset = 0h]

Epwm halt enable.

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Table 2-1989. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0514h

Figure 2-992. CONTROLSS_CTRL_EPWM5_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM5_HALTEN_CR5B1	EPWM5_HALTEN_CR5A1	EPWM5_HALTEN_CR5B0	EPWM5_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1990. CONTROLSS_CTRL_EPWM5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM5_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM5_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM5_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM5_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.265 CONTROLSS_CTRL_EPWM6_HALTEN Register

2.6.2.265.1 CONTROLSS_CTRL_EPWM6_HALTEN Register (Offset = 518h) [reset = 0h]

Epwm halt enable.

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Table 2-1991. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0518h

Figure 2-993. CONTROLSS_CTRL_EPWM6_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM6_HALTEN_CR5B1	EPWM6_HALTEN_CR5A1	EPWM6_HALTEN_CR5B0	EPWM6_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1992. CONTROLSS_CTRL_EPWM6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM6_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM6_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM6_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM6_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.266 CONTROLSS_CTRL_EPWM7_HALTEN Register

2.6.2.266.1 CONTROLSS_CTRL_EPWM7_HALTEN Register (Offset = 51Ch) [reset = 0h]

Epwm halt enable.

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Table 2-1993. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 051Ch

Figure 2-994. CONTROLSS_CTRL_EPWM7_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM7_HALTEN_CR5B1	EPWM7_HALTEN_CR5A1	EPWM7_HALTEN_CR5B0	EPWM7_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1994. CONTROLSS_CTRL_EPWM7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM7_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM7_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM7_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM7_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.267 CONTROLSS_CTRL_EPWM8_HALTEN Register

2.6.2.267.1 CONTROLSS_CTRL_EPWM8_HALTEN Register (Offset = 520h) [reset = 0h]

Epwm halt enable.

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Table 2-1995. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0520h

Figure 2-995. CONTROLSS_CTRL_EPWM8_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM8_HALTEN_CR5B1	EPWM8_HALTEN_CR5A1	EPWM8_HALTEN_CR5B0	EPWM8_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1996. CONTROLSS_CTRL_EPWM8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM8_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM8_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM8_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM8_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.268 CONTROLSS_CTRL_EPWM9_HALTEN Register

2.6.2.268.1 CONTROLSS_CTRL_EPWM9_HALTEN Register (Offset = 524h) [reset = 0h]

Epwm halt enable.

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Table 2-1997. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0524h

Figure 2-996. CONTROLSS_CTRL_EPWM9_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EPWM9_HALTEN_CR5B1	EPWM9_HALTEN_CR5A1	EPWM9_HALTEN_CR5B0	EPWM9_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-1998. CONTROLSS_CTRL_EPWM9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM9_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM9_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM9_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM9_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.269 CONTROLSS_CTRL_EPWM10_HALTEN Register

2.6.2.269.1 CONTROLSS_CTRL_EPWM10_HALTEN Register (Offset = 528h) [reset = 0h]

Epwm halt enable.

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Table 2-1999. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0528h

Figure 2-997. CONTROLSS_CTRL_EPWM10_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EPWM10_HALTEN_CR5B1	EPWM10_HALTEN_CR5A1	EPWM10_HALTEN_CR5B0	EPWM10_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2000. CONTROLSS_CTRL_EPWM10_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM10_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM10_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM10_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM10_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.270 CONTROLSS_CTRL_EPWM11_HALTEN Register

2.6.2.270.1 CONTROLSS_CTRL_EPWM11_HALTEN Register (Offset = 52Ch) [reset = 0h]

Epwm halt enable.

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Table 2-2001. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 052Ch

Figure 2-998. CONTROLSS_CTRL_EPWM11_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM11_HALTEN_CR5B1	EPWM11_HALTEN_CR5A1	EPWM11_HALTEN_CR5B0	EPWM11_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2002. CONTROLSS_CTRL_EPWM11_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM11_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM11_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM11_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM11_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.271 CONTROLSS_CTRL_EPWM12_HALTEN Register

2.6.2.271.1 CONTROLSS_CTRL_EPWM12_HALTEN Register (Offset = 530h) [reset = 0h]

Epwm halt enable.

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Table 2-2003. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0530h

Figure 2-999. CONTROLSS_CTRL_EPWM12_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM12_HALTEN_CR5B1	EPWM12_HALTEN_CR5A1	EPWM12_HALTEN_CR5B0	EPWM12_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2004. CONTROLSS_CTRL_EPWM12_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM12_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM12_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM12_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM12_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.272 CONTROLSS_CTRL_EPWM13_HALTEN Register

2.6.2.272.1 CONTROLSS_CTRL_EPWM13_HALTEN Register (Offset = 534h) [reset = 0h]

Epwm halt enable.

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Table 2-2005. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0534h

Figure 2-1000. CONTROLSS_CTRL_EPWM13_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM13_HALTEN_CR5B1	EPWM13_HALTEN_CR5A1	EPWM13_HALTEN_CR5B0	EPWM13_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2006. CONTROLSS_CTRL_EPWM13_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM13_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM13_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM13_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM13_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.273 CONTROLSS_CTRL_EPWM14_HALTEN Register

2.6.2.273.1 CONTROLSS_CTRL_EPWM14_HALTEN Register (Offset = 538h) [reset = 0h]

Epwm halt enable.

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Table 2-2007. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0538h

Figure 2-1001. CONTROLSS_CTRL_EPWM14_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EPWM14_HALTEN_CR5B1	EPWM14_HALTEN_CR5A1	EPWM14_HALTEN_CR5B0	EPWM14_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2008. CONTROLSS_CTRL_EPWM14_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM14_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM14_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM14_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM14_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.274 CONTROLSS_CTRL_EPWM15_HALTEN Register

2.6.2.274.1 CONTROLSS_CTRL_EPWM15_HALTEN Register (Offset = 53Ch) [reset = 0h]

Epwm halt enable.

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Table 2-2009. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 053Ch

Figure 2-1002. CONTROLSS_CTRL_EPWM15_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EPWM15_HALTEN_CR5B1	EPWM15_HALTEN_CR5A1	EPWM15_HALTEN_CR5B0	EPWM15_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2010. CONTROLSS_CTRL_EPWM15_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM15_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM15_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM15_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM15_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.275 CONTROLSS_CTRL_EPWM16_HALTEN Register

2.6.2.275.1 CONTROLSS_CTRL_EPWM16_HALTEN Register (Offset = 540h) [reset = 0h]

Epwm halt enable.

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Table 2-2011. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0540h

Figure 2-1003. CONTROLSS_CTRL_EPWM16_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM16_HALTEN_CR5B1	EPWM16_HALTEN_CR5A1	EPWM16_HALTEN_CR5B0	EPWM16_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2012. CONTROLSS_CTRL_EPWM16_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM16_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM16_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM16_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM16_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.276 CONTROLSS_CTRL_EPWM17_HALTEN Register

2.6.2.276.1 CONTROLSS_CTRL_EPWM17_HALTEN Register (Offset = 544h) [reset = 0h]

Epwm halt enable.

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Table 2-2013. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0544h

Figure 2-1004. CONTROLSS_CTRL_EPWM17_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EPWM17_HALTEN_CR5B1	EPWM17_HALTEN_CR5A1	EPWM17_HALTEN_CR5B0	EPWM17_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2014. CONTROLSS_CTRL_EPWM17_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM17_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM17_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM17_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM17_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.277 CONTROLSS_CTRL_EPWM18_HALTEN Register

2.6.2.277.1 CONTROLSS_CTRL_EPWM18_HALTEN Register (Offset = 548h) [reset = 0h]

Epwm halt enable.

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Table 2-2015. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0548h

Figure 2-1005. CONTROLSS_CTRL_EPWM18_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM18_HALTEN_CR5B1	EPWM18_HALTEN_CR5A1	EPWM18_HALTEN_CR5B0	EPWM18_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2016. CONTROLSS_CTRL_EPWM18_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM18_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM18_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM18_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM18_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.278 CONTROLSS_CTRL_EPWM19_HALTEN Register

2.6.2.278.1 CONTROLSS_CTRL_EPWM19_HALTEN Register (Offset = 54Ch) [reset = 0h]

Epwm halt enable.

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Table 2-2017. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 054Ch

Figure 2-1006. CONTROLSS_CTRL_EPWM19_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM19_HALTEN_CR5B1	EPWM19_HALTEN_CR5A1	EPWM19_HALTEN_CR5B0	EPWM19_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2018. CONTROLSS_CTRL_EPWM19_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM19_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM19_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM19_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM19_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.279 CONTROLSS_CTRL_EPWM20_HALTEN Register

2.6.2.279.1 CONTROLSS_CTRL_EPWM20_HALTEN Register (Offset = 550h) [reset = 0h]

Epwm halt enable.

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Table 2-2019. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0550h

Figure 2-1007. CONTROLSS_CTRL_EPWM20_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM20_HALTEN_CR5B1	EPWM20_HALTEN_CR5A1	EPWM20_HALTEN_CR5B0	EPWM20_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2020. CONTROLSS_CTRL_EPWM20_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM20_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM20_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM20_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM20_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.280 CONTROLSS_CTRL_EPWM21_HALTEN Register

2.6.2.280.1 CONTROLSS_CTRL_EPWM21_HALTEN Register (Offset = 554h) [reset = 0h]

Epwm halt enable.

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Table 2-2021. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0554h

Figure 2-1008. CONTROLSS_CTRL_EPWM21_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM21_HALTEN_CR5B1	EPWM21_HALTEN_CR5A1	EPWM21_HALTEN_CR5B0	EPWM21_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2022. CONTROLSS_CTRL_EPWM21_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM21_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM21_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM21_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM21_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.281 CONTROLSS_CTRL_EPWM22_HALTEN Register

2.6.2.281.1 CONTROLSS_CTRL_EPWM22_HALTEN Register (Offset = 558h) [reset = 0h]

Epwm halt enable.

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Table 2-2023. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0558h

Figure 2-1009. CONTROLSS_CTRL_EPWM22_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM22_HALTEN_CR5B1	EPWM22_HALTEN_CR5A1	EPWM22_HALTEN_CR5B0	EPWM22_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2024. CONTROLSS_CTRL_EPWM22_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM22_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM22_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM22_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM22_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.282 CONTROLSS_CTRL_EPWM23_HALTEN Register

2.6.2.282.1 CONTROLSS_CTRL_EPWM23_HALTEN Register (Offset = 55Ch) [reset = 0h]

Epwm halt enable.

Return to Summary Table

Table 2-2025. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 055Ch

Figure 2-1010. CONTROLSS_CTRL_EPWM23_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM23_HALTEN_CR5B1	EPWM23_HALTEN_CR5A1	EPWM23_HALTEN_CR5B0	EPWM23_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2026. CONTROLSS_CTRL_EPWM23_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM23_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM23_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM23_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM23_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.283 CONTROLSS_CTRL_EPWM24_HALTEN Register

2.6.2.283.1 CONTROLSS_CTRL_EPWM24_HALTEN Register (Offset = 560h) [reset = 0h]

Epwm halt enable.

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Table 2-2027. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0560h

Figure 2-1011. CONTROLSS_CTRL_EPWM24_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM24_HALTEN_CR5B1	EPWM24_HALTEN_CR5A1	EPWM24_HALTEN_CR5B0	EPWM24_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2028. CONTROLSS_CTRL_EPWM24_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM24_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM24_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM24_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM24_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.284 CONTROLSS_CTRL_EPWM25_HALTEN Register

2.6.2.284.1 CONTROLSS_CTRL_EPWM25_HALTEN Register (Offset = 564h) [reset = 0h]

Epwm halt enable.

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Table 2-2029. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0564h

Figure 2-1012. CONTROLSS_CTRL_EPWM25_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED				EPWM25_HALTEN_CR5B1	EPWM25_HALTEN_CR5A1	EPWM25_HALTEN_CR5B0	EPWM25_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2030. CONTROLSS_CTRL_EPWM25_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM25_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM25_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM25_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM25_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.285 CONTROLSS_CTRL_EPWM26_HALTEN Register

2.6.2.285.1 CONTROLSS_CTRL_EPWM26_HALTEN Register (Offset = 568h) [reset = 0h]

Epwm halt enable.

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Table 2-2031. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0568h

Figure 2-1013. CONTROLSS_CTRL_EPWM26_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EPWM26_HALTEN_CR5B1	EPWM26_HALTEN_CR5A1	EPWM26_HALTEN_CR5B0	EPWM26_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2032. CONTROLSS_CTRL_EPWM26_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM26_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM26_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM26_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM26_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.286 CONTROLSS_CTRL_EPWM27_HALTEN Register

2.6.2.286.1 CONTROLSS_CTRL_EPWM27_HALTEN Register (Offset = 56Ch) [reset = 0h]

Epwm halt enable.

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Table 2-2033. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 056Ch

Figure 2-1014. CONTROLSS_CTRL_EPWM27_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM27_HALTEN_CR5B1	EPWM27_HALTEN_CR5A1	EPWM27_HALTEN_CR5B0	EPWM27_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2034. CONTROLSS_CTRL_EPWM27_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM27_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM27_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM27_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM27_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.287 CONTROLSS_CTRL_EPWM28_HALTEN Register

2.6.2.287.1 CONTROLSS_CTRL_EPWM28_HALTEN Register (Offset = 570h) [reset = 0h]

Epwm halt enable.

Return to Summary Table

Table 2-2035. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0570h

Figure 2-1015. CONTROLSS_CTRL_EPWM28_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EPWM28_HALTEN_CR5B1	EPWM28_HALTEN_CR5A1	EPWM28_HALTEN_CR5B0	EPWM28_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2036. CONTROLSS_CTRL_EPWM28_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM28_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM28_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM28_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM28_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.288 CONTROLSS_CTRL_EPWM29_HALTEN Register

2.6.2.288.1 CONTROLSS_CTRL_EPWM29_HALTEN Register (Offset = 574h) [reset = 0h]

Epwm halt enable.

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Table 2-2037. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0574h

Figure 2-1016. CONTROLSS_CTRL_EPWM29_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM29_HALTEN_CR5B1	EPWM29_HALTEN_CR5A1	EPWM29_HALTEN_CR5B0	EPWM29_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2038. CONTROLSS_CTRL_EPWM29_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM29_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM29_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM29_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM29_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.289 CONTROLSS_CTRL_EPWM30_HALTEN Register

2.6.2.289.1 CONTROLSS_CTRL_EPWM30_HALTEN Register (Offset = 578h) [reset = 0h]

Epwm halt enable.

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Table 2-2039. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0578h

Figure 2-1017. CONTROLSS_CTRL_EPWM30_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM30_HALTEN_CR5B1	EPWM30_HALTEN_CR5A1	EPWM30_HALTEN_CR5B0	EPWM30_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2040. CONTROLSS_CTRL_EPWM30_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM30_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM30_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM30_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM30_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.290 CONTROLSS_CTRL_EPWM31_HALTEN Register

2.6.2.290.1 CONTROLSS_CTRL_EPWM31_HALTEN Register (Offset = 57Ch) [reset = 0h]

Epwm halt enable.

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Table 2-2041. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 057Ch

Figure 2-1018. CONTROLSS_CTRL_EPWM31_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EPWM31_HALTEN_CR5B1	EPWM31_HALTEN_CR5A1	EPWM31_HALTEN_CR5B0	EPWM31_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2042. CONTROLSS_CTRL_EPWM31_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EPWM31_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EPWM31_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EPWM31_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EPWM31_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.291 CONTROLSS_CTRL_CMPSSA0_HALTEN Register

2.6.2.291.1 CONTROLSS_CTRL_CMPSSA0_HALTEN Register (Offset = 580h) [reset = 0h]

cmpssa halt enable.

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Table 2-2043. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0580h

Figure 2-1019. CONTROLSS_CTRL_CMPSSA0_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSA0_HALTEN_CR5B1	CMPSSA0_HALTEN_CR5A1	CMPSSA0_HALTEN_CR5B0	CMPSSA0_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2044. CONTROLSS_CTRL_CMPSSA0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSA0_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSA0_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSA0_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSA0_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.292 CONTROLSS_CTRL_CMPSSA1_HALTEN Register

2.6.2.292.1 CONTROLSS_CTRL_CMPSSA1_HALTEN Register (Offset = 584h) [reset = 0h]

cmpssa halt enable.

Return to Summary Table

Table 2-2045. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0584h

Figure 2-1020. CONTROLSS_CTRL_CMPSSA1_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSA1_HALTEN_CR5B1	CMPSSA1_HALTEN_CR5A1	CMPSSA1_HALTEN_CR5B0	CMPSSA1_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2046. CONTROLSS_CTRL_CMPSSA1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSA1_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSA1_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSA1_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSA1_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.293 CONTROLSS_CTRL_CMPSSA2_HALTEN Register

2.6.2.293.1 CONTROLSS_CTRL_CMPSSA2_HALTEN Register (Offset = 588h) [reset = 0h]

cmpssa halt enable.

Return to Summary Table

Table 2-2047. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0588h

Figure 2-1021. CONTROLSS_CTRL_CMPSSA2_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSA2_HALTEN_CR5B1	CMPSSA2_HALTEN_CR5A1	CMPSSA2_HALTEN_CR5B0	CMPSSA2_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2048. CONTROLSS_CTRL_CMPSSA2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSA2_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSA2_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSA2_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSA2_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.294 CONTROLSS_CTRL_CMPSSA3_HALTEN Register

2.6.2.294.1 CONTROLSS_CTRL_CMPSSA3_HALTEN Register (Offset = 58Ch) [reset = 0h]

cmpssa halt enable.

Return to Summary Table

Table 2-2049. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 058Ch

Figure 2-1022. CONTROLSS_CTRL_CMPSSA3_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSA3_HALTEN_CR5B1	CMPSSA3_HALTEN_CR5A1	CMPSSA3_HALTEN_CR5B0	CMPSSA3_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2050. CONTROLSS_CTRL_CMPSSA3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSA3_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSA3_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSA3_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSA3_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.295 CONTROLSS_CTRL_CMPSSA4_HALTEN Register

2.6.2.295.1 CONTROLSS_CTRL_CMPSSA4_HALTEN Register (Offset = 590h) [reset = 0h]

cmpssa halt enable.

Return to Summary Table

Table 2-2051. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0590h

Figure 2-1023. CONTROLSS_CTRL_CMPSSA4_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSA4_HALTEN_CR5B1	CMPSSA4_HALTEN_CR5A1	CMPSSA4_HALTEN_CR5B0	CMPSSA4_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2052. CONTROLSS_CTRL_CMPSSA4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSA4_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSA4_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSA4_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSA4_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.296 CONTROLSS_CTRL_CMPSSA5_HALTEN Register

2.6.2.296.1 CONTROLSS_CTRL_CMPSSA5_HALTEN Register (Offset = 594h) [reset = 0h]

cmpssa halt enable.

Return to Summary Table

Table 2-2053. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0594h

Figure 2-1024. CONTROLSS_CTRL_CMPSSA5_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSA5_HALTEN_CR5B1	CMPSSA5_HALTEN_CR5A1	CMPSSA5_HALTEN_CR5B0	CMPSSA5_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2054. CONTROLSS_CTRL_CMPSSA5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSA5_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSA5_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSA5_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSA5_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.297 CONTROLSS_CTRL_CMPSSA6_HALTEN Register

2.6.2.297.1 CONTROLSS_CTRL_CMPSSA6_HALTEN Register (Offset = 598h) [reset = 0h]

cmpssa halt enable.

Return to Summary Table

Table 2-2055. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0598h

Figure 2-1025. CONTROLSS_CTRL_CMPSSA6_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CMPSSA6_HALTEN_CR5B1	CMPSSA6_HALTEN_CR5A1	CMPSSA6_HALTEN_CR5B0	CMPSSA6_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2056. CONTROLSS_CTRL_CMPSSA6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSA6_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSA6_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSA6_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSA6_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.298 CONTROLSS_CTRL_CMPSSA7_HALTEN Register

2.6.2.298.1 CONTROLSS_CTRL_CMPSSA7_HALTEN Register (Offset = 59Ch) [reset = 0h]

cmpssa halt enable.

Return to Summary Table

Table 2-2057. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 059Ch

Figure 2-1026. CONTROLSS_CTRL_CMPSSA7_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CMPSSA7_HALTEN_CR5B1	CMPSSA7_HALTEN_CR5A1	CMPSSA7_HALTEN_CR5B0	CMPSSA7_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2058. CONTROLSS_CTRL_CMPSSA7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSA7_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSA7_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSA7_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSA7_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.299 CONTROLSS_CTRL_CMPSSA8_HALTEN Register

2.6.2.299.1 CONTROLSS_CTRL_CMPSSA8_HALTEN Register (Offset = 5A0h) [reset = 0h]

cmpssa halt enable.

Return to Summary Table

Table 2-2059. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05A0h

Figure 2-1027. CONTROLSS_CTRL_CMPSSA8_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CMPSSA8_HALTEN_CR5B1	CMPSSA8_HALTEN_CR5A1	CMPSSA8_HALTEN_CR5B0	CMPSSA8_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2060. CONTROLSS_CTRL_CMPSSA8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSA8_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSA8_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSA8_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSA8_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.300 CONTROLSS_CTRL_CMPSSA9_HALTEN Register

2.6.2.300.1 CONTROLSS_CTRL_CMPSSA9_HALTEN Register (Offset = 5A4h) [reset = 0h]

cmpssa halt enable.

Return to Summary Table

Table 2-2061. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05A4h

Figure 2-1028. CONTROLSS_CTRL_CMPSSA9_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CMPSSA9_HALTEN_CR5B1	CMPSSA9_HALTEN_CR5A1	CMPSSA9_HALTEN_CR5B0	CMPSSA9_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2062. CONTROLSS_CTRL_CMPSSA9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSA9_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSA9_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSA9_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSA9_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.301 CONTROLSS_CTRL_CMPSSB0_HALTEN Register

2.6.2.301.1 CONTROLSS_CTRL_CMPSSB0_HALTEN Register (Offset = 5A8h) [reset = 0h]

cmpssb halt enable.

Return to Summary Table

Table 2-2063. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05A8h

Figure 2-1029. CONTROLSS_CTRL_CMPSSB0_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSB0_HALTEN_CR5B1	CMPSSB0_HALTEN_CR5A1	CMPSSB0_HALTEN_CR5B0	CMPSSB0_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2064. CONTROLSS_CTRL_CMPSSB0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSB0_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSB0_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSB0_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSB0_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.302 CONTROLSS_CTRL_CMPSSB1_HALTEN Register

2.6.2.302.1 CONTROLSS_CTRL_CMPSSB1_HALTEN Register (Offset = 5ACh) [reset = 0h]

cmpssb halt enable.

Return to Summary Table

Table 2-2065. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05ACh

Figure 2-1030. CONTROLSS_CTRL_CMPSSB1_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSB1_HALTEN_CR5B1	CMPSSB1_HALTEN_CR5A1	CMPSSB1_HALTEN_CR5B0	CMPSSB1_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2066. CONTROLSS_CTRL_CMPSSB1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSB1_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSB1_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSB1_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSB1_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.303 CONTROLSS_CTRL_CMPSSB2_HALTEN Register

2.6.2.303.1 CONTROLSS_CTRL_CMPSSB2_HALTEN Register (Offset = 5B0h) [reset = 0h]

cmpssb halt enable.

Return to Summary Table

Table 2-2067. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05B0h

Figure 2-1031. CONTROLSS_CTRL_CMPSSB2_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CMPSSB2_HALTEN_CR5B1	CMPSSB2_HALTEN_CR5A1	CMPSSB2_HALTEN_CR5B0	CMPSSB2_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2068. CONTROLSS_CTRL_CMPSSB2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSB2_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSB2_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSB2_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSB2_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.304 CONTROLSS_CTRL_CMPSSB3_HALTEN Register

2.6.2.304.1 CONTROLSS_CTRL_CMPSSB3_HALTEN Register (Offset = 5B4h) [reset = 0h]

cmpssb halt enable.

Return to Summary Table

Table 2-2069. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05B4h

Figure 2-1032. CONTROLSS_CTRL_CMPSSB3_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSB3_HALTEN_CR5B1	CMPSSB3_HALTEN_CR5A1	CMPSSB3_HALTEN_CR5B0	CMPSSB3_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2070. CONTROLSS_CTRL_CMPSSB3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSB3_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSB3_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSB3_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSB3_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.305 CONTROLSS_CTRL_CMPSSB4_HALTEN Register

2.6.2.305.1 CONTROLSS_CTRL_CMPSSB4_HALTEN Register (Offset = 5B8h) [reset = 0h]

cmpssb halt enable.

Return to Summary Table

Table 2-2071. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05B8h

Figure 2-1033. CONTROLSS_CTRL_CMPSSB4_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSB4_HALTEN_CR5B1	CMPSSB4_HALTEN_CR5A1	CMPSSB4_HALTEN_CR5B0	CMPSSB4_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2072. CONTROLSS_CTRL_CMPSSB4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSB4_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSB4_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSB4_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSB4_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.306 CONTROLSS_CTRL_CMPSSB5_HALTEN Register

2.6.2.306.1 CONTROLSS_CTRL_CMPSSB5_HALTEN Register (Offset = 5BCh) [reset = 0h]

cmpssb halt enable.

Return to Summary Table

Table 2-2073. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05BCh

Figure 2-1034. CONTROLSS_CTRL_CMPSSB5_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSB5_HALTEN_CR5B1	CMPSSB5_HALTEN_CR5A1	CMPSSB5_HALTEN_CR5B0	CMPSSB5_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2074. CONTROLSS_CTRL_CMPSSB5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSB5_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSB5_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSB5_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSB5_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.307 CONTROLSS_CTRL_CMPSSB6_HALTEN Register

2.6.2.307.1 CONTROLSS_CTRL_CMPSSB6_HALTEN Register (Offset = 5C0h) [reset = 0h]

cmpssb halt enable.

Return to Summary Table

Table 2-2075. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05C0h

Figure 2-1035. CONTROLSS_CTRL_CMPSSB6_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CMPSSB6_HALTEN_CR5B1	CMPSSB6_HALTEN_CR5A1	CMPSSB6_HALTEN_CR5B0	CMPSSB6_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2076. CONTROLSS_CTRL_CMPSSB6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSB6_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSB6_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSB6_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSB6_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.308 CONTROLSS_CTRL_CMPSSB7_HALTEN Register

2.6.2.308.1 CONTROLSS_CTRL_CMPSSB7_HALTEN Register (Offset = 5C4h) [reset = 0h]

cmpssb halt enable.

Return to Summary Table

Table 2-2077. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05C4h

Figure 2-1036. CONTROLSS_CTRL_CMPSSB7_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSB7_HALTEN_CR5B1	CMPSSB7_HALTEN_CR5A1	CMPSSB7_HALTEN_CR5B0	CMPSSB7_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2078. CONTROLSS_CTRL_CMPSSB7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSB7_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSB7_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSB7_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSB7_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.309 CONTROLSS_CTRL_CMPSSB8_HALTEN Register

2.6.2.309.1 CONTROLSS_CTRL_CMPSSB8_HALTEN Register (Offset = 5C8h) [reset = 0h]

cmpssb halt enable.

Return to Summary Table

Table 2-2079. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05C8h

Figure 2-1037. CONTROLSS_CTRL_CMPSSB8_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CMPSSB8_HALTEN_CR5B1	CMPSSB8_HALTEN_CR5A1	CMPSSB8_HALTEN_CR5B0	CMPSSB8_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2080. CONTROLSS_CTRL_CMPSSB8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSB8_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSB8_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSB8_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSB8_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.310 CONTROLSS_CTRL_CMPSSB9_HALTEN Register

2.6.2.310.1 CONTROLSS_CTRL_CMPSSB9_HALTEN Register (Offset = 5CCh) [reset = 0h]

cmpssb halt enable.

Return to Summary Table

Table 2-2081. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05CCh

Figure 2-1038. CONTROLSS_CTRL_CMPSSB9_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				CMPSSB9_HALTEN_CR5B1	CMPSSB9_HALTEN_CR5A1	CMPSSB9_HALTEN_CR5B0	CMPSSB9_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2082. CONTROLSS_CTRL_CMPSSB9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	CMPSSB9_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	CMPSSB9_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	CMPSSB9_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	CMPSSB9_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.311 CONTROLSS_CTRL_ECAP0_HALTEN Register

2.6.2.311.1 CONTROLSS_CTRL_ECAP0_HALTEN Register (Offset = 5D0h) [reset = 0h]

Ecap halt enable.

Return to Summary Table

Table 2-2083. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05D0h

Figure 2-1039. CONTROLSS_CTRL_ECAP0_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP0_HALTEN_CR5B1	ECAP0_HALTEN_CR5A1	ECAP0_HALTEN_CR5B0	ECAP0_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2084. CONTROLSS_CTRL_ECAP0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP0_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP0_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP0_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP0_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.312 CONTROLSS_CTRL_ECAP1_HALTEN Register

2.6.2.312.1 CONTROLSS_CTRL_ECAP1_HALTEN Register (Offset = 5D4h) [reset = 0h]

Ecap halt enable.

Return to Summary Table

Table 2-2085. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05D4h

Figure 2-1040. CONTROLSS_CTRL_ECAP1_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP1_HALTEN_CR5B1	ECAP1_HALTEN_CR5A1	ECAP1_HALTEN_CR5B0	ECAP1_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2086. CONTROLSS_CTRL_ECAP1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP1_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP1_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP1_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP1_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.313 CONTROLSS_CTRL_ECAP2_HALTEN Register

2.6.2.313.1 CONTROLSS_CTRL_ECAP2_HALTEN Register (Offset = 5D8h) [reset = 0h]

Ecap halt enable.

Return to Summary Table

Table 2-2087. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05D8h

Figure 2-1041. CONTROLSS_CTRL_ECAP2_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ECAP2_HALTEN_CR5B1	ECAP2_HALTEN_CR5A1	ECAP2_HALTEN_CR5B0	ECAP2_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2088. CONTROLSS_CTRL_ECAP2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP2_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP2_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP2_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP2_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.314 CONTROLSS_CTRL_ECAP3_HALTEN Register

2.6.2.314.1 CONTROLSS_CTRL_ECAP3_HALTEN Register (Offset = 5DCh) [reset = 0h]

Ecap halt enable.

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Table 2-2089. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05DCh

Figure 2-1042. CONTROLSS_CTRL_ECAP3_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ECAP3_HALTEN_CR5B1	ECAP3_HALTEN_CR5A1	ECAP3_HALTEN_CR5B0	ECAP3_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2090. CONTROLSS_CTRL_ECAP3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP3_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP3_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP3_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP3_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.315 CONTROLSS_CTRL_ECAP4_HALTEN Register

2.6.2.315.1 CONTROLSS_CTRL_ECAP4_HALTEN Register (Offset = 5E0h) [reset = 0h]

Ecap halt enable.

Return to Summary Table

Table 2-2091. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05E0h

Figure 2-1043. CONTROLSS_CTRL_ECAP4_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ECAP4_HALTEN_CR5B1	ECAP4_HALTEN_CR5A1	ECAP4_HALTEN_CR5B0	ECAP4_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2092. CONTROLSS_CTRL_ECAP4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP4_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP4_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP4_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP4_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.316 CONTROLSS_CTRL_ECAP5_HALTEN Register

2.6.2.316.1 CONTROLSS_CTRL_ECAP5_HALTEN Register (Offset = 5E4h) [reset = 0h]

Ecap halt enable.

Return to Summary Table

Table 2-2093. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05E4h

Figure 2-1044. CONTROLSS_CTRL_ECAP5_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP5_HALTEN_CR5B1	ECAP5_HALTEN_CR5A1	ECAP5_HALTEN_CR5B0	ECAP5_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2094. CONTROLSS_CTRL_ECAP5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP5_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP5_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP5_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP5_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.317 CONTROLSS_CTRL_ECAP6_HALTEN Register

2.6.2.317.1 CONTROLSS_CTRL_ECAP6_HALTEN Register (Offset = 5E8h) [reset = 0h]

Ecap halt enable.

Return to Summary Table

Table 2-2095. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05E8h

Figure 2-1045. CONTROLSS_CTRL_ECAP6_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP6_HALTEN_CR5B1	ECAP6_HALTEN_CR5A1	ECAP6_HALTEN_CR5B0	ECAP6_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2096. CONTROLSS_CTRL_ECAP6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP6_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP6_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP6_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP6_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.318 CONTROLSS_CTRL_ECAP7_HALTEN Register

2.6.2.318.1 CONTROLSS_CTRL_ECAP7_HALTEN Register (Offset = 5ECh) [reset = 0h]

Ecap halt enable.

Return to Summary Table

Table 2-2097. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05ECh

Figure 2-1046. CONTROLSS_CTRL_ECAP7_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP7_HALTEN_CR5B1	ECAP7_HALTEN_CR5A1	ECAP7_HALTEN_CR5B0	ECAP7_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2098. CONTROLSS_CTRL_ECAP7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP7_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP7_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP7_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP7_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.319 CONTROLSS_CTRL_ECAP8_HALTEN Register

2.6.2.319.1 CONTROLSS_CTRL_ECAP8_HALTEN Register (Offset = 5F0h) [reset = 0h]

Ecap halt enable.

Return to Summary Table

Table 2-2099. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05F0h

Figure 2-1047. CONTROLSS_CTRL_ECAP8_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP8_HALTEN_CR5B1	ECAP8_HALTEN_CR5A1	ECAP8_HALTEN_CR5B0	ECAP8_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2100. CONTROLSS_CTRL_ECAP8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP8_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP8_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP8_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP8_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.320 CONTROLSS_CTRL_ECAP9_HALTEN Register

2.6.2.320.1 CONTROLSS_CTRL_ECAP9_HALTEN Register (Offset = 5F4h) [reset = 0h]

Ecap halt enable.

Return to Summary Table

Table 2-2101. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05F4h

Figure 2-1048. CONTROLSS_CTRL_ECAP9_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP9_HALTEN_CR5B1	ECAP9_HALTEN_CR5A1	ECAP9_HALTEN_CR5B0	ECAP9_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2102. CONTROLSS_CTRL_ECAP9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP9_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP9_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP9_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP9_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.321 CONTROLSS_CTRL_EQEP0_HALTEN Register

2.6.2.321.1 CONTROLSS_CTRL_EQEP0_HALTEN Register (Offset = 5F8h) [reset = 0h]

Eqep halt enable.

Return to Summary Table

Table 2-2103. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05F8h

Figure 2-1049. CONTROLSS_CTRL_EQEP0_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EQEP0_HALTEN_CR5B1	EQEP0_HALTEN_CR5A1	EQEP0_HALTEN_CR5B0	EQEP0_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2104. CONTROLSS_CTRL_EQEP0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EQEP0_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EQEP0_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EQEP0_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EQEP0_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.322 CONTROLSS_CTRL_EQEP1_HALTEN Register

2.6.2.322.1 CONTROLSS_CTRL_EQEP1_HALTEN Register (Offset = 5FCh) [reset = 0h]

Eqep halt enable.

Return to Summary Table

Table 2-2105. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 05FCh

Figure 2-1050. CONTROLSS_CTRL_EQEP1_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EQEP1_HALTEN_CR5B1	EQEP1_HALTEN_CR5A1	EQEP1_HALTEN_CR5B0	EQEP1_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2106. CONTROLSS_CTRL_EQEP1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EQEP1_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EQEP1_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EQEP1_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EQEP1_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.323 CONTROLSS_CTRL_EQEP2_HALTEN Register

2.6.2.323.1 CONTROLSS_CTRL_EQEP2_HALTEN Register (Offset = 600h) [reset = 0h]

Eqep halt enable.

Return to Summary Table

Table 2-2107. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0600h

Figure 2-1051. CONTROLSS_CTRL_EQEP2_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				EQEP2_HALTEN_CR5B1	EQEP2_HALTEN_CR5A1	EQEP2_HALTEN_CR5B0	EQEP2_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2108. CONTROLSS_CTRL_EQEP2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EQEP2_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	EQEP2_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	EQEP2_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	EQEP2_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.324 CONTROLSS_CTRL_ECAP10_HALTEN Register

2.6.2.324.1 CONTROLSS_CTRL_ECAP10_HALTEN Register (Offset = 604h) [reset = 0h]

Ecap halt enable.

Return to Summary Table

Table 2-2109. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0604h

Figure 2-1052. CONTROLSS_CTRL_ECAP10_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP10_HALTEN_CR5B1	ECAP10_HALTEN_CR5A1	ECAP10_HALTEN_CR5B0	ECAP10_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2110. CONTROLSS_CTRL_ECAP10_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP10_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP10_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP10_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP10_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.325 CONTROLSS_CTRL_ECAP11_HALTEN Register

2.6.2.325.1 CONTROLSS_CTRL_ECAP11_HALTEN Register (Offset = 608h) [reset = 0h]

Ecap halt enable.

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Table 2-2111. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0608h

Figure 2-1053. CONTROLSS_CTRL_ECAP11_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP11_HALTEN_CR5B1	ECAP11_HALTEN_CR5A1	ECAP11_HALTEN_CR5B0	ECAP11_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2112. CONTROLSS_CTRL_ECAP11_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP11_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP11_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP11_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP11_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.326 CONTROLSS_CTRL_ECAP12_HALTEN Register

2.6.2.326.1 CONTROLSS_CTRL_ECAP12_HALTEN Register (Offset = 60Ch) [reset = 0h]

Ecap halt enable.

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Table 2-2113. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 060Ch

Figure 2-1054. CONTROLSS_CTRL_ECAP12_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ECAP12_HALTEN_CR5B1	ECAP12_HALTEN_CR5A1	ECAP12_HALTEN_CR5B0	ECAP12_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2114. CONTROLSS_CTRL_ECAP12_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP12_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP12_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP12_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP12_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.327 CONTROLSS_CTRL_ECAP13_HALTEN Register

2.6.2.327.1 CONTROLSS_CTRL_ECAP13_HALTEN Register (Offset = 610h) [reset = 0h]

Ecap halt enable.

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Table 2-2115. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0610h

Figure 2-1055. CONTROLSS_CTRL_ECAP13_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP13_HALTEN_CR5B1	ECAP13_HALTEN_CR5A1	ECAP13_HALTEN_CR5B0	ECAP13_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2116. CONTROLSS_CTRL_ECAP13_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP13_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP13_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP13_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP13_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.328 CONTROLSS_CTRL_ECAP14_HALTEN Register

2.6.2.328.1 CONTROLSS_CTRL_ECAP14_HALTEN Register (Offset = 614h) [reset = 0h]

Ecap halt enable.

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Table 2-2117. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0614h

Figure 2-1056. CONTROLSS_CTRL_ECAP14_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ECAP14_HALTEN_CR5B1	ECAP14_HALTEN_CR5A1	ECAP14_HALTEN_CR5B0	ECAP14_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2118. CONTROLSS_CTRL_ECAP14_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP14_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP14_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP14_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP14_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.329 CONTROLSS_CTRL_ECAP15_HALTEN Register

2.6.2.329.1 CONTROLSS_CTRL_ECAP15_HALTEN Register (Offset = 618h) [reset = 0h]

Ecap halt enable.

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Table 2-2119. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 0618h

Figure 2-1057. CONTROLSS_CTRL_ECAP15_HALTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				ECAP15_HALTEN_CR5B1	ECAP15_HALTEN_CR5A1	ECAP15_HALTEN_CR5B0	ECAP15_HALTEN_CR5A0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 2-2120. CONTROLSS_CTRL_ECAP15_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ECAP15_HALTEN_CR5B1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
2	ECAP15_HALTEN_CR5A1	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
1	ECAP15_HALTEN_CR5B0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt
0	ECAP15_HALTEN_CR5A0	R/W	0h	Write 1'b0: IP Halt disabled with corresponding CPU halt Write 1'b1: IP Halt enabled with corresponding CPU halt

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2.6.2.330 CONTROLSS_CTRL_LOCK0_KICK0 Register

2.6.2.330.1 CONTROLSS_CTRL_LOCK0_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component.

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Table 2-2121. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 1008h

Figure 2-1058. CONTROLSS_CTRL_LOCK0_KICK0 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK0							
R/W							
0h							

Table 2-2122. CONTROLSS_CTRL_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK0	R/W	0h	- KICK0 component

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2.6.2.331 CONTROLSS_CTRL_LOCK0_KICK1 Register

2.6.2.331.1 CONTROLSS_CTRL_LOCK0_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component.

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Table 2-2123. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 100Ch

Figure 2-1059. CONTROLSS_CTRL_LOCK0_KICK1 Name Register

31	30	29	28	27	26	25	24
LOCK0_KICK1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOCK0_KICK1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOCK0_KICK1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOCK0_KICK1							
R/W							
0h							

Table 2-2124. CONTROLSS_CTRL_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOCK0_KICK1	R/W	0h	- KICK1 component

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2.6.2.332 CONTROLSS_CTRL_INTR_RAW_STATUS Register

2.6.2.332.1 CONTROLSS_CTRL_INTR_RAW_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register.

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Table 2-2125. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 1010h

Figure 2-1060. CONTROLSS_CTRL_INTR_RAW_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	KICK_ERR	ADDR_ERR	PROT_ERR
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 2-2126. CONTROLSS_CTRL_INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR	R/W1TS	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	R/W1TS	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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2.6.2.333 CONTROLSS_CTRL_INTR_ENABLED_STATUS_CLEAR Register

2.6.2.333.1 CONTROLSS_CTRL_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register.

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Table 2-2127. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 1014h

Figure 2-1061. CONTROLSS_CTRL_INTR_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				ENABLED_PROXY_ERR	ENABLED_KICK_ERR	ENABLED_ADDR_ERR	ENABLED_PROT_ERR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 2-2128. CONTROLSS_CTRL_INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	ENABLED_PROXY_ERR	R/W1TC	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	R/W1TC	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	R/W1TC	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	R/W1TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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2.6.2.334 CONTROLSS_CTRL_INTR_ENABLE Register

2.6.2.334.1 CONTROLSS_CTRL_INTR_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register.

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Table 2-2129. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 1018h

Figure 2-1062. CONTROLSS_CTRL_INTR_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN	KICK_ERR_EN	ADDR_ERR_EN	PROT_ERR_EN
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 2-2130. CONTROLSS_CTRL_INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN	R/W1TS	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	R/W1TS	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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2.6.2.335 CONTROLSS_CTRL_INTR_ENABLE_CLEAR Register

2.6.2.335.1 CONTROLSS_CTRL_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register.

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Table 2-2131. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 101Ch

Figure 2-1063. CONTROLSS_CTRL_INTR_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PROXY_ERR_EN_CLR	KICK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h

Table 2-2132. CONTROLSS_CTRL_INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PROXY_ERR_EN_CLR	R/W1TC	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	R/W1TC	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	R/W1TC	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	R/W1TC	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

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2.6.2.336 CONTROLSS_CTRL_EOI Register

2.6.2.336.1 CONTROLSS_CTRL_EOI Register (Offset = 1020h) [reset = 0h]

EOI register.

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Table 2-2133. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 1020h

Figure 2-1064. CONTROLSS_CTRL_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI_VECTOR							
R/W							
0h							

Table 2-2134. CONTROLSS_CTRL_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI_VECTOR	R/W	0h	EOI vector value. Write this with interrupt distribution value in the chip.

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2.6.2.337 CONTROLSS_CTRL_FAULT_ADDRESS Register

2.6.2.337.1 CONTROLSS_CTRL_FAULT_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register.

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Table 2-2135. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 1024h

Figure 2-1065. CONTROLSS_CTRL_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 2-2136. CONTROLSS_CTRL_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault Address.

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2.6.2.338 CONTROLSS_CTRL_FAULT_TYPE_STATUS Register

2.6.2.338.1 CONTROLSS_CTRL_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register.

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Table 2-2137. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 1028h

Figure 2-1066. CONTROLSS_CTRL_FAULT_TYPE_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	FAULT_NS	FAULT_TYPE					
NONE	R	R					
0h	0h	0h					

Table 2-2138. CONTROLSS_CTRL_FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	FAULT_NS	R	0h	Non-secure access.
5:0	FAULT_TYPE	R	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

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2.6.2.339 CONTROLSS_CTRL_FAULT_ATTR_STATUS Register

2.6.2.339.1 CONTROLSS_CTRL_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register.

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Table 2-2139. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 102Ch

Figure 2-1067. CONTROLSS_CTRL_FAULT_ATTR_STATUS Name Register

31	30	29	28	27	26	25	24
FAULT_XID							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FAULT_XID				FAULT_ROUTEID			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FAULT_ROUTEID							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FAULT_PRIVID							
R							
0h							

Table 2-2140. CONTROLSS_CTRL_FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	FAULT_XID	R	0h	XID.
19:8	FAULT_ROUTEID	R	0h	Route ID.
7:0	FAULT_PRIVID	R	0h	Privilege ID.

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2.6.2.340 CONTROLSS_CTRL_FAULT_CLEAR Register

2.6.2.340.1 CONTROLSS_CTRL_FAULT_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register.

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Table 2-2141. Instance Table

Instance Name	Physical Address
CONTROLSS_GLOBAL_CTRL	502F 1030h

Figure 2-1068. CONTROLSS_CTRL_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
NONE							W
0h							0h

Table 2-2142. CONTROLSS_CTRL_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

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2.7 MSS_IOMUX

MSS_IOMUX

2.7.1 MSS_IOMUX Summaries

MSS_IOMUX Summaries

Table 2-2143. IOMUX Registers, Base Address=5310 0000h, Length=4096

Offset	Length	Register Name	MSS_IOMUX Physical Address
0h	32	IOMUX_QSPI0_CSN0_CFG_REG	5310 0000h
4h	32	IOMUX_QSPI0_CSN1_CFG_REG	5310 0004h
8h	32	IOMUX_QSPI0_CLK_CFG_REG	5310 0008h
Ch	32	IOMUX_QSPI0_D0_CFG_REG	5310 000Ch
10h	32	IOMUX_QSPI0_D1_CFG_REG	5310 0010h
14h	32	IOMUX_QSPI0_D2_CFG_REG	5310 0014h
18h	32	IOMUX_QSPI0_D3_CFG_REG	5310 0018h
1Ch	32	IOMUX_MCAN0_RX_CFG_REG	5310 001Ch
20h	32	IOMUX_MCAN0_TX_CFG_REG	5310 0020h
24h	32	IOMUX_MCAN1_RX_CFG_REG	5310 0024h
28h	32	IOMUX_MCAN1_TX_CFG_REG	5310 0028h
2Ch	32	IOMUX_SPI0_CS0_CFG_REG	5310 002Ch
30h	32	IOMUX_SPI0_CLK_CFG_REG	5310 0030h
34h	32	IOMUX_SPI0_D0_CFG_REG	5310 0034h
38h	32	IOMUX_SPI0_D1_CFG_REG	5310 0038h
3Ch	32	IOMUX_SPI1_CS0_CFG_REG	5310 003Ch
40h	32	IOMUX_SPI1_CLK_CFG_REG	5310 0040h
44h	32	IOMUX_SPI1_D0_CFG_REG	5310 0044h
48h	32	IOMUX_SPI1_D1_CFG_REG	5310 0048h
4Ch	32	IOMUX_LIN1_RXD_CFG_REG	5310 004Ch
50h	32	IOMUX_LIN1_TXD_CFG_REG	5310 0050h
54h	32	IOMUX_LIN2_RXD_CFG_REG	5310 0054h
58h	32	IOMUX_LIN2_TXD_CFG_REG	5310 0058h
5Ch	32	IOMUX_I2C1_SCL_CFG_REG	5310 005Ch
60h	32	IOMUX_I2C1_SDA_CFG_REG	5310 0060h
64h	32	IOMUX_UART0_RTSN_CFG_REG	5310 0064h
68h	32	IOMUX_UART0_CTSN_CFG_REG	5310 0068h
6Ch	32	IOMUX_UART0_RXD_CFG_REG	5310 006Ch
70h	32	IOMUX_UART0_TXD_CFG_REG	5310 0070h
74h	32	IOMUX_RGMII1_RXC_CFG_REG	5310 0074h
78h	32	IOMUX_RGMII1_RX_CTL_CFG_REG	5310 0078h
7Ch	32	IOMUX_RGMII1_RD0_CFG_REG	5310 007Ch
80h	32	IOMUX_RGMII1_RD1_CFG_REG	5310 0080h
84h	32	IOMUX_RGMII1_RD2_CFG_REG	5310 0084h
88h	32	IOMUX_RGMII1_RD3_CFG_REG	5310 0088h
8Ch	32	IOMUX_RGMII1_TXC_CFG_REG	5310 008Ch
90h	32	IOMUX_RGMII1_TX_CTL_CFG_REG	5310 0090h
94h	32	IOMUX_RGMII1_TD0_CFG_REG	5310 0094h
98h	32	IOMUX_RGMII1_TD1_CFG_REG	5310 0098h
9Ch	32	IOMUX_RGMII1_TD2_CFG_REG	5310 009Ch

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Table 2-2143. IOMUX Registers, Base Address=5310 0000h, Length=4096 (continued)

Offset	Length	Register Name	MSS_IOMUX Physical Address
A0h	32	IOMUX_RGMII1_TD3_CFG_REG	5310 00A0h
A4h	32	IOMUX_MDIO0_MDIO_CFG_REG	5310 00A4h
A8h	32	IOMUX_MDIO0_MDC_CFG_REG	5310 00A8h
ACh	32	IOMUX_EPWM0_A_CFG_REG	5310 00ACh
B0h	32	IOMUX_EPWM0_B_CFG_REG	5310 00B0h
B4h	32	IOMUX_EPWM1_A_CFG_REG	5310 00B4h
B8h	32	IOMUX_EPWM1_B_CFG_REG	5310 00B8h
BCh	32	IOMUX_EPWM2_A_CFG_REG	5310 00BCh
C0h	32	IOMUX_EPWM2_B_CFG_REG	5310 00C0h
C4h	32	IOMUX_EPWM3_A_CFG_REG	5310 00C4h
C8h	32	IOMUX_EPWM3_B_CFG_REG	5310 00C8h
CCh	32	IOMUX_EPWM4_A_CFG_REG	5310 00CCh
D0h	32	IOMUX_EPWM4_B_CFG_REG	5310 00D0h
D4h	32	IOMUX_EPWM5_A_CFG_REG	5310 00D4h
D8h	32	IOMUX_EPWM5_B_CFG_REG	5310 00D8h
DCh	32	IOMUX_EPWM6_A_CFG_REG	5310 00DCh
E0h	32	IOMUX_EPWM6_B_CFG_REG	5310 00E0h
E4h	32	IOMUX_EPWM7_A_CFG_REG	5310 00E4h
E8h	32	IOMUX_EPWM7_B_CFG_REG	5310 00E8h
ECh	32	IOMUX_EPWM8_A_CFG_REG	5310 00ECh
F0h	32	IOMUX_EPWM8_B_CFG_REG	5310 00F0h
F4h	32	IOMUX_EPWM9_A_CFG_REG	5310 00F4h
F8h	32	IOMUX_EPWM9_B_CFG_REG	5310 00F8h
FCh	32	IOMUX_EPWM10_A_CFG_REG	5310 00FCh
100h	32	IOMUX_EPWM10_B_CFG_REG	5310 0100h
104h	32	IOMUX_EPWM11_A_CFG_REG	5310 0104h
108h	32	IOMUX_EPWM11_B_CFG_REG	5310 0108h
10Ch	32	IOMUX_EPWM12_A_CFG_REG	5310 010Ch
110h	32	IOMUX_EPWM12_B_CFG_REG	5310 0110h
114h	32	IOMUX_EPWM13_A_CFG_REG	5310 0114h
118h	32	IOMUX_EPWM13_B_CFG_REG	5310 0118h
11Ch	32	IOMUX_EPWM14_A_CFG_REG	5310 011Ch
120h	32	IOMUX_EPWM14_B_CFG_REG	5310 0120h
124h	32	IOMUX_EPWM15_A_CFG_REG	5310 0124h
128h	32	IOMUX_EPWM15_B_CFG_REG	5310 0128h
12Ch	32	IOMUX_UART1_RXD_CFG_REG	5310 012Ch
130h	32	IOMUX_UART1_TXD_CFG_REG	5310 0130h
134h	32	IOMUX_MMC0_CLK_CFG_REG	5310 0134h
138h	32	IOMUX_MMC0_CMD_CFG_REG	5310 0138h
13Ch	32	IOMUX_MMC0_D0_CFG_REG	5310 013Ch
140h	32	IOMUX_MMC0_D1_CFG_REG	5310 0140h
144h	32	IOMUX_MMC0_D2_CFG_REG	5310 0144h
148h	32	IOMUX_MMC0_D3_CFG_REG	5310 0148h
14Ch	32	IOMUX_MMC0_WP_CFG_REG	5310 014Ch
150h	32	IOMUX_MMC0_CD_CFG_REG	5310 0150h
154h	32	IOMUX_PR0_MDIO0_MDIO_CFG_REG	5310 0154h
158h	32	IOMUX_PR0_MDIO0_MDC_CFG_REG	5310 0158h

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Table 2-2143. IOMUX Registers, Base Address=5310 0000h, Length=4096 (continued)

Offset	Length	Register Name	MSS_IOMUX Physical Address
15Ch	32	IOMUX_PR0_PRU0_GPO5_CFG_REG	5310 015Ch
160h	32	IOMUX_PR0_PRU0_GPO9_CFG_REG	5310 0160h
164h	32	IOMUX_PR0_PRU0_GPO10_CFG_REG	5310 0164h
168h	32	IOMUX_PR0_PRU0_GPO8_CFG_REG	5310 0168h
16Ch	32	IOMUX_PR0_PRU0_GPO6_CFG_REG	5310 016Ch
170h	32	IOMUX_PR0_PRU0_GPO4_CFG_REG	5310 0170h
174h	32	IOMUX_PR0_PRU0_GPO0_CFG_REG	5310 0174h
178h	32	IOMUX_PR0_PRU0_GPO1_CFG_REG	5310 0178h
17Ch	32	IOMUX_PR0_PRU0_GPO2_CFG_REG	5310 017Ch
180h	32	IOMUX_PR0_PRU0_GPO3_CFG_REG	5310 0180h
184h	32	IOMUX_PR0_PRU0_GPO16_CFG_REG	5310 0184h
188h	32	IOMUX_PR0_PRU0_GPO15_CFG_REG	5310 0188h
18Ch	32	IOMUX_PR0_PRU0_GPO11_CFG_REG	5310 018Ch
190h	32	IOMUX_PR0_PRU0_GPO12_CFG_REG	5310 0190h
194h	32	IOMUX_PR0_PRU0_GPO13_CFG_REG	5310 0194h
198h	32	IOMUX_PR0_PRU0_GPO14_CFG_REG	5310 0198h
19Ch	32	IOMUX_PR0_PRU1_GPO5_CFG_REG	5310 019Ch
1A0h	32	IOMUX_PR0_PRU1_GPO9_CFG_REG	5310 01A0h
1A4h	32	IOMUX_PR0_PRU1_GPO10_CFG_REG	5310 01A4h
1A8h	32	IOMUX_PR0_PRU1_GPO8_CFG_REG	5310 01A8h
1ACh	32	IOMUX_PR0_PRU1_GPO6_CFG_REG	5310 01ACh
1B0h	32	IOMUX_PR0_PRU1_GPO4_CFG_REG	5310 01B0h
1B4h	32	IOMUX_PR0_PRU1_GPO0_CFG_REG	5310 01B4h
1B8h	32	IOMUX_PR0_PRU1_GPO1_CFG_REG	5310 01B8h
1BCh	32	IOMUX_PR0_PRU1_GPO2_CFG_REG	5310 01BCh
1C0h	32	IOMUX_PR0_PRU1_GPO3_CFG_REG	5310 01C0h
1C4h	32	IOMUX_PR0_PRU1_GPO16_CFG_REG	5310 01C4h
1C8h	32	IOMUX_PR0_PRU1_GPO15_CFG_REG	5310 01C8h
1CCh	32	IOMUX_PR0_PRU1_GPO11_CFG_REG	5310 01CCh
1D0h	32	IOMUX_PR0_PRU1_GPO12_CFG_REG	5310 01D0h
1D4h	32	IOMUX_PR0_PRU1_GPO13_CFG_REG	5310 01D4h
1D8h	32	IOMUX_PR0_PRU1_GPO14_CFG_REG	5310 01D8h
1DCh	32	IOMUX_PR0_PRU1_GPO19_CFG_REG	5310 01DCh
1E0h	32	IOMUX_PR0_PRU1_GPO18_CFG_REG	5310 01E0h
1E4h	32	IOMUX_EXT_REFCLK0_CFG_REG	5310 01E4h
1E8h	32	IOMUX_SDFM0_CLK0_CFG_REG	5310 01E8h
1ECh	32	IOMUX_SDFM0_D0_CFG_REG	5310 01ECh
1F0h	32	IOMUX_SDFM0_CLK1_CFG_REG	5310 01F0h
1F4h	32	IOMUX_SDFM0_D1_CFG_REG	5310 01F4h
1F8h	32	IOMUX_SDFM0_CLK2_CFG_REG	5310 01F8h
1FCh	32	IOMUX_SDFM0_D2_CFG_REG	5310 01FCh
200h	32	IOMUX_SDFM0_CLK3_CFG_REG	5310 0200h
204h	32	IOMUX_SDFM0_D3_CFG_REG	5310 0204h
208h	32	IOMUX_EQEP0_A_CFG_REG	5310 0208h
20Ch	32	IOMUX_EQEP0_B_CFG_REG	5310 020Ch
210h	32	IOMUX_EQEP0_STROBE_CFG_REG	5310 0210h
214h	32	IOMUX_EQEP0_INDEX_CFG_REG	5310 0214h

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Table 2-2143. IOMUX Registers, Base Address=5310 0000h, Length=4096 (continued)

Offset	Length	Register Name	MSS_IOMUX Physical Address
218h	32	IOMUX_I2C0_SDA_CFG_REG	5310 0218h
21Ch	32	IOMUX_I2C0_SCL_CFG_REG	5310 021Ch
220h	32	IOMUX_MCAN2_TX_CFG_REG	5310 0220h
224h	32	IOMUX_MCAN2_RX_CFG_REG	5310 0224h
228h	32	IOMUX_CLKOUT0_CFG_REG	5310 0228h
22Ch	32	IOMUX_WARMRSTN_CFG_REG	5310 022Ch
230h	32	IOMUX_SAFETY_ERRORN_CFG_REG	5310 0230h
234h	32	IOMUX_TDI_CFG_REG	5310 0234h
238h	32	IOMUX_TDO_CFG_REG	5310 0238h
23Ch	32	IOMUX_TMS_CFG_REG	5310 023Ch
240h	32	IOMUX_TCK_CFG_REG	5310 0240h
244h	32	IOMUX_OSPI0_CLKLB_CFG_REG	5310 0244h
248h	32	IOMUX_QUAL_GRP_0_CFG_REG	5310 0248h
24Ch	32	IOMUX_QUAL_GRP_1_CFG_REG	5310 024Ch
250h	32	IOMUX_QUAL_GRP_2_CFG_REG	5310 0250h
254h	32	IOMUX_QUAL_GRP_3_CFG_REG	5310 0254h
258h	32	IOMUX_QUAL_GRP_4_CFG_REG	5310 0258h
25Ch	32	IOMUX_QUAL_GRP_5_CFG_REG	5310 025Ch
260h	32	IOMUX_QUAL_GRP_6_CFG_REG	5310 0260h
264h	32	IOMUX_QUAL_GRP_7_CFG_REG	5310 0264h
268h	32	IOMUX_QUAL_GRP_8_CFG_REG	5310 0268h
26Ch	32	IOMUX_QUAL_GRP_9_CFG_REG	5310 026Ch
270h	32	IOMUX_QUAL_GRP_10_CFG_REG	5310 0270h
274h	32	IOMUX_QUAL_GRP_11_CFG_REG	5310 0274h
278h	32	IOMUX_QUAL_GRP_12_CFG_REG	5310 0278h
27Ch	32	IOMUX_QUAL_GRP_13_CFG_REG	5310 027Ch
280h	32	IOMUX_QUAL_GRP_14_CFG_REG	5310 0280h
284h	32	IOMUX_QUAL_GRP_15_CFG_REG	5310 0284h
288h	32	IOMUX_QUAL_GRP_16_CFG_REG	5310 0288h
28Ch	32	IOMUX_QUAL_GRP_17_CFG_REG	5310 028Ch
290h	32	IOMUX_USER_MODE_EN	5310 0290h
294h	32	IOMUX_PADGLBL_CFG_REG	5310 0294h
298h	32	IOMUX_IO_CFG_KICK0	5310 0298h
29Ch	32	IOMUX_IO_CFG_KICK1	5310 029Ch

2.7.2 MSS_IOMUX Registers

MSS_IOMUX Registers

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2.7.2.1 IOMUX_QSPI0_CSN0_CFG_REG Register

2.7.2.1.1 IOMUX_QSPI0_CSN0_CFG_REG Register (Offset = 0h) [reset = 5F7h]

QSPI0_CSn0 IO config register.

Return to Summary Table

Table 2-2144. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0000h

Figure 2-1069. IOMUX_QSPI0_CSN0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2145. IOMUX_QSPI0_CSN0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2145. IOMUX_QSPI0_CSN0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.2 IOMUX_QSPI0_CSN1_CFG_REG Register

2.7.2.2.1 IOMUX_QSPI0_CSN1_CFG_REG Register (Offset = 4h) [reset = 5F7h]

QSPI0_CSn1 IO config register.

Return to Summary Table

Table 2-2146. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0004h

Figure 2-1070. IOMUX_QSPI0_CSN1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2147. IOMUX_QSPI0_CSN1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2147. IOMUX_QSPI0_CSN1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.3 IOMUX_QSPI0_CLK_CFG_REG Register

2.7.2.3.1 IOMUX_QSPI0_CLK_CFG_REG Register (Offset = 8h) [reset = 5F7h]

QSPI0_CLK IO config register.

Return to Summary Table

Table 2-2148. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0008h

Figure 2-1071. IOMUX_QSPI0_CLK_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2149. IOMUX_QSPI0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2149. IOMUX_QSPI0_CLK_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.4 IOMUX_QSPI0_D0_CFG_REG Register

2.7.2.4.1 IOMUX_QSPI0_D0_CFG_REG Register (Offset = Ch) [reset = 5D7h]

QSPI0_D0 IO config register.

Return to Summary Table

Table 2-2150. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 000Ch

Figure 2-1072. IOMUX_QSPI0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	0h	1h	7h			

Table 2-2151. IOMUX_QSPI0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2151. IOMUX_QSPI0_D0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	0h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.5 IOMUX_QSPI0_D1_CFG_REG Register

2.7.2.5.1 IOMUX_QSPI0_D1_CFG_REG Register (Offset = 10h) [reset = 5D7h]

QSPI0_D1 IO config register.

Return to Summary Table

Table 2-2152. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0010h

Figure 2-1073. IOMUX_QSPI0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	0h	1h	7h			

Table 2-2153. IOMUX_QSPI0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2153. IOMUX_QSPI0_D1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	0h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.6 IOMUX_QSPI0_D2_CFG_REG Register

2.7.2.6.1 IOMUX_QSPI0_D2_CFG_REG Register (Offset = 14h) [reset = 5F7h]

QSPI0_D2 IO config register.

Return to Summary Table

Table 2-2154. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0014h

Figure 2-1074. IOMUX_QSPI0_D2_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2155. IOMUX_QSPI0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2155. IOMUX_QSPI0_D2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.7 IOMUX_QSPI0_D3_CFG_REG Register

2.7.2.7.1 IOMUX_QSPI0_D3_CFG_REG Register (Offset = 18h) [reset = 5F7h]

QSPI0_D3 IO config register.

Return to Summary Table

Table 2-2156. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0018h

Figure 2-1075. IOMUX_QSPI0_D3_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2157. IOMUX_QSPI0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2157. IOMUX_QSPI0_D3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.8 IOMUX_MCAN0_RX_CFG_REG Register

2.7.2.8.1 IOMUX_MCAN0_RX_CFG_REG Register (Offset = 1Ch) [reset = 5F7h]

MCAN0_RX IO config register.

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Table 2-2158. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 001Ch

Figure 2-1076. IOMUX_MCAN0_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2159. IOMUX_MCAN0_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2159. IOMUX_MCAN0_RX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.9 IOMUX_MCAN0_TX_CFG_REG Register

2.7.2.9.1 IOMUX_MCAN0_TX_CFG_REG Register (Offset = 20h) [reset = 5F7h]

MCAN0_TX IO config register.

Return to Summary Table

Table 2-2160. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0020h

Figure 2-1077. IOMUX_MCAN0_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2161. IOMUX_MCAN0_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2161. IOMUX_MCAN0_TX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.10 IOMUX_MCAN1_RX_CFG_REG Register

2.7.2.10.1 IOMUX_MCAN1_RX_CFG_REG Register (Offset = 24h) [reset = 5F7h]

MCAN1_RX IO config register.

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Table 2-2162. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0024h

Figure 2-1078. IOMUX_MCAN1_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2163. IOMUX_MCAN1_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2163. IOMUX_MCAN1_RX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.11 IOMUX_MCAN1_TX_CFG_REG Register

2.7.2.11.1 IOMUX_MCAN1_TX_CFG_REG Register (Offset = 28h) [reset = 5F7h]

MCAN1_TX IO config register.

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Table 2-2164. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0028h

Figure 2-1079. IOMUX_MCAN1_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2165. IOMUX_MCAN1_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2165. IOMUX_MCAN1_TX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.12 IOMUX_SPI0_CS0_CFG_REG Register

2.7.2.12.1 IOMUX_SPI0_CS0_CFG_REG Register (Offset = 2Ch) [reset = 5F7h]

SPI0_CS0 IO config register.

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Table 2-2166. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 002Ch

Figure 2-1080. IOMUX_SPI0_CS0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2167. IOMUX_SPI0_CS0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2167. IOMUX_SPI0_CS0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.13 IOMUX_SPI0_CLK_CFG_REG Register

2.7.2.13.1 IOMUX_SPI0_CLK_CFG_REG Register (Offset = 30h) [reset = 5D7h]

SPI0_CLK IO config register.

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Table 2-2168. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0030h

Figure 2-1081. IOMUX_SPI0_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	0h	1h	7h			

Table 2-2169. IOMUX_SPI0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2169. IOMUX_SPI0_CLK_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	0h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.14 IOMUX_SPI0_D0_CFG_REG Register

2.7.2.14.1 IOMUX_SPI0_D0_CFG_REG Register (Offset = 34h) [reset = 5D7h]

SPI0_D0 IO config register.

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Table 2-2170. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0034h

Figure 2-1082. IOMUX_SPI0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	0h	1h	7h			

Table 2-2171. IOMUX_SPI0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2171. IOMUX_SPI0_D0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	0h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.15 IOMUX_SPI0_D1_CFG_REG Register

2.7.2.15.1 IOMUX_SPI0_D1_CFG_REG Register (Offset = 38h) [reset = 5F7h]

SPI0_D1 IO config register.

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Table 2-2172. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0038h

Figure 2-1083. IOMUX_SPI0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2173. IOMUX_SPI0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2173. IOMUX_SPI0_D1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.16 IOMUX_SPI1_CS0_CFG_REG Register

2.7.2.16.1 IOMUX_SPI1_CS0_CFG_REG Register (Offset = 3Ch) [reset = 5F7h]

SPI1_CS0 IO config register.

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Table 2-2174. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 003Ch

Figure 2-1084. IOMUX_SPI1_CS0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2175. IOMUX_SPI1_CS0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2175. IOMUX_SPI1_CS0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.17 IOMUX_SPI1_CLK_CFG_REG Register

2.7.2.17.1 IOMUX_SPI1_CLK_CFG_REG Register (Offset = 40h) [reset = 5F7h]

SPI1_CLK IO config register.

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Table 2-2176. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0040h

Figure 2-1085. IOMUX_SPI1_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2177. IOMUX_SPI1_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2177. IOMUX_SPI1_CLK_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.18 IOMUX_SPI1_D0_CFG_REG Register

2.7.2.18.1 IOMUX_SPI1_D0_CFG_REG Register (Offset = 44h) [reset = 5F7h]

SPI1_D0 IO config register.

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Table 2-2178. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0044h

Figure 2-1086. IOMUX_SPI1_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2179. IOMUX_SPI1_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2179. IOMUX_SPI1_D0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.19 IOMUX_SPI1_D1_CFG_REG Register

2.7.2.19.1 IOMUX_SPI1_D1_CFG_REG Register (Offset = 48h) [reset = 5F7h]

SPI1_D1 IO config register.

Return to Summary Table

Table 2-2180. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0048h

Figure 2-1087. IOMUX_SPI1_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2181. IOMUX_SPI1_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2181. IOMUX_SPI1_D1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.20 IOMUX_LIN1_RXD_CFG_REG Register

2.7.2.20.1 IOMUX_LIN1_RXD_CFG_REG Register (Offset = 4Ch) [reset = 5F7h]

LIN1_RXD IO config register.

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Table 2-2182. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 004Ch

Figure 2-1088. IOMUX_LIN1_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2183. IOMUX_LIN1_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2183. IOMUX_LIN1_RXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.21 IOMUX_LIN1_TXD_CFG_REG Register

2.7.2.21.1 IOMUX_LIN1_TXD_CFG_REG Register (Offset = 50h) [reset = 5F7h]

LIN1_TXD IO config register.

Return to Summary Table

Table 2-2184. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0050h

Figure 2-1089. IOMUX_LIN1_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2185. IOMUX_LIN1_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2185. IOMUX_LIN1_TXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.22 IOMUX_LIN2_RXD_CFG_REG Register

2.7.2.22.1 IOMUX_LIN2_RXD_CFG_REG Register (Offset = 54h) [reset = 5F7h]

LIN2_RXD IO config register.

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Table 2-2186. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0054h

Figure 2-1090. IOMUX_LIN2_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2187. IOMUX_LIN2_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2187. IOMUX_LIN2_RXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.23 IOMUX_LIN2_TXD_CFG_REG Register

2.7.2.23.1 IOMUX_LIN2_TXD_CFG_REG Register (Offset = 58h) [reset = 5F7h]

LIN2_TXD IO config register.

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Table 2-2188. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0058h

Figure 2-1091. IOMUX_LIN2_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2189. IOMUX_LIN2_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2189. IOMUX_LIN2_TXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.24 IOMUX_I2C1_SCL_CFG_REG Register

2.7.2.24.1 IOMUX_I2C1_SCL_CFG_REG Register (Offset = 5Ch) [reset = 5F7h]

I2C1_SCL IO config register.

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Table 2-2190. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 005Ch

Figure 2-1092. IOMUX_I2C1_SCL_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2191. IOMUX_I2C1_SCL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2191. IOMUX_I2C1_SCL_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.25 IOMUX_I2C1_SDA_CFG_REG Register

2.7.2.25.1 IOMUX_I2C1_SDA_CFG_REG Register (Offset = 60h) [reset = 5F7h]

I2C1_SDA IO config register.

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Table 2-2192. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0060h

Figure 2-1093. IOMUX_I2C1_SDA_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2193. IOMUX_I2C1_SDA_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2193. IOMUX_I2C1_SDA_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.26 IOMUX_UART0_RTSN_CFG_REG Register

2.7.2.26.1 IOMUX_UART0_RTSN_CFG_REG Register (Offset = 64h) [reset = 5F7h]

UART0_RTSn IO config register.

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Table 2-2194. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0064h

Figure 2-1094. IOMUX_UART0_RTSN_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2195. IOMUX_UART0_RTSN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2195. IOMUX_UART0_RTSN_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.27 IOMUX_UART0_CTSN_CFG_REG Register

2.7.2.27.1 IOMUX_UART0_CTSN_CFG_REG Register (Offset = 68h) [reset = 5F7h]

UART0_CTSn IO config register.

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Table 2-2196. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0068h

Figure 2-1095. IOMUX_UART0_CTSN_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2197. IOMUX_UART0_CTSN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2197. IOMUX_UART0_CTSN_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.28 IOMUX_UART0_RXD_CFG_REG Register

2.7.2.28.1 IOMUX_UART0_RXD_CFG_REG Register (Offset = 6Ch) [reset = 5F7h]

UART0_RXD IO config register.

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Table 2-2198. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 006Ch

Figure 2-1096. IOMUX_UART0_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2199. IOMUX_UART0_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2199. IOMUX_UART0_RXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.29 IOMUX_UART0_TXD_CFG_REG Register

2.7.2.29.1 IOMUX_UART0_TXD_CFG_REG Register (Offset = 70h) [reset = 5F7h]

UART0_TXD IO config register.

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Table 2-2200. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0070h

Figure 2-1097. IOMUX_UART0_TXD_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2201. IOMUX_UART0_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2201. IOMUX_UART0_TXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.30 IOMUX_RGMII1_RXC_CFG_REG Register

2.7.2.30.1 IOMUX_RGMII1_RXC_CFG_REG Register (Offset = 74h) [reset = 5F7h]

RGMII1_RXC IO config register.

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Table 2-2202. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0074h

Figure 2-1098. IOMUX_RGMII1_RXC_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2203. IOMUX_RGMII1_RXC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2203. IOMUX_RGMII1_RXC_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.31 IOMUX_RGMII1_RX_CTL_CFG_REG Register

2.7.2.31.1 IOMUX_RGMII1_RX_CTL_CFG_REG Register (Offset = 78h) [reset = 5F7h]

RGMII1_RX_CTL IO config register.

Return to Summary Table

Table 2-2204. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0078h

Figure 2-1099. IOMUX_RGMII1_RX_CTL_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2205. IOMUX_RGMII1_RX_CTL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2205. IOMUX_RGMII1_RX_CTL_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.32 IOMUX_RGMII1_RD0_CFG_REG Register

2.7.2.32.1 IOMUX_RGMII1_RD0_CFG_REG Register (Offset = 7Ch) [reset = 5F7h]

RGMII1_RD0 IO config register.

Return to Summary Table

Table 2-2206. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 007Ch

Figure 2-1100. IOMUX_RGMII1_RD0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2207. IOMUX_RGMII1_RD0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2207. IOMUX_RGMII1_RD0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.33 IOMUX_RGMII1_RD1_CFG_REG Register

2.7.2.33.1 IOMUX_RGMII1_RD1_CFG_REG Register (Offset = 80h) [reset = 5F7h]

RGMII1_RD1 IO config register.

Return to Summary Table

Table 2-2208. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0080h

Figure 2-1101. IOMUX_RGMII1_RD1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2209. IOMUX_RGMII1_RD1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2209. IOMUX_RGMII1_RD1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.34 IOMUX_RGMII1_RD2_CFG_REG Register

2.7.2.34.1 IOMUX_RGMII1_RD2_CFG_REG Register (Offset = 84h) [reset = 5F7h]

RGMII1_RD2 IO config register.

Return to Summary Table

Table 2-2210. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0084h

Figure 2-1102. IOMUX_RGMII1_RD2_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2211. IOMUX_RGMII1_RD2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2211. IOMUX_RGMII1_RD2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.35 IOMUX_RGMII1_RD3_CFG_REG Register

2.7.2.35.1 IOMUX_RGMII1_RD3_CFG_REG Register (Offset = 88h) [reset = 5F7h]

RGMII1_RD3 IO config register.

Return to Summary Table

Table 2-2212. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0088h

Figure 2-1103. IOMUX_RGMII1_RD3_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2213. IOMUX_RGMII1_RD3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2213. IOMUX_RGMII1_RD3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.36 IOMUX_RGMII1_TXC_CFG_REG Register

2.7.2.36.1 IOMUX_RGMII1_TXC_CFG_REG Register (Offset = 8Ch) [reset = 5F7h]

RGMII1_TXC IO config register.

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Table 2-2214. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 008Ch

Figure 2-1104. IOMUX_RGMII1_TXC_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2215. IOMUX_RGMII1_TXC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2215. IOMUX_RGMII1_TXC_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.37 IOMUX_RGMII1_TX_CTL_CFG_REG Register

2.7.2.37.1 IOMUX_RGMII1_TX_CTL_CFG_REG Register (Offset = 90h) [reset = 5F7h]

RGMII1_TX_CTL IO config register.

Return to Summary Table

Table 2-2216. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0090h

Figure 2-1105. IOMUX_RGMII1_TX_CTL_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2217. IOMUX_RGMII1_TX_CTL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2217. IOMUX_RGMII1_TX_CTL_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.38 IOMUX_RGMII1_TD0_CFG_REG Register

2.7.2.38.1 IOMUX_RGMII1_TD0_CFG_REG Register (Offset = 94h) [reset = 5F7h]

RGMII1_TD0 IO config register.

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Table 2-2218. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0094h

Figure 2-1106. IOMUX_RGMII1_TD0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2219. IOMUX_RGMII1_TD0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2219. IOMUX_RGMII1_TD0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.39 IOMUX_RGMII1_TD1_CFG_REG Register

2.7.2.39.1 IOMUX_RGMII1_TD1_CFG_REG Register (Offset = 98h) [reset = 5F7h]

RGMII1_TD1 IO config register.

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Table 2-2220. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0098h

Figure 2-1107. IOMUX_RGMII1_TD1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2221. IOMUX_RGMII1_TD1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2221. IOMUX_RGMII1_TD1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.40 IOMUX_RGMII1_TD2_CFG_REG Register

2.7.2.40.1 IOMUX_RGMII1_TD2_CFG_REG Register (Offset = 9Ch) [reset = 5F7h]

RGMII1_TD2 IO config register.

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Table 2-2222. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 009Ch

Figure 2-1108. IOMUX_RGMII1_TD2_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2223. IOMUX_RGMII1_TD2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2223. IOMUX_RGMII1_TD2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.41 IOMUX_RGMII1_TD3_CFG_REG Register

2.7.2.41.1 IOMUX_RGMII1_TD3_CFG_REG Register (Offset = A0h) [reset = 5F7h]

RGMII1_TD3 IO config register.

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Table 2-2224. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00A0h

Figure 2-1109. IOMUX_RGMII1_TD3_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2225. IOMUX_RGMII1_TD3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2225. IOMUX_RGMII1_TD3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.42 IOMUX_MDIO0_MDIO_CFG_REG Register

2.7.2.42.1 IOMUX_MDIO0_MDIO_CFG_REG Register (Offset = A4h) [reset = 5F7h]

MDIO0_MDIO IO config register.

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Table 2-2226. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00A4h

Figure 2-1110. IOMUX_MDIO0_MDIO_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2227. IOMUX_MDIO0_MDIO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2227. IOMUX_MDIO0_MDIO_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.43 IOMUX_MDIO0_MDC_CFG_REG Register

2.7.2.43.1 IOMUX_MDIO0_MDC_CFG_REG Register (Offset = A8h) [reset = 5F7h]

MDIO0_MDC IO config register.

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Table 2-2228. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00A8h

Figure 2-1111. IOMUX_MDIO0_MDC_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2229. IOMUX_MDIO0_MDC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2229. IOMUX_MDIO0_MDC_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.44 IOMUX_EPWM0_A_CFG_REG Register

2.7.2.44.1 IOMUX_EPWM0_A_CFG_REG Register (Offset = ACh) [reset = 5F7h]

EPWM0_A IO config register.

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Table 2-2230. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00ACh

Figure 2-1112. IOMUX_EPWM0_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2231. IOMUX_EPWM0_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2231. IOMUX_EPWM0_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.45 IOMUX_EPWM0_B_CFG_REG Register

2.7.2.45.1 IOMUX_EPWM0_B_CFG_REG Register (Offset = B0h) [reset = 5F7h]

EPWM0_B IO config register.

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Table 2-2232. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00B0h

Figure 2-1113. IOMUX_EPWM0_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2233. IOMUX_EPWM0_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2233. IOMUX_EPWM0_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.46 IOMUX_EPWM1_A_CFG_REG Register

2.7.2.46.1 IOMUX_EPWM1_A_CFG_REG Register (Offset = B4h) [reset = 5F7h]

EPWM1_A IO config register.

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Table 2-2234. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00B4h

Figure 2-1114. IOMUX_EPWM1_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2235. IOMUX_EPWM1_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2235. IOMUX_EPWM1_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.47 IOMUX_EPWM1_B_CFG_REG Register

2.7.2.47.1 IOMUX_EPWM1_B_CFG_REG Register (Offset = B8h) [reset = 5F7h]

EPWM1_B IO config register.

Return to Summary Table

Table 2-2236. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00B8h

Figure 2-1115. IOMUX_EPWM1_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2237. IOMUX_EPWM1_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2237. IOMUX_EPWM1_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.48 IOMUX_EPWM2_A_CFG_REG Register

2.7.2.48.1 IOMUX_EPWM2_A_CFG_REG Register (Offset = BCh) [reset = 5F7h]

EPWM2_A IO config register.

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Table 2-2238. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00BCh

Figure 2-1116. IOMUX_EPWM2_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2239. IOMUX_EPWM2_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2239. IOMUX_EPWM2_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.49 IOMUX_EPWM2_B_CFG_REG Register

2.7.2.49.1 IOMUX_EPWM2_B_CFG_REG Register (Offset = C0h) [reset = 5F7h]

EPWM2_B IO config register.

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Table 2-2240. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00C0h

Figure 2-1117. IOMUX_EPWM2_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2241. IOMUX_EPWM2_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2241. IOMUX_EPWM2_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.50 IOMUX_EPWM3_A_CFG_REG Register

2.7.2.50.1 IOMUX_EPWM3_A_CFG_REG Register (Offset = C4h) [reset = 5F7h]

EPWM3_A IO config register.

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Table 2-2242. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00C4h

Figure 2-1118. IOMUX_EPWM3_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2243. IOMUX_EPWM3_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2243. IOMUX_EPWM3_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.51 IOMUX_EPWM3_B_CFG_REG Register

2.7.2.51.1 IOMUX_EPWM3_B_CFG_REG Register (Offset = C8h) [reset = 5F7h]

EPWM3_B IO config register.

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Table 2-2244. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00C8h

Figure 2-1119. IOMUX_EPWM3_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2245. IOMUX_EPWM3_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2245. IOMUX_EPWM3_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.52 IOMUX_EPWM4_A_CFG_REG Register

2.7.2.52.1 IOMUX_EPWM4_A_CFG_REG Register (Offset = CCh) [reset = 5F7h]

EPWM4_A IO config register.

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Table 2-2246. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00CCh

Figure 2-1120. IOMUX_EPWM4_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2247. IOMUX_EPWM4_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2247. IOMUX_EPWM4_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.53 IOMUX_EPWM4_B_CFG_REG Register

2.7.2.53.1 IOMUX_EPWM4_B_CFG_REG Register (Offset = D0h) [reset = 5F7h]

EPWM4_B IO config register.

Return to Summary Table

Table 2-2248. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00D0h

Figure 2-1121. IOMUX_EPWM4_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2249. IOMUX_EPWM4_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2249. IOMUX_EPWM4_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.54 IOMUX_EPWM5_A_CFG_REG Register

2.7.2.54.1 IOMUX_EPWM5_A_CFG_REG Register (Offset = D4h) [reset = 5F7h]

EPWM5_A IO config register.

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Table 2-2250. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00D4h

Figure 2-1122. IOMUX_EPWM5_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2251. IOMUX_EPWM5_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2251. IOMUX_EPWM5_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.55 IOMUX_EPWM5_B_CFG_REG Register

2.7.2.55.1 IOMUX_EPWM5_B_CFG_REG Register (Offset = D8h) [reset = 5F7h]

EPWM5_B IO config register.

Return to Summary Table

Table 2-2252. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00D8h

Figure 2-1123. IOMUX_EPWM5_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2253. IOMUX_EPWM5_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2253. IOMUX_EPWM5_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.56 IOMUX_EPWM6_A_CFG_REG Register

2.7.2.56.1 IOMUX_EPWM6_A_CFG_REG Register (Offset = DCh) [reset = 5F7h]

EPWM6_A IO config register.

Return to Summary Table

Table 2-2254. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00DCh

Figure 2-1124. IOMUX_EPWM6_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2255. IOMUX_EPWM6_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2255. IOMUX_EPWM6_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.57 IOMUX_EPWM6_B_CFG_REG Register

2.7.2.57.1 IOMUX_EPWM6_B_CFG_REG Register (Offset = E0h) [reset = 5F7h]

EPWM6_B IO config register.

Return to Summary Table

Table 2-2256. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00E0h

Figure 2-1125. IOMUX_EPWM6_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2257. IOMUX_EPWM6_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2257. IOMUX_EPWM6_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.58 IOMUX_EPWM7_A_CFG_REG Register

2.7.2.58.1 IOMUX_EPWM7_A_CFG_REG Register (Offset = E4h) [reset = 5F7h]

EPWM7_A IO config register.

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Table 2-2258. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00E4h

Figure 2-1126. IOMUX_EPWM7_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2259. IOMUX_EPWM7_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2259. IOMUX_EPWM7_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.59 IOMUX_EPWM7_B_CFG_REG Register

2.7.2.59.1 IOMUX_EPWM7_B_CFG_REG Register (Offset = E8h) [reset = 5F7h]

EPWM7_B IO config register.

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Table 2-2260. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00E8h

Figure 2-1127. IOMUX_EPWM7_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2261. IOMUX_EPWM7_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2261. IOMUX_EPWM7_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.60 IOMUX_EPWM8_A_CFG_REG Register

2.7.2.60.1 IOMUX_EPWM8_A_CFG_REG Register (Offset = ECh) [reset = 5F7h]

EPWM8_A IO config register.

Return to Summary Table

Table 2-2262. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00ECh

Figure 2-1128. IOMUX_EPWM8_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2263. IOMUX_EPWM8_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2263. IOMUX_EPWM8_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.61 IOMUX_EPWM8_B_CFG_REG Register

2.7.2.61.1 IOMUX_EPWM8_B_CFG_REG Register (Offset = F0h) [reset = 5F7h]

EPWM8_B IO config register.

Return to Summary Table

Table 2-2264. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00F0h

Figure 2-1129. IOMUX_EPWM8_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2265. IOMUX_EPWM8_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2265. IOMUX_EPWM8_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.62 IOMUX_EPWM9_A_CFG_REG Register

2.7.2.62.1 IOMUX_EPWM9_A_CFG_REG Register (Offset = F4h) [reset = 5F7h]

EPWM9_A IO config register.

Return to Summary Table

Table 2-2266. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00F4h

Figure 2-1130. IOMUX_EPWM9_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2267. IOMUX_EPWM9_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2267. IOMUX_EPWM9_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.63 IOMUX_EPWM9_B_CFG_REG Register

2.7.2.63.1 IOMUX_EPWM9_B_CFG_REG Register (Offset = F8h) [reset = 5F7h]

EPWM9_B IO config register.

Return to Summary Table

Table 2-2268. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00F8h

Figure 2-1131. IOMUX_EPWM9_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2269. IOMUX_EPWM9_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2269. IOMUX_EPWM9_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.64 IOMUX_EPWM10_A_CFG_REG Register

2.7.2.64.1 IOMUX_EPWM10_A_CFG_REG Register (Offset = FCh) [reset = 5F7h]

EPWM10_A IO config register.

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Table 2-2270. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 00FCh

Figure 2-1132. IOMUX_EPWM10_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2271. IOMUX_EPWM10_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2271. IOMUX_EPWM10_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.65 IOMUX_EPWM10_B_CFG_REG Register

2.7.2.65.1 IOMUX_EPWM10_B_CFG_REG Register (Offset = 100h) [reset = 5F7h]

EPWM10_B IO config register.

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Table 2-2272. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0100h

Figure 2-1133. IOMUX_EPWM10_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2273. IOMUX_EPWM10_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2273. IOMUX_EPWM10_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.66 IOMUX_EPWM11_A_CFG_REG Register

2.7.2.66.1 IOMUX_EPWM11_A_CFG_REG Register (Offset = 104h) [reset = 5F7h]

EPWM11_A IO config register.

Return to Summary Table

Table 2-2274. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0104h

Figure 2-1134. IOMUX_EPWM11_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2275. IOMUX_EPWM11_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2275. IOMUX_EPWM11_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.67 IOMUX_EPWM11_B_CFG_REG Register

2.7.2.67.1 IOMUX_EPWM11_B_CFG_REG Register (Offset = 108h) [reset = 5F7h]

EPWM11_B IO config register.

Return to Summary Table

Table 2-2276. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0108h

Figure 2-1135. IOMUX_EPWM11_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2277. IOMUX_EPWM11_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2277. IOMUX_EPWM11_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.68 IOMUX_EPWM12_A_CFG_REG Register

2.7.2.68.1 IOMUX_EPWM12_A_CFG_REG Register (Offset = 10Ch) [reset = 5F7h]

EPWM12_A IO config register.

Return to Summary Table

Table 2-2278. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 010Ch

Figure 2-1136. IOMUX_EPWM12_A_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2279. IOMUX_EPWM12_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2279. IOMUX_EPWM12_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.69 IOMUX_EPWM12_B_CFG_REG Register

2.7.2.69.1 IOMUX_EPWM12_B_CFG_REG Register (Offset = 110h) [reset = 5F7h]

EPWM12_B IO config register.

Return to Summary Table

Table 2-2280. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0110h

Figure 2-1137. IOMUX_EPWM12_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2281. IOMUX_EPWM12_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2281. IOMUX_EPWM12_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.70 IOMUX_EPWM13_A_CFG_REG Register

2.7.2.70.1 IOMUX_EPWM13_A_CFG_REG Register (Offset = 114h) [reset = 5F7h]

EPWM13_A IO config register.

Return to Summary Table

Table 2-2282. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0114h

Figure 2-1138. IOMUX_EPWM13_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2283. IOMUX_EPWM13_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2283. IOMUX_EPWM13_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.71 IOMUX_EPWM13_B_CFG_REG Register

2.7.2.71.1 IOMUX_EPWM13_B_CFG_REG Register (Offset = 118h) [reset = 5F7h]

EPWM13_B IO config register.

Return to Summary Table

Table 2-2284. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0118h

Figure 2-1139. IOMUX_EPWM13_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2285. IOMUX_EPWM13_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2285. IOMUX_EPWM13_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.72 IOMUX_EPWM14_A_CFG_REG Register

2.7.2.72.1 IOMUX_EPWM14_A_CFG_REG Register (Offset = 11Ch) [reset = 5F7h]

EPWM14_A IO config register.

Return to Summary Table

Table 2-2286. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 011Ch

Figure 2-1140. IOMUX_EPWM14_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2287. IOMUX_EPWM14_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2287. IOMUX_EPWM14_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.73 IOMUX_EPWM14_B_CFG_REG Register

2.7.2.73.1 IOMUX_EPWM14_B_CFG_REG Register (Offset = 120h) [reset = 5F7h]

EPWM14_B IO config register.

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Table 2-2288. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0120h

Figure 2-1141. IOMUX_EPWM14_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2289. IOMUX_EPWM14_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2289. IOMUX_EPWM14_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.74 IOMUX_EPWM15_A_CFG_REG Register

2.7.2.74.1 IOMUX_EPWM15_A_CFG_REG Register (Offset = 124h) [reset = 5F7h]

EPWM15_A IO config register.

Return to Summary Table

Table 2-2290. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0124h

Figure 2-1142. IOMUX_EPWM15_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2291. IOMUX_EPWM15_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2291. IOMUX_EPWM15_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.75 IOMUX_EPWM15_B_CFG_REG Register

2.7.2.75.1 IOMUX_EPWM15_B_CFG_REG Register (Offset = 128h) [reset = 5F7h]

EPWM15_B IO config register.

Return to Summary Table

Table 2-2292. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0128h

Figure 2-1143. IOMUX_EPWM15_B_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2293. IOMUX_EPWM15_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2293. IOMUX_EPWM15_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.76 IOMUX_UART1_RXD_CFG_REG Register

2.7.2.76.1 IOMUX_UART1_RXD_CFG_REG Register (Offset = 12Ch) [reset = 5F7h]

UART1_RXD IO config register.

Return to Summary Table

Table 2-2294. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 012Ch

Figure 2-1144. IOMUX_UART1_RXD_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2295. IOMUX_UART1_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2295. IOMUX_UART1_RXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.77 IOMUX_UART1_TXD_CFG_REG Register

2.7.2.77.1 IOMUX_UART1_TXD_CFG_REG Register (Offset = 130h) [reset = 5F7h]

UART1_TXD IO config register.

Return to Summary Table

Table 2-2296. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0130h

Figure 2-1145. IOMUX_UART1_TXD_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2297. IOMUX_UART1_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2297. IOMUX_UART1_TXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.78 IOMUX_MMC0_CLK_CFG_REG Register

2.7.2.78.1 IOMUX_MMC0_CLK_CFG_REG Register (Offset = 134h) [reset = 5F7h]

MMC0_CLK IO config register.

Return to Summary Table

Table 2-2298. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0134h

Figure 2-1146. IOMUX_MMC0_CLK_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2299. IOMUX_MMC0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2299. IOMUX_MMC0_CLK_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.79 IOMUX_MMC0_CMD_CFG_REG Register

2.7.2.79.1 IOMUX_MMC0_CMD_CFG_REG Register (Offset = 138h) [reset = 5F7h]

MMC0_CMD IO config register.

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Table 2-2300. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0138h

Figure 2-1147. IOMUX_MMC0_CMD_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2301. IOMUX_MMC0_CMD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2301. IOMUX_MMC0_CMD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.80 IOMUX_MMC0_D0_CFG_REG Register

2.7.2.80.1 IOMUX_MMC0_D0_CFG_REG Register (Offset = 13Ch) [reset = 5F7h]

MMC0_D0 IO config register.

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Table 2-2302. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 013Ch

Figure 2-1148. IOMUX_MMC0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2303. IOMUX_MMC0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2303. IOMUX_MMC0_D0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.81 IOMUX_MMC0_D1_CFG_REG Register

2.7.2.81.1 IOMUX_MMC0_D1_CFG_REG Register (Offset = 140h) [reset = 5F7h]

MMC0_D1 IO config register.

Return to Summary Table

Table 2-2304. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0140h

Figure 2-1149. IOMUX_MMC0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2305. IOMUX_MMC0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2305. IOMUX_MMC0_D1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.82 IOMUX_MMC0_D2_CFG_REG Register

2.7.2.82.1 IOMUX_MMC0_D2_CFG_REG Register (Offset = 144h) [reset = 5F7h]

MMC0_D2 IO config register.

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Table 2-2306. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0144h

Figure 2-1150. IOMUX_MMC0_D2_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2307. IOMUX_MMC0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2307. IOMUX_MMC0_D2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.83 IOMUX_MMC0_D3_CFG_REG Register

2.7.2.83.1 IOMUX_MMC0_D3_CFG_REG Register (Offset = 148h) [reset = 5F7h]

MMC0_D3 IO config register.

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Table 2-2308. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0148h

Figure 2-1151. IOMUX_MMC0_D3_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2309. IOMUX_MMC0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2309. IOMUX_MMC0_D3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.84 IOMUX_MMC0_WP_CFG_REG Register

2.7.2.84.1 IOMUX_MMC0_WP_CFG_REG Register (Offset = 14Ch) [reset = 5F7h]

MMC0_WP IO config register.

Return to Summary Table

Table 2-2310. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 014Ch

Figure 2-1152. IOMUX_MMC0_WP_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2311. IOMUX_MMC0_WP_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2311. IOMUX_MMC0_WP_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.85 IOMUX_MMC0_CD_CFG_REG Register

2.7.2.85.1 IOMUX_MMC0_CD_CFG_REG Register (Offset = 150h) [reset = 5F7h]

MMC0_CD IO config register.

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Table 2-2312. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0150h

Figure 2-1153. IOMUX_MMC0_CD_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2313. IOMUX_MMC0_CD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2313. IOMUX_MMC0_CD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.86 IOMUX_PR0_MDIO0_MDIO_CFG_REG Register

2.7.2.86.1 IOMUX_PR0_MDIO0_MDIO_CFG_REG Register (Offset = 154h) [reset = 5F7h]

PR0_MDIO0_MDIO IO config register.

Return to Summary Table

Table 2-2314. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0154h

Figure 2-1154. IOMUX_PR0_MDIO0_MDIO_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2315. IOMUX_PR0_MDIO0_MDIO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2315. IOMUX_PR0_MDIO0_MDIO_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.87 IOMUX_PR0_MDIO0_MDC_CFG_REG Register

2.7.2.87.1 IOMUX_PR0_MDIO0_MDC_CFG_REG Register (Offset = 158h) [reset = 5F7h]

PR0_MDIO0_MDC IO config register.

Return to Summary Table

Table 2-2316. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0158h

Figure 2-1155. IOMUX_PR0_MDIO0_MDC_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2317. IOMUX_PR0_MDIO0_MDC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2317. IOMUX_PR0_MDIO0_MDC_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.88 IOMUX_PR0_PRU0_GPO5_CFG_REG Register

2.7.2.88.1 IOMUX_PR0_PRU0_GPO5_CFG_REG Register (Offset = 15Ch) [reset = 5F7h]

PR0_PRU0_GPO5 IO config register.

Return to Summary Table

Table 2-2318. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 015Ch

Figure 2-1156. IOMUX_PR0_PRU0_GPO5_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2319. IOMUX_PR0_PRU0_GPO5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2319. IOMUX_PR0_PRU0_GPO5_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.89 IOMUX_PR0_PRU0_GPO9_CFG_REG Register

2.7.2.89.1 IOMUX_PR0_PRU0_GPO9_CFG_REG Register (Offset = 160h) [reset = 5F7h]

PR0_PRU0_GPO9 IO config register.

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Table 2-2320. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0160h

Figure 2-1157. IOMUX_PR0_PRU0_GPO9_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2321. IOMUX_PR0_PRU0_GPO9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2321. IOMUX_PR0_PRU0_GPO9_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.90 IOMUX_PR0_PRU0_GPO10_CFG_REG Register

2.7.2.90.1 IOMUX_PR0_PRU0_GPO10_CFG_REG Register (Offset = 164h) [reset = 5F7h]

PR0_PRU0_GPO10 IO config register.

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Table 2-2322. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0164h

Figure 2-1158. IOMUX_PR0_PRU0_GPO10_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2323. IOMUX_PR0_PRU0_GPO10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2323. IOMUX_PR0_PRU0_GPO10_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.91 IOMUX_PR0_PRU0_GPO8_CFG_REG Register

2.7.2.91.1 IOMUX_PR0_PRU0_GPO8_CFG_REG Register (Offset = 168h) [reset = 5F7h]

PR0_PRU0_GPO8 IO config register.

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Table 2-2324. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0168h

Figure 2-1159. IOMUX_PR0_PRU0_GPO8_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2325. IOMUX_PR0_PRU0_GPO8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2325. IOMUX_PR0_PRU0_GPO8_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.92 IOMUX_PR0_PRU0_GPO6_CFG_REG Register

2.7.2.92.1 IOMUX_PR0_PRU0_GPO6_CFG_REG Register (Offset = 16Ch) [reset = 5F7h]

PR0_PRU0_GPO6 IO config register.

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Table 2-2326. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 016Ch

Figure 2-1160. IOMUX_PR0_PRU0_GPO6_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2327. IOMUX_PR0_PRU0_GPO6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2327. IOMUX_PR0_PRU0_GPO6_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.93 IOMUX_PR0_PRU0_GPO4_CFG_REG Register

2.7.2.93.1 IOMUX_PR0_PRU0_GPO4_CFG_REG Register (Offset = 170h) [reset = 5F7h]

PR0_PRU0_GPO4 IO config register.

Return to Summary Table

Table 2-2328. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0170h

Figure 2-1161. IOMUX_PR0_PRU0_GPO4_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2329. IOMUX_PR0_PRU0_GPO4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2329. IOMUX_PR0_PRU0_GPO4_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.94 IOMUX_PR0_PRU0_GPO0_CFG_REG Register

2.7.2.94.1 IOMUX_PR0_PRU0_GPO0_CFG_REG Register (Offset = 174h) [reset = 5F7h]

PR0_PRU0_GPO0 IO config register.

Return to Summary Table

Table 2-2330. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0174h

Figure 2-1162. IOMUX_PR0_PRU0_GPO0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2331. IOMUX_PR0_PRU0_GPO0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2331. IOMUX_PR0_PRU0_GPO0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.95 IOMUX_PR0_PRU0_GPO1_CFG_REG Register

2.7.2.95.1 IOMUX_PR0_PRU0_GPO1_CFG_REG Register (Offset = 178h) [reset = 5F7h]

PR0_PRU0_GPO1 IO config register.

Return to Summary Table

Table 2-2332. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0178h

Figure 2-1163. IOMUX_PR0_PRU0_GPO1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2333. IOMUX_PR0_PRU0_GPO1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2333. IOMUX_PR0_PRU0_GPO1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.96 IOMUX_PR0_PRU0_GPO2_CFG_REG Register

2.7.2.96.1 IOMUX_PR0_PRU0_GPO2_CFG_REG Register (Offset = 17Ch) [reset = 5F7h]

PR0_PRU0_GPO2 IO config register.

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Table 2-2334. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 017Ch

Figure 2-1164. IOMUX_PR0_PRU0_GPO2_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2335. IOMUX_PR0_PRU0_GPO2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2335. IOMUX_PR0_PRU0_GPO2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.97 IOMUX_PR0_PRU0_GPO3_CFG_REG Register

2.7.2.97.1 IOMUX_PR0_PRU0_GPO3_CFG_REG Register (Offset = 180h) [reset = 5F7h]

PR0_PRU0_GPO3 IO config register.

Return to Summary Table

Table 2-2336. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0180h

Figure 2-1165. IOMUX_PR0_PRU0_GPO3_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2337. IOMUX_PR0_PRU0_GPO3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2337. IOMUX_PR0_PRU0_GPO3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.98 IOMUX_PR0_PRU0_GPO16_CFG_REG Register

2.7.2.98.1 IOMUX_PR0_PRU0_GPO16_CFG_REG Register (Offset = 184h) [reset = 5F7h]

PR0_PRU0_GPO16 IO config register.

Return to Summary Table

Table 2-2338. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0184h

Figure 2-1166. IOMUX_PR0_PRU0_GPO16_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2339. IOMUX_PR0_PRU0_GPO16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2339. IOMUX_PR0_PRU0_GPO16_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.99 IOMUX_PR0_PRU0_GPO15_CFG_REG Register

2.7.2.99.1 IOMUX_PR0_PRU0_GPO15_CFG_REG Register (Offset = 188h) [reset = 5F7h]

PR0_PRU0_GPO15 IO config register.

Return to Summary Table

Table 2-2340. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0188h

Figure 2-1167. IOMUX_PR0_PRU0_GPO15_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2341. IOMUX_PR0_PRU0_GPO15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2341. IOMUX_PR0_PRU0_GPO15_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.100 IOMUX_PR0_PRU0_GPO11_CFG_REG Register

2.7.2.100.1 IOMUX_PR0_PRU0_GPO11_CFG_REG Register (Offset = 18Ch) [reset = 5F7h]

PR0_PRU0_GPO11 IO config register.

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Table 2-2342. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 018Ch

Figure 2-1168. IOMUX_PR0_PRU0_GPO11_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2343. IOMUX_PR0_PRU0_GPO11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2343. IOMUX_PR0_PRU0_GPO11_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.101 IOMUX_PR0_PRU0_GPO12_CFG_REG Register

2.7.2.101.1 IOMUX_PR0_PRU0_GPO12_CFG_REG Register (Offset = 190h) [reset = 5F7h]

PR0_PRU0_GPO12 IO config register.

Return to Summary Table

Table 2-2344. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0190h

Figure 2-1169. IOMUX_PR0_PRU0_GPO12_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2345. IOMUX_PR0_PRU0_GPO12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2345. IOMUX_PR0_PRU0_GPO12_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.102 IOMUX_PR0_PRU0_GPO13_CFG_REG Register

2.7.2.102.1 IOMUX_PR0_PRU0_GPO13_CFG_REG Register (Offset = 194h) [reset = 5F7h]

PR0_PRU0_GPO13 IO config register.

Return to Summary Table

Table 2-2346. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0194h

Figure 2-1170. IOMUX_PR0_PRU0_GPO13_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2347. IOMUX_PR0_PRU0_GPO13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2347. IOMUX_PR0_PRU0_GPO13_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.103 IOMUX_PR0_PRU0_GPO14_CFG_REG Register

2.7.2.103.1 IOMUX_PR0_PRU0_GPO14_CFG_REG Register (Offset = 198h) [reset = 5F7h]

PR0_PRU0_GPO14 IO config register.

Return to Summary Table

Table 2-2348. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0198h

Figure 2-1171. IOMUX_PR0_PRU0_GPO14_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2349. IOMUX_PR0_PRU0_GPO14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2349. IOMUX_PR0_PRU0_GPO14_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.104 IOMUX_PR0_PRU1_GPO5_CFG_REG Register

2.7.2.104.1 IOMUX_PR0_PRU1_GPO5_CFG_REG Register (Offset = 19Ch) [reset = 5F7h]

PR0_PRU1_GPO5 IO config register.

Return to Summary Table

Table 2-2350. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 019Ch

Figure 2-1172. IOMUX_PR0_PRU1_GPO5_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2351. IOMUX_PR0_PRU1_GPO5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2351. IOMUX_PR0_PRU1_GPO5_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.105 IOMUX_PR0_PRU1_GPO9_CFG_REG Register

2.7.2.105.1 IOMUX_PR0_PRU1_GPO9_CFG_REG Register (Offset = 1A0h) [reset = 5F7h]

PR0_PRU1_GPO9 IO config register.

Return to Summary Table

Table 2-2352. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01A0h

Figure 2-1173. IOMUX_PR0_PRU1_GPO9_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2353. IOMUX_PR0_PRU1_GPO9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2353. IOMUX_PR0_PRU1_GPO9_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.106 IOMUX_PR0_PRU1_GPO10_CFG_REG Register

2.7.2.106.1 IOMUX_PR0_PRU1_GPO10_CFG_REG Register (Offset = 1A4h) [reset = 5F7h]

PR0_PRU1_GPO10 IO config register.

Return to Summary Table

Table 2-2354. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01A4h

Figure 2-1174. IOMUX_PR0_PRU1_GPO10_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2355. IOMUX_PR0_PRU1_GPO10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2355. IOMUX_PR0_PRU1_GPO10_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.107 IOMUX_PR0_PRU1_GPO8_CFG_REG Register

2.7.2.107.1 IOMUX_PR0_PRU1_GPO8_CFG_REG Register (Offset = 1A8h) [reset = 5F7h]

PR0_PRU1_GPO8 IO config register.

Return to Summary Table

Table 2-2356. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01A8h

Figure 2-1175. IOMUX_PR0_PRU1_GPO8_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2357. IOMUX_PR0_PRU1_GPO8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2357. IOMUX_PR0_PRU1_GPO8_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.108 IOMUX_PR0_PRU1_GPO6_CFG_REG Register

2.7.2.108.1 IOMUX_PR0_PRU1_GPO6_CFG_REG Register (Offset = 1ACh) [reset = 5F7h]

PR0_PRU1_GPO6 IO config register.

Return to Summary Table

Table 2-2358. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01ACh

Figure 2-1176. IOMUX_PR0_PRU1_GPO6_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2359. IOMUX_PR0_PRU1_GPO6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2359. IOMUX_PR0_PRU1_GPO6_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.109 IOMUX_PR0_PRU1_GPO4_CFG_REG Register

2.7.2.109.1 IOMUX_PR0_PRU1_GPO4_CFG_REG Register (Offset = 1B0h) [reset = 5F7h]

PR0_PRU1_GPO4 IO config register.

Return to Summary Table

Table 2-2360. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01B0h

Figure 2-1177. IOMUX_PR0_PRU1_GPO4_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2361. IOMUX_PR0_PRU1_GPO4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2361. IOMUX_PR0_PRU1_GPO4_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.110 IOMUX_PR0_PRU1_GPO0_CFG_REG Register

2.7.2.110.1 IOMUX_PR0_PRU1_GPO0_CFG_REG Register (Offset = 1B4h) [reset = 5F7h]

PR0_PRU1_GPO0 IO config register.

Return to Summary Table

Table 2-2362. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01B4h

Figure 2-1178. IOMUX_PR0_PRU1_GPO0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2363. IOMUX_PR0_PRU1_GPO0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2363. IOMUX_PR0_PRU1_GPO0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.111 IOMUX_PR0_PRU1_GPO1_CFG_REG Register

2.7.2.111.1 IOMUX_PR0_PRU1_GPO1_CFG_REG Register (Offset = 1B8h) [reset = 5F7h]

PR0_PRU1_GPO1 IO config register.

Return to Summary Table

Table 2-2364. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01B8h

Figure 2-1179. IOMUX_PR0_PRU1_GPO1_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2365. IOMUX_PR0_PRU1_GPO1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2365. IOMUX_PR0_PRU1_GPO1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.112 IOMUX_PR0_PRU1_GPO2_CFG_REG Register

2.7.2.112.1 IOMUX_PR0_PRU1_GPO2_CFG_REG Register (Offset = 1BCh) [reset = 5F7h]

PR0_PRU1_GPO2 IO config register.

Return to Summary Table

Table 2-2366. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01BCh

Figure 2-1180. IOMUX_PR0_PRU1_GPO2_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2367. IOMUX_PR0_PRU1_GPO2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2367. IOMUX_PR0_PRU1_GPO2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.113 IOMUX_PR0_PRU1_GPO3_CFG_REG Register

2.7.2.113.1 IOMUX_PR0_PRU1_GPO3_CFG_REG Register (Offset = 1C0h) [reset = 5F7h]

PR0_PRU1_GPO3 IO config register.

Return to Summary Table

Table 2-2368. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01C0h

Figure 2-1181. IOMUX_PR0_PRU1_GPO3_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2369. IOMUX_PR0_PRU1_GPO3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2369. IOMUX_PR0_PRU1_GPO3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.114 IOMUX_PR0_PRU1_GPO16_CFG_REG Register

2.7.2.114.1 IOMUX_PR0_PRU1_GPO16_CFG_REG Register (Offset = 1C4h) [reset = 5F7h]

PR0_PRU1_GPO16 IO config register.

Return to Summary Table

Table 2-2370. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01C4h

Figure 2-1182. IOMUX_PR0_PRU1_GPO16_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2371. IOMUX_PR0_PRU1_GPO16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2371. IOMUX_PR0_PRU1_GPO16_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.115 IOMUX_PR0_PRU1_GPO15_CFG_REG Register

2.7.2.115.1 IOMUX_PR0_PRU1_GPO15_CFG_REG Register (Offset = 1C8h) [reset = 5F7h]

PR0_PRU1_GPO15 IO config register.

Return to Summary Table

Table 2-2372. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01C8h

Figure 2-1183. IOMUX_PR0_PRU1_GPO15_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2373. IOMUX_PR0_PRU1_GPO15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2373. IOMUX_PR0_PRU1_GPO15_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.116 IOMUX_PR0_PRU1_GPO11_CFG_REG Register

2.7.2.116.1 IOMUX_PR0_PRU1_GPO11_CFG_REG Register (Offset = 1CCh) [reset = 5F7h]

PR0_PRU1_GPO11 IO config register.

Return to Summary Table

Table 2-2374. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01CCh

Figure 2-1184. IOMUX_PR0_PRU1_GPO11_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2375. IOMUX_PR0_PRU1_GPO11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2375. IOMUX_PR0_PRU1_GPO11_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.117 IOMUX_PR0_PRU1_GPO12_CFG_REG Register

2.7.2.117.1 IOMUX_PR0_PRU1_GPO12_CFG_REG Register (Offset = 1D0h) [reset = 5F7h]

PR0_PRU1_GPO12 IO config register.

Return to Summary Table

Table 2-2376. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01D0h

Figure 2-1185. IOMUX_PR0_PRU1_GPO12_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2377. IOMUX_PR0_PRU1_GPO12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2377. IOMUX_PR0_PRU1_GPO12_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.118 IOMUX_PR0_PRU1_GPO13_CFG_REG Register

2.7.2.118.1 IOMUX_PR0_PRU1_GPO13_CFG_REG Register (Offset = 1D4h) [reset = 5F7h]

PR0_PRU1_GPO13 IO config register.

Return to Summary Table

Table 2-2378. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01D4h

Figure 2-1186. IOMUX_PR0_PRU1_GPO13_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2379. IOMUX_PR0_PRU1_GPO13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2379. IOMUX_PR0_PRU1_GPO13_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.119 IOMUX_PR0_PRU1_GPO14_CFG_REG Register

2.7.2.119.1 IOMUX_PR0_PRU1_GPO14_CFG_REG Register (Offset = 1D8h) [reset = 5F7h]

PR0_PRU1_GPO14 IO config register.

Return to Summary Table

Table 2-2380. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01D8h

Figure 2-1187. IOMUX_PR0_PRU1_GPO14_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2381. IOMUX_PR0_PRU1_GPO14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2381. IOMUX_PR0_PRU1_GPO14_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.120 IOMUX_PR0_PRU1_GPO19_CFG_REG Register

2.7.2.120.1 IOMUX_PR0_PRU1_GPO19_CFG_REG Register (Offset = 1DCh) [reset = 5F7h]

PR0_PRU1_GPO19 IO config register.

Return to Summary Table

Table 2-2382. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01DCh

Figure 2-1188. IOMUX_PR0_PRU1_GPO19_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2383. IOMUX_PR0_PRU1_GPO19_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2383. IOMUX_PR0_PRU1_GPO19_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.121 IOMUX_PR0_PRU1_GPO18_CFG_REG Register

2.7.2.121.1 IOMUX_PR0_PRU1_GPO18_CFG_REG Register (Offset = 1E0h) [reset = 5F7h]

PR0_PRU1_GPO18 IO config register.

Return to Summary Table

Table 2-2384. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01E0h

Figure 2-1189. IOMUX_PR0_PRU1_GPO18_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2385. IOMUX_PR0_PRU1_GPO18_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2385. IOMUX_PR0_PRU1_GPO18_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.122 IOMUX_EXT_REFCLK0_CFG_REG Register

2.7.2.122.1 IOMUX_EXT_REFCLK0_CFG_REG Register (Offset = 1E4h) [reset = 5F7h]

EXT_REFCLK0 IO config register.

Return to Summary Table

Table 2-2386. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01E4h

Figure 2-1190. IOMUX_EXT_REFCLK0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2387. IOMUX_EXT_REFCLK0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2387. IOMUX_EXT_REFCLK0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.123 IOMUX_SDFM0_CLK0_CFG_REG Register

2.7.2.123.1 IOMUX_SDFM0_CLK0_CFG_REG Register (Offset = 1E8h) [reset = 5F7h]

SDFM0_CLK0 IO config register.

Return to Summary Table

Table 2-2388. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01E8h

Figure 2-1191. IOMUX_SDFM0_CLK0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2389. IOMUX_SDFM0_CLK0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2389. IOMUX_SDFM0_CLK0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.124 IOMUX_SDFM0_D0_CFG_REG Register

2.7.2.124.1 IOMUX_SDFM0_D0_CFG_REG Register (Offset = 1ECh) [reset = 5F7h]

SDFM0_D0 IO config register.

Return to Summary Table

Table 2-2390. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01ECh

Figure 2-1192. IOMUX_SDFM0_D0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2391. IOMUX_SDFM0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2391. IOMUX_SDFM0_D0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.125 IOMUX_SDFM0_CLK1_CFG_REG Register

2.7.2.125.1 IOMUX_SDFM0_CLK1_CFG_REG Register (Offset = 1F0h) [reset = 5F7h]

SDFM0_CLK1 IO config register.

Return to Summary Table

Table 2-2392. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01F0h

Figure 2-1193. IOMUX_SDFM0_CLK1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2393. IOMUX_SDFM0_CLK1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2393. IOMUX_SDFM0_CLK1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.126 IOMUX_SDFM0_D1_CFG_REG Register

2.7.2.126.1 IOMUX_SDFM0_D1_CFG_REG Register (Offset = 1F4h) [reset = 5F7h]

SDFM0_D1 IO config register.

Return to Summary Table

Table 2-2394. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01F4h

Figure 2-1194. IOMUX_SDFM0_D1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2395. IOMUX_SDFM0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2395. IOMUX_SDFM0_D1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.127 IOMUX_SDFM0_CLK2_CFG_REG Register

2.7.2.127.1 IOMUX_SDFM0_CLK2_CFG_REG Register (Offset = 1F8h) [reset = 5F7h]

SDFM0_CLK2 IO config register.

Return to Summary Table

Table 2-2396. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01F8h

Figure 2-1195. IOMUX_SDFM0_CLK2_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2397. IOMUX_SDFM0_CLK2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2397. IOMUX_SDFM0_CLK2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.128 IOMUX_SDFM0_D2_CFG_REG Register

2.7.2.128.1 IOMUX_SDFM0_D2_CFG_REG Register (Offset = 1FCh) [reset = 5F7h]

SDFM0_D2 IO config register.

Return to Summary Table

Table 2-2398. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 01FCh

Figure 2-1196. IOMUX_SDFM0_D2_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2399. IOMUX_SDFM0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2399. IOMUX_SDFM0_D2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.129 IOMUX_SDFM0_CLK3_CFG_REG Register

2.7.2.129.1 IOMUX_SDFM0_CLK3_CFG_REG Register (Offset = 200h) [reset = 5F7h]

SDFM0_CLK3 IO config register.

Return to Summary Table

Table 2-2400. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0200h

Figure 2-1197. IOMUX_SDFM0_CLK3_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2401. IOMUX_SDFM0_CLK3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2401. IOMUX_SDFM0_CLK3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.130 IOMUX_SDFM0_D3_CFG_REG Register

2.7.2.130.1 IOMUX_SDFM0_D3_CFG_REG Register (Offset = 204h) [reset = 5F7h]

SDFM0_D3 IO config register.

Return to Summary Table

Table 2-2402. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0204h

Figure 2-1198. IOMUX_SDFM0_D3_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2403. IOMUX_SDFM0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2403. IOMUX_SDFM0_D3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.131 IOMUX_EQEP0_A_CFG_REG Register

2.7.2.131.1 IOMUX_EQEP0_A_CFG_REG Register (Offset = 208h) [reset = 5F7h]

EQEP0_A IO config register.

Return to Summary Table

Table 2-2404. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0208h

Figure 2-1199. IOMUX_EQEP0_A_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					

23	22	21	20	19	18	17	16
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2405. IOMUX_EQEP0_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2405. IOMUX_EQEP0_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.132 IOMUX_EQEP0_B_CFG_REG Register

2.7.2.132.1 IOMUX_EQEP0_B_CFG_REG Register (Offset = 20Ch) [reset = 5F7h]

EQEP0_B IO config register.

Return to Summary Table

Table 2-2406. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 020Ch

Figure 2-1200. IOMUX_EQEP0_B_CFG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>RSVD</td><td>RSVD</td><td colspan="6">RESERVED</td></tr>
<tr><td></td><td></td><td colspan="6">NONE</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>SAFETY_OVERRIDE_SEL</td><td>ICSSM_GPIO_SEL</td><td>INP_INV_SEL</td><td colspan="2">QUAL_SEL</td><td colspan="2">GPIO_SEL</td></tr>
<tr><td>NONE</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="2">R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td>SC1</td><td>PUPDSEL</td><td>PI</td></tr>
<tr><td colspan="5">NONE</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="5">0h</td><td>1h</td><td>0h</td><td>1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>OE_OVERRIDE</td><td>OE_OVERRIDE_CTRL</td><td>IE_OVERRIDE</td><td>IE_OVERRIDE_CTRL</td><td colspan="4">FUNC_SEL</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td><td colspan="4">7h</td></tr>
</table>

Table 2-2407. IOMUX_EQEP0_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2407. IOMUX_EQEP0_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.133 IOMUX_EQEP0_STROBE_CFG_REG Register

2.7.2.133.1 IOMUX_EQEP0_STROBE_CFG_REG Register (Offset = 210h) [reset = 5F7h]

EQEP0_STROBE IO config register.

Return to Summary Table

Table 2-2408. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0210h

Figure 2-1201. IOMUX_EQEP0_STROBE_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2409. IOMUX_EQEP0_STROBE_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2409. IOMUX_EQEP0_STROBE_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.134 IOMUX_EQEP0_INDEX_CFG_REG Register

2.7.2.134.1 IOMUX_EQEP0_INDEX_CFG_REG Register (Offset = 214h) [reset = 5F7h]

EQEP0_INDEX IO config register.

Return to Summary Table

Table 2-2410. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0214h

Figure 2-1202. IOMUX_EQEP0_INDEX_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2411. IOMUX_EQEP0_INDEX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2411. IOMUX_EQEP0_INDEX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.135 IOMUX_I2C0_SDA_CFG_REG Register

2.7.2.135.1 IOMUX_I2C0_SDA_CFG_REG Register (Offset = 218h) [reset = 5F7h]

I2C0_SDA IO config register.

Return to Summary Table

Table 2-2412. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0218h

Figure 2-1203. IOMUX_I2C0_SDA_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2413. IOMUX_I2C0_SDA_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2413. IOMUX_I2C0_SDA_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.136 IOMUX_I2C0_SCL_CFG_REG Register

2.7.2.136.1 IOMUX_I2C0_SCL_CFG_REG Register (Offset = 21Ch) [reset = 5F7h]

I2C0_SCL IO config register.

Return to Summary Table

Table 2-2414. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 021Ch

Figure 2-1204. IOMUX_I2C0_SCL_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2415. IOMUX_I2C0_SCL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2415. IOMUX_I2C0_SCL_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.137 IOMUX_MCAN2_TX_CFG_REG Register

2.7.2.137.1 IOMUX_MCAN2_TX_CFG_REG Register (Offset = 220h) [reset = 5F7h]

MCAN2_TX IO config register.

Return to Summary Table

Table 2-2416. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0220h

Figure 2-1205. IOMUX_MCAN2_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2417. IOMUX_MCAN2_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2417. IOMUX_MCAN2_TX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.138 IOMUX_MCAN2_RX_CFG_REG Register

2.7.2.138.1 IOMUX_MCAN2_RX_CFG_REG Register (Offset = 224h) [reset = 5F7h]

MCAN2_RX IO config register.

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Table 2-2418. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0224h

Figure 2-1206. IOMUX_MCAN2_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
1h	1h	1h	1h	7h			

Table 2-2419. IOMUX_MCAN2_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2419. IOMUX_MCAN2_RX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	7h	Function select

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2.7.2.139 IOMUX_CLKOUT0_CFG_REG Register

2.7.2.139.1 IOMUX_CLKOUT0_CFG_REG Register (Offset = 228h) [reset = 570h]

CLKOUT0 IO config register.

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Table 2-2420. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0228h

Figure 2-1207. IOMUX_CLKOUT0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RSVD	RSVD	RESERVED					
		NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	SAFETY_OVERRIDE_SEL	ICSSM_GPIO_SEL	INP_INV_SEL	QUAL_SEL		GPIO_SEL	
NONE	R/W	R/W	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	FUNC_SEL			
R/W	R/W	R/W	R/W	R/W			
0h	1h	1h	1h	0h			

Table 2-2421. IOMUX_CLKOUT0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
29:23	RESERVED	NONE	0h	Reserved
22	SAFETY_OVERRIDE_SEL	R/W	0h	mux Select Value to choose between Actual IO pad input and Safety override mux output 1 Safety override mux output is selected 0 Actual IO pad input is selected
21	ICSSM_GPIO_SEL	R/W	0h	mux Select Value to choose between ICSSM_GPIO and normal GPIO 1 ICSSM_GPIO is selected 0 Normal GPIO is selected
20	INP_INV_SEL	R/W	0h	Select Value for chosing inverted version of PAD input for chip: 0 : Non Inverted 1 : Inverted
19:18	QUAL_SEL	R/W	0h	Select Value for chosing input qualifer type for PAD. 00 : Sync, 01 : 3 Sample qual 10 : 6 Samples qual 11 : Async
17:16	GPIO_SEL	R/W	0h	R5F CPU ownership select for GPIO. 0 : GPO0, 1 :GPO1, 2 : GPO2, 3:GPO3
15:11	RESERVED	NONE	0h	Reserved

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Table 2-2421. IOMUX_CLKOUT0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3:0	FUNC_SEL	R/W	0h	Function select

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2.7.2.140 IOMUX_WARMRSTN_CFG_REG Register

2.7.2.140.1 IOMUX_WARMRSTN_CFG_REG Register (Offset = 22Ch) [reset = 510h]

WARMRSTn IO config register.

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Table 2-2422. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 022Ch

Figure 2-1208. IOMUX_WARMRSTN_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	1h	0h			

Table 2-2423. IOMUX_WARMRSTN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:11	RESERVED	NONE	0h	Reserved
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	0h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	0h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-2423. IOMUX_WARMRSTN_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	NONE	0h	Reserved

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2.7.2.141 IOMUX_SAFETY_ERRORN_CFG_REG Register

2.7.2.141.1 IOMUX_SAFETY_ERRORN_CFG_REG Register (Offset = 230h) [reset = 410h]

SAFETY_ERRORn IO config register.

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Table 2-2424. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0230h

Figure 2-1209. IOMUX_SAFETY_ERRORN_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	0h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	1h	0h			

Table 2-2425. IOMUX_SAFETY_ERRORN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:11	RESERVED	NONE	0h	Reserved
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	0h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	0h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-2425. IOMUX_SAFETY_ERRORN_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	NONE	0h	Reserved

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2.7.2.142 IOMUX_TDI_CFG_REG Register

2.7.2.142.1 IOMUX_TDI_CFG_REG Register (Offset = 234h) [reset = 6D0h]

TDI IO config register.

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Table 2-2426. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0234h

Figure 2-1210. IOMUX_TDI_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	1h	0h

7	6	5	4	3	2	1	0
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
1h	1h	0h	1h	0h			

Table 2-2427. IOMUX_TDI_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:11	RESERVED	NONE	0h	Reserved
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	1h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	0h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-2427. IOMUX_TDI_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	NONE	0h	Reserved

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2.7.2.143 IOMUX_TDO_CFG_REG Register

2.7.2.143.1 IOMUX_TDO_CFG_REG Register (Offset = 238h) [reset = 630h]

TDO IO config register.

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Table 2-2428. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0238h

Figure 2-1211. IOMUX_TDO_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	1h	1h	0h			

Table 2-2429. IOMUX_TDO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:11	RESERVED	NONE	0h	Reserved
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	1h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	0h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-2429. IOMUX_TDO_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	NONE	0h	Reserved

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2.7.2.144 IOMUX_TMS_CFG_REG Register

2.7.2.144.1 IOMUX_TMS_CFG_REG Register (Offset = 23Ch) [reset = 610h]

TMS IO config register.

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Table 2-2430. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 023Ch

Figure 2-1212. IOMUX_TMS_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	1h	0h			

Table 2-2431. IOMUX_TMS_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:11	RESERVED	NONE	0h	Reserved
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	1h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	0h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	0h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-2431. IOMUX_TMS_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	NONE	0h	Reserved

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2.7.2.145 IOMUX_TCK_CFG_REG Register

2.7.2.145.1 IOMUX_TCK_CFG_REG Register (Offset = 240h) [reset = 210h]

TCK IO config register.

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Table 2-2432. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0240h

Figure 2-1213. IOMUX_TCK_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					0h	1h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	1h	0h			

Table 2-2433. IOMUX_TCK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:11	RESERVED	NONE	0h	Reserved
10	SC1	R/W	0h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	1h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	0h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	0h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	0h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-2433. IOMUX_TCK_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	NONE	0h	Reserved

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2.7.2.146 IOMUX_OSPI0_CLKLB_CFG_REG Register

2.7.2.146.1 IOMUX_OSPI0_CLKLB_CFG_REG Register (Offset = 244h) [reset = 5F0h]

OSPI0_CLKLB IO config register.

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Table 2-2434. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0244h

Figure 2-1214. IOMUX_OSPI0_CLKLB_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					SC1	PUPDSEL	PI
NONE					R/W	R/W	R/W
0h					1h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OE_OVERRIDE	OE_OVERRIDE_CTRL	IE_OVERRIDE	IE_OVERRIDE_CTRL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
1h	1h	1h	1h	0h			

Table 2-2435. IOMUX_OSPI0_CLKLB_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:11	RESERVED	NONE	0h	Reserved
10	SC1	R/W	1h	IO Slew Rate Control : 0 : higher slew rate. 1:Lower slew rate.
9	PUPDSEL	R/W	0h	Internal Pull Resistor Direction Control bit 0:Pull-down Resistor 1:Pull-up Resistor
8	PI	R/W	1h	Pull Inhibit/Pull Disable 0 -- Enable 1- Disable
7	OE_OVERRIDE	R/W	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	R/W	1h	Output Override Control bit (Active Low) This bit provides a software override for the default OE_N/GZ hardware control. 0:Enable pad input override 1:Disable pad input override
5	IE_OVERRIDE	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH)
4	IE_OVERRIDE_CTRL	R/W	1h	Input Override (Active Low) 0:Override pad input signal to 0 (LOW) 1:Override pad input signal to 1 (HIGH) Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-2435. IOMUX_OSPI0_CLKLB_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	RESERVED	NONE	0h	Reserved

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2.7.2.147 IOMUX_QUAL_GRP_0_CFG_REG Register

2.7.2.147.1 IOMUX_QUAL_GRP_0_CFG_REG Register (Offset = 248h) [reset = 0h]

QUAL_GRP_0 config register.

Return to Summary Table

Table 2-2436. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0248h

Figure 2-1215. IOMUX_QUAL_GRP_0_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2437. IOMUX_QUAL_GRP_0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.148 IOMUX_QUAL_GRP_1_CFG_REG Register

2.7.2.148.1 IOMUX_QUAL_GRP_1_CFG_REG Register (Offset = 24Ch) [reset = 0h]

QUAL_GRP_1 config register.

Return to Summary Table

Table 2-2438. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 024Ch

Figure 2-1216. IOMUX_QUAL_GRP_1_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2439. IOMUX_QUAL_GRP_1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.149 IOMUX_QUAL_GRP_2_CFG_REG Register

2.7.2.149.1 IOMUX_QUAL_GRP_2_CFG_REG Register (Offset = 250h) [reset = 0h]

QUAL_GRP_2 config register.

Return to Summary Table

Table 2-2440. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0250h

Figure 2-1217. IOMUX_QUAL_GRP_2_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2441. IOMUX_QUAL_GRP_2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.150 IOMUX_QUAL_GRP_3_CFG_REG Register

2.7.2.150.1 IOMUX_QUAL_GRP_3_CFG_REG Register (Offset = 254h) [reset = 0h]

QUAL_GRP_3 config register.

Return to Summary Table

Table 2-2442. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0254h

Figure 2-1218. IOMUX_QUAL_GRP_3_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2443. IOMUX_QUAL_GRP_3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.151 IOMUX_QUAL_GRP_4_CFG_REG Register

2.7.2.151.1 IOMUX_QUAL_GRP_4_CFG_REG Register (Offset = 258h) [reset = 0h]

QUAL_GRP_4 config register.

Return to Summary Table

Table 2-2444. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0258h

Figure 2-1219. IOMUX_QUAL_GRP_4_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2445. IOMUX_QUAL_GRP_4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.152 IOMUX_QUAL_GRP_5_CFG_REG Register

2.7.2.152.1 IOMUX_QUAL_GRP_5_CFG_REG Register (Offset = 25Ch) [reset = 0h]

QUAL_GRP_5 config register.

Return to Summary Table

Table 2-2446. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 025Ch

Figure 2-1220. IOMUX_QUAL_GRP_5_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2447. IOMUX_QUAL_GRP_5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.153 IOMUX_QUAL_GRP_6_CFG_REG Register

2.7.2.153.1 IOMUX_QUAL_GRP_6_CFG_REG Register (Offset = 260h) [reset = 0h]

QUAL_GRP_6 config register.

Return to Summary Table

Table 2-2448. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0260h

Figure 2-1221. IOMUX_QUAL_GRP_6_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2449. IOMUX_QUAL_GRP_6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.154 IOMUX_QUAL_GRP_7_CFG_REG Register

2.7.2.154.1 IOMUX_QUAL_GRP_7_CFG_REG Register (Offset = 264h) [reset = 0h]

QUAL_GRP_7 config register.

Return to Summary Table

Table 2-2450. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0264h

Figure 2-1222. IOMUX_QUAL_GRP_7_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2451. IOMUX_QUAL_GRP_7_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.155 IOMUX_QUAL_GRP_8_CFG_REG Register

2.7.2.155.1 IOMUX_QUAL_GRP_8_CFG_REG Register (Offset = 268h) [reset = 0h]

QUAL_GRP_8 config register.

Return to Summary Table

Table 2-2452. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0268h

Figure 2-1223. IOMUX_QUAL_GRP_8_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2453. IOMUX_QUAL_GRP_8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.156 IOMUX_QUAL_GRP_9_CFG_REG Register

2.7.2.156.1 IOMUX_QUAL_GRP_9_CFG_REG Register (Offset = 26Ch) [reset = 0h]

QUAL_GRP_9 config register.

Return to Summary Table

Table 2-2454. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 026Ch

Figure 2-1224. IOMUX_QUAL_GRP_9_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2455. IOMUX_QUAL_GRP_9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.157 IOMUX_QUAL_GRP_10_CFG_REG Register

2.7.2.157.1 IOMUX_QUAL_GRP_10_CFG_REG Register (Offset = 270h) [reset = 0h]

QUAL_GRP_10 config register.

Return to Summary Table

Table 2-2456. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0270h

Figure 2-1225. IOMUX_QUAL_GRP_10_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2457. IOMUX_QUAL_GRP_10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.158 IOMUX_QUAL_GRP_11_CFG_REG Register

2.7.2.158.1 IOMUX_QUAL_GRP_11_CFG_REG Register (Offset = 274h) [reset = 0h]

QUAL_GRP_11 config register.

Return to Summary Table

Table 2-2458. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0274h

Figure 2-1226. IOMUX_QUAL_GRP_11_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2459. IOMUX_QUAL_GRP_11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.159 IOMUX_QUAL_GRP_12_CFG_REG Register

2.7.2.159.1 IOMUX_QUAL_GRP_12_CFG_REG Register (Offset = 278h) [reset = 0h]

QUAL_GRP_12 config register.

Return to Summary Table

Table 2-2460. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0278h

Figure 2-1227. IOMUX_QUAL_GRP_12_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2461. IOMUX_QUAL_GRP_12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.160 IOMUX_QUAL_GRP_13_CFG_REG Register

2.7.2.160.1 IOMUX_QUAL_GRP_13_CFG_REG Register (Offset = 27Ch) [reset = 0h]

QUAL_GRP_13 config register.

Return to Summary Table

Table 2-2462. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 027Ch

Figure 2-1228. IOMUX_QUAL_GRP_13_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2463. IOMUX_QUAL_GRP_13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.161 IOMUX_QUAL_GRP_14_CFG_REG Register

2.7.2.161.1 IOMUX_QUAL_GRP_14_CFG_REG Register (Offset = 280h) [reset = 0h]

QUAL_GRP_14 config register.

Return to Summary Table

Table 2-2464. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0280h

Figure 2-1229. IOMUX_QUAL_GRP_14_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2465. IOMUX_QUAL_GRP_14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.162 IOMUX_QUAL_GRP_15_CFG_REG Register

2.7.2.162.1 IOMUX_QUAL_GRP_15_CFG_REG Register (Offset = 284h) [reset = 0h]

QUAL_GRP_15 config register.

Return to Summary Table

Table 2-2466. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0284h

Figure 2-1230. IOMUX_QUAL_GRP_15_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2467. IOMUX_QUAL_GRP_15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.163 IOMUX_QUAL_GRP_16_CFG_REG Register

2.7.2.163.1 IOMUX_QUAL_GRP_16_CFG_REG Register (Offset = 288h) [reset = 0h]

QUAL_GRP_16 config register.

Return to Summary Table

Table 2-2468. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0288h

Figure 2-1231. IOMUX_QUAL_GRP_16_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2469. IOMUX_QUAL_GRP_16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.164 IOMUX_QUAL_GRP_17_CFG_REG Register

2.7.2.164.1 IOMUX_QUAL_GRP_17_CFG_REG Register (Offset = 28Ch) [reset = 0h]

QUAL_GRP_17 config register.

Return to Summary Table

Table 2-2470. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 028Ch

Figure 2-1232. IOMUX_QUAL_GRP_17_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
QUAL_PERIOD_PER_SAMPLE							
R/W							
0h							

Table 2-2471. IOMUX_QUAL_GRP_17_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30:8	RESERVED	NONE	0h	Reserved
7:0	QUAL_PERIOD_PER_SAMPLE	R/W	0h	MMR bits for programming the qualifier clock count per sample

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2.7.2.165 IOMUX_USER_MODE_EN Register

2.7.2.165.1 IOMUX_USER_MODE_EN Register (Offset = 290h) [reset = 0h]

USER_MODE_EN config register.

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Table 2-2472. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0290h

Figure 2-1233. IOMUX_USER_MODE_EN Name Register

31	30	29	28	27	26	25	24
USER_MODE_EN							
R/W							
0h							
23	22	21	20	19	18	17	16
USER_MODE_EN							
R/W							
0h							
15	14	13	12	11	10	9	8
USER_MODE_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
USER_MODE_EN							
R/W							
0h							

Table 2-2473. IOMUX_USER_MODE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	USER_MODE_EN	R/W	0h	Write 0XADADADAD to enable user mode write access to IO CFG space

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2.7.2.166 IOMUX_PADGLBL_CFG_REG Register

2.7.2.166.1 IOMUX_PADGLBL_CFG_REG Register (Offset = 294h) [reset = 0h]

Global config register for IO.

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Table 2-2474. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0294h

Figure 2-1234. IOMUX_PADGLBL_CFG_REG Name Register

31	30	29	28	27	26	25	24
PADGLBL_CFG_REG							
R/W							
0h							
23	22	21	20	19	18	17	16
PADGLBL_CFG_REG							
R/W							
0h							
15	14	13	12	11	10	9	8
PADGLBL_CFG_REG							
R/W							
0h							
7	6	5	4	3	2	1	0
PADGLBL_CFG_REG							
R/W							
0h							

Table 2-2475. IOMUX_PADGLBL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PADGLBL_CFG_REG	R/W	0h	2 0 : global_ie_n_ctl - Write 3'b111 to pass global_ie_n_val to IE_N/ RXACTIVE_N pin of all the IOs. 3 : global_ie_n_val - Active low 10 8 : global_oe_n_ctl - Write 3'b111 to pass global_oe_n_val to OE_N/GZ pin of all the IOs. 11 : global_oe_n_val - Active low 18 16 : global_pi_ctl - Write 3'b111 to pass global_pi_val and global_pu_val to all the IOs 19 : global_pi_val 20 : global_pu_val

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2.7.2.167 IOMUX_IO_CFG_KICK0 Register

2.7.2.167.1 IOMUX_IO_CFG_KICK0 Register (Offset = 298h) [reset = 0h]

KICK0 config register.

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Table 2-2476. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 0298h

Figure 2-1235. IOMUX_IO_CFG_KICK0 Name Register

31	30	29	28	27	26	25	24
IO_CFG_KICK0							
R/W							
0h							
23	22	21	20	19	18	17	16
IO_CFG_KICK0							
R/W							
0h							
15	14	13	12	11	10	9	8
IO_CFG_KICK0							
R/W							
0h							
7	6	5	4	3	2	1	0
IO_CFG_KICK0							
R/W							
0h							

Table 2-2477. IOMUX_IO_CFG_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IO_CFG_KICK0	R/W	0h	Kicker 0 Register. The value 83E7 0B13h must be written to KICK0 as part of the process to unlock the CPU.write access to the above PIN MUX registers [including IOCFGKICK1]

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2.7.2.168 IOMUX_IO_CFG_KICK1 Register

2.7.2.168.1 IOMUX_IO_CFG_KICK1 Register (Offset = 29Ch) [reset = C1h]

KICK1 config register.

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Table 2-2478. Instance Table

Instance Name	Physical Address
MSS_IOMUX	5310 029Ch

Figure 2-1236. IOMUX_IO_CFG_KICK1 Name Register

31	30	29	28	27	26	25	24
IO_CFG_KICK1							
R/W							
C1h							
23	22	21	20	19	18	17	16
IO_CFG_KICK1							
R/W							
C1h							
15	14	13	12	11	10	9	8
IO_CFG_KICK1							
R/W							
C1h							
7	6	5	4	3	2	1	0
IO_CFG_KICK1							
R/W							
C1h							

Table 2-2479. IOMUX_IO_CFG_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IO_CFG_KICK1	R/W	C1h	Kicker 1 Register. The value 95A4 F1E0h must be written to the KICK1 as part of the process to unlock the CPU write access to above PINMUX registers [excluding IOCFGKICK0]. IOCFGKICK0 has to be written with 83E70B13h to enable access to IOCFGKICK1.

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3 Real-time Control Subsystem (CONTROLSS) Registers

The Real-time Control Subsystem (CONTROLSS) registers are described in the following sections.

3.1 CONTROLSS 16-bit Register Access Note

Note

8-bit wide register access is **not allowed** for ADC, EPWM, DAC, CMPSS, EQEP, SDFM, and FSI MMR regions. 16-bit access must be used instead.

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3.2 ADC

ADC

3.2.1 ADC Summaries

ADC Summaries

Table 3-1. ADC_RESULTS Registers, Base Address=5010 0000h, Length=256

Offset	Length	Register Name	ADC0_G0_G5 Physical Address	ADC1_G0_G5 Physical Address	ADC2_G0_G5 Physical Address
0h	16	ADC_RESULTS_ADCRESULT0	5010 0000h	5010 1000h	5010 2000h
2h	16	ADC_RESULTS_ADCRESULT1	5010 0002h	5010 1002h	5010 2002h
4h	16	ADC_RESULTS_ADCRESULT2	5010 0004h	5010 1004h	5010 2004h
6h	16	ADC_RESULTS_ADCRESULT3	5010 0006h	5010 1006h	5010 2006h
8h	16	ADC_RESULTS_ADCRESULT4	5010 0008h	5010 1008h	5010 2008h
Ah	16	ADC_RESULTS_ADCRESULT5	5010 000Ah	5010 100Ah	5010 200Ah
Ch	16	ADC_RESULTS_ADCRESULT6	5010 000Ch	5010 100Ch	5010 200Ch
Eh	16	ADC_RESULTS_ADCRESULT7	5010 000Eh	5010 100Eh	5010 200Eh
10h	16	ADC_RESULTS_ADCRESULT8	5010 0010h	5010 1010h	5010 2010h
12h	16	ADC_RESULTS_ADCRESULT9	5010 0012h	5010 1012h	5010 2012h
14h	16	ADC_RESULTS_ADCRESULT10	5010 0014h	5010 1014h	5010 2014h
16h	16	ADC_RESULTS_ADCRESULT11	5010 0016h	5010 1016h	5010 2016h
18h	16	ADC_RESULTS_ADCRESULT12	5010 0018h	5010 1018h	5010 2018h
1Ah	16	ADC_RESULTS_ADCRESULT13	5010 001Ah	5010 101Ah	5010 201Ah
1Ch	16	ADC_RESULTS_ADCRESULT14	5010 001Ch	5010 101Ch	5010 201Ch
1Eh	16	ADC_RESULTS_ADCRESULT15	5010 001Eh	5010 101Eh	5010 201Eh
20h	32	ADC_RESULTS_ADCPPB1RESULT	5010 0020h	5010 1020h	5010 2020h
24h	32	ADC_RESULTS_ADCPPB2RESULT	5010 0024h	5010 1024h	5010 2024h
28h	32	ADC_RESULTS_ADCPPB3RESULT	5010 0028h	5010 1028h	5010 2028h
2Ch	32	ADC_RESULTS_ADCPPB4RESULT	5010 002Ch	5010 102Ch	5010 202Ch
30h	32	ADC_RESULTS_ADCPPB1SUM	5010 0030h	5010 1030h	5010 2030h
34h	16	ADC_RESULTS_ADCPPB1COUNT	5010 0034h	5010 1034h	5010 2034h
38h	32	ADC_RESULTS_ADCPPB2SUM	5010 0038h	5010 1038h	5010 2038h
3Ch	16	ADC_RESULTS_ADCPPB2COUNT	5010 003Ch	5010 103Ch	5010 203Ch
40h	32	ADC_RESULTS_ADCPPB3SUM	5010 0040h	5010 1040h	5010 2040h
44h	16	ADC_RESULTS_ADCPPB3COUNT	5010 0044h	5010 1044h	5010 2044h
48h	32	ADC_RESULTS_ADCPPB4SUM	5010 0048h	5010 1048h	5010 2048h
4Ch	16	ADC_RESULTS_ADCPPB4COUNT	5010 004Ch	5010 104Ch	5010 204Ch
50h	32	ADC_RESULTS_ADCPPB1MAX	5010 0050h	5010 1050h	5010 2050h
54h	16	ADC_RESULTS_ADCPPB1MAXI	5010 0054h	5010 1054h	5010 2054h
58h	32	ADC_RESULTS_ADCPPB1MIN	5010 0058h	5010 1058h	5010 2058h
5Ch	16	ADC_RESULTS_ADCPPB1MINI	5010 005Ch	5010 105Ch	5010 205Ch
60h	32	ADC_RESULTS_ADCPPB2MAX	5010 0060h	5010 1060h	5010 2060h

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Table 3-1. ADC_RESULTS Registers, Base Address=5010 0000h, Length=256 (continued)

Offset	Length	Register Name	ADC0_G0_G5 Physical Address	ADC1_G0_G5 Physical Address	ADC2_G0_G5 Physical Address
64h	16	ADC_RESULTS_ADCPPB2MAXI	5010 0064h	5010 1064h	5010 2064h
68h	32	ADC_RESULTS_ADCPPB2MIN	5010 0068h	5010 1068h	5010 2068h
6Ch	16	ADC_RESULTS_ADCPPB2MINI	5010 006Ch	5010 106Ch	5010 206Ch
70h	32	ADC_RESULTS_ADCPPB3MAX	5010 0070h	5010 1070h	5010 2070h
74h	16	ADC_RESULTS_ADCPPB3MAXI	5010 0074h	5010 1074h	5010 2074h
78h	32	ADC_RESULTS_ADCPPB3MIN	5010 0078h	5010 1078h	5010 2078h
7Ch	16	ADC_RESULTS_ADCPPB3MINI	5010 007Ch	5010 107Ch	5010 207Ch
80h	32	ADC_RESULTS_ADCPPB4MAX	5010 0080h	5010 1080h	5010 2080h
84h	16	ADC_RESULTS_ADCPPB4MAXI	5010 0084h	5010 1084h	5010 2084h
88h	32	ADC_RESULTS_ADCPPB4MIN	5010 0088h	5010 1088h	5010 2088h
8Ch	16	ADC_RESULTS_ADCPPB4MINI	5010 008Ch	5010 108Ch	5010 208Ch

Table 3-2. ADC_RESULTS Registers, Base Address=5010 0000h, Length=256

Offset	Length	Register Name	ADC3_G0_G5 Physical Address	ADC4_G0_G5 Physical Address
0h	16	ADC_RESULTS_ADCRESULT0	5010 3000h	5010 4000h
2h	16	ADC_RESULTS_ADCRESULT1	5010 3002h	5010 4002h
4h	16	ADC_RESULTS_ADCRESULT2	5010 3004h	5010 4004h
6h	16	ADC_RESULTS_ADCRESULT3	5010 3006h	5010 4006h
8h	16	ADC_RESULTS_ADCRESULT4	5010 3008h	5010 4008h
Ah	16	ADC_RESULTS_ADCRESULT5	5010 300Ah	5010 400Ah
Ch	16	ADC_RESULTS_ADCRESULT6	5010 300Ch	5010 400Ch
Eh	16	ADC_RESULTS_ADCRESULT7	5010 300Eh	5010 400Eh
10h	16	ADC_RESULTS_ADCRESULT8	5010 3010h	5010 4010h
12h	16	ADC_RESULTS_ADCRESULT9	5010 3012h	5010 4012h
14h	16	ADC_RESULTS_ADCRESULT10	5010 3014h	5010 4014h
16h	16	ADC_RESULTS_ADCRESULT11	5010 3016h	5010 4016h
18h	16	ADC_RESULTS_ADCRESULT12	5010 3018h	5010 4018h
1Ah	16	ADC_RESULTS_ADCRESULT13	5010 301Ah	5010 401Ah
1Ch	16	ADC_RESULTS_ADCRESULT14	5010 301Ch	5010 401Ch
1Eh	16	ADC_RESULTS_ADCRESULT15	5010 301Eh	5010 401Eh
20h	32	ADC_RESULTS_ADCPPB1RESULT	5010 3020h	5010 4020h
24h	32	ADC_RESULTS_ADCPPB2RESULT	5010 3024h	5010 4024h
28h	32	ADC_RESULTS_ADCPPB3RESULT	5010 3028h	5010 4028h
2Ch	32	ADC_RESULTS_ADCPPB4RESULT	5010 302Ch	5010 402Ch
30h	32	ADC_RESULTS_ADCPPB1SUM	5010 3030h	5010 4030h
34h	16	ADC_RESULTS_ADCPPB1COUNT	5010 3034h	5010 4034h
38h	32	ADC_RESULTS_ADCPPB2SUM	5010 3038h	5010 4038h
3Ch	16	ADC_RESULTS_ADCPPB2COUNT	5010 303Ch	5010 403Ch
40h	32	ADC_RESULTS_ADCPPB3SUM	5010 3040h	5010 4040h
44h	16	ADC_RESULTS_ADCPPB3COUNT	5010 3044h	5010 4044h
48h	32	ADC_RESULTS_ADCPPB4SUM	5010 3048h	5010 4048h
4Ch	16	ADC_RESULTS_ADCPPB4COUNT	5010 304Ch	5010 404Ch
50h	32	ADC_RESULTS_ADCPPB1MAX	5010 3050h	5010 4050h
54h	16	ADC_RESULTS_ADCPPB1MAXI	5010 3054h	5010 4054h
58h	32	ADC_RESULTS_ADCPPB1MIN	5010 3058h	5010 4058h

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Table 3-2. ADC_RESULTS Registers, Base Address=5010 0000h, Length=256 (continued)

Offset	Length	Register Name	ADC3_G0_G5 Physical Address	ADC4_G0_G5 Physical Address
5Ch	16	ADC_RESULTS_ADCPPB1MINI	5010 305Ch	5010 405Ch
60h	32	ADC_RESULTS_ADCPPB2MAX	5010 3060h	5010 4060h
64h	16	ADC_RESULTS_ADCPPB2MAXI	5010 3064h	5010 4064h
68h	32	ADC_RESULTS_ADCPPB2MIN	5010 3068h	5010 4068h
6Ch	16	ADC_RESULTS_ADCPPB2MINI	5010 306Ch	5010 406Ch
70h	32	ADC_RESULTS_ADCPPB3MAX	5010 3070h	5010 4070h
74h	16	ADC_RESULTS_ADCPPB3MAXI	5010 3074h	5010 4074h
78h	32	ADC_RESULTS_ADCPPB3MIN	5010 3078h	5010 4078h
7Ch	16	ADC_RESULTS_ADCPPB3MINI	5010 307Ch	5010 407Ch
80h	32	ADC_RESULTS_ADCPPB4MAX	5010 3080h	5010 4080h
84h	16	ADC_RESULTS_ADCPPB4MAXI	5010 3084h	5010 4084h
88h	32	ADC_RESULTS_ADCPPB4MIN	5010 3088h	5010 4088h
8Ch	16	ADC_RESULTS_ADCPPB4MINI	5010 308Ch	5010 408Ch

Table 3-3. ADC_CFG Registers, Base Address=502C 0000h, Length=256

Offset	Length	Register Name	ADC0_G0_G5 Physical Address	ADC1_G0_G5 Physical Address	ADC2_G0_G5 Physical Address
0h	16	ADC_CFG_ADCCTL1	502C 0000h	502C 1000h	502C 2000h
2h	16	ADC_CFG_ADCCTL2	502C 0002h	502C 1002h	502C 2002h
4h	16	ADC_CFG_ADCBURSTCTL	502C 0004h	502C 1004h	502C 2004h
6h	16	ADC_CFG_ADCINTFLG	502C 0006h	502C 1006h	502C 2006h
8h	16	ADC_CFG_ADCINTFLGCLR	502C 0008h	502C 1008h	502C 2008h
Ah	16	ADC_CFG_ADCINTOVF	502C 000Ah	502C 100Ah	502C 200Ah
Ch	16	ADC_CFG_ADCINTOVFCLR	502C 000Ch	502C 100Ch	502C 200Ch
Eh	16	ADC_CFG_ADCINTSEL1N2	502C 000Eh	502C 100Eh	502C 200Eh
10h	16	ADC_CFG_ADCINTSEL3N4	502C 0010h	502C 1010h	502C 2010h
12h	16	ADC_CFG_ADCSOCPRICTL	502C 0012h	502C 1012h	502C 2012h
14h	16	ADC_CFG_ADCINTSOCSEL1	502C 0014h	502C 1014h	502C 2014h
16h	16	ADC_CFG_ADCINTSOCSEL2	502C 0016h	502C 1016h	502C 2016h
18h	16	ADC_CFG_ADCSOCFLG1	502C 0018h	502C 1018h	502C 2018h
1Ah	16	ADC_CFG_ADCSOCFRC1	502C 001Ah	502C 101Ah	502C 201Ah
1Ch	16	ADC_CFG_ADCSOCOVF1	502C 001Ch	502C 101Ch	502C 201Ch
1Eh	16	ADC_CFG_ADCSOCOVFCLR1	502C 001Eh	502C 101Eh	502C 201Eh
20h	32	ADC_CFG_ADCSOC0CTL	502C 0020h	502C 1020h	502C 2020h
24h	32	ADC_CFG_ADCSOC1CTL	502C 0024h	502C 1024h	502C 2024h
28h	32	ADC_CFG_ADCSOC2CTL	502C 0028h	502C 1028h	502C 2028h
2Ch	32	ADC_CFG_ADCSOC3CTL	502C 002Ch	502C 102Ch	502C 202Ch
30h	32	ADC_CFG_ADCSOC4CTL	502C 0030h	502C 1030h	502C 2030h
34h	32	ADC_CFG_ADCSOC5CTL	502C 0034h	502C 1034h	502C 2034h
38h	32	ADC_CFG_ADCSOC6CTL	502C 0038h	502C 1038h	502C 2038h
3Ch	32	ADC_CFG_ADCSOC7CTL	502C 003Ch	502C 103Ch	502C 203Ch
40h	32	ADC_CFG_ADCSOC8CTL	502C 0040h	502C 1040h	502C 2040h
44h	32	ADC_CFG_ADCSOC9CTL	502C 0044h	502C 1044h	502C 2044h
48h	32	ADC_CFG_ADCSOC10CTL	502C 0048h	502C 1048h	502C 2048h
4Ch	32	ADC_CFG_ADCSOC11CTL	502C 004Ch	502C 104Ch	502C 204Ch
50h	32	ADC_CFG_ADCSOC12CTL	502C 0050h	502C 1050h	502C 2050h

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Table 3-3. ADC_CFG Registers, Base Address=502C 0000h, Length=256 (continued)

Offset	Length	Register Name	ADC0_G0_G5 Physical Address	ADC1_G0_G5 Physical Address	ADC2_G0_G5 Physical Address
54h	32	ADC_CFG_ADCSOC13CTL	502C 0054h	502C 1054h	502C 2054h
58h	32	ADC_CFG_ADCSOC14CTL	502C 0058h	502C 1058h	502C 2058h
5Ch	32	ADC_CFG_ADCSOC15CTL	502C 005Ch	502C 105Ch	502C 205Ch
60h	16	ADC_CFG_ADCEVTSTAT	502C 0060h	502C 1060h	502C 2060h
64h	16	ADC_CFG_ADCEVTCLR	502C 0064h	502C 1064h	502C 2064h
68h	16	ADC_CFG_ADCEVTSEL	502C 0068h	502C 1068h	502C 2068h
6Ch	16	ADC_CFG_ADCEVTINTSEL	502C 006Ch	502C 106Ch	502C 206Ch
72h	16	ADC_CFG_ADCCOUNTER	502C 0072h	502C 1072h	502C 2072h
74h	16	ADC_CFG_ADCREV	502C 0074h	502C 1074h	502C 2074h
80h	16	ADC_CFG_ADCPPB1CONFIG	502C 0080h	502C 1080h	502C 2080h
82h	16	ADC_CFG_ADCPPB1STAMP	502C 0082h	502C 1082h	502C 2082h
84h	16	ADC_CFG_ADCPPB1OFFCAL	502C 0084h	502C 1084h	502C 2084h
86h	16	ADC_CFG_ADCPPB1OFFREF	502C 0086h	502C 1086h	502C 2086h
88h	32	ADC_CFG_ADCPPB1TRIPHI	502C 0088h	502C 1088h	502C 2088h
8Ch	32	ADC_CFG_ADCPPB1TRIPLO	502C 008Ch	502C 108Ch	502C 208Ch
90h	16	ADC_CFG_ADCPPB2CONFIG	502C 0090h	502C 1090h	502C 2090h
92h	16	ADC_CFG_ADCPPB2STAMP	502C 0092h	502C 1092h	502C 2092h
94h	16	ADC_CFG_ADCPPB2OFFCAL	502C 0094h	502C 1094h	502C 2094h
96h	16	ADC_CFG_ADCPPB2OFFREF	502C 0096h	502C 1096h	502C 2096h
98h	32	ADC_CFG_ADCPPB2TRIPHI	502C 0098h	502C 1098h	502C 2098h
9Ch	32	ADC_CFG_ADCPPB2TRIPLO	502C 009Ch	502C 109Ch	502C 209Ch
A0h	16	ADC_CFG_ADCPPB3CONFIG	502C 00A0h	502C 10A0h	502C 20A0h
A2h	16	ADC_CFG_ADCPPB3STAMP	502C 00A2h	502C 10A2h	502C 20A2h
A4h	16	ADC_CFG_ADCPPB3OFFCAL	502C 00A4h	502C 10A4h	502C 20A4h
A6h	16	ADC_CFG_ADCPPB3OFFREF	502C 00A6h	502C 10A6h	502C 20A6h
A8h	32	ADC_CFG_ADCPPB3TRIPHI	502C 00A8h	502C 10A8h	502C 20A8h
ACh	32	ADC_CFG_ADCPPB3TRIPLO	502C 00ACh	502C 10ACh	502C 20ACh
B0h	16	ADC_CFG_ADCPPB4CONFIG	502C 00B0h	502C 10B0h	502C 20B0h
B2h	16	ADC_CFG_ADCPPB4STAMP	502C 00B2h	502C 10B2h	502C 20B2h
B4h	16	ADC_CFG_ADCPPB4OFFCAL	502C 00B4h	502C 10B4h	502C 20B4h
B6h	16	ADC_CFG_ADCPPB4OFFREF	502C 00B6h	502C 10B6h	502C 20B6h
B8h	32	ADC_CFG_ADCPPB4TRIPHI	502C 00B8h	502C 10B8h	502C 20B8h
BCh	32	ADC_CFG_ADCPPB4TRIPLO	502C 00BCh	502C 10BCh	502C 20BCh
C0h	32	ADC_CFG_ADCSAFECHECKRESEN	502C 00C0h	502C 10C0h	502C 20C0h
DEh	16	ADC_CFG_ADCINTCYCLE	502C 00DEh	502C 10DEh	502C 20DEh
FAh	16	ADC_CFG_ADCREV2	502C 00FAh	502C 10FAh	502C 20FAh
FCh	32	ADC_CFG_ADCINLTRIMCTL	502C 00FCh	502C 10FCh	502C 20FCh
100h	32	ADC_CFG_REP1CTL	502C 0100h	502C 1100h	502C 2100h
104h	32	ADC_CFG_REP1N	502C 0104h	502C 1104h	502C 2104h
108h	32	ADC_CFG_REP1PHASE	502C 0108h	502C 1108h	502C 2108h
10Ch	32	ADC_CFG_REP1SPREAD	502C 010Ch	502C 110Ch	502C 210Ch
110h	16	ADC_CFG_REP1FRC	502C 0110h	502C 1110h	502C 2110h
120h	32	ADC_CFG_REP2CTL	502C 0120h	502C 1120h	502C 2120h
124h	32	ADC_CFG_REP2N	502C 0124h	502C 1124h	502C 2124h
128h	32	ADC_CFG_REP2PHASE	502C 0128h	502C 1128h	502C 2128h

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Table 3-3. ADC_CFG Registers, Base Address=502C 0000h, Length=256 (continued)

Offset	Length	Register Name	ADC0_G0_G5 Physical Address	ADC1_G0_G5 Physical Address	ADC2_G0_G5 Physical Address
12Ch	32	ADC_CFG_REP2SPREAD	502C 012Ch	502C 112Ch	502C 212Ch
130h	16	ADC_CFG_REP2FRC	502C 0130h	502C 1130h	502C 2130h
140h	16	ADC_CFG_ADCPPB1LIMIT	502C 0140h	502C 1140h	502C 2140h
144h	16	ADC_CFG_ADCPPBP1PCOUNT	502C 0144h	502C 1144h	502C 2144h
148h	16	ADC_CFG_ADCPPB1CONFIG2	502C 0148h	502C 1148h	502C 2148h
14Ch	32	ADC_CFG_ADCPPB1PSUM	502C 014Ch	502C 114Ch	502C 214Ch
150h	32	ADC_CFG_ADCPPB1PMAX	502C 0150h	502C 1150h	502C 2150h
154h	16	ADC_CFG_ADCPPB1PMAXI	502C 0154h	502C 1154h	502C 2154h
158h	32	ADC_CFG_ADCPPB1PMIN	502C 0158h	502C 1158h	502C 2158h
15Ch	16	ADC_CFG_ADCPPB1PMINI	502C 015Ch	502C 115Ch	502C 215Ch
160h	32	ADC_CFG_ADCPPB1TRIPLO2	502C 0160h	502C 1160h	502C 2160h
174h	16	ADC_CFG_ADCPPB2LIMIT	502C 0174h	502C 1174h	502C 2174h
178h	16	ADC_CFG_ADCPPBP2PCOUNT	502C 0178h	502C 1178h	502C 2178h
17Ch	16	ADC_CFG_ADCPPB2CONFIG2	502C 017Ch	502C 117Ch	502C 217Ch
180h	32	ADC_CFG_ADCPPB2PSUM	502C 0180h	502C 1180h	502C 2180h
184h	32	ADC_CFG_ADCPPB2PMAX	502C 0184h	502C 1184h	502C 2184h
188h	16	ADC_CFG_ADCPPB2PMAXI	502C 0188h	502C 1188h	502C 2188h
18Ch	32	ADC_CFG_ADCPPB2PMIN	502C 018Ch	502C 118Ch	502C 218Ch
190h	16	ADC_CFG_ADCPPB2PMINI	502C 0190h	502C 1190h	502C 2190h
194h	32	ADC_CFG_ADCPPB2TRIPLO2	502C 0194h	502C 1194h	502C 2194h
1A8h	16	ADC_CFG_ADCPPB3LIMIT	502C 01A8h	502C 11A8h	502C 21A8h
1ACh	16	ADC_CFG_ADCPPBP3PCOUNT	502C 01ACh	502C 11ACh	502C 21ACh
1B0h	16	ADC_CFG_ADCPPB3CONFIG2	502C 01B0h	502C 11B0h	502C 21B0h
1B4h	32	ADC_CFG_ADCPPB3PSUM	502C 01B4h	502C 11B4h	502C 21B4h
1B8h	32	ADC_CFG_ADCPPB3PMAX	502C 01B8h	502C 11B8h	502C 21B8h
1BCh	16	ADC_CFG_ADCPPB3PMAXI	502C 01BCh	502C 11BCh	502C 21BCh
1C0h	32	ADC_CFG_ADCPPB3PMIN	502C 01C0h	502C 11C0h	502C 21C0h
1C4h	16	ADC_CFG_ADCPPB3PMINI	502C 01C4h	502C 11C4h	502C 21C4h
1C8h	32	ADC_CFG_ADCPPB3TRIPLO2	502C 01C8h	502C 11C8h	502C 21C8h
1DCh	16	ADC_CFG_ADCPPB4LIMIT	502C 01DCh	502C 11DCh	502C 21DCh
1E0h	16	ADC_CFG_ADCPPBP4PCOUNT	502C 01E0h	502C 11E0h	502C 21E0h
1E4h	16	ADC_CFG_ADCPPB4CONFIG2	502C 01E4h	502C 11E4h	502C 21E4h
1E8h	32	ADC_CFG_ADCPPB4PSUM	502C 01E8h	502C 11E8h	502C 21E8h
1ECh	32	ADC_CFG_ADCPPB4PMAX	502C 01ECh	502C 11ECh	502C 21ECh
1F0h	16	ADC_CFG_ADCPPB4PMAXI	502C 01F0h	502C 11F0h	502C 21F0h
1F4h	32	ADC_CFG_ADCPPB4PMIN	502C 01F4h	502C 11F4h	502C 21F4h
1F8h	16	ADC_CFG_ADCPPB4PMINI	502C 01F8h	502C 11F8h	502C 21F8h
1FCh	32	ADC_CFG_ADCPPB4TRIPLO2	502C 01FCh	502C 11FCh	502C 21FCh

Table 3-4. ADC_CFG Registers, Base Address=502C 0000h, Length=256

Offset	Length	Register Name	ADC3_G0_G5 Physical Address	ADC4_G0_G5 Physical Address
0h	16	ADC_CFG_ADCCTL1	502C 3000h	502C 4000h
2h	16	ADC_CFG_ADCCTL2	502C 3002h	502C 4002h
4h	16	ADC_CFG_ADCBURSTCTL	502C 3004h	502C 4004h
6h	16	ADC_CFG_ADCINTFLG	502C 3006h	502C 4006h

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Table 3-4. ADC_CFG Registers, Base Address=502C 0000h, Length=256 (continued)

Offset	Length	Register Name	ADC3_G0_G5 Physical Address	ADC4_G0_G5 Physical Address
8h	16	ADC_CFG_ADCINTFLGCLR	502C 3008h	502C 4008h
Ah	16	ADC_CFG_ADCINTOVF	502C 300Ah	502C 400Ah
Ch	16	ADC_CFG_ADCINTOVFCLR	502C 300Ch	502C 400Ch
Eh	16	ADC_CFG_ADCINTSEL1N2	502C 300Eh	502C 400Eh
10h	16	ADC_CFG_ADCINTSEL3N4	502C 3010h	502C 4010h
12h	16	ADC_CFG_ADCSOCPRICTL	502C 3012h	502C 4012h
14h	16	ADC_CFG_ADCINTSOCSEL1	502C 3014h	502C 4014h
16h	16	ADC_CFG_ADCINTSOCSEL2	502C 3016h	502C 4016h
18h	16	ADC_CFG_ADCSOCFLG1	502C 3018h	502C 4018h
1Ah	16	ADC_CFG_ADCSOCFRC1	502C 301Ah	502C 401Ah
1Ch	16	ADC_CFG_ADCSOCOVF1	502C 301Ch	502C 401Ch
1Eh	16	ADC_CFG_ADCSOCOVFCLR1	502C 301Eh	502C 401Eh
20h	32	ADC_CFG_ADCSOC0CTL	502C 3020h	502C 4020h
24h	32	ADC_CFG_ADCSOC1CTL	502C 3024h	502C 4024h
28h	32	ADC_CFG_ADCSOC2CTL	502C 3028h	502C 4028h
2Ch	32	ADC_CFG_ADCSOC3CTL	502C 302Ch	502C 402Ch
30h	32	ADC_CFG_ADCSOC4CTL	502C 3030h	502C 4030h
34h	32	ADC_CFG_ADCSOC5CTL	502C 3034h	502C 4034h
38h	32	ADC_CFG_ADCSOC6CTL	502C 3038h	502C 4038h
3Ch	32	ADC_CFG_ADCSOC7CTL	502C 303Ch	502C 403Ch
40h	32	ADC_CFG_ADCSOC8CTL	502C 3040h	502C 4040h
44h	32	ADC_CFG_ADCSOC9CTL	502C 3044h	502C 4044h
48h	32	ADC_CFG_ADCSOC10CTL	502C 3048h	502C 4048h
4Ch	32	ADC_CFG_ADCSOC11CTL	502C 304Ch	502C 404Ch
50h	32	ADC_CFG_ADCSOC12CTL	502C 3050h	502C 4050h
54h	32	ADC_CFG_ADCSOC13CTL	502C 3054h	502C 4054h
58h	32	ADC_CFG_ADCSOC14CTL	502C 3058h	502C 4058h
5Ch	32	ADC_CFG_ADCSOC15CTL	502C 305Ch	502C 405Ch
60h	16	ADC_CFG_ADCEVTSTAT	502C 3060h	502C 4060h
64h	16	ADC_CFG_ADCEVTCLR	502C 3064h	502C 4064h
68h	16	ADC_CFG_ADCEVTSEL	502C 3068h	502C 4068h
6Ch	16	ADC_CFG_ADCEVTINTSEL	502C 306Ch	502C 406Ch
72h	16	ADC_CFG_ADCCOUNTER	502C 3072h	502C 4072h
74h	16	ADC_CFG_ADCREV	502C 3074h	502C 4074h
80h	16	ADC_CFG_ADCPPB1CONFIG	502C 3080h	502C 4080h
82h	16	ADC_CFG_ADCPPB1STAMP	502C 3082h	502C 4082h
84h	16	ADC_CFG_ADCPPB1OFFCAL	502C 3084h	502C 4084h
86h	16	ADC_CFG_ADCPPB1OFFREF	502C 3086h	502C 4086h
88h	32	ADC_CFG_ADCPPB1TRIPHI	502C 3088h	502C 4088h
8Ch	32	ADC_CFG_ADCPPB1TRIPLO	502C 308Ch	502C 408Ch
90h	16	ADC_CFG_ADCPPB2CONFIG	502C 3090h	502C 4090h
92h	16	ADC_CFG_ADCPPB2STAMP	502C 3092h	502C 4092h
94h	16	ADC_CFG_ADCPPB2OFFCAL	502C 3094h	502C 4094h
96h	16	ADC_CFG_ADCPPB2OFFREF	502C 3096h	502C 4096h
98h	32	ADC_CFG_ADCPPB2TRIPHI	502C 3098h	502C 4098h
9Ch	32	ADC_CFG_ADCPPB2TRIPLO	502C 309Ch	502C 409Ch

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Table 3-4. ADC_CFG Registers, Base Address=502C 0000h, Length=256 (continued)

Offset	Length	Register Name	ADC3_G0_G5 Physical Address	ADC4_G0_G5 Physical Address
A0h	16	ADC_CFG_ADCPPB3CONFIG	502C 30A0h	502C 40A0h
A2h	16	ADC_CFG_ADCPPB3STAMP	502C 30A2h	502C 40A2h
A4h	16	ADC_CFG_ADCPPB3OFFCAL	502C 30A4h	502C 40A4h
A6h	16	ADC_CFG_ADCPPB3OFFREF	502C 30A6h	502C 40A6h
A8h	32	ADC_CFG_ADCPPB3TRIPHI	502C 30A8h	502C 40A8h
ACh	32	ADC_CFG_ADCPPB3TRIPLO	502C 30ACh	502C 40ACh
B0h	16	ADC_CFG_ADCPPB4CONFIG	502C 30B0h	502C 40B0h
B2h	16	ADC_CFG_ADCPPB4STAMP	502C 30B2h	502C 40B2h
B4h	16	ADC_CFG_ADCPPB4OFFCAL	502C 30B4h	502C 40B4h
B6h	16	ADC_CFG_ADCPPB4OFFREF	502C 30B6h	502C 40B6h
B8h	32	ADC_CFG_ADCPPB4TRIPHI	502C 30B8h	502C 40B8h
BCh	32	ADC_CFG_ADCPPB4TRIPLO	502C 30BCh	502C 40BCh
C0h	32	ADC_CFG_ADCSAFECHECKRESEN	502C 30C0h	502C 40C0h
DEh	16	ADC_CFG_ADCINTCYCLE	502C 30DEh	502C 40DEh
FAh	16	ADC_CFG_ADCREV2	502C 30FAh	502C 40FAh
FCh	32	ADC_CFG_ADCINLTRIMCTL	502C 30FCh	502C 40FCh
100h	32	ADC_CFG_REP1CTL	502C 3100h	502C 4100h
104h	32	ADC_CFG_REP1N	502C 3104h	502C 4104h
108h	32	ADC_CFG_REP1PHASE	502C 3108h	502C 4108h
10Ch	32	ADC_CFG_REP1SPREAD	502C 310Ch	502C 410Ch
110h	16	ADC_CFG_REP1FRC	502C 3110h	502C 4110h
120h	32	ADC_CFG_REP2CTL	502C 3120h	502C 4120h
124h	32	ADC_CFG_REP2N	502C 3124h	502C 4124h
128h	32	ADC_CFG_REP2PHASE	502C 3128h	502C 4128h
12Ch	32	ADC_CFG_REP2SPREAD	502C 312Ch	502C 412Ch
130h	16	ADC_CFG_REP2FRC	502C 3130h	502C 4130h
140h	16	ADC_CFG_ADCPPB1LIMIT	502C 3140h	502C 4140h
144h	16	ADC_CFG_ADCPPBP1PCOUNT	502C 3144h	502C 4144h
148h	16	ADC_CFG_ADCPPB1CONFIG2	502C 3148h	502C 4148h
14Ch	32	ADC_CFG_ADCPPB1PSUM	502C 314Ch	502C 414Ch
150h	32	ADC_CFG_ADCPPB1PMAX	502C 3150h	502C 4150h
154h	16	ADC_CFG_ADCPPB1PMAXI	502C 3154h	502C 4154h
158h	32	ADC_CFG_ADCPPB1PMIN	502C 3158h	502C 4158h
15Ch	16	ADC_CFG_ADCPPB1PMINI	502C 315Ch	502C 415Ch
160h	32	ADC_CFG_ADCPPB1TRIPLO2	502C 3160h	502C 4160h
174h	16	ADC_CFG_ADCPPB2LIMIT	502C 3174h	502C 4174h
178h	16	ADC_CFG_ADCPPBP2PCOUNT	502C 3178h	502C 4178h
17Ch	16	ADC_CFG_ADCPPB2CONFIG2	502C 317Ch	502C 417Ch
180h	32	ADC_CFG_ADCPPB2PSUM	502C 3180h	502C 4180h
184h	32	ADC_CFG_ADCPPB2PMAX	502C 3184h	502C 4184h
188h	16	ADC_CFG_ADCPPB2PMAXI	502C 3188h	502C 4188h
18Ch	32	ADC_CFG_ADCPPB2PMIN	502C 318Ch	502C 418Ch
190h	16	ADC_CFG_ADCPPB2PMINI	502C 3190h	502C 4190h
194h	32	ADC_CFG_ADCPPB2TRIPLO2	502C 3194h	502C 4194h
1A8h	16	ADC_CFG_ADCPPB3LIMIT	502C 31A8h	502C 41A8h
1ACh	16	ADC_CFG_ADCPPBP3PCOUNT	502C 31ACh	502C 41ACh

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Table 3-4. ADC_CFG Registers, Base Address=502C 0000h, Length=256 (continued)

Offset	Length	Register Name	ADC3_G0_G5 Physical Address	ADC4_G0_G5 Physical Address
1B0h	16	ADC_CFG_ADCPPB3CONFIG2	502C 31B0h	502C 41B0h
1B4h	32	ADC_CFG_ADCPPB3PSUM	502C 31B4h	502C 41B4h
1B8h	32	ADC_CFG_ADCPPB3PMAX	502C 31B8h	502C 41B8h
1BCh	16	ADC_CFG_ADCPPB3PMAXI	502C 31BCh	502C 41BCh
1C0h	32	ADC_CFG_ADCPPB3PMIN	502C 31C0h	502C 41C0h
1C4h	16	ADC_CFG_ADCPPB3PMINI	502C 31C4h	502C 41C4h
1C8h	32	ADC_CFG_ADCPPB3TRIPLO2	502C 31C8h	502C 41C8h
1DCh	16	ADC_CFG_ADCPPB4LIMIT	502C 31DCh	502C 41DCh
1E0h	16	ADC_CFG_ADCPPBP4PCOUNT	502C 31E0h	502C 41E0h
1E4h	16	ADC_CFG_ADCPPB4CONFIG2	502C 31E4h	502C 41E4h
1E8h	32	ADC_CFG_ADCPPB4PSUM	502C 31E8h	502C 41E8h
1ECh	32	ADC_CFG_ADCPPB4PMAX	502C 31ECh	502C 41ECh
1F0h	16	ADC_CFG_ADCPPB4PMAXI	502C 31F0h	502C 41F0h
1F4h	32	ADC_CFG_ADCPPB4PMIN	502C 31F4h	502C 41F4h
1F8h	16	ADC_CFG_ADCPPB4PMINI	502C 31F8h	502C 41F8h
1FCh	32	ADC_CFG_ADCPPB4TRIPLO2	502C 31FCh	502C 41FCh

3.2.2 ADC Registers

ADC Registers

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3.2.2.1 ADC_RESULTS_ADCRESULT0 Register

3.2.2.1.1 ADC_RESULTS_ADCRESULT0 Register (Offset = 0h) [reset = 0h]

ADC Result 0 Register.

Return to Summary Table

Table 3-5. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0000h
ADC1_G0_G5	5010 1000h
ADC2_G0_G5	5010 2000h
ADC3_G0_G5	5010 3000h
ADC4_G0_G5	5010 4000h

Figure 3-1. ADC_RESULTS_ADCRESULT0 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-6. ADC_RESULTS_ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 0 16-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field.

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3.2.2.2 ADC_RESULTS_ADCRESULT1 Register

3.2.2.2.1 ADC_RESULTS_ADCRESULT1 Register (Offset = 2h) [reset = 0h]

ADC Result 1 Register.

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Table 3-7. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0002h
ADC1_G0_G5	5010 1002h
ADC2_G0_G5	5010 2002h
ADC3_G0_G5	5010 3002h
ADC4_G0_G5	5010 4002h

Figure 3-2. ADC_RESULTS_ADCRESULT1 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-8. ADC_RESULTS_ADCRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 1 16-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field.

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3.2.2.3 ADC_RESULTS_ADCRESULT2 Register

3.2.2.3.1 ADC_RESULTS_ADCRESULT2 Register (Offset = 4h) [reset = 0h]

ADC Result 2 Register.

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Table 3-9. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0004h
ADC1_G0_G5	5010 1004h
ADC2_G0_G5	5010 2004h
ADC3_G0_G5	5010 3004h
ADC4_G0_G5	5010 4004h

Figure 3-3. ADC_RESULTS_ADCRESULT2 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-10. ADC_RESULTS_ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 2 16-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field.

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3.2.2.4 ADC_RESULTS_ADCRESULT3 Register

3.2.2.4.1 ADC_RESULTS_ADCRESULT3 Register (Offset = 6h) [reset = 0h]

ADC Result 3 Register.

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Table 3-11. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0006h
ADC1_G0_G5	5010 1006h
ADC2_G0_G5	5010 2006h
ADC3_G0_G5	5010 3006h
ADC4_G0_G5	5010 4006h

Figure 3-4. ADC_RESULTS_ADCRESULT3 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-12. ADC_RESULTS_ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 3 16-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field.

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3.2.2.5 ADC_RESULTS_ADCRESULT4 Register

3.2.2.5.1 ADC_RESULTS_ADCRESULT4 Register (Offset = 8h) [reset = 0h]

ADC Result 4 Register.

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Table 3-13. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0008h
ADC1_G0_G5	5010 1008h
ADC2_G0_G5	5010 2008h
ADC3_G0_G5	5010 3008h
ADC4_G0_G5	5010 4008h

Figure 3-5. ADC_RESULTS_ADCRESULT4 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-14. ADC_RESULTS_ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 4 16-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field.

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3.2.2.6 ADC_RESULTS_ADCRESULT5 Register

3.2.2.6.1 ADC_RESULTS_ADCRESULT5 Register (Offset = Ah) [reset = 0h]

ADC Result 5 Register.

Return to Summary Table

Table 3-15. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 000Ah
ADC1_G0_G5	5010 100Ah
ADC2_G0_G5	5010 200Ah
ADC3_G0_G5	5010 300Ah
ADC4_G0_G5	5010 400Ah

Figure 3-6. ADC_RESULTS_ADCRESULT5 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-16. ADC_RESULTS_ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 5 16-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field.

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3.2.2.7 ADC_RESULTS_ADCRESULT6 Register

3.2.2.7.1 ADC_RESULTS_ADCRESULT6 Register (Offset = Ch) [reset = 0h]

ADC Result 6 Register.

Return to Summary Table

Table 3-17. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 000Ch
ADC1_G0_G5	5010 100Ch
ADC2_G0_G5	5010 200Ch
ADC3_G0_G5	5010 300Ch
ADC4_G0_G5	5010 400Ch

Figure 3-7. ADC_RESULTS_ADCRESULT6 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-18. ADC_RESULTS_ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 6 16-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field.

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3.2.2.8 ADC_RESULTS_ADCRESULT7 Register

3.2.2.8.1 ADC_RESULTS_ADCRESULT7 Register (Offset = Eh) [reset = 0h]

ADC Result 7 Register.

Return to Summary Table

Table 3-19. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 000Eh
ADC1_G0_G5	5010 100Eh
ADC2_G0_G5	5010 200Eh
ADC3_G0_G5	5010 300Eh
ADC4_G0_G5	5010 400Eh

Figure 3-8. ADC_RESULTS_ADCRESULT7 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-20. ADC_RESULTS_ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 7 16-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field.

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3.2.2.9 ADC_RESULTS_ADCRESULT8 Register

3.2.2.9.1 ADC_RESULTS_ADCRESULT8 Register (Offset = 10h) [reset = 0h]

ADC Result 8 Register.

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Table 3-21. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0010h
ADC1_G0_G5	5010 1010h
ADC2_G0_G5	5010 2010h
ADC3_G0_G5	5010 3010h
ADC4_G0_G5	5010 4010h

Figure 3-9. ADC_RESULTS_ADCRESULT8 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-22. ADC_RESULTS_ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 8 16-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field.

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3.2.2.10 ADC_RESULTS_ADCRESULT9 Register

3.2.2.10.1 ADC_RESULTS_ADCRESULT9 Register (Offset = 12h) [reset = 0h]

ADC Result 9 Register.

Return to Summary Table

Table 3-23. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0012h
ADC1_G0_G5	5010 1012h
ADC2_G0_G5	5010 2012h
ADC3_G0_G5	5010 3012h
ADC4_G0_G5	5010 4012h

Figure 3-10. ADC_RESULTS_ADCRESULT9 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-24. ADC_RESULTS_ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 9 16-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field.

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3.2.2.11 ADC_RESULTS_ADCRESULT10 Register

3.2.2.11.1 ADC_RESULTS_ADCRESULT10 Register (Offset = 14h) [reset = 0h]

ADC Result 10 Register.

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Table 3-25. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0014h
ADC1_G0_G5	5010 1014h
ADC2_G0_G5	5010 2014h
ADC3_G0_G5	5010 3014h
ADC4_G0_G5	5010 4014h

Figure 3-11. ADC_RESULTS_ADCRESULT10 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-26. ADC_RESULTS_ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 10 16-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field.

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3.2.2.12 ADC_RESULTS_ADCRESULT11 Register

3.2.2.12.1 ADC_RESULTS_ADCRESULT11 Register (Offset = 16h) [reset = 0h]

ADC Result 11 Register.

Return to Summary Table

Table 3-27. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0016h
ADC1_G0_G5	5010 1016h
ADC2_G0_G5	5010 2016h
ADC3_G0_G5	5010 3016h
ADC4_G0_G5	5010 4016h

Figure 3-12. ADC_RESULTS_ADCRESULT11 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-28. ADC_RESULTS_ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 11 16-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field.

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3.2.2.13 ADC_RESULTS_ADCRESULT12 Register

3.2.2.13.1 ADC_RESULTS_ADCRESULT12 Register (Offset = 18h) [reset = 0h]

ADC Result 12 Register.

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Table 3-29. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0018h
ADC1_G0_G5	5010 1018h
ADC2_G0_G5	5010 2018h
ADC3_G0_G5	5010 3018h
ADC4_G0_G5	5010 4018h

Figure 3-13. ADC_RESULTS_ADCRESULT12 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-30. ADC_RESULTS_ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 12 16-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field.

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3.2.2.14 ADC_RESULTS_ADCRESULT13 Register

3.2.2.14.1 ADC_RESULTS_ADCRESULT13 Register (Offset = 1Ah) [reset = 0h]

ADC Result 13 Register.

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Table 3-31. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 001Ah
ADC1_G0_G5	5010 101Ah
ADC2_G0_G5	5010 201Ah
ADC3_G0_G5	5010 301Ah
ADC4_G0_G5	5010 401Ah

Figure 3-14. ADC_RESULTS_ADCRESULT13 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-32. ADC_RESULTS_ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 13 16-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field.

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3.2.2.15 ADC_RESULTS_ADCRESULT14 Register

3.2.2.15.1 ADC_RESULTS_ADCRESULT14 Register (Offset = 1Ch) [reset = 0h]

ADC Result 14 Register.

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Table 3-33. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 001Ch
ADC1_G0_G5	5010 101Ch
ADC2_G0_G5	5010 201Ch
ADC3_G0_G5	5010 301Ch
ADC4_G0_G5	5010 401Ch

Figure 3-15. ADC_RESULTS_ADCRESULT14 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-34. ADC_RESULTS_ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 14 16-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field.

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3.2.2.16 ADC_RESULTS_ADCRESULT15 Register

3.2.2.16.1 ADC_RESULTS_ADCRESULT15 Register (Offset = 1Eh) [reset = 0h]

ADC Result 15 Register.

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Table 3-35. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 001Eh
ADC1_G0_G5	5010 101Eh
ADC2_G0_G5	5010 201Eh
ADC3_G0_G5	5010 301Eh
ADC4_G0_G5	5010 401Eh

Figure 3-16. ADC_RESULTS_ADCRESULT15 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-36. ADC_RESULTS_ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 15 16-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field.

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3.2.2.17 ADC_RESULTS_ADCPPB1RESULT Register

3.2.2.17.1 ADC_RESULTS_ADCPPB1RESULT Register (Offset = 20h) [reset = 0h]

ADC Post Processing Block 1 Result Register.

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Table 3-37. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0020h
ADC1_G0_G5	5010 1020h
ADC2_G0_G5	5010 2020h
ADC3_G0_G5	5010 3020h
ADC4_G0_G5	5010 4020h

Figure 3-17. ADC_RESULTS_ADCPPB1RESULT Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							
R							
0h							
15	14	13	12	11	10	9	8
PPBRESULT							
R							
0h							
7	6	5	4	3	2	1	0
PPBRESULT							
R							
0h							

Table 3-38. ADC_RESULTS_ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15:0	PPBRESULT	R	0h	ADC Post Processing Block Result 1 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information]. If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.2.2.18 ADC_RESULTS_ADCPPB2RESULT Register

3.2.2.18.1 ADC_RESULTS_ADCPPB2RESULT Register (Offset = 24h) [reset = 0h]

ADC Post Processing Block 2 Result Register.

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Table 3-39. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0024h
ADC1_G0_G5	5010 1024h
ADC2_G0_G5	5010 2024h
ADC3_G0_G5	5010 3024h
ADC4_G0_G5	5010 4024h

Figure 3-18. ADC_RESULTS_ADCPPB2RESULT Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							
R							
0h							
15	14	13	12	11	10	9	8
PPBRESULT							
R							
0h							
7	6	5	4	3	2	1	0
PPBRESULT							
R							
0h							

Table 3-40. ADC_RESULTS_ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15:0	PPBRESULT	R	0h	ADC Post Processing Block Result 2 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information]. If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.2.2.19 ADC_RESULTS_ADCPPB3RESULT Register

3.2.2.19.1 ADC_RESULTS_ADCPPB3RESULT Register (Offset = 28h) [reset = 0h]

ADC Post Processing Block 3 Result Register.

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Table 3-41. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0028h
ADC1_G0_G5	5010 1028h
ADC2_G0_G5	5010 2028h
ADC3_G0_G5	5010 3028h
ADC4_G0_G5	5010 4028h

Figure 3-19. ADC_RESULTS_ADCPPB3RESULT Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							
R							
0h							
15	14	13	12	11	10	9	8
PPBRESULT							
R							
0h							
7	6	5	4	3	2	1	0
PPBRESULT							
R							
0h							

Table 3-42. ADC_RESULTS_ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15:0	PPBRESULT	R	0h	ADC Post Processing Block Result 3 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information]. If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.2.2.20 ADC_RESULTS_ADCPPB4RESULT Register

3.2.2.20.1 ADC_RESULTS_ADCPPB4RESULT Register (Offset = 2Ch) [reset = 0h]

ADC Post Processing Block 4 Result Register.

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Table 3-43. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 002Ch
ADC1_G0_G5	5010 102Ch
ADC2_G0_G5	5010 202Ch
ADC3_G0_G5	5010 302Ch
ADC4_G0_G5	5010 402Ch

Figure 3-20. ADC_RESULTS_ADCPPB4RESULT Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							
R							
0h							
15	14	13	12	11	10	9	8
PPBRESULT							
R							
0h							
7	6	5	4	3	2	1	0
PPBRESULT							
R							
0h							

Table 3-44. ADC_RESULTS_ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15:0	PPBRESULT	R	0h	ADC Post Processing Block Result 4 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information]. If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.2.2.21 ADC_RESULTS_ADCPPB1SUM Register

3.2.2.21.1 ADC_RESULTS_ADCPPB1SUM Register (Offset = 30h) [reset = 0h]

ADC PPB 1 Final Sum Result Register.

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Table 3-45. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0030h
ADC1_G0_G5	5010 1030h
ADC2_G0_G5	5010 2030h
ADC3_G0_G5	5010 3030h
ADC4_G0_G5	5010 4030h

Figure 3-21. ADC_RESULTS_ADCPPB1SUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SUM							
R							
0h							
15	14	13	12	11	10	9	8
SUM							
R							
0h							
7	6	5	4	3	2	1	0
SUM							
R							
0h							

Table 3-46. ADC_RESULTS_ADCPPB1SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	SUM	R	0h	Post Processing Block 1 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.22 ADC_RESULTS_ADCPPB1COUNT Register

3.2.2.22.1 ADC_RESULTS_ADCPPB1COUNT Register (Offset = 34h) [reset = 0h]

ADC PPB1 Final Conversion Count Register.

Return to Summary Table

Table 3-47. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0034h
ADC1_G0_G5	5010 1034h
ADC2_G0_G5	5010 2034h
ADC3_G0_G5	5010 3034h
ADC4_G0_G5	5010 4034h

Figure 3-22. ADC_RESULTS_ADCPPB1COUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						COUNT	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 3-48. ADC_RESULTS_ADCPPB1COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	COUNT	R	0h	Post Processing Block 1 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.23 ADC_RESULTS_ADCPPB2SUM Register

3.2.2.23.1 ADC_RESULTS_ADCPPB2SUM Register (Offset = 38h) [reset = 0h]

ADC PPB 2 Final Sum Result Register.

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Table 3-49. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0038h
ADC1_G0_G5	5010 1038h
ADC2_G0_G5	5010 2038h
ADC3_G0_G5	5010 3038h
ADC4_G0_G5	5010 4038h

Figure 3-23. ADC_RESULTS_ADCPPB2SUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SUM							
R							
0h							
15	14	13	12	11	10	9	8
SUM							
R							
0h							
7	6	5	4	3	2	1	0
SUM							
R							
0h							

Table 3-50. ADC_RESULTS_ADCPPB2SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	SUM	R	0h	Post Processing Block 2 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.24 ADC_RESULTS_ADCPPB2COUNT Register

3.2.2.24.1 ADC_RESULTS_ADCPPB2COUNT Register (Offset = 3Ch) [reset = 0h]

ADC PPB2 Final Conversion Count Register.

Return to Summary Table

Table 3-51. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 003Ch
ADC1_G0_G5	5010 103Ch
ADC2_G0_G5	5010 203Ch
ADC3_G0_G5	5010 303Ch
ADC4_G0_G5	5010 403Ch

Figure 3-24. ADC_RESULTS_ADCPPB2COUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						COUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 3-52. ADC_RESULTS_ADCPPB2COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	COUNT	R	0h	Post Processing Block 2 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.25 ADC_RESULTS_ADCPPB3SUM Register

3.2.2.25.1 ADC_RESULTS_ADCPPB3SUM Register (Offset = 40h) [reset = 0h]

ADC PPB 3 Final Sum Result Register.

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Table 3-53. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0040h
ADC1_G0_G5	5010 1040h
ADC2_G0_G5	5010 2040h
ADC3_G0_G5	5010 3040h
ADC4_G0_G5	5010 4040h

Figure 3-25. ADC_RESULTS_ADCPPB3SUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SUM							
R							
0h							
15	14	13	12	11	10	9	8
SUM							
R							
0h							
7	6	5	4	3	2	1	0
SUM							
R							
0h							

Table 3-54. ADC_RESULTS_ADCPPB3SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	SUM	R	0h	Post Processing Block 3 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.26 ADC_RESULTS_ADCPPB3COUNT Register

3.2.2.26.1 ADC_RESULTS_ADCPPB3COUNT Register (Offset = 44h) [reset = 0h]

ADC PPB3 Final Conversion Count Register.

Return to Summary Table

Table 3-55. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0044h
ADC1_G0_G5	5010 1044h
ADC2_G0_G5	5010 2044h
ADC3_G0_G5	5010 3044h
ADC4_G0_G5	5010 4044h

Figure 3-26. ADC_RESULTS_ADCPPB3COUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						COUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 3-56. ADC_RESULTS_ADCPPB3COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	COUNT	R	0h	Post Processing Block 3 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.27 ADC_RESULTS_ADCPPB4SUM Register

3.2.2.27.1 ADC_RESULTS_ADCPPB4SUM Register (Offset = 48h) [reset = 0h]

ADC PPB 4 Final Sum Result Register.

Return to Summary Table

Table 3-57. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0048h
ADC1_G0_G5	5010 1048h
ADC2_G0_G5	5010 2048h
ADC3_G0_G5	5010 3048h
ADC4_G0_G5	5010 4048h

Figure 3-27. ADC_RESULTS_ADCPPB4SUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SUM							
R							
0h							
15	14	13	12	11	10	9	8
SUM							
R							
0h							
7	6	5	4	3	2	1	0
SUM							
R							
0h							

Table 3-58. ADC_RESULTS_ADCPPB4SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	SUM	R	0h	Post Processing Block 4 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.28 ADC_RESULTS_ADCPPB4COUNT Register

3.2.2.28.1 ADC_RESULTS_ADCPPB4COUNT Register (Offset = 4Ch) [reset = 0h]

ADC PPB4 Final Conversion Count Register.

Return to Summary Table

Table 3-59. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 004Ch
ADC1_G0_G5	5010 104Ch
ADC2_G0_G5	5010 204Ch
ADC3_G0_G5	5010 304Ch
ADC4_G0_G5	5010 404Ch

Figure 3-28. ADC_RESULTS_ADCPPB4COUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						COUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 3-60. ADC_RESULTS_ADCPPB4COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	COUNT	R	0h	Post Processing Block 4 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.29 ADC_RESULTS_ADCPPB1MAX Register

3.2.2.29.1 ADC_RESULTS_ADCPPB1MAX Register (Offset = 50h) [reset = 0h]

ADC PPB 1 Final Max Result Register.

Return to Summary Table

Table 3-61. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0050h
ADC1_G0_G5	5010 1050h
ADC2_G0_G5	5010 2050h
ADC3_G0_G5	5010 3050h
ADC4_G0_G5	5010 4050h

Figure 3-29. ADC_RESULTS_ADCPPB1MAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MAX
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAX							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX							
R							
0h							

Table 3-62. ADC_RESULTS_ADCPPB1MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MAX	R	0h	Post Processing Block 1 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.30 ADC_RESULTS_ADCPPB1MAXI Register

3.2.2.30.1 ADC_RESULTS_ADCPPB1MAXI Register (Offset = 54h) [reset = 0h]

ADC PPB 1 Final Max Index Result Register.

Return to Summary Table

Table 3-63. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0054h
ADC1_G0_G5	5010 1054h
ADC2_G0_G5	5010 2054h
ADC3_G0_G5	5010 3054h
ADC4_G0_G5	5010 4054h

Figure 3-30. ADC_RESULTS_ADCPPB1MAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MAXI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
MAXI							
R							
0h							

Table 3-64. ADC_RESULTS_ADCPPB1MAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MAXI	R	0h	Post Processing Block 1 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMAXI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.31 ADC_RESULTS_ADCPPB1MIN Register

3.2.2.31.1 ADC_RESULTS_ADCPPB1MIN Register (Offset = 58h) [reset = 0h]

ADC PPB 1 Final Min Result Register.

Return to Summary Table

Table 3-65. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0058h
ADC1_G0_G5	5010 1058h
ADC2_G0_G5	5010 2058h
ADC3_G0_G5	5010 3058h
ADC4_G0_G5	5010 4058h

Figure 3-31. ADC_RESULTS_ADCPPB1MIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MIN							
R							
0h							

Table 3-66. ADC_RESULTS_ADCPPB1MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MIN	R	0h	Post Processing Block 1 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.32 ADC_RESULTS_ADCPPB1MINI Register

3.2.2.32.1 ADC_RESULTS_ADCPPB1MINI Register (Offset = 5Ch) [reset = 0h]

ADC PPB 1 Final Min Index Result Register.

Return to Summary Table

Table 3-67. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 005Ch
ADC1_G0_G5	5010 105Ch
ADC2_G0_G5	5010 205Ch
ADC3_G0_G5	5010 305Ch
ADC4_G0_G5	5010 405Ch

Figure 3-32. ADC_RESULTS_ADCPPB1MINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MINI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MINI							
R							
0h							

Table 3-68. ADC_RESULTS_ADCPPB1MINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MINI	R	0h	Post Processing Block 1 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.33 ADC_RESULTS_ADCPPB2MAX Register

3.2.2.33.1 ADC_RESULTS_ADCPPB2MAX Register (Offset = 60h) [reset = 0h]

ADC PPB 2 Final Max Result Register.

Return to Summary Table

Table 3-69. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0060h
ADC1_G0_G5	5010 1060h
ADC2_G0_G5	5010 2060h
ADC3_G0_G5	5010 3060h
ADC4_G0_G5	5010 4060h

Figure 3-33. ADC_RESULTS_ADCPPB2MAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MAX
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAX							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX							
R							
0h							

Table 3-70. ADC_RESULTS_ADCPPB2MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MAX	R	0h	Post Processing Block 2 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.34 ADC_RESULTS_ADCPPB2MAXI Register

3.2.2.34.1 ADC_RESULTS_ADCPPB2MAXI Register (Offset = 64h) [reset = 0h]

ADC PPB 2 Final Max Index Result Register.

Return to Summary Table

Table 3-71. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0064h
ADC1_G0_G5	5010 1064h
ADC2_G0_G5	5010 2064h
ADC3_G0_G5	5010 3064h
ADC4_G0_G5	5010 4064h

Figure 3-34. ADC_RESULTS_ADCPPB2MAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAXI							
R							
0h							

Table 3-72. ADC_RESULTS_ADCPPB2MAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MAXI	R	0h	Post Processing Block 2 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMAXI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.35 ADC_RESULTS_ADCPPB2MIN Register

3.2.2.35.1 ADC_RESULTS_ADCPPB2MIN Register (Offset = 68h) [reset = 0h]

ADC PPB 2 Final Min Result Register.

Return to Summary Table

Table 3-73. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0068h
ADC1_G0_G5	5010 1068h
ADC2_G0_G5	5010 2068h
ADC3_G0_G5	5010 3068h
ADC4_G0_G5	5010 4068h

Figure 3-35. ADC_RESULTS_ADCPPB2MIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							MIN
R							R
0h							0h
15	14	13	12	11	10	9	8
MIN							
R							
0h							
7	6	5	4	3	2	1	0
MIN							
R							
0h							

Table 3-74. ADC_RESULTS_ADCPPB2MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MIN	R	0h	Post Processing Block 2 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.36 ADC_RESULTS_ADCPPB2MINI Register

3.2.2.36.1 ADC_RESULTS_ADCPPB2MINI Register (Offset = 6Ch) [reset = 0h]

ADC PPB 2 Final Min Index Result Register.

Return to Summary Table

Table 3-75. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 006Ch
ADC1_G0_G5	5010 106Ch
ADC2_G0_G5	5010 206Ch
ADC3_G0_G5	5010 306Ch
ADC4_G0_G5	5010 406Ch

Figure 3-36. ADC_RESULTS_ADCPPB2MINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MINI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
MINI							
R							
0h							

Table 3-76. ADC_RESULTS_ADCPPB2MINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MINI	R	0h	Post Processing Block 2 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.37 ADC_RESULTS_ADCPPB3MAX Register

3.2.2.37.1 ADC_RESULTS_ADCPPB3MAX Register (Offset = 70h) [reset = 0h]

ADC PPB 3 Final Max Result Register.

Return to Summary Table

Table 3-77. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0070h
ADC1_G0_G5	5010 1070h
ADC2_G0_G5	5010 2070h
ADC3_G0_G5	5010 3070h
ADC4_G0_G5	5010 4070h

Figure 3-37. ADC_RESULTS_ADCPPB3MAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MAX
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAX							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX							
R							
0h							

Table 3-78. ADC_RESULTS_ADCPPB3MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MAX	R	0h	Post Processing Block 3 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.38 ADC_RESULTS_ADCPPB3MAXI Register

3.2.2.38.1 ADC_RESULTS_ADCPPB3MAXI Register (Offset = 74h) [reset = 0h]

ADC PPB 3 Final Max Index Result Register.

Return to Summary Table

Table 3-79. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0074h
ADC1_G0_G5	5010 1074h
ADC2_G0_G5	5010 2074h
ADC3_G0_G5	5010 3074h
ADC4_G0_G5	5010 4074h

Figure 3-38. ADC_RESULTS_ADCPPB3MAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MAXI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
MAXI							
R							
0h							

Table 3-80. ADC_RESULTS_ADCPPB3MAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MAXI	R	0h	Post Processing Block 3 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMAXI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.39 ADC_RESULTS_ADCPPB3MIN Register

3.2.2.39.1 ADC_RESULTS_ADCPPB3MIN Register (Offset = 78h) [reset = 0h]

ADC PPB 3 Final Min Result Register.

Return to Summary Table

Table 3-81. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0078h
ADC1_G0_G5	5010 1078h
ADC2_G0_G5	5010 2078h
ADC3_G0_G5	5010 3078h
ADC4_G0_G5	5010 4078h

Figure 3-39. ADC_RESULTS_ADCPPB3MIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							MIN
R							R
0h							0h
15	14	13	12	11	10	9	8
MIN							
R							
0h							
7	6	5	4	3	2	1	0
MIN							
R							
0h							

Table 3-82. ADC_RESULTS_ADCPPB3MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MIN	R	0h	Post Processing Block 3 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.40 ADC_RESULTS_ADCPPB3MINI Register

3.2.2.40.1 ADC_RESULTS_ADCPPB3MINI Register (Offset = 7Ch) [reset = 0h]

ADC PPB 3 Final Min Index Result Register.

Return to Summary Table

Table 3-83. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 007Ch
ADC1_G0_G5	5010 107Ch
ADC2_G0_G5	5010 207Ch
ADC3_G0_G5	5010 307Ch
ADC4_G0_G5	5010 407Ch

Figure 3-40. ADC_RESULTS_ADCPPB3MINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MINI	
R						R	
0h						0h	

7	6	5	4	3	2	1	0
MINI							
R							
0h							

Table 3-84. ADC_RESULTS_ADCPPB3MINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MINI	R	0h	Post Processing Block 3 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.41 ADC_RESULTS_ADCPPB4MAX Register

3.2.2.41.1 ADC_RESULTS_ADCPPB4MAX Register (Offset = 80h) [reset = 0h]

ADC PPB 4 Final Max Result Register.

Return to Summary Table

Table 3-85. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0080h
ADC1_G0_G5	5010 1080h
ADC2_G0_G5	5010 2080h
ADC3_G0_G5	5010 3080h
ADC4_G0_G5	5010 4080h

Figure 3-41. ADC_RESULTS_ADCPPB4MAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MAX
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAX							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX							
R							
0h							

Table 3-86. ADC_RESULTS_ADCPPB4MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MAX	R	0h	Post Processing Block 4 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.42 ADC_RESULTS_ADCPPB4MAXI Register

3.2.2.42.1 ADC_RESULTS_ADCPPB4MAXI Register (Offset = 84h) [reset = 0h]

ADC PPB 4 Final Max Index Result Register.

Return to Summary Table

Table 3-87. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0084h
ADC1_G0_G5	5010 1084h
ADC2_G0_G5	5010 2084h
ADC3_G0_G5	5010 3084h
ADC4_G0_G5	5010 4084h

Figure 3-42. ADC_RESULTS_ADCPPB4MAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAXI							
R							
0h							

Table 3-88. ADC_RESULTS_ADCPPB4MAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MAXI	R	0h	Post Processing Block 4 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMAXI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.43 ADC_RESULTS_ADCPPB4MIN Register

3.2.2.43.1 ADC_RESULTS_ADCPPB4MIN Register (Offset = 88h) [reset = 0h]

ADC PPB 4 Final Min Result Register.

Return to Summary Table

Table 3-89. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 0088h
ADC1_G0_G5	5010 1088h
ADC2_G0_G5	5010 2088h
ADC3_G0_G5	5010 3088h
ADC4_G0_G5	5010 4088h

Figure 3-43. ADC_RESULTS_ADCPPB4MIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MIN							
R							
0h							

Table 3-90. ADC_RESULTS_ADCPPB4MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MIN	R	0h	Post Processing Block 4 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.44 ADC_RESULTS_ADCPPB4MINI Register

3.2.2.44.1 ADC_RESULTS_ADCPPB4MINI Register (Offset = 8Ch) [reset = 0h]

ADC PPB 4 Final Min Index Result Register.

Return to Summary Table

Table 3-91. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	5010 008Ch
ADC1_G0_G5	5010 108Ch
ADC2_G0_G5	5010 208Ch
ADC3_G0_G5	5010 308Ch
ADC4_G0_G5	5010 408Ch

Figure 3-44. ADC_RESULTS_ADCPPB4MINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MINI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
MINI							
R							
0h							

Table 3-92. ADC_RESULTS_ADCPPB4MINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MINI	R	0h	Post Processing Block 4 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.45 ADC_CFG_ADCCTL1 Register

3.2.2.45.1 ADC_CFG_ADCCTL1 Register (Offset = 0h) [reset = 0h]

ADC Control 1 Register.

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Table 3-93. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0000h
ADC1_G0_G5	502C 1000h
ADC2_G0_G5	502C 2000h
ADC3_G0_G5	502C 3000h
ADC4_G0_G5	502C 4000h

Figure 3-45. ADC_CFG_ADCCTL1 Name Register

15	14	13	12	11	10	9	8
TDMAEN	EXTMUXPRESELECTEN	ADCBSY	RESERVED_3	ADCBSYCHN			
R/W	R/W	R	R	R			
0h	0h	0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADCPWDNZ	RESERVED_2				INTPULSEPOS	RESERVED_1	
R/W	R				R/W	R	
0h	0h				0h	0h	

Table 3-94. ADC_CFG_ADCCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TDMAEN	R/W	0h	Enable Alternate DMA Timings. This bit controls when the DMA is triggered. 0 DMA is triggered at the same time as the CPU interrupt 1 DMA is always triggered at tDMA regardless or whether the ADC is in early interrupt mode or late interrupt mode
14	EXTMUXPRESELECTEN	R/W	0h	If th the ADC SOC sequence is deterministic, the ADCEXTMUX pins can be set earlier: at the end of the S+H window of the previous conversion instead of the beginning of the S+H window of the current conversion. This allows some of the external mux settling time to be pipelined with the previous conversion's conversion time. However, this will not work in the case where high-priority SOCs can arrive asynchronously. 0 ADCEXTMUX pins only change at beginning of S+H window 1 ADCEXTMUX pins are set after the end of S+H window based on pending SOCs
13	ADCBSY	R	0h	ADC Busy. Set when ADC SOC is generated, cleared by hardware four ADC clocks after negative edge of S/H pulse. Used by the ADC state machine to determine if ADC is available to sample. 0 ADC is available to sample next channel 1 ADC is busy and cannot sample another channel
12	RESERVED_3	R	0h	Reserved

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Table 3-94. ADC_CFG_ADCCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	ADCBSYCHN	R	0h	ADC Busy Channel. Set when an ADC Start of Conversion [SOC] is generated. When ADCBSY 0:holds the value of the last converted SOC When ADCBSY 1:reflects the SOC currently being processed 0h SOC0 is currently processing or was last SOC converted 1h SOC1 is currently processing or was last SOC converted 2h SOC2 is currently processing or was last SOC converted 3h SOC3 is currently processing or was last SOC converted 4h SOC4 is currently processing or was last SOC converted 5h SOC5 is currently processing or was last SOC converted 6h SOC6 is currently processing or was last SOC converted 7h SOC7 is currently processing or was last SOC converted 8h SOC8 is currently processing or was last SOC converted 9h SOC9 is currently processing or was last SOC converted Ah SOC10 is currently processing or was last SOC converted Bh SOC11 is currently processing or was last SOC converted Ch SOC12 is currently processing or was last SOC converted Dh SOC13 is currently processing or was last SOC converted Eh SOC14 is currently processing or was last SOC converted Fh SOC15 is currently processing or was last SOC converted
7	ADCPWDNZ	R/W	0h	ADC Power Down [active low]. This bit controls the power up and power down of all the analog circuitry inside the analog core. 0 All analog circuitry inside the core is powered down 1 All analog circuitry inside the core is powered up
6:3	RESERVED_2	R	0h	Reserved
2	INTPULSEPOS	R/W	0h	ADC Interrupt Pulse Position. 0 Interrupt pulse generation occurs when ADC begins conversion [at the end of the acquisition window] plus a number of SYSCLK cycles as specified in the ADCINTCYCLE.OFFSET register. 1 Interrupt pulse generation occurs at the end of the conversion, 1 cycle prior to the ADC result latching into its result register
1:0	RESERVED_1	R	0h	Reserved

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3.2.2.46 ADC_CFG_ADCCTL2 Register

3.2.2.46.1 ADC_CFG_ADCCTL2 Register (Offset = 2h) [reset = 0h]

ADC Control 2 Register.

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Table 3-95. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0002h
ADC1_G0_G5	502C 1002h
ADC2_G0_G5	502C 2002h
ADC3_G0_G5	502C 3002h
ADC4_G0_G5	502C 4002h

Figure 3-46. ADC_CFG_ADCCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_3			RESERVED_2				
R			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIGNALMODE	RESOLUTION	RESERVED_1		PRESCALE			
R/W	R/W	R		R/W			
0h	0h	0h		0h			

Table 3-96. ADC_CFG_ADCCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_3	R	0h	Reserved
12:8	RESERVED_2	R	0h	Reserved
7	SIGNALMODE	R/W	0h	SOC Signaling Mode. Selects the input mode of the converter. Use the AdcSetMode function to change the signal mode. 0 Single-ended 1 Differential
6	RESOLUTION	R/W	0h	SOC Conversion Resolution. Selects the resolution of the converter. Use the AdcSetMode function to change the resolution. 0 12-bit resolution
5:4	RESERVED_1	R	0h	Reserved
3:0	PRESCALE	R/W	0h	ADC Clock Prescaler. 0000 ADCCLK = Input Clock / 1.0 0001 Invalid 0010 ADCCLK = Input Clock / 2.0 0011 ADCCLK = Input Clock / 2.5 0100 ADCCLK = Input Clock / 3.0 0101 ADCCLK = Input Clock / 3.5 0110 ADCCLK = Input Clock / 4.0 0111 ADCCLK = Input Clock / 4.5 1000 ADCCLK = Input Clock / 5.0 1001 ADCCLK = Input Clock / 5.5 1010 ADCCLK = Input Clock / 6.0 1011 ADCCLK = Input Clock / 6.5 1100 ADCCLK = Input Clock / 7.0 1101 ADCCLK = Input Clock / 7.5 1110 ADCCLK = Input Clock / 8.0 1111 ADCCLK = Input Clock / 8.5

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3.2.2.47 ADC_CFG_ADCBURSTCTL Register

3.2.2.47.1 ADC_CFG_ADCBURSTCTL Register (Offset = 4h) [reset = 0h]

ADC Burst Control Register.

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Table 3-97. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0004h
ADC1_G0_G5	502C 1004h
ADC2_G0_G5	502C 2004h
ADC3_G0_G5	502C 3004h
ADC4_G0_G5	502C 4004h

Figure 3-47. ADC_CFG_ADCBURSTCTL Name Register

15	14	13	12	11	10	9	8
BURSTEN	RESERVED_2			BURSTSIZE			
R/W	R			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	BURSTTRIGSEL						
R	R/W						
0h	0h						

Table 3-98. ADC_CFG_ADCBURSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BURSTEN	R/W	0h	SOC Burst Mode Enable. This bit enables the SOC Burst Mode of operation. 0 Burst mode is disabled. 1 Burst mode is enabled.
14:12	RESERVED_2	R	0h	Reserved
11:8	BURSTSIZE	R/W	0h	SOC Burst Size Select. This bit field determines how many SOCs are converted when a burst conversion sequence is started. The first SOC converted is defined by the round robin pointer, which is advanced as each SOC is converted. 0h 1 SOC converted 1h 2 SOCs converted 2h 3 SOCs converted 3h 4 SOCs converted 4h 5 SOCs converted 5h 6 SOCs converted 6h 7 SOCs converted 7h 8 SOCs converted 8h 9 SOCs converted 9h 10 SOCs converted Ah 11 SOCs converted Bh 12 SOCs converted Ch 13 SOCs converted Dh 14 SOCs converted Eh 15 SOCs converted Fh 16 SOCs converted Note: If the burst causes SOCs to be set for conversion that were already pending, the corresponding bits in the ADCSOCOVF register will be set.
7	RESERVED_1	R	0h	Reserved

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Table 3-98. ADC_CFG_ADCBURSTCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	BURSTTRIGSEL	R/W	0h	SOC Burst Trigger Source Select. Configures which trigger will start a burst conversion sequence. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h BURSTTRIG0 - Software only 01h BURSTTRIG1 - RTI0 Timer 02h BURSTTRIG2 - RTI1 Timer 03h BURSTTRIG3 - RTI2 Timer 04h BURSTTRIG4 - RTI3 Timer 05h BURSTTRIG5 - InputXBAR.Out[5] 06h BURSTTRIG6 - spare 07h BURSTTRIG7 - spare 08h BURSTTRIG8 - EPWM0, ADCSOCA 09h BURSTTRIG9 - EPWM0, ADCSOCB 0Ah BURSTTRIG10 - EPWM1, ADCSOCA 0Bh BURSTTRIG11 - EPWM1, ADCSOCB 0Ch BURSTTRIG12 - EPWM2, ADCSOCA 0Dh BURSTTRIG13 - EPWM2, ADCSOCB 0Eh BURSTTRIG14 - EPWM3, ADCSOCA 0Fh BURSTTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h BURSTTRIG64 - EPWM28, ADCSOCA 41h BURSTTRIG65 - EPWM28, ADCSOCB 42h BURSTTRIG66 - EPWM29, ADCSOCA 43h BURSTTRIG67 - EPWM29, ADCSOCB 44h BURSTTRIG68 - EPWM30, ADCSOCA 45h BURSTTRIG69 - EPWM30, ADCSOCB 46h BURSTTRIG70 - EPWM31, ADCSOCA 47h BURSTTRIG71 - EPWM31, ADCSOCB 48h BURSTTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h BURSTTRIG81 - ECAP9, TRIGOUT 52h BURSTTRIG82 - ECAP10, TRIGOUT .... 57h BURSTTRIG73 - ECAP15, TRIGOUT 58h BURSTTRIG1 - RTI4 Timer 59h BURSTTRIG1 - RTI5 Timer 5Ah BURSTTRIG1 - RTI6 Timer 5Bh BURSTTRIG1 - RTI7 Timer

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3.2.2.48 ADC_CFG_ADCINTFLG Register

3.2.2.48.1 ADC_CFG_ADCINTFLG Register (Offset = 6h) [reset = 0h]

ADC Interrupt Flag Register.

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Table 3-99. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0006h
ADC1_G0_G5	502C 1006h
ADC2_G0_G5	502C 2006h
ADC3_G0_G5	502C 3006h
ADC4_G0_G5	502C 4006h

Figure 3-48. ADC_CFG_ADCINTFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADCINT4RESULT	ADCINT3RESULT	ADCINT2RESULT	ADCINT1RESULT	ADCINT4	ADCINT3	ADCINT2	ADCINT1
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-100. ADC_CFG_ADCINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7	ADCINT4RESULT	R	0h	ADC Interrupt 4 Results Ready Flag. This flag is set when the conversions results associated with ADCINT4 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT4 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.
6	ADCINT3RESULT	R	0h	ADC Interrupt 3 Results Ready Flag. This flag is set when the conversions results associated with ADCINT3 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT3 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.

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Table 3-100. ADC_CFG_ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ADCINT2RESULT	R	0h	ADC Interrupt 2 Results Ready Flag. This flag is set when the conversions results associated with ADCINT2 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT2 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.
4	ADCINT1RESULT	R	0h	ADC Interrupt 1 Results Ready Flag. This flag is set when the conversions results associated with ADCINT1 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT1 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.
3	ADCINT4	R	0h	ADC Interrupt 4 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
2	ADCINT3	R	0h	ADC Interrupt 3 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
1	ADCINT2	R	0h	ADC Interrupt 2 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

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Table 3-100. ADC_CFG_ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADCINT1	R	0h	ADC Interrupt 1 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

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3.2.2.49 ADC_CFG_ADCINTFLGCLR Register

3.2.2.49.1 ADC_CFG_ADCINTFLGCLR Register (Offset = 8h) [reset = 0h]

ADC Interrupt Flag Clear Register.

Return to Summary Table

Table 3-101. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0008h
ADC1_G0_G5	502C 1008h
ADC2_G0_G5	502C 2008h
ADC3_G0_G5	502C 3008h
ADC4_G0_G5	502C 4008h

Figure 3-49. ADC_CFG_ADCINTFLGCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 3-102. ADC_CFG_ADCINTFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	ADCINT4	R/W1TS	0h	ADC Interrupt 4 Flag Clear. Reads return 0. 0 No action 1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
2	ADCINT3	R/W1TS	0h	ADC Interrupt 3 Flag Clear. Reads return 0. 0 No action 1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
1	ADCINT2	R/W1TS	0h	ADC Interrupt 2 Flag Clear. Reads return 0. 0 No action 1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
0	ADCINT1	R/W1TS	0h	ADC Interrupt 1 Flag Clear. Reads return 0. 0 No action 1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set

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3.2.2.50 ADC_CFG_ADCINTOVF Register

3.2.2.50.1 ADC_CFG_ADCINTOVF Register (Offset = Ah) [reset = 0h]

ADC Interrupt Overflow Register.

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Table 3-103. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 000Ah
ADC1_G0_G5	502C 100Ah
ADC2_G0_G5	502C 200Ah
ADC3_G0_G5	502C 300Ah
ADC4_G0_G5	502C 400Ah

Figure 3-50. ADC_CFG_ADCINTOVF Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R	R	R	R
0h				0h	0h	0h	0h

Table 3-104. ADC_CFG_ADCINTOVF Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	ADCINT4	R	0h	ADC Interrupt 4 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
2	ADCINT3	R	0h	ADC Interrupt 3 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
1	ADCINT2	R	0h	ADC Interrupt 2 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.

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Table 3-104. ADC_CFG_ADCINTOVF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADCINT1	R	0h	ADC Interrupt 1 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.

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3.2.2.51 ADC_CFG_ADCINTOVFCLR Register

3.2.2.51.1 ADC_CFG_ADCINTOVFCLR Register (Offset = Ch) [reset = 0h]

ADC Interrupt Overflow Clear Register.

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Table 3-105. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 000Ch
ADC1_G0_G5	502C 100Ch
ADC2_G0_G5	502C 200Ch
ADC3_G0_G5	502C 300Ch
ADC4_G0_G5	502C 400Ch

Figure 3-51. ADC_CFG_ADCINTOVFCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 3-106. ADC_CFG_ADCINTOVFCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	ADCINT4	R/W1TS	0h	ADC Interrupt 4 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
2	ADCINT3	R/W1TS	0h	ADC Interrupt 3 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
1	ADCINT2	R/W1TS	0h	ADC Interrupt 2 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
0	ADCINT1	R/W1TS	0h	ADC Interrupt 1 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.

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3.2.2.52 ADC_CFG_ADCINTSEL1N2 Register

3.2.2.52.1 ADC_CFG_ADCINTSEL1N2 Register (Offset = Eh) [reset = 0h]

ADC Interrupt 1 and 2 Selection Register.

Return to Summary Table

Table 3-107. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 000Eh
ADC1_G0_G5	502C 100Eh
ADC2_G0_G5	502C 200Eh
ADC3_G0_G5	502C 300Eh
ADC4_G0_G5	502C 400Eh

Figure 3-52. ADC_CFG_ADCINTSEL1N2 Name Register

15	14	13	12	11	10	9	8
RESERVED_2	INT2CONT	INT2E	INT2SEL				
R	R/W	R/W	R/W				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	INT1CONT	INT1E	INT1SEL				
R	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 3-108. ADC_CFG_ADCINTSEL1N2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_2	R	0h	Reserved
14	INT2CONT	R/W	0h	ADCINT2 Continue to Interrupt Mode 0 No further ADCINT2 pulses are generated until ADCINT2 flag [in ADCINTFLG register] is cleared by user. 1 ADCINT2 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT2E	R/W	0h	ADCINT2 Interrupt Enable 0 ADCINT2 is disabled 1 ADCINT2 is enabled
12:8	INT2SEL	R/W	0h	ADCINT2 EOC Source Select 00h EOC0 is trigger for ADCINT2 01h EOC1 is trigger for ADCINT2 02h EOC2 is trigger for ADCINT2 03h EOC3 is trigger for ADCINT2 04h EOC4 is trigger for ADCINT2 05h EOC5 is trigger for ADCINT2 06h EOC6 is trigger for ADCINT2 07h EOC7 is trigger for ADCINT2 08h EOC8 is trigger for ADCINT2 09h EOC9 is trigger for ADCINT2 0Ah EOC10 is trigger for ADCINT2 0Bh EOC11 is trigger for ADCINT2 0Ch EOC12 is trigger for ADCINT2 0Dh EOC13 is trigger for ADCINT2 0Eh EOC14 is trigger for ADCINT2 0Fh EOC15 is trigger for ADCINT2 10h OSINT1 is trigger for ADCINT2 11h OSINT2 is trigger for ADCINT2 12h OSINT3 is trigger for ADCINT2 13h OSINT4 is trigger for ADCINT2
7	RESERVED_1	R	0h	Reserved

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Table 3-108. ADC_CFG_ADCINTSEL1N2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INT1CONT	R/W	0h	ADCINT1 Continue to Interrupt Mode 0 No further ADCINT1 pulses are generated until ADCINT1 flag [in ADCINTFLG register] is cleared by user. 1 ADCINT1 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
5	INT1E	R/W	0h	ADCINT1 Interrupt Enable 0 ADCINT1 is disabled 1 ADCINT1 is enabled
4:0	INT1SEL	R/W	0h	ADCINT1 EOC Source Select 00h EOC0 is trigger for ADCINT1 01h EOC1 is trigger for ADCINT1 02h EOC2 is trigger for ADCINT1 03h EOC3 is trigger for ADCINT1 04h EOC4 is trigger for ADCINT1 05h EOC5 is trigger for ADCINT1 06h EOC6 is trigger for ADCINT1 07h EOC7 is trigger for ADCINT1 08h EOC8 is trigger for ADCINT1 09h EOC9 is trigger for ADCINT1 0Ah EOC10 is trigger for ADCINT1 0Bh EOC11 is trigger for ADCINT1 0Ch EOC12 is trigger for ADCINT1 0Dh EOC13 is trigger for ADCINT1 0Eh EOC14 is trigger for ADCINT1 0Fh EOC15 is trigger for ADCINT1 10h OSINT1 is trigger for ADCINT1 11h OSINT2 is trigger for ADCINT1 12h OSINT3 is trigger for ADCINT1 13h OSINT4 is trigger for ADCINT1

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3.2.2.53 ADC_CFG_ADCINTSEL3N4 Register

3.2.2.53.1 ADC_CFG_ADCINTSEL3N4 Register (Offset = 10h) [reset = 0h]

ADC Interrupt 3 and 4 Selection Register.

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Table 3-109. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0010h
ADC1_G0_G5	502C 1010h
ADC2_G0_G5	502C 2010h
ADC3_G0_G5	502C 3010h
ADC4_G0_G5	502C 4010h

Figure 3-53. ADC_CFG_ADCINTSEL3N4 Name Register

15	14	13	12	11	10	9	8
RESERVED_2	INT4CONT	INT4E	INT4SEL				
R	R/W	R/W	R/W				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	INT3CONT	INT3E	INT3SEL				
R	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 3-110. ADC_CFG_ADCINTSEL3N4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_2	R	0h	Reserved
14	INT4CONT	R/W	0h	ADCINT4 Continue to Interrupt Mode 0 No further ADCINT4 pulses are generated until ADCINT4 flag [in ADCINTFLG register] is cleared by user. 1 ADCINT4 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT4E	R/W	0h	ADCINT4 Interrupt Enable 0 ADCINT4 is disabled 1 ADCINT4 is enabled
12:8	INT4SEL	R/W	0h	ADCINT4 EOC Source Select 00h EOC0 is trigger for ADCINT4 01h EOC1 is trigger for ADCINT4 02h EOC2 is trigger for ADCINT4 03h EOC3 is trigger for ADCINT4 04h EOC4 is trigger for ADCINT4 05h EOC5 is trigger for ADCINT4 06h EOC6 is trigger for ADCINT4 07h EOC7 is trigger for ADCINT4 08h EOC8 is trigger for ADCINT4 09h EOC9 is trigger for ADCINT4 0Ah EOC10 is trigger for ADCINT4 0Bh EOC11 is trigger for ADCINT4 0Ch EOC12 is trigger for ADCINT4 0Dh EOC13 is trigger for ADCINT4 0Eh EOC14 is trigger for ADCINT4 0Fh EOC15 is trigger for ADCINT4 10hOSINT1 is trigger for ADCINT4 11hOSINT2 is trigger for ADCINT4 12hOSINT3 is trigger for ADCINT4 13hOSINT4 is trigger for ADCINT4
7	RESERVED_1	R	0h	Reserved

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Table 3-110. ADC_CFG_ADCINTSEL3N4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	INT3CONT	R/W	0h	ADCINT3 Continue to Interrupt Mode 0 No further ADCINT3 pulses are generated until ADCINT3 flag [in ADCINTFLG register] is cleared by user. 1 ADCINT3 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
5	INT3E	R/W	0h	ADCINT3 Interrupt Enable 0 ADCINT3 is disabled 1 ADCINT3 is enabled
4:0	INT3SEL	R/W	0h	ADCINT3 EOC Source Select 00h EOC0 is trigger for ADCINT3 01h EOC1 is trigger for ADCINT3 02h EOC2 is trigger for ADCINT3 03h EOC3 is trigger for ADCINT3 04h EOC4 is trigger for ADCINT3 05h EOC5 is trigger for ADCINT3 06h EOC6 is trigger for ADCINT3 07h EOC7 is trigger for ADCINT3 08h EOC8 is trigger for ADCINT3 09h EOC9 is trigger for ADCINT3 0Ah EOC10 is trigger for ADCINT3 0Bh EOC11 is trigger for ADCINT3 0Ch EOC12 is trigger for ADCINT3 0Dh EOC13 is trigger for ADCINT3 0Eh EOC14 is trigger for ADCINT3 0Fh EOC15 is trigger for ADCINT3 10h OSINT1 is trigger for ADCINT3 11h OSINT2 is trigger for ADCINT3 12h OSINT3 is trigger for ADCINT3 13h OSINT4 is trigger for ADCINT3

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3.2.2.54 ADC_CFG_ADCSOCPRICTL Register

3.2.2.54.1 ADC_CFG_ADCSOCPRICTL Register (Offset = 12h) [reset = 200h]

ADC SOC Priority Control Register.

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Table 3-111. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0012h
ADC1_G0_G5	502C 1012h
ADC2_G0_G5	502C 2012h
ADC3_G0_G5	502C 3012h
ADC4_G0_G5	502C 4012h

Figure 3-54. ADC_CFG_ADCSOCPRICTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						RRPOINTER	
R						R	
0h						10h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RRPOINTER			SOCPRIORITY				
R			R/W				
10h			0h				

Table 3-112. ADC_CFG_ADCSOCPRICTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved

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Table 3-112. ADC_CFG_ADCSOCPRICTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:5	RRPOINTER	R	10h	Round Robin Pointer. Holds the value of the last converted round robin SOCx to be used by the round robin scheme to determine order of conversions. 00h SOC0 was last round robin SOC to convert, SOC1 is highest round robin priority. 01h SOC1 was last round robin SOC to convert, SOC2 is highest round robin priority. 02h SOC2 was last round robin SOC to convert, SOC3 is highest round robin priority. 03h SOC3 was last round robin SOC to convert, SOC4 is highest round robin priority. 04h SOC4 was last round robin SOC to convert, SOC5 is highest round robin priority. 05h SOC5 was last round robin SOC to convert, SOC6 is highest round robin priority. 06h SOC6 was last round robin SOC to convert, SOC7 is highest round robin priority. 07h SOC7 was last round robin SOC to convert, SOC8 is highest round robin priority. 08h SOC8 was last round robin SOC to convert, SOC9 is highest round robin priority. 09h SOC9 was last round robin SOC to convert, SOC10 is highest round robin priority. 0Ah SOC10 was last round robin SOC to convert, SOC11 is highest round robin priority. 0Bh SOC11 was last round robin SOC to convert, SOC12 is highest round robin priority. 0Ch SOC12 was last round robin SOC to convert, SOC13 is highest round robin priority. 0Dh SOC13 was last round robin SOC to convert, SOC14 is highest round robin priority. 0Eh SOC14 was last round robin SOC to convert, SOC15 is highest round robin priority. 0Fh SOC15 was last round robin SOC to convert, SOC0 is highest round robin priority. 10h Reset value to indicate no SOC has been converted. SOC0 is highest round robin priority. Set to this value when the ADC module is reset by SOFTPRES or when the ADCSOCPRICTL register is written. In the latter case, if a conversion is currently in progress, it will complete and then the new priority will take effect. Others Invalid value.

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Table 3-112. ADC_CFG_ADCSOCPRICTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	SOCPRIORITY	R/W	0h	SOC Priority Determines the cutoff point for priority mode and round robin arbitration for SOCx 00h SOC priority is handled in round robin mode for all channels. 01h SOC0 is high priority, rest of channels are in round robin mode. 02h SOC0-SOC1 are high priority, SOC2-SOC15 are in round robin mode. 03h SOC0-SOC2 are high priority, SOC3-SOC15 are in round robin mode. 04h SOC0-SOC3 are high priority, SOC4-SOC15 are in round robin mode. 05h SOC0-SOC4 are high priority, SOC5-SOC15 are in round robin mode. 06h SOC0-SOC5 are high priority, SOC6-SOC15 are in round robin mode. 07h SOC0-SOC6 are high priority, SOC7-SOC15 are in round robin mode. 08h SOC0-SOC7 are high priority, SOC8-SOC15 are in round robin mode. 09h SOC0-SOC8 are high priority, SOC9-SOC15 are in round robin mode. 0Ah SOC0-SOC9 are high priority, SOC10-SOC15 are in round robin mode. 0Bh SOC0-SOC10 are high priority, SOC11-SOC15 are in round robin mode. 0Ch SOC0-SOC11 are high priority, SOC12-SOC15 are in round robin mode. 0Dh SOC0-SOC12 are high priority, SOC13-SOC15 are in round robin mode. 0Eh SOC0-SOC13 are high priority, SOC14-SOC15 are in round robin mode. 0Fh SOC0-SOC14 are high priority, SOC15 is in round robin mode. 10h All SOCs are in high priority mode, arbitrated by SOC number. Others Invalid selection.

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3.2.2.55 ADC_CFG_ADCINTSOCSEL1 Register

3.2.2.55.1 ADC_CFG_ADCINTSOCSEL1 Register (Offset = 14h) [reset = 0h]

ADC Interrupt SOC Selection 1 Register.

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Table 3-113. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0014h
ADC1_G0_G5	502C 1014h
ADC2_G0_G5	502C 2014h
ADC3_G0_G5	502C 3014h
ADC4_G0_G5	502C 4014h

Figure 3-55. ADC_CFG_ADCINTSOCSEL1 Name Register

15	14	13	12	11	10	9	8
SOC7		SOC6		SOC5		SOC4	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SOC3		SOC2		SOC1		SOC0	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-114. ADC_CFG_ADCINTSOCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SOC7	R/W	0h	SOC7 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC7. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC7. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC7. 10 ADCINT2 will trigger SOC7. 11 Invalid selection.
13:12	SOC6	R/W	0h	SOC6 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC6. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC6. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC6. 10 ADCINT2 will trigger SOC6. 11 Invalid selection.
11:10	SOC5	R/W	0h	SOC5 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC5. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC5. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC5. 10 ADCINT2 will trigger SOC5. 11 Invalid selection.
9:8	SOC4	R/W	0h	SOC4 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC4. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC4. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC4. 10 ADCINT2 will trigger SOC4. 11 Invalid selection.

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Table 3-114. ADC_CFG_ADCINTSOCSEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	SOC3	R/W	0h	SOC3 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC3. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC3. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC3. 10 ADCINT2 will trigger SOC3. 11 Invalid selection.
5:4	SOC2	R/W	0h	SOC2 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC2. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC2. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC2. 10 ADCINT2 will trigger SOC2. 11 Invalid selection.
3:2	SOC1	R/W	0h	SOC1 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC1. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC1. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC1. 10 ADCINT2 will trigger SOC1. 11 Invalid selection.
1:0	SOC0	R/W	0h	SOC0 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC0. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC0. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC0. 10 ADCINT2 will trigger SOC0. 11 Invalid selection.

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3.2.2.56 ADC_CFG_ADCINTSOCSEL2 Register

3.2.2.56.1 ADC_CFG_ADCINTSOCSEL2 Register (Offset = 16h) [reset = 0h]

ADC Interrupt SOC Selection 2 Register.

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Table 3-115. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0016h
ADC1_G0_G5	502C 1016h
ADC2_G0_G5	502C 2016h
ADC3_G0_G5	502C 3016h
ADC4_G0_G5	502C 4016h

Figure 3-56. ADC_CFG_ADCINTSOCSEL2 Name Register

15	14	13	12	11	10	9	8
SOC15		SOC14		SOC13		SOC12	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
SOC11		SOC10		SOC9		SOC8	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-116. ADC_CFG_ADCINTSOCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SOC15	R/W	0h	SOC15 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC15. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC15. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC15. 10 ADCINT2 will trigger SOC15. 11 Invalid selection.
13:12	SOC14	R/W	0h	SOC14 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC14. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC14. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC14. 10 ADCINT2 will trigger SOC14. 11 Invalid selection.
11:10	SOC13	R/W	0h	SOC13 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC13. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC13. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC13. 10 ADCINT2 will trigger SOC13. 11 Invalid selection.
9:8	SOC12	R/W	0h	SOC12 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC12. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC12. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC12. 10 ADCINT2 will trigger SOC12. 11 Invalid selection.

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Table 3-116. ADC_CFG_ADCINTSOCSEL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	SOC11	R/W	0h	SOC11 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC11. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC11. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC11. 10 ADCINT2 will trigger SOC11. 11 Invalid selection.
5:4	SOC10	R/W	0h	SOC10 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC10. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC10. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC10. 10 ADCINT2 will trigger SOC10. 11 Invalid selection.
3:2	SOC9	R/W	0h	SOC9 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC9. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC9. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC9. 10 ADCINT2 will trigger SOC9. 11 Invalid selection.
1:0	SOC8	R/W	0h	SOC8 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC8. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC8. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC8. 10 ADCINT2 will trigger SOC8. 11 Invalid selection.

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3.2.2.57 ADC_CFG_ADCSOCFLG1 Register

3.2.2.57.1 ADC_CFG_ADCSOCFLG1 Register (Offset = 18h) [reset = 0h]

ADC SOC Flag 1 Register.

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Table 3-117. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0018h
ADC1_G0_G5	502C 1018h
ADC2_G0_G5	502C 2018h
ADC3_G0_G5	502C 3018h
ADC4_G0_G5	502C 4018h

Figure 3-57. ADC_CFG_ADCSOCFLG1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-118. ADC_CFG_ADCSOCFLG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R	0h	SOC15 Start of Conversion Flag. Indicates the state of SOC15 conversions. 0 No sample pending for SOC15. 1 Trigger has been received and sample is pending for SOC15. This bit will be automatically cleared when the SOC15 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
14	SOC14	R	0h	SOC14 Start of Conversion Flag. Indicates the state of SOC14 conversions. 0 No sample pending for SOC14. 1 Trigger has been received and sample is pending for SOC14. This bit will be automatically cleared when the SOC14 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
13	SOC13	R	0h	SOC13 Start of Conversion Flag. Indicates the state of SOC13 conversions. 0 No sample pending for SOC13. 1 Trigger has been received and sample is pending for SOC13. This bit will be automatically cleared when the SOC13 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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Table 3-118. ADC_CFG_ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	SOC12	R	0h	SOC12 Start of Conversion Flag. Indicates the state of SOC12 conversions. 0 No sample pending for SOC12. 1 Trigger has been received and sample is pending for SOC12. This bit will be automatically cleared when the SOC12 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
11	SOC11	R	0h	SOC11 Start of Conversion Flag. Indicates the state of SOC11 conversions. 0 No sample pending for SOC11. 1 Trigger has been received and sample is pending for SOC11. This bit will be automatically cleared when the SOC11 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
10	SOC10	R	0h	SOC10 Start of Conversion Flag. Indicates the state of SOC10 conversions. 0 No sample pending for SOC10. 1 Trigger has been received and sample is pending for SOC10. This bit will be automatically cleared when the SOC10 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
9	SOC9	R	0h	SOC9 Start of Conversion Flag. Indicates the state of SOC9 conversions. 0 No sample pending for SOC9. 1 Trigger has been received and sample is pending for SOC9. This bit will be automatically cleared when the SOC9 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
8	SOC8	R	0h	SOC8 Start of Conversion Flag. Indicates the state of SOC8 conversions. 0 No sample pending for SOC8. 1 Trigger has been received and sample is pending for SOC8. This bit will be automatically cleared when the SOC8 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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Table 3-118. ADC_CFG_ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SOC7	R	0h	SOC7 Start of Conversion Flag. Indicates the state of SOC7 conversions. 0 No sample pending for SOC7. 1 Trigger has been received and sample is pending for SOC7. This bit will be automatically cleared when the SOC7 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
6	SOC6	R	0h	SOC6 Start of Conversion Flag. Indicates the state of SOC6 conversions. 0 No sample pending for SOC6. 1 Trigger has been received and sample is pending for SOC6. This bit will be automatically cleared when the SOC6 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
5	SOC5	R	0h	SOC5 Start of Conversion Flag. Indicates the state of SOC5 conversions. 0 No sample pending for SOC5. 1 Trigger has been received and sample is pending for SOC5. This bit will be automatically cleared when the SOC5 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
4	SOC4	R	0h	SOC4 Start of Conversion Flag. Indicates the state of SOC4 conversions. 0 No sample pending for SOC4. 1 Trigger has been received and sample is pending for SOC4. This bit will be automatically cleared when the SOC4 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
3	SOC3	R	0h	SOC3 Start of Conversion Flag. Indicates the state of SOC3 conversions. 0 No sample pending for SOC3. 1 Trigger has been received and sample is pending for SOC3. This bit will be automatically cleared when the SOC3 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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Table 3-118. ADC_CFG_ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SOC2	R	0h	SOC2 Start of Conversion Flag. Indicates the state of SOC2 conversions. 0 No sample pending for SOC2. 1 Trigger has been received and sample is pending for SOC2. This bit will be automatically cleared when the SOC2 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
1	SOC1	R	0h	SOC1 Start of Conversion Flag. Indicates the state of SOC1 conversions. 0 No sample pending for SOC1. 1 Trigger has been received and sample is pending for SOC1. This bit will be automatically cleared when the SOC1 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
0	SOC0	R	0h	SOC0 Start of Conversion Flag. Indicates the state of SOC0 conversions. 0 No sample pending for SOC0. 1 Trigger has been received and sample is pending for SOC0. This bit will be automatically cleared when the SOC0 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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3.2.2.58 ADC_CFG_ADCSOCFRC1 Register

3.2.2.58.1 ADC_CFG_ADCSOCFRC1 Register (Offset = 1Ah) [reset = 0h]

ADC SOC Force 1 Register.

Return to Summary Table

Table 3-119. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 001Ah
ADC1_G0_G5	502C 101Ah
ADC2_G0_G5	502C 201Ah
ADC3_G0_G5	502C 301Ah
ADC4_G0_G5	502C 401Ah

Figure 3-58. ADC_CFG_ADCSOCFRC1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-120. ADC_CFG_ADCSOCFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R/W1TS	0h	SOC15 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC15 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC15 flag bit to 1. This will cause a conversion to start once priority is given to SOC15. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC15 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
14	SOC14	R/W1TS	0h	SOC14 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC14 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC14 flag bit to 1. This will cause a conversion to start once priority is given to SOC14. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC14 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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Table 3-120. ADC_CFG_ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SOC13	R/W1TS	0h	SOC13 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC13 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC13 flag bit to 1. This will cause a conversion to start once priority is given to SOC13. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC13 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
12	SOC12	R/W1TS	0h	SOC12 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC12 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC12 flag bit to 1. This will cause a conversion to start once priority is given to SOC12. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC12 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
11	SOC11	R/W1TS	0h	SOC11 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC11 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC11 flag bit to 1. This will cause a conversion to start once priority is given to SOC11. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC11 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
10	SOC10	R/W1TS	0h	SOC10 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC10 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC10 flag bit to 1. This will cause a conversion to start once priority is given to SOC10. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC10 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
9	SOC9	R/W1TS	0h	SOC9 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC9 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC9 flag bit to 1. This will cause a conversion to start once priority is given to SOC9. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC9 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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Table 3-120. ADC_CFG_ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SOC8	R/W1TS	0h	SOC8 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC8 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC8 flag bit to 1. This will cause a conversion to start once priority is given to SOC8. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC8 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
7	SOC7	R/W1TS	0h	SOC7 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC7 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC7 flag bit to 1. This will cause a conversion to start once priority is given to SOC7. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC7 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
6	SOC6	R/W1TS	0h	SOC6 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC6 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC6 flag bit to 1. This will cause a conversion to start once priority is given to SOC6. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC6 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
5	SOC5	R/W1TS	0h	SOC5 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC5 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC5 flag bit to 1. This will cause a conversion to start once priority is given to SOC5. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC5 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
4	SOC4	R/W1TS	0h	SOC4 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC4 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC4 flag bit to 1. This will cause a conversion to start once priority is given to SOC4. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC4 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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Table 3-120. ADC_CFG_ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SOC3	R/W1TS	0h	SOC3 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC3 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC3 flag bit to 1. This will cause a conversion to start once priority is given to SOC3. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC3 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
2	SOC2	R/W1TS	0h	SOC2 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC2 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC2 flag bit to 1. This will cause a conversion to start once priority is given to SOC2. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC2 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
1	SOC1	R/W1TS	0h	SOC1 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC1 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC1 flag bit to 1. This will cause a conversion to start once priority is given to SOC1. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC1 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
0	SOC0	R/W1TS	0h	SOC0 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC0 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC0 flag bit to 1. This will cause a conversion to start once priority is given to SOC0. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC0 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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3.2.2.59 ADC_CFG_ADCSOCOVF1 Register

3.2.2.59.1 ADC_CFG_ADCSOCOVF1 Register (Offset = 1Ch) [reset = 0h]

ADC SOC Overflow 1 Register.

Return to Summary Table

Table 3-121. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 001Ch
ADC1_G0_G5	502C 101Ch
ADC2_G0_G5	502C 201Ch
ADC3_G0_G5	502C 301Ch
ADC4_G0_G5	502C 401Ch

Figure 3-59. ADC_CFG_ADCSOCOVF1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-122. ADC_CFG_ADCSOCOVF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R	0h	SOC15 Start of Conversion Overflow Flag. Indicates an SOC15 event was generated in hardware while an existing SOC15 event was already pending. 0 No SOC15 event overflow. 1 SOC15 event overflow. An overflow condition does not stop SOC15 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
14	SOC14	R	0h	SOC14 Start of Conversion Overflow Flag. Indicates an SOC14 event was generated in hardware while an existing SOC14 event was already pending. 0 No SOC14 event overflow. 1 SOC14 event overflow. An overflow condition does not stop SOC14 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
13	SOC13	R	0h	SOC13 Start of Conversion Overflow Flag. Indicates an SOC13 event was generated in hardware while an existing SOC13 event was already pending. 0 No SOC13 event overflow. 1 SOC13 event overflow. An overflow condition does not stop SOC13 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
12	SOC12	R	0h	SOC12 Start of Conversion Overflow Flag. Indicates an SOC12 event was generated in hardware while an existing SOC12 event was already pending. 0 No SOC12 event overflow. 1 SOC12 event overflow. An overflow condition does not stop SOC12 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.

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Table 3-122. ADC_CFG_ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	R	0h	SOC11 Start of Conversion Overflow Flag. Indicates an SOC11 event was generated in hardware while an existing SOC11 event was already pending. 0 No SOC11 event overflow. 1 SOC11 event overflow. An overflow condition does not stop SOC11 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
10	SOC10	R	0h	SOC10 Start of Conversion Overflow Flag. Indicates an SOC10 event was generated in hardware while an existing SOC10 event was already pending. 0 No SOC10 event overflow. 1 SOC10 event overflow. An overflow condition does not stop SOC10 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
9	SOC9	R	0h	SOC9 Start of Conversion Overflow Flag. Indicates an SOC9 event was generated in hardware while an existing SOC9 event was already pending. 0 No SOC9 event overflow. 1 SOC9 event overflow. An overflow condition does not stop SOC9 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
8	SOC8	R	0h	SOC8 Start of Conversion Overflow Flag. Indicates an SOC8 event was generated in hardware while an existing SOC8 event was already pending. 0 No SOC8 event overflow. 1 SOC8 event overflow. An overflow condition does not stop SOC8 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
7	SOC7	R	0h	SOC7 Start of Conversion Overflow Flag. Indicates an SOC7 event was generated in hardware while an existing SOC7 event was already pending. 0 No SOC7 event overflow. 1 SOC7 event overflow. An overflow condition does not stop SOC7 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
6	SOC6	R	0h	SOC6 Start of Conversion Overflow Flag. Indicates an SOC6 event was generated in hardware while an existing SOC6 event was already pending. 0 No SOC6 event overflow. 1 SOC6 event overflow. An overflow condition does not stop SOC6 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
5	SOC5	R	0h	SOC5 Start of Conversion Overflow Flag. Indicates an SOC5 event was generated in hardware while an existing SOC5 event was already pending. 0 No SOC5 event overflow. 1 SOC5 event overflow. An overflow condition does not stop SOC5 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
4	SOC4	R	0h	SOC4 Start of Conversion Overflow Flag. Indicates an SOC4 event was generated in hardware while an existing SOC4 event was already pending. 0 No SOC4 event overflow. 1 SOC4 event overflow. An overflow condition does not stop SOC4 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.

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Table 3-122. ADC_CFG_ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SOC3	R	0h	SOC3 Start of Conversion Overflow Flag. Indicates an SOC3 event was generated in hardware while an existing SOC3 event was already pending. 0 No SOC3 event overflow. 1 SOC3 event overflow. An overflow condition does not stop SOC3 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
2	SOC2	R	0h	SOC2 Start of Conversion Overflow Flag. Indicates an SOC2 event was generated in hardware while an existing SOC2 event was already pending. 0 No SOC2 event overflow. 1 SOC2 event overflow. An overflow condition does not stop SOC2 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
1	SOC1	R	0h	SOC1 Start of Conversion Overflow Flag. Indicates an SOC1 event was generated in hardware while an existing SOC1 event was already pending. 0 No SOC1 event overflow. 1 SOC1 event overflow. An overflow condition does not stop SOC1 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
0	SOC0	R	0h	SOC0 Start of Conversion Overflow Flag. Indicates an SOC0 event was generated in hardware while an existing SOC0 event was already pending. 0 No SOC0 event overflow. 1 SOC0 event overflow. An overflow condition does not stop SOC0 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.

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3.2.2.60 ADC_CFG_ADCSOCOVFCLR1 Register

3.2.2.60.1 ADC_CFG_ADCSOCOVFCLR1 Register (Offset = 1Eh) [reset = 0h]

ADC SOC Overflow Clear 1 Register.

Return to Summary Table

Table 3-123. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 001Eh
ADC1_G0_G5	502C 101Eh
ADC2_G0_G5	502C 201Eh
ADC3_G0_G5	502C 301Eh
ADC4_G0_G5	502C 401Eh

Figure 3-60. ADC_CFG_ADCSOCOVFCLR1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-124. ADC_CFG_ADCSOCOVFCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R/W1TS	0h	SOC15 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC15 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC15 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
14	SOC14	R/W1TS	0h	SOC14 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC14 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC14 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
13	SOC13	R/W1TS	0h	SOC13 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC13 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC13 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
12	SOC12	R/W1TS	0h	SOC12 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC12 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC12 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

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Table 3-124. ADC_CFG_ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	R/W1TS	0h	SOC11 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC11 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC11 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
10	SOC10	R/W1TS	0h	SOC10 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC10 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC10 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
9	SOC9	R/W1TS	0h	SOC9 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC9 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC9 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
8	SOC8	R/W1TS	0h	SOC8 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC8 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC8 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
7	SOC7	R/W1TS	0h	SOC7 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC7 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC7 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
6	SOC6	R/W1TS	0h	SOC6 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC6 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC6 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
5	SOC5	R/W1TS	0h	SOC5 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC5 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC5 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
4	SOC4	R/W1TS	0h	SOC4 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC4 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC4 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

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Table 3-124. ADC_CFG_ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SOC3	R/W1TS	0h	SOC3 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC3 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC3 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
2	SOC2	R/W1TS	0h	SOC2 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC2 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC2 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
1	SOC1	R/W1TS	0h	SOC1 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC1 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC1 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
0	SOC0	R/W1TS	0h	SOC0 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC0 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC0 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

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3.2.2.61 ADC_CFG_ADCSOC0CTL Register

3.2.2.61.1 ADC_CFG_ADCSOC0CTL Register (Offset = 20h) [reset = 0h]

ADC SOC0 Control Register.

Return to Summary Table

Table 3-125. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0020h
ADC1_G0_G5	502C 1020h
ADC2_G0_G5	502C 2020h
ADC3_G0_G5	502C 3020h
ADC4_G0_G5	502C 4020h

Figure 3-61. ADC_CFG_ADCSOC0CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		

23	22	21	20	19	18	17	16
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			

15	14	13	12	11	10	9	8
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h

7	6	5	4	3	2	1	0
ACQPS							
R/W							
0h							

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Table 3-126. ADC_CFG_ADCSOC0CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC0 External Channel Mux Select. Selects the external mux combination to output when SOC0 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-126. ADC_CFG_ADCSOC0CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC0 Trigger Source Select. Along with the SOC0 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC0 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-126. ADC_CFG_ADCSOC0CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC0 Channel Select. Selects the channel to be converted when SOC0 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC0 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.62 ADC_CFG_ADCSOC1CTL Register

3.2.2.62.1 ADC_CFG_ADCSOC1CTL Register (Offset = 24h) [reset = 0h]

ADC SOC1 Control Register.

Return to Summary Table

Table 3-127. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0024h
ADC1_G0_G5	502C 1024h
ADC2_G0_G5	502C 2024h
ADC3_G0_G5	502C 3024h
ADC4_G0_G5	502C 4024h

Figure 3-62. ADC_CFG_ADCSOC1CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-128. ADC_CFG_ADCSOC1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC1 External Channel Mux Select. Selects the external mux combination to output when SOC1 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-128. ADC_CFG_ADCSOC1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC1 Trigger Source Select. Along with the SOC1 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC1 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-128. ADC_CFG_ADCSOC1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC1 Channel Select. Selects the channel to be converted when SOC1 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC1 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.63 ADC_CFG_ADCSOC2CTL Register

3.2.2.63.1 ADC_CFG_ADCSOC2CTL Register (Offset = 28h) [reset = 0h]

ADC SOC2 Control Register.

Return to Summary Table

Table 3-129. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0028h
ADC1_G0_G5	502C 1028h
ADC2_G0_G5	502C 2028h
ADC3_G0_G5	502C 3028h
ADC4_G0_G5	502C 4028h

Figure 3-63. ADC_CFG_ADCSOC2CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-130. ADC_CFG_ADCSOC2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC2 External Channel Mux Select. Selects the external mux combination to output when SOC2 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-130. ADC_CFG_ADCSOC2CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC2 Trigger Source Select. Along with the SOC2 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC2 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-130. ADC_CFG_ADCSOC2CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC2 Channel Select. Selects the channel to be converted when SOC2 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC2 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.64 ADC_CFG_ADCSOC3CTL Register

3.2.2.64.1 ADC_CFG_ADCSOC3CTL Register (Offset = 2Ch) [reset = 0h]

ADC SOC3 Control Register.

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Table 3-131. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 002Ch
ADC1_G0_G5	502C 102Ch
ADC2_G0_G5	502C 202Ch
ADC3_G0_G5	502C 302Ch
ADC4_G0_G5	502C 402Ch

Figure 3-64. ADC_CFG_ADCSOC3CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-132. ADC_CFG_ADCSOC3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC3 External Channel Mux Select. Selects the external mux combination to output when SOC3 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-132. ADC_CFG_ADCSOC3CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC3 Trigger Source Select. Along with the SOC3 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC3 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-132. ADC_CFG_ADCSOC3CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC3 Channel Select. Selects the channel to be converted when SOC3 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC3 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.65 ADC_CFG_ADCSOC4CTL Register

3.2.2.65.1 ADC_CFG_ADCSOC4CTL Register (Offset = 30h) [reset = 0h]

ADC SOC4 Control Register.

Return to Summary Table

Table 3-133. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0030h
ADC1_G0_G5	502C 1030h
ADC2_G0_G5	502C 2030h
ADC3_G0_G5	502C 3030h
ADC4_G0_G5	502C 4030h

Figure 3-65. ADC_CFG_ADCSOC4CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-134. ADC_CFG_ADCSOC4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC4 External Channel Mux Select. Selects the external mux combination to output when SOC4 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-134. ADC_CFG_ADCSOC4CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC4 Trigger Source Select. Along with the SOC4 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC4 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-134. ADC_CFG_ADCSOC4CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC4 Channel Select. Selects the channel to be converted when SOC4 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC4 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.66 ADC_CFG_ADCSOC5CTL Register

3.2.2.66.1 ADC_CFG_ADCSOC5CTL Register (Offset = 34h) [reset = 0h]

ADC SOC5 Control Register.

Return to Summary Table

Table 3-135. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0034h
ADC1_G0_G5	502C 1034h
ADC2_G0_G5	502C 2034h
ADC3_G0_G5	502C 3034h
ADC4_G0_G5	502C 4034h

Figure 3-66. ADC_CFG_ADCSOC5CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-136. ADC_CFG_ADCSOC5CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC5 External Channel Mux Select. Selects the external mux combination to output when SOC5 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-136. ADC_CFG_ADCSOC5CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC5 Trigger Source Select. Along with the SOC5 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC5 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-136. ADC_CFG_ADCSOC5CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC5 Channel Select. Selects the channel to be converted when SOC5 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC5 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.67 ADC_CFG_ADCSOC6CTL Register

3.2.2.67.1 ADC_CFG_ADCSOC6CTL Register (Offset = 38h) [reset = 0h]

ADC SOC6 Control Register.

Return to Summary Table

Table 3-137. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0038h
ADC1_G0_G5	502C 1038h
ADC2_G0_G5	502C 2038h
ADC3_G0_G5	502C 3038h
ADC4_G0_G5	502C 4038h

Figure 3-67. ADC_CFG_ADCSOC6CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-138. ADC_CFG_ADCSOC6CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC6 External Channel Mux Select. Selects the external mux combination to output when SOC6 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-138. ADC_CFG_ADCSOC6CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC6 Trigger Source Select. Along with the SOC6 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC6 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-138. ADC_CFG_ADCSOC6CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC6 Channel Select. Selects the channel to be converted when SOC6 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC6 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.68 ADC_CFG_ADCSOC7CTL Register

3.2.2.68.1 ADC_CFG_ADCSOC7CTL Register (Offset = 3Ch) [reset = 0h]

ADC SOC7 Control Register.

Return to Summary Table

Table 3-139. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 003Ch
ADC1_G0_G5	502C 103Ch
ADC2_G0_G5	502C 203Ch
ADC3_G0_G5	502C 303Ch
ADC4_G0_G5	502C 403Ch

Figure 3-68. ADC_CFG_ADCSOC7CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-140. ADC_CFG_ADCSOC7CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC7 External Channel Mux Select. Selects the external mux combination to output when SOC7 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-140. ADC_CFG_ADCSOC7CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC7 Trigger Source Select. Along with the SOC7 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC7 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-140. ADC_CFG_ADCSOC7CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC7 Channel Select. Selects the channel to be converted when SOC7 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC7 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.69 ADC_CFG_ADCSOC8CTL Register

3.2.2.69.1 ADC_CFG_ADCSOC8CTL Register (Offset = 40h) [reset = 0h]

ADC SOC8 Control Register.

Return to Summary Table

Table 3-141. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0040h
ADC1_G0_G5	502C 1040h
ADC2_G0_G5	502C 2040h
ADC3_G0_G5	502C 3040h
ADC4_G0_G5	502C 4040h

Figure 3-69. ADC_CFG_ADCSOC8CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-142. ADC_CFG_ADCSOC8CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC8 External Channel Mux Select. Selects the external mux combination to output when SOC8 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-142. ADC_CFG_ADCSOC8CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC8 Trigger Source Select. Along with the SOC8 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC8 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-142. ADC_CFG_ADCSOC8CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC8 Channel Select. Selects the channel to be converted when SOC8 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC8 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.70 ADC_CFG_ADCSOC9CTL Register

3.2.2.70.1 ADC_CFG_ADCSOC9CTL Register (Offset = 44h) [reset = 0h]

ADC SOC9 Control Register.

Return to Summary Table

Table 3-143. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0044h
ADC1_G0_G5	502C 1044h
ADC2_G0_G5	502C 2044h
ADC3_G0_G5	502C 3044h
ADC4_G0_G5	502C 4044h

Figure 3-70. ADC_CFG_ADCSOC9CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-144. ADC_CFG_ADCSOC9CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC9 External Channel Mux Select. Selects the external mux combination to output when SOC9 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-144. ADC_CFG_ADCSOC9CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC9 Trigger Source Select. Along with the SOC9 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC9 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-144. ADC_CFG_ADCSOC9CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC9 Channel Select. Selects the channel to be converted when SOC9 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC9 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.71 ADC_CFG_ADCSOC10CTL Register

3.2.2.71.1 ADC_CFG_ADCSOC10CTL Register (Offset = 48h) [reset = 0h]

ADC SOC10 Control Register.

Return to Summary Table

Table 3-145. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0048h
ADC1_G0_G5	502C 1048h
ADC2_G0_G5	502C 2048h
ADC3_G0_G5	502C 3048h
ADC4_G0_G5	502C 4048h

Figure 3-71. ADC_CFG_ADCSOC10CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-146. ADC_CFG_ADCSOC10CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC10 External Channel Mux Select. Selects the external mux combination to output when SOC10 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-146. ADC_CFG_ADCSOC10CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC10 Trigger Source Select. Along with the SOC10 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC10 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-146. ADC_CFG_ADCSOC10CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC10 Channel Select. Selects the channel to be converted when SOC10 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC10 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.72 ADC_CFG_ADCSOC11CTL Register

3.2.2.72.1 ADC_CFG_ADCSOC11CTL Register (Offset = 4Ch) [reset = 0h]

ADC SOC11 Control Register.

Return to Summary Table

Table 3-147. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 004Ch
ADC1_G0_G5	502C 104Ch
ADC2_G0_G5	502C 204Ch
ADC3_G0_G5	502C 304Ch
ADC4_G0_G5	502C 404Ch

Figure 3-72. ADC_CFG_ADCSOC11CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-148. ADC_CFG_ADCSOC11CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC11 External Channel Mux Select. Selects the external mux combination to output when SOC11 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-148. ADC_CFG_ADCSOC11CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC11 Trigger Source Select. Along with the SOC11 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC11 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-148. ADC_CFG_ADCSOC11CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC11 Channel Select. Selects the channel to be converted when SOC11 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC11 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.73 ADC_CFG_ADCSOC12CTL Register

3.2.2.73.1 ADC_CFG_ADCSOC12CTL Register (Offset = 50h) [reset = 0h]

ADC SOC12 Control Register.

Return to Summary Table

Table 3-149. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0050h
ADC1_G0_G5	502C 1050h
ADC2_G0_G5	502C 2050h
ADC3_G0_G5	502C 3050h
ADC4_G0_G5	502C 4050h

Figure 3-73. ADC_CFG_ADCSOC12CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-150. ADC_CFG_ADCSOC12CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC12 External Channel Mux Select. Selects the external mux combination to output when SOC12 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-150. ADC_CFG_ADCSOC12CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC12 Trigger Source Select. Along with the SOC12 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC12 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-150. ADC_CFG_ADCSOC12CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC12 Channel Select. Selects the channel to be converted when SOC12 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC12 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.74 ADC_CFG_ADCSOC13CTL Register

3.2.2.74.1 ADC_CFG_ADCSOC13CTL Register (Offset = 54h) [reset = 0h]

ADC SOC13 Control Register.

Return to Summary Table

Table 3-151. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0054h
ADC1_G0_G5	502C 1054h
ADC2_G0_G5	502C 2054h
ADC3_G0_G5	502C 3054h
ADC4_G0_G5	502C 4054h

Figure 3-74. ADC_CFG_ADCSOC13CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-152. ADC_CFG_ADCSOC13CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC13 External Channel Mux Select. Selects the external mux combination to output when SOC13 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-152. ADC_CFG_ADCSOC13CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC13 Trigger Source Select. Along with the SOC13 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC13 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-152. ADC_CFG_ADCSOC13CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC13 Channel Select. Selects the channel to be converted when SOC13 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC13 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.75 ADC_CFG_ADCSOC14CTL Register

3.2.2.75.1 ADC_CFG_ADCSOC14CTL Register (Offset = 58h) [reset = 0h]

ADC SOC14 Control Register.

Return to Summary Table

Table 3-153. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0058h
ADC1_G0_G5	502C 1058h
ADC2_G0_G5	502C 2058h
ADC3_G0_G5	502C 3058h
ADC4_G0_G5	502C 4058h

Figure 3-75. ADC_CFG_ADCSOC14CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	22	21	20	19	18	17	16
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	6	5	4	3	2	1	0
ACQPS							
R/W							
0h							

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Table 3-154. ADC_CFG_ADCSOC14CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC14 External Channel Mux Select. Selects the external mux combination to output when SOC14 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-154. ADC_CFG_ADCSOC14CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC14 Trigger Source Select. Along with the SOC14 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC14 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-154. ADC_CFG_ADCSOC14CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC14 Channel Select. Selects the channel to be converted when SOC14 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC14 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.76 ADC_CFG_ADCSOC15CTL Register

3.2.2.76.1 ADC_CFG_ADCSOC15CTL Register (Offset = 5Ch) [reset = 0h]

ADC SOC15 Control Register.

Return to Summary Table

Table 3-155. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 005Ch
ADC1_G0_G5	502C 105Ch
ADC2_G0_G5	502C 205Ch
ADC3_G0_G5	502C 305Ch
ADC4_G0_G5	502C 405Ch

Figure 3-76. ADC_CFG_ADCSOC15CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-156. ADC_CFG_ADCSOC15CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC15 External Channel Mux Select. Selects the external mux combination to output when SOC15 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-156. ADC_CFG_ADCSOC15CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC15 Trigger Source Select. Along with the SOC15 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC15 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-156. ADC_CFG_ADCSOC15CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC15 Channel Select. Selects the channel to be converted when SOC15 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC15 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.2.2.77 ADC_CFG_ADCEVTSTAT Register

3.2.2.77.1 ADC_CFG_ADCEVTSTAT Register (Offset = 60h) [reset = 0h]

ADC Event Status Register.

Return to Summary Table

Table 3-157. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0060h
ADC1_G0_G5	502C 1060h
ADC2_G0_G5	502C 2060h
ADC3_G0_G5	502C 3060h
ADC4_G0_G5	502C 4060h

Figure 3-77. ADC_CFG_ADCEVTSTAT Name Register

15	14	13	12	11	10	9	8
RESERVED_4	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED_3	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED_1	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-158. ADC_CFG_ADCEVTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_4	R	0h	Reserved
14	PPB4ZERO	R	0h	Post Processing Block 4 Zero Crossing Flag. When set indicates the ADCPPB4RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
13	PPB4TRIPLO	R	0h	Post Processing Block 4 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
12	PPB4TRIPHI	R	0h	Post Processing Block 4 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
11	RESERVED_3	R	0h	Reserved

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Table 3-158. ADC_CFG_ADCEVTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PPB3ZERO	R	0h	Post Processing Block 3 Zero Crossing Flag. When set indicates the ADCPPB3RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
9	PPB3TRIPLO	R	0h	Post Processing Block 3 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
8	PPB3TRIPHI	R	0h	Post Processing Block 3 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
7	RESERVED_2	R	0h	Reserved
6	PPB2ZERO	R	0h	Post Processing Block 2 Zero Crossing Flag. When set indicates the ADCPPB2RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
5	PPB2TRIPLO	R	0h	Post Processing Block 2 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
4	PPB2TRIPHI	R	0h	Post Processing Block 2 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
3	RESERVED_1	R	0h	Reserved
2	PPB1ZERO	R	0h	Post Processing Block 1 Zero Crossing Flag. When set indicates the ADCPPB1RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority

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Table 3-158. ADC_CFG_ADCEVTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PPB1TRIPLO	R	0h	Post Processing Block 1 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
0	PPB1TRIPHI	R	0h	Post Processing Block 1 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority

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3.2.2.78 ADC_CFG_ADCEVTCLR Register

3.2.2.78.1 ADC_CFG_ADCEVTCLR Register (Offset = 64h) [reset = 0h]

ADC Event Clear Register.

Return to Summary Table

Table 3-159. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0064h
ADC1_G0_G5	502C 1064h
ADC2_G0_G5	502C 2064h
ADC3_G0_G5	502C 3064h
ADC4_G0_G5	502C 4064h

Figure 3-78. ADC_CFG_ADCEVTCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_4	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED_3	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R	R/W1TS	R/W1TS	R/W1TS	R	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_2	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED_1	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R	R/W1TS	R/W1TS	R/W1TS	R	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-160. ADC_CFG_ADCEVTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_4	R	0h	Reserved
14	PPB4ZERO	R/W1TS	0h	Post Processing Block 4 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
13	PPB4TRIPLO	R/W1TS	0h	Post Processing Block 4 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
12	PPB4TRIPHI	R/W1TS	0h	Post Processing Block 4 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
11	RESERVED_3	R	0h	Reserved
10	PPB3ZERO	R/W1TS	0h	Post Processing Block 3 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
9	PPB3TRIPLO	R/W1TS	0h	Post Processing Block 3 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
8	PPB3TRIPHI	R/W1TS	0h	Post Processing Block 3 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
7	RESERVED_2	R	0h	Reserved

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Table 3-160. ADC_CFG_ADCEVTCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PPB2ZERO	R/W1TS	0h	Post Processing Block 2 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
5	PPB2TRIPLO	R/W1TS	0h	Post Processing Block 2 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
4	PPB2TRIPHI	R/W1TS	0h	Post Processing Block 2 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
3	RESERVED_1	R	0h	Reserved
2	PPB1ZERO	R/W1TS	0h	Post Processing Block 1 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
1	PPB1TRIPLO	R/W1TS	0h	Post Processing Block 1 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
0	PPB1TRIPHI	R/W1TS	0h	Post Processing Block 1 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority

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3.2.2.79 ADC_CFG_ADCEVTSEL Register

3.2.2.79.1 ADC_CFG_ADCEVTSEL Register (Offset = 68h) [reset = 0h]

ADC Event Selection Register.

Return to Summary Table

Table 3-161. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0068h
ADC1_G0_G5	502C 1068h
ADC2_G0_G5	502C 2068h
ADC3_G0_G5	502C 3068h
ADC4_G0_G5	502C 4068h

Figure 3-79. ADC_CFG_ADCEVTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_4	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED_3	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_2	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED_1	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-162. ADC_CFG_ADCEVTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_4	R	0h	Reserved
14	PPB4ZERO	R/W	0h	Post Processing Block 4 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
11	RESERVED_3	R	0h	Reserved
10	PPB3ZERO	R/W	0h	Post Processing Block 3 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
7	RESERVED_2	R	0h	Reserved

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Table 3-162. ADC_CFG_ADCEVTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PPB2ZERO	R/W	0h	Post Processing Block 2 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
3	RESERVED_1	R	0h	Reserved
2	PPB1ZERO	R/W	0h	Post Processing Block 1 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.

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3.2.2.80 ADC_CFG_ADCEVTINTSEL Register

3.2.2.80.1 ADC_CFG_ADCEVTINTSEL Register (Offset = 6Ch) [reset = 0h]

ADC Event Interrupt Selection Register.

Return to Summary Table

Table 3-163. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 006Ch
ADC1_G0_G5	502C 106Ch
ADC2_G0_G5	502C 206Ch
ADC3_G0_G5	502C 306Ch
ADC4_G0_G5	502C 406Ch

Figure 3-80. ADC_CFG_ADCEVTINTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_4	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED_3	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_2	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED_1	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-164. ADC_CFG_ADCEVTINTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_4	R	0h	Reserved
14	PPB4ZERO	R/W	0h	Post Processing Block 4 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
11	RESERVED_3	R	0h	Reserved
10	PPB3ZERO	R/W	0h	Post Processing Block 3 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
7	RESERVED_2	R	0h	Reserved

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Table 3-164. ADC_CFG_ADCEVTINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PPB2ZERO	R/W	0h	Post Processing Block 2 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
3	RESERVED_1	R	0h	Reserved
2	PPB1ZERO	R/W	0h	Post Processing Block 1 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.

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3.2.2.81 ADC_CFG_ADCCOUNTER Register

3.2.2.81.1 ADC_CFG_ADCCOUNTER Register (Offset = 72h) [reset = 0h]

ADC Counter Register.

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Table 3-165. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0072h
ADC1_G0_G5	502C 1072h
ADC2_G0_G5	502C 2072h
ADC3_G0_G5	502C 3072h
ADC4_G0_G5	502C 4072h

Figure 3-81. ADC_CFG_ADCCOUNTER Name Register

15	14	13	12	11	10	9	8
RESERVED_1				FREECOUNT			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FREECOUNT							
R							
0h							

Table 3-166. ADC_CFG_ADCCOUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	FREECOUNT	R	0h	ADC Free Running Counter Value. This bit field reflects the status of the free running ADC counter.

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3.2.2.82 ADC_CFG_ADCREV Register

3.2.2.82.1 ADC_CFG_ADCREV Register (Offset = 74h) [reset = 105h]

ADC Revision Register.

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Table 3-167. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0074h
ADC1_G0_G5	502C 1074h
ADC2_G0_G5	502C 2074h
ADC3_G0_G5	502C 3074h
ADC4_G0_G5	502C 4074h

Figure 3-82. ADC_CFG_ADCREV Name Register

15	14	13	12	11	10	9	8
REV							
R							
1h							
7	6	5	4	3	2	1	0
TYPE							
R							
5h							

Table 3-168. ADC_CFG_ADCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	REV	R	1h	ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h
7:0	TYPE	R	5h	ADC Type. Always set to 5 for this ADC.

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3.2.2.83 ADC_CFG_ADCPPB1CONFIG Register

3.2.2.83.1 ADC_CFG_ADCPPB1CONFIG Register (Offset = 80h) [reset = 0h]

ADC PPB1 Config Register.

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Table 3-169. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0080h
ADC1_G0_G5	502C 1080h
ADC2_G0_G5	502C 2080h
ADC3_G0_G5	502C 3080h
ADC4_G0_G5	502C 4080h

Figure 3-83. ADC_CFG_ADCPPB1CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	ABSEN	CBCEN	TWOSCOMPEN	CONFIG			
R	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			

Table 3-170. ADC_CFG_ADCPPB1CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6	ABSEN	R/W	0h	ADC Post Processing Block 1 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULx associated with ADCPPB1. This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT] 0 ADCPPB1RESULT = ADCRESULTx - ADCPPB1OFFREF 1 ADCPPB1RESULT = abs[ADCRESULTx - ADCPPB1OFFREF]
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 1 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB1RESULT register. 0 ADCPPB1RESULT = ADCRESULTx - ADCPPB1OFFREF 1 ADCPPB1RESULT = ADCPPB1OFFREF - ADCRESULTx

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Table 3-170. ADC_CFG_ADCPPB1CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CONFIG	R/W	0h	ADC Post Processing Block 1 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 1 0001 SOC1/EOC1/RESULT1 is associated with post processing block 1 0010 SOC2/EOC2/RESULT2 is associated with post processing block 1 0011 SOC3/EOC3/RESULT3 is associated with post processing block 1 0100 SOC4/EOC4/RESULT4 is associated with post processing block 1 0101 SOC5/EOC5/RESULT5 is associated with post processing block 1 0110 SOC6/EOC6/RESULT6 is associated with post processing block 1 0111 SOC7/EOC7/RESULT7 is associated with post processing block 1 1000 SOC8/EOC8/RESULT8 is associated with post processing block 1 1001 SOC9/EOC9/RESULT9 is associated with post processing block 1 1010 SOC10/EOC10/RESULT10 is associated with post processing block 1 1011 SOC11/EOC11/RESULT11 is associated with post processing block 1 1100 SOC12/EOC12/RESULT12 is associated with post processing block 1 1101 SOC13/EOC13/RESULT13 is associated with post processing block 1 1110 SOC14/EOC14/RESULT14 is associated with post processing block 1 1111 SOC15/EOC15/RESULT15 is associated with post processing block 1

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3.2.2.84 ADC_CFG_ADCPPB1STAMP Register

3.2.2.84.1 ADC_CFG_ADCPPB1STAMP Register (Offset = 82h) [reset = 0h]

ADC PPB1 Sample Delay Time Stamp Register.

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Table 3-171. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0082h
ADC1_G0_G5	502C 1082h
ADC2_G0_G5	502C 2082h
ADC3_G0_G5	502C 3082h
ADC4_G0_G5	502C 4082h

Figure 3-84. ADC_CFG_ADCPPB1STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DLYSTAMP			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0h							

Table 3-172. ADC_CFG_ADCPPB1STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DLYSTAMP	R	0h	ADC Post Processing Block 1 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.2.2.85 ADC_CFG_ADCPPB1OFFCAL Register

3.2.2.85.1 ADC_CFG_ADCPPB1OFFCAL Register (Offset = 84h) [reset = 0h]

ADC PPB1 Offset Calibration Register.

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Table 3-173. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0084h
ADC1_G0_G5	502C 1084h
ADC2_G0_G5	502C 2084h
ADC3_G0_G5	502C 3084h
ADC4_G0_G5	502C 4084h

Figure 3-85. ADC_CFG_ADCPPB1OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						OFFCAL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFCAL							
R/W							
0h							

Table 3-174. ADC_CFG_ADCPPB1OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	OFFCAL	R/W	0h	ADC Post Processing Block 1 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000hand FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000hand 0FFFh before being stored into the ADCRESULT register. Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.

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3.2.2.86 ADC_CFG_ADCPPB1OFFREF Register

3.2.2.86.1 ADC_CFG_ADCPPB1OFFREF Register (Offset = 86h) [reset = 0h]

ADC PPB1 Offset Reference Register.

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Table 3-175. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0086h
ADC1_G0_G5	502C 1086h
ADC2_G0_G5	502C 2086h
ADC3_G0_G5	502C 3086h
ADC4_G0_G5	502C 4086h

Figure 3-86. ADC_CFG_ADCPPB1OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0h							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0h							

Table 3-176. ADC_CFG_ADCPPB1OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFREF	R/W	0h	ADC Post Processing Block 1 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB1RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.2.2.87 ADC_CFG_ADCPPB1TRIPHI Register

3.2.2.87.1 ADC_CFG_ADCPPB1TRIPHI Register (Offset = 88h) [reset = 0h]

ADC PPB1 Trip High Register.

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Table 3-177. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0088h
ADC1_G0_G5	502C 1088h
ADC2_G0_G5	502C 2088h
ADC3_G0_G5	502C 3088h
ADC4_G0_G5	502C 4088h

Figure 3-87. ADC_CFG_ADCPPB1TRIPHI Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITHI							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITHI							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITHI							
R/W							
0h							

Table 3-178. ADC_CFG_ADCPPB1TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITHI	R/W	0h	ADC Post Processing Block 1 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPHI[23:17] will be ignored in 16 bit mode - TRIPHI[23:13] will be ignored in 12 bit mode

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3.2.2.88 ADC_CFG_ADCPPB1TRIPLO Register

3.2.2.88.1 ADC_CFG_ADCPPB1TRIPLO Register (Offset = 8Ch) [reset = 0h]

ADC PPB1 Trip Low/Trigger Time Stamp Register.

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Table 3-179. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 008Ch
ADC1_G0_G5	502C 108Ch
ADC2_G0_G5	502C 208Ch
ADC3_G0_G5	502C 308Ch
ADC4_G0_G5	502C 408Ch

Figure 3-88. ADC_CFG_ADCPPB1TRIPLO Name Register

31	30	29	28	27	26	25	24
REQSTAMP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REQSTAMP				LIMITLO2EN	RESERVED_1		LSIGN
R				R/W	R		R/W
0h				0h	0h		0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LIMITLO							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMITLO							
R/W							
0h							

Table 3-180. ADC_CFG_ADCPPB1TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	REQSTAMP	R	0h	ADC Post Processing Block 1 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19	LIMITLO2EN	R/W	0h	Extended Low Limit 2 Enable. 0 = Low limit set by ADCPPB1TRIPLO register. Not compatible with comparison with ADCPPB1PSUM or ADCPPB1SUM 1 = Low limit set by ADCPPB1TRIPLO2 register
18:17	RESERVED_1	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.
15:0	LIMITLO	R/W	0h	ADC Post Processing Block 1 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB1RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB1RESULT register.

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3.2.2.89 ADC_CFG_ADCPPB2CONFIG Register

3.2.2.89.1 ADC_CFG_ADCPPB2CONFIG Register (Offset = 90h) [reset = 1h]

ADC PPB2 Config Register.

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Table 3-181. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0090h
ADC1_G0_G5	502C 1090h
ADC2_G0_G5	502C 2090h
ADC3_G0_G5	502C 3090h
ADC4_G0_G5	502C 4090h

Figure 3-89. ADC_CFG_ADCPPB2CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	ABSEN	CBCEN	TWOSCOMPEN	CONFIG			
R	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	1h			

Table 3-182. ADC_CFG_ADCPPB2CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6	ABSEN	R/W	0h	ADC Post Processing Block 2 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULx associated with ADCPPB2. This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT] 0 ADCPPB2RESULT = ADCRESULTx - ADCPPB2OFFREF 1 ADCPPB2RESULT = abs[ADCRESULTx - ADCPPB2OFFREF]
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 2 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB2RESULT register. 0 ADCPPB2RESULT = ADCRESULTx - ADCPPB2OFFREF 1 ADCPPB2RESULT = ADCPPB2OFFREF - ADCRESULTx

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Table 3-182. ADC_CFG_ADCPPB2CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CONFIG	R/W	1h	ADC Post Processing Block 2 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 2 0001 SOC1/EOC1/RESULT1 is associated with post processing block 2 0010 SOC2/EOC2/RESULT2 is associated with post processing block 2 0011 SOC3/EOC3/RESULT3 is associated with post processing block 2 0100 SOC4/EOC4/RESULT4 is associated with post processing block 2 0101 SOC5/EOC5/RESULT5 is associated with post processing block 2 0110 SOC6/EOC6/RESULT6 is associated with post processing block 2 0111 SOC7/EOC7/RESULT7 is associated with post processing block 2 1000 SOC8/EOC8/RESULT8 is associated with post processing block 2 1001 SOC9/EOC9/RESULT9 is associated with post processing block 2 1010 SOC10/EOC10/RESULT10 is associated with post processing block 2 1011 SOC11/EOC11/RESULT11 is associated with post processing block 2 1100 SOC12/EOC12/RESULT12 is associated with post processing block 2 1101 SOC13/EOC13/RESULT13 is associated with post processing block 2 1110 SOC14/EOC14/RESULT14 is associated with post processing block 2 1111 SOC15/EOC15/RESULT15 is associated with post processing block 2

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3.2.2.90 ADC_CFG_ADCPPB2STAMP Register

3.2.2.90.1 ADC_CFG_ADCPPB2STAMP Register (Offset = 92h) [reset = 0h]

ADC PPB2 Sample Delay Time Stamp Register.

Return to Summary Table

Table 3-183. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0092h
ADC1_G0_G5	502C 1092h
ADC2_G0_G5	502C 2092h
ADC3_G0_G5	502C 3092h
ADC4_G0_G5	502C 4092h

Figure 3-90. ADC_CFG_ADCPPB2STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DLYSTAMP			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0h							

Table 3-184. ADC_CFG_ADCPPB2STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DLYSTAMP	R	0h	ADC Post Processing Block 2 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.2.2.91 ADC_CFG_ADCPPB2OFFCAL Register

3.2.2.91.1 ADC_CFG_ADCPPB2OFFCAL Register (Offset = 94h) [reset = 0h]

ADC PPB2 Offset Calibration Register.

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Table 3-185. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0094h
ADC1_G0_G5	502C 1094h
ADC2_G0_G5	502C 2094h
ADC3_G0_G5	502C 3094h
ADC4_G0_G5	502C 4094h

Figure 3-91. ADC_CFG_ADCPPB2OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						OFFCAL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFCAL							
R/W							
0h							

Table 3-186. ADC_CFG_ADCPPB2OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	OFFCAL	R/W	0h	ADC Post Processing Block 2 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000hand FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000hand 0FFFh before being stored into the ADCRESULT register. Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.

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3.2.2.92 ADC_CFG_ADCPPB2OFFREF Register

3.2.2.92.1 ADC_CFG_ADCPPB2OFFREF Register (Offset = 96h) [reset = 0h]

ADC PPB2 Offset Reference Register.

Return to Summary Table

Table 3-187. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0096h
ADC1_G0_G5	502C 1096h
ADC2_G0_G5	502C 2096h
ADC3_G0_G5	502C 3096h
ADC4_G0_G5	502C 4096h

Figure 3-92. ADC_CFG_ADCPPB2OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFREF							
R/W							
0h							

Table 3-188. ADC_CFG_ADCPPB2OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFREF	R/W	0h	ADC Post Processing Block 2 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB2RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.2.2.93 ADC_CFG_ADCPPB2TRIPHI Register

3.2.2.93.1 ADC_CFG_ADCPPB2TRIPHI Register (Offset = 98h) [reset = 0h]

ADC PPB2 Trip High Register.

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Table 3-189. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0098h
ADC1_G0_G5	502C 1098h
ADC2_G0_G5	502C 2098h
ADC3_G0_G5	502C 3098h
ADC4_G0_G5	502C 4098h

Figure 3-93. ADC_CFG_ADCPPB2TRIPHI Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITHI							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITHI							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITHI							
R/W							
0h							

Table 3-190. ADC_CFG_ADCPPB2TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITHI	R/W	0h	ADC Post Processing Block 2 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPHI[23:17] will be ignored in 16 bit mode - TRIPHI[23:13] will be ignored in 12 bit mode

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3.2.2.94 ADC_CFG_ADCPPB2TRIPLO Register

3.2.2.94.1 ADC_CFG_ADCPPB2TRIPLO Register (Offset = 9Ch) [reset = 0h]

ADC PPB2 Trip Low/Trigger Time Stamp Register.

Return to Summary Table

Table 3-191. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 009Ch
ADC1_G0_G5	502C 109Ch
ADC2_G0_G5	502C 209Ch
ADC3_G0_G5	502C 309Ch
ADC4_G0_G5	502C 409Ch

Figure 3-94. ADC_CFG_ADCPPB2TRIPLO Name Register

31	30	29	28	27	26	25	24
REQSTAMP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REQSTAMP				LIMITLO2EN	RESERVED_1		LSIGN
R				R/W	R		R/W
0h				0h	0h		0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LIMITLO							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMITLO							
R/W							
0h							

Table 3-192. ADC_CFG_ADCPPB2TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	REQSTAMP	R	0h	ADC Post Processing Block 2 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19	LIMITLO2EN	R/W	0h	Extended Low Limit 2 Enable. 0 = Low limit set by ADCPPB2TRIPLO register. Not compatible with comparison with ADCPPB2PSUM or ADCPPB2SUM 1 = Low limit set by ADCPPB2TRIPLO2 register
18:17	RESERVED_1	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.
15:0	LIMITLO	R/W	0h	ADC Post Processing Block 2 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB2RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB2RESULT register.

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3.2.2.95 ADC_CFG_ADCPPB3CONFIG Register

3.2.2.95.1 ADC_CFG_ADCPPB3CONFIG Register (Offset = A0h) [reset = 2h]

ADC PPB3 Config Register.

Return to Summary Table

Table 3-193. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00A0h
ADC1_G0_G5	502C 10A0h
ADC2_G0_G5	502C 20A0h
ADC3_G0_G5	502C 30A0h
ADC4_G0_G5	502C 40A0h

Figure 3-95. ADC_CFG_ADCPPB3CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	ABSEN	CBCEN	TWOSCOMPEN	CONFIG			
R	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	2h			

Table 3-194. ADC_CFG_ADCPPB3CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6	ABSEN	R/W	0h	ADC Post Processing Block 3 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULx associated with ADCPPB3. This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT] 0 ADCPPB3RESULT = ADCRESULTx - ADCPPB3OFFREF 1 ADCPPB3RESULT = abs[ADCRESULTx - ADCPPB3OFFREF]
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 3 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB3RESULT register. 0 ADCPPB3RESULT = ADCRESULTx - ADCPPB3OFFREF 1 ADCPPB3RESULT = ADCPPB3OFFREF - ADCRESULTx

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Table 3-194. ADC_CFG_ADCPPB3CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CONFIG	R/W	2h	ADC Post Processing Block 3 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 3 0001 SOC1/EOC1/RESULT1 is associated with post processing block 3 0010 SOC2/EOC2/RESULT2 is associated with post processing block 3 0011 SOC3/EOC3/RESULT3 is associated with post processing block 3 0100 SOC4/EOC4/RESULT4 is associated with post processing block 3 0101 SOC5/EOC5/RESULT5 is associated with post processing block 3 0110 SOC6/EOC6/RESULT6 is associated with post processing block 3 0111 SOC7/EOC7/RESULT7 is associated with post processing block 3 1000 SOC8/EOC8/RESULT8 is associated with post processing block 3 1001 SOC9/EOC9/RESULT9 is associated with post processing block 3 1010 SOC10/EOC10/RESULT10 is associated with post processing block 3 1011 SOC11/EOC11/RESULT11 is associated with post processing block 3 1100 SOC12/EOC12/RESULT12 is associated with post processing block 3 1101 SOC13/EOC13/RESULT13 is associated with post processing block 3 1110 SOC14/EOC14/RESULT14 is associated with post processing block 3 1111 SOC15/EOC15/RESULT15 is associated with post processing block 3

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3.2.2.96 ADC_CFG_ADCPPB3STAMP Register

3.2.2.96.1 ADC_CFG_ADCPPB3STAMP Register (Offset = A2h) [reset = 0h]

ADC PPB3 Sample Delay Time Stamp Register.

Return to Summary Table

Table 3-195. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00A2h
ADC1_G0_G5	502C 10A2h
ADC2_G0_G5	502C 20A2h
ADC3_G0_G5	502C 30A2h
ADC4_G0_G5	502C 40A2h

Figure 3-96. ADC_CFG_ADCPPB3STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DLYSTAMP			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0h							

Table 3-196. ADC_CFG_ADCPPB3STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DLYSTAMP	R	0h	ADC Post Processing Block 3 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.2.2.97 ADC_CFG_ADCPPB3OFFCAL Register

3.2.2.97.1 ADC_CFG_ADCPPB3OFFCAL Register (Offset = A4h) [reset = 0h]

ADC PPB3 Offset Calibration Register.

Return to Summary Table

Table 3-197. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00A4h
ADC1_G0_G5	502C 10A4h
ADC2_G0_G5	502C 20A4h
ADC3_G0_G5	502C 30A4h
ADC4_G0_G5	502C 40A4h

Figure 3-97. ADC_CFG_ADCPPB3OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						OFFCAL	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
OFFCAL							
R/W							
0h							

Table 3-198. ADC_CFG_ADCPPB3OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	OFFCAL	R/W	0h	ADC Post Processing Block 3 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000hand FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000hand 0FFFh before being stored into the ADCRESULT register. Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.

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3.2.2.98 ADC_CFG_ADCPPB3OFFREF Register

3.2.2.98.1 ADC_CFG_ADCPPB3OFFREF Register (Offset = A6h) [reset = 0h]

ADC PPB3 Offset Reference Register.

Return to Summary Table

Table 3-199. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00A6h
ADC1_G0_G5	502C 10A6h
ADC2_G0_G5	502C 20A6h
ADC3_G0_G5	502C 30A6h
ADC4_G0_G5	502C 40A6h

Figure 3-98. ADC_CFG_ADCPPB3OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFREF							
R/W							
0h							

Table 3-200. ADC_CFG_ADCPPB3OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFREF	R/W	0h	ADC Post Processing Block 3 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB3RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.2.2.99 ADC_CFG_ADCPPB3TRIPHI Register

3.2.2.99.1 ADC_CFG_ADCPPB3TRIPHI Register (Offset = A8h) [reset = 0h]

ADC PPB3 Trip High Register.

Return to Summary Table

Table 3-201. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00A8h
ADC1_G0_G5	502C 10A8h
ADC2_G0_G5	502C 20A8h
ADC3_G0_G5	502C 30A8h
ADC4_G0_G5	502C 40A8h

Figure 3-99. ADC_CFG_ADCPPB3TRIPHI Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITHI							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITHI							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITHI							
R/W							
0h							

Table 3-202. ADC_CFG_ADCPPB3TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITHI	R/W	0h	ADC Post Processing Block 3 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPHI[23:17] will be ignored in 16 bit mode - TRIPHI[23:13] will be ignored in 12 bit mode

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3.2.2.100 ADC_CFG_ADCPPB3TRIPLO Register

3.2.2.100.1 ADC_CFG_ADCPPB3TRIPLO Register (Offset = ACh) [reset = 0h]

ADC PPB3 Trip Low/Trigger Time Stamp Register.

Return to Summary Table

Table 3-203. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00ACh
ADC1_G0_G5	502C 10ACh
ADC2_G0_G5	502C 20ACh
ADC3_G0_G5	502C 30ACh
ADC4_G0_G5	502C 40ACh

Figure 3-100. ADC_CFG_ADCPPB3TRIPLO Name Register

31	30	29	28	27	26	25	24
REQSTAMP							
R							
0h							
23	22	21	20	19	18	17	16
REQSTAMP				LIMITLO2EN	RESERVED_1		LSIGN
R				R/W	R		R/W
0h				0h	0h		0h
15	14	13	12	11	10	9	8
LIMITLO							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITLO							
R/W							
0h							

Table 3-204. ADC_CFG_ADCPPB3TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	REQSTAMP	R	0h	ADC Post Processing Block 3 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19	LIMITLO2EN	R/W	0h	Extended Low Limit 2 Enable. 0 = Low limit set by ADCPPB3TRIPLO register. Not compatible with comparison with ADCPPB3PSUM or ADCPPB3SUM 1 = Low limit set by ADCPPB3TRIPLO2 register
18:17	RESERVED_1	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.
15:0	LIMITLO	R/W	0h	ADC Post Processing Block 3 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB3RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB3RESULT register.

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3.2.2.101 ADC_CFG_ADCPPB4CONFIG Register

3.2.2.101.1 ADC_CFG_ADCPPB4CONFIG Register (Offset = B0h) [reset = 3h]

ADC PPB4 Config Register.

Return to Summary Table

Table 3-205. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00B0h
ADC1_G0_G5	502C 10B0h
ADC2_G0_G5	502C 20B0h
ADC3_G0_G5	502C 30B0h
ADC4_G0_G5	502C 40B0h

Figure 3-101. ADC_CFG_ADCPPB4CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	ABSEN	CBCEN	TWOSCOMPEN	CONFIG			
R	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	3h			

Table 3-206. ADC_CFG_ADCPPB4CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6	ABSEN	R/W	0h	ADC Post Processing Block 4 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULx associated with ADCPPB4. This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT] 0 ADCPPB4RESULT = ADCRESULTx - ADCPPB4OFFREF 1 ADCPPB4RESULT = abs[ADCRESULTx - ADCPPB4OFFREF]
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 4 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB4RESULT register. 0 ADCPPB4RESULT = ADCRESULTx - ADCPPB4OFFREF 1 ADCPPB4RESULT = ADCPPB4OFFREF - ADCRESULTx

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Table 3-206. ADC_CFG_ADCPPB4CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CONFIG	R/W	3h	ADC Post Processing Block 4 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 4 0001 SOC1/EOC1/RESULT1 is associated with post processing block 4 0010 SOC2/EOC2/RESULT2 is associated with post processing block 4 0011 SOC3/EOC3/RESULT3 is associated with post processing block 4 0100 SOC4/EOC4/RESULT4 is associated with post processing block 4 0101 SOC5/EOC5/RESULT5 is associated with post processing block 4 0110 SOC6/EOC6/RESULT6 is associated with post processing block 4 0111 SOC7/EOC7/RESULT7 is associated with post processing block 4 1000 SOC8/EOC8/RESULT8 is associated with post processing block 4 1001 SOC9/EOC9/RESULT9 is associated with post processing block 4 1010 SOC10/EOC10/RESULT10 is associated with post processing block 4 1011 SOC11/EOC11/RESULT11 is associated with post processing block 4 1100 SOC12/EOC12/RESULT12 is associated with post processing block 4 1101 SOC13/EOC13/RESULT13 is associated with post processing block 4 1110 SOC14/EOC14/RESULT14 is associated with post processing block 4 1111 SOC15/EOC15/RESULT15 is associated with post processing block 4

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3.2.2.102 ADC_CFG_ADCPPB4STAMP Register

3.2.2.102.1 ADC_CFG_ADCPPB4STAMP Register (Offset = B2h) [reset = 0h]

ADC PPB4 Sample Delay Time Stamp Register.

Return to Summary Table

Table 3-207. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00B2h
ADC1_G0_G5	502C 10B2h
ADC2_G0_G5	502C 20B2h
ADC3_G0_G5	502C 30B2h
ADC4_G0_G5	502C 40B2h

Figure 3-102. ADC_CFG_ADCPPB4STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DLYSTAMP			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0h							

Table 3-208. ADC_CFG_ADCPPB4STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DLYSTAMP	R	0h	ADC Post Processing Block 4 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.2.2.103 ADC_CFG_ADCPPB4OFFCAL Register

3.2.2.103.1 ADC_CFG_ADCPPB4OFFCAL Register (Offset = B4h) [reset = 0h]

ADC PPB4 Offset Calibration Register.

Return to Summary Table

Table 3-209. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00B4h
ADC1_G0_G5	502C 10B4h
ADC2_G0_G5	502C 20B4h
ADC3_G0_G5	502C 30B4h
ADC4_G0_G5	502C 40B4h

Figure 3-103. ADC_CFG_ADCPPB4OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						OFFCAL	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
OFFCAL							
R/W							
0h							

Table 3-210. ADC_CFG_ADCPPB4OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	OFFCAL	R/W	0h	ADC Post Processing Block 4 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000hand FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000hand 0FFFh before being stored into the ADCRESULT register. Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.

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3.2.2.104 ADC_CFG_ADCPPB4OFFREF Register

3.2.2.104.1 ADC_CFG_ADCPPB4OFFREF Register (Offset = B6h) [reset = 0h]

ADC PPB4 Offset Reference Register.

Return to Summary Table

Table 3-211. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00B6h
ADC1_G0_G5	502C 10B6h
ADC2_G0_G5	502C 20B6h
ADC3_G0_G5	502C 30B6h
ADC4_G0_G5	502C 40B6h

Figure 3-104. ADC_CFG_ADCPPB4OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0h							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0h							

Table 3-212. ADC_CFG_ADCPPB4OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFREF	R/W	0h	ADC Post Processing Block 4 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB4RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.2.2.105 ADC_CFG_ADCPPB4TRIPHI Register

3.2.2.105.1 ADC_CFG_ADCPPB4TRIPHI Register (Offset = B8h) [reset = 0h]

ADC PPB4 Trip High Register.

Return to Summary Table

Table 3-213. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00B8h
ADC1_G0_G5	502C 10B8h
ADC2_G0_G5	502C 20B8h
ADC3_G0_G5	502C 30B8h
ADC4_G0_G5	502C 40B8h

Figure 3-105. ADC_CFG_ADCPPB4TRIPHI Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITHI							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITHI							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITHI							
R/W							
0h							

Table 3-214. ADC_CFG_ADCPPB4TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITHI	R/W	0h	ADC Post Processing Block 4 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPHI[23:17] will be ignored in 16 bit mode - TRIPHI[23:13] will be ignored in 12 bit mode

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3.2.2.106 ADC_CFG_ADCPPB4TRIPLO Register

3.2.2.106.1 ADC_CFG_ADCPPB4TRIPLO Register (Offset = BCh) [reset = 0h]

ADC PPB4 Trip Low/Trigger Time Stamp Register.

Return to Summary Table

Table 3-215. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00BCh
ADC1_G0_G5	502C 10BCh
ADC2_G0_G5	502C 20BCh
ADC3_G0_G5	502C 30BCh
ADC4_G0_G5	502C 40BCh

Figure 3-106. ADC_CFG_ADCPPB4TRIPLO Name Register

31	30	29	28	27	26	25	24
REQSTAMP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REQSTAMP				LIMITLO2EN	RESERVED_1		LSIGN
R				R/W	R		R/W
0h				0h	0h		0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LIMITLO							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMITLO							
R/W							
0h							

Table 3-216. ADC_CFG_ADCPPB4TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	REQSTAMP	R	0h	ADC Post Processing Block 4 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19	LIMITLO2EN	R/W	0h	Extended Low Limit 2 Enable. 0 = Low limit set by ADCPPB4TRIPLO register. Not compatible with comparison with ADCPPB4PSUM or ADCPPB4SUM 1 = Low limit set by ADCPPB4TRIPLO2 register
18:17	RESERVED_1	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.
15:0	LIMITLO	R/W	0h	ADC Post Processing Block 4 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB4RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB4RESULT register.

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3.2.2.107 ADC_CFG_ADCSAFECHECKRESEN Register

3.2.2.107.1 ADC_CFG_ADCSAFECHECKRESEN Register (Offset = C0h) [reset = 0h]

ADC Safe Check Result Enable Register.

Return to Summary Table

Table 3-217. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00C0h
ADC1_G0_G5	502C 10C0h
ADC2_G0_G5	502C 20C0h
ADC3_G0_G5	502C 30C0h
ADC4_G0_G5	502C 40C0h

Figure 3-107. ADC_CFG_ADCSAFECHECKRESEN Name Register

31	30	29	28	27	26	25	24
SOC15CHKEN		SOC14CHKEN		SOC13CHKEN		SOC12CHKEN	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	22	21	20	19	18	17	16
SOC11CHKEN		SOC10CHKEN		SOC9CHKEN		SOC8CHKEN	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
15	14	13	12	11	10	9	8
SOC7CHKEN		SOC6CHKEN		SOC5CHKEN		SOC4CHKEN	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
SOC3CHKEN		SOC2CHKEN		SOC1CHKEN		SOC0CHKEN	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-218. ADC_CFG_ADCSAFECHECKRESEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SOC15CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT15 passed to safety checker 10 PPB Result associated with SOC15 passed to safety checker 11 PPB Sum associated with SOC15 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
29:28	SOC14CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT14 passed to safety checker 10 PPB Result associated with SOC14 passed to safety checker 11 PPB Sum associated with SOC14 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker

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Table 3-218. ADC_CFG_ADCSAFECHECKRESEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:26	SOC13CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT13 passed to safety checker 10 PPB Result associated with SOC13 passed to safety checker 11 PPB Sum associated with SOC13 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
25:24	SOC12CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT12 passed to safety checker 10 PPB Result associated with SOC12 passed to safety checker 11 PPB Sum associated with SOC12 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
23:22	SOC11CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT11 passed to safety checker 10 PPB Result associated with SOC11 passed to safety checker 11 PPB Sum associated with SOC11 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
21:20	SOC10CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT10 passed to safety checker 10 PPB Result associated with SOC10 passed to safety checker 11 PPB Sum associated with SOC10 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
19:18	SOC9CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT9 passed to safety checker 10 PPB Result associated with SOC9 passed to safety checker 11 PPB Sum associated with SOC9 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
17:16	SOC8CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT8 passed to safety checker 10 PPB Result associated with SOC8 passed to safety checker 11 PPB Sum associated with SOC8 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker

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Table 3-218. ADC_CFG_ADCSAFECHECKRESEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SOC7CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT7 passed to safety checker 10 PPB Result associated with SOC7 passed to safety checker 11 PPB Sum associated with SOC7 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
13:12	SOC6CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT6 passed to safety checker 10 PPB Result associated with SOC6 passed to safety checker 11 PPB Sum associated with SOC6 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
11:10	SOC5CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT5 passed to safety checker 10 PPB Result associated with SOC5 passed to safety checker 11 PPB Sum associated with SOC5 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
9:8	SOC4CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT4 passed to safety checker 10 PPB Result associated with SOC4 passed to safety checker 11 PPB Sum associated with SOC4 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
7:6	SOC3CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT3 passed to safety checker 10 PPB Result associated with SOC3 passed to safety checker 11 PPB Sum associated with SOC3 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
5:4	SOC2CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT2 passed to safety checker 10 PPB Result associated with SOC2 passed to safety checker 11 PPB Sum associated with SOC2 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker

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Table 3-218. ADC_CFG_ADCSAFECHECKRESEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	SOC1CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT1 passed to safety checker 10 PPB Result associated with SOC1 passed to safety checker 11 PPB Sum associated with SOC1 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
1:0	SOC0CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT0 passed to safety checker 10 PPB Result associated with SOC0 passed to safety checker 11 PPB Sum associated with SOC0 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker

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3.2.2.108 ADC_CFG_ADCINTCYCLE Register

3.2.2.108.1 ADC_CFG_ADCINTCYCLE Register (Offset = DEh) [reset = 0h]

ADC Early Interrupt Generation Cycle.

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Table 3-219. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00DEh
ADC1_G0_G5	502C 10DEh
ADC2_G0_G5	502C 20DEh
ADC3_G0_G5	502C 30DEh
ADC4_G0_G5	502C 40DEh

Figure 3-108. ADC_CFG_ADCINTCYCLE Name Register

15	14	13	12	11	10	9	8
DELAY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DELAY							
R/W							
0h							

Table 3-220. ADC_CFG_ADCINTCYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DELAY	R/W	0h	ADC Early Interrupt Generation Cycle Delay: Defines the delay from the fall edge of ADCSOC in terms of system clock cycles, for the interrupt to be generated.

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3.2.2.109 ADC_CFG_ADCREV2 Register

3.2.2.109.1 ADC_CFG_ADCREV2 Register (Offset = FAh) [reset = 4h]

ADC Wrapper Revision Register.

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Table 3-221. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00FAh
ADC1_G0_G5	502C 10FAh
ADC2_G0_G5	502C 20FAh
ADC3_G0_G5	502C 30FAh
ADC4_G0_G5	502C 40FAh

Figure 3-109. ADC_CFG_ADCREV2 Name Register

15	14	13	12	11	10	9	8
WRAPPERREV							
R							
0h							
7	6	5	4	3	2	1	0
WRAPPERTYPE							
R							
4h							

Table 3-222. ADC_CFG_ADCREV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	WRAPPERREV	R	0h	ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h
7:0	WRAPPERTYPE	R	4h	ADC Wrapper Type. Always set to 4 for this ADC.

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3.2.2.110 ADC_CFG_ADCINLTRIMCTL Register

3.2.2.110.1 ADC_CFG_ADCINLTRIMCTL Register (Offset = FCh) [reset = 0h]

ADC Linearity Trim Control Register.

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Table 3-223. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 00FCh
ADC1_G0_G5	502C 10FCh
ADC2_G0_G5	502C 20FCh
ADC3_G0_G5	502C 30FCh
ADC4_G0_G5	502C 40FCh

Figure 3-110. ADC_CFG_ADCINLTRIMCTL Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1		CALIBSTEP					CALIBMODE
R		R/W					R/W
0h		0h					0h

Table 3-224. ADC_CFG_ADCINLTRIMCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	KEY	R/W	0h	ADC Linearity Trim Control Write Key. Any write to this register must contain the value 0xA5A5 in these bit locations. If a write request attempts to load any other value into these bits, the write for the entire register is ignored. These bits always read back a zero.
15:6	RESERVED_1	R	0h	Reserved
5:1	CALIBSTEP	R/W	0h	ADC Linearity Calibration Step. Defines which of the 24 steps of calibration is to be executed. Never set this bit field while the ADC SELFTRIM is in progress. The R-M-W operation could unintentionally set the CALIBMODE bit again.
0	CALIBMODE	R/W	0h	ADC Linearity Calibration Mode.

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3.2.2.111 ADC_CFG_REP1CTL Register

3.2.2.111.1 ADC_CFG_REP1CTL Register (Offset = 100h) [reset = 0h]

ADC Trigger Repeater 1 Control Register.

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Table 3-225. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0100h
ADC1_G0_G5	502C 1100h
ADC2_G0_G5	502C 2100h
ADC3_G0_G5	502C 3100h
ADC4_G0_G5	502C 4100h

Figure 3-111. ADC_CFG_REP1CTL Name Register

31	30	29	28	27	26	25	24
RESERVED_5							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SWSYNC	RESERVED_4	SYNCINSEL					
R/W1TS	R	R/W					
0h	0h	0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_3	TRIGGER						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIGGEROVF	PHASEOVF	RESERVED_2	SOCBUSY	MODULEBUSY	RESERVED_1	ACTIVEMODE	MODE
R/W1TC	R/W1TC	R	R	R	R	R	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-226. ADC_CFG_REP1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_5	R	0h	Reserved
23	SWSYNC	R/W1TS	0h	Trigger repeater 1 software force sync. On a sync. event, all registers in repeater 1 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved. Note: SOCs associated with repeater 1 are not cleared.
22	RESERVED_4	R	0h	Reserved
21:16	SYNCINSEL	R/W	0h	Trigger repeater 1 sync. input select. On a sync. event, all registers in repeater 1 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved. Note: SOCs associated with repeater 1 are not cleared.
15	RESERVED_3	R	0h	Reserved

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Table 3-226. ADC_CFG_REP1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:8	TRIGGER	R/W	0h	ADC Trigger Repeater 1 Trigger Select. Selects the trigger to modify via oversampling or undersampling. 00h REPTRIG0 - Software only 01h REPTRIG1 - RTI0 Timer 02h REPTRIG2 - RTI1 Timer 03h REPTRIG3 - RTI2 Timer 04h REPTRIG4 - RTI3 Timer 05h REPTRIG5 - InputXBAR.Out[5] 06h REPTRIG6 - spare 07h REPTRIG7 - spare 08h REPTRIG8 - EPWM0, ADCSOCA 09h REPTRIG9 - EPWM0, ADCSOCB 0Ah REPTRIG10 - EPWM1, ADCSOCA 0Bh REPTRIG11 - EPWM1, ADCSOCB 0Ch REPTRIG12 - EPWM2, ADCSOCA 0Dh REPTRIG13 - EPWM2, ADCSOCB 0Eh REPTRIG14 - EPWM3, ADCSOCA 0Fh REPTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h REPTRIG64 - EPWM28, ADCSOCA 41h REPTRIG65 - EPWM28, ADCSOCB 42h REPTRIG66 - EPWM29, ADCSOCA 43h REPTRIG67 - EPWM29, ADCSOCB 44h REPTRIG68 - EPWM30, ADCSOCA 45h REPTRIG69 - EPWM30, ADCSOCB 46h REPTRIG70 - EPWM31, ADCSOCA 47h REPTRIG71 - EPWM31, ADCSOCB 48h REPTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h REPTRIG81 - ECAP9, TRIGOUT 52h REPTRIG82 - ECAP10, TRIGOUT .... 57h REPTRIG73 - ECAP15, TRIGOUT 58h REPTRIG1 - RTI4 Timer 59h REPTRIG1 - RTI5 Timer 5Ah REPTRIG1 - RTI6 Timer 5Bh REPTRIG1 - RTI7 Timer .... 7Fh - Reserved
7	TRIGGEROVF	R/W1TC	0h	ADC Trigger Repeater 1 Oversampled Trigger Overflow. Indicates that a trigger was dropped because a trigger arrived while the repeater was still generating repeated oversampled triggers [NCOUNT was not 0 or SOCs associated with Repeater 1 were still pending]. Writing a 1 will clear this flag. Note: This flag won't be set in undersampling mode or when NSEL = 0; if a trigger arrives before the previous SOCs have completed, the trigger will be passed and the overflow flags of the SOCs that were still pending will be set. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
6	PHASEOVF	R/W1TC	0h	ADC Trigger Repeater 1 Phase Delay Overflow. Indicates that a trigger was dropped because a trigger arrived when the phase delay logic was still waiting to send the delayed trigger [PHASECOUNT was not 0]. Writing a 1 will clear this flag. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
5	RESERVED_2	R	0h	Reserved

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Table 3-226. ADC_CFG_REP1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SOCBUSY	R	0h	ADC Trigger Repeater 1 Associated SOCs Busy indicator. In oversampling mode: 0 = no SOCs associated with this repeater are pending 1 = SOCs associated with this repeater are still pending The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP1CTL.BUSY = 0 [SOCs associated with trigger repeater 1 are no longer pending]. Note: If the ADC is in burstmode and the BURSTTRIG is Repeater 1, then all round-robin SOCs are considered associated with this repeater and the repeater will not re-trigger until there are no pending round-robin SOCs [in addition to any associated pending high-priority SOCs].
3	MODULEBUSY	R	0h	ADC Trigger Repeater 1 Module Busy indicator. In oversampling mode: 0 = Repeater 1 is idle and can accept a new repeated trigger in oversampling mode 1 = Repeater 1 still has repeated triggers remaining [NCOUNT ' 0] or associated SOCs are still pending [SOCBUSY is 1] If a new oversampled trigger is received while the module is still busy, the TRIGGEROVF bit will be set and the trigger will be ignored.
2	RESERVED_1	R	0h	Reserved
1	ACTIVEMODE	R	0h	When a trigger is recived in oversampling or undersampling mode the value of MODE is copied to ACTIVEMODE. ACTIVEMODE determines if the repeater will repeat of filter triggers. Changes to MODE while the repeater is working therefore won't cause any changes in functionality until the module becomes idle and then a new trigger is received. 0 = module is oversampling 1 = module is undersampling
0	MODE	R/W	0h	ADC trigger repeater 1 mode selection. Select either oversampling or undersampling mode. In oversampling mode, when the trigger selected by REP1CTL.TRIGSEL is received, the repeater will repeat the trigger REP1N.NSEL + 1 times. In undersampling mode, when the trigger selected by REP1CTL.TRIGSEL is received the first time, the repeater will pass the trigger through. The next REP1N.NSEL triggers will be ignored. 0 = oversampling 1 = undersampling

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3.2.2.112 ADC_CFG_REP1N Register

3.2.2.112.1 ADC_CFG_REP1N Register (Offset = 104h) [reset = 0h]

ADC Trigger Repeater 1 N Select Register.

Return to Summary Table

Table 3-227. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0104h
ADC1_G0_G5	502C 1104h
ADC2_G0_G5	502C 2104h
ADC3_G0_G5	502C 3104h
ADC4_G0_G5	502C 4104h

Figure 3-112. ADC_CFG_REP1N Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2	NCOUNT						
R	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	NSEL						
R	R/W						
0h	0h						

Table 3-228. ADC_CFG_REP1N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED_2	R	0h	Reserved
22:16	NCOUNT	R	0h	ADC trigger repeater 1 trigger count. In oversampling mode, indicates the number of triggers remaining to be generated. If a trigger is received corresponding to REP1CTL.TRIGSEL while NCOUNT is not 0 [the repeater is still busy generating the repeated triggers] then the trigger will be ignored and REP1CTL.TRIGOVF will be set to 1. In undersampling mode, indicates the number of triggers remaining to be supressed.
15:7	RESERVED_1	R	0h	Reserved

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Table 3-228. ADC_CFG_REP1N Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	NSEL	R/W	0h	ADC Trigger Repeater 1 selection of number of triggers. In oversampling mode, selects the number of repeated triggers. For each trigger received corresponding to REP1CTL.TRIGSEL, NSEL + 1 triggers will be generated. 0 = 1 trigger is generated [pass-through] 1 = 2 triggers are generated 2 = 3 triggers are generated ... 127 = 128 triggers are generated In undersampling mode, selects the number triggers to be supressed. 1 out NSEL + 1 triggers received corresponding to REP1CTL.TRIGSEL will be passed through [the first trigger will be passed through and the subsequent NSEL triggers will be supressed]. 0 = all triggers are passed 1 = 1 out of 2 triggers are passed 2 = 1 out of 3 triggers are passed ... 127 = 1 out of 128 triggers are passed

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3.2.2.113 ADC_CFG_REP1PHASE Register

3.2.2.113.1 ADC_CFG_REP1PHASE Register (Offset = 108h) [reset = 0h]

ADC Trigger Repeater 1 Phase Select Register.

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Table 3-229. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0108h
ADC1_G0_G5	502C 1108h
ADC2_G0_G5	502C 2108h
ADC3_G0_G5	502C 3108h
ADC4_G0_G5	502C 4108h

Figure 3-113. ADC_CFG_REP1PHASE Name Register

31	30	29	28	27	26	25	24
PHASECOUNT							
R							
0h							
23	22	21	20	19	18	17	16
PHASECOUNT							
R							
0h							
15	14	13	12	11	10	9	8
PHASE							
R/W							
0h							
7	6	5	4	3	2	1	0
PHASE							
R/W							
0h							

Table 3-230. ADC_CFG_REP1PHASE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHASECOUNT	R	0h	ADC trigger repeater 1 phase delay status. When the trigger selected by REP1CTL.TRIGSEL is received, this register will start counting down from PHASECOUNT until the counter reaches 0, at which point the trigger will be passed on to the repeater re-trigger logic. If the trigger selected by REP1CTL.TRIGSEL is recieved when PHASECOUNT is not 0 [the phase delay logic is busy from the previous trigger] then the new trigger will be ignored and REP1CTL.PHASEOVF will be set to 1.
15:0	PHASE	R/W	0h	ADC trigger repeater 1 phase delay configuration. Defines the number of SYSCLKs to delay the selected trigger before passing it on to the re-triggering logic. 0 = trigger is passed through without delay 1 = trigger is delayed by 1 SYSCLK 2 = trigger is delayed by 2 SYSCLKs ... 65535 = trigger is delayed by 65535 SYSCLKs

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3.2.2.114 ADC_CFG_REP1SPREAD Register

3.2.2.114.1 ADC_CFG_REP1SPREAD Register (Offset = 10Ch) [reset = 0h]

ADC Trigger Repeater 1 Spread Select Register.

Return to Summary Table

Table 3-231. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 010Ch
ADC1_G0_G5	502C 110Ch
ADC2_G0_G5	502C 210Ch
ADC3_G0_G5	502C 310Ch
ADC4_G0_G5	502C 410Ch

Figure 3-114. ADC_CFG_REP1SPREAD Name Register

31	30	29	28	27	26	25	24
SPREADCOUNT							
R							
0h							
23	22	21	20	19	18	17	16
SPREADCOUNT							
R							
0h							
15	14	13	12	11	10	9	8
SPREAD							
R/W							
0h							
7	6	5	4	3	2	1	0
SPREAD							
R/W							
0h							

Table 3-232. ADC_CFG_REP1SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SPREADCOUNT	R	0h	ADC trigger repeater 1 spread status. When a trigger is sent to the ADC in oversampling mode, this register will start counting down from SPREAD until SPREADCOUNT equals 0. The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP1CTL.BUSY = 0 [SOCs associated with trigger repeater 1 are no longer pending].

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Table 3-232. ADC_CFG_REP1SPREAD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SPREAD	R/W	0h	ADC trigger repeater 1 spread delay configuration. In oversampling mode, defines the minimum number of SYSCLKs to wait before creating the next repeated trigger to the ADC. If SPREAD is less than the time needed for all SOCs associated with repeater 1 to sample and convert, then the repeater will generate triggers as fast as the ADC can convert the associated conversions. If SPREAD is greater than the time needed for all SOCs associated with repeater 1 to sample and convert, then repeated triggers to the ADC will be SPREAD SYSCLK cycles apart. 0 = oversampled repeated triggers occur as fast as the ADC can sample and convert associated SOCs 1 = time between repeated triggers is at least 1 SYSCLKs 2 = time between repeated triggers is at least 2 SYSCLKs ... 65535 = time between repeated triggers is at least 65535 SYSCLKs

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3.2.2.115 ADC_CFG_REP1FRC Register

3.2.2.115.1 ADC_CFG_REP1FRC Register (Offset = 110h) [reset = 0h]

ADC Trigger Repeater 1 Software Force Register.

Return to Summary Table

Table 3-233. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0110h
ADC1_G0_G5	502C 1110h
ADC2_G0_G5	502C 2110h
ADC3_G0_G5	502C 3110h
ADC4_G0_G5	502C 4110h

Figure 3-115. ADC_CFG_REP1FRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							SWFRC
R							R/W1TS
0h							0h

Table 3-234. ADC_CFG_REP1FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	SWFRC	R/W1TS	0h	Write 1 to force a trigger to repeat block 1 input regardless of the value of TRIGGER. Always reads 0.

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3.2.2.116 ADC_CFG_REP2CTL Register

3.2.2.116.1 ADC_CFG_REP2CTL Register (Offset = 120h) [reset = 0h]

ADC Trigger Repeater 2 Control Register.

Return to Summary Table

Table 3-235. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0120h
ADC1_G0_G5	502C 1120h
ADC2_G0_G5	502C 2120h
ADC3_G0_G5	502C 3120h
ADC4_G0_G5	502C 4120h

Figure 3-116. ADC_CFG_REP2CTL Name Register

31	30	29	28	27	26	25	24
RESERVED_5							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SWSYNC	RESERVED_4	SYNCINSEL					
R/W1TS	R	R/W					
0h	0h	0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_3	TRIGGER						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIGGEROVF	PHASEOVF	RESERVED_2	SOCBUSY	MODULEBUSY	RESERVED_1	ACTIVEMODE	MODE
R/W1TC	R/W1TC	R	R	R	R	R	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-236. ADC_CFG_REP2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_5	R	0h	Reserved
23	SWSYNC	R/W1TS	0h	Trigger repeater 2 software force sync. On a sync. event, all registers in repeater 2 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved. Note: SOCs associated with repeater 2 are not cleared.
22	RESERVED_4	R	0h	Reserved
21:16	SYNCINSEL	R/W	0h	Trigger repeater 2 sync. input select. On a sync. event, all registers in repeater 2 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved. Note: SOCs associated with repeater 2 are not cleared.
15	RESERVED_3	R	0h	Reserved

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Table 3-236. ADC_CFG_REP2CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:8	TRIGGER	R/W	0h	ADC Trigger Repeater 2 Trigger Select. Selects the trigger to modify via oversampling or undersampling. 00h REPTRIG0 - Software only 01h REPTRIG1 - RTI0 Timer 02h REPTRIG2 - RTI1 Timer 03h REPTRIG3 - RTI2 Timer 04h REPTRIG4 - RTI3 Timer 05h REPTRIG5 - InputXBAR.Out[5] 06h REPTRIG6 - spare 07h REPTRIG7 - spare 08h REPTRIG8 - EPWM0, ADCSOCA 09h REPTRIG9 - EPWM0, ADCSOCB 0Ah REPTRIG10 - EPWM1, ADCSOCA 0Bh REPTRIG11 - EPWM1, ADCSOCB 0Ch REPTRIG12 - EPWM2, ADCSOCA 0Dh REPTRIG13 - EPWM2, ADCSOCB 0Eh REPTRIG14 - EPWM3, ADCSOCA 0Fh REPTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h REPTRIG64 - EPWM28, ADCSOCA 41h REPTRIG65 - EPWM28, ADCSOCB 42h REPTRIG66 - EPWM29, ADCSOCA 43h REPTRIG67 - EPWM29, ADCSOCB 44h REPTRIG68 - EPWM30, ADCSOCA 45h REPTRIG69 - EPWM30, ADCSOCB 46h REPTRIG70 - EPWM31, ADCSOCA 47h REPTRIG71 - EPWM31, ADCSOCB 48h REPTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h REPTRIG81 - ECAP9, TRIGOUT 52h REPTRIG82 - ECAP10, TRIGOUT .... 57h REPTRIG73 - ECAP15, TRIGOUT 58h REPTRIG1 - RTI4 Timer 59h REPTRIG1 - RTI5 Timer 5Ah REPTRIG1 - RTI6 Timer 5Bh REPTRIG1 - RTI7 Timer .... 64h- 7Fh - Reserved
7	TRIGGEROVF	R/W1TC	0h	ADC Trigger Repeater 2 Oversampled Trigger Overflow. Indicates that a trigger was dropped because a trigger arrived while the repeater was still generating repeated oversampled triggers [NCOUNT was not 0 or SOCs associated with Repeater 2 were still pending]. Writing a 1 will clear this flag. Note: This flag won't be set in undersampling mode or when NSEL = 0; if a trigger arrives before the previous SOCs have completed, the trigger will be passed and the overflow flags of the SOCs that were still pending will be set. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
6	PHASEOVF	R/W1TC	0h	ADC Trigger Repeater 2 Phase Delay Overflow. Indicates that a trigger was dropped because a trigger arrived when the phase delay logic was still waiting to send the delayed trigger [PHASECOUNT was not 0]. Writing a 1 will clear this flag. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
5	RESERVED_2	R	0h	Reserved

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Table 3-236. ADC_CFG_REP2CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SOCBUSY	R	0h	ADC Trigger Repeater 2 Associated SOCs Busy indicator. In oversampling mode: 0 = no SOCs associated with this repeater are pending 1 = SOCs associated with this repeater are still pending The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP2CTL.BUSY = 0 [SOCs associated with trigger repeater 2 are no longer pending]. Note: If the ADC is in burstmode and the BURSTTRIG is Repeater 2, then all round-robin SOCs are considered associated with this repeater and the repeater will not re-trigger until there are no pending round-robin SOCs [in addition to any associated pending high-priority SOCs].
3	MODULEBUSY	R	0h	ADC Trigger Repeater 2 Module Busy indicator. In oversampling mode: 0 = Repeater 2 is idle and can accept a new repeated trigger in oversampling mode 1 = Repeater 2 still has repeated triggers remaining [NCOUNT ' 0] or associated SOCs are still pending [SOCBUSY is 1] If a new oversampled trigger is received while the module is still busy, the TRIGGEROVF bit will be set and the trigger will be ignored.
2	RESERVED_1	R	0h	Reserved
1	ACTIVEMODE	R	0h	When a trigger is recived in oversampling or undersampling mode the value of MODE is copied to ACTIVEMODE. ACTIVEMODE determines if the repeater will repeat of filter triggers. Changes to MODE while the repeater is working therefore won't cause any changes in functionality until the module becomes idle and then a new trigger is received. 0 = module is oversampling 1 = module is undersampling
0	MODE	R/W	0h	ADC trigger repeater 2 mode selection. Select either oversampling or undersampling mode. In oversampling mode, when the trigger selected by REP2CTL.TRIGSEL is received, the repeater will repeat the trigger REP2N.NSEL + 1 times. In undersampling mode, when the trigger selected by REP2CTL.TRIGSEL is received the first time, the repeater will pass the trigger through. The next REP2N.NSEL triggers will be ignored. 0 = oversampling 1 = undersampling

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3.2.2.117 ADC_CFG_REP2N Register

3.2.2.117.1 ADC_CFG_REP2N Register (Offset = 124h) [reset = 0h]

ADC Trigger Repeater 2 N Select Register.

Return to Summary Table

Table 3-237. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0124h
ADC1_G0_G5	502C 1124h
ADC2_G0_G5	502C 2124h
ADC3_G0_G5	502C 3124h
ADC4_G0_G5	502C 4124h

Figure 3-117. ADC_CFG_REP2N Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2	NCOUNT						
R	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	NSEL						
R	R/W						
0h	0h						

Table 3-238. ADC_CFG_REP2N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED_2	R	0h	Reserved
22:16	NCOUNT	R	0h	ADC trigger repeater 2 trigger count. In oversampling mode, indicates the number of triggers remaining to be generated. If a trigger is received corresponding to REP2CTL.TRIGSEL while NCOUNT is not 0 [the repeater is still busy generating the repeated triggers] then the trigger will be ignored and REP2CTL.TRIGOVF will be set to 1. In undersampling mode, indicates the number of triggers remaining to be supressed.
15:7	RESERVED_1	R	0h	Reserved

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Table 3-238. ADC_CFG_REP2N Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	NSEL	R/W	0h	ADC Trigger Repeater 2 selection of number of triggers. In oversampling mode, selects the number of repeated triggers. For each trigger received corresponding to REP2CTL.TRIGSEL, NSEL + 1 triggers will be generated. 0 = 1 trigger is generated [pass-through] 1 = 2 triggers are generated 2 = 3 triggers are generated ... 127 = 128 triggers are generated In undersampling mode, selects the number triggers to be supressed. 1 out NSEL + 1 triggers received corresponding to REP2CTL.TRIGSEL will be passed through [the first trigger will be passed through and the subsequent NSEL triggers will be supressed]. 0 = all triggers are passed 1 = 1 out of 2 triggers are passed 2 = 1 out of 3 triggers are passed ... 127 = 1 out of 128 triggers are passed

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3.2.2.118 ADC_CFG_REP2PHASE Register

3.2.2.118.1 ADC_CFG_REP2PHASE Register (Offset = 128h) [reset = 0h]

ADC Trigger Repeater 2 Phase Select Register.

Return to Summary Table

Table 3-239. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0128h
ADC1_G0_G5	502C 1128h
ADC2_G0_G5	502C 2128h
ADC3_G0_G5	502C 3128h
ADC4_G0_G5	502C 4128h

Figure 3-118. ADC_CFG_REP2PHASE Name Register

31	30	29	28	27	26	25	24
PHASECOUNT							
R							
0h							
23	22	21	20	19	18	17	16
PHASECOUNT							
R							
0h							
15	14	13	12	11	10	9	8
PHASE							
R/W							
0h							
7	6	5	4	3	2	1	0
PHASE							
R/W							
0h							

Table 3-240. ADC_CFG_REP2PHASE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHASECOUNT	R	0h	ADC trigger repeater 2 phase delay status. When the trigger selected by REP2CTL.TRIGSEL is received, this register will start counting down from PHASECOUNT until the counter reaches 0, at which point the trigger will be passed on to the repeater re-trigger logic. If the trigger selected by REP2CTL.TRIGSEL is recieved when PHASECOUNT is not 0 [the phase delay logic is busy from the previous trigger] then the new trigger will be ignored and REP2CTL.PHASEOVF will be set to 1.
15:0	PHASE	R/W	0h	ADC trigger repeater 2 phase delay configuration. Defines the number of SYSCLKs to delay the selected trigger before passing it on to the re-triggering logic. 0 = trigger is passed through without delay 1 = trigger is delayed by 1 SYSCLK 2 = trigger is delayed by 2 SYSCLKs ... 65535 = trigger is delayed by 65535 SYSCLKs

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3.2.2.119 ADC_CFG_REP2SPREAD Register

3.2.2.119.1 ADC_CFG_REP2SPREAD Register (Offset = 12Ch) [reset = 0h]

ADC Trigger Repeater 2 Spread Select Register.

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Table 3-241. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 012Ch
ADC1_G0_G5	502C 112Ch
ADC2_G0_G5	502C 212Ch
ADC3_G0_G5	502C 312Ch
ADC4_G0_G5	502C 412Ch

Figure 3-119. ADC_CFG_REP2SPREAD Name Register

31	30	29	28	27	26	25	24
SPREADCOUNT							
R							
0h							
23	22	21	20	19	18	17	16
SPREADCOUNT							
R							
0h							
15	14	13	12	11	10	9	8
SPREAD							
R/W							
0h							
7	6	5	4	3	2	1	0
SPREAD							
R/W							
0h							

Table 3-242. ADC_CFG_REP2SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SPREADCOUNT	R	0h	ADC trigger repeater 2 spread status. When a trigger is sent to the ADC in oversampling mode, this register will start counting down from SPREAD until SPREADCOUNT equals 0. The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP2CTL.BUSY = 0 [SOCs associated with trigger repeater 2 are no longer pending].

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Table 3-242. ADC_CFG_REP2SPREAD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	SPREAD	R/W	0h	ADC trigger repeater 2 spread delay configuration. In oversampling mode, defines the minimum number of SYSCLKs to wait before creating the next repeated trigger to the ADC. If SPREAD is less than the time needed for all SOCs associated with repeater 2 to sample and convert, then the repeater will generate triggers as fast as the ADC can convert the associated conversions. If SPREAD is greater than the time needed for all SOCs associated with repeater 2 to sample and convert, then repeated triggers to the ADC will be SPREAD SYSCLK cycles apart. 0 = oversampled repeated triggers occur as fast as the ADC can sample and convert associated SOCs 1 = time between repeated triggers is at least 1 SYSCLKs 2 = time between repeated triggers is at least 2 SYSCLKs ... 65535 = time between repeated triggers is at least 65535 SYSCLKs

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3.2.2.120 ADC_CFG_REP2FRC Register

3.2.2.120.1 ADC_CFG_REP2FRC Register (Offset = 130h) [reset = 0h]

ADC Trigger Repeater 2 Software Force Register.

Return to Summary Table

Table 3-243. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0130h
ADC1_G0_G5	502C 1130h
ADC2_G0_G5	502C 2130h
ADC3_G0_G5	502C 3130h
ADC4_G0_G5	502C 4130h

Figure 3-120. ADC_CFG_REP2FRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							SWFRC
R							R/W1TS
0h							0h

Table 3-244. ADC_CFG_REP2FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	SWFRC	R/W1TS	0h	Write 1 to force a trigger to repeat block 2 input regardless of the value of TRIGGER. Always reads 0.

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3.2.2.121 ADC_CFG_ADCPPB1LIMIT Register

3.2.2.121.1 ADC_CFG_ADCPPB1LIMIT Register (Offset = 140h) [reset = 0h]

ADC PPB1Conversion Count Limit Register.

Return to Summary Table

Table 3-245. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0140h
ADC1_G0_G5	502C 1140h
ADC2_G0_G5	502C 2140h
ADC3_G0_G5	502C 3140h
ADC4_G0_G5	502C 4140h

Figure 3-121. ADC_CFG_ADCPPB1LIMIT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						LIMIT	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMIT							
R/W							
0h							

Table 3-246. ADC_CFG_ADCPPB1LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	LIMIT	R/W	0h	Post Processing Block 1 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. To prevent PSUM from overflowing, do not write a value larger than 128 when the ADC is operating in 16-bit mode.

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3.2.2.122 ADC_CFG_ADCPPBP1PCOUNT Register

3.2.2.122.1 ADC_CFG_ADCPPBP1PCOUNT Register (Offset = 144h) [reset = 0h]

ADC PPB1 Partial Conversion Count Register.

Return to Summary Table

Table 3-247. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0144h
ADC1_G0_G5	502C 1144h
ADC2_G0_G5	502C 2144h
ADC3_G0_G5	502C 3144h
ADC4_G0_G5	502C 4144h

Figure 3-122. ADC_CFG_ADCPPBP1PCOUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PCOUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCOUNT							
R							
0h							

Table 3-248. ADC_CFG_ADCPPBP1PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PCOUNT	R	0h	Post Processing Block 1 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB1PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.123 ADC_CFG_ADCPPB1CONFIG2 Register

3.2.2.123.1 ADC_CFG_ADCPPB1CONFIG2 Register (Offset = 148h) [reset = 0h]

ADC PPB1 Sum Shift Register.

Return to Summary Table

Table 3-249. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0148h
ADC1_G0_G5	502C 1148h
ADC2_G0_G5	502C 2148h
ADC3_G0_G5	502C 3148h
ADC4_G0_G5	502C 4148h

Figure 3-123. ADC_CFG_ADCPPB1CONFIG2 Name Register

15	14	13	12	11	10	9	8
COMPSEL		RESERVED_2	OSINTSEL	SWSYNC	RESERVED_1	SYNCINSEL	
R/W		R	R/W	R/W1TS	R	R/W	
0h		0h	0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYNCINSEL				SHIFT			
R/W				R/W			
0h				0h			

Table 3-250. ADC_CFG_ADCPPB1CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	COMPSEL	R/W	0h	Post Processing Block 1 Compare Source Select. This field determines whether ADCPPB1RESULT, ADCPPB1PSUM, or ADCPPB1SUM is used for the zero-crossing detect logic and threshold compare. 00 = ADCPPB1RESULT is used for compare logic 01 = ADCPPB1PSUM is used for compare logic 10 = ADCPPB1SUM is used for compare logic 11 = Reserved Note: when ADCPPB1PSUM is selected as the compare source and when a LIMIT match occurs [ADCPPB1LIMIT equals ADCPPB1COUNT] the ADCPPB1PSUM register will be cleared and the final sum will be loaded into ADCPPB1SUM. For this sample, the final sum, ADCPPB1SUM will be used for the compariosn instead of ADCPPB1PSUM.
13	RESERVED_2	R	0h	Reserved
12	OSINTSEL	R/W	0h	Post Processing Block 1 Interrupt Source Select. OSINT1 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT1 in addition to a PCOUNT = LIMIT event. 0 = OSINT1 will be generated from PCOUNT = LIMIT only 1 = OSTIN1 will be generated form PCOUNT = LIMIT or a sync. event. Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.
11	SWSYNC	R/W1TS	0h	PPB 1 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur.

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Table 3-250. ADC_CFG_ADCPPB1CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RESERVED_1	R	0h	Reserved
9:4	SYNCINSEL	R/W	0h	PPB 1 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details
3:0	SHIFT	R/W	0h	Post Processing Block 1 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM " 1 2 : SUM = PSUM " 2 ... 10 : SUM = PSUM " 10 11 - 15 : Reserved

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3.2.2.124 ADC_CFG_ADCPPB1PSUM Register

3.2.2.124.1 ADC_CFG_ADCPPB1PSUM Register (Offset = 14Ch) [reset = 0h]

ADC PPB1 Partial Sum Register.

Return to Summary Table

Table 3-251. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 014Ch
ADC1_G0_G5	502C 114Ch
ADC2_G0_G5	502C 214Ch
ADC3_G0_G5	502C 314Ch
ADC4_G0_G5	502C 414Ch

Figure 3-124. ADC_CFG_ADCPPB1PSUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
PSUM							
R							
0h							
15	14	13	12	11	10	9	8
PSUM							
R							
0h							
7	6	5	4	3	2	1	0
PSUM							
R							
0h							

Table 3-252. ADC_CFG_ADCPPB1PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	PSUM	R	0h	Post Processing Block 1 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information].

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3.2.2.125 ADC_CFG_ADCPPB1PMAX Register

3.2.2.125.1 ADC_CFG_ADCPPB1PMAX Register (Offset = 150h) [reset = 0h]

ADC PPB1 Partial Max Register.

Return to Summary Table

Table 3-253. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0150h
ADC1_G0_G5	502C 1150h
ADC2_G0_G5	502C 2150h
ADC3_G0_G5	502C 3150h
ADC4_G0_G5	502C 4150h

Figure 3-125. ADC_CFG_ADCPPB1PMAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							PMAX
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMAX							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMAX							
R							
0h							

Table 3-254. ADC_CFG_ADCPPB1PMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMAX	R	0h	Post Processing Block 1 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.126 ADC_CFG_ADCPPB1PMAXI Register

3.2.2.126.1 ADC_CFG_ADCPPB1PMAXI Register (Offset = 154h) [reset = 0h]

ADC PPB1 Partial Max Index Register.

Return to Summary Table

Table 3-255. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0154h
ADC1_G0_G5	502C 1154h
ADC2_G0_G5	502C 2154h
ADC3_G0_G5	502C 3154h
ADC4_G0_G5	502C 4154h

Figure 3-126. ADC_CFG_ADCPPB1PMAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMAXI							
R							
0h							

Table 3-256. ADC_CFG_ADCPPB1PMAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMAXI	R	0h	Post Processing Block 1 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.127 ADC_CFG_ADCPPB1PMIN Register

3.2.2.127.1 ADC_CFG_ADCPPB1PMIN Register (Offset = 158h) [reset = 0h]

ADC PPB1 Partial MIN Register.

Return to Summary Table

Table 3-257. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0158h
ADC1_G0_G5	502C 1158h
ADC2_G0_G5	502C 2158h
ADC3_G0_G5	502C 3158h
ADC4_G0_G5	502C 4158h

Figure 3-127. ADC_CFG_ADCPPB1PMIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							PMIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMIN							
R							
0h							

Table 3-258. ADC_CFG_ADCPPB1PMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMIN	R	0h	Post Processing Block 1 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.128 ADC_CFG_ADCPPB1PMINI Register

3.2.2.128.1 ADC_CFG_ADCPPB1PMINI Register (Offset = 15Ch) [reset = 0h]

ADC PPB1 Partial Min Index Register.

Return to Summary Table

Table 3-259. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 015Ch
ADC1_G0_G5	502C 115Ch
ADC2_G0_G5	502C 215Ch
ADC3_G0_G5	502C 315Ch
ADC4_G0_G5	502C 415Ch

Figure 3-128. ADC_CFG_ADCPPB1PMINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMINI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMINI							
R							
0h							

Table 3-260. ADC_CFG_ADCPPB1PMINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMINI	R	0h	Post Processing Block 1 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.2.2.129 ADC_CFG_ADCPPB1TRIPLO2 Register

3.2.2.129.1 ADC_CFG_ADCPPB1TRIPLO2 Register (Offset = 160h) [reset = 0h]

ADC PPB1 Extended Trip Low Register.

Return to Summary Table

Table 3-261. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0160h
ADC1_G0_G5	502C 1160h
ADC2_G0_G5	502C 2160h
ADC3_G0_G5	502C 3160h
ADC4_G0_G5	502C 4160h

Figure 3-129. ADC_CFG_ADCPPB1TRIPLO2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITLO							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITLO							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITLO							
R/W							
0h							

Table 3-262. ADC_CFG_ADCPPB1TRIPLO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITLO	R/W	0h	ADC Post Processing Block 1 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB1TRIPLO.LIMITLO2EN = 1. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPLO2[23:17] will be ignored in 16 bit mode - TRIPLO2[23:13] will be ignored in 12 bit mode

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3.2.2.130 ADC_CFG_ADCPPB2LIMIT Register

3.2.2.130.1 ADC_CFG_ADCPPB2LIMIT Register (Offset = 174h) [reset = 0h]

ADC PPB2Conversion Count Limit Register.

Return to Summary Table

Table 3-263. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0174h
ADC1_G0_G5	502C 1174h
ADC2_G0_G5	502C 2174h
ADC3_G0_G5	502C 3174h
ADC4_G0_G5	502C 4174h

Figure 3-130. ADC_CFG_ADCPPB2LIMIT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						LIMIT	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMIT							
R/W							
0h							

Table 3-264. ADC_CFG_ADCPPB2LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	LIMIT	R/W	0h	Post Processing Block 2 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. To prevent PSUM from overflowing, do not write a value larger than 128 when the ADC is operating in 16-bit mode.

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3.2.2.131 ADC_CFG_ADCPPBP2PCOUNT Register

3.2.2.131.1 ADC_CFG_ADCPPBP2PCOUNT Register (Offset = 178h) [reset = 0h]

ADC PPB2 Partial Conversion Count Register.

Return to Summary Table

Table 3-265. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0178h
ADC1_G0_G5	502C 1178h
ADC2_G0_G5	502C 2178h
ADC3_G0_G5	502C 3178h
ADC4_G0_G5	502C 4178h

Figure 3-131. ADC_CFG_ADCPPBP2PCOUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PCOUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCOUNT							
R							
0h							

Table 3-266. ADC_CFG_ADCPPBP2PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PCOUNT	R	0h	Post Processing Block 2 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB2PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.132 ADC_CFG_ADCPPB2CONFIG2 Register

3.2.2.132.1 ADC_CFG_ADCPPB2CONFIG2 Register (Offset = 17Ch) [reset = 0h]

ADC PPB2 Sum Shift Register.

Return to Summary Table

Table 3-267. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 017Ch
ADC1_G0_G5	502C 117Ch
ADC2_G0_G5	502C 217Ch
ADC3_G0_G5	502C 317Ch
ADC4_G0_G5	502C 417Ch

Figure 3-132. ADC_CFG_ADCPPB2CONFIG2 Name Register

15	14	13	12	11	10	9	8
COMPSEL		RESERVED_2	OSINTSEL	SWSYNC	RESERVED_1	SYNCINSEL	
R/W		R	R/W	R/W1TS	R	R/W	
0h		0h	0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYNCINSEL				SHIFT			
R/W				R/W			
0h				0h			

Table 3-268. ADC_CFG_ADCPPB2CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	COMPSEL	R/W	0h	Post Processing Block 2 Compare Source Select. This field determines whether ADCPPB2RESULT, ADCPPB2PSUM, or ADCPPB2SUM is used for the zero-crossing detect logic and threshold compare. 00 = ADCPPB2RESULT is used for compare logic 01 = ADCPPB2PSUM is used for compare logic 10 = ADCPPB2SUM is used for compare logic 11 = Reserved Note: when ADCPPB2PSUM is selected as the compare source and when a LIMIT match occurs [ADCPPB2LIMIT equals ADCPPB2COUNT] the ADCPPB2PSUM register will be cleared and the final sum will be loaded into ADCPPB2SUM. For this sample, the final sum, ADCPPB2SUM will be used for the compariosn instead of ADCPPB2PSUM.
13	RESERVED_2	R	0h	Reserved
12	OSINTSEL	R/W	0h	Post Processing Block 2 Interrupt Source Select. OSINT2 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT2 in addition to a PCOUNT = LIMIT event. 0 = OSINT2 will be generated from PCOUNT = LIMIT only 1 = OSTIN2 will be generated form PCOUNT = LIMIT or a sync. event. Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.
11	SWSYNC	R/W1TS	0h	PPB 2 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur.

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Table 3-268. ADC_CFG_ADCPPB2CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RESERVED_1	R	0h	Reserved
9:4	SYNCINSEL	R/W	0h	PPB 2 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details
3:0	SHIFT	R/W	0h	Post Processing Block 2 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM " 1 2 : SUM = PSUM " 2 ... 10 : SUM = PSUM " 10 11 - 15 : Reserved

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3.2.2.133 ADC_CFG_ADCPPB2PSUM Register

3.2.2.133.1 ADC_CFG_ADCPPB2PSUM Register (Offset = 180h) [reset = 0h]

ADC PPB2 Partial Sum Register.

Return to Summary Table

Table 3-269. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0180h
ADC1_G0_G5	502C 1180h
ADC2_G0_G5	502C 2180h
ADC3_G0_G5	502C 3180h
ADC4_G0_G5	502C 4180h

Figure 3-133. ADC_CFG_ADCPPB2PSUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
PSUM							
R							
0h							
15	14	13	12	11	10	9	8
PSUM							
R							
0h							
7	6	5	4	3	2	1	0
PSUM							
R							
0h							

Table 3-270. ADC_CFG_ADCPPB2PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	PSUM	R	0h	Post Processing Block 2 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information].

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3.2.2.134 ADC_CFG_ADCPPB2PMAX Register

3.2.2.134.1 ADC_CFG_ADCPPB2PMAX Register (Offset = 184h) [reset = 0h]

ADC PPB2 Partial Max Register.

Return to Summary Table

Table 3-271. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0184h
ADC1_G0_G5	502C 1184h
ADC2_G0_G5	502C 2184h
ADC3_G0_G5	502C 3184h
ADC4_G0_G5	502C 4184h

Figure 3-134. ADC_CFG_ADCPPB2PMAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							PMAX
R							R
0h							0h
15	14	13	12	11	10	9	8
PMAX							
R							
0h							
7	6	5	4	3	2	1	0
PMAX							
R							
0h							

Table 3-272. ADC_CFG_ADCPPB2PMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMAX	R	0h	Post Processing Block 2 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.135 ADC_CFG_ADCPPB2PMAXI Register

3.2.2.135.1 ADC_CFG_ADCPPB2PMAXI Register (Offset = 188h) [reset = 0h]

ADC PPB2 Partial Max Index Register.

Return to Summary Table

Table 3-273. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0188h
ADC1_G0_G5	502C 1188h
ADC2_G0_G5	502C 2188h
ADC3_G0_G5	502C 3188h
ADC4_G0_G5	502C 4188h

Figure 3-135. ADC_CFG_ADCPPB2PMAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMAXI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
PMAXI							
R							
0h							

Table 3-274. ADC_CFG_ADCPPB2PMAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMAXI	R	0h	Post Processing Block 2 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.136 ADC_CFG_ADCPPB2PMIN Register

3.2.2.136.1 ADC_CFG_ADCPPB2PMIN Register (Offset = 18Ch) [reset = 0h]

ADC PPB2 Partial MIN Register.

Return to Summary Table

Table 3-275. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 018Ch
ADC1_G0_G5	502C 118Ch
ADC2_G0_G5	502C 218Ch
ADC3_G0_G5	502C 318Ch
ADC4_G0_G5	502C 418Ch

Figure 3-136. ADC_CFG_ADCPPB2PMIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							PMIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMIN							
R							
0h							

Table 3-276. ADC_CFG_ADCPPB2PMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMIN	R	0h	Post Processing Block 2 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.137 ADC_CFG_ADCPPB2PMINI Register

3.2.2.137.1 ADC_CFG_ADCPPB2PMINI Register (Offset = 190h) [reset = 0h]

ADC PPB2 Partial Min Index Register.

Return to Summary Table

Table 3-277. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0190h
ADC1_G0_G5	502C 1190h
ADC2_G0_G5	502C 2190h
ADC3_G0_G5	502C 3190h
ADC4_G0_G5	502C 4190h

Figure 3-137. ADC_CFG_ADCPPB2PMINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMINI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMINI							
R							
0h							

Table 3-278. ADC_CFG_ADCPPB2PMINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMINI	R	0h	Post Processing Block 2 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.2.2.138 ADC_CFG_ADCPPB2TRIPLO2 Register

3.2.2.138.1 ADC_CFG_ADCPPB2TRIPLO2 Register (Offset = 194h) [reset = 0h]

ADC PPB2 Extended Trip Low Register.

Return to Summary Table

Table 3-279. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 0194h
ADC1_G0_G5	502C 1194h
ADC2_G0_G5	502C 2194h
ADC3_G0_G5	502C 3194h
ADC4_G0_G5	502C 4194h

Figure 3-138. ADC_CFG_ADCPPB2TRIPLO2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITLO							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITLO							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITLO							
R/W							
0h							

Table 3-280. ADC_CFG_ADCPPB2TRIPLO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITLO	R/W	0h	ADC Post Processing Block 2 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB2TRIPLO.LIMITLO2EN = 1. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPLO2[23:17] will be ignored in 16 bit mode - TRIPLO2[23:13] will be ignored in 12 bit mode

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3.2.2.139 ADC_CFG_ADCPPB3LIMIT Register

3.2.2.139.1 ADC_CFG_ADCPPB3LIMIT Register (Offset = 1A8h) [reset = 0h]

ADC PPB3Conversion Count Limit Register.

Return to Summary Table

Table 3-281. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01A8h
ADC1_G0_G5	502C 11A8h
ADC2_G0_G5	502C 21A8h
ADC3_G0_G5	502C 31A8h
ADC4_G0_G5	502C 41A8h

Figure 3-139. ADC_CFG_ADCPPB3LIMIT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						LIMIT	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMIT							
R/W							
0h							

Table 3-282. ADC_CFG_ADCPPB3LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	LIMIT	R/W	0h	Post Processing Block 3 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. To prevent PSUM from overflowing, do not write a value larger than 128 when the ADC is operating in 16-bit mode.

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3.2.2.140 ADC_CFG_ADCPPBP3PCOUNT Register

3.2.2.140.1 ADC_CFG_ADCPPBP3PCOUNT Register (Offset = 1ACh) [reset = 0h]

ADC PPB3 Partial Conversion Count Register.

Return to Summary Table

Table 3-283. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01ACh
ADC1_G0_G5	502C 11ACh
ADC2_G0_G5	502C 21ACh
ADC3_G0_G5	502C 31ACh
ADC4_G0_G5	502C 41ACh

Figure 3-140. ADC_CFG_ADCPPBP3PCOUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PCOUNT	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
PCOUNT							
R							
0h							

Table 3-284. ADC_CFG_ADCPPBP3PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PCOUNT	R	0h	Post Processing Block 3 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB3PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.141 ADC_CFG_ADCPPB3CONFIG2 Register

3.2.2.141.1 ADC_CFG_ADCPPB3CONFIG2 Register (Offset = 1B0h) [reset = 0h]

ADC PPB3 Sum Shift Register.

Return to Summary Table

Table 3-285. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01B0h
ADC1_G0_G5	502C 11B0h
ADC2_G0_G5	502C 21B0h
ADC3_G0_G5	502C 31B0h
ADC4_G0_G5	502C 41B0h

Figure 3-141. ADC_CFG_ADCPPB3CONFIG2 Name Register

15	14	13	12	11	10	9	8
COMPSEL		RESERVED_2	OSINTSEL	SWSYNC	RESERVED_1	SYNCINSEL	
R/W		R	R/W	R/W1TS	R	R/W	
0h		0h	0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYNCINSEL				SHIFT			
R/W				R/W			
0h				0h			

Table 3-286. ADC_CFG_ADCPPB3CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	COMPSEL	R/W	0h	Post Processing Block 3 Compare Source Select. This field determines whether ADCPPB3RESULT, ADCPPB3PSUM, or ADCPPB3SUM is used for the zero-crossing detect logic and threshold compare. 00 = ADCPPB3RESULT is used for compare logic 01 = ADCPPB3PSUM is used for compare logic 10 = ADCPPB3SUM is used for compare logic 11 = Reserved Note: when ADCPPB3PSUM is selected as the compare source and when a LIMIT match occurs [ADCPPB3LIMIT equals ADCPPB3COUNT] the ADCPPB3PSUM register will be cleared and the final sum will be loaded into ADCPPB3SUM. For this sample, the final sum, ADCPPB3SUM will be used for the compariosn instead of ADCPPB3PSUM.
13	RESERVED_2	R	0h	Reserved
12	OSINTSEL	R/W	0h	Post Processing Block 3 Interrupt Source Select. OSINT3 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT3 in addition to a PCOUNT = LIMIT event. 0 = OSINT3 will be generated from PCOUNT = LIMIT only 1 = OSTIN3 will be generated form PCOUNT = LIMIT or a sync. event. Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.
11	SWSYNC	R/W1TS	0h	PPB 3 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur.

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Table 3-286. ADC_CFG_ADCPPB3CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RESERVED_1	R	0h	Reserved
9:4	SYNCINSEL	R/W	0h	PPB 3 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details
3:0	SHIFT	R/W	0h	Post Processing Block 3 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM " 1 2 : SUM = PSUM " 2 ... 10 : SUM = PSUM " 10 11 - 15 : Reserved

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3.2.2.142 ADC_CFG_ADCPPB3PSUM Register

3.2.2.142.1 ADC_CFG_ADCPPB3PSUM Register (Offset = 1B4h) [reset = 0h]

ADC PPB3 Partial Sum Register.

Return to Summary Table

Table 3-287. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01B4h
ADC1_G0_G5	502C 11B4h
ADC2_G0_G5	502C 21B4h
ADC3_G0_G5	502C 31B4h
ADC4_G0_G5	502C 41B4h

Figure 3-142. ADC_CFG_ADCPPB3PSUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
PSUM							
R							
0h							
15	14	13	12	11	10	9	8
PSUM							
R							
0h							
7	6	5	4	3	2	1	0
PSUM							
R							
0h							

Table 3-288. ADC_CFG_ADCPPB3PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	PSUM	R	0h	Post Processing Block 3 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information].

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3.2.2.143 ADC_CFG_ADCPPB3PMAX Register

3.2.2.143.1 ADC_CFG_ADCPPB3PMAX Register (Offset = 1B8h) [reset = 0h]

ADC PPB3 Partial Max Register.

Return to Summary Table

Table 3-289. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01B8h
ADC1_G0_G5	502C 11B8h
ADC2_G0_G5	502C 21B8h
ADC3_G0_G5	502C 31B8h
ADC4_G0_G5	502C 41B8h

Figure 3-143. ADC_CFG_ADCPPB3PMAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							PMAX
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMAX							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMAX							
R							
0h							

Table 3-290. ADC_CFG_ADCPPB3PMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMAX	R	0h	Post Processing Block 3 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.144 ADC_CFG_ADCPPB3PMAXI Register

3.2.2.144.1 ADC_CFG_ADCPPB3PMAXI Register (Offset = 1BCh) [reset = 0h]

ADC PPB3 Partial Max Index Register.

Return to Summary Table

Table 3-291. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01BCh
ADC1_G0_G5	502C 11BCh
ADC2_G0_G5	502C 21BCh
ADC3_G0_G5	502C 31BCh
ADC4_G0_G5	502C 41BCh

Figure 3-144. ADC_CFG_ADCPPB3PMAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMAXI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
PMAXI							
R							
0h							

Table 3-292. ADC_CFG_ADCPPB3PMAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMAXI	R	0h	Post Processing Block 3 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.145 ADC_CFG_ADCPPB3PMIN Register

3.2.2.145.1 ADC_CFG_ADCPPB3PMIN Register (Offset = 1C0h) [reset = 0h]

ADC PPB3 Partial MIN Register.

Return to Summary Table

Table 3-293. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01C0h
ADC1_G0_G5	502C 11C0h
ADC2_G0_G5	502C 21C0h
ADC3_G0_G5	502C 31C0h
ADC4_G0_G5	502C 41C0h

Figure 3-145. ADC_CFG_ADCPPB3PMIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							PMIN
R							R
0h							0h
15	14	13	12	11	10	9	8
PMIN							
R							
0h							
7	6	5	4	3	2	1	0
PMIN							
R							
0h							

Table 3-294. ADC_CFG_ADCPPB3PMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMIN	R	0h	Post Processing Block 3 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.146 ADC_CFG_ADCPPB3PMINI Register

3.2.2.146.1 ADC_CFG_ADCPPB3PMINI Register (Offset = 1C4h) [reset = 0h]

ADC PPB3 Partial Min Index Register.

Return to Summary Table

Table 3-295. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01C4h
ADC1_G0_G5	502C 11C4h
ADC2_G0_G5	502C 21C4h
ADC3_G0_G5	502C 31C4h
ADC4_G0_G5	502C 41C4h

Figure 3-146. ADC_CFG_ADCPPB3PMINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMINI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMINI							
R							
0h							

Table 3-296. ADC_CFG_ADCPPB3PMINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMINI	R	0h	Post Processing Block 3 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.2.2.147 ADC_CFG_ADCPPB3TRIPLO2 Register

3.2.2.147.1 ADC_CFG_ADCPPB3TRIPLO2 Register (Offset = 1C8h) [reset = 0h]

ADC PPB3 Extended Trip Low Register.

Return to Summary Table

Table 3-297. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01C8h
ADC1_G0_G5	502C 11C8h
ADC2_G0_G5	502C 21C8h
ADC3_G0_G5	502C 31C8h
ADC4_G0_G5	502C 41C8h

Figure 3-147. ADC_CFG_ADCPPB3TRIPLO2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITLO							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITLO							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITLO							
R/W							
0h							

Table 3-298. ADC_CFG_ADCPPB3TRIPLO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITLO	R/W	0h	ADC Post Processing Block 3 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB3TRIPLO.LIMITLO2EN = 1. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPLO2[23:17] will be ignored in 16 bit mode - TRIPLO2[23:13] will be ignored in 12 bit mode

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3.2.2.148 ADC_CFG_ADCPPB4LIMIT Register

3.2.2.148.1 ADC_CFG_ADCPPB4LIMIT Register (Offset = 1DCh) [reset = 0h]

ADC PPB4Conversion Count Limit Register.

Return to Summary Table

Table 3-299. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01DCh
ADC1_G0_G5	502C 11DCh
ADC2_G0_G5	502C 21DCh
ADC3_G0_G5	502C 31DCh
ADC4_G0_G5	502C 41DCh

Figure 3-148. ADC_CFG_ADCPPB4LIMIT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						LIMIT	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
LIMIT							
R/W							
0h							

Table 3-300. ADC_CFG_ADCPPB4LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	LIMIT	R/W	0h	Post Processing Block 4 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. To prevent PSUM from overflowing, do not write a value larger than 128 when the ADC is operating in 16-bit mode.

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3.2.2.149 ADC_CFG_ADCPPBP4PCOUNT Register

3.2.2.149.1 ADC_CFG_ADCPPBP4PCOUNT Register (Offset = 1E0h) [reset = 0h]

ADC PPB4 Partial Conversion Count Register.

Return to Summary Table

Table 3-301. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01E0h
ADC1_G0_G5	502C 11E0h
ADC2_G0_G5	502C 21E0h
ADC3_G0_G5	502C 31E0h
ADC4_G0_G5	502C 41E0h

Figure 3-149. ADC_CFG_ADCPPBP4PCOUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PCOUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCOUNT							
R							
0h							

Table 3-302. ADC_CFG_ADCPPBP4PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PCOUNT	R	0h	Post Processing Block 4 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB4PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.150 ADC_CFG_ADCPPB4CONFIG2 Register

3.2.2.150.1 ADC_CFG_ADCPPB4CONFIG2 Register (Offset = 1E4h) [reset = 0h]

ADC PPB4 Sum Shift Register.

Return to Summary Table

Table 3-303. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01E4h
ADC1_G0_G5	502C 11E4h
ADC2_G0_G5	502C 21E4h
ADC3_G0_G5	502C 31E4h
ADC4_G0_G5	502C 41E4h

Figure 3-150. ADC_CFG_ADCPPB4CONFIG2 Name Register

15	14	13	12	11	10	9	8
COMPSEL		RESERVED_2	OSINTSEL	SWSYNC	RESERVED_1	SYNCINSEL	
R/W		R	R/W	R/W1TS	R	R/W	
0h		0h	0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYNCINSEL				SHIFT			
R/W				R/W			
0h				0h			

Table 3-304. ADC_CFG_ADCPPB4CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	COMPSEL	R/W	0h	Post Processing Block 4 Compare Source Select. This field determines whether ADCPPB4RESULT, ADCPPB4PSUM, or ADCPPB4SUM is used for the zero-crossing detect logic and threshold compare. 00 = ADCPPB4RESULT is used for compare logic 01 = ADCPPB4PSUM is used for compare logic 10 = ADCPPB4SUM is used for compare logic 11 = Reserved Note: when ADCPPB4PSUM is selected as the compare source and when a LIMIT match occurs [ADCPPB4LIMIT equals ADCPPB4COUNT] the ADCPPB4PSUM register will be cleared and the final sum will be loaded into ADCPPB4SUM. For this sample, the final sum, ADCPPB4SUM will be used for the compariosn instead of ADCPPB4PSUM.
13	RESERVED_2	R	0h	Reserved
12	OSINTSEL	R/W	0h	Post Processing Block 4 Interrupt Source Select. OSINT4 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT4 in addition to a PCOUNT = LIMIT event. 0 = OSINT4 will be generated from PCOUNT = LIMIT only 1 = OSTIN4 will be generated form PCOUNT = LIMIT or a sync. event. Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.
11	SWSYNC	R/W1TS	0h	PPB 4 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur.

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Table 3-304. ADC_CFG_ADCPPB4CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RESERVED_1	R	0h	Reserved
9:4	SYNCINSEL	R/W	0h	PPB 4 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details
3:0	SHIFT	R/W	0h	Post Processing Block 4 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM " 1 2 : SUM = PSUM " 2 ... 10 : SUM = PSUM " 10 11 - 15 : Reserved

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3.2.2.151 ADC_CFG_ADCPPB4PSUM Register

3.2.2.151.1 ADC_CFG_ADCPPB4PSUM Register (Offset = 1E8h) [reset = 0h]

ADC PPB4 Partial Sum Register.

Return to Summary Table

Table 3-305. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01E8h
ADC1_G0_G5	502C 11E8h
ADC2_G0_G5	502C 21E8h
ADC3_G0_G5	502C 31E8h
ADC4_G0_G5	502C 41E8h

Figure 3-151. ADC_CFG_ADCPPB4PSUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
PSUM							
R							
0h							
15	14	13	12	11	10	9	8
PSUM							
R							
0h							
7	6	5	4	3	2	1	0
PSUM							
R							
0h							

Table 3-306. ADC_CFG_ADCPPB4PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	PSUM	R	0h	Post Processing Block 4 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information].

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3.2.2.152 ADC_CFG_ADCPPB4PMAX Register

3.2.2.152.1 ADC_CFG_ADCPPB4PMAX Register (Offset = 1ECh) [reset = 0h]

ADC PPB4 Partial Max Register.

Return to Summary Table

Table 3-307. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01ECh
ADC1_G0_G5	502C 11ECh
ADC2_G0_G5	502C 21ECh
ADC3_G0_G5	502C 31ECh
ADC4_G0_G5	502C 41ECh

Figure 3-152. ADC_CFG_ADCPPB4PMAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							PMAX
R							R
0h							0h
15	14	13	12	11	10	9	8
PMAX							
R							
0h							
7	6	5	4	3	2	1	0
PMAX							
R							
0h							

Table 3-308. ADC_CFG_ADCPPB4PMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMAX	R	0h	Post Processing Block 4 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.153 ADC_CFG_ADCPPB4PMAXI Register

3.2.2.153.1 ADC_CFG_ADCPPB4PMAXI Register (Offset = 1F0h) [reset = 0h]

ADC PPB4 Partial Max Index Register.

Return to Summary Table

Table 3-309. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01F0h
ADC1_G0_G5	502C 11F0h
ADC2_G0_G5	502C 21F0h
ADC3_G0_G5	502C 31F0h
ADC4_G0_G5	502C 41F0h

Figure 3-153. ADC_CFG_ADCPPB4PMAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMAXI							
R							
0h							

Table 3-310. ADC_CFG_ADCPPB4PMAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMAXI	R	0h	Post Processing Block 4 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.154 ADC_CFG_ADCPPB4PMIN Register

3.2.2.154.1 ADC_CFG_ADCPPB4PMIN Register (Offset = 1F4h) [reset = 0h]

ADC PPB4 Partial MIN Register.

Return to Summary Table

Table 3-311. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01F4h
ADC1_G0_G5	502C 11F4h
ADC2_G0_G5	502C 21F4h
ADC3_G0_G5	502C 31F4h
ADC4_G0_G5	502C 41F4h

Figure 3-154. ADC_CFG_ADCPPB4PMIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							PMIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMIN							
R							
0h							

Table 3-312. ADC_CFG_ADCPPB4PMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMIN	R	0h	Post Processing Block 4 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.155 ADC_CFG_ADCPPB4PMINI Register

3.2.2.155.1 ADC_CFG_ADCPPB4PMINI Register (Offset = 1F8h) [reset = 0h]

ADC PPB4 Partial Min Index Register.

Return to Summary Table

Table 3-313. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01F8h
ADC1_G0_G5	502C 11F8h
ADC2_G0_G5	502C 21F8h
ADC3_G0_G5	502C 31F8h
ADC4_G0_G5	502C 41F8h

Figure 3-155. ADC_CFG_ADCPPB4PMINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMINI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
PMINI							
R							
0h							

Table 3-314. ADC_CFG_ADCPPB4PMINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMINI	R	0h	Post Processing Block 4 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.2.2.156 ADC_CFG_ADCPPB4TRIPLO2 Register

3.2.2.156.1 ADC_CFG_ADCPPB4TRIPLO2 Register (Offset = 1FCh) [reset = 0h]

ADC PPB4 Extended Trip Low Register.

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Table 3-315. Instance Table

Instance Name	Physical Address
ADC0_G0_G5	502C 01FCh
ADC1_G0_G5	502C 11FCh
ADC2_G0_G5	502C 21FCh
ADC3_G0_G5	502C 31FCh
ADC4_G0_G5	502C 41FCh

Figure 3-156. ADC_CFG_ADCPPB4TRIPLO2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITLO							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITLO							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITLO							
R/W							
0h							

Table 3-316. ADC_CFG_ADCPPB4TRIPLO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITLO	R/W	0h	ADC Post Processing Block 4 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB4TRIPLO.LIMITLO2EN = 1. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPLO2[23:17] will be ignored in 16 bit mode - TRIPLO2[23:13] will be ignored in 12 bit mode

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3.3 ADC_SAFETY

ADC_SAFETY

3.3.1 ADC_SAFETY Summaries

ADC_SAFETY Summaries

Table 3-317. ADC_SAFETY Registers, Base Address=502C B400h, Length=256

Offset	Length	Register Name	ADCSAFE_00 Physical Address	ADCSAFE_01 Physical Address	ADCSAFE_02 Physical Address
0h	16	ADC_SAFETY_CHECKCONFIG	502C B400h	502C B800h	502C BC00h
4h	16	ADC_SAFETY_CHECKSTATUS	502C B404h	502C B804h	502C BC04h
8h	16	ADC_SAFETY_ADCRESSEL1	502C B408h	502C B808h	502C BC08h
Ch	16	ADC_SAFETY_ADCRESSEL2	502C B40Ch	502C B80Ch	502C BC0Ch
10h	32	ADC_SAFETY_TOLERANCE	502C B410h	502C B810h	502C BC10h
18h	32	ADC_SAFETY_CHECKRESULT1	502C B418h	502C B818h	502C BC18h
1Ch	32	ADC_SAFETY_CHECKRESULT2	502C B41Ch	502C B81Ch	502C BC1Ch

Table 3-318. ADC_SAFETY Registers, Base Address=502C B400h, Length=256

Offset	Length	Register Name	ADCSAFE_03 Physical Address	ADCSAFE_04 Physical Address	ADCSAFE_05 Physical Address
0h	16	ADC_SAFETY_CHECKCONFIG	502C C000h	502C C400h	502C C800h
4h	16	ADC_SAFETY_CHECKSTATUS	502C C004h	502C C404h	502C C804h
8h	16	ADC_SAFETY_ADCRESSEL1	502C C008h	502C C408h	502C C808h
Ch	16	ADC_SAFETY_ADCRESSEL2	502C C00Ch	502C C40Ch	502C C80Ch
10h	32	ADC_SAFETY_TOLERANCE	502C C010h	502C C410h	502C C810h
18h	32	ADC_SAFETY_CHECKRESULT1	502C C018h	502C C418h	502C C818h
1Ch	32	ADC_SAFETY_CHECKRESULT2	502C C01Ch	502C C41Ch	502C C81Ch

Table 3-319. ADC_SAFETY Registers, Base Address=502C B400h, Length=256

Offset	Length	Register Name	ADCSAFE_06 Physical Address	ADCSAFE_07 Physical Address	ADCSAFE_08 Physical Address
0h	16	ADC_SAFETY_CHECKCONFIG	502C CC00h	502C D000h	502C D400h
4h	16	ADC_SAFETY_CHECKSTATUS	502C CC04h	502C D004h	502C D404h
8h	16	ADC_SAFETY_ADCRESSEL1	502C CC08h	502C D008h	502C D408h
Ch	16	ADC_SAFETY_ADCRESSEL2	502C CC0Ch	502C D00Ch	502C D40Ch
10h	32	ADC_SAFETY_TOLERANCE	502C CC10h	502C D010h	502C D410h
18h	32	ADC_SAFETY_CHECKRESULT1	502C CC18h	502C D018h	502C D418h
1Ch	32	ADC_SAFETY_CHECKRESULT2	502C CC1Ch	502C D01Ch	502C D41Ch

Table 3-320. ADC_SAFETY Registers, Base Address=502C B400h, Length=256

Offset	Length	Register Name	ADCSAFE_09 Physical Address	ADCSAFE_10 Physical Address	ADCSAFE_11 Physical Address
0h	16	ADC_SAFETY_CHECKCONFIG	502C D800h	502C DC00h	502C E000h
4h	16	ADC_SAFETY_CHECKSTATUS	502C D804h	502C DC04h	502C E004h
8h	16	ADC_SAFETY_ADCRESSEL1	502C D808h	502C DC08h	502C E008h
Ch	16	ADC_SAFETY_ADCRESSEL2	502C D80Ch	502C DC0Ch	502C E00Ch
10h	32	ADC_SAFETY_TOLERANCE	502C D810h	502C DC10h	502C E010h
18h	32	ADC_SAFETY_CHECKRESULT1	502C D818h	502C DC18h	502C E018h

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Table 3-320. ADC_SAFETY Registers, Base Address=502C B400h, Length=256 (continued)

Offset	Length	Register Name	ADCSAFE_09 Physical Address	ADCSAFE_10 Physical Address	ADCSAFE_11 Physical Address
1Ch	32	ADC_SAFETY_CHECKRESULT2	502C D81Ch	502C DC1Ch	502C E01Ch

Table 3-321. ADC_SAFETY_AGGR Registers, Base Address=502C EC00h, Length=256

Offset	Length	Register Name	ADCSAFE_00 Physical Address
0h	32	ADC_SAFETY_AGGR_OOTFLG	502C EC00h
4h	32	ADC_SAFETY_AGGR_OOTFLGCLR	502C EC04h
8h	32	ADC_SAFETY_AGGR_RES1OVF	502C EC08h
Ch	32	ADC_SAFETY_AGGR_RES1OVFCLR	502C EC0Ch
10h	32	ADC_SAFETY_AGGR_RES2OVF	502C EC10h
14h	32	ADC_SAFETY_AGGR_RES2OVFCLR	502C EC14h
18h	16	ADC_SAFETY_AGGR_CHECKINTFLG	502C EC18h
1Ch	16	ADC_SAFETY_AGGR_CHECKINTFLGCLR	502C EC1Ch
20h	32	ADC_SAFETY_AGGR_CHECKINTSEL1	502C EC20h
24h	32	ADC_SAFETY_AGGR_CHECKINTSEL2	502C EC24h
28h	32	ADC_SAFETY_AGGR_CHECKINTSEL3	502C EC28h
30h	32	ADC_SAFETY_AGGR_CHECKEVT1SEL1	502C EC30h
34h	32	ADC_SAFETY_AGGR_CHECKEVT1SEL2	502C EC34h
38h	32	ADC_SAFETY_AGGR_CHECKEVT1SEL3	502C EC38h
40h	32	ADC_SAFETY_AGGR_CHECKEVT2SEL1	502C EC40h
44h	32	ADC_SAFETY_AGGR_CHECKEVT2SEL2	502C EC44h
48h	32	ADC_SAFETY_AGGR_CHECKEVT2SEL3	502C EC48h
50h	32	ADC_SAFETY_AGGR_CHECKEVT3SEL1	502C EC50h
54h	32	ADC_SAFETY_AGGR_CHECKEVT3SEL2	502C EC54h
58h	32	ADC_SAFETY_AGGR_CHECKEVT3SEL3	502C EC58h
60h	32	ADC_SAFETY_AGGR_CHECKEVT4SEL1	502C EC60h
64h	32	ADC_SAFETY_AGGR_CHECKEVT4SEL2	502C EC64h
68h	32	ADC_SAFETY_AGGR_CHECKEVT4SEL3	502C EC68h

3.3.2 ADC_SAFETY Registers

ADC_SAFETY Registers

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3.3.2.1 ADC_SAFETY_CHECKCONFIG Register

3.3.2.1.1 ADC_SAFETY_CHECKCONFIG Register (Offset = 0h) [reset = 0h]

ADC Check Configuration Register.

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Table 3-322. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C B400h
ADCSAFE_01	502C B800h
ADCSAFE_02	502C BC00h
ADCSAFE_03	502C C000h
ADCSAFE_04	502C C400h
ADCSAFE_05	502C C800h
ADCSAFE_06	502C CC00h
ADCSAFE_07	502C D000h
ADCSAFE_08	502C D400h
ADCSAFE_09	502C D800h
ADCSAFE_10	502C DC00h
ADCSAFE_11	502C E000h

Figure 3-157. ADC_SAFETY_CHECKCONFIG Name Register

15	14	13	12	11	10	9	8
CHKEN	RESERVED_2						
R/W	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2	SWSYNC	RESERVED_1	SYNCINSEL				
R	R/W1TS	R	R				
0h	0h	0h	0h				

Table 3-323. ADC_SAFETY_CHECKCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CHKEN	R/W	0h	Result Safe Check Module enable
14:7	RESERVED_2	R	0h	Reserved
6	SWSYNC	R/W1TS	0h	Result Safe Check SW Force Sync.
5	RESERVED_1	R	0h	Reserved
4:0	SYNCINSEL	R	0h	Result Safe Check Sync. In sel

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3.3.2.2 ADC_SAFETY_CHECKSTATUS Register

3.3.2.2.1 ADC_SAFETY_CHECKSTATUS Register (Offset = 4h) [reset = 0h]

ADC Check Status Register.

Return to Summary Table

Table 3-324. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C B404h
ADCSAFE_01	502C B804h
ADCSAFE_02	502C BC04h
ADCSAFE_03	502C C004h
ADCSAFE_04	502C C404h
ADCSAFE_05	502C C804h
ADCSAFE_06	502C CC04h
ADCSAFE_07	502C D004h
ADCSAFE_08	502C D404h
ADCSAFE_09	502C D804h
ADCSAFE_10	502C DC04h
ADCSAFE_11	502C E004h

Figure 3-158. ADC_SAFETY_CHECKSTATUS Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1					OOT	RES2READY	RES1READY
R					R	R	R
0h					0h	0h	0h

Table 3-325. ADC_SAFETY_CHECKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED_1	R	0h	Reserved
2	OOT	R	0h	Set when the difference between CHECKRESULT1 and CHECKRESULT2 is greater than TOLERANCE after both results have arrived. When set, further results will not be captured into the safety checker module CHECKRESULT1 or CHECKRESULT2 registers and further OOT or OVF events can't be generated. Cleared when the associated OOTx flag for all CPUs are either cleared [via the OOTFLGCLR.OOTx bit] or disabled to all ISR and events [via the CHECKINTSEL3.OOTx, CHECKEVT1SEL3.OOTx, CHECKEVT2SEL3.OOTx, CHECKEVT3SEL3.OOTx, and CHECKEVT4SEL3.OOTx registers]
1	RES2READY	R	0h	Result Safe Check Result 2 arrived. Cleared automatically when both results have arrived and the comparison occurs. Can also be cleared by issuing a software sync to the tile via the CHECKCONFIG.SWSYNC field.
0	RES1READY	R	0h	Result Safe Check Result 1 arrived. Cleared automatically when both results have arrived and the comparison occurs. Can also be cleared by issuing a software sync to the tile via the CHECKCONFIG.SWSYNC field.

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3.3.2.3 ADC_SAFETY_ADCRESSEL1 Register

3.3.2.3.1 ADC_SAFETY_ADCRESSEL1 Register (Offset = 8h) [reset = 0h]

ADC Check 1 Select Register.

Return to Summary Table

Table 3-326. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C B408h
ADCSAFE_01	502C B808h
ADCSAFE_02	502C BC08h
ADCSAFE_03	502C C008h
ADCSAFE_04	502C C408h
ADCSAFE_05	502C C808h
ADCSAFE_06	502C CC08h
ADCSAFE_07	502C D008h
ADCSAFE_08	502C D408h
ADCSAFE_09	502C D808h
ADCSAFE_10	502C DC08h
ADCSAFE_11	502C E008h

Figure 3-159. ADC_SAFETY_ADCRESSEL1 Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED_2</td><td colspan="2">ADCRESULTSEL</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">ADCRESULTSEL</td><td>RESERVED_1</td><td colspan="3">ADCSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
</table>

Table 3-327. ADC_SAFETY_ADCRESSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_2	R	0h	Reserved

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Table 3-327. ADC_SAFETY_ADCRESSEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:4	ADCRESULTSEL	R/W	0h	ADC Result Safety Checker Result Select 1 0 = ADCRESULT0 1 = ADCRESULT1 2= ADCRESULT2 3 = ADCRESULT3 4 = ADCRESULT4 5 = ADCRESULT5 6 = ADCRESULT6 7 = ADCRESULT7 8 = ADCRESULT8 9 = ADCRESULT9 10 = ADCRESULT10 11 = ADCRESULT11 12 = ADCRESULT12 13 = ADCRESULT13 14 = ADCRESULT14 15 = ADCRESULT15 16 = RESERVED 17 = RESERVED 18 = RESERVED 19 = RESERVED 20 = RESERVED 21 = RESERVED 22 = RESERVED 23 = RESERVED 24 = RESERVED 25 = RESERVED 26 = RESERVED 27 = RESERVED 28 = RESERVED 29 = RESERVED 30 = RESERVED 31 = RESERVED 32 = ADCPPBRESULT1 33 = ADCPPBRESULT2 34 = ADCPPBRESULT3 35 = ADCPPBRESULT4 36 = ADCPPBSUM1 37 = ADCPPBSUM2 38 = ADCPPBSUM3 39 = ADCPPBSUM4 ... 40 - 61 = Reserved
3	RESERVED_1	R	0h	Reserved
2:0	ADCSEL	R/W	0h	ADC Result Safety Checker ADC Select 1 0 = ADC-0 1 = ADC-1 2 = ADC-2 3 = ADC-3 4 = ADC-4 5 - 7 = Reserved

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3.3.2.4 ADC_SAFETY_ADCRESSEL2 Register

3.3.2.4.1 ADC_SAFETY_ADCRESSEL2 Register (Offset = Ch) [reset = 0h]

ADC Check 2 Select Register.

Return to Summary Table

Table 3-328. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C B40Ch
ADCSAFE_01	502C B80Ch
ADCSAFE_02	502C BC0Ch
ADCSAFE_03	502C C00Ch
ADCSAFE_04	502C C40Ch
ADCSAFE_05	502C C80Ch
ADCSAFE_06	502C CC0Ch
ADCSAFE_07	502C D00Ch
ADCSAFE_08	502C D40Ch
ADCSAFE_09	502C D80Ch
ADCSAFE_10	502C DC0Ch
ADCSAFE_11	502C E00Ch

Figure 3-160. ADC_SAFETY_ADCRESSEL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_2						ADCRESULTSEL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADCRESULTSEL				RESERVED_1	ADCSEL		
R/W				R	R/W		
0h				0h	0h		

Table 3-329. ADC_SAFETY_ADCRESSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_2	R	0h	Reserved

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Table 3-329. ADC_SAFETY_ADCRESSEL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:4	ADCRESULTSEL	R/W	0h	ADC Result Safety Checker Result Select 2 0 = ADCRESULT0 1 = ADCRESULT1 2= ADCRESULT2 3 = ADCRESULT3 4 = ADCRESULT4 5 = ADCRESULT5 6 = ADCRESULT6 7 = ADCRESULT7 8 = ADCRESULT8 9 = ADCRESULT9 10 = ADCRESULT10 11 = ADCRESULT11 12 = ADCRESULT12 13 = ADCRESULT13 14 = ADCRESULT14 15 = ADCRESULT15 16 = RESERVED 17 = RESERVED 18 = RESERVED 19 = RESERVED 20 = RESERVED 21 = RESERVED 22 = RESERVED 23 = RESERVED 24 = RESERVED 25 = RESERVED 26 = RESERVED 27 = RESERVED 28 = RESERVED 29 = RESERVED 30 = RESERVED 31 = RESERVED 32 = ADCPPBRESULT1 33 = ADCPPBRESULT2 34 = ADCPPBRESULT3 35 = ADCPPBRESULT4 36 = ADCPPBSUM1 37 = ADCPPBSUM2 38 = ADCPPBSUM3 39 = ADCPPBSUM4 ... 40 - 61 = Reserved
3	RESERVED_1	R	0h	Reserved
2:0	ADCSEL	R/W	0h	ADC Result Safety Checker ADC Select 2 0 = ADC-0 1 = ADC-1 2 = ADC-2 3 = ADC-3 4 = ADC-4 5 - 7 = Reserved

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3.3.2.5 ADC_SAFETY_TOLERANCE Register

3.3.2.5.1 ADC_SAFETY_TOLERANCE Register (Offset = 10h) [reset = 0h]

ADC Check Tolerance Register.

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Table 3-330. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C B410h
ADCSAFE_01	502C B810h
ADCSAFE_02	502C BC10h
ADCSAFE_03	502C C010h
ADCSAFE_04	502C C410h
ADCSAFE_05	502C C810h
ADCSAFE_06	502C CC10h
ADCSAFE_07	502C D010h
ADCSAFE_08	502C D410h
ADCSAFE_09	502C D810h
ADCSAFE_10	502C DC10h
ADCSAFE_11	502C E010h

Figure 3-161. ADC_SAFETY_TOLERANCE Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
TOLERANCE							
R/W							
0h							
15	14	13	12	11	10	9	8
TOLERANCE							
R/W							
0h							
7	6	5	4	3	2	1	0
TOLERANCE							
R/W							
0h							

Table 3-331. ADC_SAFETY_TOLERANCE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	TOLERANCE	R/W	0h	Tolerance for the difference between CHECKRESULT1 and CHECKRESULT2. If the difference is greater than [but not equal to] the tolerance, an out-of-tolerance event will be generated, indicated the compared ADC results are not within expected tolerance of each other.

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3.3.2.6 ADC_SAFETY_CHECKRESULT1 Register

3.3.2.6.1 ADC_SAFETY_CHECKRESULT1 Register (Offset = 18h) [reset = 0h]

ADC Check Captured Result 1 .

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Table 3-332. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C B418h
ADCSAFE_01	502C B818h
ADCSAFE_02	502C BC18h
ADCSAFE_03	502C C018h
ADCSAFE_04	502C C418h
ADCSAFE_05	502C C818h
ADCSAFE_06	502C CC18h
ADCSAFE_07	502C D018h
ADCSAFE_08	502C D418h
ADCSAFE_09	502C D818h
ADCSAFE_10	502C DC18h
ADCSAFE_11	502C E018h

Figure 3-162. ADC_SAFETY_CHECKRESULT1 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESULT							
R							
0h							
15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-333. ADC_SAFETY_CHECKRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	RESULT	R	0h	ADC Result Safety Checker Captured Result Result that was captured In the case that multiple results arrive for one selected result before one result arrives for the other result for comparison, the RES1OVF flag in CHECKSTATUS will be set. This does not prevent CHECKRESULT1 from updating to the latest result.

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3.3.2.7 ADC_SAFETY_CHECKRESULT2 Register

3.3.2.7.1 ADC_SAFETY_CHECKRESULT2 Register (Offset = 1Ch) [reset = 0h]

ADC Check Captured Result 2 .

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Table 3-334. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C B41Ch
ADCSAFE_01	502C B81Ch
ADCSAFE_02	502C BC1Ch
ADCSAFE_03	502C C01Ch
ADCSAFE_04	502C C41Ch
ADCSAFE_05	502C C81Ch
ADCSAFE_06	502C CC1Ch
ADCSAFE_07	502C D01Ch
ADCSAFE_08	502C D41Ch
ADCSAFE_09	502C D81Ch
ADCSAFE_10	502C DC1Ch
ADCSAFE_11	502C E01Ch

Figure 3-163. ADC_SAFETY_CHECKRESULT2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESULT							
R							
0h							
15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-335. ADC_SAFETY_CHECKRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	RESULT	R	0h	ADC Result Safety Checker Captured Result Result that was captured In the case that multiple results arrive for one selected result before one result arrives for the other result for comparison, the RES2OVF flag in CHECKSTATUS will be set. This does not prevent CHECKRESULT2 from updating to the latest result.

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3.3.2.8 ADC_SAFETY_AGGR_OOTFLG Register

3.3.2.8.1 ADC_SAFETY_AGGR_OOTFLG Register (Offset = 0h) [reset = 0h]

Checker Out-of-Tolerance Flag Register.

Return to Summary Table

Table 3-336. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC00h

Figure 3-164. ADC_SAFETY_AGGR_OOTFLG Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				OOT12	OOT11	OOT10	OOT9
R				R	R	R	R
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
OOT8	OOT7	OOT6	OOT5	OOT4	OOT3	OOT2	OOT1
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-337. ADC_SAFETY_AGGR_OOTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	OOT12	R	0h	ADC results safety checker 12 out-of-tolerance flag. Set when CHECK12 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
10	OOT11	R	0h	ADC results safety checker 11 out-of-tolerance flag. Set when CHECK11 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
9	OOT10	R	0h	ADC results safety checker 10 out-of-tolerance flag. Set when CHECK10 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].

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Table 3-337. ADC_SAFETY_AGGR_OOTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	OOT9	R	0h	ADC results safety checker 1 out-of-tolerance flag. Set when CHECK9 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
7	OOT8	R	0h	ADC results safety checker 8 out-of-tolerance flag. Set when CHECK8 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
6	OOT7	R	0h	ADC results safety checker 7 out-of-tolerance flag. Set when CHECK7 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
5	OOT6	R	0h	ADC results safety checker 6 out-of-tolerance flag. Set when CHECK6 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
4	OOT5	R	0h	ADC results safety checker 5 out-of-tolerance flag. Set when CHECK5 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
3	OOT4	R	0h	ADC results safety checker 4 out-of-tolerance flag. Set when CHECK4 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
2	OOT3	R	0h	ADC results safety checker 3 out-of-tolerance flag. Set when CHECK3 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
1	OOT2	R	0h	ADC results safety checker 2 out-of-tolerance flag. Set when CHECK2 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
0	OOT1	R	0h	ADC results safety checker 1 out-of-tolerance flag. Set when CHECK1 detects a difference between configured conversion results greater than the configured tolerance. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].

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3.3.2.9 ADC_SAFETY_AGGR_OOTFLGCLR Register

3.3.2.9.1 ADC_SAFETY_AGGR_OOTFLGCLR Register (Offset = 4h) [reset = 0h]

Checker Out-of-Tolerance Flag Clear Register.

Return to Summary Table

Table 3-338. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC04h

Figure 3-165. ADC_SAFETY_AGGR_OOTFLGCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				OOT12	OOT11	OOT10	OOT9
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
OOT8	OOT7	OOT6	OOT5	OOT4	OOT3	OOT2	OOT1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-339. ADC_SAFETY_AGGR_OOTFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	OOT12	R/W1TS	0h	ADC results safety checker 12 out-of-tolerance flag clear. Used to clear OOT status from CHECK12. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
10	OOT11	R/W1TS	0h	ADC results safety checker 11 out-of-tolerance flag clear. Used to clear OOT status from CHECK11. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
9	OOT10	R/W1TS	0h	ADC results safety checker 10 out-of-tolerance flag clear. Used to clear OOT status from CHECK10. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.

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Table 3-339. ADC_SAFETY_AGGR_OOTFLGCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	OOT9	R/W1TS	0h	ADC results safety checker 9 out-of-tolerance flag clear. Used to clear OOT status from CHECK9. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
7	OOT8	R/W1TS	0h	ADC results safety checker 8 out-of-tolerance flag clear. Used to clear OOT status from CHECK8. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
6	OOT7	R/W1TS	0h	ADC results safety checker 7 out-of-tolerance flag clear. Used to clear OOT status from CHECK7. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
5	OOT6	R/W1TS	0h	ADC results safety checker 6 out-of-tolerance flag clear. Used to clear OOT status from CHECK6. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
4	OOT5	R/W1TS	0h	ADC results safety checker 5 out-of-tolerance flag clear. Used to clear OOT status from CHECK5. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
3	OOT4	R/W1TS	0h	ADC results safety checker 4 out-of-tolerance flag clear. Used to clear OOT status from CHECK4. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
2	OOT3	R/W1TS	0h	ADC results safety checker 3 out-of-tolerance flag clear. Used to clear OOT status from CHECK3. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
1	OOT2	R/W1TS	0h	ADC results safety checker 2 out-of-tolerance flag clear. Used to clear OOT status from CHECK2. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
0	OOT1	R/W1TS	0h	ADC results safety checker 1 out-of-tolerance flag clear. Used to clear OOT status from CHECK1. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.

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3.3.2.10 ADC_SAFETY_AGGR_RES1OVF Register

3.3.2.10.1 ADC_SAFETY_AGGR_RES1OVF Register (Offset = 8h) [reset = 0h]

Checker Overflow Result 1 Flag Register.

Return to Summary Table

Table 3-340. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC08h

Figure 3-166. ADC_SAFETY_AGGR_RES1OVF Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				RES1OVF12	RES1OVF11	RES1OVF10	RES1OVF9
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES1OVF8	RES1OVF7	RES1OVF6	RES1OVF5	RES1OVF4	RES1OVF3	RES1OVF2	RES1OVF1
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-341. ADC_SAFETY_AGGR_RES1OVF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES1OVF12	R	0h	ADC results safety checker 12 overflow flag for result 1. Set when CHECK12 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
10	RES1OVF11	R	0h	ADC results safety checker 11 overflow flag for result 1. Set when CHECK11 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
9	RES1OVF10	R	0h	ADC results safety checker 10 overflow flag for result 1. Set when CHECK10 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].

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Table 3-341. ADC_SAFETY_AGGR_RES1OVF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RES1OVF9	R	0h	ADC results safety checker 9 overflow flag for result 1. Set when CHECK9 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
7	RES1OVF8	R	0h	ADC results safety checker 8 overflow flag for result 1. Set when CHECK8 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
6	RES1OVF7	R	0h	ADC results safety checker 7 overflow flag for result 1. Set when CHECK7 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
5	RES1OVF6	R	0h	ADC results safety checker 6 overflow flag for result 1. Set when CHECK6 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
4	RES1OVF5	R	0h	ADC results safety checker 5 overflow flag for result 1. Set when CHECK5 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
3	RES1OVF4	R	0h	ADC results safety checker 4 overflow flag for result 1. Set when CHECK4 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
2	RES1OVF3	R	0h	ADC results safety checker 3 overflow flag for result 1. Set when CHECK3 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
1	RES1OVF2	R	0h	ADC results safety checker 2 overflow flag for result 1. Set when CHECK2 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
0	RES1OVF1	R	0h	ADC results safety checker 1 overflow flag for result 1. Set when CHECK1 detects that conversion result 1 has arrived more than once before result 2 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].

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3.3.2.11 ADC_SAFETY_AGGR_RES1OVFCLR Register

3.3.2.11.1 ADC_SAFETY_AGGR_RES1OVFCLR Register (Offset = Ch) [reset = 0h]

Checker Overflow Result 1 Flag Clear Register.

Return to Summary Table

Table 3-342. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC0Ch

Figure 3-167. ADC_SAFETY_AGGR_RES1OVFCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				RES1OVF12	RES1OVF11	RES1OVF10	RES1OVF9
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RES1OVF8	RES1OVF7	RES1OVF6	RES1OVF5	RES1OVF4	RES1OVF3	RES1OVF2	RES1OVF1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-343. ADC_SAFETY_AGGR_RES1OVFCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES1OVF12	R/W1TS	0h	ADC results safety checker 12 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK12. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
10	RES1OVF11	R/W1TS	0h	ADC results safety checker 11 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK11. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
9	RES1OVF10	R/W1TS	0h	ADC results safety checker 10 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK10. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.

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Table 3-343. ADC_SAFETY_AGGR_RES1OVFCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RES1OVF9	R/W1TS	0h	ADC results safety checker 9 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK9. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
7	RES1OVF8	R/W1TS	0h	ADC results safety checker 8 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK8. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
6	RES1OVF7	R/W1TS	0h	ADC results safety checker 7 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK7. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
5	RES1OVF6	R/W1TS	0h	ADC results safety checker 6 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK6. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
4	RES1OVF5	R/W1TS	0h	ADC results safety checker 5 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK5. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
3	RES1OVF4	R/W1TS	0h	ADC results safety checker 4 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK4. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
2	RES1OVF3	R/W1TS	0h	ADC results safety checker 3 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK3. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
1	RES1OVF2	R/W1TS	0h	ADC results safety checker 2 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK2. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
0	RES1OVF1	R/W1TS	0h	ADC results safety checker 1 result 1 overflow flag clear. Used to clear RES1OVF status from CHECK1. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.

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3.3.2.12 ADC_SAFETY_AGGR_RES2OVF Register

3.3.2.12.1 ADC_SAFETY_AGGR_RES2OVF Register (Offset = 10h) [reset = 0h]

Checker Overflow Result 2 Flag Register.

Return to Summary Table

Table 3-344. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC10h

Figure 3-168. ADC_SAFETY_AGGR_RES2OVF Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				RES2OVF12	RES2OVF11	RES2OVF10	RES2OVF9
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES2OVF8	RES2OVF7	RES2OVF6	RES2OVF5	RES2OVF4	RES2OVF3	RES2OVF2	RES2OVF1
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-345. ADC_SAFETY_AGGR_RES2OVF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES2OVF12	R	0h	ADC results safety checker 12 overflow flag for result 2. Set when CHECK12 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
10	RES2OVF11	R	0h	ADC results safety checker 11 overflow flag for result 2. Set when CHECK11 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
9	RES2OVF10	R	0h	ADC results safety checker 10 overflow flag for result 2. Set when CHECK10 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].

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Table 3-345. ADC_SAFETY_AGGR_RES2OVF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RES2OVF9	R	0h	ADC results safety checker 9 overflow flag for result 2. Set when CHECK9 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
7	RES2OVF8	R	0h	ADC results safety checker 8 overflow flag for result 2. Set when CHECK8 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
6	RES2OVF7	R	0h	ADC results safety checker 7 overflow flag for result 2. Set when CHECK7 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
5	RES2OVF6	R	0h	ADC results safety checker 6 overflow flag for result 2. Set when CHECK6 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
4	RES2OVF5	R	0h	ADC results safety checker 5 overflow flag for result 2. Set when CHECK5 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
3	RES2OVF4	R	0h	ADC results safety checker 4 overflow flag for result 2. Set when CHECK4 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
2	RES2OVF3	R	0h	ADC results safety checker 3 overflow flag for result 2. Set when CHECK3 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
1	RES2OVF2	R	0h	ADC results safety checker 2 overflow flag for result 2. Set when CHECK2 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].
0	RES2OVF1	R	0h	ADC results safety checker 1 overflow flag for result 2. Set when CHECK1 detects that conversion result 2 has arrived more than once before result 1 has arrived. Use the CHECKINTSEL1, CHECKINTSEL2, CHECKINTSEL3, CHECKEVTxSEL1, CHECKEVTxSEL2, and CHECKEVTxSEL3 registers to aggregate detected OOT and OVF flags into interrupt [INT] or X-bar events [EVT].

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3.3.2.13 ADC_SAFETY_AGGR_RES2OVFCLR Register

3.3.2.13.1 ADC_SAFETY_AGGR_RES2OVFCLR Register (Offset = 14h) [reset = 0h]

Checker Overflow Result 2 Flag Clear Register.

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Table 3-346. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC14h

Figure 3-169. ADC_SAFETY_AGGR_RES2OVFCLR Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				RES2OVF12	RES2OVF11	RES2OVF10	RES2OVF9
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES2OVF8	RES2OVF7	RES2OVF6	RES2OVF5	RES2OVF4	RES2OVF3	RES2OVF2	RES2OVF1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-347. ADC_SAFETY_AGGR_RES2OVFCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES2OVF12	R/W1TS	0h	ADC results safety checker 12 result overflow flag clear. Used to clear OVF status from CHECK12. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHECKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
10	RES2OVF11	R/W1TS	0h	ADC results safety checker 11 result overflow flag clear. Used to clear OVF status from CHECK11. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHECKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
9	RES2OVF10	R/W1TS	0h	ADC results safety checker 10 result overflow flag clear. Used to clear OVF status from CHECK10. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHECKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.

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Table 3-347. ADC_SAFETY_AGGR_RES2OVFCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RES2OVF9	R/W1TS	0h	ADC results safety checker 9 result overflow flag clear. Used to clear OVF status from CHECK9. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
7	RES2OVF8	R/W1TS	0h	ADC results safety checker 8 result overflow flag clear. Used to clear OVF status from CHECK8. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHECKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
6	RES2OVF7	R/W1TS	0h	ADC results safety checker 7 result overflow flag clear. Used to clear OVF status from CHECK7. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHECKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
5	RES2OVF6	R/W1TS	0h	ADC results safety checker 6 result overflow flag clear. Used to clear OVF status from CHECK6. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHECKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
4	RES2OVF5	R/W1TS	0h	ADC results safety checker 5 result overflow flag clear. Used to clear OVF status from CHECK5. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
3	RES2OVF4	R/W1TS	0h	ADC results safety checker 4 result overflow flag clear. Used to clear OVF status from CHECK4. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHECKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
2	RES2OVF3	R/W1TS	0h	ADC results safety checker 3 result overflow flag clear. Used to clear OVF status from CHECK3. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHECKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
1	RES2OVF2	R/W1TS	0h	ADC results safety checker 2 result overflow flag clear. Used to clear OVF status from CHECK2. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHECKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.
0	RES2OVF1	R/W1TS	0h	ADC results safety checker 1 result overflow flag clear. Used to clear OVF status from CHECK1. In the case of a safety checker interrupt, clear all serviced OOT or OVF flags first, then clear the global interrupt flag [in the CHECKINTFLG register] using the CHKINTFLGCLR register. In the case of a safety checker X-bar event, clear all associated OOT or OVF flags to clear the event.

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3.3.2.14 ADC_SAFETY_AGGR_CHECKINTFLG Register

3.3.2.14.1 ADC_SAFETY_AGGR_CHECKINTFLG Register (Offset = 18h) [reset = 0h]

Checker Interrupt Flag Register.

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Table 3-348. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC18h

Figure 3-170. ADC_SAFETY_AGGR_CHECKINTFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							CHECKINT
R							R
0h							0h

Table 3-349. ADC_SAFETY_AGGR_CHECKINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	CHECKINT	R	0h	ADC results safety checker subsytem interrupt flag. Indicates that one or more configured OOT or OVF conditions have occurred in the individual safety checker modules. In the ISR, clear all serviced OOT or OVF flags first [using the OOTFLGCLR and OVFFLGCLR registers], then clear this flag using the CHKINTFLGCLR register. The CHECKINTSEL1 and CHECKINTSEL2 registers are used to select which OOT and OVF flags from the individual checker modules can trigger this interrupt.

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3.3.2.15 ADC_SAFETY_AGGR_CHECKINTFLGCLR Register

3.3.2.15.1 ADC_SAFETY_AGGR_CHECKINTFLGCLR Register (Offset = 1Ch) [reset = 0h]

Checker Interrupt Flag Clear Register.

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Table 3-350. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC1Ch

Figure 3-171. ADC_SAFETY_AGGR_CHECKINTFLGCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							CHECKINTCLR
R							R/W1TS
0h							0h

Table 3-351. ADC_SAFETY_AGGR_CHECKINTFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	CHECKINTCLR	R/W1TS	0h	ADC results safety checker subsytem interrupt flag clear. Used to clear the global safety checker subsystem interrupt flag. In the ISR, clear all serviced OOT or OVF flags first [using the OOTFLGCLR and OVFFLGCLR registers], then clear the global CHECKINT flag using the this register.

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3.3.2.16 ADC_SAFETY_AGGR_CHECKINTSEL1 Register

3.3.2.16.1 ADC_SAFETY_AGGR_CHECKINTSEL1 Register (Offset = 20h) [reset = 0h]

Checker Interrupt Source Select Register 1

Return to Summary Table

Table 3-352. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC20h

Figure 3-172. ADC_SAFETY_AGGR_CHECKINTSEL1 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				RES1OVF12EN	RES1OVF11EN	RES1OVF10EN	RES1OVF9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES1OVF8EN	RES1OVF7EN	RES1OVF6EN	RES1OVF5EN	RES1OVF4EN	RES1OVF3EN	RES1OVF2EN	RES1OVF1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-353. ADC_SAFETY_AGGR_CHECKINTSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES1OVF12EN	R/W	0h	Enable CHECK12 RES1OVF as a source for CHECKINT.
10	RES1OVF11EN	R/W	0h	Enable CHECK11 RES1OVF as a source for CHECKINT.
9	RES1OVF10EN	R/W	0h	Enable CHECK10 RES1OVF as a source for CHECKINT.
8	RES1OVF9EN	R/W	0h	Enable CHECK9 RES1OVF as a source for CHECKINT.
7	RES1OVF8EN	R/W	0h	Enable CHECK8 RES1OVF as a source for CHECKINT.
6	RES1OVF7EN	R/W	0h	Enable CHECK7 RES1OVF as a source for CHECKINT.
5	RES1OVF6EN	R/W	0h	Enable CHECK6 RES1OVF as a source for CHECKINT.
4	RES1OVF5EN	R/W	0h	Enable CHECK5 RES1OVF as a source for CHECKINT.
3	RES1OVF4EN	R/W	0h	Enable CHECK4 RES1OVF as a source for CHECKINT.
2	RES1OVF3EN	R/W	0h	Enable CHECK3 RES1OVF as a source for CHECKINT.
1	RES1OVF2EN	R/W	0h	Enable CHECK2 RES1OVF as a source for CHECKINT.
0	RES1OVF1EN	R/W	0h	Enable CHECK1 RES1OVF as a source for CHECKINT.

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3.3.2.17 ADC_SAFETY_AGGR_CHECKINTSEL2 Register

3.3.2.17.1 ADC_SAFETY_AGGR_CHECKINTSEL2 Register (Offset = 24h) [reset = 0h]

Checker Interrupt Source Select Register 2

Return to Summary Table

Table 3-354. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC24h

Figure 3-173. ADC_SAFETY_AGGR_CHECKINTSEL2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				RES2OVF12EN	RES2OVF11EN	RES2OVF10EN	RES2OVF9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES2OVF8EN	RES2OVF7EN	RES2OVF6EN	RES2OVF5EN	RES2OVF4EN	RES2OVF3EN	RES2OVF2EN	RES2OVF1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-355. ADC_SAFETY_AGGR_CHECKINTSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES2OVF12EN	R/W	0h	Enable CHECK12 RES2OVF as a source for CHECKINT.
10	RES2OVF11EN	R/W	0h	Enable CHECK11 RES2OVF as a source for CHECKINT.
9	RES2OVF10EN	R/W	0h	Enable CHECK10 RES2OVF as a source for CHECKINT.
8	RES2OVF9EN	R/W	0h	Enable CHECK9 RES2OVF as a source for CHECKINT.
7	RES2OVF8EN	R/W	0h	Enable CHECK8 RES2OVF as a source for CHECKINT.
6	RES2OVF7EN	R/W	0h	Enable CHECK7 RES2OVF as a source for CHECKINT.
5	RES2OVF6EN	R/W	0h	Enable CHECK6 RES2OVF as a source for CHECKINT.
4	RES2OVF5EN	R/W	0h	Enable CHECK5 RES2OVF as a source for CHECKINT.
3	RES2OVF4EN	R/W	0h	Enable CHECK4 RES2OVF as a source for CHECKINT.
2	RES2OVF3EN	R/W	0h	Enable CHECK3 RES2OVF as a source for CHECKINT.
1	RES2OVF2EN	R/W	0h	Enable CHECK2 RES2OVF as a source for CHECKINT.
0	RES2OVF1EN	R/W	0h	Enable CHECK1 RES2OVF as a source for CHECKINT.

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3.3.2.18 ADC_SAFETY_AGGR_CHECKINTSEL3 Register

3.3.2.18.1 ADC_SAFETY_AGGR_CHECKINTSEL3 Register (Offset = 28h) [reset = 0h]

Checker Interrupt Source Select Register 3

Return to Summary Table

Table 3-356. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC28h

Figure 3-174. ADC_SAFETY_AGGR_CHECKINTSEL3 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				OOT12EN	OOT11EN	OOT10EN	OOT9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
OOT8EN	OOT7EN	OOT6EN	OOT5EN	OOT4EN	OOT3EN	OOT2EN	OOT1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-357. ADC_SAFETY_AGGR_CHECKINTSEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	OOT12EN	R/W	0h	Enable CHECK12 OOT as a source for CHECKINT.
10	OOT11EN	R/W	0h	Enable CHECK11 OOT as a source for CHECKINT.
9	OOT10EN	R/W	0h	Enable CHECK10 OOT as a source for CHECKINT.
8	OOT9EN	R/W	0h	Enable CHECK9 OOT as a source for CHECKINT.
7	OOT8EN	R/W	0h	Enable CHECK8 OOT as a source for CHECKINT.
6	OOT7EN	R/W	0h	Enable CHECK7 OOT as a source for CHECKINT.
5	OOT6EN	R/W	0h	Enable CHECK6 OOT as a source for CHECKINT.
4	OOT5EN	R/W	0h	Enable CHECK5 OOT as a source for CHECKINT.
3	OOT4EN	R/W	0h	Enable CHECK4 OOT as a source for CHECKINT.
2	OOT3EN	R/W	0h	Enable CHECK3 OOT as a source for CHECKINT.
1	OOT2EN	R/W	0h	Enable CHECK2 OOT as a source for CHECKINT.
0	OOT1EN	R/W	0h	Enable CHECK1 OOT as a source for CHECKINT.

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3.3.2.19 ADC_SAFETY_AGGR_CHECKEVT1SEL1 Register

3.3.2.19.1 ADC_SAFETY_AGGR_CHECKEVT1SEL1 Register (Offset = 30h) [reset = 0h]

Checker X-Bar EVT1 Source Select Register 1

Return to Summary Table

Table 3-358. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC30h

Figure 3-175. ADC_SAFETY_AGGR_CHECKEVT1SEL1 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				RES1OVF12EN	RES1OVF11EN	RES1OVF10EN	RES1OVF9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RES1OVF8EN	RES1OVF7EN	RES1OVF6EN	RES1OVF5EN	RES1OVF4EN	RES1OVF3EN	RES1OVF2EN	RES1OVF1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-359. ADC_SAFETY_AGGR_CHECKEVT1SEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES1OVF12EN	R/W	0h	Enable CHECK12 RES1OVF as a source for CHECKEVT1.
10	RES1OVF11EN	R/W	0h	Enable CHECK11 RES1OVF as a source for CHECKEVT1.
9	RES1OVF10EN	R/W	0h	Enable CHECK10 RES1OVF as a source for CHECKEVT1.
8	RES1OVF9EN	R/W	0h	Enable CHECK9 RES1OVF as a source for CHECKEVT1.
7	RES1OVF8EN	R/W	0h	Enable CHECK8 RES1OVF as a source for CHECKEVT1.
6	RES1OVF7EN	R/W	0h	Enable CHECK7 RES1OVF as a source for CHECKEVT1.
5	RES1OVF6EN	R/W	0h	Enable CHECK6 RES1OVF as a source for CHECKEVT1.
4	RES1OVF5EN	R/W	0h	Enable CHECK5 RES1OVF as a source for CHECKEVT1.
3	RES1OVF4EN	R/W	0h	Enable CHECK4 RES1OVF as a source for CHECKEVT1.
2	RES1OVF3EN	R/W	0h	Enable CHECK3 RES1OVF as a source for CHECKEVT1.
1	RES1OVF2EN	R/W	0h	Enable CHECK2 RES1OVF as a source for CHECKEVT1.
0	RES1OVF1EN	R/W	0h	Enable CHECK1 RES1OVF as a source for CHECKEVT1.

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3.3.2.20 ADC_SAFETY_AGGR_CHECKEVT1SEL2 Register

3.3.2.20.1 ADC_SAFETY_AGGR_CHECKEVT1SEL2 Register (Offset = 34h) [reset = 0h]

Checker X-Bar EVT1 Source Select Register 2

Return to Summary Table

Table 3-360. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC34h

Figure 3-176. ADC_SAFETY_AGGR_CHECKEVT1SEL2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				RES2OVF12EN	RES2OVF11EN	RES2OVF10EN	RES2OVF9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES2OVF8EN	RES2OVF7EN	RES2OVF6EN	RES2OVF5EN	RES2OVF4EN	RES2OVF3EN	RES2OVF2EN	RES2OVF1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-361. ADC_SAFETY_AGGR_CHECKEVT1SEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES2OVF12EN	R/W	0h	Enable CHECK12 RES2OVF as a source for CHECKEVT1.
10	RES2OVF11EN	R/W	0h	Enable CHECK11 RES2OVF as a source for CHECKEVT1.
9	RES2OVF10EN	R/W	0h	Enable CHECK10 RES2OVF as a source for CHECKEVT1.
8	RES2OVF9EN	R/W	0h	Enable CHECK9 RES2OVF as a source for CHECKEVT1.
7	RES2OVF8EN	R/W	0h	Enable CHECK8 RES2OVF as a source for CHECKEVT1.
6	RES2OVF7EN	R/W	0h	Enable CHECK7 RES2OVF as a source for CHECKEVT1.
5	RES2OVF6EN	R/W	0h	Enable CHECK6 RES2OVF as a source for CHECKEVT1.
4	RES2OVF5EN	R/W	0h	Enable CHECK5 RES2OVF as a source for CHECKEVT1.
3	RES2OVF4EN	R/W	0h	Enable CHECK4 RES2OVF as a source for CHECKEVT1.
2	RES2OVF3EN	R/W	0h	Enable CHECK3 RES2OVF as a source for CHECKEVT1.
1	RES2OVF2EN	R/W	0h	Enable CHECK2 RES2OVF as a source for CHECKEVT1.
0	RES2OVF1EN	R/W	0h	Enable CHECK1 RES2OVF as a source for CHECKEVT1.

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3.3.2.21 ADC_SAFETY_AGGR_CHECKEVT1SEL3 Register

3.3.2.21.1 ADC_SAFETY_AGGR_CHECKEVT1SEL3 Register (Offset = 38h) [reset = 0h]

Checker X-Bar EVT1 Source Select Register 3

Return to Summary Table

Table 3-362. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC38h

Figure 3-177. ADC_SAFETY_AGGR_CHECKEVT1SEL3 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				OOT12EN	OOT11EN	OOT10EN	OOT9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
OOT8EN	OOT7EN	OOT6EN	OOT5EN	OOT4EN	OOT3EN	OOT2EN	OOT1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-363. ADC_SAFETY_AGGR_CHECKEVT1SEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	OOT12EN	R/W	0h	Enable CHECK12 OOT as a source for CHECKEVT1.
10	OOT11EN	R/W	0h	Enable CHECK11 OOTas a source for CHECKEVT1.
9	OOT10EN	R/W	0h	Enable CHECK10 OOT as a source for CHECKEVT1.
8	OOT9EN	R/W	0h	Enable CHECK9 OOT as a source for CHECKEVT1.
7	OOT8EN	R/W	0h	Enable CHECK8 OOT as a source for CHECKEVT1.
6	OOT7EN	R/W	0h	Enable CHECK7 OOTas a source for CHECKEVT1.
5	OOT6EN	R/W	0h	Enable CHECK6 OOT as a source for CHECKEVT1.
4	OOT5EN	R/W	0h	Enable CHECK5 OOT as a source for CHECKEVT1.
3	OOT4EN	R/W	0h	Enable CHECK4 OOT as a source for CHECKEVT1.
2	OOT3EN	R/W	0h	Enable CHECK3 OOTas a source for CHECKEVT1.
1	OOT2EN	R/W	0h	Enable CHECK2 OOT as a source for CHECKEVT1.
0	OOT1EN	R/W	0h	Enable CHECK1 OOT as a source for CHECKEVT1.

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3.3.2.22 ADC_SAFETY_AGGR_CHECKEVT2SEL1 Register

3.3.2.22.1 ADC_SAFETY_AGGR_CHECKEVT2SEL1 Register (Offset = 40h) [reset = 0h]

Checker X-Bar EVT2 Source Select Register 1

Return to Summary Table

Table 3-364. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC40h

Figure 3-178. ADC_SAFETY_AGGR_CHECKEVT2SEL1 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				RES1OVF12EN	RES1OVF11EN	RES1OVF10EN	RES1OVF9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES1OVF8EN	RES1OVF7EN	RES1OVF6EN	RES1OVF5EN	RES1OVF4EN	RES1OVF3EN	RES1OVF2EN	RES1OVF1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-365. ADC_SAFETY_AGGR_CHECKEVT2SEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES1OVF12EN	R/W	0h	Enable CHECK12 RES1OVF as a source for CHECKEVT2.
10	RES1OVF11EN	R/W	0h	Enable CHECK11 RES1OVF as a source for CHECKEVT2.
9	RES1OVF10EN	R/W	0h	Enable CHECK10 RES1OVF as a source for CHECKEVT2.
8	RES1OVF9EN	R/W	0h	Enable CHECK9 RES1OVF as a source for CHECKEVT2.
7	RES1OVF8EN	R/W	0h	Enable CHECK8 RES1OVF as a source for CHECKEVT2.
6	RES1OVF7EN	R/W	0h	Enable CHECK7 RES1OVF as a source for CHECKEVT2.
5	RES1OVF6EN	R/W	0h	Enable CHECK6 RES1OVF as a source for CHECKEVT2.
4	RES1OVF5EN	R/W	0h	Enable CHECK5 RES1OVF as a source for CHECKEVT2.
3	RES1OVF4EN	R/W	0h	Enable CHECK4 RES1OVF as a source for CHECKEVT2.
2	RES1OVF3EN	R/W	0h	Enable CHECK3 RES1OVF as a source for CHECKEVT2.
1	RES1OVF2EN	R/W	0h	Enable CHECK2 RES1OVF as a source for CHECKEVT2.
0	RES1OVF1EN	R/W	0h	Enable CHECK1 RES1OVF as a source for CHECKEVT2.

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3.3.2.23 ADC_SAFETY_AGGR_CHECKEVT2SEL2 Register

3.3.2.23.1 ADC_SAFETY_AGGR_CHECKEVT2SEL2 Register (Offset = 44h) [reset = 0h]

Checker X-Bar EVT2 Source Select Register 2

Return to Summary Table

Table 3-366. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC44h

Figure 3-179. ADC_SAFETY_AGGR_CHECKEVT2SEL2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				RES2OVF12EN	RES2OVF11EN	RES2OVF10EN	RES2OVF9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RES2OVF8EN	RES2OVF7EN	RES2OVF6EN	RES2OVF5EN	RES2OVF4EN	RES2OVF3EN	RES2OVF2EN	RES2OVF1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-367. ADC_SAFETY_AGGR_CHECKEVT2SEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES2OVF12EN	R/W	0h	Enable CHECK12 RES2OVF as a source for CHECKEVT2.
10	RES2OVF11EN	R/W	0h	Enable CHECK11 RES2OVF as a source for CHECKEVT2.
9	RES2OVF10EN	R/W	0h	Enable CHECK10 RES2OVF as a source for CHECKEVT2.
8	RES2OVF9EN	R/W	0h	Enable CHECK9 RES2OVF as a source for CHECKEVT2.
7	RES2OVF8EN	R/W	0h	Enable CHECK8 RES2OVF as a source for CHECKEVT2.
6	RES2OVF7EN	R/W	0h	Enable CHECK7 RES2OVF as a source for CHECKEVT2.
5	RES2OVF6EN	R/W	0h	Enable CHECK6 RES2OVF as a source for CHECKEVT2.
4	RES2OVF5EN	R/W	0h	Enable CHECK5 RES2OVF as a source for CHECKEVT2.
3	RES2OVF4EN	R/W	0h	Enable CHECK4 RES2OVF as a source for CHECKEVT2.
2	RES2OVF3EN	R/W	0h	Enable CHECK3 RES2OVF as a source for CHECKEVT2.
1	RES2OVF2EN	R/W	0h	Enable CHECK2 RES2OVF as a source for CHECKEVT2.
0	RES2OVF1EN	R/W	0h	Enable CHECK1 RES2OVF as a source for CHECKEVT2.

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3.3.2.24 ADC_SAFETY_AGGR_CHECKEVT2SEL3 Register

3.3.2.24.1 ADC_SAFETY_AGGR_CHECKEVT2SEL3 Register (Offset = 48h) [reset = 0h]

Checker X-Bar EVT2 Source Select Register 3

Return to Summary Table

Table 3-368. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC48h

Figure 3-180. ADC_SAFETY_AGGR_CHECKEVT2SEL3 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				OOT12EN	OOT11EN	OOT10EN	OOT9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
OOT8EN	OOT7EN	OOT6EN	OOT5EN	OOT4EN	OOT3EN	OOT2EN	OOT1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-369. ADC_SAFETY_AGGR_CHECKEVT2SEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	OOT12EN	R/W	0h	Enable CHECK12 OOT as a source for CHECKEVT2.
10	OOT11EN	R/W	0h	Enable CHECK11 OOTas a source for CHECKEVT2.
9	OOT10EN	R/W	0h	Enable CHECK10 OOT as a source for CHECKEVT2.
8	OOT9EN	R/W	0h	Enable CHECK9 OOT as a source for CHECKEVT2.
7	OOT8EN	R/W	0h	Enable CHECK8 OOT as a source for CHECKEVT2.
6	OOT7EN	R/W	0h	Enable CHECK7 OOTas a source for CHECKEVT2.
5	OOT6EN	R/W	0h	Enable CHECK6 OOT as a source for CHECKEVT2.
4	OOT5EN	R/W	0h	Enable CHECK5 OOT as a source for CHECKEVT2.
3	OOT4EN	R/W	0h	Enable CHECK4 OOT as a source for CHECKEVT2.
2	OOT3EN	R/W	0h	Enable CHECK3 OOTas a source for CHECKEVT2.
1	OOT2EN	R/W	0h	Enable CHECK2 OOT as a source for CHECKEVT2.
0	OOT1EN	R/W	0h	Enable CHECK1 OOT as a source for CHECKEVT2.

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3.3.2.25 ADC_SAFETY_AGGR_CHECKEVT3SEL1 Register

3.3.2.25.1 ADC_SAFETY_AGGR_CHECKEVT3SEL1 Register (Offset = 50h) [reset = 0h]

Checker X-Bar EVT3 Source Select Register 1

Return to Summary Table

Table 3-370. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC50h

Figure 3-181. ADC_SAFETY_AGGR_CHECKEVT3SEL1 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				RES1OVF12EN	RES1OVF11EN	RES1OVF10EN	RES1OVF9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES1OVF8EN	RES1OVF7EN	RES1OVF6EN	RES1OVF5EN	RES1OVF4EN	RES1OVF3EN	RES1OVF2EN	RES1OVF1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-371. ADC_SAFETY_AGGR_CHECKEVT3SEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES1OVF12EN	R/W	0h	Enable CHECK12 RES1OVF as a source for CHECKEVT3.
10	RES1OVF11EN	R/W	0h	Enable CHECK11 RES1OVF as a source for CHECKEVT3.
9	RES1OVF10EN	R/W	0h	Enable CHECK10 RES1OVF as a source for CHECKEVT3.
8	RES1OVF9EN	R/W	0h	Enable CHECK9 RES1OVF as a source for CHECKEVT3.
7	RES1OVF8EN	R/W	0h	Enable CHECK8 RES1OVF as a source for CHECKEVT3.
6	RES1OVF7EN	R/W	0h	Enable CHECK7 RES1OVF as a source for CHECKEVT3.
5	RES1OVF6EN	R/W	0h	Enable CHECK6 RES1OVF as a source for CHECKEVT3.
4	RES1OVF5EN	R/W	0h	Enable CHECK5 RES1OVF as a source for CHECKEVT3.
3	RES1OVF4EN	R/W	0h	Enable CHECK4 RES1OVF as a source for CHECKEVT3.
2	RES1OVF3EN	R/W	0h	Enable CHECK3 RES1OVF as a source for CHECKEVT3.
1	RES1OVF2EN	R/W	0h	Enable CHECK2 RES1OVF as a source for CHECKEVT3.
0	RES1OVF1EN	R/W	0h	Enable CHECK1 RES1OVF as a source for CHECKEVT3.

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3.3.2.26 ADC_SAFETY_AGGR_CHECKEVT3SEL2 Register

3.3.2.26.1 ADC_SAFETY_AGGR_CHECKEVT3SEL2 Register (Offset = 54h) [reset = 0h]

Checker X-Bar EVT3 Source Select Register 2

Return to Summary Table

Table 3-372. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC54h

Figure 3-182. ADC_SAFETY_AGGR_CHECKEVT3SEL2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				RES2OVF12EN	RES2OVF11EN	RES2OVF10EN	RES2OVF9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RES2OVF8EN	RES2OVF7EN	RES2OVF6EN	RES2OVF5EN	RES2OVF4EN	RES2OVF3EN	RES2OVF2EN	RES2OVF1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-373. ADC_SAFETY_AGGR_CHECKEVT3SEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES2OVF12EN	R/W	0h	Enable CHECK12 RES2OVF as a source for CHECKEVT3.
10	RES2OVF11EN	R/W	0h	Enable CHECK11 RES2OVF as a source for CHECKEVT3.
9	RES2OVF10EN	R/W	0h	Enable CHECK10 RES2OVF as a source for CHECKEVT3.
8	RES2OVF9EN	R/W	0h	Enable CHECK9 RES2OVF as a source for CHECKEVT3.
7	RES2OVF8EN	R/W	0h	Enable CHECK8 RES2OVF as a source for CHECKEVT3.
6	RES2OVF7EN	R/W	0h	Enable CHECK7 RES2OVF as a source for CHECKEVT3.
5	RES2OVF6EN	R/W	0h	Enable CHECK6 RES2OVF as a source for CHECKEVT3.
4	RES2OVF5EN	R/W	0h	Enable CHECK5 RES2OVF as a source for CHECKEVT3.
3	RES2OVF4EN	R/W	0h	Enable CHECK4 RES2OVF as a source for CHECKEVT3.
2	RES2OVF3EN	R/W	0h	Enable CHECK3 RES2OVF as a source for CHECKEVT3.
1	RES2OVF2EN	R/W	0h	Enable CHECK2 RES2OVF as a source for CHECKEVT3.
0	RES2OVF1EN	R/W	0h	Enable CHECK1 RES2OVF as a source for CHECKEVT3.

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3.3.2.27 ADC_SAFETY_AGGR_CHECKEVT3SEL3 Register

3.3.2.27.1 ADC_SAFETY_AGGR_CHECKEVT3SEL3 Register (Offset = 58h) [reset = 0h]

Checker X-Bar EVT3 Source Select Register 3

Return to Summary Table

Table 3-374. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC58h

Figure 3-183. ADC_SAFETY_AGGR_CHECKEVT3SEL3 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				OOT12EN	OOT11EN	OOT10EN	OOT9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
OOT8EN	OOT7EN	OOT6EN	OOT5EN	OOT4EN	OOT3EN	OOT2EN	OOT1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-375. ADC_SAFETY_AGGR_CHECKEVT3SEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	OOT12EN	R/W	0h	Enable CHECK12 OOT as a source for CHECKEVT3.
10	OOT11EN	R/W	0h	Enable CHECK11 OOTas a source for CHECKEVT3.
9	OOT10EN	R/W	0h	Enable CHECK10 OOT as a source for CHECKEVT3.
8	OOT9EN	R/W	0h	Enable CHECK9 OOT as a source for CHECKEVT3.
7	OOT8EN	R/W	0h	Enable CHECK8 OOT as a source for CHECKEVT3.
6	OOT7EN	R/W	0h	Enable CHECK7 OOTas a source for CHECKEVT3.
5	OOT6EN	R/W	0h	Enable CHECK6 OOT as a source for CHECKEVT3.
4	OOT5EN	R/W	0h	Enable CHECK5 OOT as a source for CHECKEVT3.
3	OOT4EN	R/W	0h	Enable CHECK4 OOT as a source for CHECKEVT3.
2	OOT3EN	R/W	0h	Enable CHECK3 OOTas a source for CHECKEVT3.
1	OOT2EN	R/W	0h	Enable CHECK2 OOT as a source for CHECKEVT3.
0	OOT1EN	R/W	0h	Enable CHECK1 OOT as a source for CHECKEVT3.

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3.3.2.28 ADC_SAFETY_AGGR_CHECKEVT4SEL1 Register

3.3.2.28.1 ADC_SAFETY_AGGR_CHECKEVT4SEL1 Register (Offset = 60h) [reset = 0h]

Checker X-Bar EVT4 Source Select Register 1

Return to Summary Table

Table 3-376. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC60h

Figure 3-184. ADC_SAFETY_AGGR_CHECKEVT4SEL1 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				RES1OVF12EN	RES1OVF11EN	RES1OVF10EN	RES1OVF9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES1OVF8EN	RES1OVF7EN	RES1OVF6EN	RES1OVF5EN	RES1OVF4EN	RES1OVF3EN	RES1OVF2EN	RES1OVF1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-377. ADC_SAFETY_AGGR_CHECKEVT4SEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES1OVF12EN	R/W	0h	Enable CHECK12 RES1OVF as a source for CHECKEVT4.
10	RES1OVF11EN	R/W	0h	Enable CHECK11 RES1OVF as a source for CHECKEVT4.
9	RES1OVF10EN	R/W	0h	Enable CHECK10 RES1OVF as a source for CHECKEVT4.
8	RES1OVF9EN	R/W	0h	Enable CHECK9 RES1OVF as a source for CHECKEVT4.
7	RES1OVF8EN	R/W	0h	Enable CHECK8 RES1OVF as a source for CHECKEVT4.
6	RES1OVF7EN	R/W	0h	Enable CHECK7 RES1OVF as a source for CHECKEVT4.
5	RES1OVF6EN	R/W	0h	Enable CHECK6 RES1OVF as a source for CHECKEVT4.
4	RES1OVF5EN	R/W	0h	Enable CHECK5 RES1OVF as a source for CHECKEVT4.
3	RES1OVF4EN	R/W	0h	Enable CHECK4 RES1OVF as a source for CHECKEVT4.
2	RES1OVF3EN	R/W	0h	Enable CHECK3 RES1OVF as a source for CHECKEVT4.
1	RES1OVF2EN	R/W	0h	Enable CHECK2 RES1OVF as a source for CHECKEVT4.
0	RES1OVF1EN	R/W	0h	Enable CHECK1 RES1OVF as a source for CHECKEVT4.

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3.3.2.29 ADC_SAFETY_AGGR_CHECKEVT4SEL2 Register

3.3.2.29.1 ADC_SAFETY_AGGR_CHECKEVT4SEL2 Register (Offset = 64h) [reset = 0h]

Checker X-Bar EVT4 Source Select Register 2

Return to Summary Table

Table 3-378. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC64h

Figure 3-185. ADC_SAFETY_AGGR_CHECKEVT4SEL2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1				RES2OVF12EN	RES2OVF11EN	RES2OVF10EN	RES2OVF9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES2OVF8EN	RES2OVF7EN	RES2OVF6EN	RES2OVF5EN	RES2OVF4EN	RES2OVF3EN	RES2OVF2EN	RES2OVF1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-379. ADC_SAFETY_AGGR_CHECKEVT4SEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	RES2OVF12EN	R/W	0h	Enable CHECK12 RES2OVF as a source for CHECKEVT4.
10	RES2OVF11EN	R/W	0h	Enable CHECK11 RES2OVF as a source for CHECKEVT4.
9	RES2OVF10EN	R/W	0h	Enable CHECK10 RES2OVF as a source for CHECKEVT4.
8	RES2OVF9EN	R/W	0h	Enable CHECK9 RES2OVF as a source for CHECKEVT4.
7	RES2OVF8EN	R/W	0h	Enable CHECK8 RES2OVF as a source for CHECKEVT4.
6	RES2OVF7EN	R/W	0h	Enable CHECK7 RES2OVF as a source for CHECKEVT4.
5	RES2OVF6EN	R/W	0h	Enable CHECK6 RES2OVF as a source for CHECKEVT4.
4	RES2OVF5EN	R/W	0h	Enable CHECK5 RES2OVF as a source for CHECKEVT4.
3	RES2OVF4EN	R/W	0h	Enable CHECK4 RES2OVF as a source for CHECKEVT4.
2	RES2OVF3EN	R/W	0h	Enable CHECK3 RES2OVF as a source for CHECKEVT4.
1	RES2OVF2EN	R/W	0h	Enable CHECK2 RES2OVF as a source for CHECKEVT4.
0	RES2OVF1EN	R/W	0h	Enable CHECK1 RES2OVF as a source for CHECKEVT4.

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3.3.2.30 ADC_SAFETY_AGGR_CHECKEVT4SEL3 Register

3.3.2.30.1 ADC_SAFETY_AGGR_CHECKEVT4SEL3 Register (Offset = 68h) [reset = 0h]

Checker X-Bar EVT4 Source Select Register 3

Return to Summary Table

Table 3-380. Instance Table

Instance Name	Physical Address
ADCSAFE_00	502C EC68h

Figure 3-186. ADC_SAFETY_AGGR_CHECKEVT4SEL3 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1				OOT12EN	OOT11EN	OOT10EN	OOT9EN
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
OOT8EN	OOT7EN	OOT6EN	OOT5EN	OOT4EN	OOT3EN	OOT2EN	OOT1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-381. ADC_SAFETY_AGGR_CHECKEVT4SEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_1	R	0h	Reserved
11	OOT12EN	R/W	0h	Enable CHECK12 OOT as a source for CHECKEVT4.
10	OOT11EN	R/W	0h	Enable CHECK11 OOTas a source for CHECKEVT4.
9	OOT10EN	R/W	0h	Enable CHECK10 OOT as a source for CHECKEVT4.
8	OOT9EN	R/W	0h	Enable CHECK9 OOT as a source for CHECKEVT4.
7	OOT8EN	R/W	0h	Enable CHECK8 OOT as a source for CHECKEVT4.
6	OOT7EN	R/W	0h	Enable CHECK7 OOTas a source for CHECKEVT4.
5	OOT6EN	R/W	0h	Enable CHECK6 OOT as a source for CHECKEVT4.
4	OOT5EN	R/W	0h	Enable CHECK5 OOT as a source for CHECKEVT4.
3	OOT4EN	R/W	0h	Enable CHECK4 OOT as a source for CHECKEVT4.
2	OOT3EN	R/W	0h	Enable CHECK3 OOTas a source for CHECKEVT4.
1	OOT2EN	R/W	0h	Enable CHECK2 OOT as a source for CHECKEVT4.
0	OOT1EN	R/W	0h	Enable CHECK1 OOT as a source for CHECKEVT4.

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3.4 DAC

DAC

3.4.1 DAC Summaries

DAC Summaries

Table 3-382. DAC Registers, Base Address=5026 0000h, Length=4096

Offset	Length	Register Name	DAC0 Physical Address
0h	16	DAC_DACREV	5026 0000h
2h	16	DAC_DACCTL_ALT2_	5026 0002h
4h	16	DAC_DACVALA	5026 0004h
6h	16	DAC_DACVALS	5026 0006h
8h	16	DAC_DACOUTEN	5026 0008h
Ah	16	DAC_DACLOCK	5026 000Ah
Eh	16	DAC_DACCONFIG	5026 000Eh

3.4.2 DAC Registers

DAC Registers

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3.4.2.1 DAC_DACREV Register

3.4.2.1.1 DAC_DACREV Register (Offset = 0h) [reset = 0h]

DAC Revision Register.

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Table 3-383. Instance Table

Instance Name	Physical Address
DAC0	5026 0000h

Figure 3-187. DAC_DACREV Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REV							
R							
0h							

Table 3-384. DAC_DACREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7:0	REV	R	0h	DAC Revision

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3.4.2.2 DAC_DACCTL_ALT2_ Register

3.4.2.2.1 DAC_DACCTL_ALT2_ Register (Offset = 2h) [reset = 0h]

DAC Control Register.

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Table 3-385. Instance Table

Instance Name	Physical Address
DAC0	5026 0002h

Figure 3-188. DAC_DACCTL_ALT2_ Name Register

15	14	13	12	11	10	9	8
RESERVED_2							SYNCSEL
R							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYNCSEL				RESERVED_1	LOADMODE	MODE	DACREFSEL
R/W				R	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 3-386. DAC_DACCTL_ALT2_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_2	R	0h	Reserved
8:4	SYNCSEL	R/W	0h	DAC EPWMSYNCPER select. Determines which EPWMSYNCPER signal will update the DACVALA register. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER
3	RESERVED_1	R	0h	Reserved
2	LOADMODE	R/W	0h	DACVALA load mode. Determines when the DACVALA register is updated with the value from DACVALS. 0 Load on next SYSCLK 1 Load on next EPWMSYNCPER specified by SYNCSEL
1	MODE	R/W	0h	DAC gain mode select. Selects the gain mode for the buffered output. The MODE value is only used when DACREFSEL=1 and internal ADC reference mode is selected. 0 Gain is 1 1 Gain is 2
0	DACREFSEL	R/W	0h	DAC reference select. Selects which voltage references are used by the DAC. 0 VDAC/VSSA are the reference voltages 1 ADC VREFHI/VSSA are the reference voltages

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3.4.2.3 DAC_DACVALA Register

3.4.2.3.1 DAC_DACVALA Register (Offset = 4h) [reset = 0h]

DAC Value Register - Active.

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Table 3-387. Instance Table

Instance Name	Physical Address
DAC0	5026 0004h

Figure 3-189. DAC_DACVALA Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED_1</td><td colspan="4">DACVALA</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DACVALA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 3-388. DAC_DACVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVALA	R	0h	Active output code currently driven by the DAC

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3.4.2.4 DAC_DACVALS Register

3.4.2.4.1 DAC_DACVALS Register (Offset = 6h) [reset = 0h]

DAC Value Register - Shadow.

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Table 3-389. Instance Table

Instance Name	Physical Address
DAC0	5026 0006h

Figure 3-190. DAC_DACVALS Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVALS			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DACVALS							
R/W							
0h							

Table 3-390. DAC_DACVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVALS	R/W	0h	Shadow output code to be loaded into DACVALA

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3.4.2.5 DAC_DACOUTEN Register

3.4.2.5.1 DAC_DACOUTEN Register (Offset = 8h) [reset = 0h]

DAC Output Enable Register.

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Table 3-391. Instance Table

Instance Name	Physical Address
DAC0	5026 0008h

Figure 3-191. DAC_DACOUTEN Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							DACOUTEN
R							R/W
0h							0h

Table 3-392. DAC_DACOUTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	DACOUTEN	R/W	0h	DAC output enable 0 DAC output is disabled 1 DAC output is enabled

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3.4.2.6 DAC_DACLOCK Register

3.4.2.6.1 DAC_DACLOCK Register (Offset = Ah) [reset = 0h]

DAC Lock Register.

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Table 3-393. Instance Table

Instance Name	Physical Address
DAC0	5026 000Ah

Figure 3-192. DAC_DACLOCK Name Register

15	14	13	12	11	10	9	8
KEY				RESERVED_1			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1					DACOUTEN	DACVAL	DACCTL
R					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 3-394. DAC_DACLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	KEY	R/W	0h	Writes to this register succeed only if this field is written with a value of 0xA. Only 16-bit writes will succeed [provided the KEY matches]. Read-modify-writes to individual bits in this register will be ignored.
11:3	RESERVED_1	R	0h	Reserved
2	DACOUTEN	R/W1TS	0h	Lock write-access to the DACOUTEN register. 0 DACOUTEN register is not locked. Write 0 to this bit has no effect. 1 DACOUTEN register is locked. Only a system reset can clear this bit.
1	DACVAL	R/W1TS	0h	Lock write-access to the DACVALS register. 0 DACVALS register is not locked. Write 0 to this bit has no effect. 1 DACVALS register is locked. Only a system reset can clear this bit.
0	DACCTL	R/W1TS	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit.

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3.4.2.7 DAC_DACCONFIG Register

3.4.2.7.1 DAC_DACCONFIG Register (Offset = Eh) [reset = 0h]

DAC Configuration Register.

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Table 3-395. Instance Table

Instance Name	Physical Address
DAC0	5026 000Eh

Figure 3-193. DAC_DACCONFIG Name Register

15	14	13	12	11	10	9	8
CONFIG							
R/W							
0h							
7	6	5	4	3	2	1	0
CONFIG							
R/W							
0h							

Table 3-396. DAC_DACCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CONFIG	R/W	0h	DAC Configuration. This bit field is used for TI internal testing/ debugging.

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3.5 CMPSSA

CMPSSA

3.5.1 CMPSSA Summaries

CMPSSA Summaries

Table 3-397. CMPSSA Registers, Base Address=5020 0000h, Length=4096

Offset	Length	Register Name	CMPSSA0 Physical Address	CMPSSA1 Physical Address	CMPSSA2 Physical Address
0h	16	CMPSSA_COMPCTL	5020 0000h	5020 1000h	5020 2000h
4h	16	CMPSSA_COMPSTS	5020 0004h	5020 1004h	5020 2004h
6h	16	CMPSSA_COMPSTSCLR	5020 0006h	5020 1006h	5020 2006h
8h	16	CMPSSA_COMPDACCTL	5020 0008h	5020 1008h	5020 2008h
Ah	16	CMPSSA_COMPDACCTL2	5020 000Ah	5020 100Ah	5020 200Ah
Ch	16	CMPSSA_DACHVALS	5020 000Ch	5020 100Ch	5020 200Ch
Eh	16	CMPSSA_DACHVALA	5020 000Eh	5020 100Eh	5020 200Eh
10h	16	CMPSSA_RAMPMAXREFA	5020 0010h	5020 1010h	5020 2010h
14h	16	CMPSSA_RAMPMAXREFS	5020 0014h	5020 1014h	5020 2014h
18h	16	CMPSSA_RAMPDECVALA	5020 0018h	5020 1018h	5020 2018h
1Ch	16	CMPSSA_RAMPDECVALS	5020 001Ch	5020 101Ch	5020 201Ch
20h	16	CMPSSA_RAMPSTS	5020 0020h	5020 1020h	5020 2020h
24h	16	CMPSSA_DACLVALS	5020 0024h	5020 1024h	5020 2024h
26h	16	CMPSSA_DACLVALA	5020 0026h	5020 1026h	5020 2026h
28h	16	CMPSSA_RAMPDLYA	5020 0028h	5020 1028h	5020 2028h
2Ah	16	CMPSSA_RAMPDLYS	5020 002Ah	5020 102Ah	5020 202Ah
2Ch	16	CMPSSA_CTRIPLFILCTL	5020 002Ch	5020 102Ch	5020 202Ch
2Eh	16	CMPSSA_CTRIPLFILCLKCTL	5020 002Eh	5020 102Eh	5020 202Eh
30h	16	CMPSSA_CTRIPHFILCTL	5020 0030h	5020 1030h	5020 2030h
32h	16	CMPSSA_CTRIPHFILCLKCTL	5020 0032h	5020 1032h	5020 2032h
34h	16	CMPSSA_COMPLOCK	5020 0034h	5020 1034h	5020 2034h
38h	16	CMPSSA_DACHVALS2	5020 0038h	5020 1038h	5020 2038h
3Ah	16	CMPSSA_DACLVALS2	5020 003Ah	5020 103Ah	5020 203Ah
3Ch	16	CMPSSA_CONFIG1	5020 003Ch	5020 103Ch	5020 203Ch

Table 3-398. CMPSSA Registers, Base Address=5020 0000h, Length=4096

Offset	Length	Register Name	CMPSSA3 Physical Address	CMPSSA4 Physical Address	CMPSSA5 Physical Address
0h	16	CMPSSA_COMPCTL	5020 3000h	5020 4000h	5020 5000h
4h	16	CMPSSA_COMPSTS	5020 3004h	5020 4004h	5020 5004h
6h	16	CMPSSA_COMPSTSCLR	5020 3006h	5020 4006h	5020 5006h
8h	16	CMPSSA_COMPDACCTL	5020 3008h	5020 4008h	5020 5008h
Ah	16	CMPSSA_COMPDACCTL2	5020 300Ah	5020 400Ah	5020 500Ah
Ch	16	CMPSSA_DACHVALS	5020 300Ch	5020 400Ch	5020 500Ch
Eh	16	CMPSSA_DACHVALA	5020 300Eh	5020 400Eh	5020 500Eh
10h	16	CMPSSA_RAMPMAXREFA	5020 3010h	5020 4010h	5020 5010h
14h	16	CMPSSA_RAMPMAXREFS	5020 3014h	5020 4014h	5020 5014h
18h	16	CMPSSA_RAMPDECVALA	5020 3018h	5020 4018h	5020 5018h
1Ch	16	CMPSSA_RAMPDECVALS	5020 301Ch	5020 401Ch	5020 501Ch

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Table 3-398. CMPSSA Registers, Base Address=5020 0000h, Length=4096 (continued)

Offset	Length	Register Name	CMPSSA3 Physical Address	CMPSSA4 Physical Address	CMPSSA5 Physical Address
20h	16	CMPSSA_RAMPSTS	5020 3020h	5020 4020h	5020 5020h
24h	16	CMPSSA_DACLVALS	5020 3024h	5020 4024h	5020 5024h
26h	16	CMPSSA_DACLVALA	5020 3026h	5020 4026h	5020 5026h
28h	16	CMPSSA_RAMPDLYA	5020 3028h	5020 4028h	5020 5028h
2Ah	16	CMPSSA_RAMPDLYS	5020 302Ah	5020 402Ah	5020 502Ah
2Ch	16	CMPSSA_CTRIPLFILCTL	5020 302Ch	5020 402Ch	5020 502Ch
2Eh	16	CMPSSA_CTRIPLFILCLKCTL	5020 302Eh	5020 402Eh	5020 502Eh
30h	16	CMPSSA_CTRIPHFILCTL	5020 3030h	5020 4030h	5020 5030h
32h	16	CMPSSA_CTRIPHFILCLKCTL	5020 3032h	5020 4032h	5020 5032h
34h	16	CMPSSA_COMPLOCK	5020 3034h	5020 4034h	5020 5034h
38h	16	CMPSSA_DACHVALS2	5020 3038h	5020 4038h	5020 5038h
3Ah	16	CMPSSA_DACLVALS2	5020 303Ah	5020 403Ah	5020 503Ah
3Ch	16	CMPSSA_CONFIG1	5020 303Ch	5020 403Ch	5020 503Ch

Table 3-399. CMPSSA Registers, Base Address=5020 0000h, Length=4096

Offset	Length	Register Name	CMPSSA6 Physical Address	CMPSSA7 Physical Address	CMPSSA8 Physical Address
0h	16	CMPSSA_COMPCTL	5020 6000h	5020 7000h	5020 8000h
4h	16	CMPSSA_COMPSTS	5020 6004h	5020 7004h	5020 8004h
6h	16	CMPSSA_COMPSTSCLR	5020 6006h	5020 7006h	5020 8006h
8h	16	CMPSSA_COMPDACCTL	5020 6008h	5020 7008h	5020 8008h
Ah	16	CMPSSA_COMPDACCTL2	5020 600Ah	5020 700Ah	5020 800Ah
Ch	16	CMPSSA_DACHVALS	5020 600Ch	5020 700Ch	5020 800Ch
Eh	16	CMPSSA_DACHVALA	5020 600Eh	5020 700Eh	5020 800Eh
10h	16	CMPSSA_RAMPMAXREFA	5020 6010h	5020 7010h	5020 8010h
14h	16	CMPSSA_RAMPMAXREFS	5020 6014h	5020 7014h	5020 8014h
18h	16	CMPSSA_RAMPDECVALA	5020 6018h	5020 7018h	5020 8018h
1Ch	16	CMPSSA_RAMPDECVALS	5020 601Ch	5020 701Ch	5020 801Ch
20h	16	CMPSSA_RAMPSTS	5020 6020h	5020 7020h	5020 8020h
24h	16	CMPSSA_DACLVALS	5020 6024h	5020 7024h	5020 8024h
26h	16	CMPSSA_DACLVALA	5020 6026h	5020 7026h	5020 8026h
28h	16	CMPSSA_RAMPDLYA	5020 6028h	5020 7028h	5020 8028h
2Ah	16	CMPSSA_RAMPDLYS	5020 602Ah	5020 702Ah	5020 802Ah
2Ch	16	CMPSSA_CTRIPLFILCTL	5020 602Ch	5020 702Ch	5020 802Ch
2Eh	16	CMPSSA_CTRIPLFILCLKCTL	5020 602Eh	5020 702Eh	5020 802Eh
30h	16	CMPSSA_CTRIPHFILCTL	5020 6030h	5020 7030h	5020 8030h
32h	16	CMPSSA_CTRIPHFILCLKCTL	5020 6032h	5020 7032h	5020 8032h
34h	16	CMPSSA_COMPLOCK	5020 6034h	5020 7034h	5020 8034h
38h	16	CMPSSA_DACHVALS2	5020 6038h	5020 7038h	5020 8038h
3Ah	16	CMPSSA_DACLVALS2	5020 603Ah	5020 703Ah	5020 803Ah
3Ch	16	CMPSSA_CONFIG1	5020 603Ch	5020 703Ch	5020 803Ch

Table 3-400. CMPSSA Registers, Base Address=5020 0000h, Length=4096

Offset	Length	Register Name	CMPSSA9 Physical Address
0h	16	CMPSSA_COMPCTL	5020 9000h

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Table 3-400. CMPSSA Registers, Base Address=5020 0000h, Length=4096 (continued)

Offset	Length	Register Name	CMPSSA9 Physical Address
4h	16	CMPSSA_COMPSTS	5020 9004h
6h	16	CMPSSA_COMPSTSCLR	5020 9006h
8h	16	CMPSSA_COMPDACCTL	5020 9008h
Ah	16	CMPSSA_COMPDACCTL2	5020 900Ah
Ch	16	CMPSSA_DACHVALS	5020 900Ch
Eh	16	CMPSSA_DACHVALA	5020 900Eh
10h	16	CMPSSA_RAMPMAXREFA	5020 9010h
14h	16	CMPSSA_RAMPMAXREFS	5020 9014h
18h	16	CMPSSA_RAMPDECVALA	5020 9018h
1Ch	16	CMPSSA_RAMPDECVALS	5020 901Ch
20h	16	CMPSSA_RAMPSTS	5020 9020h
24h	16	CMPSSA_DACLVALS	5020 9024h
26h	16	CMPSSA_DACLVALA	5020 9026h
28h	16	CMPSSA_RAMPDLYA	5020 9028h
2Ah	16	CMPSSA_RAMPDLYS	5020 902Ah
2Ch	16	CMPSSA_CTRIPLFILCTL	5020 902Ch
2Eh	16	CMPSSA_CTRIPLFILCLKCTL	5020 902Eh
30h	16	CMPSSA_CTRIPHFILCTL	5020 9030h
32h	16	CMPSSA_CTRIPHFILCLKCTL	5020 9032h
34h	16	CMPSSA_COMPLOCK	5020 9034h
38h	16	CMPSSA_DACHVALS2	5020 9038h
3Ah	16	CMPSSA_DACLVALS2	5020 903Ah
3Ch	16	CMPSSA_CONFIG1	5020 903Ch

3.5.2 CMPSSA Registers

CMPSSA Registers

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3.5.2.1 CMPSSA_COMPCTL Register

3.5.2.1.1 CMPSSA_COMPCTL Register (Offset = 0h) [reset = 0h]

CMPSS Comparator Control Register.

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Table 3-401. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0000h
CMPSSA1	5020 1000h
CMPSSA2	5020 2000h
CMPSSA3	5020 3000h
CMPSSA4	5020 4000h
CMPSSA5	5020 5000h
CMPSSA6	5020 6000h
CMPSSA7	5020 7000h
CMPSSA8	5020 8000h
CMPSSA9	5020 9000h

Figure 3-194. CMPSSA_COMPCTL Name Register

15	14	13	12	11	10	9	8
COMPDACE	ASYNCLEN	CTRIPOUTLSEL		CTRIPLSEL		COMPLINV	COMPLSOURCE
R/W	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	ASYNCHEN	CTRIPOUTHSEL		CTRIPHSEL		COMPHINV	COMPHSOURCE
R	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		0h		0h	0h

Table 3-402. CMPSSA_COMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	COMPDACE	R/W	0h	Comparator/DAC enable. 0 Comparator/DAC disabled 1 Comparator/DAC enabled
14	ASYNCLEN	R/W	0h	Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIPOUTLSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
13:12	CTRIPOUTLSEL	R/W	0h	Low comparator CTRIPOUTL source select. 0 Asynchronous comparator output drives CTRIPOUTL 1 Synchronous comparator output drives CTRIPOUTL 2 Output of digital filter drives CTRIPOUTL 3 Latched output of digital filter drives CTRIPOUTL
11:10	CTRIPLSEL	R/W	0h	Low comparator CTRIPL source select. 0 Asynchronous comparator output drives CTRIPL 1 Synchronous comparator output drives CTRIPL 2 Output of digital filter drives CTRIPL 3 Latched output of digital filter drives CTRIPL
9	COMPLINV	R/W	0h	Low comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted

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Table 3-402. CMPSSA_COMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	COMPLSOURCE	R/W	0h	CompL Pos Mux Select 0 positive mux selects INL_3p3v voltage [default] 1 postive mux selects INH_3p3v
7	RESERVED_1	R	0h	Reserved
6	ASYNCHEN	R/W	0h	High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
5:4	CTRIPOUTHSEL	R/W	0h	High comparator CTRIPOUTH source select. 0 Asynchronous comparator output drives CTRIPOUTH 1 Synchronous comparator output drives CTRIPOUTH 2 Output of digital filter drives CTRIPOUTH 3 Latched output of digital filter drives CTRIPOUTH
3:2	CTRIPHSEL	R/W	0h	High comparator CTRIPH source select. 0 Asynchronous comparator output drives CTRIPH 1 Synchronous comparator output drives CTRIPH 2 Output of digital filter drives CTRIPH 3 Latched output of digital filter drives CTRIPH
1	COMPHINV	R/W	0h	High comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
0	COMPHSOURCE	R/W	0h	CompH neg Mux slect 0 negative mux selects DAC voltage [default] 1 negative mux selects INL_3p3v

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3.5.2.2 CMPSSA_COMPSTS Register

3.5.2.2.1 CMPSSA_COMPSTS Register (Offset = 4h) [reset = 0h]

CMPSS Comparator Status Register.

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Table 3-403. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0004h
CMPSSA1	5020 1004h
CMPSSA2	5020 2004h
CMPSSA3	5020 3004h
CMPSSA4	5020 4004h
CMPSSA5	5020 5004h
CMPSSA6	5020 6004h
CMPSSA7	5020 7004h
CMPSSA8	5020 8004h
CMPSSA9	5020 9004h

Figure 3-195. CMPSSA_COMPSTS Name Register

15	14	13	12	11	10	9	8
RESERVED_2						COMPLLATCH	COMPLSTS
R						R	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						COMPHLATCH	COMPHSTS
R						R	R
0h						0h	0h

Table 3-404. CMPSSA_COMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_2	R	0h	Reserved
9	COMPLLATCH	R	0h	Latched value of low comparator digital filter output
8	COMPLSTS	R	0h	Low comparator digital filter output
7:2	RESERVED_1	R	0h	Reserved
1	COMPHLATCH	R	0h	Latched value of high comparator digital filter output
0	COMPHSTS	R	0h	High comparator digital filter output

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3.5.2.3 CMPSSA_COMPSTSCLR Register

3.5.2.3.1 CMPSSA_COMPSTSCLR Register (Offset = 6h) [reset = 0h]

CMPSS Comparator Status Clear Register.

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Table 3-405. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0006h
CMPSSA1	5020 1006h
CMPSSA2	5020 2006h
CMPSSA3	5020 3006h
CMPSSA4	5020 4006h
CMPSSA5	5020 5006h
CMPSSA6	5020 6006h
CMPSSA7	5020 7006h
CMPSSA8	5020 8006h
CMPSSA9	5020 9006h

Figure 3-196. CMPSSA_COMPSTSCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_3					LSYNCCLREN	LLATCHCLR	RESERVED_2
R					R/W	R/W1TS	R
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2					HSYNCCLREN	HLATCHCLR	RESERVED_1
R					R/W	R/W1TS	R
0h					0h	0h	0h

Table 3-406. CMPSSA_COMPSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_3	R	0h	Reserved
10	LSYNCCLREN	R/W	0h	Low comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
9	LLATCHCLR	R/W1TS	0h	Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH]
8:3	RESERVED_2	R	0h	Reserved
2	HSYNCCLREN	R/W	0h	High comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
1	HLATCHCLR	R/W1TS	0h	High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH]

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Table 3-406. CMPSSA_COMPSTSCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED_1	R	0h	Reserved

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3.5.2.4 CMPSSA_COMPDACCTL Register

3.5.2.4.1 CMPSSA_COMPDACCTL Register (Offset = 8h) [reset = 0h]

CMPSS DAC Control Register.

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Table 3-407. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0008h
CMPSSA1	5020 1008h
CMPSSA2	5020 2008h
CMPSSA3	5020 3008h
CMPSSA4	5020 4008h
CMPSSA5	5020 5008h
CMPSSA6	5020 6008h
CMPSSA7	5020 7008h
CMPSSA8	5020 8008h
CMPSSA9	5020 9008h

Figure 3-197. CMPSSA_COMPDACCTL Name Register

15	14	13	12	11	10	9	8
FREESOFT		RESERVED_1	BLANKEN	BLANKSOURCE			
R/W		R	R/W	R/W			
0h		0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SWLOADSEL	RAMPLOADSEL	SELREF	RAMPSOURCE				DACSOURCE
R/W	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Table 3-408. CMPSSA_COMPDACCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREESOFT	R/W	0h	Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend. 00b Ramp generator stops immediately during emulation suspend 01b Ramp generator completes current ramp and stops at next EPWMSYNCPER during emulation suspend 1Xb Ramp generator runs freely
13	RESERVED_1	R	0h	Reserved
12	BLANKEN	R/W	0h	EPWMBLANK enable. This bit enables the EPWMBLANK signal. 0 EPWMBLANK signal is disabled. 1 EPWMBLANK signal is enabled.
11:8	BLANKSOURCE	R/W	0h	EPWMBLANK source select. This bit field determines which EPWMnBLANK is passed on as the EPWMBLANK signal. Where n represents the maximum number of EPWMBLANK signals available on the device: 0 EPWM0BLANK 1 EPWM1BLANK 2 EPWM2BLANK ... n-1 EPWM(n-1)BLANK
7	SWLOADSEL	R/W	0h	Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or EPWMSYNCPER. 0 DACxVALA is updated from DACxVALS on SYSCLK 1 DACxVALA is updated from DACxVALS on EPWMSYNCPER

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Table 3-408. CMPSSA_COMPDACCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RAMPLOADSEL	R/W	0h	Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered. 0 RAMPSTS is loaded from RAMPMAXREFA 1 RAMPSTS is loaded from RAMPMAXREFS
5	SELREF	R/W	0h	CMPSS reference select 0 vref_1p8v as reference voltage [default] 1 vdd_1p8v as reference voltage
4:1	RAMPSOURCE	R/W	0h	EPWMSYNCPER source select. Determines which EPWMnSYNCPER signal is used within the CMPSS module. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER
0	DACSOURCE	R/W	0h	DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator. 0 DACHVALA is updated from DACHVALS 1 DACHVALA is updated from the ramp generator

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3.5.2.5 CMPSSA_COMPDACCTL2 Register

3.5.2.5.1 CMPSSA_COMPDACCTL2 Register (Offset = Ah) [reset = 0h]

CMPSS DAC Control Register 2

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Table 3-409. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 000Ah
CMPSSA1	5020 100Ah
CMPSSA2	5020 200Ah
CMPSSA3	5020 300Ah
CMPSSA4	5020 400Ah
CMPSSA5	5020 500Ah
CMPSSA6	5020 600Ah
CMPSSA7	5020 700Ah
CMPSSA8	5020 800Ah
CMPSSA9	5020 900Ah

Figure 3-198. CMPSSA_COMPDACCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_3					RAMPSOURCEUSEL	RESERVED_2	BLANKSOURCEUSEL
R					R/W	R	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1		DEACTIVESEL					DEENABLE
R		R/W					R/W
0h		0h					0h

Table 3-410. CMPSSA_COMPDACCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_3	R	0h	Reserved
10	RAMPSOURCEUSEL	R/W	0h	0: Selects EPWM0 to 15 as RAMP source 1:Selects EPWM16 to 31 as RAMP source
9	RESERVED_2	R	0h	Reserved
8	BLANKSOURCEUSEL	R/W	0h	0: Selects EPWM0 to 15 as blank source 1:Selects EPWM16 to 31 as blank source
7:6	RESERVED_1	R	0h	Reserved
5:1	DEACTIVESEL	R/W	0h	DEACTIVE source select: 0 : EPWM0.DEACTIVE 1 : EPWM1.DEACTIVE 2 : EPWM2.DEACTIVE 3 : EPWM3.DEACTIVE . . 31 : EPWM31.DEACTIVE
0	DEENABLE	R/W	0h	DE mode enable. 0 DE mode features disabled. 1 DE mode features enabled.

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3.5.2.6 CMPSSA_DACHVALS Register

3.5.2.6.1 CMPSSA_DACHVALS Register (Offset = Ch) [reset = 0h]

CMPSS High DAC Value Shadow Register.

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Table 3-411. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 000Ch
CMPSSA1	5020 100Ch
CMPSSA2	5020 200Ch
CMPSSA3	5020 300Ch
CMPSSA4	5020 400Ch
CMPSSA5	5020 500Ch
CMPSSA6	5020 600Ch
CMPSSA7	5020 700Ch
CMPSSA8	5020 800Ch
CMPSSA9	5020 900Ch

Figure 3-199. CMPSSA_DACHVALS Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACVAL							
R/W							
0h							

Table 3-412. CMPSSA_DACHVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R/W	0h	High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

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3.5.2.7 CMPSSA_DACHVALA Register

3.5.2.7.1 CMPSSA_DACHVALA Register (Offset = Eh) [reset = 0h]

CMPSS High DAC Value Active Register.

Return to Summary Table

Table 3-413. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 000Eh
CMPSSA1	5020 100Eh
CMPSSA2	5020 200Eh
CMPSSA3	5020 300Eh
CMPSSA4	5020 400Eh
CMPSSA5	5020 500Eh
CMPSSA6	5020 600Eh
CMPSSA7	5020 700Eh
CMPSSA8	5020 800Eh
CMPSSA9	5020 900Eh

Figure 3-200. CMPSSA_DACHVALA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R			
0h				0h			

7	6	5	4	3	2	1	0
DACVAL							
R							
0h							

Table 3-414. CMPSSA_DACHVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R	0h	High DAC active value. Value that is actively driven by the high DAC.

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3.5.2.8 CMPSSA_RAMPMAXREFA Register

3.5.2.8.1 CMPSSA_RAMPMAXREFA Register (Offset = 10h) [reset = 0h]

CMPSS Ramp Max Reference Active Register.

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Table 3-415. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0010h
CMPSSA1	5020 1010h
CMPSSA2	5020 2010h
CMPSSA3	5020 3010h
CMPSSA4	5020 4010h
CMPSSA5	5020 5010h
CMPSSA6	5020 6010h
CMPSSA7	5020 7010h
CMPSSA8	5020 8010h
CMPSSA9	5020 9010h

Figure 3-201. CMPSSA_RAMPMAXREFA Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMPMAXREF							
R							
0h							

Table 3-416. CMPSSA_RAMPMAXREFA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPMAXREF	R	0h	Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS.

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3.5.2.9 CMPSSA_RAMPMAXREFS Register

3.5.2.9.1 CMPSSA_RAMPMAXREFS Register (Offset = 14h) [reset = 0h]

CMPSS Ramp Max Reference Shadow Register.

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Table 3-417. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0014h
CMPSSA1	5020 1014h
CMPSSA2	5020 2014h
CMPSSA3	5020 3014h
CMPSSA4	5020 4014h
CMPSSA5	5020 5014h
CMPSSA6	5020 6014h
CMPSSA7	5020 7014h
CMPSSA8	5020 8014h
CMPSSA9	5020 9014h

Figure 3-202. CMPSSA_RAMPMAXREFS Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMPMAXREF							
R/W							
0h							

Table 3-418. CMPSSA_RAMPMAXREFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPMAXREF	R/W	0h	Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS.

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3.5.2.10 CMPSSA_RAMPDECVALA Register

3.5.2.10.1 CMPSSA_RAMPDECVALA Register (Offset = 18h) [reset = 0h]

CMPSS Ramp Decrement Value Active Register.

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Table 3-419. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0018h
CMPSSA1	5020 1018h
CMPSSA2	5020 2018h
CMPSSA3	5020 3018h
CMPSSA4	5020 4018h
CMPSSA5	5020 5018h
CMPSSA6	5020 6018h
CMPSSA7	5020 7018h
CMPSSA8	5020 8018h
CMPSSA9	5020 9018h

Figure 3-203. CMPSSA_RAMPDECVALA Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMPDECVAL							
R							
0h							

Table 3-420. CMPSSA_RAMPDECVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPDECVAL	R	0h	Ramp decrement value active. Latched value that will be subtracted from RAMPSTS.

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3.5.2.11 CMPSSA_RAMPDECVALS Register

3.5.2.11.1 CMPSSA_RAMPDECVALS Register (Offset = 1Ch) [reset = 0h]

CMPSS Ramp Decrement Value Shadow Register.

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Table 3-421. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 001Ch
CMPSSA1	5020 101Ch
CMPSSA2	5020 201Ch
CMPSSA3	5020 301Ch
CMPSSA4	5020 401Ch
CMPSSA5	5020 501Ch
CMPSSA6	5020 601Ch
CMPSSA7	5020 701Ch
CMPSSA8	5020 801Ch
CMPSSA9	5020 901Ch

Figure 3-204. CMPSSA_RAMPDECVALS Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMPDECVAL							
R/W							
0h							

Table 3-422. CMPSSA_RAMPDECVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPDECVAL	R/W	0h	Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA.

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3.5.2.12 CMPSSA_RAMPSTS Register

3.5.2.12.1 CMPSSA_RAMPSTS Register (Offset = 20h) [reset = 0h]

CMPSS Ramp Status Register.

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Table 3-423. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0020h
CMPSSA1	5020 1020h
CMPSSA2	5020 2020h
CMPSSA3	5020 3020h
CMPSSA4	5020 4020h
CMPSSA5	5020 5020h
CMPSSA6	5020 6020h
CMPSSA7	5020 7020h
CMPSSA8	5020 8020h
CMPSSA9	5020 9020h

Figure 3-205. CMPSSA_RAMPSTS Name Register

15	14	13	12	11	10	9	8
RAMPVALUE							
R							
0h							
7	6	5	4	3	2	1	0
RAMPVALUE							
R							
0h							

Table 3-424. CMPSSA_RAMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPVALUE	R	0h	Ramp value. Present value of ramp generator.

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3.5.2.13 CMPSSA_DACLVALS Register

3.5.2.13.1 CMPSSA_DACLVALS Register (Offset = 24h) [reset = 0h]

CMPSS Low DAC Value Shadow Register.

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Table 3-425. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0024h
CMPSSA1	5020 1024h
CMPSSA2	5020 2024h
CMPSSA3	5020 3024h
CMPSSA4	5020 4024h
CMPSSA5	5020 5024h
CMPSSA6	5020 6024h
CMPSSA7	5020 7024h
CMPSSA8	5020 8024h
CMPSSA9	5020 9024h

Figure 3-206. CMPSSA_DACLVALS Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACVAL							
R/W							
0h							

Table 3-426. CMPSSA_DACLVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R/W	0h	Low DAC shadow value. value to be loaded into DACLVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

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3.5.2.14 CMPSSA_DACLVALA Register

3.5.2.14.1 CMPSSA_DACLVALA Register (Offset = 26h) [reset = 0h]

CMPSS Low DAC Value Active Register.

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Table 3-427. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0026h
CMPSSA1	5020 1026h
CMPSSA2	5020 2026h
CMPSSA3	5020 3026h
CMPSSA4	5020 4026h
CMPSSA5	5020 5026h
CMPSSA6	5020 6026h
CMPSSA7	5020 7026h
CMPSSA8	5020 8026h
CMPSSA9	5020 9026h

Figure 3-207. CMPSSA_DACLVALA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R							
0h							

Table 3-428. CMPSSA_DACLVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R	0h	Low DAC active value. Value that is actively driven by the low DAC.

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3.5.2.15 CMPSSA_RAMPDLYA Register

3.5.2.15.1 CMPSSA_RAMPDLYA Register (Offset = 28h) [reset = 0h]

CMPSS Ramp Delay Active Register.

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Table 3-429. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0028h
CMPSSA1	5020 1028h
CMPSSA2	5020 2028h
CMPSSA3	5020 3028h
CMPSSA4	5020 4028h
CMPSSA5	5020 5028h
CMPSSA6	5020 6028h
CMPSSA7	5020 7028h
CMPSSA8	5020 8028h
CMPSSA9	5020 9028h

Figure 3-208. CMPSSA_RAMPDLYA Name Register

15	14	13	12	11	10	9	8
RESERVED_1			DELAY				
R			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DELAY							
R							
0h							

Table 3-430. CMPSSA_RAMPDLYA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12:0	DELAY	R	0h	Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a EPWMSYNCPER is received.

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3.5.2.16 CMPSSA_RAMPDLYS Register

3.5.2.16.1 CMPSSA_RAMPDLYS Register (Offset = 2Ah) [reset = 0h]

CMPSS Ramp Delay Shadow Register.

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Table 3-431. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 002Ah
CMPSSA1	5020 102Ah
CMPSSA2	5020 202Ah
CMPSSA3	5020 302Ah
CMPSSA4	5020 402Ah
CMPSSA5	5020 502Ah
CMPSSA6	5020 602Ah
CMPSSA7	5020 702Ah
CMPSSA8	5020 802Ah
CMPSSA9	5020 902Ah

Figure 3-209. CMPSSA_RAMPDLYS Name Register

15	14	13	12	11	10	9	8
RESERVED_1			DELAY				
R			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DELAY							
R/W							
0h							

Table 3-432. CMPSSA_RAMPDLYS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12:0	DELAY	R/W	0h	Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA.

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3.5.2.17 CMPSSA_CTRIPLFILCTL Register

3.5.2.17.1 CMPSSA_CTRIPLFILCTL Register (Offset = 2Ch) [reset = 0h]

CTRIPL Filter Control Register.

Return to Summary Table

Table 3-433. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 002Ch
CMPSSA1	5020 102Ch
CMPSSA2	5020 202Ch
CMPSSA3	5020 302Ch
CMPSSA4	5020 402Ch
CMPSSA5	5020 502Ch
CMPSSA6	5020 602Ch
CMPSSA7	5020 702Ch
CMPSSA8	5020 802Ch
CMPSSA9	5020 902Ch

Figure 3-210. CMPSSA_CTRIPLFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h

7	6	5	4	3	2	1	0
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-434. CMPSSA_CTRIPLFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.5.2.18 CMPSSA_CTRIPLFILCLKCTL Register

3.5.2.18.1 CMPSSA_CTRIPLFILCLKCTL Register (Offset = 2Eh) [reset = 0h]

CTRIPL Filter Clock Control Register.

Return to Summary Table

Table 3-435. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 002Eh
CMPSSA1	5020 102Eh
CMPSSA2	5020 202Eh
CMPSSA3	5020 302Eh
CMPSSA4	5020 402Eh
CMPSSA5	5020 502Eh
CMPSSA6	5020 602Eh
CMPSSA7	5020 702Eh
CMPSSA8	5020 802Eh
CMPSSA9	5020 902Eh

Figure 3-211. CMPSSA_CTRIPLFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKPRESCALE							
R/W							
0h							

Table 3-436. CMPSSA_CTRIPLFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

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3.5.2.19 CMPSSA_CTRIPHFILCTL Register

3.5.2.19.1 CMPSSA_CTRIPHFILCTL Register (Offset = 30h) [reset = 0h]

CTRIPH Filter Control Register.

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Table 3-437. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0030h
CMPSSA1	5020 1030h
CMPSSA2	5020 2030h
CMPSSA3	5020 3030h
CMPSSA4	5020 4030h
CMPSSA5	5020 5030h
CMPSSA6	5020 6030h
CMPSSA7	5020 7030h
CMPSSA8	5020 8030h
CMPSSA9	5020 9030h

Figure 3-212. CMPSSA_CTRIPHFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-438. CMPSSA_CTRIPHFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.5.2.20 CMPSSA_CTRIPHFILCLKCTL Register

3.5.2.20.1 CMPSSA_CTRIPHFILCLKCTL Register (Offset = 32h) [reset = 0h]

CTRIPH Filter Clock Control Register.

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Table 3-439. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0032h
CMPSSA1	5020 1032h
CMPSSA2	5020 2032h
CMPSSA3	5020 3032h
CMPSSA4	5020 4032h
CMPSSA5	5020 5032h
CMPSSA6	5020 6032h
CMPSSA7	5020 7032h
CMPSSA8	5020 8032h
CMPSSA9	5020 9032h

Figure 3-213. CMPSSA_CTRIPHFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
R/W							
0h							
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Table 3-440. CMPSSA_CTRIPHFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

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3.5.2.21 CMPSSA_COMPLOCK Register

3.5.2.21.1 CMPSSA_COMPLOCK Register (Offset = 34h) [reset = 0h]

CMPSS Lock Register.

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Table 3-441. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0034h
CMPSSA1	5020 1034h
CMPSSA2	5020 2034h
CMPSSA3	5020 3034h
CMPSSA4	5020 4034h
CMPSSA5	5020 5034h
CMPSSA6	5020 6034h
CMPSSA7	5020 7034h
CMPSSA8	5020 8034h
CMPSSA9	5020 9034h

Figure 3-214. CMPSSA_COMPLOCK Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED_1</td><td>TEST</td><td>CTRIP</td><td>DACCTL</td><td>COMPHYSCTL</td><td>COMPCTL</td></tr>
<tr><td colspan="3">R</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 3-442. CMPSSA_COMPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_1	R	0h	Reserved
4	TEST	R/W1TS	0h	TEST Lock. This bit, when set, will prevent any further writes to the any undocumented registers that may effect the performance/ behavior of this block. Once set this bit can only be cleared by a reset.
3	CTRIP	R/W1TS	0h	Lock write-access to the CTRIPxFILTCTL and CTRIPxFILCLKCTL registers. 0 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are locked. Only a system reset can clear this bit.
2	DACCTL	R/W1TS	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit.
1	COMPHYSCTL	R/W1TS	0h	Lock write-access to the COMPHYSCTL register. 0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect. 1 COMPHYSCTL register is locked. Only a system reset can clear this bit.
0	COMPCTL	R/W1TS	0h	Lock write-access to the COMPCTL register. 0 COMPCTL register is not locked. Write 0 to this bit has no effect. 1 COMPCTL register is locked. Only a system reset can clear this bit.

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3.5.2.22 CMPSSA_DACHVALS2 Register

3.5.2.22.1 CMPSSA_DACHVALS2 Register (Offset = 38h) [reset = 0h]

CMPSS High DAC Value Shadow Register 2

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Table 3-443. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 0038h
CMPSSA1	5020 1038h
CMPSSA2	5020 2038h
CMPSSA3	5020 3038h
CMPSSA4	5020 4038h
CMPSSA5	5020 5038h
CMPSSA6	5020 6038h
CMPSSA7	5020 7038h
CMPSSA8	5020 8038h
CMPSSA9	5020 9038h

Figure 3-215. CMPSSA_DACHVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			

7	6	5	4	3	2	1	0
DACVAL							
R/W							
0h							

Table 3-444. CMPSSA_DACHVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R/W	0h	High DAC shadow register2 value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

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3.5.2.23 CMPSSA_DACLVALS2 Register

3.5.2.23.1 CMPSSA_DACLVALS2 Register (Offset = 3Ah) [reset = 0h]

CMPSS Low DAC Value Shadow Register 2

Return to Summary Table

Table 3-445. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 003Ah
CMPSSA1	5020 103Ah
CMPSSA2	5020 203Ah
CMPSSA3	5020 303Ah
CMPSSA4	5020 403Ah
CMPSSA5	5020 503Ah
CMPSSA6	5020 603Ah
CMPSSA7	5020 703Ah
CMPSSA8	5020 803Ah
CMPSSA9	5020 903Ah

Figure 3-216. CMPSSA_DACLVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACVAL							
R/W							
0h							

Table 3-446. CMPSSA_DACLVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R/W	0h	Low DAC shadow register2 value. Value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

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3.5.2.24 CMPSSA_CONFIG1 Register

3.5.2.24.1 CMPSSA_CONFIG1 Register (Offset = 3Ch) [reset = 0h]

CMPSS Config1 Register.

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Table 3-447. Instance Table

Instance Name	Physical Address
CMPSSA0	5020 003Ch
CMPSSA1	5020 103Ch
CMPSSA2	5020 203Ch
CMPSSA3	5020 303Ch
CMPSSA4	5020 403Ch
CMPSSA5	5020 503Ch
CMPSSA6	5020 603Ch
CMPSSA7	5020 703Ch
CMPSSA8	5020 803Ch
CMPSSA9	5020 903Ch

Figure 3-217. CMPSSA_CONFIG1 Name Register

15	14	13	12	11	10	9	8
SPARE							
R/W							
0h							
7	6	5	4	3	2	1	0
COMPLHYS				COMPHHYS			
R/W				R/W			
0h				0h			

Table 3-448. CMPSSA_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	SPARE	R/W	0h	SPARE
7:4	COMPLHYS	R/W	0h	CompL Hysteresis COMPLHYS[3] : reserved COMPLHYS[2] : Controls which comparator output value hysteresis is applied to. 1'b0 : Hysteresis is applied when the comparator output is 1'b1 1'b1 : Hysteresis is applied when the comparator output is 1'b0 COMPLHYS[1:0] = hysteresis value 2'b00 : 0 LSB 2'b01 : 17.5 LSB 2'b10 : 35 LSB 2'b11 : 52.5 LSB
3:0	COMPHHYS	R/W	0h	CompH Hysteresis COMPHHYS[3] : reserved COMPHHYS[2] : Controls which comparator output value hysteresis is applied to. 1'b0 : Hysteresis is applied when the comparator output is 1'b1 1'b1 : Hysteresis is applied when the comparator output is 1'b0 COMPHHYS[1:0] = hysteresis value 2'b00 : 0 LSB 2'b01 : 17.5 LSB 2'b10 : 35 LSB 2'b11 : 52.5 LSB

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3.6 CMPSSB

CMPSSB

3.6.1 CMPSSB Summaries

CMPSSB Summaries

Table 3-449. CMPSSB Registers, Base Address=5022 0000h, Length=4096

Offset	Length	Register Name	CMPSSB0 Physical Address	CMPSSB1 Physical Address	CMPSSB2 Physical Address
0h	16	CMPSSB_COMPCTL	5022 0000h	5022 1000h	5022 2000h
4h	16	CMPSSB_COMPSTS	5022 0004h	5022 1004h	5022 2004h
6h	16	CMPSSB_COMPSTSCLR	5022 0006h	5022 1006h	5022 2006h
8h	16	CMPSSB_COMPDACCTL	5022 0008h	5022 1008h	5022 2008h
Ah	16	CMPSSB_COMPDACCTL2	5022 000Ah	5022 100Ah	5022 200Ah
Ch	16	CMPSSB_DACHVALS	5022 000Ch	5022 100Ch	5022 200Ch
Eh	16	CMPSSB_DACHVALA	5022 000Eh	5022 100Eh	5022 200Eh
10h	16	CMPSSB_RAMPMAXREFA	5022 0010h	5022 1010h	5022 2010h
14h	16	CMPSSB_RAMPMAXREFS	5022 0014h	5022 1014h	5022 2014h
18h	16	CMPSSB_RAMPDECVALA	5022 0018h	5022 1018h	5022 2018h
1Ch	16	CMPSSB_RAMPDECVALS	5022 001Ch	5022 101Ch	5022 201Ch
20h	16	CMPSSB_RAMPSTS	5022 0020h	5022 1020h	5022 2020h
24h	16	CMPSSB_DACLVALS	5022 0024h	5022 1024h	5022 2024h
26h	16	CMPSSB_DACLVALA	5022 0026h	5022 1026h	5022 2026h
28h	16	CMPSSB_RAMPDLYA	5022 0028h	5022 1028h	5022 2028h
2Ah	16	CMPSSB_RAMPDLYS	5022 002Ah	5022 102Ah	5022 202Ah
2Ch	16	CMPSSB_CTRIPLFILCTL	5022 002Ch	5022 102Ch	5022 202Ch
2Eh	16	CMPSSB_CTRIPLFILCLKCTL	5022 002Eh	5022 102Eh	5022 202Eh
30h	16	CMPSSB_CTRIPHFILCTL	5022 0030h	5022 1030h	5022 2030h
32h	16	CMPSSB_CTRIPHFILCLKCTL	5022 0032h	5022 1032h	5022 2032h
34h	16	CMPSSB_COMPLOCK	5022 0034h	5022 1034h	5022 2034h
38h	16	CMPSSB_DACHVALS2	5022 0038h	5022 1038h	5022 2038h
3Ah	16	CMPSSB_DACLVALS2	5022 003Ah	5022 103Ah	5022 203Ah
3Ch	16	CMPSSB_CONFIG1	5022 003Ch	5022 103Ch	5022 203Ch

Table 3-450. CMPSSB Registers, Base Address=5022 0000h, Length=4096

Offset	Length	Register Name	CMPSSB3 Physical Address	CMPSSB4 Physical Address	CMPSSB5 Physical Address
0h	16	CMPSSB_COMPCTL	5022 3000h	5022 4000h	5022 5000h
4h	16	CMPSSB_COMPSTS	5022 3004h	5022 4004h	5022 5004h
6h	16	CMPSSB_COMPSTSCLR	5022 3006h	5022 4006h	5022 5006h
8h	16	CMPSSB_COMPDACCTL	5022 3008h	5022 4008h	5022 5008h
Ah	16	CMPSSB_COMPDACCTL2	5022 300Ah	5022 400Ah	5022 500Ah
Ch	16	CMPSSB_DACHVALS	5022 300Ch	5022 400Ch	5022 500Ch
Eh	16	CMPSSB_DACHVALA	5022 300Eh	5022 400Eh	5022 500Eh
10h	16	CMPSSB_RAMPMAXREFA	5022 3010h	5022 4010h	5022 5010h
14h	16	CMPSSB_RAMPMAXREFS	5022 3014h	5022 4014h	5022 5014h
18h	16	CMPSSB_RAMPDECVALA	5022 3018h	5022 4018h	5022 5018h
1Ch	16	CMPSSB_RAMPDECVALS	5022 301Ch	5022 401Ch	5022 501Ch

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Table 3-450. CMPSSB Registers, Base Address=5022 0000h, Length=4096 (continued)

Offset	Length	Register Name	CMPSSB3 Physical Address	CMPSSB4 Physical Address	CMPSSB5 Physical Address
20h	16	CMPSSB_RAMPSTS	5022 3020h	5022 4020h	5022 5020h
24h	16	CMPSSB_DACLVALS	5022 3024h	5022 4024h	5022 5024h
26h	16	CMPSSB_DACLVALA	5022 3026h	5022 4026h	5022 5026h
28h	16	CMPSSB_RAMPDLYA	5022 3028h	5022 4028h	5022 5028h
2Ah	16	CMPSSB_RAMPDLYS	5022 302Ah	5022 402Ah	5022 502Ah
2Ch	16	CMPSSB_CTRIPLFILCTL	5022 302Ch	5022 402Ch	5022 502Ch
2Eh	16	CMPSSB_CTRIPLFILCLKCTL	5022 302Eh	5022 402Eh	5022 502Eh
30h	16	CMPSSB_CTRIPHFILCTL	5022 3030h	5022 4030h	5022 5030h
32h	16	CMPSSB_CTRIPHFILCLKCTL	5022 3032h	5022 4032h	5022 5032h
34h	16	CMPSSB_COMPLOCK	5022 3034h	5022 4034h	5022 5034h
38h	16	CMPSSB_DACHVALS2	5022 3038h	5022 4038h	5022 5038h
3Ah	16	CMPSSB_DACLVALS2	5022 303Ah	5022 403Ah	5022 503Ah
3Ch	16	CMPSSB_CONFIG1	5022 303Ch	5022 403Ch	5022 503Ch

Table 3-451. CMPSSB Registers, Base Address=5022 0000h, Length=4096

Offset	Length	Register Name	CMPSSB6 Physical Address	CMPSSB7 Physical Address	CMPSSB8 Physical Address
0h	16	CMPSSB_COMPCTL	5022 6000h	5022 7000h	5022 8000h
4h	16	CMPSSB_COMPSTS	5022 6004h	5022 7004h	5022 8004h
6h	16	CMPSSB_COMPSTSCLR	5022 6006h	5022 7006h	5022 8006h
8h	16	CMPSSB_COMPDACCTL	5022 6008h	5022 7008h	5022 8008h
Ah	16	CMPSSB_COMPDACCTL2	5022 600Ah	5022 700Ah	5022 800Ah
Ch	16	CMPSSB_DACHVALS	5022 600Ch	5022 700Ch	5022 800Ch
Eh	16	CMPSSB_DACHVALA	5022 600Eh	5022 700Eh	5022 800Eh
10h	16	CMPSSB_RAMPMAXREFA	5022 6010h	5022 7010h	5022 8010h
14h	16	CMPSSB_RAMPMAXREFS	5022 6014h	5022 7014h	5022 8014h
18h	16	CMPSSB_RAMPDECVALA	5022 6018h	5022 7018h	5022 8018h
1Ch	16	CMPSSB_RAMPDECVALS	5022 601Ch	5022 701Ch	5022 801Ch
20h	16	CMPSSB_RAMPSTS	5022 6020h	5022 7020h	5022 8020h
24h	16	CMPSSB_DACLVALS	5022 6024h	5022 7024h	5022 8024h
26h	16	CMPSSB_DACLVALA	5022 6026h	5022 7026h	5022 8026h
28h	16	CMPSSB_RAMPDLYA	5022 6028h	5022 7028h	5022 8028h
2Ah	16	CMPSSB_RAMPDLYS	5022 602Ah	5022 702Ah	5022 802Ah
2Ch	16	CMPSSB_CTRIPLFILCTL	5022 602Ch	5022 702Ch	5022 802Ch
2Eh	16	CMPSSB_CTRIPLFILCLKCTL	5022 602Eh	5022 702Eh	5022 802Eh
30h	16	CMPSSB_CTRIPHFILCTL	5022 6030h	5022 7030h	5022 8030h
32h	16	CMPSSB_CTRIPHFILCLKCTL	5022 6032h	5022 7032h	5022 8032h
34h	16	CMPSSB_COMPLOCK	5022 6034h	5022 7034h	5022 8034h
38h	16	CMPSSB_DACHVALS2	5022 6038h	5022 7038h	5022 8038h
3Ah	16	CMPSSB_DACLVALS2	5022 603Ah	5022 703Ah	5022 803Ah
3Ch	16	CMPSSB_CONFIG1	5022 603Ch	5022 703Ch	5022 803Ch

Table 3-452. CMPSSB Registers, Base Address=5022 0000h, Length=4096

Offset	Length	Register Name	CMPSSB9 Physical Address
0h	16	CMPSSB_COMPCTL	5022 9000h

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Table 3-452. CMPSSB Registers, Base Address=5022 0000h, Length=4096 (continued)

Offset	Length	Register Name	CMPSSB9 Physical Address
4h	16	CMPSSB_COMPSTS	5022 9004h
6h	16	CMPSSB_COMPSTSCLR	5022 9006h
8h	16	CMPSSB_COMPDACCTL	5022 9008h
Ah	16	CMPSSB_COMPDACCTL2	5022 900Ah
Ch	16	CMPSSB_DACHVALS	5022 900Ch
Eh	16	CMPSSB_DACHVALA	5022 900Eh
10h	16	CMPSSB_RAMPMAXREFA	5022 9010h
14h	16	CMPSSB_RAMPMAXREFS	5022 9014h
18h	16	CMPSSB_RAMPDECVALA	5022 9018h
1Ch	16	CMPSSB_RAMPDECVALS	5022 901Ch
20h	16	CMPSSB_RAMPSTS	5022 9020h
24h	16	CMPSSB_DACLVALS	5022 9024h
26h	16	CMPSSB_DACLVALA	5022 9026h
28h	16	CMPSSB_RAMPDLYA	5022 9028h
2Ah	16	CMPSSB_RAMPDLYS	5022 902Ah
2Ch	16	CMPSSB_CTRIPLFILCTL	5022 902Ch
2Eh	16	CMPSSB_CTRIPLFILCLKCTL	5022 902Eh
30h	16	CMPSSB_CTRIPHFILCTL	5022 9030h
32h	16	CMPSSB_CTRIPHFILCLKCTL	5022 9032h
34h	16	CMPSSB_COMPLOCK	5022 9034h
38h	16	CMPSSB_DACHVALS2	5022 9038h
3Ah	16	CMPSSB_DACLVALS2	5022 903Ah
3Ch	16	CMPSSB_CONFIG1	5022 903Ch

3.6.2 CMPSSB Registers

CMPSSB Registers

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3.6.2.1 CMPSSB_COMPCTL Register

3.6.2.1.1 CMPSSB_COMPCTL Register (Offset = 0h) [reset = 0h]

CMPSS Comparator Control Register.

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Table 3-453. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0000h
CMPSSB1	5022 1000h
CMPSSB2	5022 2000h
CMPSSB3	5022 3000h
CMPSSB4	5022 4000h
CMPSSB5	5022 5000h
CMPSSB6	5022 6000h
CMPSSB7	5022 7000h
CMPSSB8	5022 8000h
CMPSSB9	5022 9000h

Figure 3-218. CMPSSB_COMPCTL Name Register

15	14	13	12	11	10	9	8
COMPDACE	ASYNCLEN	CTRIPOUTLSEL		CTRIPLSEL		COMPLINV	RESERVED_3
R/W	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2	ASYNCHEN	CTRIPOUTHSEL		CTRIPHSEL		COMPHINV	RESERVED_1
R	R/W	R/W		R/W		R/W	R/W
0h	0h	0h		0h		0h	0h

Table 3-454. CMPSSB_COMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	COMPDACE	R/W	0h	Comparator/DAC enable. 0 Comparator/DAC disabled 1 Comparator/DAC enabled
14	ASYNCLEN	R/W	0h	Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIPOUTLSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
13:12	CTRIPOUTLSEL	R/W	0h	Low comparator CTRIPOUTL source select. 0 Asynchronous comparator output drives CTRIPOUTL 1 Synchronous comparator output drives CTRIPOUTL 2 Output of digital filter drives CTRIPOUTL 3 Latched output of digital filter drives CTRIPOUTL
11:10	CTRIPLSEL	R/W	0h	Low comparator CTRIPL source select. 0 Asynchronous comparator output drives CTRIPL 1 Synchronous comparator output drives CTRIPL 2 Output of digital filter drives CTRIPL 3 Latched output of digital filter drives CTRIPL
9	COMPLINV	R/W	0h	Low comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
8	RESERVED_3	R/W	0h	Reserved for CMPSSB

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Table 3-454. CMPSSB_COMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED_2	R	0h	Reserved
6	ASYNCHEN	R/W	0h	High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
5:4	CTRIPOUTHSEL	R/W	0h	High comparator CTRIPOUTH source select. 0 Asynchronous comparator output drives CTRIPOUTH 1 Synchronous comparator output drives CTRIPOUTH 2 Output of digital filter drives CTRIPOUTH 3 Latched output of digital filter drives CTRIPOUTH
3:2	CTRIPHSEL	R/W	0h	High comparator CTRIPH source select. 0 Asynchronous comparator output drives CTRIPH 1 Synchronous comparator output drives CTRIPH 2 Output of digital filter drives CTRIPH 3 Latched output of digital filter drives CTRIPH
1	COMPHINV	R/W	0h	High comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
0	RESERVED_1	R/W	0h	Reserved for CMPSSB

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3.6.2.2 CMPSSB_COMPSTS Register

3.6.2.2.1 CMPSSB_COMPSTS Register (Offset = 4h) [reset = 0h]

CMPSS Comparator Status Register.

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Table 3-455. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0004h
CMPSSB1	5022 1004h
CMPSSB2	5022 2004h
CMPSSB3	5022 3004h
CMPSSB4	5022 4004h
CMPSSB5	5022 5004h
CMPSSB6	5022 6004h
CMPSSB7	5022 7004h
CMPSSB8	5022 8004h
CMPSSB9	5022 9004h

Figure 3-219. CMPSSB_COMPSTS Name Register

15	14	13	12	11	10	9	8
RESERVED_2						COMPLLATCH	COMPLSTS
R						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED_1						COMPHLATCH	COMPHSTS
R						R	R
0h						0h	0h

Table 3-456. CMPSSB_COMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_2	R	0h	Reserved
9	COMPLLATCH	R	0h	Latched value of low comparator digital filter output
8	COMPLSTS	R	0h	Low comparator digital filter output
7:2	RESERVED_1	R	0h	Reserved
1	COMPHLATCH	R	0h	Latched value of high comparator digital filter output
0	COMPHSTS	R	0h	High comparator digital filter output

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3.6.2.3 CMPSSB_COMPSTSCLR Register

3.6.2.3.1 CMPSSB_COMPSTSCLR Register (Offset = 6h) [reset = 0h]

CMPSS Comparator Status Clear Register.

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Table 3-457. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0006h
CMPSSB1	5022 1006h
CMPSSB2	5022 2006h
CMPSSB3	5022 3006h
CMPSSB4	5022 4006h
CMPSSB5	5022 5006h
CMPSSB6	5022 6006h
CMPSSB7	5022 7006h
CMPSSB8	5022 8006h
CMPSSB9	5022 9006h

Figure 3-220. CMPSSB_COMPSTSCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_3					LSYNCCLREN	LLATCHCLR	RESERVED_2
R					R/W	R/W1TS	R
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2					HSYNCCLREN	HLATCHCLR	RESERVED_1
R					R/W	R/W1TS	R
0h					0h	0h	0h

Table 3-458. CMPSSB_COMPSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_3	R	0h	Reserved
10	LSYNCCLREN	R/W	0h	Low comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
9	LLATCHCLR	R/W1TS	0h	Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH]
8:3	RESERVED_2	R	0h	Reserved
2	HSYNCCLREN	R/W	0h	High comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
1	HLATCHCLR	R/W1TS	0h	High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH]

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Table 3-458. CMPSSB_COMPSTSCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED_1	R	0h	Reserved

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3.6.2.4 CMPSSB_COMPDACCTL Register

3.6.2.4.1 CMPSSB_COMPDACCTL Register (Offset = 8h) [reset = 0h]

CMPSS DAC Control Register.

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Table 3-459. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0008h
CMPSSB1	5022 1008h
CMPSSB2	5022 2008h
CMPSSB3	5022 3008h
CMPSSB4	5022 4008h
CMPSSB5	5022 5008h
CMPSSB6	5022 6008h
CMPSSB7	5022 7008h
CMPSSB8	5022 8008h
CMPSSB9	5022 9008h

Figure 3-221. CMPSSB_COMPDACCTL Name Register

15	14	13	12	11	10	9	8
FREESOFT		RESERVED_1	BLANKEN	BLANKSOURCE			
R/W		R	R/W	R/W			
0h		0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SWLOADSEL	RAMPLOADSEL	SELREF	RAMPSOURCE				DACSOURCE
R/W	R/W	R/W	R/W				R/W
0h	0h	0h	0h				0h

Table 3-460. CMPSSB_COMPDACCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREESOFT	R/W	0h	Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend. 00b Ramp generator stops immediately during emulation suspend 01b Ramp generator completes current ramp and stops at next EPWMSYNCPER during emulation suspend 1Xb Ramp generator runs freely
13	RESERVED_1	R	0h	Reserved
12	BLANKEN	R/W	0h	EPWMBLANK enable. This bit enables the EPWMBLANK signal. 0 EPWMBLANK signal is disabled. 1 EPWMBLANK signal is enabled.
11:8	BLANKSOURCE	R/W	0h	EPWMBLANK source select. This bit field determines which EPWMnBLANK is passed on as the EPWMBLANK signal. Where n represents the maximum number of EPWMBLANK signals available on the device: 0 EPWM1BLANK 1 EPWM2BLANK 2 EPWM3BLANK ... n-1 EPWMnBLANK
7	SWLOADSEL	R/W	0h	Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or EPWMSYNCPER. 0 DACxVALA is updated from DACxVALS on SYSCLK 1 DACxVALA is updated from DACxVALS on EPWMSYNCPER

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Table 3-460. CMPSSB_COMPDACCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RAMPLOADSEL	R/W	0h	Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered. 0 RAMPSTS is loaded from RAMPMAXREFA 1 RAMPSTS is loaded from RAMPMAXREFS
5	SELREF	R/W	0h	CMPSS reference select 0 vref_1p8v as reference voltage [default] 1 vdd_1p8v as reference voltage
4:1	RAMPSOURCE	R/W	0h	EPWMSYNCPER source select. Determines which EPWMnSYNCPER signal is used within the CMPSS module. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER
0	DACSOURCE	R/W	0h	DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator. 0 DACHVALA is updated from DACHVALS 1 DACHVALA is updated from the ramp generator

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3.6.2.5 CMPSSB_COMPDACCTL2 Register

3.6.2.5.1 CMPSSB_COMPDACCTL2 Register (Offset = Ah) [reset = 0h]

CMPSS DAC Control Register 2

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Table 3-461. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 000Ah
CMPSSB1	5022 100Ah
CMPSSB2	5022 200Ah
CMPSSB3	5022 300Ah
CMPSSB4	5022 400Ah
CMPSSB5	5022 500Ah
CMPSSB6	5022 600Ah
CMPSSB7	5022 700Ah
CMPSSB8	5022 800Ah
CMPSSB9	5022 900Ah

Figure 3-222. CMPSSB_COMPDACCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_3					RAMPSOURCEUSEL	RESERVED_2	BLANKSOURCEUSEL
R					R/W	R	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1		DEACTIVESEL					DEENABLE
R		R/W					R/W
0h		0h					0h

Table 3-462. CMPSSB_COMPDACCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_3	R	0h	Reserved
10	RAMPSOURCEUSEL	R/W	0h	0: Selects EPWM0 to 15 as RAMP source 1:Selects EPWM16 to 31 as RAMP source
9	RESERVED_2	R	0h	Reserved
8	BLANKSOURCEUSEL	R/W	0h	0: Selects EPWM0 to 15 as blank source 1:Selects EPWM16 to 31 as blank source
7:6	RESERVED_1	R	0h	Reserved
5:1	DEACTIVESEL	R/W	0h	DEACTIVE source select: 0x0 : EPWM0.DEACTIVE 0x1 : EPWM1.DEACTIVE 0x2 : EPWM2.DEACTIVE 0x3 : EPWM3.DEACTIVE . . 0x31 : EPWM31.DEACTIVE
0	DEENABLE	R/W	0h	DE mode enable. 0 DE mode features disabled. 1 DE mode features enabled.

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3.6.2.6 CMPSSB_DACHVALS Register

3.6.2.6.1 CMPSSB_DACHVALS Register (Offset = Ch) [reset = 0h]

CMPSS High DAC Value Shadow Register.

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Table 3-463. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 000Ch
CMPSSB1	5022 100Ch
CMPSSB2	5022 200Ch
CMPSSB3	5022 300Ch
CMPSSB4	5022 400Ch
CMPSSB5	5022 500Ch
CMPSSB6	5022 600Ch
CMPSSB7	5022 700Ch
CMPSSB8	5022 800Ch
CMPSSB9	5022 900Ch

Figure 3-223. CMPSSB_DACHVALS Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACVAL							
R/W							
0h							

Table 3-464. CMPSSB_DACHVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R/W	0h	High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

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3.6.2.7 CMPSSB_DACHVALA Register

3.6.2.7.1 CMPSSB_DACHVALA Register (Offset = Eh) [reset = 0h]

CMPSS High DAC Value Active Register.

Return to Summary Table

Table 3-465. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 000Eh
CMPSSB1	5022 100Eh
CMPSSB2	5022 200Eh
CMPSSB3	5022 300Eh
CMPSSB4	5022 400Eh
CMPSSB5	5022 500Eh
CMPSSB6	5022 600Eh
CMPSSB7	5022 700Eh
CMPSSB8	5022 800Eh
CMPSSB9	5022 900Eh

Figure 3-224. CMPSSB_DACHVALA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACVAL							
R							
0h							

Table 3-466. CMPSSB_DACHVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R	0h	High DAC active value. Value that is actively driven by the high DAC.

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3.6.2.8 CMPSSB_RAMPMAXREFA Register

3.6.2.8.1 CMPSSB_RAMPMAXREFA Register (Offset = 10h) [reset = 0h]

CMPSS Ramp Max Reference Active Register.

Return to Summary Table

Table 3-467. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0010h
CMPSSB1	5022 1010h
CMPSSB2	5022 2010h
CMPSSB3	5022 3010h
CMPSSB4	5022 4010h
CMPSSB5	5022 5010h
CMPSSB6	5022 6010h
CMPSSB7	5022 7010h
CMPSSB8	5022 8010h
CMPSSB9	5022 9010h

Figure 3-225. CMPSSB_RAMPMAXREFA Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
R							
0h							
7	6	5	4	3	2	1	0
RAMPMAXREF							
R							
0h							

Table 3-468. CMPSSB_RAMPMAXREFA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPMAXREF	R	0h	Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS.

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3.6.2.9 CMPSSB_RAMPMAXREFS Register

3.6.2.9.1 CMPSSB_RAMPMAXREFS Register (Offset = 14h) [reset = 0h]

CMPSS Ramp Max Reference Shadow Register.

Return to Summary Table

Table 3-469. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0014h
CMPSSB1	5022 1014h
CMPSSB2	5022 2014h
CMPSSB3	5022 3014h
CMPSSB4	5022 4014h
CMPSSB5	5022 5014h
CMPSSB6	5022 6014h
CMPSSB7	5022 7014h
CMPSSB8	5022 8014h
CMPSSB9	5022 9014h

Figure 3-226. CMPSSB_RAMPMAXREFS Name Register

15	14	13	12	11	10	9	8
RAMPMAXREF							
R/W							
0h							
7	6	5	4	3	2	1	0
RAMPMAXREF							
R/W							
0h							

Table 3-470. CMPSSB_RAMPMAXREFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPMAXREF	R/W	0h	Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS.

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3.6.2.10 CMPSSB_RAMPDECVALA Register

3.6.2.10.1 CMPSSB_RAMPDECVALA Register (Offset = 18h) [reset = 0h]

CMPSS Ramp Decrement Value Active Register.

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Table 3-471. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0018h
CMPSSB1	5022 1018h
CMPSSB2	5022 2018h
CMPSSB3	5022 3018h
CMPSSB4	5022 4018h
CMPSSB5	5022 5018h
CMPSSB6	5022 6018h
CMPSSB7	5022 7018h
CMPSSB8	5022 8018h
CMPSSB9	5022 9018h

Figure 3-227. CMPSSB_RAMPDECVALA Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
R							
0h							
7	6	5	4	3	2	1	0
RAMPDECVAL							
R							
0h							

Table 3-472. CMPSSB_RAMPDECVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPDECVAL	R	0h	Ramp decrement value active. Latched value that will be subtracted from RAMPSTS.

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3.6.2.11 CMPSSB_RAMPDECVALS Register

3.6.2.11.1 CMPSSB_RAMPDECVALS Register (Offset = 1Ch) [reset = 0h]

CMPSS Ramp Decrement Value Shadow Register.

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Table 3-473. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 001Ch
CMPSSB1	5022 101Ch
CMPSSB2	5022 201Ch
CMPSSB3	5022 301Ch
CMPSSB4	5022 401Ch
CMPSSB5	5022 501Ch
CMPSSB6	5022 601Ch
CMPSSB7	5022 701Ch
CMPSSB8	5022 801Ch
CMPSSB9	5022 901Ch

Figure 3-228. CMPSSB_RAMPDECVALS Name Register

15	14	13	12	11	10	9	8
RAMPDECVAL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMPDECVAL							
R/W							
0h							

Table 3-474. CMPSSB_RAMPDECVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPDECVAL	R/W	0h	Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA.

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3.6.2.12 CMPSSB_RAMPSTS Register

3.6.2.12.1 CMPSSB_RAMPSTS Register (Offset = 20h) [reset = 0h]

CMPSS Ramp Status Register.

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Table 3-475. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0020h
CMPSSB1	5022 1020h
CMPSSB2	5022 2020h
CMPSSB3	5022 3020h
CMPSSB4	5022 4020h
CMPSSB5	5022 5020h
CMPSSB6	5022 6020h
CMPSSB7	5022 7020h
CMPSSB8	5022 8020h
CMPSSB9	5022 9020h

Figure 3-229. CMPSSB_RAMPSTS Name Register

15	14	13	12	11	10	9	8
RAMPVALUE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMPVALUE							
R							
0h							

Table 3-476. CMPSSB_RAMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RAMPVALUE	R	0h	Ramp value. Present value of ramp generator.

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3.6.2.13 CMPSSB_DACLVALS Register

3.6.2.13.1 CMPSSB_DACLVALS Register (Offset = 24h) [reset = 0h]

CMPSS Low DAC Value Shadow Register.

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Table 3-477. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0024h
CMPSSB1	5022 1024h
CMPSSB2	5022 2024h
CMPSSB3	5022 3024h
CMPSSB4	5022 4024h
CMPSSB5	5022 5024h
CMPSSB6	5022 6024h
CMPSSB7	5022 7024h
CMPSSB8	5022 8024h
CMPSSB9	5022 9024h

Figure 3-230. CMPSSB_DACLVALS Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACVAL							
R/W							
0h							

Table 3-478. CMPSSB_DACLVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R/W	0h	Low DAC shadow value. value to be loaded into DACLVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

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3.6.2.14 CMPSSB_DACLVALA Register

3.6.2.14.1 CMPSSB_DACLVALA Register (Offset = 26h) [reset = 0h]

CMPSS Low DAC Value Active Register.

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Table 3-479. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0026h
CMPSSB1	5022 1026h
CMPSSB2	5022 2026h
CMPSSB3	5022 3026h
CMPSSB4	5022 4026h
CMPSSB5	5022 5026h
CMPSSB6	5022 6026h
CMPSSB7	5022 7026h
CMPSSB8	5022 8026h
CMPSSB9	5022 9026h

Figure 3-231. CMPSSB_DACLVALA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R			
0h				0h			
7	6	5	4	3	2	1	0
DACVAL							
R							
0h							

Table 3-480. CMPSSB_DACLVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R	0h	Low DAC active value. Value that is actively driven by the low DAC.

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3.6.2.15 CMPSSB_RAMPDLYA Register

3.6.2.15.1 CMPSSB_RAMPDLYA Register (Offset = 28h) [reset = 0h]

CMPSS Ramp Delay Active Register.

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Table 3-481. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0028h
CMPSSB1	5022 1028h
CMPSSB2	5022 2028h
CMPSSB3	5022 3028h
CMPSSB4	5022 4028h
CMPSSB5	5022 5028h
CMPSSB6	5022 6028h
CMPSSB7	5022 7028h
CMPSSB8	5022 8028h
CMPSSB9	5022 9028h

Figure 3-232. CMPSSB_RAMPDLYA Name Register

15	14	13	12	11	10	9	8
RESERVED_1			DELAY				
R			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DELAY							
R							
0h							

Table 3-482. CMPSSB_RAMPDLYA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12:0	DELAY	R	0h	Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a EPWMSYNCPER is received.

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3.6.2.16 CMPSSB_RAMPDLYS Register

3.6.2.16.1 CMPSSB_RAMPDLYS Register (Offset = 2Ah) [reset = 0h]

CMPSS Ramp Delay Shadow Register.

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Table 3-483. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 002Ah
CMPSSB1	5022 102Ah
CMPSSB2	5022 202Ah
CMPSSB3	5022 302Ah
CMPSSB4	5022 402Ah
CMPSSB5	5022 502Ah
CMPSSB6	5022 602Ah
CMPSSB7	5022 702Ah
CMPSSB8	5022 802Ah
CMPSSB9	5022 902Ah

Figure 3-233. CMPSSB_RAMPDLYS Name Register

15	14	13	12	11	10	9	8
RESERVED_1			DELAY				
R			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DELAY							
R/W							
0h							

Table 3-484. CMPSSB_RAMPDLYS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12:0	DELAY	R/W	0h	Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA.

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3.6.2.17 CMPSSB_CTRIPLFILCTL Register

3.6.2.17.1 CMPSSB_CTRIPLFILCTL Register (Offset = 2Ch) [reset = 0h]

CTRIPL Filter Control Register.

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Table 3-485. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 002Ch
CMPSSB1	5022 102Ch
CMPSSB2	5022 202Ch
CMPSSB3	5022 302Ch
CMPSSB4	5022 402Ch
CMPSSB5	5022 502Ch
CMPSSB6	5022 602Ch
CMPSSB7	5022 702Ch
CMPSSB8	5022 802Ch
CMPSSB9	5022 902Ch

Figure 3-234. CMPSSB_CTRIPLFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-486. CMPSSB_CTRIPLFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.6.2.18 CMPSSB_CTRIPLFILCLKCTL Register

3.6.2.18.1 CMPSSB_CTRIPLFILCLKCTL Register (Offset = 2Eh) [reset = 0h]

CTRIPL Filter Clock Control Register.

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Table 3-487. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 002Eh
CMPSSB1	5022 102Eh
CMPSSB2	5022 202Eh
CMPSSB3	5022 302Eh
CMPSSB4	5022 402Eh
CMPSSB5	5022 502Eh
CMPSSB6	5022 602Eh
CMPSSB7	5022 702Eh
CMPSSB8	5022 802Eh
CMPSSB9	5022 902Eh

Figure 3-235. CMPSSB_CTRIPLFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKPRESCALE							
R/W							
0h							

Table 3-488. CMPSSB_CTRIPLFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

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3.6.2.19 CMPSSB_CTRIPHFILCTL Register

3.6.2.19.1 CMPSSB_CTRIPHFILCTL Register (Offset = 30h) [reset = 0h]

CTRIPH Filter Control Register.

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Table 3-489. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0030h
CMPSSB1	5022 1030h
CMPSSB2	5022 2030h
CMPSSB3	5022 3030h
CMPSSB4	5022 4030h
CMPSSB5	5022 5030h
CMPSSB6	5022 6030h
CMPSSB7	5022 7030h
CMPSSB8	5022 8030h
CMPSSB9	5022 9030h

Figure 3-236. CMPSSB_CTRIPHFILCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-490. CMPSSB_CTRIPHFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.6.2.20 CMPSSB_CTRIPHFILCLKCTL Register

3.6.2.20.1 CMPSSB_CTRIPHFILCLKCTL Register (Offset = 32h) [reset = 0h]

CTRIPH Filter Clock Control Register.

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Table 3-491. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0032h
CMPSSB1	5022 1032h
CMPSSB2	5022 2032h
CMPSSB3	5022 3032h
CMPSSB4	5022 4032h
CMPSSB5	5022 5032h
CMPSSB6	5022 6032h
CMPSSB7	5022 7032h
CMPSSB8	5022 8032h
CMPSSB9	5022 9032h

Figure 3-237. CMPSSB_CTRIPHFILCLKCTL Name Register

15	14	13	12	11	10	9	8
CLKPRESCALE							
R/W							
0h							
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Table 3-492. CMPSSB_CTRIPHFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

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3.6.2.21 CMPSSB_COMPLOCK Register

3.6.2.21.1 CMPSSB_COMPLOCK Register (Offset = 34h) [reset = 0h]

CMPSS Lock Register.

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Table 3-493. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0034h
CMPSSB1	5022 1034h
CMPSSB2	5022 2034h
CMPSSB3	5022 3034h
CMPSSB4	5022 4034h
CMPSSB5	5022 5034h
CMPSSB6	5022 6034h
CMPSSB7	5022 7034h
CMPSSB8	5022 8034h
CMPSSB9	5022 9034h

Figure 3-238. CMPSSB_COMPLOCK Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED_1</td><td>TEST</td><td>CTRIP</td><td>DACCTL</td><td>COMPHYSCTL</td><td>COMPCTL</td></tr>
<tr><td colspan="3">R</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td><td>R/W1TS</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 3-494. CMPSSB_COMPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_1	R	0h	Reserved
4	TEST	R/W1TS	0h	TEST Lock. This bit, when set, will prevent any further writes to the any undocumented registers that may effect the performance/ behavior of this block. Once set this bit can only be cleared by a reset.
3	CTRIP	R/W1TS	0h	Lock write-access to the CTRIPxFILTCTL and CTRIPxFILCLKCTL registers. 0 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are locked. Only a system reset can clear this bit.
2	DACCTL	R/W1TS	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit.
1	COMPHYSCTL	R/W1TS	0h	Lock write-access to the COMPHYSCTL register. 0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect. 1 COMPHYSCTL register is locked. Only a system reset can clear this bit.
0	COMPCTL	R/W1TS	0h	Lock write-access to the COMPCTL register. 0 COMPCTL register is not locked. Write 0 to this bit has no effect. 1 COMPCTL register is locked. Only a system reset can clear this bit.

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3.6.2.22 CMPSSB_DACHVALS2 Register

3.6.2.22.1 CMPSSB_DACHVALS2 Register (Offset = 38h) [reset = 0h]

CMPSS High DAC Value Shadow Register 2

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Table 3-495. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 0038h
CMPSSB1	5022 1038h
CMPSSB2	5022 2038h
CMPSSB3	5022 3038h
CMPSSB4	5022 4038h
CMPSSB5	5022 5038h
CMPSSB6	5022 6038h
CMPSSB7	5022 7038h
CMPSSB8	5022 8038h
CMPSSB9	5022 9038h

Figure 3-239. CMPSSB_DACHVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			

7	6	5	4	3	2	1	0
DACVAL							
R/W							
0h							

Table 3-496. CMPSSB_DACHVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R/W	0h	High DAC shadow register2 value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

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3.6.2.23 CMPSSB_DACLVALS2 Register

3.6.2.23.1 CMPSSB_DACLVALS2 Register (Offset = 3Ah) [reset = 0h]

CMPSS Low DAC Value Shadow Register 2

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Table 3-497. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 003Ah
CMPSSB1	5022 103Ah
CMPSSB2	5022 203Ah
CMPSSB3	5022 303Ah
CMPSSB4	5022 403Ah
CMPSSB5	5022 503Ah
CMPSSB6	5022 603Ah
CMPSSB7	5022 703Ah
CMPSSB8	5022 803Ah
CMPSSB9	5022 903Ah

Figure 3-240. CMPSSB_DACLVALS2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DACVAL			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DACVAL							
R/W							
0h							

Table 3-498. CMPSSB_DACLVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DACVAL	R/W	0h	Low DAC shadow register2 value. Value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

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3.6.2.24 CMPSSB_CONFIG1 Register

3.6.2.24.1 CMPSSB_CONFIG1 Register (Offset = 3Ch) [reset = 0h]

CMPSS Config1 Register.

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Table 3-499. Instance Table

Instance Name	Physical Address
CMPSSB0	5022 003Ch
CMPSSB1	5022 103Ch
CMPSSB2	5022 203Ch
CMPSSB3	5022 303Ch
CMPSSB4	5022 403Ch
CMPSSB5	5022 503Ch
CMPSSB6	5022 603Ch
CMPSSB7	5022 703Ch
CMPSSB8	5022 803Ch
CMPSSB9	5022 903Ch

Figure 3-241. CMPSSB_CONFIG1 Name Register

15	14	13	12	11	10	9	8
SPARE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMPLHYS				COMPHHYS			
R/W				R/W			
0h				0h			

Table 3-500. CMPSSB_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	SPARE	R/W	0h	SPARE
7:4	COMPLHYS	R/W	0h	CompL Hysteresis COMPLHYS[3] : reserved COMPLHYS[2] : Controls which comparator output value hysteresis is applied to. 1'b0 : Hysteresis is applied when the comparator output is 1'b1 1'b1 : Hysteresis is applied when the comparator output is 1'b0 COMPLHYS[1:0] = hysteresis value 2'b00 : 0 LSB 2'b01 : 17.5 LSB 2'b10 : 35 LSB 2'b11 : 52.5 LSB
3:0	COMPHHYS	R/W	0h	CompH Hysteresis COMPHHYS[3] : reserved COMPHHYS[2] : Controls which comparator output value hysteresis is applied to. 1'b0 : Hysteresis is applied when the comparator output is 1'b1 1'b1 : Hysteresis is applied when the comparator output is 1'b0 COMPHHYS[1:0] = hysteresis value 2'b00 : 0 LSB 2'b01 : 17.5 LSB 2'b10 : 35 LSB 2'b11 : 52.5 LSB

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3.7 ECAP

ECAP

3.7.1 ECAP Summaries

ECAP Summaries

Table 3-501. ECAP Registers, Base Address=5024 0000h, Length=256

Offset	Length	Register Name	ECAP00 Physical Address	ECAP01 Physical Address	ECAP02 Physical Address
0h	32	ECAP_TSCTR	5024 0000h	5024 1000h	5024 2000h
4h	32	ECAP_CTRPHS	5024 0004h	5024 1004h	5024 2004h
8h	32	ECAP_CAP1	5024 0008h	5024 1008h	5024 2008h
Ch	32	ECAP_CAP2	5024 000Ch	5024 100Ch	5024 200Ch
10h	32	ECAP_CAP3	5024 0010h	5024 1010h	5024 2010h
14h	32	ECAP_CAP4	5024 0014h	5024 1014h	5024 2014h
24h	32	ECAP_ECCTL0	5024 0024h	5024 1024h	5024 2024h
28h	16	ECAP_ECCTL1	5024 0028h	5024 1028h	5024 2028h
2Ah	16	ECAP_ECCTL2	5024 002Ah	5024 102Ah	5024 202Ah
2Ch	16	ECAP_ECEINT	5024 002Ch	5024 102Ch	5024 202Ch
2Eh	16	ECAP_ECFLG	5024 002Eh	5024 102Eh	5024 202Eh
30h	16	ECAP_ECCLR	5024 0030h	5024 1030h	5024 2030h
32h	16	ECAP_ECFRC	5024 0032h	5024 1032h	5024 2032h
3Ch	32	ECAP_ECAPSYNCINSEL	5024 003Ch	5024 103Ch	5024 203Ch
80h	32	ECAP_MUNIT_COMMON_CTL	5024 0080h	5024 1080h	5024 2080h
C0h	32	ECAP_MUNIT_1_CTL	5024 00C0h	5024 10C0h	5024 20C0h
C4h	32	ECAP_MUNIT_1_SHADOW_CTL	5024 00C4h	5024 10C4h	5024 20C4h
D0h	32	ECAP_MUNIT_1_MIN	5024 00D0h	5024 10D0h	5024 20D0h
D4h	32	ECAP_MUNIT_1_MAX	5024 00D4h	5024 10D4h	5024 20D4h
D8h	32	ECAP_MUNIT_1_MIN_SHADOW	5024 00D8h	5024 10D8h	5024 20D8h
DCh	32	ECAP_MUNIT_1_MAX_SHADOW	5024 00DCh	5024 10DCh	5024 20DCh
E0h	32	ECAP_MUNIT_1_DEBUG_RANGE_MIN	5024 00E0h	5024 10E0h	5024 20E0h
E4h	32	ECAP_MUNIT_1_DEBUG_RANGE_MAX	5024 00E4h	5024 10E4h	5024 20E4h
100h	32	ECAP_MUNIT_2_CTL	5024 0100h	5024 1100h	5024 2100h
104h	32	ECAP_MUNIT_2_SHADOW_CTL	5024 0104h	5024 1104h	5024 2104h
110h	32	ECAP_MUNIT_2_MIN	5024 0110h	5024 1110h	5024 2110h
114h	32	ECAP_MUNIT_2_MAX	5024 0114h	5024 1114h	5024 2114h
118h	32	ECAP_MUNIT_2_MIN_SHADOW	5024 0118h	5024 1118h	5024 2118h
11Ch	32	ECAP_MUNIT_2_MAX_SHADOW	5024 011Ch	5024 111Ch	5024 211Ch
120h	32	ECAP_MUNIT_2_DEBUG_RANGE_MIN	5024 0120h	5024 1120h	5024 2120h
124h	32	ECAP_MUNIT_2_DEBUG_RANGE_MAX	5024 0124h	5024 1124h	5024 2124h

Table 3-502. ECAP Registers, Base Address=5024 0000h, Length=256

Offset	Length	Register Name	ECAP03 Physical Address	ECAP04 Physical Address	ECAP05 Physical Address
0h	32	ECAP_TSCTR	5024 3000h	5024 4000h	5024 5000h

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Table 3-502. ECAP Registers, Base Address=5024 0000h, Length=256 (continued)

Offset	Length	Register Name	ECAP03 Physical Address	ECAP04 Physical Address	ECAP05 Physical Address
4h	32	ECAP_CTRPHS	5024 3004h	5024 4004h	5024 5004h
8h	32	ECAP_CAP1	5024 3008h	5024 4008h	5024 5008h
Ch	32	ECAP_CAP2	5024 300Ch	5024 400Ch	5024 500Ch
10h	32	ECAP_CAP3	5024 3010h	5024 4010h	5024 5010h
14h	32	ECAP_CAP4	5024 3014h	5024 4014h	5024 5014h
24h	32	ECAP_ECCTL0	5024 3024h	5024 4024h	5024 5024h
28h	16	ECAP_ECCTL1	5024 3028h	5024 4028h	5024 5028h
2Ah	16	ECAP_ECCTL2	5024 302Ah	5024 402Ah	5024 502Ah
2Ch	16	ECAP_ECEINT	5024 302Ch	5024 402Ch	5024 502Ch
2Eh	16	ECAP_ECFLG	5024 302Eh	5024 402Eh	5024 502Eh
30h	16	ECAP_ECCLR	5024 3030h	5024 4030h	5024 5030h
32h	16	ECAP_ECFRC	5024 3032h	5024 4032h	5024 5032h
3Ch	32	ECAP_ECAPSYNCINSEL	5024 303Ch	5024 403Ch	5024 503Ch
80h	32	ECAP_MUNIT_COMMON_CTL	5024 3080h	5024 4080h	5024 5080h
C0h	32	ECAP_MUNIT_1_CTL	5024 30C0h	5024 40C0h	5024 50C0h
C4h	32	ECAP_MUNIT_1_SHADOW_CTL	5024 30C4h	5024 40C4h	5024 50C4h
D0h	32	ECAP_MUNIT_1_MIN	5024 30D0h	5024 40D0h	5024 50D0h
D4h	32	ECAP_MUNIT_1_MAX	5024 30D4h	5024 40D4h	5024 50D4h
D8h	32	ECAP_MUNIT_1_MIN_SHADOW	5024 30D8h	5024 40D8h	5024 50D8h
DCh	32	ECAP_MUNIT_1_MAX_SHADOW	5024 30DCh	5024 40DCh	5024 50DCh
E0h	32	ECAP_MUNIT_1_DEBUG_RANGE_MIN	5024 30E0h	5024 40E0h	5024 50E0h
E4h	32	ECAP_MUNIT_1_DEBUG_RANGE_MAX	5024 30E4h	5024 40E4h	5024 50E4h
100h	32	ECAP_MUNIT_2_CTL	5024 3100h	5024 4100h	5024 5100h
104h	32	ECAP_MUNIT_2_SHADOW_CTL	5024 3104h	5024 4104h	5024 5104h
110h	32	ECAP_MUNIT_2_MIN	5024 3110h	5024 4110h	5024 5110h
114h	32	ECAP_MUNIT_2_MAX	5024 3114h	5024 4114h	5024 5114h
118h	32	ECAP_MUNIT_2_MIN_SHADOW	5024 3118h	5024 4118h	5024 5118h
11Ch	32	ECAP_MUNIT_2_MAX_SHADOW	5024 311Ch	5024 411Ch	5024 511Ch
120h	32	ECAP_MUNIT_2_DEBUG_RANGE_MIN	5024 3120h	5024 4120h	5024 5120h
124h	32	ECAP_MUNIT_2_DEBUG_RANGE_MAX	5024 3124h	5024 4124h	5024 5124h

Table 3-503. ECAP Registers, Base Address=5024 0000h, Length=256

Offset	Length	Register Name	ECAP06 Physical Address	ECAP07 Physical Address	ECAP08 Physical Address
0h	32	ECAP_TSCTR	5024 6000h	5024 7000h	5024 8000h
4h	32	ECAP_CTRPHS	5024 6004h	5024 7004h	5024 8004h
8h	32	ECAP_CAP1	5024 6008h	5024 7008h	5024 8008h
Ch	32	ECAP_CAP2	5024 600Ch	5024 700Ch	5024 800Ch
10h	32	ECAP_CAP3	5024 6010h	5024 7010h	5024 8010h
14h	32	ECAP_CAP4	5024 6014h	5024 7014h	5024 8014h
24h	32	ECAP_ECCTL0	5024 6024h	5024 7024h	5024 8024h
28h	16	ECAP_ECCTL1	5024 6028h	5024 7028h	5024 8028h
2Ah	16	ECAP_ECCTL2	5024 602Ah	5024 702Ah	5024 802Ah

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Table 3-503. ECAP Registers, Base Address=5024 0000h, Length=256 (continued)

Offset	Length	Register Name	ECAP06 Physical Address	ECAP07 Physical Address	ECAP08 Physical Address
2Ch	16	ECAP_ECEINT	5024 602Ch	5024 702Ch	5024 802Ch
2Eh	16	ECAP_ECFLG	5024 602Eh	5024 702Eh	5024 802Eh
30h	16	ECAP_ECCLR	5024 6030h	5024 7030h	5024 8030h
32h	16	ECAP_ECFRC	5024 6032h	5024 7032h	5024 8032h
3Ch	32	ECAP_ECAPSYNCINSEL	5024 603Ch	5024 703Ch	5024 803Ch
80h	32	ECAP_MUNIT_COMMON_CTL	5024 6080h	5024 7080h	5024 8080h
C0h	32	ECAP_MUNIT_1_CTL	5024 60C0h	5024 70C0h	5024 80C0h
C4h	32	ECAP_MUNIT_1_SHADOW_CTL	5024 60C4h	5024 70C4h	5024 80C4h
D0h	32	ECAP_MUNIT_1_MIN	5024 60D0h	5024 70D0h	5024 80D0h
D4h	32	ECAP_MUNIT_1_MAX	5024 60D4h	5024 70D4h	5024 80D4h
D8h	32	ECAP_MUNIT_1_MIN_SHADOW	5024 60D8h	5024 70D8h	5024 80D8h
DCh	32	ECAP_MUNIT_1_MAX_SHADOW	5024 60DCh	5024 70DCh	5024 80DCh
E0h	32	ECAP_MUNIT_1_DEBUG_RANGE_MIN	5024 60E0h	5024 70E0h	5024 80E0h
E4h	32	ECAP_MUNIT_1_DEBUG_RANGE_MAX	5024 60E4h	5024 70E4h	5024 80E4h
100h	32	ECAP_MUNIT_2_CTL	5024 6100h	5024 7100h	5024 8100h
104h	32	ECAP_MUNIT_2_SHADOW_CTL	5024 6104h	5024 7104h	5024 8104h
110h	32	ECAP_MUNIT_2_MIN	5024 6110h	5024 7110h	5024 8110h
114h	32	ECAP_MUNIT_2_MAX	5024 6114h	5024 7114h	5024 8114h
118h	32	ECAP_MUNIT_2_MIN_SHADOW	5024 6118h	5024 7118h	5024 8118h
11Ch	32	ECAP_MUNIT_2_MAX_SHADOW	5024 611Ch	5024 711Ch	5024 811Ch
120h	32	ECAP_MUNIT_2_DEBUG_RANGE_MIN	5024 6120h	5024 7120h	5024 8120h
124h	32	ECAP_MUNIT_2_DEBUG_RANGE_MAX	5024 6124h	5024 7124h	5024 8124h

Table 3-504. ECAP Registers, Base Address=5024 0000h, Length=256

Offset	Length	Register Name	ECAP09 Physical Address	ECAP10 Physical Address	ECAP11 Physical Address
0h	32	ECAP_TSCTR	5024 9000h	5024 A000h	5024 B000h
4h	32	ECAP_CTRPHS	5024 9004h	5024 A004h	5024 B004h
8h	32	ECAP_CAP1	5024 9008h	5024 A008h	5024 B008h
Ch	32	ECAP_CAP2	5024 900Ch	5024 A00Ch	5024 B00Ch
10h	32	ECAP_CAP3	5024 9010h	5024 A010h	5024 B010h
14h	32	ECAP_CAP4	5024 9014h	5024 A014h	5024 B014h
24h	32	ECAP_ECCTL0	5024 9024h	5024 A024h	5024 B024h
28h	16	ECAP_ECCTL1	5024 9028h	5024 A028h	5024 B028h
2Ah	16	ECAP_ECCTL2	5024 902Ah	5024 A02Ah	5024 B02Ah
2Ch	16	ECAP_ECEINT	5024 902Ch	5024 A02Ch	5024 B02Ch
2Eh	16	ECAP_ECFLG	5024 902Eh	5024 A02Eh	5024 B02Eh
30h	16	ECAP_ECCLR	5024 9030h	5024 A030h	5024 B030h
32h	16	ECAP_ECFRC	5024 9032h	5024 A032h	5024 B032h
3Ch	32	ECAP_ECAPSYNCINSEL	5024 903Ch	5024 A03Ch	5024 B03Ch
80h	32	ECAP_MUNIT_COMMON_CTL	5024 9080h	5024 A080h	5024 B080h
C0h	32	ECAP_MUNIT_1_CTL	5024 90C0h	5024 A0C0h	5024 B0C0h
C4h	32	ECAP_MUNIT_1_SHADOW_CTL	5024 90C4h	5024 A0C4h	5024 B0C4h

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Table 3-504. ECAP Registers, Base Address=5024 0000h, Length=256 (continued)

Offset	Length	Register Name	ECAP09 Physical Address	ECAP10 Physical Address	ECAP11 Physical Address
D0h	32	ECAP_MUNIT_1_MIN	5024 90D0h	5024 A0D0h	5024 B0D0h
D4h	32	ECAP_MUNIT_1_MAX	5024 90D4h	5024 A0D4h	5024 B0D4h
D8h	32	ECAP_MUNIT_1_MIN_SHADOW	5024 90D8h	5024 A0D8h	5024 B0D8h
DCh	32	ECAP_MUNIT_1_MAX_SHADOW	5024 90DCh	5024 A0DCh	5024 B0DCh
E0h	32	ECAP_MUNIT_1_DEBUG_RANGE_MIN	5024 90E0h	5024 A0E0h	5024 B0E0h
E4h	32	ECAP_MUNIT_1_DEBUG_RANGE_MAX	5024 90E4h	5024 A0E4h	5024 B0E4h
100h	32	ECAP_MUNIT_2_CTL	5024 9100h	5024 A100h	5024 B100h
104h	32	ECAP_MUNIT_2_SHADOW_CTL	5024 9104h	5024 A104h	5024 B104h
110h	32	ECAP_MUNIT_2_MIN	5024 9110h	5024 A110h	5024 B110h
114h	32	ECAP_MUNIT_2_MAX	5024 9114h	5024 A114h	5024 B114h
118h	32	ECAP_MUNIT_2_MIN_SHADOW	5024 9118h	5024 A118h	5024 B118h
11Ch	32	ECAP_MUNIT_2_MAX_SHADOW	5024 911Ch	5024 A11Ch	5024 B11Ch
120h	32	ECAP_MUNIT_2_DEBUG_RANGE_MIN	5024 9120h	5024 A120h	5024 B120h
124h	32	ECAP_MUNIT_2_DEBUG_RANGE_MAX	5024 9124h	5024 A124h	5024 B124h

Table 3-505. ECAP Registers, Base Address=5024 0000h, Length=256

Offset	Length	Register Name	ECAP12 Physical Address	ECAP13 Physical Address	ECAP14 Physical Address
0h	32	ECAP_TSCTR	5024 C000h	5024 D000h	5024 E000h
4h	32	ECAP_CTRPHS	5024 C004h	5024 D004h	5024 E004h
8h	32	ECAP_CAP1	5024 C008h	5024 D008h	5024 E008h
Ch	32	ECAP_CAP2	5024 C00Ch	5024 D00Ch	5024 E00Ch
10h	32	ECAP_CAP3	5024 C010h	5024 D010h	5024 E010h
14h	32	ECAP_CAP4	5024 C014h	5024 D014h	5024 E014h
24h	32	ECAP_ECCTL0	5024 C024h	5024 D024h	5024 E024h
28h	16	ECAP_ECCTL1	5024 C028h	5024 D028h	5024 E028h
2Ah	16	ECAP_ECCTL2	5024 C02Ah	5024 D02Ah	5024 E02Ah
2Ch	16	ECAP_ECEINT	5024 C02Ch	5024 D02Ch	5024 E02Ch
2Eh	16	ECAP_ECFLG	5024 C02Eh	5024 D02Eh	5024 E02Eh
30h	16	ECAP_ECCLR	5024 C030h	5024 D030h	5024 E030h
32h	16	ECAP_ECFRC	5024 C032h	5024 D032h	5024 E032h
3Ch	32	ECAP_ECAPSYNCINSEL	5024 C03Ch	5024 D03Ch	5024 E03Ch
80h	32	ECAP_MUNIT_COMMON_CTL	5024 C080h	5024 D080h	5024 E080h
C0h	32	ECAP_MUNIT_1_CTL	5024 C0C0h	5024 D0C0h	5024 E0C0h
C4h	32	ECAP_MUNIT_1_SHADOW_CTL	5024 C0C4h	5024 D0C4h	5024 E0C4h
D0h	32	ECAP_MUNIT_1_MIN	5024 C0D0h	5024 D0D0h	5024 E0D0h
D4h	32	ECAP_MUNIT_1_MAX	5024 C0D4h	5024 D0D4h	5024 E0D4h
D8h	32	ECAP_MUNIT_1_MIN_SHADOW	5024 C0D8h	5024 D0D8h	5024 E0D8h
DCh	32	ECAP_MUNIT_1_MAX_SHADOW	5024 C0DCh	5024 D0DCh	5024 E0DCh
E0h	32	ECAP_MUNIT_1_DEBUG_RANGE_MIN	5024 C0E0h	5024 D0E0h	5024 E0E0h
E4h	32	ECAP_MUNIT_1_DEBUG_RANGE_MAX	5024 C0E4h	5024 D0E4h	5024 E0E4h
100h	32	ECAP_MUNIT_2_CTL	5024 C100h	5024 D100h	5024 E100h

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Table 3-505. ECAP Registers, Base Address=5024 0000h, Length=256 (continued)

Offset	Length	Register Name	ECAP12 Physical Address	ECAP13 Physical Address	ECAP14 Physical Address
104h	32	ECAP_MUNIT_2_SHADOW_CTL	5024 C104h	5024 D104h	5024 E104h
110h	32	ECAP_MUNIT_2_MIN	5024 C110h	5024 D110h	5024 E110h
114h	32	ECAP_MUNIT_2_MAX	5024 C114h	5024 D114h	5024 E114h
118h	32	ECAP_MUNIT_2_MIN_SHADOW	5024 C118h	5024 D118h	5024 E118h
11Ch	32	ECAP_MUNIT_2_MAX_SHADOW	5024 C11Ch	5024 D11Ch	5024 E11Ch
120h	32	ECAP_MUNIT_2_DEBUG_RANGE_MIN	5024 C120h	5024 D120h	5024 E120h
124h	32	ECAP_MUNIT_2_DEBUG_RANGE_MAX	5024 C124h	5024 D124h	5024 E124h

Table 3-506. ECAP Registers, Base Address=5024 0000h, Length=256

Offset	Length	Register Name	ECAP15 Physical Address
0h	32	ECAP_TSCTR	5024 F000h
4h	32	ECAP_CTRPHS	5024 F004h
8h	32	ECAP_CAP1	5024 F008h
Ch	32	ECAP_CAP2	5024 F00Ch
10h	32	ECAP_CAP3	5024 F010h
14h	32	ECAP_CAP4	5024 F014h
24h	32	ECAP_ECCTL0	5024 F024h
28h	16	ECAP_ECCTL1	5024 F028h
2Ah	16	ECAP_ECCTL2	5024 F02Ah
2Ch	16	ECAP_ECEINT	5024 F02Ch
2Eh	16	ECAP_ECFLG	5024 F02Eh
30h	16	ECAP_ECCLR	5024 F030h
32h	16	ECAP_ECFRC	5024 F032h
3Ch	32	ECAP_ECAPSYNCINSEL	5024 F03Ch
80h	32	ECAP_MUNIT_COMMON_CTL	5024 F080h
C0h	32	ECAP_MUNIT_1_CTL	5024 F0C0h
C4h	32	ECAP_MUNIT_1_SHADOW_CTL	5024 F0C4h
D0h	32	ECAP_MUNIT_1_MIN	5024 F0D0h
D4h	32	ECAP_MUNIT_1_MAX	5024 F0D4h
D8h	32	ECAP_MUNIT_1_MIN_SHADOW	5024 F0D8h
DCh	32	ECAP_MUNIT_1_MAX_SHADOW	5024 F0DCh
E0h	32	ECAP_MUNIT_1_DEBUG_RANGE_MIN	5024 F0E0h
E4h	32	ECAP_MUNIT_1_DEBUG_RANGE_MAX	5024 F0E4h
100h	32	ECAP_MUNIT_2_CTL	5024 F100h
104h	32	ECAP_MUNIT_2_SHADOW_CTL	5024 F104h
110h	32	ECAP_MUNIT_2_MIN	5024 F110h
114h	32	ECAP_MUNIT_2_MAX	5024 F114h
118h	32	ECAP_MUNIT_2_MIN_SHADOW	5024 F118h
11Ch	32	ECAP_MUNIT_2_MAX_SHADOW	5024 F11Ch
120h	32	ECAP_MUNIT_2_DEBUG_RANGE_MIN	5024 F120h
124h	32	ECAP_MUNIT_2_DEBUG_RANGE_MAX	5024 F124h

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3.7.2 ECAP Registers

ECAP Registers

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3.7.2.1 ECAP_TSCTR Register

3.7.2.1.1 ECAP_TSCTR Register (Offset = 0h) [reset = 0h]

Time-Stamp Counter.

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Table 3-507. Instance Table

Instance Name	Physical Address
ECAP00	5024 0000h
ECAP01	5024 1000h
ECAP02	5024 2000h
ECAP03	5024 3000h
ECAP04	5024 4000h
ECAP05	5024 5000h
ECAP06	5024 6000h
ECAP07	5024 7000h
ECAP08	5024 8000h
ECAP09	5024 9000h
ECAP10	5024 A000h
ECAP11	5024 B000h
ECAP12	5024 C000h
ECAP13	5024 D000h
ECAP14	5024 E000h
ECAP15	5024 F000h

Figure 3-242. ECAP_TSCTR Name Register

31	30	29	28	27	26	25	24
TSCTR							
R/W							
0h							
23	22	21	20	19	18	17	16
TSCTR							
R/W							
0h							
15	14	13	12	11	10	9	8
TSCTR							
R/W							
0h							
7	6	5	4	3	2	1	0
TSCTR							
R/W							
0h							

Table 3-508. ECAP_TSCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSCTR	R/W	0h	Active 32-bit counter register that is used as the capture time-base HR mode : 1] This register reads HRCOUNTER value and is not writable 2] can be reset using CTRFILTRESET 3] Its not synchronized to SYSCLK domain so reads may not be accurate

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3.7.2.2 ECAP_CTRPHS Register

3.7.2.2.1 ECAP_CTRPHS Register (Offset = 4h) [reset = 0h]

Counter Phase Offset Value Register.

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Table 3-509. Instance Table

Instance Name	Physical Address
ECAP00	5024 0004h
ECAP01	5024 1004h
ECAP02	5024 2004h
ECAP03	5024 3004h
ECAP04	5024 4004h
ECAP05	5024 5004h
ECAP06	5024 6004h
ECAP07	5024 7004h
ECAP08	5024 8004h
ECAP09	5024 9004h
ECAP10	5024 A004h
ECAP11	5024 B004h
ECAP12	5024 C004h
ECAP13	5024 D004h
ECAP14	5024 E004h
ECAP15	5024 F004h

Figure 3-243. ECAP_CTRPHS Name Register

31	30	29	28	27	26	25	24
CTRPHS							
R/W							
0h							
23	22	21	20	19	18	17	16
CTRPHS							
R/W							
0h							
15	14	13	12	11	10	9	8
CTRPHS							
R/W							
0h							
7	6	5	4	3	2	1	0
CTRPHS							
R/W							
0h							

Table 3-510. ECAP_CTRPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CTRPHS	R/W	0h	Counter phase value register that can be programmed for phase lag/lead. This register CTRPHS is loaded into TSCTR upon either a SYNCI event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and EPWM time-bases. This register is not applicable in HR mode.

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3.7.2.3 ECAP_CAP1 Register

3.7.2.3.1 ECAP_CAP1 Register (Offset = 8h) [reset = 0h]

Capture 1 Register.

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Table 3-511. Instance Table

Instance Name	Physical Address
ECAP00	5024 0008h
ECAP01	5024 1008h
ECAP02	5024 2008h
ECAP03	5024 3008h
ECAP04	5024 4008h
ECAP05	5024 5008h
ECAP06	5024 6008h
ECAP07	5024 7008h
ECAP08	5024 8008h
ECAP09	5024 9008h
ECAP10	5024 A008h
ECAP11	5024 B008h
ECAP12	5024 C008h
ECAP13	5024 D008h
ECAP14	5024 E008h
ECAP15	5024 F008h

Figure 3-244. ECAP_CAP1 Name Register

31	30	29	28	27	26	25	24
CAP1							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP1							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP1							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP1							
R/W							
0h							

Table 3-512. ECAP_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP1	R/W	0h	This register can be loaded (written) by: 1. Time-Stamp (counter value) during a capture event. 2. Software - may be useful for test purposes/initialization. 3. APRD shadow register (ECAP_CAP3) when used in APWM mode.

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3.7.2.4 ECAP_CAP2 Register

3.7.2.4.1 ECAP_CAP2 Register (Offset = Ch) [reset = 0h]

Capture 2 Register.

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Table 3-513. Instance Table

Instance Name	Physical Address
ECAP00	5024 000Ch
ECAP01	5024 100Ch
ECAP02	5024 200Ch
ECAP03	5024 300Ch
ECAP04	5024 400Ch
ECAP05	5024 500Ch
ECAP06	5024 600Ch
ECAP07	5024 700Ch
ECAP08	5024 800Ch
ECAP09	5024 900Ch
ECAP10	5024 A00Ch
ECAP11	5024 B00Ch
ECAP12	5024 C00Ch
ECAP13	5024 D00Ch
ECAP14	5024 E00Ch
ECAP15	5024 F00Ch

Figure 3-245. ECAP_CAP2 Name Register

31	30	29	28	27	26	25	24
CAP2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CAP2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CAP2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAP2							
R/W							
0h							

Table 3-514. ECAP_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP2	R/W	0h	This register can be loaded (written) by: 1. Time-Stamp (counter value) during a capture event. 2. Software - may be useful for test purposes. 3. ACMP shadow register (ECAP_CAP4) when used in APWM mode.

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3.7.2.5 ECAP_CAP3 Register

3.7.2.5.1 ECAP_CAP3 Register (Offset = 10h) [reset = 0h]

Capture 3 Register.

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Table 3-515. Instance Table

Instance Name	Physical Address
ECAP00	5024 0010h
ECAP01	5024 1010h
ECAP02	5024 2010h
ECAP03	5024 3010h
ECAP04	5024 4010h
ECAP05	5024 5010h
ECAP06	5024 6010h
ECAP07	5024 7010h
ECAP08	5024 8010h
ECAP09	5024 9010h
ECAP10	5024 A010h
ECAP11	5024 B010h
ECAP12	5024 C010h
ECAP13	5024 D010h
ECAP14	5024 E010h
ECAP15	5024 F010h

Figure 3-246. ECAP_CAP3 Name Register

31	30	29	28	27	26	25	24
CAP3							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP3							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP3							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP3							
R/W							
0h							

Table 3-516. ECAP_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP3	R/W	0h	In CMP mode this is a time-stamp capture register. In APMW mode this is the period shadow (APER) register. User updates the PWM period value via this register. In this mode the ECAP_CAP3 (APRD) register shadows the ECAP_CAP1 register.

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3.7.2.6 ECAP_CAP4 Register

3.7.2.6.1 ECAP_CAP4 Register (Offset = 14h) [reset = 0h]

Capture 4 Register.

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Table 3-517. Instance Table

Instance Name	Physical Address
ECAP00	5024 0014h
ECAP01	5024 1014h
ECAP02	5024 2014h
ECAP03	5024 3014h
ECAP04	5024 4014h
ECAP05	5024 5014h
ECAP06	5024 6014h
ECAP07	5024 7014h
ECAP08	5024 8014h
ECAP09	5024 9014h
ECAP10	5024 A014h
ECAP11	5024 B014h
ECAP12	5024 C014h
ECAP13	5024 D014h
ECAP14	5024 E014h
ECAP15	5024 F014h

Figure 3-247. ECAP_CAP4 Name Register

31	30	29	28	27	26	25	24
CAP4							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP4							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP4							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP4							
R/W							
0h							

Table 3-518. ECAP_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP4	R/W	0h	In CMP mode this is a time-stamp capture register. In APMW mode this is the compare shadow (ACMP) register. User updates the PWM Compare value via this register. In this mode the ECAP_CAP4 (ACMP) register shadows the ECAP_CAP2 register.

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3.7.2.7 ECAP_ECCTL0 Register

3.7.2.7.1 ECAP_ECCTL0 Register (Offset = 24h) [reset = FFh]

Capture Control Register 0

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Table 3-519. Instance Table

Instance Name	Physical Address
ECAP00	5024 0024h
ECAP01	5024 1024h
ECAP02	5024 2024h
ECAP03	5024 3024h
ECAP04	5024 4024h
ECAP05	5024 5024h
ECAP06	5024 6024h
ECAP07	5024 7024h
ECAP08	5024 8024h
ECAP09	5024 9024h
ECAP10	5024 A024h
ECAP11	5024 B024h
ECAP12	5024 C024h
ECAP13	5024 D024h
ECAP14	5024 E024h
ECAP15	5024 F024h

Figure 3-248. ECAP_ECCTL0 Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2						SOCEVTSEL	
R						R/W	
0h						0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
QUALPRD				RESERVED_1			
R/W				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INPUTSEL							
R/W							
FFh							

Table 3-520. ECAP_ECCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_2	R	0h	Reserved

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Table 3-520. ECAP_ECCTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:16	SOCEVTSEL	R/W	0h	ADC SOC event select Capture Mode: 00b[R/W] = SOC trigger source is CEVT1 01b[R/W] = SOC trigger source is CEVT2 10b[R/W] = SOC trigger source is CEVT3 11b[R/W] = SOC trigger source is CEVT4 APWM Mode: 00b[R/W] = SOC trigger interrupt source is period match 01b[R/W] = SOC trigger interrupt source is compare match 10b[R/W] = SOC trigger interrupt source is period match or compare match 11b[R/W] = Disabled
15:12	QUALPRD	R/W	0h	Qual period to filter out noise on input signals being monitored, Not applicable for HR mode. 0x0 : Bypass 0x1 : pulses of with 1 cycle or less will be filtered out 0x2 : pulses of with 2 cycles or less will be filtered out .... 0xF : pulses of with 15 cycles or less will be filtered out
11:8	RESERVED_1	R	0h	Reserved
7:0	INPUTSEL	R/W	FFh	Capture input source select bits 0x0 capture input is ECAPxINPUT[0] 0x1 capture input is ECAPxINPUT[1] 0x2 capture input is ECAPxINPUT[2] ... 0xFF capture input is ECAPxINPUT[256]

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3.7.2.8 ECAP_ECCTL1 Register

3.7.2.8.1 ECAP_ECCTL1 Register (Offset = 28h) [reset = 0h]

Capture Control Register 1

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Table 3-521. Instance Table

Instance Name	Physical Address
ECAP00	5024 0028h
ECAP01	5024 1028h
ECAP02	5024 2028h
ECAP03	5024 3028h
ECAP04	5024 4028h
ECAP05	5024 5028h
ECAP06	5024 6028h
ECAP07	5024 7028h
ECAP08	5024 8028h
ECAP09	5024 9028h
ECAP10	5024 A028h
ECAP11	5024 B028h
ECAP12	5024 C028h
ECAP13	5024 D028h
ECAP14	5024 E028h
ECAP15	5024 F028h

Figure 3-249. ECAP_ECCTL1 Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PRESCALE					CAPLDEN
R/W		R/W					R/W
0h		0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-522. ECAP_ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation Control 0 TSCTR counter stops immediately on emulation suspend 1 TSCTR counter runs until = 0 2 TSCTR counter is unaffected by emulation suspend (Run Free) 3 TSCTR counter is unaffected by emulation suspend (Run Free)
13:9	PRESCALE	R/W	0h	Event Filter prescale select 0 Divide by 1 (i.e,. no prescale, by-pass the prescaler) 1 Divide by 2 2 Divide by 4 3 Divide by 6 4 Divide by 8 5 Divide by 10 30 Divide by 60 31 Divide by 62

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Table 3-522. ECAP_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CAPLDEN	R/W	0h	Enable Loading of CAP1-4 registers on a capture event. Note that this bit does not disable CEVTn events from being generated. 0 Disable CAP1-4 register loads at capture event time. 1 Enable CAP1-4 register loads at capture event time.
7	CTRRST4	R/W	0h	Counter Reset on Capture Event 4 0 Do not reset counter on Capture Event 4 (absolute time stamp operation) 1 Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	R/W	0h	Capture Event 4 Polarity select 0 Capture Event 4 triggered on a rising edge (RE) 1 Capture Event 4 triggered on a falling edge (FE)
5	CTRRST3	R/W	0h	Counter Reset on Capture Event 3 0 Do not reset counter on Capture Event 3 (absolute time stamp) 1 Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture Event 3 Polarity select 0 Capture Event 3 triggered on a rising edge (RE) 1 Capture Event 3 triggered on a falling edge (FE)
3	CTRRST2	R/W	0h	Counter Reset on Capture Event 2 0 Do not reset counter on Capture Event 2 (absolute time stamp) 1 Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture Event 2 Polarity select 0 Capture Event 2 triggered on a rising edge (RE) 1 Capture Event 2 triggered on a falling edge (FE)
1	CTRRST1	R/W	0h	Counter Reset on Capture Event 1 0 Do not reset counter on Capture Event 1 (absolute time stamp) 1 Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	R/W	0h	Capture Event 1 Polarity select 0 Capture Event 1 triggered on a rising edge (RE) 1 Capture Event 1 triggered on a falling edge (FE)

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3.7.2.9 ECAP_ECCTL2 Register

3.7.2.9.1 ECAP_ECCTL2 Register (Offset = 2Ah) [reset = 6h]

Capture Control Register 2

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Table 3-523. Instance Table

Instance Name	Physical Address
ECAP00	5024 002Ah
ECAP01	5024 102Ah
ECAP02	5024 202Ah
ECAP03	5024 302Ah
ECAP04	5024 402Ah
ECAP05	5024 502Ah
ECAP06	5024 602Ah
ECAP07	5024 702Ah
ECAP08	5024 802Ah
ECAP09	5024 902Ah
ECAP10	5024 A02Ah
ECAP11	5024 B02Ah
ECAP12	5024 C02Ah
ECAP13	5024 D02Ah
ECAP14	5024 E02Ah
ECAP15	5024 F02Ah

Figure 3-250. ECAP_ECCTL2 Name Register

15	14	13	12	11	10	9	8
MODCNTRSTS		DMAEVTSEL		CTRFILTRESET	APWMPOL	CAP_APWM	SWSYNC
R/W		R/W		R/W1TC	R/W	R/W	R/W1TS
0h		0h		0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYNCO_SEL		SYNCI_EN	TSCTRSTOP	REARM	STOP_WRAP		CONT_ONESHT
R/W		R/W	R/W	R/W1TS	R/W		R/W
0h		0h	0h	0h	3h		0h

Table 3-524. ECAP_ECCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	MODCNTRSTS	R/W	0h	This bit field reads current status on modulo counter 00b[R] = CAP1 register gets loaded on next capture event. 01b[R] = CAP2 register gets loaded on next capture event. 10b[R] = CAP3 register gets loaded on next capture event. 11b[R] = CAP4 register gets loaded on next capture event.
13:12	DMAEVTSEL	R/W	0h	DMA event select Capture Mode: 00b[R/W] = DMA interrupt source is CEVT1 01b[R/W] = DMA interrupt source is CEVT2 10b[R/W] = DMA interrupt source is CEVT3 11b[R/W] = DMA interrupt source is CEVT4 APWM Mode: 00b[R/W] = DMA interrupt source is period match 01b[R/W] = DMA interrupt source is compare match 10b[R/W] = DMA interrupt source is period match or compare match 11b[R/W] = Disabled

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Table 3-524. ECAP_ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CTRFILTRESET	R/W1TC	0h	Reset Bit 0h[R] = No effect 1h[W] = Resets event filter, counter, modulo counter and CEVT[1,2,3,4] and CNTOVF , HRERROR flags Note: This provides an ability start capture module from known state in case spurious inputs are captured while ECAP is configured.
10	APWMPOL	R/W	0h	APWM output polarity select. This is applicable only in APWM operating mode. 0 Output is active high (Compare value defines high time) 1 Output is active low (Compare value defines low time)
9	CAP_APWM	R/W	0h	CAP/APWM operating mode select 0 ECAP module operates in capture mode. This mode forces the following configuration: - Inhibits TSCTR resets via CTR = PRD event - Inhibits shadow loads on CAP1 and 2 registers - Permits user to enable CAP1-4 register load - CAPx/APWMx pin operates as a capture input 1 ECAP module operates in APWM mode. This mode forces the following configuration: - Resets TSCTR on CTR = PRD event (period boundary) - Permits shadow loading on CAP1 and 2 registers - Disables loading of time-stamps into CAP1-4 registers - CAPx/APWMx pin operates as a APWM output
8	SWSYNC	R/W1TS	0h	Software-forced Counter [TSCTR] Synchronizer. This provides the user a method to generate a synchronization pulse through software. In APWM mode, the synchronization pulse can also be sourced from the CTR = PRD event. 0 Writing a zero has no effect. Reading always returns a zero 1 Writing a one forces a TSCTR shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0,0. After writing a 1, this bit returns to a zero. Note: Selection CTR = PRD is meaningful only in APWM mode; however, you can choose it in CAP mode if you find doing so useful.
7:6	SYNCO_SEL	R/W	0h	Sync-Out Select 0 sync out signal is SWSYNC 1 Select CTR = PRD event to be the sync-out signal 3 Disable sync out signal
5	SYNCI_EN	R/W	0h	Counter [TSCTR] Sync-In select mode 0 Disable sync-in option 1 Enable counter (TSCTR) to be loaded from CTRPHS register upon either a SYNCI signal or a S/W force event.
4	TSCTRSTOP	R/W	0h	Time Stamp [TSCTR] Counter Stop [freeze] Control 0 TSCTR stopped 1 TSCTR free-running
3	REARM	R/W1TS	0h	Re-Arming Control. Note: The re-arm function is valid in one shot or continuous mode 0 Has no effect (reading always returns a 0) 1 Arms the one-shot sequence as follows: (1) Resets the Mod4 counter to zero (2) Unfreezes the Mod4 counter (3) Enables capture register loads

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Table 3-524. ECAP_ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:1	STOP_WRAP	R/W	3h	Stop value for one-shot mode. This is the number [between 1-4] of captures allowed to occur before the CAP[1-4] registers are frozen, that is, capture sequence is stopped. Wrap value for continuous mode. This is the number [between 1-4] of the capture register in which the circular buffer wraps around and starts again. Notes: STOP_WRAP is compared to Mod4 counter and, when equal, 2 actions occur: - Mod4 counter is stopped [frozen] - Capture register loads are inhibited In one-shot mode, further interrupt events are blocked until re-armed. 0 Stop after Capture Event 1 in one-shot mode Wrap after Capture Event 1 in continuous mode. 1 Stop after Capture Event 2 in one-shot mode Wrap after Capture Event 2 in continuous mode. 2 Stop after Capture Event 3 in one-shot mode Wrap after Capture Event 3 in continuous mode. 3 Stop after Capture Event 4 in one-shot mode Wrap after Capture Event 4 in continuous mode.
0	CONT_ONESHT	R/W	0h	Continuous or one-shot mode control [applicable only in capture mode] 0 Operate in continuous mode 1 Operate in one-Shot mode

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3.7.2.10 ECAP_ECEINT Register

3.7.2.10.1 ECAP_ECEINT Register (Offset = 2Ch) [reset = 0h]

The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ECCLR registers.
The proper procedure for configuring peripheral modes and interrupts is as follows:
- Disable global interrupts
- Stop eCAP counter
- Disable eCAP interrupts
- Configure peripheral registers
- Clear spurious eCAP interrupt flags
- Enable eCAP interrupts
- Start eCAP counter
- Enable global interrupts.

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Table 3-525. Instance Table

Instance Name	Physical Address
ECAP00	5024 002Ch
ECAP01	5024 102Ch
ECAP02	5024 202Ch
ECAP03	5024 302Ch
ECAP04	5024 402Ch
ECAP05	5024 502Ch
ECAP06	5024 602Ch
ECAP07	5024 702Ch
ECAP08	5024 802Ch
ECAP09	5024 902Ch
ECAP10	5024 A02Ch
ECAP11	5024 B02Ch
ECAP12	5024 C02Ch
ECAP13	5024 D02Ch
ECAP14	5024 E02Ch
ECAP15	5024 F02Ch

Figure 3-251. ECAP_ECEINT Name Register

15	14	13	12	11	10	9	8
RESERVED_2			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTR_EQ_CMP	CTR_EQ_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-526. ECAP_ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12	MUNIT_2_ERROR_EVT2	R/W	0h	Monitoring unit 2 error event 2 interrupt enable 0 : Disable Monitoring unit 2 error event 2 interrupt 1 : Enable Monitoring unit 2 error event 2 interrupt

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Table 3-526. ECAP_ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	MUNIT_2_ERROR_EVT1	R/W	0h	Monitoring unit 2 error event 2 interrupt enable 0 : Disable Monitoring unit 2 error event 1 interrupt 1 : Enable Monitoring unit 2 error event 1 interrupt
10	MUNIT_1_ERROR_EVT2	R/W	0h	Monitoring unit 1 error event 1 interrupt enable 0 : Disable Monitoring unit 1 error event 2 interrupt 1 : Enable Monitoring unit 1 error event 2 interrupt
9	MUNIT_1_ERROR_EVT1	R/W	0h	Monitoring unit 1 error event 1 interrupt enable 0 : Disable Monitoring unit 1 error event 1 interrupt 1 : Enable Monitoring unit 1 error event 1 interrupt
8	HRERROR	R/W	0h	High resolution error interrupt enable 0 Disable High Resolution Error as an Interrupt source 1 Enable High Resolution Error as an Interrupt source
7	CTR_EQ_CMP	R/W	0h	Counter Equal Compare Interrupt Enable 0 Disable Compare Equal as an Interrupt source 1 Enable Compare Equal as an Interrupt source
6	CTR_EQ_PRD	R/W	0h	Counter Equal Period Interrupt Enable 0 Disable Period Equal as an Interrupt source 1 Enable Period Equal as an Interrupt source
5	CTROVF	R/W	0h	Counter Overflow Interrupt Enable 0 Disabled counter Overflow as an Interrupt source 1 Enable counter Overflow as an Interrupt source
4	CEVT4	R/W	0h	Capture Event 4 Interrupt Enable 0 Disable Capture Event 4 as an Interrupt source 1 Capture Event 4 Interrupt Enable
3	CEVT3	R/W	0h	Capture Event 3 Interrupt Enable 0 Disable Capture Event 3 as an Interrupt source 1 Enable Capture Event 3 as an Interrupt source
2	CEVT2	R/W	0h	Capture Event 2 Interrupt Enable 0 Disable Capture Event 2 as an Interrupt source 1 Enable Capture Event 2 as an Interrupt source
1	CEVT1	R/W	0h	Capture Event 1 Interrupt Enable 0 Disable Capture Event 1 as an Interrupt source 1 Enable Capture Event 1 as an Interrupt source
0	RESERVED_1	R	0h	Reserved

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3.7.2.11 ECAP_ECFLG Register

3.7.2.11.1 ECAP_ECFLG Register (Offset = 2Eh) [reset = 0h]

Capture Interrupt Flag Register.

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Table 3-527. Instance Table

Instance Name	Physical Address
ECAP00	5024 002Eh
ECAP01	5024 102Eh
ECAP02	5024 202Eh
ECAP03	5024 302Eh
ECAP04	5024 402Eh
ECAP05	5024 502Eh
ECAP06	5024 602Eh
ECAP07	5024 702Eh
ECAP08	5024 802Eh
ECAP09	5024 902Eh
ECAP10	5024 A02Eh
ECAP11	5024 B02Eh
ECAP12	5024 C02Eh
ECAP13	5024 D02Eh
ECAP14	5024 E02Eh
ECAP15	5024 F02Eh

Figure 3-252. ECAP_ECFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_1			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-528. ECAP_ECFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	MUNIT_2_ERROR_EVT2	R	0h	Error event 2 Interrupt Flag from monitoring unit 2
11	MUNIT_2_ERROR_EVT1	R	0h	Error event 2 Interrupt Flag from monitoring unit 2
10	MUNIT_1_ERROR_EVT2	R	0h	Error event 2 Interrupt Flag from monitoring unit 1
9	MUNIT_1_ERROR_EVT1	R	0h	Error event 2 Interrupt Flag from monitoring unit 1
8	HRERROR	R	0h	High resolution error status flag 0 Indicates no event occurred 1 Indicates the High resolution Error occurred

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Table 3-528. ECAP_ECFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CTR_CMP	R	0h	Compare Equal Compare Status Flag. This flag is active only in APWM mode. 0 Indicates no event occurred 1 Indicates the counter (TSCTR) reached the compare register value (ACMP)
6	CTR_PRD	R	0h	Counter Equal Period Status Flag. This flag is only active in APWM mode. 0 Indicates no event occurred 1 Indicates the counter (TSCTR) reached the period register value (APRD) and was reset.
5	CTROVF	R	0h	Counter Overflow Status Flag. This flag is active in CAP and APWM mode. 0 Indicates no event occurred 1 Indicates the counter (TSCTR) has made the transition from FFFFFFFF to 00000000
4	CEVT4	R	0h	Capture Event 4 Status Flag This flag is only active in CAP mode. 0 Indicates no event occurred 1 Indicates the fourth event occurred at ECAPx pin
3	CEVT3	R	0h	Capture Event 3 Status Flag. This flag is active only in CAP mode. 0 Indicates no event occurred 1 Indicates the third event occurred at ECAPx pin.
2	CEVT2	R	0h	Capture Event 2 Status Flag. This flag is only active in CAP mode. 0 Indicates no event occurred 1 Indicates the second event occurred at ECAPx pin.
1	CEVT1	R	0h	Capture Event 1 Status Flag. This flag is only active in CAP mode. 0 Indicates no event occurred 1 Indicates the first event occurred at ECAPx pin.
0	INT	R	0h	Global Interrupt Status Flag 0 Indicates no event occurred 1 Indicates that an interrupt was generated.

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3.7.2.12 ECAP_ECCLR Register

3.7.2.12.1 ECAP_ECCLR Register (Offset = 30h) [reset = 0h]

Capture Interrupt Clear Register.

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Table 3-529. Instance Table

Instance Name	Physical Address
ECAP00	5024 0030h
ECAP01	5024 1030h
ECAP02	5024 2030h
ECAP03	5024 3030h
ECAP04	5024 4030h
ECAP05	5024 5030h
ECAP06	5024 6030h
ECAP07	5024 7030h
ECAP08	5024 8030h
ECAP09	5024 9030h
ECAP10	5024 A030h
ECAP11	5024 B030h
ECAP12	5024 C030h
ECAP13	5024 D030h
ECAP14	5024 E030h
ECAP15	5024 F030h

Figure 3-253. ECAP_ECCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
R			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-530. ECAP_ECCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	MUNIT_2_ERROR_EVT2	R/W1TC	0h	Writing '1' clears MUNIT_2_ERROR_EVT2 interrupt flag
11	MUNIT_2_ERROR_EVT1	R/W1TC	0h	Writing '1' clears MUNIT_2_ERROR_EVT1 interrupt flag
10	MUNIT_1_ERROR_EVT2	R/W1TC	0h	Writing '1' clears MUNIT_1_ERROR_EVT2 interrupt flag
9	MUNIT_1_ERROR_EVT1	R/W1TC	0h	Writing '1' clears MUNIT_1_ERROR_EVT1 interrupt flag
8	HRERROR	R/W1TC	0h	High resolution error status Clear 0 Writing a 0 has no effect. Always reads back a 0 1 Writing a 1 clears the HRERROR flag.
7	CTR_CMP	R/W1TC	0h	Counter Equal Compare Status Clear 0 Writing a 0 has no effect. Always reads back a 0 1 Writing a 1 clears the CTR=CMP flag.

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Table 3-530. ECAP_ECCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CTR_PRD	R/W1TC	0h	Counter Equal Period Status Clear 0 `Writing a 0 has no effect. Always reads back a 0` 1 `Writing a 1 clears the CTR=PRD flag.`
5	CTROVF	R/W1TC	0h	Counter Overflow Status Clear 0 `Writing a 0 has no effect. Always reads back a 0` 1 `Writing a 1 clears the CTROVF flag.`
4	CEVT4	R/W1TC	0h	Capture Event 4 Status Clear 0 `Writing a 0 has no effect. Always reads back a 0` 1 `Writing a 1 clears the CEVT4 flag.`
3	CEVT3	R/W1TC	0h	Capture Event 3 Status Clear 0 `Writing a 0 has no effect. Always reads back a 0` 1 `Writing a 1 clears the CEVT3 flag.`
2	CEVT2	R/W1TC	0h	Capture Event 2 Status Clear 0 `Writing a 0 has no effect. Always reads back a 0` 1 `Writing a 1 clears the CEVT2 flag.`
1	CEVT1	R/W1TC	0h	Capture Event 1 Status Clear 0 `Writing a 0 has no effect. Always reads back a 0` 1 `Writing a 1 clears the CEVT1 flag.`
0	INT	R/W1TC	0h	ECAP Global Interrupt Status Clear 0 `Writing a 0 has no effect. Always reads back a 0` 1 `Writing a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1`

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3.7.2.13 ECAP_ECFRC Register

3.7.2.13.1 ECAP_ECFRC Register (Offset = 32h) [reset = 0h]

Capture Interrupt Force Register.

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Table 3-531. Instance Table

Instance Name	Physical Address
ECAP00	5024 0032h
ECAP01	5024 1032h
ECAP02	5024 2032h
ECAP03	5024 3032h
ECAP04	5024 4032h
ECAP05	5024 5032h
ECAP06	5024 6032h
ECAP07	5024 7032h
ECAP08	5024 8032h
ECAP09	5024 9032h
ECAP10	5024 A032h
ECAP11	5024 B032h
ECAP12	5024 C032h
ECAP13	5024 D032h
ECAP14	5024 E032h
ECAP15	5024 F032h

Figure 3-254. ECAP_ECFRC Name Register

15	14	13	12	11	10	9	8
RESERVED_2			MUNIT_2_ERROR_EVT2	MUNIT_2_ERROR_EVT1	MUNIT_1_ERROR_EVT2	MUNIT_1_ERROR_EVT1	HRERROR
R			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTR_CMP	CTR_PRD	CTROVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED_1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-532. ECAP_ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12	MUNIT_2_ERROR_EVT2	R/W1TS	0h	Writing '1' sets MUNIT_2_ERROR_EVT2 interrupt flag
11	MUNIT_2_ERROR_EVT1	R/W1TS	0h	Writing '1' sets MUNIT_2_ERROR_EVT1 interrupt flag
10	MUNIT_1_ERROR_EVT2	R/W1TS	0h	Writing '1' sets MUNIT_1_ERROR_EVT2 interrupt flag
9	MUNIT_1_ERROR_EVT1	R/W1TS	0h	Writing '1' sets MUNIT_1_ERROR_EVT1 interrupt flag
8	HRERROR	R/W1TS	0h	High resolution error Force interrupt 0 No effect. Always reads back a 0. 1 Writing a 1 sets the CTR_CMP flag.
7	CTR_CMP	R/W1TS	0h	Force Counter Equal Compare Interrupt. This event is only active in APWM mode. 0 No effect. Always reads back a 0. 1 Writing a 1 sets the CTR_CMP flag.

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Table 3-532. ECAP_ECFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CTR_PRD	R/W1TS	0h	Force Counter Equal Period Interrupt. This event is only active in APWM mode. 0 No effect. Always reads back a 0. 1 Writing a 1 sets the CTR_PRD flag.
5	CTROVF	R/W1TS	0h	Force Counter Overflow 0 No effect. Always reads back a 0. 1 Writing a 1 to this bit sets the CTROVF flag.
4	CEVT4	R/W1TS	0h	Force Capture Event 4. This event is only active in CAP mode. 0 No effect. Always reads back a 0. 1 Writing a 1 sets the CEVT4 flag.
3	CEVT3	R/W1TS	0h	Force Capture Event 3. This event is only active in CAP mode. 0 No effect. Always reads back a 0. 1 Writing a 1 sets the CEVT3 flag.
2	CEVT2	R/W1TS	0h	Force Capture Event 2. This event is only active in CAP mode. 0 No effect. Always reads back a 0. 1 Writing a 1 sets the CEVT2 flag.
1	CEVT1	R/W1TS	0h	Force Capture Event 1. This event is only active in CAP mode. 0 No effect. Always reads back a 0. 1 Sets the CEVT1 flag.
0	RESERVED_1	R	0h	Reserved

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3.7.2.14 ECAP_ECAPSYNCINSEL Register

3.7.2.14.1 ECAP_ECAPSYNCINSEL Register (Offset = 3Ch) [reset = 1h]

SYNC source select register.

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Table 3-533. Instance Table

Instance Name	Physical Address
ECAP00	5024 003Ch
ECAP01	5024 103Ch
ECAP02	5024 203Ch
ECAP03	5024 303Ch
ECAP04	5024 403Ch
ECAP05	5024 503Ch
ECAP06	5024 603Ch
ECAP07	5024 703Ch
ECAP08	5024 803Ch
ECAP09	5024 903Ch
ECAP10	5024 A03Ch
ECAP11	5024 B03Ch
ECAP12	5024 C03Ch
ECAP13	5024 D03Ch
ECAP14	5024 E03Ch
ECAP15	5024 F03Ch

Figure 3-255. ECAP_ECAPSYNCINSEL Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	SEL						
R	R/W						
0h	1h						

Table 3-534. ECAP_ECAPSYNCINSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_1	R	0h	Reserved

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Table 3-534. ECAP_ECAPSYNCINSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	SEL	R/W	1h	These bits determine the source of SYNCIN signal. 0x0 : Reserved. 0x1: EPWM0.SYNCOUT 0x1: EPWM1.SYNCOUT 0x3: EPWM2.SYNCOUT ... 0x32: EPWM31.SYNCOUT 0x33-0x128: Reserved

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3.7.2.15 ECAP_MUNIT_COMMON_CTL Register

3.7.2.15.1 ECAP_MUNIT_COMMON_CTL Register (Offset = 80h) [reset = 0h]

Control registers for monitoring unit {#}

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Table 3-535. Instance Table

Instance Name	Physical Address
ECAP00	5024 0080h
ECAP01	5024 1080h
ECAP02	5024 2080h
ECAP03	5024 3080h
ECAP04	5024 4080h
ECAP05	5024 5080h
ECAP06	5024 6080h
ECAP07	5024 7080h
ECAP08	5024 8080h
ECAP09	5024 9080h
ECAP10	5024 A080h
ECAP11	5024 B080h
ECAP12	5024 C080h
ECAP13	5024 D080h
ECAP14	5024 E080h
ECAP15	5024 F080h

Figure 3-256. ECAP_MUNIT_COMMON_CTL Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2	GLDSTRBSEL						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	TRIPSEL						
R	R/W						
0h	0h						

Table 3-536. ECAP_MUNIT_COMMON_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15	RESERVED_2	R	0h	Reserved
14:8	GLDSTRBSEL	R/W	0h	Global load strobe select to enable shadow to active loading 0x0 : Reserved. 0x1 to 0x7F : Global load strobe from SOC level including EPWM global load strobes.

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Table 3-536. ECAP_MUNIT_COMMON_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED_1	R	0h	Reserved
6:0	TRIPSEL	R/W	0h	Trip signal select to disable and enable signal monitoring automatically 0x0 : Disabled, Trip signals does not effect signal monitoring. 0x1 to 0x7F : Signal monioring is disabled when selected signal is high and enabled when it is low

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3.7.2.16 ECAP_MUNIT_1_CTL Register

3.7.2.16.1 ECAP_MUNIT_1_CTL Register (Offset = C0h) [reset = 0h]

Control registers for monitoring unit 1

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Table 3-537. Instance Table

Instance Name	Physical Address
ECAP00	5024 00C0h
ECAP01	5024 10C0h
ECAP02	5024 20C0h
ECAP03	5024 30C0h
ECAP04	5024 40C0h
ECAP05	5024 50C0h
ECAP06	5024 60C0h
ECAP07	5024 70C0h
ECAP08	5024 80C0h
ECAP09	5024 90C0h
ECAP10	5024 A0C0h
ECAP11	5024 B0C0h
ECAP12	5024 C0C0h
ECAP13	5024 D0C0h
ECAP14	5024 E0C0h
ECAP15	5024 F0C0h

Figure 3-257. ECAP_MUNIT_1_CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED_3</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED_2</td><td colspan="4">MON_SEL</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED_1</td><td>DEBUG_RANGE_EN</td><td>EN</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 3-538. ECAP_MUNIT_1_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:12	RESERVED_2	R	0h	Reserved

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Table 3-538. ECAP_MUNIT_1_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	MON_SEL	R/W	0h	Type of monitoring 0 : High Pulse width 1 : Low Pulse width 2 : Period width from Rise to Rise 3 : Period width from fall to fall 4 : Monitor rise edge 5 : Monitor fall edge 6 15 : Reserved [High Pulse width]
7:2	RESERVED_1	R	0h	Reserved
1	DEBUG_RANGE_EN	R/W	0h	Debug mode enable. 0 : Debug mode is disabled. 1 : Debug mode of monitoring unit 1 is enabled to obtain the variation seen in the system for debug purpose. Range is captured in MUNIT_1_DEBUG_RANGE_MIN and MUNIT_1_DEBUG_RANGE_MAX registers Toggle DEBUG_RANGE_EN to restart this process, this will initialize MUNIT_1_DEBUG_RANGE_MIN and MUNIT_1_DEBUG_RANGE_MAX registers.
0	EN	R/W	0h	0 : Monitoring unit 1 is disabled 1 : Monitoring unit 1 is enabled

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3.7.2.17 ECAP_MUNIT_1_SHADOW_CTL Register

3.7.2.17.1 ECAP_MUNIT_1_SHADOW_CTL Register (Offset = C4h) [reset = 0h]

Shadow control registers for monitoring unit 1

Return to Summary Table

Table 3-539. Instance Table

Instance Name	Physical Address
ECAP00	5024 00C4h
ECAP01	5024 10C4h
ECAP02	5024 20C4h
ECAP03	5024 30C4h
ECAP04	5024 40C4h
ECAP05	5024 50C4h
ECAP06	5024 60C4h
ECAP07	5024 70C4h
ECAP08	5024 80C4h
ECAP09	5024 90C4h
ECAP10	5024 A0C4h
ECAP11	5024 B0C4h
ECAP12	5024 C0C4h
ECAP13	5024 D0C4h
ECAP14	5024 E0C4h
ECAP15	5024 F0C4h

Figure 3-258. ECAP_MUNIT_1_SHADOW_CTL Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1					LOADMODE	SWSYNC	SYNCI_EN
R					R/W	R/W1TS	R/W
0h					0h	0h	0h

Table 3-540. ECAP_MUNIT_1_SHADOW_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_1	R	0h	Reserved
2	LOADMODE	R/W	0h	Load mode 0 : Active registers are loaded with shadow on next sync event 1 : Active registers are loaded with shadow on EPWMx.GLDLCSTRB event

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Table 3-540. ECAP_MUNIT_1_SHADOW_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SWSYNC	R/W1TS	0h	Copies Min and Max values from shadow to active registers immediately if MUNIT_1_SHADOW_CTL.SYNCI_EN is set.
0	SYNCI_EN	R/W	0h	Shadow Enable 0 : Disabled 1 : Enabled

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3.7.2.18 ECAP_MUNIT_1_MIN Register

3.7.2.18.1 ECAP_MUNIT_1_MIN Register (Offset = D0h) [reset = 0h]

Min value for monitoring unit 1

Return to Summary Table

Table 3-541. Instance Table

Instance Name	Physical Address
ECAP00	5024 00D0h
ECAP01	5024 10D0h
ECAP02	5024 20D0h
ECAP03	5024 30D0h
ECAP04	5024 40D0h
ECAP05	5024 50D0h
ECAP06	5024 60D0h
ECAP07	5024 70D0h
ECAP08	5024 80D0h
ECAP09	5024 90D0h
ECAP10	5024 A0D0h
ECAP11	5024 B0D0h
ECAP12	5024 C0D0h
ECAP13	5024 D0D0h
ECAP14	5024 E0D0h
ECAP15	5024 F0D0h

Figure 3-259. ECAP_MUNIT_1_MIN Name Register

31	30	29	28	27	26	25	24
MIN_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MIN_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MIN_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MIN_VALUE							
R/W							
0h							

Table 3-542. ECAP_MUNIT_1_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE	R/W	0h	Minimum value for monitoring

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3.7.2.19 ECAP_MUNIT_1_MAX Register

3.7.2.19.1 ECAP_MUNIT_1_MAX Register (Offset = D4h) [reset = 0h]

Max value for monitoring unit 1

Return to Summary Table

Table 3-543. Instance Table

Instance Name	Physical Address
ECAP00	5024 00D4h
ECAP01	5024 10D4h
ECAP02	5024 20D4h
ECAP03	5024 30D4h
ECAP04	5024 40D4h
ECAP05	5024 50D4h
ECAP06	5024 60D4h
ECAP07	5024 70D4h
ECAP08	5024 80D4h
ECAP09	5024 90D4h
ECAP10	5024 A0D4h
ECAP11	5024 B0D4h
ECAP12	5024 C0D4h
ECAP13	5024 D0D4h
ECAP14	5024 E0D4h
ECAP15	5024 F0D4h

Figure 3-260. ECAP_MUNIT_1_MAX Name Register

31	30	29	28	27	26	25	24
MAX_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MAX_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MAX_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MAX_VALUE							
R/W							
0h							

Table 3-544. ECAP_MUNIT_1_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE	R/W	0h	Maximum value for monitoring

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3.7.2.20 ECAP_MUNIT_1_MIN_SHADOW Register

3.7.2.20.1 ECAP_MUNIT_1_MIN_SHADOW Register (Offset = D8h) [reset = 0h]

Shadow register for Min value of monitoring unit 1

Return to Summary Table

Table 3-545. Instance Table

Instance Name	Physical Address
ECAP00	5024 00D8h
ECAP01	5024 10D8h
ECAP02	5024 20D8h
ECAP03	5024 30D8h
ECAP04	5024 40D8h
ECAP05	5024 50D8h
ECAP06	5024 60D8h
ECAP07	5024 70D8h
ECAP08	5024 80D8h
ECAP09	5024 90D8h
ECAP10	5024 A0D8h
ECAP11	5024 B0D8h
ECAP12	5024 C0D8h
ECAP13	5024 D0D8h
ECAP14	5024 E0D8h
ECAP15	5024 F0D8h

Figure 3-261. ECAP_MUNIT_1_MIN_SHADOW Name Register

31	30	29	28	27	26	25	24
MIN_VALUE_SHADOW							
R/W							
0h							
23	22	21	20	19	18	17	16
MIN_VALUE_SHADOW							
R/W							
0h							
15	14	13	12	11	10	9	8
MIN_VALUE_SHADOW							
R/W							
0h							
7	6	5	4	3	2	1	0
MIN_VALUE_SHADOW							
R/W							
0h							

Table 3-546. ECAP_MUNIT_1_MIN_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE_SHADOW	R/W	0h	Shadow minimum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

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3.7.2.21 ECAP_MUNIT_1_MAX_SHADOW Register

3.7.2.21.1 ECAP_MUNIT_1_MAX_SHADOW Register (Offset = DCh) [reset = 0h]

Shadow register for Max value of monitoring unit 1

Return to Summary Table

Table 3-547. Instance Table

Instance Name	Physical Address
ECAP00	5024 00DCh
ECAP01	5024 10DCh
ECAP02	5024 20DCh
ECAP03	5024 30DCh
ECAP04	5024 40DCh
ECAP05	5024 50DCh
ECAP06	5024 60DCh
ECAP07	5024 70DCh
ECAP08	5024 80DCh
ECAP09	5024 90DCh
ECAP10	5024 A0DCh
ECAP11	5024 B0DCh
ECAP12	5024 C0DCh
ECAP13	5024 D0DCh
ECAP14	5024 E0DCh
ECAP15	5024 F0DCh

Figure 3-262. ECAP_MUNIT_1_MAX_SHADOW Name Register

31	30	29	28	27	26	25	24
MAX_VALUE_SHADOW							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAX_VALUE_SHADOW							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAX_VALUE_SHADOW							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX_VALUE_SHADOW							
R/W							
0h							

Table 3-548. ECAP_MUNIT_1_MAX_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE_SHADOW	R/W	0h	Shadow maximum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

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3.7.2.22 ECAP_MUNIT_1_DEBUG_RANGE_MIN Register

3.7.2.22.1 ECAP_MUNIT_1_DEBUG_RANGE_MIN Register (Offset = E0h) [reset = FFFFFFFFh]

Observed Min value of check being enabled on minotoring unit 1

Return to Summary Table

Table 3-549. Instance Table

Instance Name	Physical Address
ECAP00	5024 00E0h
ECAP01	5024 10E0h
ECAP02	5024 20E0h
ECAP03	5024 30E0h
ECAP04	5024 40E0h
ECAP05	5024 50E0h
ECAP06	5024 60E0h
ECAP07	5024 70E0h
ECAP08	5024 80E0h
ECAP09	5024 90E0h
ECAP10	5024 A0E0h
ECAP11	5024 B0E0h
ECAP12	5024 C0E0h
ECAP13	5024 D0E0h
ECAP14	5024 E0E0h
ECAP15	5024 F0E0h

Figure 3-263. ECAP_MUNIT_1_DEBUG_RANGE_MIN Name Register

31	30	29	28	27	26	25	24
MIN_VALUE							
R							
FFFFFFFFh							
23	22	21	20	19	18	17	16
MIN_VALUE							
R							
FFFFFFFFh							
15	14	13	12	11	10	9	8
MIN_VALUE							
R							
FFFFFFFFh							
7	6	5	4	3	2	1	0
MIN_VALUE							
R							
FFFFFFFFh							

Table 3-550. ECAP_MUNIT_1_DEBUG_RANGE_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE	R	FFFFFFFFh	Observed Min value of check being enabled on minotoring unit 1. Is updated when MUNIT_1_CTL.DEBUG_RANGE_EN is set to '1'

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3.7.2.23 ECAP_MUNIT_1_DEBUG_RANGE_MAX Register

3.7.2.23.1 ECAP_MUNIT_1_DEBUG_RANGE_MAX Register (Offset = E4h) [reset = 0h]

Observed Max value of check being enabled on minotoring unit 1

Return to Summary Table

Table 3-551. Instance Table

Instance Name	Physical Address
ECAP00	5024 00E4h
ECAP01	5024 10E4h
ECAP02	5024 20E4h
ECAP03	5024 30E4h
ECAP04	5024 40E4h
ECAP05	5024 50E4h
ECAP06	5024 60E4h
ECAP07	5024 70E4h
ECAP08	5024 80E4h
ECAP09	5024 90E4h
ECAP10	5024 A0E4h
ECAP11	5024 B0E4h
ECAP12	5024 C0E4h
ECAP13	5024 D0E4h
ECAP14	5024 E0E4h
ECAP15	5024 F0E4h

Figure 3-264. ECAP_MUNIT_1_DEBUG_RANGE_MAX Name Register

31	30	29	28	27	26	25	24
MAX_VALUE							
R							
0h							
23	22	21	20	19	18	17	16
MAX_VALUE							
R							
0h							
15	14	13	12	11	10	9	8
MAX_VALUE							
R							
0h							
7	6	5	4	3	2	1	0
MAX_VALUE							
R							
0h							

Table 3-552. ECAP_MUNIT_1_DEBUG_RANGE_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE	R	0h	Observed Min value of check being enabled on minotoring unit 1. Is updated when MUNIT_1_CTL.DEBUG_RANGE_EN is set to '1'

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3.7.2.24 ECAP_MUNIT_2_CTL Register

3.7.2.24.1 ECAP_MUNIT_2_CTL Register (Offset = 100h) [reset = 0h]

Control registers for monitoring unit 2

Return to Summary Table

Table 3-553. Instance Table

Instance Name	Physical Address
ECAP00	5024 0100h
ECAP01	5024 1100h
ECAP02	5024 2100h
ECAP03	5024 3100h
ECAP04	5024 4100h
ECAP05	5024 5100h
ECAP06	5024 6100h
ECAP07	5024 7100h
ECAP08	5024 8100h
ECAP09	5024 9100h
ECAP10	5024 A100h
ECAP11	5024 B100h
ECAP12	5024 C100h
ECAP13	5024 D100h
ECAP14	5024 E100h
ECAP15	5024 F100h

Figure 3-265. ECAP_MUNIT_2_CTL Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2				MON_SEL			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						DEBUG_RANGE_EN	EN
R						R/W	R/W
0h						0h	0h

Table 3-554. ECAP_MUNIT_2_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:12	RESERVED_2	R	0h	Reserved

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Table 3-554. ECAP_MUNIT_2_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	MON_SEL	R/W	0h	Type of monitoring 0 : High Pulse width 1 : Low Pulse width 2 : Period width from Rise to Rise 3 : Period width from fall to fall 4 : Monitor rise edge 5 : Monitor fall edge 6 15 : Reserved [High Pulse width]
7:2	RESERVED_1	R	0h	Reserved
1	DEBUG_RANGE_EN	R/W	0h	Debug mode enable. 0 : Debug mode is disabled. 1 : Debug mode of monitoring unit 2 is enabled to obtain the variation seen in the system for debug purpose. Range is captured in MUNIT_2_DEBUG_RANGE_MIN and MUNIT_2_DEBUG_RANGE_MAX registers Toggle DEBUG_RANGE_EN to restart this process, this will initialize MUNIT_2_DEBUG_RANGE_MIN and MUNIT_2_DEBUG_RANGE_MAX registers.
0	EN	R/W	0h	0 : Monitoring unit 2 is disabled 1 : Monitoring unit 2 is enabled

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3.7.2.25 ECAP_MUNIT_2_SHADOW_CTL Register

3.7.2.25.1 ECAP_MUNIT_2_SHADOW_CTL Register (Offset = 104h) [reset = 0h]

Shadow control registers for monitoring unit 2

Return to Summary Table

Table 3-555. Instance Table

Instance Name	Physical Address
ECAP00	5024 0104h
ECAP01	5024 1104h
ECAP02	5024 2104h
ECAP03	5024 3104h
ECAP04	5024 4104h
ECAP05	5024 5104h
ECAP06	5024 6104h
ECAP07	5024 7104h
ECAP08	5024 8104h
ECAP09	5024 9104h
ECAP10	5024 A104h
ECAP11	5024 B104h
ECAP12	5024 C104h
ECAP13	5024 D104h
ECAP14	5024 E104h
ECAP15	5024 F104h

Figure 3-266. ECAP_MUNIT_2_SHADOW_CTL Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1					LOADMODE	SWSYNC	SYNCI_EN
R					R/W	R/W1TS	R/W
0h					0h	0h	0h

Table 3-556. ECAP_MUNIT_2_SHADOW_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_1	R	0h	Reserved
2	LOADMODE	R/W	0h	Load mode 0 : Active registers are loaded with shadow on next sync event 1 : Active registers are loaded with shadow on EPWMx.GLDLCSTRB event

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Table 3-556. ECAP_MUNIT_2_SHADOW_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SWSYNC	R/W1TS	0h	Copies Min and Max values from shadow to active registers immediately if MUNIT_2_SHADOW_CTL.SYNCI_EN is set.
0	SYNCI_EN	R/W	0h	Shadow Enable 0 : Disabled 1 : Enabled

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3.7.2.26 ECAP_MUNIT_2_MIN Register

3.7.2.26.1 ECAP_MUNIT_2_MIN Register (Offset = 110h) [reset = 0h]

Min value for monitoring unit 2

Return to Summary Table

Table 3-557. Instance Table

Instance Name	Physical Address
ECAP00	5024 0110h
ECAP01	5024 1110h
ECAP02	5024 2110h
ECAP03	5024 3110h
ECAP04	5024 4110h
ECAP05	5024 5110h
ECAP06	5024 6110h
ECAP07	5024 7110h
ECAP08	5024 8110h
ECAP09	5024 9110h
ECAP10	5024 A110h
ECAP11	5024 B110h
ECAP12	5024 C110h
ECAP13	5024 D110h
ECAP14	5024 E110h
ECAP15	5024 F110h

Figure 3-267. ECAP_MUNIT_2_MIN Name Register

31	30	29	28	27	26	25	24
MIN_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MIN_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MIN_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MIN_VALUE							
R/W							
0h							

Table 3-558. ECAP_MUNIT_2_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE	R/W	0h	Minimum value for monitoring

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3.7.2.27 ECAP_MUNIT_2_MAX Register

3.7.2.27.1 ECAP_MUNIT_2_MAX Register (Offset = 114h) [reset = 0h]

Max value for monitoring unit 2

Return to Summary Table

Table 3-559. Instance Table

Instance Name	Physical Address
ECAP00	5024 0114h
ECAP01	5024 1114h
ECAP02	5024 2114h
ECAP03	5024 3114h
ECAP04	5024 4114h
ECAP05	5024 5114h
ECAP06	5024 6114h
ECAP07	5024 7114h
ECAP08	5024 8114h
ECAP09	5024 9114h
ECAP10	5024 A114h
ECAP11	5024 B114h
ECAP12	5024 C114h
ECAP13	5024 D114h
ECAP14	5024 E114h
ECAP15	5024 F114h

Figure 3-268. ECAP_MUNIT_2_MAX Name Register

31	30	29	28	27	26	25	24
MAX_VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
MAX_VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
MAX_VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
MAX_VALUE							
R/W							
0h							

Table 3-560. ECAP_MUNIT_2_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE	R/W	0h	Maximum value for monitoring

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3.7.2.28 ECAP_MUNIT_2_MIN_SHADOW Register

3.7.2.28.1 ECAP_MUNIT_2_MIN_SHADOW Register (Offset = 118h) [reset = 0h]

Shadow register for Min value of monitoring unit 2

Return to Summary Table

Table 3-561. Instance Table

Instance Name	Physical Address
ECAP00	5024 0118h
ECAP01	5024 1118h
ECAP02	5024 2118h
ECAP03	5024 3118h
ECAP04	5024 4118h
ECAP05	5024 5118h
ECAP06	5024 6118h
ECAP07	5024 7118h
ECAP08	5024 8118h
ECAP09	5024 9118h
ECAP10	5024 A118h
ECAP11	5024 B118h
ECAP12	5024 C118h
ECAP13	5024 D118h
ECAP14	5024 E118h
ECAP15	5024 F118h

Figure 3-269. ECAP_MUNIT_2_MIN_SHADOW Name Register

31	30	29	28	27	26	25	24
MIN_VALUE_SHADOW							
R/W							
0h							
23	22	21	20	19	18	17	16
MIN_VALUE_SHADOW							
R/W							
0h							
15	14	13	12	11	10	9	8
MIN_VALUE_SHADOW							
R/W							
0h							
7	6	5	4	3	2	1	0
MIN_VALUE_SHADOW							
R/W							
0h							

Table 3-562. ECAP_MUNIT_2_MIN_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE_SHADOW	R/W	0h	Shadow minimum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

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3.7.2.29 ECAP_MUNIT_2_MAX_SHADOW Register

3.7.2.29.1 ECAP_MUNIT_2_MAX_SHADOW Register (Offset = 11Ch) [reset = 0h]

Shadow register for Max value of monitoring unit 2

Return to Summary Table

Table 3-563. Instance Table

Instance Name	Physical Address
ECAP00	5024 011Ch
ECAP01	5024 111Ch
ECAP02	5024 211Ch
ECAP03	5024 311Ch
ECAP04	5024 411Ch
ECAP05	5024 511Ch
ECAP06	5024 611Ch
ECAP07	5024 711Ch
ECAP08	5024 811Ch
ECAP09	5024 911Ch
ECAP10	5024 A11Ch
ECAP11	5024 B11Ch
ECAP12	5024 C11Ch
ECAP13	5024 D11Ch
ECAP14	5024 E11Ch
ECAP15	5024 F11Ch

Figure 3-270. ECAP_MUNIT_2_MAX_SHADOW Name Register

31	30	29	28	27	26	25	24
MAX_VALUE_SHADOW							
R/W							
0h							
23	22	21	20	19	18	17	16
MAX_VALUE_SHADOW							
R/W							
0h							
15	14	13	12	11	10	9	8
MAX_VALUE_SHADOW							
R/W							
0h							
7	6	5	4	3	2	1	0
MAX_VALUE_SHADOW							
R/W							
0h							

Table 3-564. ECAP_MUNIT_2_MAX_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE_SHADOW	R/W	0h	Shadow maximum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

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3.7.2.30 ECAP_MUNIT_2_DEBUG_RANGE_MIN Register

3.7.2.30.1 ECAP_MUNIT_2_DEBUG_RANGE_MIN Register (Offset = 120h) [reset = FFFFFFFFh]

Observed Min value of check being enabled on minotoring unit 2

Return to Summary Table

Table 3-565. Instance Table

Instance Name	Physical Address
ECAP00	5024 0120h
ECAP01	5024 1120h
ECAP02	5024 2120h
ECAP03	5024 3120h
ECAP04	5024 4120h
ECAP05	5024 5120h
ECAP06	5024 6120h
ECAP07	5024 7120h
ECAP08	5024 8120h
ECAP09	5024 9120h
ECAP10	5024 A120h
ECAP11	5024 B120h
ECAP12	5024 C120h
ECAP13	5024 D120h
ECAP14	5024 E120h
ECAP15	5024 F120h

Figure 3-271. ECAP_MUNIT_2_DEBUG_RANGE_MIN Name Register

31	30	29	28	27	26	25	24
MIN_VALUE							
R							
FFFFFFFFh							
23	22	21	20	19	18	17	16
MIN_VALUE							
R							
FFFFFFFFh							
15	14	13	12	11	10	9	8
MIN_VALUE							
R							
FFFFFFFFh							
7	6	5	4	3	2	1	0
MIN_VALUE							
R							
FFFFFFFFh							

Table 3-566. ECAP_MUNIT_2_DEBUG_RANGE_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MIN_VALUE	R	FFFFFFFFh	Observed Min value of check being enabled on minotoring unit 2. Is updated when MUNIT_2_CTL.DEBUG_RANGE_EN is set to '1'

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3.7.2.31 ECAP_MUNIT_2_DEBUG_RANGE_MAX Register

3.7.2.31.1 ECAP_MUNIT_2_DEBUG_RANGE_MAX Register (Offset = 124h) [reset = 0h]

Observed Max value of check being enabled on minotoring unit 2

Return to Summary Table

Table 3-567. Instance Table

Instance Name	Physical Address
ECAP00	5024 0124h
ECAP01	5024 1124h
ECAP02	5024 2124h
ECAP03	5024 3124h
ECAP04	5024 4124h
ECAP05	5024 5124h
ECAP06	5024 6124h
ECAP07	5024 7124h
ECAP08	5024 8124h
ECAP09	5024 9124h
ECAP10	5024 A124h
ECAP11	5024 B124h
ECAP12	5024 C124h
ECAP13	5024 D124h
ECAP14	5024 E124h
ECAP15	5024 F124h

Figure 3-272. ECAP_MUNIT_2_DEBUG_RANGE_MAX Name Register

31	30	29	28	27	26	25	24
MAX_VALUE							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MAX_VALUE							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAX_VALUE							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX_VALUE							
R							
0h							

Table 3-568. ECAP_MUNIT_2_DEBUG_RANGE_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MAX_VALUE	R	0h	Observed Min value of check being enabled on minotoring unit 2. Is updated when MUNIT_2_CTL.DEBUG_RANGE_EN is set to '1'

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3.8 EPWM

EPWM

3.8.1 EPWM Summaries

Table 3-569. EPWM Instance Table

Instance Name	Physical Address
EPWM00_G0	5000 0000h
EPWM00_G1	5004 0000h
EPWM00_G2	5008 0000h
EPWM00_G3	500C 0000h
EPWM01_G0	5000 1000h
EPWM01_G1	5004 1000h
EPWM01_G2	5008 1000h
EPWM01_G3	500C 1000h
EPWM02_G0	5000 2000h
EPWM02_G1	5004 2000h
EPWM02_G2	5008 2000h
EPWM02_G3	500C 2000h
EPWM03_G0	5000 3000h
EPWM03_G1	5004 3000h
EPWM03_G2	5008 3000h
EPWM03_G3	500C 3000h
EPWM04_G0	5000 4000h
EPWM04_G1	5004 4000h
EPWM04_G2	5008 4000h
EPWM04_G3	500C 4000h
EPWM05_G0	5000 5000h
EPWM05_G1	5004 5000h
EPWM05_G2	5008 5000h
EPWM05_G3	500C 5000h
EPWM06_G0	5000 6000h
EPWM06_G1	5004 6000h
EPWM06_G2	5008 6000h
EPWM06_G3	500C 6000h
EPWM07_G0	5000 7000h
EPWM07_G1	5004 7000h
EPWM07_G2	5008 7000h
EPWM07_G3	500C 7000h
EPWM08_G0	5000 8000h
EPWM08_G1	5004 8000h
EPWM08_G2	5008 8000h
EPWM08_G3	500C 8000h
EPWM09_G0	5000 9000h
EPWM09_G1	5004 9000h
EPWM09_G2	5008 9000h
EPWM09_G3	500C 9000h
EPWM10_G0	5000 A000h
EPWM10_G1	5004 A000h

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Table 3-569. EPWM Instance Table (continued)

Instance Name	Physical Address
EPWM10_G2	5008 A000h
EPWM10_G3	500C A000h
EPWM11_G0	5000 B000h
EPWM11_G1	5004 B000h
EPWM11_G2	5008 B000h
EPWM11_G3	500C B000h
EPWM12_G0	5000 C000h
EPWM12_G1	5004 C000h
EPWM12_G2	5008 C000h
EPWM12_G3	500C C000h
EPWM13_G0	5000 D000h
EPWM13_G1	5004 D000h
EPWM13_G2	5008 D000h
EPWM13_G3	500C D000h
EPWM14_G0	5000 E000h
EPWM14_G1	5004 E000h
EPWM14_G2	5008 E000h
EPWM14_G3	500C E000h
EPWM15_G0	5000 F000h
EPWM15_G1	5004 F000h
EPWM15_G2	5008 F000h
EPWM15_G3	500C F000h
EPWM16_G0	5001 0000h
EPWM16_G1	5005 0000h
EPWM16_G2	5009 0000h
EPWM16_G3	500D 0000h
EPWM17_G0	5001 1000h
EPWM17_G1	5005 1000h
EPWM17_G2	5009 1000h
EPWM17_G3	500D 1000h
EPWM18_G0	5001 2000h
EPWM18_G1	5005 2000h
EPWM18_G2	5009 2000h
EPWM18_G3	500D 2000h
EPWM19_G0	5001 3000h
EPWM19_G1	5005 3000h
EPWM19_G2	5009 3000h
EPWM19_G3	500D 3000h
EPWM20_G0	5001 4000h
EPWM20_G1	5005 4000h
EPWM20_G2	5009 4000h
EPWM20_G3	500D 4000h
EPWM21_G0	5001 5000h
EPWM21_G1	5005 5000h
EPWM21_G2	5009 5000h
EPWM21_G3	500D 5000h
EPWM22_G0	5001 6000h

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Table 3-569. EPWM Instance Table (continued)

Instance Name	Physical Address
EPWM22_G1	5005 6000h
EPWM22_G2	5009 6000h
EPWM22_G3	500D 6000h
EPWM23_G0	5001 7000h
EPWM23_G1	5005 7000h
EPWM23_G2	5009 7000h
EPWM23_G3	500D 7000h
EPWM24_G0	5001 8000h
EPWM24_G1	5005 8000h
EPWM24_G2	5009 8000h
EPWM24_G3	500D 8000h
EPWM25_G0	5001 9000h
EPWM25_G1	5005 9000h
EPWM25_G2	5009 9000h
EPWM25_G3	500D 9000h
EPWM26_G0	5001 A000h
EPWM26_G1	5005 A000h
EPWM26_G2	5009 A000h
EPWM26_G3	500D A000h
EPWM27_G0	5001 B000h
EPWM27_G1	5005 B000h
EPWM27_G2	5009 B000h
EPWM27_G3	500D B000h
EPWM28_G0	5001 C000h
EPWM28_G1	5005 C000h
EPWM28_G2	5009 C000h
EPWM28_G3	500D C000h
EPWM29_G0	5001 D000h
EPWM29_G1	5005 D000h
EPWM29_G2	5009 D000h
EPWM29_G3	500D D000h
EPWM30_G0	5001 E000h
EPWM30_G1	5005 E000h
EPWM30_G2	5009 E000h
EPWM30_G3	500D E000h
EPWM31_G0	5001 F000h
EPWM31_G1	5005 F000h
EPWM31_G2	5009 F000h
EPWM31_G3	500D F000h
EPWM_WLINK_G0	5002 0000h
EPWM_WLINK_G1	5006 0000h
EPWM_WLINK_G2	500A 0000h
EPWM_WLINK_G3	500E 0000h

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Table 3-570. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM00_G0 Physical Address	EPWM01_G0 Physical Address	EPWM02_G0 Physical Address
0h	16	EPWM_TBCTL	5000 0000h	5004 0000h	5008 0000h
2h	16	EPWM_TBCTL2	5000 0002h	5004 0002h	5008 0002h
6h	16	EPWM_EPWMSYNCINSEL	5000 0006h	5004 0006h	5008 0006h
8h	16	EPWM_TBCTR	5000 0008h	5004 0008h	5008 0008h
Ah	16	EPWM_TBSTS	5000 000Ah	5004 000Ah	5008 000Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5000 000Ch	5004 000Ch	5008 000Ch
Eh	16	EPWM_TBCTL3	5000 000Eh	5004 000Eh	5008 000Eh
10h	16	EPWM_CMPCTL	5000 0010h	5004 0010h	5008 0010h
12h	16	EPWM_CMPCTL2	5000 0012h	5004 0012h	5008 0012h
18h	16	EPWM_DBCTL	5000 0018h	5004 0018h	5008 0018h
1Ah	16	EPWM_DBCTL2	5000 001Ah	5004 001Ah	5008 001Ah
20h	16	EPWM_AQCTL	5000 0020h	5004 0020h	5008 0020h
22h	16	EPWM_AQTSRCSEL	5000 0022h	5004 0022h	5008 0022h
28h	16	EPWM_PCCTL	5000 0028h	5004 0028h	5008 0028h
30h	16	EPWM_VCAPCTL	5000 0030h	5004 0030h	5008 0030h
32h	16	EPWM_VCNTCFG	5000 0032h	5004 0032h	5008 0032h
40h	16	EPWM_HRCNFG	5000 0040h	5004 0040h	5008 0040h
4Eh	16	EPWM_HRCNFG2	5000 004Eh	5004 004Eh	5008 004Eh
5Ah	16	EPWM_HRPCTL	5000 005Ah	5004 005Ah	5008 005Ah
5Ch	16	EPWM_TRREM	5000 005Ch	5004 005Ch	5008 005Ch
68h	16	EPWM_GLDCTL	5000 0068h	5004 0068h	5008 0068h
6Ah	16	EPWM_GLDCFG	5000 006Ah	5004 006Ah	5008 006Ah
70h	32	EPWM_EPWMXLINK	5000 0070h	5004 0070h	5008 0070h
74h	32	EPWM_EPWMXLINK2	5000 0074h	5004 0074h	5008 0074h
7Ah	16	EPWM_ETEST	5000 007Ah	5004 007Ah	5008 007Ah
7Ch	16	EPWM_EPWMREV	5000 007Ch	5004 007Ch	5008 007Ch
7Eh	16	EPWM_HRPWMREV	5000 007Eh	5004 007Eh	5008 007Eh
80h	16	EPWM_AQCTLA	5000 0080h	5004 0080h	5008 0080h
82h	16	EPWM_AQCTLA2	5000 0082h	5004 0082h	5008 0082h
84h	16	EPWM_AQCTLB	5000 0084h	5004 0084h	5008 0084h
86h	16	EPWM_AQCTLB2	5000 0086h	5004 0086h	5008 0086h
8Eh	16	EPWM_AQSFRC	5000 008Eh	5004 008Eh	5008 008Eh
92h	16	EPWM_AQCSFRC	5000 0092h	5004 0092h	5008 0092h
A0h	16	EPWM_DBREDHR	5000 00A0h	5004 00A0h	5008 00A0h
A2h	16	EPWM_DBRED	5000 00A2h	5004 00A2h	5008 00A2h
A4h	16	EPWM_DBFEDHR	5000 00A4h	5004 00A4h	5008 00A4h
A6h	16	EPWM_DBFED	5000 00A6h	5004 00A6h	5008 00A6h
C0h	32	EPWM_TBPHS	5000 00C0h	5004 00C0h	5008 00C0h
C4h	16	EPWM_TBPRDHR	5000 00C4h	5004 00C4h	5008 00C4h
C6h	16	EPWM_TBPRD	5000 00C6h	5004 00C6h	5008 00C6h
C8h	16	EPWM_TBPRDHRB	5000 00C8h	5004 00C8h	5008 00C8h
D4h	32	EPWM_CMPA	5000 00D4h	5004 00D4h	5008 00D4h
D8h	32	EPWM_CMPB	5000 00D8h	5004 00D8h	5008 00D8h
DEh	16	EPWM_CMPC	5000 00DEh	5004 00DEh	5008 00DEh
E2h	16	EPWM_CMPD	5000 00E2h	5004 00E2h	5008 00E2h
E8h	16	EPWM_GLDCTL2	5000 00E8h	5004 00E8h	5008 00E8h

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Table 3-570. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM00_G0 Physical Address	EPWM01_G0 Physical Address	EPWM02_G0 Physical Address
EEh	16	EPWM_SWVDELVAL	5000 00EEh	5004 00EEh	5008 00EEh
100h	16	EPWM_TZSEL	5000 0100h	5004 0100h	5008 0100h
102h	16	EPWM_TZSEL2	5000 0102h	5004 0102h	5008 0102h
104h	16	EPWM_TZDCSEL	5000 0104h	5004 0104h	5008 0104h
108h	16	EPWM_TZCTL	5000 0108h	5004 0108h	5008 0108h
10Ah	16	EPWM_TZCTL2	5000 010Ah	5004 010Ah	5008 010Ah
10Ch	16	EPWM_TZCTLDCA	5000 010Ch	5004 010Ch	5008 010Ch
10Eh	16	EPWM_TZCTLDCB	5000 010Eh	5004 010Eh	5008 010Eh
11Ah	16	EPWM_TZEINT	5000 011Ah	5004 011Ah	5008 011Ah
126h	16	EPWM_TZFLG	5000 0126h	5004 0126h	5008 0126h
128h	16	EPWM_TZCBCFLG	5000 0128h	5004 0128h	5008 0128h
12Ah	16	EPWM_TZOSTFLG	5000 012Ah	5004 012Ah	5008 012Ah
12Eh	16	EPWM_TZCLR	5000 012Eh	5004 012Eh	5008 012Eh
130h	16	EPWM_TZCBCCLR	5000 0130h	5004 0130h	5008 0130h
132h	16	EPWM_TZOSTCLR	5000 0132h	5004 0132h	5008 0132h
136h	16	EPWM_TZFRC	5000 0136h	5004 0136h	5008 0136h
13Ah	16	EPWM_TZTRIPOUTSEL	5000 013Ah	5004 013Ah	5008 013Ah
148h	16	EPWM_ETSEL	5000 0148h	5004 0148h	5008 0148h
14Ch	16	EPWM_ETPS	5000 014Ch	5004 014Ch	5008 014Ch
150h	16	EPWM_ETFLG	5000 0150h	5004 0150h	5008 0150h
154h	16	EPWM_ETCLR	5000 0154h	5004 0154h	5008 0154h
158h	16	EPWM_ETFRC	5000 0158h	5004 0158h	5008 0158h
15Ch	16	EPWM_ETINTPS	5000 015Ch	5004 015Ch	5008 015Ch
160h	16	EPWM_ETSOCPS	5000 0160h	5004 0160h	5008 0160h
164h	16	EPWM_ETCNTINITCTL	5000 0164h	5004 0164h	5008 0164h
168h	16	EPWM_ETCNTINIT	5000 0168h	5004 0168h	5008 0168h
16Ch	16	EPWM_ETINTMIXEN	5000 016Ch	5004 016Ch	5008 016Ch
170h	16	EPWM_ETSOCAMIXEN	5000 0170h	5004 0170h	5008 0170h
174h	16	EPWM_ETSOCBMIXEN	5000 0174h	5004 0174h	5008 0174h
180h	16	EPWM_DCTRIPSEL	5000 0180h	5004 0180h	5008 0180h
186h	16	EPWM_DCACTL	5000 0186h	5004 0186h	5008 0186h
188h	16	EPWM_DCBCTL	5000 0188h	5004 0188h	5008 0188h
18Eh	16	EPWM_DCFCTL	5000 018Eh	5004 018Eh	5008 018Eh
190h	16	EPWM_DCCAPCTL	5000 0190h	5004 0190h	5008 0190h
192h	16	EPWM_DCFOFFSET	5000 0192h	5004 0192h	5008 0192h
194h	16	EPWM_DCFOFFSETCNT	5000 0194h	5004 0194h	5008 0194h
196h	16	EPWM_DCFWINDOW	5000 0196h	5004 0196h	5008 0196h
198h	16	EPWM_DCFWINDOWCNT	5000 0198h	5004 0198h	5008 0198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5000 019Ah	5004 019Ah	5008 019Ah
19Ch	16	EPWM_DCCAPMIXSEL	5000 019Ch	5004 019Ch	5008 019Ch
19Eh	16	EPWM_DCCAP	5000 019Eh	5004 019Eh	5008 019Eh
1A4h	16	EPWM_DCAHTRIPSEL	5000 01A4h	5004 01A4h	5008 01A4h
1A6h	16	EPWM_DCALTRIPSEL	5000 01A6h	5004 01A6h	5008 01A6h
1A8h	16	EPWM_DCBHTRIPSEL	5000 01A8h	5004 01A8h	5008 01A8h
1AAh	16	EPWM_DCBLTRIPSEL	5000 01AAh	5004 01AAh	5008 01AAh
1ACh	16	EPWM_CAPCTL	5000 01ACh	5004 01ACh	5008 01ACh

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Table 3-570. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM00_G0 Physical Address	EPWM01_G0 Physical Address	EPWM02_G0 Physical Address
1AEh	16	EPWM_CAPGATETRIPSEL	5000 01AEh	5004 01AEh	5008 01AEh
1B0h	16	EPWM_CAPINTRIPSEL	5000 01B0h	5004 01B0h	5008 01B0h
1B2h	16	EPWM_CAPTRIPSEL	5000 01B2h	5004 01B2h	5008 01B2h
1F4h	32	EPWM_EPWMLOCK	5000 01F4h	5004 01F4h	5008 01F4h
1FAh	16	EPWM_HWVDELVAL	5000 01FAh	5004 01FAh	5008 01FAh
1FCh	16	EPWM_VCNTVAL	5000 01FCh	5004 01FCh	5008 01FCh
400h	32	EPWM_XCMPCTL1	5000 0400h	5004 0400h	5008 0400h
410h	32	EPWM_XLOADCTL	5000 0410h	5004 0410h	5008 0410h
418h	32	EPWM_XLOAD	5000 0418h	5004 0418h	5008 0418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5000 041Ch	5004 041Ch	5008 041Ch
420h	32	EPWM_XREGSHDW1STS	5000 0420h	5004 0420h	5008 0420h
428h	32	EPWM_XREGSHDW2STS	5000 0428h	5004 0428h	5008 0428h
430h	32	EPWM_XREGSHDW3STS	5000 0430h	5004 0430h	5008 0430h
600h	32	EPWM_XCMP1_ACTIVE	5000 0600h	5004 0600h	5008 0600h
604h	32	EPWM_XCMP2_ACTIVE	5000 0604h	5004 0604h	5008 0604h
608h	32	EPWM_XCMP3_ACTIVE	5000 0608h	5004 0608h	5008 0608h
60Ch	32	EPWM_XCMP4_ACTIVE	5000 060Ch	5004 060Ch	5008 060Ch
610h	32	EPWM_XCMP5_ACTIVE	5000 0610h	5004 0610h	5008 0610h
614h	32	EPWM_XCMP6_ACTIVE	5000 0614h	5004 0614h	5008 0614h
618h	32	EPWM_XCMP7_ACTIVE	5000 0618h	5004 0618h	5008 0618h
61Ch	32	EPWM_XCMP8_ACTIVE	5000 061Ch	5004 061Ch	5008 061Ch
620h	32	EPWM_XTBPRD_ACTIVE	5000 0620h	5004 0620h	5008 0620h
630h	16	EPWM_XAQCTLA_ACTIVE	5000 0630h	5004 0630h	5008 0630h
644h	32	EPWM_XMINMAX_ACTIVE	5000 0644h	5004 0644h	5008 0644h
680h	32	EPWM_XCMP1_SHDW1	5000 0680h	5004 0680h	5008 0680h
684h	32	EPWM_XCMP2_SHDW1	5000 0684h	5004 0684h	5008 0684h
688h	32	EPWM_XCMP3_SHDW1	5000 0688h	5004 0688h	5008 0688h
68Ch	32	EPWM_XCMP4_SHDW1	5000 068Ch	5004 068Ch	5008 068Ch
690h	32	EPWM_XCMP5_SHDW1	5000 0690h	5004 0690h	5008 0690h
694h	32	EPWM_XCMP6_SHDW1	5000 0694h	5004 0694h	5008 0694h
698h	32	EPWM_XCMP7_SHDW1	5000 0698h	5004 0698h	5008 0698h
69Ch	32	EPWM_XCMP8_SHDW1	5000 069Ch	5004 069Ch	5008 069Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5000 06A0h	5004 06A0h	5008 06A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5000 06B0h	5004 06B0h	5008 06B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5000 06B2h	5004 06B2h	5008 06B2h
6BAh	16	EPWM_CMPC_SHDW1	5000 06BAh	5004 06BAh	5008 06BAh
6BEh	16	EPWM_CMPD_SHDW1	5000 06BEh	5004 06BEh	5008 06BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5000 06C4h	5004 06C4h	5008 06C4h
700h	32	EPWM_XCMP1_SHDW2	5000 0700h	5004 0700h	5008 0700h
704h	32	EPWM_XCMP2_SHDW2	5000 0704h	5004 0704h	5008 0704h
708h	32	EPWM_XCMP3_SHDW2	5000 0708h	5004 0708h	5008 0708h
70Ch	32	EPWM_XCMP4_SHDW2	5000 070Ch	5004 070Ch	5008 070Ch
710h	32	EPWM_XCMP5_SHDW2	5000 0710h	5004 0710h	5008 0710h
714h	32	EPWM_XCMP6_SHDW2	5000 0714h	5004 0714h	5008 0714h
718h	32	EPWM_XCMP7_SHDW2	5000 0718h	5004 0718h	5008 0718h
71Ch	32	EPWM_XCMP8_SHDW2	5000 071Ch	5004 071Ch	5008 071Ch

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Table 3-570. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM00_G0 Physical Address	EPWM01_G0 Physical Address	EPWM02_G0 Physical Address
720h	32	EPWM_XTBPRD_SHDW2	5000 0720h	5004 0720h	5008 0720h
730h	16	EPWM_XAQCTLA_SHDW2	5000 0730h	5004 0730h	5008 0730h
732h	16	EPWM_XAQCTLB_SHDW2	5000 0732h	5004 0732h	5008 0732h
73Ah	16	EPWM_CMPC_SHDW2	5000 073Ah	5004 073Ah	5008 073Ah
73Eh	16	EPWM_CMPD_SHDW2	5000 073Eh	5004 073Eh	5008 073Eh
744h	32	EPWM_XMINMAX_SHDW2	5000 0744h	5004 0744h	5008 0744h
780h	32	EPWM_XCMP1_SHDW3	5000 0780h	5004 0780h	5008 0780h
784h	32	EPWM_XCMP2_SHDW3	5000 0784h	5004 0784h	5008 0784h
788h	32	EPWM_XCMP3_SHDW3	5000 0788h	5004 0788h	5008 0788h
78Ch	32	EPWM_XCMP4_SHDW3	5000 078Ch	5004 078Ch	5008 078Ch
790h	32	EPWM_XCMP5_SHDW3	5000 0790h	5004 0790h	5008 0790h
794h	32	EPWM_XCMP6_SHDW3	5000 0794h	5004 0794h	5008 0794h
798h	32	EPWM_XCMP7_SHDW3	5000 0798h	5004 0798h	5008 0798h
79Ch	32	EPWM_XCMP8_SHDW3	5000 079Ch	5004 079Ch	5008 079Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5000 07A0h	5004 07A0h	5008 07A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5000 07B0h	5004 07B0h	5008 07B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5000 07B2h	5004 07B2h	5008 07B2h
7BAh	16	EPWM_CMPC_SHDW3	5000 07BAh	5004 07BAh	5008 07BAh
7BEh	16	EPWM_CMPD_SHDW3	5000 07BEh	5004 07BEh	5008 07BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5000 07C4h	5004 07C4h	5008 07C4h
800h	32	EPWM_DECTL	5000 0800h	5004 0800h	5008 0800h
804h	32	EPWM_DECOMPSEL	5000 0804h	5004 0804h	5008 0804h
808h	32	EPWM_DEACTCTL	5000 0808h	5004 0808h	5008 0808h
80Ch	32	EPWM_DESTS	5000 080Ch	5004 080Ch	5008 080Ch
810h	32	EPWM_DEFRC	5000 0810h	5004 0810h	5008 0810h
814h	32	EPWM_DECLR	5000 0814h	5004 0814h	5008 0814h
820h	32	EPWM_DEMONCNT	5000 0820h	5004 0820h	5008 0820h
824h	32	EPWM_DEMONCTL	5000 0824h	5004 0824h	5008 0824h
828h	32	EPWM_DEMONSTEP	5000 0828h	5004 0828h	5008 0828h
82Ch	32	EPWM_DEMONTHRES	5000 082Ch	5004 082Ch	5008 082Ch
C00h	32	EPWM_MINDBCFG	5000 0C00h	5004 0C00h	5008 0C00h
C04h	32	EPWM_MINDBDLY	5000 0C04h	5004 0C04h	5008 0C04h
C20h	32	EPWM_LUTCTLA	5000 0C20h	5004 0C20h	5008 0C20h
C24h	32	EPWM_LUTCTLB	5000 0C24h	5004 0C24h	5008 0C24h

Table 3-571. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM03_G0 Physical Address	EPWM04_G0 Physical Address	EPWM05_G0 Physical Address
0h	16	EPWM_TBCTL	500C 0000h	5000 1000h	5004 1000h
2h	16	EPWM_TBCTL2	500C 0002h	5000 1002h	5004 1002h
6h	16	EPWM_EPWMSYNCINSEL	500C 0006h	5000 1006h	5004 1006h
8h	16	EPWM_TBCTR	500C 0008h	5000 1008h	5004 1008h
Ah	16	EPWM_TBSTS	500C 000Ah	5000 100Ah	5004 100Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500C 000Ch	5000 100Ch	5004 100Ch
Eh	16	EPWM_TBCTL3	500C 000Eh	5000 100Eh	5004 100Eh
10h	16	EPWM_CMPCTL	500C 0010h	5000 1010h	5004 1010h

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Table 3-571. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM03_G0 Physical Address	EPWM04_G0 Physical Address	EPWM05_G0 Physical Address
12h	16	EPWM_CMPCTL2	500C 0012h	5000 1012h	5004 1012h
18h	16	EPWM_DBCTL	500C 0018h	5000 1018h	5004 1018h
1Ah	16	EPWM_DBCTL2	500C 001Ah	5000 101Ah	5004 101Ah
20h	16	EPWM_AQCTL	500C 0020h	5000 1020h	5004 1020h
22h	16	EPWM_AQTSRCSEL	500C 0022h	5000 1022h	5004 1022h
28h	16	EPWM_PCCTL	500C 0028h	5000 1028h	5004 1028h
30h	16	EPWM_VCAPCTL	500C 0030h	5000 1030h	5004 1030h
32h	16	EPWM_VCNTCFG	500C 0032h	5000 1032h	5004 1032h
40h	16	EPWM_HRCNFG	500C 0040h	5000 1040h	5004 1040h
4Eh	16	EPWM_HRCNFG2	500C 004Eh	5000 104Eh	5004 104Eh
5Ah	16	EPWM_HRPCTL	500C 005Ah	5000 105Ah	5004 105Ah
5Ch	16	EPWM_TRREM	500C 005Ch	5000 105Ch	5004 105Ch
68h	16	EPWM_GLDCTL	500C 0068h	5000 1068h	5004 1068h
6Ah	16	EPWM_GLDCFG	500C 006Ah	5000 106Ah	5004 106Ah
70h	32	EPWM_EPWMXLINK	500C 0070h	5000 1070h	5004 1070h
74h	32	EPWM_EPWMXLINK2	500C 0074h	5000 1074h	5004 1074h
7Ah	16	EPWM_ETEST	500C 007Ah	5000 107Ah	5004 107Ah
7Ch	16	EPWM_EPWMREV	500C 007Ch	5000 107Ch	5004 107Ch
7Eh	16	EPWM_HRPWMREV	500C 007Eh	5000 107Eh	5004 107Eh
80h	16	EPWM_AQCTLA	500C 0080h	5000 1080h	5004 1080h
82h	16	EPWM_AQCTLA2	500C 0082h	5000 1082h	5004 1082h
84h	16	EPWM_AQCTLB	500C 0084h	5000 1084h	5004 1084h
86h	16	EPWM_AQCTLB2	500C 0086h	5000 1086h	5004 1086h
8Eh	16	EPWM_AQSFRC	500C 008Eh	5000 108Eh	5004 108Eh
92h	16	EPWM_AQCSFRC	500C 0092h	5000 1092h	5004 1092h
A0h	16	EPWM_DBREDHR	500C 00A0h	5000 10A0h	5004 10A0h
A2h	16	EPWM_DBRED	500C 00A2h	5000 10A2h	5004 10A2h
A4h	16	EPWM_DBFEDHR	500C 00A4h	5000 10A4h	5004 10A4h
A6h	16	EPWM_DBFED	500C 00A6h	5000 10A6h	5004 10A6h
C0h	32	EPWM_TBPHS	500C 00C0h	5000 10C0h	5004 10C0h
C4h	16	EPWM_TBPRDHR	500C 00C4h	5000 10C4h	5004 10C4h
C6h	16	EPWM_TBPRD	500C 00C6h	5000 10C6h	5004 10C6h
C8h	16	EPWM_TBPRDHRB	500C 00C8h	5000 10C8h	5004 10C8h
D4h	32	EPWM_CMPA	500C 00D4h	5000 10D4h	5004 10D4h
D8h	32	EPWM_CMPB	500C 00D8h	5000 10D8h	5004 10D8h
DEh	16	EPWM_CMPC	500C 00DEh	5000 10DEh	5004 10DEh
E2h	16	EPWM_CMPD	500C 00E2h	5000 10E2h	5004 10E2h
E8h	16	EPWM_GLDCTL2	500C 00E8h	5000 10E8h	5004 10E8h
EEh	16	EPWM_SWVDELVAL	500C 00EEh	5000 10EEh	5004 10EEh
100h	16	EPWM_TZSEL	500C 0100h	5000 1100h	5004 1100h
102h	16	EPWM_TZSEL2	500C 0102h	5000 1102h	5004 1102h
104h	16	EPWM_TZDCSEL	500C 0104h	5000 1104h	5004 1104h
108h	16	EPWM_TZCTL	500C 0108h	5000 1108h	5004 1108h
10Ah	16	EPWM_TZCTL2	500C 010Ah	5000 110Ah	5004 110Ah
10Ch	16	EPWM_TZCTLDCA	500C 010Ch	5000 110Ch	5004 110Ch
10Eh	16	EPWM_TZCTLDCB	500C 010Eh	5000 110Eh	5004 110Eh

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Table 3-571. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM03_G0 Physical Address	EPWM04_G0 Physical Address	EPWM05_G0 Physical Address
11Ah	16	EPWM_TZEINT	500C 011Ah	5000 111Ah	5004 111Ah
126h	16	EPWM_TZFLG	500C 0126h	5000 1126h	5004 1126h
128h	16	EPWM_TZCBCFLG	500C 0128h	5000 1128h	5004 1128h
12Ah	16	EPWM_TZOSTFLG	500C 012Ah	5000 112Ah	5004 112Ah
12Eh	16	EPWM_TZCLR	500C 012Eh	5000 112Eh	5004 112Eh
130h	16	EPWM_TZCBCCLR	500C 0130h	5000 1130h	5004 1130h
132h	16	EPWM_TZOSTCLR	500C 0132h	5000 1132h	5004 1132h
136h	16	EPWM_TZFRC	500C 0136h	5000 1136h	5004 1136h
13Ah	16	EPWM_TZTRIPOUTSEL	500C 013Ah	5000 113Ah	5004 113Ah
148h	16	EPWM_ETSEL	500C 0148h	5000 1148h	5004 1148h
14Ch	16	EPWM_ETPS	500C 014Ch	5000 114Ch	5004 114Ch
150h	16	EPWM_ETFLG	500C 0150h	5000 1150h	5004 1150h
154h	16	EPWM_ETCLR	500C 0154h	5000 1154h	5004 1154h
158h	16	EPWM_ETFRC	500C 0158h	5000 1158h	5004 1158h
15Ch	16	EPWM_ETINTPS	500C 015Ch	5000 115Ch	5004 115Ch
160h	16	EPWM_ETSOCPS	500C 0160h	5000 1160h	5004 1160h
164h	16	EPWM_ETCNTINITCTL	500C 0164h	5000 1164h	5004 1164h
168h	16	EPWM_ETCNTINIT	500C 0168h	5000 1168h	5004 1168h
16Ch	16	EPWM_ETINTMIXEN	500C 016Ch	5000 116Ch	5004 116Ch
170h	16	EPWM_ETSOCAMIXEN	500C 0170h	5000 1170h	5004 1170h
174h	16	EPWM_ETSOCBMIXEN	500C 0174h	5000 1174h	5004 1174h
180h	16	EPWM_DCTRIPSEL	500C 0180h	5000 1180h	5004 1180h
186h	16	EPWM_DCACTL	500C 0186h	5000 1186h	5004 1186h
188h	16	EPWM_DCBCTL	500C 0188h	5000 1188h	5004 1188h
18Eh	16	EPWM_DCFCTL	500C 018Eh	5000 118Eh	5004 118Eh
190h	16	EPWM_DCCAPCTL	500C 0190h	5000 1190h	5004 1190h
192h	16	EPWM_DCFOFFSET	500C 0192h	5000 1192h	5004 1192h
194h	16	EPWM_DCFOFFSETCNT	500C 0194h	5000 1194h	5004 1194h
196h	16	EPWM_DCFWINDOW	500C 0196h	5000 1196h	5004 1196h
198h	16	EPWM_DCFWINDOWCNT	500C 0198h	5000 1198h	5004 1198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500C 019Ah	5000 119Ah	5004 119Ah
19Ch	16	EPWM_DCCAPMIXSEL	500C 019Ch	5000 119Ch	5004 119Ch
19Eh	16	EPWM_DCCAP	500C 019Eh	5000 119Eh	5004 119Eh
1A4h	16	EPWM_DCAHTRIPSEL	500C 01A4h	5000 11A4h	5004 11A4h
1A6h	16	EPWM_DCALTRIPSEL	500C 01A6h	5000 11A6h	5004 11A6h
1A8h	16	EPWM_DCBHTRIPSEL	500C 01A8h	5000 11A8h	5004 11A8h
1AAh	16	EPWM_DCBLTRIPSEL	500C 01AAh	5000 11AAh	5004 11AAh
1ACh	16	EPWM_CAPCTL	500C 01ACh	5000 11ACh	5004 11ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500C 01AEh	5000 11AEh	5004 11AEh
1B0h	16	EPWM_CAPINTRIPSEL	500C 01B0h	5000 11B0h	5004 11B0h
1B2h	16	EPWM_CAPTRIPSEL	500C 01B2h	5000 11B2h	5004 11B2h
1F4h	32	EPWM_EPWMLOCK	500C 01F4h	5000 11F4h	5004 11F4h
1FAh	16	EPWM_HWVDELVAL	500C 01FAh	5000 11FAh	5004 11FAh
1FCh	16	EPWM_VCNTVAL	500C 01FCh	5000 11FCh	5004 11FCh
400h	32	EPWM_XCMPCTL1	500C 0400h	5000 1400h	5004 1400h
410h	32	EPWM_XLOADCTL	500C 0410h	5000 1410h	5004 1410h

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Table 3-571. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM03_G0 Physical Address	EPWM04_G0 Physical Address	EPWM05_G0 Physical Address
418h	32	EPWM_XLOAD	500C 0418h	5000 1418h	5004 1418h
41Ch	32	EPWM_EPWMXLINKXLOAD	500C 041Ch	5000 141Ch	5004 141Ch
420h	32	EPWM_XREGSHDW1STS	500C 0420h	5000 1420h	5004 1420h
428h	32	EPWM_XREGSHDW2STS	500C 0428h	5000 1428h	5004 1428h
430h	32	EPWM_XREGSHDW3STS	500C 0430h	5000 1430h	5004 1430h
600h	32	EPWM_XCMP1_ACTIVE	500C 0600h	5000 1600h	5004 1600h
604h	32	EPWM_XCMP2_ACTIVE	500C 0604h	5000 1604h	5004 1604h
608h	32	EPWM_XCMP3_ACTIVE	500C 0608h	5000 1608h	5004 1608h
60Ch	32	EPWM_XCMP4_ACTIVE	500C 060Ch	5000 160Ch	5004 160Ch
610h	32	EPWM_XCMP5_ACTIVE	500C 0610h	5000 1610h	5004 1610h
614h	32	EPWM_XCMP6_ACTIVE	500C 0614h	5000 1614h	5004 1614h
618h	32	EPWM_XCMP7_ACTIVE	500C 0618h	5000 1618h	5004 1618h
61Ch	32	EPWM_XCMP8_ACTIVE	500C 061Ch	5000 161Ch	5004 161Ch
620h	32	EPWM_XTBPRD_ACTIVE	500C 0620h	5000 1620h	5004 1620h
630h	16	EPWM_XAQCTLA_ACTIVE	500C 0630h	5000 1630h	5004 1630h
644h	32	EPWM_XMINMAX_ACTIVE	500C 0644h	5000 1644h	5004 1644h
680h	32	EPWM_XCMP1_SHDW1	500C 0680h	5000 1680h	5004 1680h
684h	32	EPWM_XCMP2_SHDW1	500C 0684h	5000 1684h	5004 1684h
688h	32	EPWM_XCMP3_SHDW1	500C 0688h	5000 1688h	5004 1688h
68Ch	32	EPWM_XCMP4_SHDW1	500C 068Ch	5000 168Ch	5004 168Ch
690h	32	EPWM_XCMP5_SHDW1	500C 0690h	5000 1690h	5004 1690h
694h	32	EPWM_XCMP6_SHDW1	500C 0694h	5000 1694h	5004 1694h
698h	32	EPWM_XCMP7_SHDW1	500C 0698h	5000 1698h	5004 1698h
69Ch	32	EPWM_XCMP8_SHDW1	500C 069Ch	5000 169Ch	5004 169Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500C 06A0h	5000 16A0h	5004 16A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500C 06B0h	5000 16B0h	5004 16B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500C 06B2h	5000 16B2h	5004 16B2h
6BAh	16	EPWM_CMPC_SHDW1	500C 06BAh	5000 16BAh	5004 16BAh
6BEh	16	EPWM_CMPD_SHDW1	500C 06BEh	5000 16BEh	5004 16BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500C 06C4h	5000 16C4h	5004 16C4h
700h	32	EPWM_XCMP1_SHDW2	500C 0700h	5000 1700h	5004 1700h
704h	32	EPWM_XCMP2_SHDW2	500C 0704h	5000 1704h	5004 1704h
708h	32	EPWM_XCMP3_SHDW2	500C 0708h	5000 1708h	5004 1708h
70Ch	32	EPWM_XCMP4_SHDW2	500C 070Ch	5000 170Ch	5004 170Ch
710h	32	EPWM_XCMP5_SHDW2	500C 0710h	5000 1710h	5004 1710h
714h	32	EPWM_XCMP6_SHDW2	500C 0714h	5000 1714h	5004 1714h
718h	32	EPWM_XCMP7_SHDW2	500C 0718h	5000 1718h	5004 1718h
71Ch	32	EPWM_XCMP8_SHDW2	500C 071Ch	5000 171Ch	5004 171Ch
720h	32	EPWM_XTBPRD_SHDW2	500C 0720h	5000 1720h	5004 1720h
730h	16	EPWM_XAQCTLA_SHDW2	500C 0730h	5000 1730h	5004 1730h
732h	16	EPWM_XAQCTLB_SHDW2	500C 0732h	5000 1732h	5004 1732h
73Ah	16	EPWM_CMPC_SHDW2	500C 073Ah	5000 173Ah	5004 173Ah
73Eh	16	EPWM_CMPD_SHDW2	500C 073Eh	5000 173Eh	5004 173Eh
744h	32	EPWM_XMINMAX_SHDW2	500C 0744h	5000 1744h	5004 1744h
780h	32	EPWM_XCMP1_SHDW3	500C 0780h	5000 1780h	5004 1780h
784h	32	EPWM_XCMP2_SHDW3	500C 0784h	5000 1784h	5004 1784h

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Table 3-571. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM03_G0 Physical Address	EPWM04_G0 Physical Address	EPWM05_G0 Physical Address
788h	32	EPWM_XCMP3_SHDW3	500C 0788h	5000 1788h	5004 1788h
78Ch	32	EPWM_XCMP4_SHDW3	500C 078Ch	5000 178Ch	5004 178Ch
790h	32	EPWM_XCMP5_SHDW3	500C 0790h	5000 1790h	5004 1790h
794h	32	EPWM_XCMP6_SHDW3	500C 0794h	5000 1794h	5004 1794h
798h	32	EPWM_XCMP7_SHDW3	500C 0798h	5000 1798h	5004 1798h
79Ch	32	EPWM_XCMP8_SHDW3	500C 079Ch	5000 179Ch	5004 179Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500C 07A0h	5000 17A0h	5004 17A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500C 07B0h	5000 17B0h	5004 17B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500C 07B2h	5000 17B2h	5004 17B2h
7BAh	16	EPWM_CMPC_SHDW3	500C 07BAh	5000 17BAh	5004 17BAh
7BEh	16	EPWM_CMPD_SHDW3	500C 07BEh	5000 17BEh	5004 17BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500C 07C4h	5000 17C4h	5004 17C4h
800h	32	EPWM_DECTL	500C 0800h	5000 1800h	5004 1800h
804h	32	EPWM_DECOMPSEL	500C 0804h	5000 1804h	5004 1804h
808h	32	EPWM_DEACTCTL	500C 0808h	5000 1808h	5004 1808h
80Ch	32	EPWM_DESTS	500C 080Ch	5000 180Ch	5004 180Ch
810h	32	EPWM_DEFRC	500C 0810h	5000 1810h	5004 1810h
814h	32	EPWM_DECLR	500C 0814h	5000 1814h	5004 1814h
820h	32	EPWM_DEMONCNT	500C 0820h	5000 1820h	5004 1820h
824h	32	EPWM_DEMONCTL	500C 0824h	5000 1824h	5004 1824h
828h	32	EPWM_DEMONSTEP	500C 0828h	5000 1828h	5004 1828h
82Ch	32	EPWM_DEMONTHRES	500C 082Ch	5000 182Ch	5004 182Ch
C00h	32	EPWM_MINDBCFG	500C 0C00h	5000 1C00h	5004 1C00h
C04h	32	EPWM_MINDBDLY	500C 0C04h	5000 1C04h	5004 1C04h
C20h	32	EPWM_LUTCTLA	500C 0C20h	5000 1C20h	5004 1C20h
C24h	32	EPWM_LUTCTLB	500C 0C24h	5000 1C24h	5004 1C24h

Table 3-572. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM06_G0 Physical Address	EPWM07_G0 Physical Address	EPWM08_G0 Physical Address
0h	16	EPWM_TBCTL	5008 1000h	500C 1000h	5000 2000h
2h	16	EPWM_TBCTL2	5008 1002h	500C 1002h	5000 2002h
6h	16	EPWM_EPWMSYNCINSEL	5008 1006h	500C 1006h	5000 2006h
8h	16	EPWM_TBCTR	5008 1008h	500C 1008h	5000 2008h
Ah	16	EPWM_TBSTS	5008 100Ah	500C 100Ah	5000 200Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5008 100Ch	500C 100Ch	5000 200Ch
Eh	16	EPWM_TBCTL3	5008 100Eh	500C 100Eh	5000 200Eh
10h	16	EPWM_CMPCTL	5008 1010h	500C 1010h	5000 2010h
12h	16	EPWM_CMPCTL2	5008 1012h	500C 1012h	5000 2012h
18h	16	EPWM_DBCTL	5008 1018h	500C 1018h	5000 2018h
1Ah	16	EPWM_DBCTL2	5008 101Ah	500C 101Ah	5000 201Ah
20h	16	EPWM_AQCTL	5008 1020h	500C 1020h	5000 2020h
22h	16	EPWM_AQTSRCSEL	5008 1022h	500C 1022h	5000 2022h
28h	16	EPWM_PCCTL	5008 1028h	500C 1028h	5000 2028h
30h	16	EPWM_VCAPCTL	5008 1030h	500C 1030h	5000 2030h
32h	16	EPWM_VCNTCFG	5008 1032h	500C 1032h	5000 2032h

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Table 3-572. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM06_G0 Physical Address	EPWM07_G0 Physical Address	EPWM08_G0 Physical Address
40h	16	EPWM_HRCNFG	5008 1040h	500C 1040h	5000 2040h
4Eh	16	EPWM_HRCNFG2	5008 104Eh	500C 104Eh	5000 204Eh
5Ah	16	EPWM_HRPCTL	5008 105Ah	500C 105Ah	5000 205Ah
5Ch	16	EPWM_TRREM	5008 105Ch	500C 105Ch	5000 205Ch
68h	16	EPWM_GLDCTL	5008 1068h	500C 1068h	5000 2068h
6Ah	16	EPWM_GLDCFG	5008 106Ah	500C 106Ah	5000 206Ah
70h	32	EPWM_EPWMXLINK	5008 1070h	500C 1070h	5000 2070h
74h	32	EPWM_EPWMXLINK2	5008 1074h	500C 1074h	5000 2074h
7Ah	16	EPWM_ETEST	5008 107Ah	500C 107Ah	5000 207Ah
7Ch	16	EPWM_EPWMREV	5008 107Ch	500C 107Ch	5000 207Ch
7Eh	16	EPWM_HRPWMREV	5008 107Eh	500C 107Eh	5000 207Eh
80h	16	EPWM_AQCTLA	5008 1080h	500C 1080h	5000 2080h
82h	16	EPWM_AQCTLA2	5008 1082h	500C 1082h	5000 2082h
84h	16	EPWM_AQCTLB	5008 1084h	500C 1084h	5000 2084h
86h	16	EPWM_AQCTLB2	5008 1086h	500C 1086h	5000 2086h
8Eh	16	EPWM_AQSFRC	5008 108Eh	500C 108Eh	5000 208Eh
92h	16	EPWM_AQCSFRC	5008 1092h	500C 1092h	5000 2092h
A0h	16	EPWM_DBREDHR	5008 10A0h	500C 10A0h	5000 20A0h
A2h	16	EPWM_DBRED	5008 10A2h	500C 10A2h	5000 20A2h
A4h	16	EPWM_DBFEDHR	5008 10A4h	500C 10A4h	5000 20A4h
A6h	16	EPWM_DBFED	5008 10A6h	500C 10A6h	5000 20A6h
C0h	32	EPWM_TBPHS	5008 10C0h	500C 10C0h	5000 20C0h
C4h	16	EPWM_TBPRDHR	5008 10C4h	500C 10C4h	5000 20C4h
C6h	16	EPWM_TBPRD	5008 10C6h	500C 10C6h	5000 20C6h
C8h	16	EPWM_TBPRDHRB	5008 10C8h	500C 10C8h	5000 20C8h
D4h	32	EPWM_CMPA	5008 10D4h	500C 10D4h	5000 20D4h
D8h	32	EPWM_CMPB	5008 10D8h	500C 10D8h	5000 20D8h
DEh	16	EPWM_CMPC	5008 10DEh	500C 10DEh	5000 20DEh
E2h	16	EPWM_CMPD	5008 10E2h	500C 10E2h	5000 20E2h
E8h	16	EPWM_GLDCTL2	5008 10E8h	500C 10E8h	5000 20E8h
EEh	16	EPWM_SWVDELVAL	5008 10EEh	500C 10EEh	5000 20EEh
100h	16	EPWM_TZSEL	5008 1100h	500C 1100h	5000 2100h
102h	16	EPWM_TZSEL2	5008 1102h	500C 1102h	5000 2102h
104h	16	EPWM_TZDCSEL	5008 1104h	500C 1104h	5000 2104h
108h	16	EPWM_TZCTL	5008 1108h	500C 1108h	5000 2108h
10Ah	16	EPWM_TZCTL2	5008 110Ah	500C 110Ah	5000 210Ah
10Ch	16	EPWM_TZCTLDCA	5008 110Ch	500C 110Ch	5000 210Ch
10Eh	16	EPWM_TZCTLDCB	5008 110Eh	500C 110Eh	5000 210Eh
11Ah	16	EPWM_TZEINT	5008 111Ah	500C 111Ah	5000 211Ah
126h	16	EPWM_TZFLG	5008 1126h	500C 1126h	5000 2126h
128h	16	EPWM_TZCBCFLG	5008 1128h	500C 1128h	5000 2128h
12Ah	16	EPWM_TZOSTFLG	5008 112Ah	500C 112Ah	5000 212Ah
12Eh	16	EPWM_TZCLR	5008 112Eh	500C 112Eh	5000 212Eh
130h	16	EPWM_TZCBCCLR	5008 1130h	500C 1130h	5000 2130h
132h	16	EPWM_TZOSTCLR	5008 1132h	500C 1132h	5000 2132h
136h	16	EPWM_TZFRC	5008 1136h	500C 1136h	5000 2136h

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Table 3-572. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM06_G0 Physical Address	EPWM07_G0 Physical Address	EPWM08_G0 Physical Address
13Ah	16	EPWM_TZTRIPOUTSEL	5008 113Ah	500C 113Ah	5000 213Ah
148h	16	EPWM_ETSEL	5008 1148h	500C 1148h	5000 2148h
14Ch	16	EPWM_ETPS	5008 114Ch	500C 114Ch	5000 214Ch
150h	16	EPWM_ETFLG	5008 1150h	500C 1150h	5000 2150h
154h	16	EPWM_ETCLR	5008 1154h	500C 1154h	5000 2154h
158h	16	EPWM_ETFRC	5008 1158h	500C 1158h	5000 2158h
15Ch	16	EPWM_ETINTPS	5008 115Ch	500C 115Ch	5000 215Ch
160h	16	EPWM_ETSOCPS	5008 1160h	500C 1160h	5000 2160h
164h	16	EPWM_ETCNTINITCTL	5008 1164h	500C 1164h	5000 2164h
168h	16	EPWM_ETCNTINIT	5008 1168h	500C 1168h	5000 2168h
16Ch	16	EPWM_ETINTMIXEN	5008 116Ch	500C 116Ch	5000 216Ch
170h	16	EPWM_ETSOCAMIXEN	5008 1170h	500C 1170h	5000 2170h
174h	16	EPWM_ETSOCBMIXEN	5008 1174h	500C 1174h	5000 2174h
180h	16	EPWM_DCTRIPSEL	5008 1180h	500C 1180h	5000 2180h
186h	16	EPWM_DCACTL	5008 1186h	500C 1186h	5000 2186h
188h	16	EPWM_DCBCTL	5008 1188h	500C 1188h	5000 2188h
18Eh	16	EPWM_DCFCTL	5008 118Eh	500C 118Eh	5000 218Eh
190h	16	EPWM_DCCAPCTL	5008 1190h	500C 1190h	5000 2190h
192h	16	EPWM_DCFOFFSET	5008 1192h	500C 1192h	5000 2192h
194h	16	EPWM_DCFOFFSETCNT	5008 1194h	500C 1194h	5000 2194h
196h	16	EPWM_DCFWINDOW	5008 1196h	500C 1196h	5000 2196h
198h	16	EPWM_DCFWINDOWCNT	5008 1198h	500C 1198h	5000 2198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5008 119Ah	500C 119Ah	5000 219Ah
19Ch	16	EPWM_DCCAPMIXSEL	5008 119Ch	500C 119Ch	5000 219Ch
19Eh	16	EPWM_DCCAP	5008 119Eh	500C 119Eh	5000 219Eh
1A4h	16	EPWM_DCAHTRIPSEL	5008 11A4h	500C 11A4h	5000 21A4h
1A6h	16	EPWM_DCALTRIPSEL	5008 11A6h	500C 11A6h	5000 21A6h
1A8h	16	EPWM_DCBHTRIPSEL	5008 11A8h	500C 11A8h	5000 21A8h
1AAh	16	EPWM_DCBLTRIPSEL	5008 11AAh	500C 11AAh	5000 21AAh
1ACh	16	EPWM_CAPCTL	5008 11ACh	500C 11ACh	5000 21ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5008 11AEh	500C 11AEh	5000 21AEh
1B0h	16	EPWM_CAPINTRIPSEL	5008 11B0h	500C 11B0h	5000 21B0h
1B2h	16	EPWM_CAPTRIPSEL	5008 11B2h	500C 11B2h	5000 21B2h
1F4h	32	EPWM_EPWMLOCK	5008 11F4h	500C 11F4h	5000 21F4h
1FAh	16	EPWM_HWVDELVAL	5008 11FAh	500C 11FAh	5000 21FAh
1FCh	16	EPWM_VCNTVAL	5008 11FCh	500C 11FCh	5000 21FCh
400h	32	EPWM_XCMPCTL1	5008 1400h	500C 1400h	5000 2400h
410h	32	EPWM_XLOADCTL	5008 1410h	500C 1410h	5000 2410h
418h	32	EPWM_XLOAD	5008 1418h	500C 1418h	5000 2418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5008 141Ch	500C 141Ch	5000 241Ch
420h	32	EPWM_XREGSHDW1STS	5008 1420h	500C 1420h	5000 2420h
428h	32	EPWM_XREGSHDW2STS	5008 1428h	500C 1428h	5000 2428h
430h	32	EPWM_XREGSHDW3STS	5008 1430h	500C 1430h	5000 2430h
600h	32	EPWM_XCMP1_ACTIVE	5008 1600h	500C 1600h	5000 2600h
604h	32	EPWM_XCMP2_ACTIVE	5008 1604h	500C 1604h	5000 2604h
608h	32	EPWM_XCMP3_ACTIVE	5008 1608h	500C 1608h	5000 2608h

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Table 3-572. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM06_G0 Physical Address	EPWM07_G0 Physical Address	EPWM08_G0 Physical Address
60Ch	32	EPWM_XCMP4_ACTIVE	5008 160Ch	500C 160Ch	5000 260Ch
610h	32	EPWM_XCMP5_ACTIVE	5008 1610h	500C 1610h	5000 2610h
614h	32	EPWM_XCMP6_ACTIVE	5008 1614h	500C 1614h	5000 2614h
618h	32	EPWM_XCMP7_ACTIVE	5008 1618h	500C 1618h	5000 2618h
61Ch	32	EPWM_XCMP8_ACTIVE	5008 161Ch	500C 161Ch	5000 261Ch
620h	32	EPWM_XTBPRD_ACTIVE	5008 1620h	500C 1620h	5000 2620h
630h	16	EPWM_XAQCTLA_ACTIVE	5008 1630h	500C 1630h	5000 2630h
644h	32	EPWM_XMINMAX_ACTIVE	5008 1644h	500C 1644h	5000 2644h
680h	32	EPWM_XCMP1_SHDW1	5008 1680h	500C 1680h	5000 2680h
684h	32	EPWM_XCMP2_SHDW1	5008 1684h	500C 1684h	5000 2684h
688h	32	EPWM_XCMP3_SHDW1	5008 1688h	500C 1688h	5000 2688h
68Ch	32	EPWM_XCMP4_SHDW1	5008 168Ch	500C 168Ch	5000 268Ch
690h	32	EPWM_XCMP5_SHDW1	5008 1690h	500C 1690h	5000 2690h
694h	32	EPWM_XCMP6_SHDW1	5008 1694h	500C 1694h	5000 2694h
698h	32	EPWM_XCMP7_SHDW1	5008 1698h	500C 1698h	5000 2698h
69Ch	32	EPWM_XCMP8_SHDW1	5008 169Ch	500C 169Ch	5000 269Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5008 16A0h	500C 16A0h	5000 26A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5008 16B0h	500C 16B0h	5000 26B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5008 16B2h	500C 16B2h	5000 26B2h
6BAh	16	EPWM_CMPC_SHDW1	5008 16BAh	500C 16BAh	5000 26BAh
6BEh	16	EPWM_CMPD_SHDW1	5008 16BEh	500C 16BEh	5000 26BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5008 16C4h	500C 16C4h	5000 26C4h
700h	32	EPWM_XCMP1_SHDW2	5008 1700h	500C 1700h	5000 2700h
704h	32	EPWM_XCMP2_SHDW2	5008 1704h	500C 1704h	5000 2704h
708h	32	EPWM_XCMP3_SHDW2	5008 1708h	500C 1708h	5000 2708h
70Ch	32	EPWM_XCMP4_SHDW2	5008 170Ch	500C 170Ch	5000 270Ch
710h	32	EPWM_XCMP5_SHDW2	5008 1710h	500C 1710h	5000 2710h
714h	32	EPWM_XCMP6_SHDW2	5008 1714h	500C 1714h	5000 2714h
718h	32	EPWM_XCMP7_SHDW2	5008 1718h	500C 1718h	5000 2718h
71Ch	32	EPWM_XCMP8_SHDW2	5008 171Ch	500C 171Ch	5000 271Ch
720h	32	EPWM_XTBPRD_SHDW2	5008 1720h	500C 1720h	5000 2720h
730h	16	EPWM_XAQCTLA_SHDW2	5008 1730h	500C 1730h	5000 2730h
732h	16	EPWM_XAQCTLB_SHDW2	5008 1732h	500C 1732h	5000 2732h
73Ah	16	EPWM_CMPC_SHDW2	5008 173Ah	500C 173Ah	5000 273Ah
73Eh	16	EPWM_CMPD_SHDW2	5008 173Eh	500C 173Eh	5000 273Eh
744h	32	EPWM_XMINMAX_SHDW2	5008 1744h	500C 1744h	5000 2744h
780h	32	EPWM_XCMP1_SHDW3	5008 1780h	500C 1780h	5000 2780h
784h	32	EPWM_XCMP2_SHDW3	5008 1784h	500C 1784h	5000 2784h
788h	32	EPWM_XCMP3_SHDW3	5008 1788h	500C 1788h	5000 2788h
78Ch	32	EPWM_XCMP4_SHDW3	5008 178Ch	500C 178Ch	5000 278Ch
790h	32	EPWM_XCMP5_SHDW3	5008 1790h	500C 1790h	5000 2790h
794h	32	EPWM_XCMP6_SHDW3	5008 1794h	500C 1794h	5000 2794h
798h	32	EPWM_XCMP7_SHDW3	5008 1798h	500C 1798h	5000 2798h
79Ch	32	EPWM_XCMP8_SHDW3	5008 179Ch	500C 179Ch	5000 279Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5008 17A0h	500C 17A0h	5000 27A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5008 17B0h	500C 17B0h	5000 27B0h

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Table 3-572. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM06_G0 Physical Address	EPWM07_G0 Physical Address	EPWM08_G0 Physical Address
7B2h	16	EPWM_XAQCTLB_SHDW3	5008 17B2h	500C 17B2h	5000 27B2h
7BAh	16	EPWM_CMPC_SHDW3	5008 17BAh	500C 17BAh	5000 27BAh
7BEh	16	EPWM_CMPD_SHDW3	5008 17BEh	500C 17BEh	5000 27BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5008 17C4h	500C 17C4h	5000 27C4h
800h	32	EPWM_DECTL	5008 1800h	500C 1800h	5000 2800h
804h	32	EPWM_DECOMPSEL	5008 1804h	500C 1804h	5000 2804h
808h	32	EPWM_DEACTCTL	5008 1808h	500C 1808h	5000 2808h
80Ch	32	EPWM_DESTS	5008 180Ch	500C 180Ch	5000 280Ch
810h	32	EPWM_DEFRC	5008 1810h	500C 1810h	5000 2810h
814h	32	EPWM_DECLR	5008 1814h	500C 1814h	5000 2814h
820h	32	EPWM_DEMONCNT	5008 1820h	500C 1820h	5000 2820h
824h	32	EPWM_DEMONCTL	5008 1824h	500C 1824h	5000 2824h
828h	32	EPWM_DEMONSTEP	5008 1828h	500C 1828h	5000 2828h
82Ch	32	EPWM_DEMONTHRES	5008 182Ch	500C 182Ch	5000 282Ch
C00h	32	EPWM_MINDBCFG	5008 1C00h	500C 1C00h	5000 2C00h
C04h	32	EPWM_MINDBDLY	5008 1C04h	500C 1C04h	5000 2C04h
C20h	32	EPWM_LUTCTLA	5008 1C20h	500C 1C20h	5000 2C20h
C24h	32	EPWM_LUTCTLB	5008 1C24h	500C 1C24h	5000 2C24h

Table 3-573. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM09_G0 Physical Address	EPWM10_G0 Physical Address	EPWM11_G0 Physical Address
0h	16	EPWM_TBCTL	5004 2000h	5008 2000h	500C 2000h
2h	16	EPWM_TBCTL2	5004 2002h	5008 2002h	500C 2002h
6h	16	EPWM_EPWMSYNCINSEL	5004 2006h	5008 2006h	500C 2006h
8h	16	EPWM_TBCTR	5004 2008h	5008 2008h	500C 2008h
Ah	16	EPWM_TBSTS	5004 200Ah	5008 200Ah	500C 200Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5004 200Ch	5008 200Ch	500C 200Ch
Eh	16	EPWM_TBCTL3	5004 200Eh	5008 200Eh	500C 200Eh
10h	16	EPWM_CMPCTL	5004 2010h	5008 2010h	500C 2010h
12h	16	EPWM_CMPCTL2	5004 2012h	5008 2012h	500C 2012h
18h	16	EPWM_DBCTL	5004 2018h	5008 2018h	500C 2018h
1Ah	16	EPWM_DBCTL2	5004 201Ah	5008 201Ah	500C 201Ah
20h	16	EPWM_AQCTL	5004 2020h	5008 2020h	500C 2020h
22h	16	EPWM_AQTSRCSEL	5004 2022h	5008 2022h	500C 2022h
28h	16	EPWM_PCCTL	5004 2028h	5008 2028h	500C 2028h
30h	16	EPWM_VCAPCTL	5004 2030h	5008 2030h	500C 2030h
32h	16	EPWM_VCNTCFG	5004 2032h	5008 2032h	500C 2032h
40h	16	EPWM_HRCNFG	5004 2040h	5008 2040h	500C 2040h
4Eh	16	EPWM_HRCNFG2	5004 204Eh	5008 204Eh	500C 204Eh
5Ah	16	EPWM_HRPCTL	5004 205Ah	5008 205Ah	500C 205Ah
5Ch	16	EPWM_TRREM	5004 205Ch	5008 205Ch	500C 205Ch
68h	16	EPWM_GLDCTL	5004 2068h	5008 2068h	500C 2068h
6Ah	16	EPWM_GLDCFG	5004 206Ah	5008 206Ah	500C 206Ah
70h	32	EPWM_EPWMXLINK	5004 2070h	5008 2070h	500C 2070h
74h	32	EPWM_EPWMXLINK2	5004 2074h	5008 2074h	500C 2074h

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Table 3-573. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM09_G0 Physical Address	EPWM10_G0 Physical Address	EPWM11_G0 Physical Address
7Ah	16	EPWM_ETEST	5004 207Ah	5008 207Ah	500C 207Ah
7Ch	16	EPWM_EPWMREV	5004 207Ch	5008 207Ch	500C 207Ch
7Eh	16	EPWM_HRPWMREV	5004 207Eh	5008 207Eh	500C 207Eh
80h	16	EPWM_AQCTLA	5004 2080h	5008 2080h	500C 2080h
82h	16	EPWM_AQCTLA2	5004 2082h	5008 2082h	500C 2082h
84h	16	EPWM_AQCTLB	5004 2084h	5008 2084h	500C 2084h
86h	16	EPWM_AQCTLB2	5004 2086h	5008 2086h	500C 2086h
8Eh	16	EPWM_AQSFRC	5004 208Eh	5008 208Eh	500C 208Eh
92h	16	EPWM_AQCSFRC	5004 2092h	5008 2092h	500C 2092h
A0h	16	EPWM_DBREDHR	5004 20A0h	5008 20A0h	500C 20A0h
A2h	16	EPWM_DBRED	5004 20A2h	5008 20A2h	500C 20A2h
A4h	16	EPWM_DBFEDHR	5004 20A4h	5008 20A4h	500C 20A4h
A6h	16	EPWM_DBFED	5004 20A6h	5008 20A6h	500C 20A6h
C0h	32	EPWM_TBPHS	5004 20C0h	5008 20C0h	500C 20C0h
C4h	16	EPWM_TBPRDHR	5004 20C4h	5008 20C4h	500C 20C4h
C6h	16	EPWM_TBPRD	5004 20C6h	5008 20C6h	500C 20C6h
C8h	16	EPWM_TBPRDHRB	5004 20C8h	5008 20C8h	500C 20C8h
D4h	32	EPWM_CMPA	5004 20D4h	5008 20D4h	500C 20D4h
D8h	32	EPWM_CMPB	5004 20D8h	5008 20D8h	500C 20D8h
DEh	16	EPWM_CMPC	5004 20DEh	5008 20DEh	500C 20DEh
E2h	16	EPWM_CMPD	5004 20E2h	5008 20E2h	500C 20E2h
E8h	16	EPWM_GLDCTL2	5004 20E8h	5008 20E8h	500C 20E8h
EEh	16	EPWM_SWVDELVAL	5004 20EEh	5008 20EEh	500C 20EEh
100h	16	EPWM_TZSEL	5004 2100h	5008 2100h	500C 2100h
102h	16	EPWM_TZSEL2	5004 2102h	5008 2102h	500C 2102h
104h	16	EPWM_TZDCSEL	5004 2104h	5008 2104h	500C 2104h
108h	16	EPWM_TZCTL	5004 2108h	5008 2108h	500C 2108h
10Ah	16	EPWM_TZCTL2	5004 210Ah	5008 210Ah	500C 210Ah
10Ch	16	EPWM_TZCTLDCA	5004 210Ch	5008 210Ch	500C 210Ch
10Eh	16	EPWM_TZCTLDCB	5004 210Eh	5008 210Eh	500C 210Eh
11Ah	16	EPWM_TZEINT	5004 211Ah	5008 211Ah	500C 211Ah
126h	16	EPWM_TZFLG	5004 2126h	5008 2126h	500C 2126h
128h	16	EPWM_TZCBCFLG	5004 2128h	5008 2128h	500C 2128h
12Ah	16	EPWM_TZOSTFLG	5004 212Ah	5008 212Ah	500C 212Ah
12Eh	16	EPWM_TZCLR	5004 212Eh	5008 212Eh	500C 212Eh
130h	16	EPWM_TZCBCCLR	5004 2130h	5008 2130h	500C 2130h
132h	16	EPWM_TZOSTCLR	5004 2132h	5008 2132h	500C 2132h
136h	16	EPWM_TZFRC	5004 2136h	5008 2136h	500C 2136h
13Ah	16	EPWM_TZTRIPOUTSEL	5004 213Ah	5008 213Ah	500C 213Ah
148h	16	EPWM_ETSEL	5004 2148h	5008 2148h	500C 2148h
14Ch	16	EPWM_ETPS	5004 214Ch	5008 214Ch	500C 214Ch
150h	16	EPWM_ETFLG	5004 2150h	5008 2150h	500C 2150h
154h	16	EPWM_ETCLR	5004 2154h	5008 2154h	500C 2154h
158h	16	EPWM_ETFRC	5004 2158h	5008 2158h	500C 2158h
15Ch	16	EPWM_ETINTPS	5004 215Ch	5008 215Ch	500C 215Ch
160h	16	EPWM_ETSOCPS	5004 2160h	5008 2160h	500C 2160h

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Table 3-573. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM09_G0 Physical Address	EPWM10_G0 Physical Address	EPWM11_G0 Physical Address
164h	16	EPWM_ETCNTINITCTL	5004 2164h	5008 2164h	500C 2164h
168h	16	EPWM_ETCNTINIT	5004 2168h	5008 2168h	500C 2168h
16Ch	16	EPWM_ETINTMIXEN	5004 216Ch	5008 216Ch	500C 216Ch
170h	16	EPWM_ETSOCAMIXEN	5004 2170h	5008 2170h	500C 2170h
174h	16	EPWM_ETSOCBMIXEN	5004 2174h	5008 2174h	500C 2174h
180h	16	EPWM_DCTRIPSEL	5004 2180h	5008 2180h	500C 2180h
186h	16	EPWM_DCACTL	5004 2186h	5008 2186h	500C 2186h
188h	16	EPWM_DCBCTL	5004 2188h	5008 2188h	500C 2188h
18Eh	16	EPWM_DCFCTL	5004 218Eh	5008 218Eh	500C 218Eh
190h	16	EPWM_DCCAPCTL	5004 2190h	5008 2190h	500C 2190h
192h	16	EPWM_DCFOFFSET	5004 2192h	5008 2192h	500C 2192h
194h	16	EPWM_DCFOFFSETCNT	5004 2194h	5008 2194h	500C 2194h
196h	16	EPWM_DCFWINDOW	5004 2196h	5008 2196h	500C 2196h
198h	16	EPWM_DCFWINDOWCNT	5004 2198h	5008 2198h	500C 2198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5004 219Ah	5008 219Ah	500C 219Ah
19Ch	16	EPWM_DCCAPMIXSEL	5004 219Ch	5008 219Ch	500C 219Ch
19Eh	16	EPWM_DCCAP	5004 219Eh	5008 219Eh	500C 219Eh
1A4h	16	EPWM_DCAHTRIPSEL	5004 21A4h	5008 21A4h	500C 21A4h
1A6h	16	EPWM_DCALTRIPSEL	5004 21A6h	5008 21A6h	500C 21A6h
1A8h	16	EPWM_DCBHTRIPSEL	5004 21A8h	5008 21A8h	500C 21A8h
1AAh	16	EPWM_DCBLTRIPSEL	5004 21AAh	5008 21AAh	500C 21AAh
1ACh	16	EPWM_CAPCTL	5004 21ACh	5008 21ACh	500C 21ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5004 21AEh	5008 21AEh	500C 21AEh
1B0h	16	EPWM_CAPINTRIPSEL	5004 21B0h	5008 21B0h	500C 21B0h
1B2h	16	EPWM_CAPTRIPSEL	5004 21B2h	5008 21B2h	500C 21B2h
1F4h	32	EPWM_EPWMLOCK	5004 21F4h	5008 21F4h	500C 21F4h
1FAh	16	EPWM_HWVDELVAL	5004 21FAh	5008 21FAh	500C 21FAh
1FCh	16	EPWM_VCNTVAL	5004 21FCh	5008 21FCh	500C 21FCh
400h	32	EPWM_XCMPCTL1	5004 2400h	5008 2400h	500C 2400h
410h	32	EPWM_XLOADCTL	5004 2410h	5008 2410h	500C 2410h
418h	32	EPWM_XLOAD	5004 2418h	5008 2418h	500C 2418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5004 241Ch	5008 241Ch	500C 241Ch
420h	32	EPWM_XREGSHDW1STS	5004 2420h	5008 2420h	500C 2420h
428h	32	EPWM_XREGSHDW2STS	5004 2428h	5008 2428h	500C 2428h
430h	32	EPWM_XREGSHDW3STS	5004 2430h	5008 2430h	500C 2430h
600h	32	EPWM_XCMP1_ACTIVE	5004 2600h	5008 2600h	500C 2600h
604h	32	EPWM_XCMP2_ACTIVE	5004 2604h	5008 2604h	500C 2604h
608h	32	EPWM_XCMP3_ACTIVE	5004 2608h	5008 2608h	500C 2608h
60Ch	32	EPWM_XCMP4_ACTIVE	5004 260Ch	5008 260Ch	500C 260Ch
610h	32	EPWM_XCMP5_ACTIVE	5004 2610h	5008 2610h	500C 2610h
614h	32	EPWM_XCMP6_ACTIVE	5004 2614h	5008 2614h	500C 2614h
618h	32	EPWM_XCMP7_ACTIVE	5004 2618h	5008 2618h	500C 2618h
61Ch	32	EPWM_XCMP8_ACTIVE	5004 261Ch	5008 261Ch	500C 261Ch
620h	32	EPWM_XTBPRD_ACTIVE	5004 2620h	5008 2620h	500C 2620h
630h	16	EPWM_XAQCTLA_ACTIVE	5004 2630h	5008 2630h	500C 2630h
644h	32	EPWM_XMINMAX_ACTIVE	5004 2644h	5008 2644h	500C 2644h

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Table 3-573. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM09_G0 Physical Address	EPWM10_G0 Physical Address	EPWM11_G0 Physical Address
680h	32	EPWM_XCMP1_SHDW1	5004 2680h	5008 2680h	500C 2680h
684h	32	EPWM_XCMP2_SHDW1	5004 2684h	5008 2684h	500C 2684h
688h	32	EPWM_XCMP3_SHDW1	5004 2688h	5008 2688h	500C 2688h
68Ch	32	EPWM_XCMP4_SHDW1	5004 268Ch	5008 268Ch	500C 268Ch
690h	32	EPWM_XCMP5_SHDW1	5004 2690h	5008 2690h	500C 2690h
694h	32	EPWM_XCMP6_SHDW1	5004 2694h	5008 2694h	500C 2694h
698h	32	EPWM_XCMP7_SHDW1	5004 2698h	5008 2698h	500C 2698h
69Ch	32	EPWM_XCMP8_SHDW1	5004 269Ch	5008 269Ch	500C 269Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5004 26A0h	5008 26A0h	500C 26A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5004 26B0h	5008 26B0h	500C 26B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5004 26B2h	5008 26B2h	500C 26B2h
6BAh	16	EPWM_CMPC_SHDW1	5004 26BAh	5008 26BAh	500C 26BAh
6BEh	16	EPWM_CMPD_SHDW1	5004 26BEh	5008 26BEh	500C 26BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5004 26C4h	5008 26C4h	500C 26C4h
700h	32	EPWM_XCMP1_SHDW2	5004 2700h	5008 2700h	500C 2700h
704h	32	EPWM_XCMP2_SHDW2	5004 2704h	5008 2704h	500C 2704h
708h	32	EPWM_XCMP3_SHDW2	5004 2708h	5008 2708h	500C 2708h
70Ch	32	EPWM_XCMP4_SHDW2	5004 270Ch	5008 270Ch	500C 270Ch
710h	32	EPWM_XCMP5_SHDW2	5004 2710h	5008 2710h	500C 2710h
714h	32	EPWM_XCMP6_SHDW2	5004 2714h	5008 2714h	500C 2714h
718h	32	EPWM_XCMP7_SHDW2	5004 2718h	5008 2718h	500C 2718h
71Ch	32	EPWM_XCMP8_SHDW2	5004 271Ch	5008 271Ch	500C 271Ch
720h	32	EPWM_XTBPRD_SHDW2	5004 2720h	5008 2720h	500C 2720h
730h	16	EPWM_XAQCTLA_SHDW2	5004 2730h	5008 2730h	500C 2730h
732h	16	EPWM_XAQCTLB_SHDW2	5004 2732h	5008 2732h	500C 2732h
73Ah	16	EPWM_CMPC_SHDW2	5004 273Ah	5008 273Ah	500C 273Ah
73Eh	16	EPWM_CMPD_SHDW2	5004 273Eh	5008 273Eh	500C 273Eh
744h	32	EPWM_XMINMAX_SHDW2	5004 2744h	5008 2744h	500C 2744h
780h	32	EPWM_XCMP1_SHDW3	5004 2780h	5008 2780h	500C 2780h
784h	32	EPWM_XCMP2_SHDW3	5004 2784h	5008 2784h	500C 2784h
788h	32	EPWM_XCMP3_SHDW3	5004 2788h	5008 2788h	500C 2788h
78Ch	32	EPWM_XCMP4_SHDW3	5004 278Ch	5008 278Ch	500C 278Ch
790h	32	EPWM_XCMP5_SHDW3	5004 2790h	5008 2790h	500C 2790h
794h	32	EPWM_XCMP6_SHDW3	5004 2794h	5008 2794h	500C 2794h
798h	32	EPWM_XCMP7_SHDW3	5004 2798h	5008 2798h	500C 2798h
79Ch	32	EPWM_XCMP8_SHDW3	5004 279Ch	5008 279Ch	500C 279Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5004 27A0h	5008 27A0h	500C 27A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5004 27B0h	5008 27B0h	500C 27B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5004 27B2h	5008 27B2h	500C 27B2h
7BAh	16	EPWM_CMPC_SHDW3	5004 27BAh	5008 27BAh	500C 27BAh
7BEh	16	EPWM_CMPD_SHDW3	5004 27BEh	5008 27BEh	500C 27BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5004 27C4h	5008 27C4h	500C 27C4h
800h	32	EPWM_DECTL	5004 2800h	5008 2800h	500C 2800h
804h	32	EPWM_DECOMPSEL	5004 2804h	5008 2804h	500C 2804h
808h	32	EPWM_DEACTCTL	5004 2808h	5008 2808h	500C 2808h
80Ch	32	EPWM_DESTS	5004 280Ch	5008 280Ch	500C 280Ch

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Table 3-573. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM09_G0 Physical Address	EPWM10_G0 Physical Address	EPWM11_G0 Physical Address
810h	32	EPWM_DEFRC	5004 2810h	5008 2810h	500C 2810h
814h	32	EPWM_DECLR	5004 2814h	5008 2814h	500C 2814h
820h	32	EPWM_DEMONCNT	5004 2820h	5008 2820h	500C 2820h
824h	32	EPWM_DEMONCTL	5004 2824h	5008 2824h	500C 2824h
828h	32	EPWM_DEMONSTEP	5004 2828h	5008 2828h	500C 2828h
82Ch	32	EPWM_DEMONTHRES	5004 282Ch	5008 282Ch	500C 282Ch
C00h	32	EPWM_MINDBCFG	5004 2C00h	5008 2C00h	500C 2C00h
C04h	32	EPWM_MINDBDLY	5004 2C04h	5008 2C04h	500C 2C04h
C20h	32	EPWM_LUTCTLA	5004 2C20h	5008 2C20h	500C 2C20h
C24h	32	EPWM_LUTCTLB	5004 2C24h	5008 2C24h	500C 2C24h

Table 3-574. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM12_G0 Physical Address	EPWM13_G0 Physical Address	EPWM14_G0 Physical Address
0h	16	EPWM_TBCTL	5000 3000h	5004 3000h	5008 3000h
2h	16	EPWM_TBCTL2	5000 3002h	5004 3002h	5008 3002h
6h	16	EPWM_EPWMSYNCINSEL	5000 3006h	5004 3006h	5008 3006h
8h	16	EPWM_TBCTR	5000 3008h	5004 3008h	5008 3008h
Ah	16	EPWM_TBSTS	5000 300Ah	5004 300Ah	5008 300Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5000 300Ch	5004 300Ch	5008 300Ch
Eh	16	EPWM_TBCTL3	5000 300Eh	5004 300Eh	5008 300Eh
10h	16	EPWM_CMPCTL	5000 3010h	5004 3010h	5008 3010h
12h	16	EPWM_CMPCTL2	5000 3012h	5004 3012h	5008 3012h
18h	16	EPWM_DBCTL	5000 3018h	5004 3018h	5008 3018h
1Ah	16	EPWM_DBCTL2	5000 301Ah	5004 301Ah	5008 301Ah
20h	16	EPWM_AQCTL	5000 3020h	5004 3020h	5008 3020h
22h	16	EPWM_AQTSRCSEL	5000 3022h	5004 3022h	5008 3022h
28h	16	EPWM_PCCTL	5000 3028h	5004 3028h	5008 3028h
30h	16	EPWM_VCAPCTL	5000 3030h	5004 3030h	5008 3030h
32h	16	EPWM_VCNTCFG	5000 3032h	5004 3032h	5008 3032h
40h	16	EPWM_HRCNFG	5000 3040h	5004 3040h	5008 3040h
4Eh	16	EPWM_HRCNFG2	5000 304Eh	5004 304Eh	5008 304Eh
5Ah	16	EPWM_HRPCTL	5000 305Ah	5004 305Ah	5008 305Ah
5Ch	16	EPWM_TRREM	5000 305Ch	5004 305Ch	5008 305Ch
68h	16	EPWM_GLDCTL	5000 3068h	5004 3068h	5008 3068h
6Ah	16	EPWM_GLDCFG	5000 306Ah	5004 306Ah	5008 306Ah
70h	32	EPWM_EPWMXLINK	5000 3070h	5004 3070h	5008 3070h
74h	32	EPWM_EPWMXLINK2	5000 3074h	5004 3074h	5008 3074h
7Ah	16	EPWM_ETEST	5000 307Ah	5004 307Ah	5008 307Ah
7Ch	16	EPWM_EPWMREV	5000 307Ch	5004 307Ch	5008 307Ch
7Eh	16	EPWM_HRPWMREV	5000 307Eh	5004 307Eh	5008 307Eh
80h	16	EPWM_AQCTLA	5000 3080h	5004 3080h	5008 3080h
82h	16	EPWM_AQCTLA2	5000 3082h	5004 3082h	5008 3082h
84h	16	EPWM_AQCTLB	5000 3084h	5004 3084h	5008 3084h
86h	16	EPWM_AQCTLB2	5000 3086h	5004 3086h	5008 3086h
8Eh	16	EPWM_AQSFRC	5000 308Eh	5004 308Eh	5008 308Eh

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Table 3-574. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM12_G0 Physical Address	EPWM13_G0 Physical Address	EPWM14_G0 Physical Address
92h	16	EPWM_AQCSFRC	5000 3092h	5004 3092h	5008 3092h
A0h	16	EPWM_DBREDHR	5000 30A0h	5004 30A0h	5008 30A0h
A2h	16	EPWM_DBRED	5000 30A2h	5004 30A2h	5008 30A2h
A4h	16	EPWM_DBFEDHR	5000 30A4h	5004 30A4h	5008 30A4h
A6h	16	EPWM_DBFED	5000 30A6h	5004 30A6h	5008 30A6h
C0h	32	EPWM_TBPHS	5000 30C0h	5004 30C0h	5008 30C0h
C4h	16	EPWM_TBPRDHR	5000 30C4h	5004 30C4h	5008 30C4h
C6h	16	EPWM_TBPRD	5000 30C6h	5004 30C6h	5008 30C6h
C8h	16	EPWM_TBPRDHRB	5000 30C8h	5004 30C8h	5008 30C8h
D4h	32	EPWM_CMPA	5000 30D4h	5004 30D4h	5008 30D4h
D8h	32	EPWM_CMPB	5000 30D8h	5004 30D8h	5008 30D8h
DEh	16	EPWM_CMPC	5000 30DEh	5004 30DEh	5008 30DEh
E2h	16	EPWM_CMPD	5000 30E2h	5004 30E2h	5008 30E2h
E8h	16	EPWM_GLDCTL2	5000 30E8h	5004 30E8h	5008 30E8h
EEh	16	EPWM_SWVDELVAL	5000 30EEh	5004 30EEh	5008 30EEh
100h	16	EPWM_TZSEL	5000 3100h	5004 3100h	5008 3100h
102h	16	EPWM_TZSEL2	5000 3102h	5004 3102h	5008 3102h
104h	16	EPWM_TZDCSEL	5000 3104h	5004 3104h	5008 3104h
108h	16	EPWM_TZCTL	5000 3108h	5004 3108h	5008 3108h
10Ah	16	EPWM_TZCTL2	5000 310Ah	5004 310Ah	5008 310Ah
10Ch	16	EPWM_TZCTLDCA	5000 310Ch	5004 310Ch	5008 310Ch
10Eh	16	EPWM_TZCTLDCB	5000 310Eh	5004 310Eh	5008 310Eh
11Ah	16	EPWM_TZEINT	5000 311Ah	5004 311Ah	5008 311Ah
126h	16	EPWM_TZFLG	5000 3126h	5004 3126h	5008 3126h
128h	16	EPWM_TZCBCFLG	5000 3128h	5004 3128h	5008 3128h
12Ah	16	EPWM_TZOSTFLG	5000 312Ah	5004 312Ah	5008 312Ah
12Eh	16	EPWM_TZCLR	5000 312Eh	5004 312Eh	5008 312Eh
130h	16	EPWM_TZCBCCLR	5000 3130h	5004 3130h	5008 3130h
132h	16	EPWM_TZOSTCLR	5000 3132h	5004 3132h	5008 3132h
136h	16	EPWM_TZFRC	5000 3136h	5004 3136h	5008 3136h
13Ah	16	EPWM_TZTRIPOUTSEL	5000 313Ah	5004 313Ah	5008 313Ah
148h	16	EPWM_ETSEL	5000 3148h	5004 3148h	5008 3148h
14Ch	16	EPWM_ETPS	5000 314Ch	5004 314Ch	5008 314Ch
150h	16	EPWM_ETFLG	5000 3150h	5004 3150h	5008 3150h
154h	16	EPWM_ETCLR	5000 3154h	5004 3154h	5008 3154h
158h	16	EPWM_ETFRC	5000 3158h	5004 3158h	5008 3158h
15Ch	16	EPWM_ETINTPS	5000 315Ch	5004 315Ch	5008 315Ch
160h	16	EPWM_ETSOCPS	5000 3160h	5004 3160h	5008 3160h
164h	16	EPWM_ETCNTINITCTL	5000 3164h	5004 3164h	5008 3164h
168h	16	EPWM_ETCNTINIT	5000 3168h	5004 3168h	5008 3168h
16Ch	16	EPWM_ETINTMIXEN	5000 316Ch	5004 316Ch	5008 316Ch
170h	16	EPWM_ETSOCAMIXEN	5000 3170h	5004 3170h	5008 3170h
174h	16	EPWM_ETSOCBMIXEN	5000 3174h	5004 3174h	5008 3174h
180h	16	EPWM_DCTRIPSEL	5000 3180h	5004 3180h	5008 3180h
186h	16	EPWM_DCACTL	5000 3186h	5004 3186h	5008 3186h
188h	16	EPWM_DCBCTL	5000 3188h	5004 3188h	5008 3188h

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Table 3-574. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM12_G0 Physical Address	EPWM13_G0 Physical Address	EPWM14_G0 Physical Address
18Eh	16	EPWM_DCFCTL	5000 318Eh	5004 318Eh	5008 318Eh
190h	16	EPWM_DCCAPCTL	5000 3190h	5004 3190h	5008 3190h
192h	16	EPWM_DCFOFFSET	5000 3192h	5004 3192h	5008 3192h
194h	16	EPWM_DCFOFFSETCNT	5000 3194h	5004 3194h	5008 3194h
196h	16	EPWM_DCFWINDOW	5000 3196h	5004 3196h	5008 3196h
198h	16	EPWM_DCFWINDOWCNT	5000 3198h	5004 3198h	5008 3198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5000 319Ah	5004 319Ah	5008 319Ah
19Ch	16	EPWM_DCCAPMIXSEL	5000 319Ch	5004 319Ch	5008 319Ch
19Eh	16	EPWM_DCCAP	5000 319Eh	5004 319Eh	5008 319Eh
1A4h	16	EPWM_DCAHTRIPSEL	5000 31A4h	5004 31A4h	5008 31A4h
1A6h	16	EPWM_DCALTRIPSEL	5000 31A6h	5004 31A6h	5008 31A6h
1A8h	16	EPWM_DCBHTRIPSEL	5000 31A8h	5004 31A8h	5008 31A8h
1AAh	16	EPWM_DCBLTRIPSEL	5000 31AAh	5004 31AAh	5008 31AAh
1ACh	16	EPWM_CAPCTL	5000 31ACh	5004 31ACh	5008 31ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5000 31AEh	5004 31AEh	5008 31AEh
1B0h	16	EPWM_CAPINTRIPSEL	5000 31B0h	5004 31B0h	5008 31B0h
1B2h	16	EPWM_CAPTRIPSEL	5000 31B2h	5004 31B2h	5008 31B2h
1F4h	32	EPWM_EPWMLOCK	5000 31F4h	5004 31F4h	5008 31F4h
1FAh	16	EPWM_HWVDELVAL	5000 31FAh	5004 31FAh	5008 31FAh
1FCh	16	EPWM_VCNTVAL	5000 31FCh	5004 31FCh	5008 31FCh
400h	32	EPWM_XCMPCTL1	5000 3400h	5004 3400h	5008 3400h
410h	32	EPWM_XLOADCTL	5000 3410h	5004 3410h	5008 3410h
418h	32	EPWM_XLOAD	5000 3418h	5004 3418h	5008 3418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5000 341Ch	5004 341Ch	5008 341Ch
420h	32	EPWM_XREGSHDW1STS	5000 3420h	5004 3420h	5008 3420h
428h	32	EPWM_XREGSHDW2STS	5000 3428h	5004 3428h	5008 3428h
430h	32	EPWM_XREGSHDW3STS	5000 3430h	5004 3430h	5008 3430h
600h	32	EPWM_XCMP1_ACTIVE	5000 3600h	5004 3600h	5008 3600h
604h	32	EPWM_XCMP2_ACTIVE	5000 3604h	5004 3604h	5008 3604h
608h	32	EPWM_XCMP3_ACTIVE	5000 3608h	5004 3608h	5008 3608h
60Ch	32	EPWM_XCMP4_ACTIVE	5000 360Ch	5004 360Ch	5008 360Ch
610h	32	EPWM_XCMP5_ACTIVE	5000 3610h	5004 3610h	5008 3610h
614h	32	EPWM_XCMP6_ACTIVE	5000 3614h	5004 3614h	5008 3614h
618h	32	EPWM_XCMP7_ACTIVE	5000 3618h	5004 3618h	5008 3618h
61Ch	32	EPWM_XCMP8_ACTIVE	5000 361Ch	5004 361Ch	5008 361Ch
620h	32	EPWM_XTBPRD_ACTIVE	5000 3620h	5004 3620h	5008 3620h
630h	16	EPWM_XAQCTLA_ACTIVE	5000 3630h	5004 3630h	5008 3630h
644h	32	EPWM_XMINMAX_ACTIVE	5000 3644h	5004 3644h	5008 3644h
680h	32	EPWM_XCMP1_SHDW1	5000 3680h	5004 3680h	5008 3680h
684h	32	EPWM_XCMP2_SHDW1	5000 3684h	5004 3684h	5008 3684h
688h	32	EPWM_XCMP3_SHDW1	5000 3688h	5004 3688h	5008 3688h
68Ch	32	EPWM_XCMP4_SHDW1	5000 368Ch	5004 368Ch	5008 368Ch
690h	32	EPWM_XCMP5_SHDW1	5000 3690h	5004 3690h	5008 3690h
694h	32	EPWM_XCMP6_SHDW1	5000 3694h	5004 3694h	5008 3694h
698h	32	EPWM_XCMP7_SHDW1	5000 3698h	5004 3698h	5008 3698h
69Ch	32	EPWM_XCMP8_SHDW1	5000 369Ch	5004 369Ch	5008 369Ch

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Table 3-574. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM12_G0 Physical Address	EPWM13_G0 Physical Address	EPWM14_G0 Physical Address
6A0h	32	EPWM_XTBPRD_SHDW1	5000 36A0h	5004 36A0h	5008 36A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5000 36B0h	5004 36B0h	5008 36B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5000 36B2h	5004 36B2h	5008 36B2h
6BAh	16	EPWM_CMPC_SHDW1	5000 36BAh	5004 36BAh	5008 36BAh
6BEh	16	EPWM_CMPD_SHDW1	5000 36BEh	5004 36BEh	5008 36BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5000 36C4h	5004 36C4h	5008 36C4h
700h	32	EPWM_XCMP1_SHDW2	5000 3700h	5004 3700h	5008 3700h
704h	32	EPWM_XCMP2_SHDW2	5000 3704h	5004 3704h	5008 3704h
708h	32	EPWM_XCMP3_SHDW2	5000 3708h	5004 3708h	5008 3708h
70Ch	32	EPWM_XCMP4_SHDW2	5000 370Ch	5004 370Ch	5008 370Ch
710h	32	EPWM_XCMP5_SHDW2	5000 3710h	5004 3710h	5008 3710h
714h	32	EPWM_XCMP6_SHDW2	5000 3714h	5004 3714h	5008 3714h
718h	32	EPWM_XCMP7_SHDW2	5000 3718h	5004 3718h	5008 3718h
71Ch	32	EPWM_XCMP8_SHDW2	5000 371Ch	5004 371Ch	5008 371Ch
720h	32	EPWM_XTBPRD_SHDW2	5000 3720h	5004 3720h	5008 3720h
730h	16	EPWM_XAQCTLA_SHDW2	5000 3730h	5004 3730h	5008 3730h
732h	16	EPWM_XAQCTLB_SHDW2	5000 3732h	5004 3732h	5008 3732h
73Ah	16	EPWM_CMPC_SHDW2	5000 373Ah	5004 373Ah	5008 373Ah
73Eh	16	EPWM_CMPD_SHDW2	5000 373Eh	5004 373Eh	5008 373Eh
744h	32	EPWM_XMINMAX_SHDW2	5000 3744h	5004 3744h	5008 3744h
780h	32	EPWM_XCMP1_SHDW3	5000 3780h	5004 3780h	5008 3780h
784h	32	EPWM_XCMP2_SHDW3	5000 3784h	5004 3784h	5008 3784h
788h	32	EPWM_XCMP3_SHDW3	5000 3788h	5004 3788h	5008 3788h
78Ch	32	EPWM_XCMP4_SHDW3	5000 378Ch	5004 378Ch	5008 378Ch
790h	32	EPWM_XCMP5_SHDW3	5000 3790h	5004 3790h	5008 3790h
794h	32	EPWM_XCMP6_SHDW3	5000 3794h	5004 3794h	5008 3794h
798h	32	EPWM_XCMP7_SHDW3	5000 3798h	5004 3798h	5008 3798h
79Ch	32	EPWM_XCMP8_SHDW3	5000 379Ch	5004 379Ch	5008 379Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5000 37A0h	5004 37A0h	5008 37A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5000 37B0h	5004 37B0h	5008 37B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5000 37B2h	5004 37B2h	5008 37B2h
7BAh	16	EPWM_CMPC_SHDW3	5000 37BAh	5004 37BAh	5008 37BAh
7BEh	16	EPWM_CMPD_SHDW3	5000 37BEh	5004 37BEh	5008 37BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5000 37C4h	5004 37C4h	5008 37C4h
800h	32	EPWM_DECTL	5000 3800h	5004 3800h	5008 3800h
804h	32	EPWM_DECOMPSEL	5000 3804h	5004 3804h	5008 3804h
808h	32	EPWM_DEACTCTL	5000 3808h	5004 3808h	5008 3808h
80Ch	32	EPWM_DESTS	5000 380Ch	5004 380Ch	5008 380Ch
810h	32	EPWM_DEFRC	5000 3810h	5004 3810h	5008 3810h
814h	32	EPWM_DECLR	5000 3814h	5004 3814h	5008 3814h
820h	32	EPWM_DEMONCNT	5000 3820h	5004 3820h	5008 3820h
824h	32	EPWM_DEMONCTL	5000 3824h	5004 3824h	5008 3824h
828h	32	EPWM_DEMONSTEP	5000 3828h	5004 3828h	5008 3828h
82Ch	32	EPWM_DEMONTHRES	5000 382Ch	5004 382Ch	5008 382Ch
C00h	32	EPWM_MINDBCFG	5000 3C00h	5004 3C00h	5008 3C00h
C04h	32	EPWM_MINDBDLY	5000 3C04h	5004 3C04h	5008 3C04h

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Table 3-574. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM12_G0 Physical Address	EPWM13_G0 Physical Address	EPWM14_G0 Physical Address
C20h	32	EPWM_LUTCTLA	5000 3C20h	5004 3C20h	5008 3C20h
C24h	32	EPWM_LUTCTLB	5000 3C24h	5004 3C24h	5008 3C24h

Table 3-575. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM15_G0 Physical Address	EPWM16_G0 Physical Address	EPWM17_G0 Physical Address
0h	16	EPWM_TBCTL	500C 3000h	5000 4000h	5004 4000h
2h	16	EPWM_TBCTL2	500C 3002h	5000 4002h	5004 4002h
6h	16	EPWM_EPWMSYNCINSEL	500C 3006h	5000 4006h	5004 4006h
8h	16	EPWM_TBCTR	500C 3008h	5000 4008h	5004 4008h
Ah	16	EPWM_TBSTS	500C 300Ah	5000 400Ah	5004 400Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500C 300Ch	5000 400Ch	5004 400Ch
Eh	16	EPWM_TBCTL3	500C 300Eh	5000 400Eh	5004 400Eh
10h	16	EPWM_CMPCTL	500C 3010h	5000 4010h	5004 4010h
12h	16	EPWM_CMPCTL2	500C 3012h	5000 4012h	5004 4012h
18h	16	EPWM_DBCTL	500C 3018h	5000 4018h	5004 4018h
1Ah	16	EPWM_DBCTL2	500C 301Ah	5000 401Ah	5004 401Ah
20h	16	EPWM_AQCTL	500C 3020h	5000 4020h	5004 4020h
22h	16	EPWM_AQTSRCSEL	500C 3022h	5000 4022h	5004 4022h
28h	16	EPWM_PCCTL	500C 3028h	5000 4028h	5004 4028h
30h	16	EPWM_VCAPCTL	500C 3030h	5000 4030h	5004 4030h
32h	16	EPWM_VCNTCFG	500C 3032h	5000 4032h	5004 4032h
40h	16	EPWM_HRCNFG	500C 3040h	5000 4040h	5004 4040h
4Eh	16	EPWM_HRCNFG2	500C 304Eh	5000 404Eh	5004 404Eh
5Ah	16	EPWM_HRPCTL	500C 305Ah	5000 405Ah	5004 405Ah
5Ch	16	EPWM_TRREM	500C 305Ch	5000 405Ch	5004 405Ch
68h	16	EPWM_GLDCTL	500C 3068h	5000 4068h	5004 4068h
6Ah	16	EPWM_GLDCFG	500C 306Ah	5000 406Ah	5004 406Ah
70h	32	EPWM_EPWMXLINK	500C 3070h	5000 4070h	5004 4070h
74h	32	EPWM_EPWMXLINK2	500C 3074h	5000 4074h	5004 4074h
7Ah	16	EPWM_ETEST	500C 307Ah	5000 407Ah	5004 407Ah
7Ch	16	EPWM_EPWMREV	500C 307Ch	5000 407Ch	5004 407Ch
7Eh	16	EPWM_HRPWMREV	500C 307Eh	5000 407Eh	5004 407Eh
80h	16	EPWM_AQCTLA	500C 3080h	5000 4080h	5004 4080h
82h	16	EPWM_AQCTLA2	500C 3082h	5000 4082h	5004 4082h
84h	16	EPWM_AQCTLB	500C 3084h	5000 4084h	5004 4084h
86h	16	EPWM_AQCTLB2	500C 3086h	5000 4086h	5004 4086h
8Eh	16	EPWM_AQSFRC	500C 308Eh	5000 408Eh	5004 408Eh
92h	16	EPWM_AQCSFRC	500C 3092h	5000 4092h	5004 4092h
A0h	16	EPWM_DBREDHR	500C 30A0h	5000 40A0h	5004 40A0h
A2h	16	EPWM_DBRED	500C 30A2h	5000 40A2h	5004 40A2h
A4h	16	EPWM_DBFEDHR	500C 30A4h	5000 40A4h	5004 40A4h
A6h	16	EPWM_DBFED	500C 30A6h	5000 40A6h	5004 40A6h
C0h	32	EPWM_TBPHS	500C 30C0h	5000 40C0h	5004 40C0h
C4h	16	EPWM_TBPRDHR	500C 30C4h	5000 40C4h	5004 40C4h
C6h	16	EPWM_TBPRD	500C 30C6h	5000 40C6h	5004 40C6h

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Table 3-575. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM15_G0 Physical Address	EPWM16_G0 Physical Address	EPWM17_G0 Physical Address
C8h	16	EPWM_TBPRDHRB	500C 30C8h	5000 40C8h	5004 40C8h
D4h	32	EPWM_CMPA	500C 30D4h	5000 40D4h	5004 40D4h
D8h	32	EPWM_CMPB	500C 30D8h	5000 40D8h	5004 40D8h
DEh	16	EPWM_CMPC	500C 30DEh	5000 40DEh	5004 40DEh
E2h	16	EPWM_CMPD	500C 30E2h	5000 40E2h	5004 40E2h
E8h	16	EPWM_GLDCTL2	500C 30E8h	5000 40E8h	5004 40E8h
EEh	16	EPWM_SWVDELVAL	500C 30EEh	5000 40EEh	5004 40EEh
100h	16	EPWM_TZSEL	500C 3100h	5000 4100h	5004 4100h
102h	16	EPWM_TZSEL2	500C 3102h	5000 4102h	5004 4102h
104h	16	EPWM_TZDCSEL	500C 3104h	5000 4104h	5004 4104h
108h	16	EPWM_TZCTL	500C 3108h	5000 4108h	5004 4108h
10Ah	16	EPWM_TZCTL2	500C 310Ah	5000 410Ah	5004 410Ah
10Ch	16	EPWM_TZCTLDCA	500C 310Ch	5000 410Ch	5004 410Ch
10Eh	16	EPWM_TZCTLDCB	500C 310Eh	5000 410Eh	5004 410Eh
11Ah	16	EPWM_TZEINT	500C 311Ah	5000 411Ah	5004 411Ah
126h	16	EPWM_TZFLG	500C 3126h	5000 4126h	5004 4126h
128h	16	EPWM_TZCBCFLG	500C 3128h	5000 4128h	5004 4128h
12Ah	16	EPWM_TZOSTFLG	500C 312Ah	5000 412Ah	5004 412Ah
12Eh	16	EPWM_TZCLR	500C 312Eh	5000 412Eh	5004 412Eh
130h	16	EPWM_TZCBCCLR	500C 3130h	5000 4130h	5004 4130h
132h	16	EPWM_TZOSTCLR	500C 3132h	5000 4132h	5004 4132h
136h	16	EPWM_TZFRC	500C 3136h	5000 4136h	5004 4136h
13Ah	16	EPWM_TZTRIPOUTSEL	500C 313Ah	5000 413Ah	5004 413Ah
148h	16	EPWM_ETSEL	500C 3148h	5000 4148h	5004 4148h
14Ch	16	EPWM_ETPS	500C 314Ch	5000 414Ch	5004 414Ch
150h	16	EPWM_ETFLG	500C 3150h	5000 4150h	5004 4150h
154h	16	EPWM_ETCLR	500C 3154h	5000 4154h	5004 4154h
158h	16	EPWM_ETFRC	500C 3158h	5000 4158h	5004 4158h
15Ch	16	EPWM_ETINTPS	500C 315Ch	5000 415Ch	5004 415Ch
160h	16	EPWM_ETSOCPS	500C 3160h	5000 4160h	5004 4160h
164h	16	EPWM_ETCNTINITCTL	500C 3164h	5000 4164h	5004 4164h
168h	16	EPWM_ETCNTINIT	500C 3168h	5000 4168h	5004 4168h
16Ch	16	EPWM_ETINTMIXEN	500C 316Ch	5000 416Ch	5004 416Ch
170h	16	EPWM_ETSOCAMIXEN	500C 3170h	5000 4170h	5004 4170h
174h	16	EPWM_ETSOCBMIXEN	500C 3174h	5000 4174h	5004 4174h
180h	16	EPWM_DCTRIPSEL	500C 3180h	5000 4180h	5004 4180h
186h	16	EPWM_DCACTL	500C 3186h	5000 4186h	5004 4186h
188h	16	EPWM_DCBCTL	500C 3188h	5000 4188h	5004 4188h
18Eh	16	EPWM_DCFCTL	500C 318Eh	5000 418Eh	5004 418Eh
190h	16	EPWM_DCCAPCTL	500C 3190h	5000 4190h	5004 4190h
192h	16	EPWM_DCFOFFSET	500C 3192h	5000 4192h	5004 4192h
194h	16	EPWM_DCFOFFSETCNT	500C 3194h	5000 4194h	5004 4194h
196h	16	EPWM_DCFWINDOW	500C 3196h	5000 4196h	5004 4196h
198h	16	EPWM_DCFWINDOWCNT	500C 3198h	5000 4198h	5004 4198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500C 319Ah	5000 419Ah	5004 419Ah
19Ch	16	EPWM_DCCAPMIXSEL	500C 319Ch	5000 419Ch	5004 419Ch

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Table 3-575. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM15_G0 Physical Address	EPWM16_G0 Physical Address	EPWM17_G0 Physical Address
19Eh	16	EPWM_DCCAP	500C 319Eh	5000 419Eh	5004 419Eh
1A4h	16	EPWM_DCAHTRIPSEL	500C 31A4h	5000 41A4h	5004 41A4h
1A6h	16	EPWM_DCALTRIPSEL	500C 31A6h	5000 41A6h	5004 41A6h
1A8h	16	EPWM_DCBHTRIPSEL	500C 31A8h	5000 41A8h	5004 41A8h
1AAh	16	EPWM_DCBLTRIPSEL	500C 31AAh	5000 41AAh	5004 41AAh
1ACh	16	EPWM_CAPCTL	500C 31ACh	5000 41ACh	5004 41ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500C 31AEh	5000 41AEh	5004 41AEh
1B0h	16	EPWM_CAPINTRIPSEL	500C 31B0h	5000 41B0h	5004 41B0h
1B2h	16	EPWM_CAPTRIPSEL	500C 31B2h	5000 41B2h	5004 41B2h
1F4h	32	EPWM_EPWMLOCK	500C 31F4h	5000 41F4h	5004 41F4h
1FAh	16	EPWM_HWVDELVAL	500C 31FAh	5000 41FAh	5004 41FAh
1FCh	16	EPWM_VCNTVAL	500C 31FCh	5000 41FCh	5004 41FCh
400h	32	EPWM_XCMPCTL1	500C 3400h	5000 4400h	5004 4400h
410h	32	EPWM_XLOADCTL	500C 3410h	5000 4410h	5004 4410h
418h	32	EPWM_XLOAD	500C 3418h	5000 4418h	5004 4418h
41Ch	32	EPWM_EPWMXLINKXLOAD	500C 341Ch	5000 441Ch	5004 441Ch
420h	32	EPWM_XREGSHDW1STS	500C 3420h	5000 4420h	5004 4420h
428h	32	EPWM_XREGSHDW2STS	500C 3428h	5000 4428h	5004 4428h
430h	32	EPWM_XREGSHDW3STS	500C 3430h	5000 4430h	5004 4430h
600h	32	EPWM_XCMP1_ACTIVE	500C 3600h	5000 4600h	5004 4600h
604h	32	EPWM_XCMP2_ACTIVE	500C 3604h	5000 4604h	5004 4604h
608h	32	EPWM_XCMP3_ACTIVE	500C 3608h	5000 4608h	5004 4608h
60Ch	32	EPWM_XCMP4_ACTIVE	500C 360Ch	5000 460Ch	5004 460Ch
610h	32	EPWM_XCMP5_ACTIVE	500C 3610h	5000 4610h	5004 4610h
614h	32	EPWM_XCMP6_ACTIVE	500C 3614h	5000 4614h	5004 4614h
618h	32	EPWM_XCMP7_ACTIVE	500C 3618h	5000 4618h	5004 4618h
61Ch	32	EPWM_XCMP8_ACTIVE	500C 361Ch	5000 461Ch	5004 461Ch
620h	32	EPWM_XTBPRD_ACTIVE	500C 3620h	5000 4620h	5004 4620h
630h	16	EPWM_XAQCTLA_ACTIVE	500C 3630h	5000 4630h	5004 4630h
644h	32	EPWM_XMINMAX_ACTIVE	500C 3644h	5000 4644h	5004 4644h
680h	32	EPWM_XCMP1_SHDW1	500C 3680h	5000 4680h	5004 4680h
684h	32	EPWM_XCMP2_SHDW1	500C 3684h	5000 4684h	5004 4684h
688h	32	EPWM_XCMP3_SHDW1	500C 3688h	5000 4688h	5004 4688h
68Ch	32	EPWM_XCMP4_SHDW1	500C 368Ch	5000 468Ch	5004 468Ch
690h	32	EPWM_XCMP5_SHDW1	500C 3690h	5000 4690h	5004 4690h
694h	32	EPWM_XCMP6_SHDW1	500C 3694h	5000 4694h	5004 4694h
698h	32	EPWM_XCMP7_SHDW1	500C 3698h	5000 4698h	5004 4698h
69Ch	32	EPWM_XCMP8_SHDW1	500C 369Ch	5000 469Ch	5004 469Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500C 36A0h	5000 46A0h	5004 46A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500C 36B0h	5000 46B0h	5004 46B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500C 36B2h	5000 46B2h	5004 46B2h
6BAh	16	EPWM_CMPC_SHDW1	500C 36BAh	5000 46BAh	5004 46BAh
6BEh	16	EPWM_CMPD_SHDW1	500C 36BEh	5000 46BEh	5004 46BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500C 36C4h	5000 46C4h	5004 46C4h
700h	32	EPWM_XCMP1_SHDW2	500C 3700h	5000 4700h	5004 4700h
704h	32	EPWM_XCMP2_SHDW2	500C 3704h	5000 4704h	5004 4704h

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Table 3-575. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM15_G0 Physical Address	EPWM16_G0 Physical Address	EPWM17_G0 Physical Address
708h	32	EPWM_XCMP3_SHDW2	500C 3708h	5000 4708h	5004 4708h
70Ch	32	EPWM_XCMP4_SHDW2	500C 370Ch	5000 470Ch	5004 470Ch
710h	32	EPWM_XCMP5_SHDW2	500C 3710h	5000 4710h	5004 4710h
714h	32	EPWM_XCMP6_SHDW2	500C 3714h	5000 4714h	5004 4714h
718h	32	EPWM_XCMP7_SHDW2	500C 3718h	5000 4718h	5004 4718h
71Ch	32	EPWM_XCMP8_SHDW2	500C 371Ch	5000 471Ch	5004 471Ch
720h	32	EPWM_XTBPRD_SHDW2	500C 3720h	5000 4720h	5004 4720h
730h	16	EPWM_XAQCTLA_SHDW2	500C 3730h	5000 4730h	5004 4730h
732h	16	EPWM_XAQCTLB_SHDW2	500C 3732h	5000 4732h	5004 4732h
73Ah	16	EPWM_CMPC_SHDW2	500C 373Ah	5000 473Ah	5004 473Ah
73Eh	16	EPWM_CMPD_SHDW2	500C 373Eh	5000 473Eh	5004 473Eh
744h	32	EPWM_XMINMAX_SHDW2	500C 3744h	5000 4744h	5004 4744h
780h	32	EPWM_XCMP1_SHDW3	500C 3780h	5000 4780h	5004 4780h
784h	32	EPWM_XCMP2_SHDW3	500C 3784h	5000 4784h	5004 4784h
788h	32	EPWM_XCMP3_SHDW3	500C 3788h	5000 4788h	5004 4788h
78Ch	32	EPWM_XCMP4_SHDW3	500C 378Ch	5000 478Ch	5004 478Ch
790h	32	EPWM_XCMP5_SHDW3	500C 3790h	5000 4790h	5004 4790h
794h	32	EPWM_XCMP6_SHDW3	500C 3794h	5000 4794h	5004 4794h
798h	32	EPWM_XCMP7_SHDW3	500C 3798h	5000 4798h	5004 4798h
79Ch	32	EPWM_XCMP8_SHDW3	500C 379Ch	5000 479Ch	5004 479Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500C 37A0h	5000 47A0h	5004 47A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500C 37B0h	5000 47B0h	5004 47B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500C 37B2h	5000 47B2h	5004 47B2h
7BAh	16	EPWM_CMPC_SHDW3	500C 37BAh	5000 47BAh	5004 47BAh
7BEh	16	EPWM_CMPD_SHDW3	500C 37BEh	5000 47BEh	5004 47BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500C 37C4h	5000 47C4h	5004 47C4h
800h	32	EPWM_DECTL	500C 3800h	5000 4800h	5004 4800h
804h	32	EPWM_DECOMPSEL	500C 3804h	5000 4804h	5004 4804h
808h	32	EPWM_DEACTCTL	500C 3808h	5000 4808h	5004 4808h
80Ch	32	EPWM_DESTS	500C 380Ch	5000 480Ch	5004 480Ch
810h	32	EPWM_DEFRC	500C 3810h	5000 4810h	5004 4810h
814h	32	EPWM_DECLR	500C 3814h	5000 4814h	5004 4814h
820h	32	EPWM_DEMONCNT	500C 3820h	5000 4820h	5004 4820h
824h	32	EPWM_DEMONCTL	500C 3824h	5000 4824h	5004 4824h
828h	32	EPWM_DEMONSTEP	500C 3828h	5000 4828h	5004 4828h
82Ch	32	EPWM_DEMONTHRES	500C 382Ch	5000 482Ch	5004 482Ch
C00h	32	EPWM_MINDBCFG	500C 3C00h	5000 4C00h	5004 4C00h
C04h	32	EPWM_MINDBDLY	500C 3C04h	5000 4C04h	5004 4C04h
C20h	32	EPWM_LUTCTLA	500C 3C20h	5000 4C20h	5004 4C20h
C24h	32	EPWM_LUTCTLB	500C 3C24h	5000 4C24h	5004 4C24h

Table 3-576. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM18_G0 Physical Address	EPWM19_G0 Physical Address	EPWM20_G0 Physical Address
0h	16	EPWM_TBCTL	5008 4000h	500C 4000h	5000 5000h
2h	16	EPWM_TBCTL2	5008 4002h	500C 4002h	5000 5002h

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Table 3-576. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM18_G0 Physical Address	EPWM19_G0 Physical Address	EPWM20_G0 Physical Address
6h	16	EPWM_EPWMSYNCINSEL	5008 4006h	500C 4006h	5000 5006h
8h	16	EPWM_TBCTR	5008 4008h	500C 4008h	5000 5008h
Ah	16	EPWM_TBSTS	5008 400Ah	500C 400Ah	5000 500Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5008 400Ch	500C 400Ch	5000 500Ch
Eh	16	EPWM_TBCTL3	5008 400Eh	500C 400Eh	5000 500Eh
10h	16	EPWM_CMPCTL	5008 4010h	500C 4010h	5000 5010h
12h	16	EPWM_CMPCTL2	5008 4012h	500C 4012h	5000 5012h
18h	16	EPWM_DBCTL	5008 4018h	500C 4018h	5000 5018h
1Ah	16	EPWM_DBCTL2	5008 401Ah	500C 401Ah	5000 501Ah
20h	16	EPWM_AQCTL	5008 4020h	500C 4020h	5000 5020h
22h	16	EPWM_AQTSRCSEL	5008 4022h	500C 4022h	5000 5022h
28h	16	EPWM_PCCTL	5008 4028h	500C 4028h	5000 5028h
30h	16	EPWM_VCAPCTL	5008 4030h	500C 4030h	5000 5030h
32h	16	EPWM_VCNTCFG	5008 4032h	500C 4032h	5000 5032h
40h	16	EPWM_HRCNFG	5008 4040h	500C 4040h	5000 5040h
4Eh	16	EPWM_HRCNFG2	5008 404Eh	500C 404Eh	5000 504Eh
5Ah	16	EPWM_HRPCTL	5008 405Ah	500C 405Ah	5000 505Ah
5Ch	16	EPWM_TRREM	5008 405Ch	500C 405Ch	5000 505Ch
68h	16	EPWM_GLDCTL	5008 4068h	500C 4068h	5000 5068h
6Ah	16	EPWM_GLDCFG	5008 406Ah	500C 406Ah	5000 506Ah
70h	32	EPWM_EPWMXLINK	5008 4070h	500C 4070h	5000 5070h
74h	32	EPWM_EPWMXLINK2	5008 4074h	500C 4074h	5000 5074h
7Ah	16	EPWM_ETEST	5008 407Ah	500C 407Ah	5000 507Ah
7Ch	16	EPWM_EPWMREV	5008 407Ch	500C 407Ch	5000 507Ch
7Eh	16	EPWM_HRPWMREV	5008 407Eh	500C 407Eh	5000 507Eh
80h	16	EPWM_AQCTLA	5008 4080h	500C 4080h	5000 5080h
82h	16	EPWM_AQCTLA2	5008 4082h	500C 4082h	5000 5082h
84h	16	EPWM_AQCTLB	5008 4084h	500C 4084h	5000 5084h
86h	16	EPWM_AQCTLB2	5008 4086h	500C 4086h	5000 5086h
8Eh	16	EPWM_AQSFRC	5008 408Eh	500C 408Eh	5000 508Eh
92h	16	EPWM_AQCSFRC	5008 4092h	500C 4092h	5000 5092h
A0h	16	EPWM_DBREDHR	5008 40A0h	500C 40A0h	5000 50A0h
A2h	16	EPWM_DBRED	5008 40A2h	500C 40A2h	5000 50A2h
A4h	16	EPWM_DBFEDHR	5008 40A4h	500C 40A4h	5000 50A4h
A6h	16	EPWM_DBFED	5008 40A6h	500C 40A6h	5000 50A6h
C0h	32	EPWM_TBPHS	5008 40C0h	500C 40C0h	5000 50C0h
C4h	16	EPWM_TBPRDHR	5008 40C4h	500C 40C4h	5000 50C4h
C6h	16	EPWM_TBPRD	5008 40C6h	500C 40C6h	5000 50C6h
C8h	16	EPWM_TBPRDHRB	5008 40C8h	500C 40C8h	5000 50C8h
D4h	32	EPWM_CMPA	5008 40D4h	500C 40D4h	5000 50D4h
D8h	32	EPWM_CMPB	5008 40D8h	500C 40D8h	5000 50D8h
DEh	16	EPWM_CMPC	5008 40DEh	500C 40DEh	5000 50DEh
E2h	16	EPWM_CMPD	5008 40E2h	500C 40E2h	5000 50E2h
E8h	16	EPWM_GLDCTL2	5008 40E8h	500C 40E8h	5000 50E8h
EEh	16	EPWM_SWVDELVAL	5008 40EEh	500C 40EEh	5000 50EEh
100h	16	EPWM_TZSEL	5008 4100h	500C 4100h	5000 5100h

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Table 3-576. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM18_G0 Physical Address	EPWM19_G0 Physical Address	EPWM20_G0 Physical Address
102h	16	EPWM_TZSEL2	5008 4102h	500C 4102h	5000 5102h
104h	16	EPWM_TZDCSEL	5008 4104h	500C 4104h	5000 5104h
108h	16	EPWM_TZCTL	5008 4108h	500C 4108h	5000 5108h
10Ah	16	EPWM_TZCTL2	5008 410Ah	500C 410Ah	5000 510Ah
10Ch	16	EPWM_TZCTLDCA	5008 410Ch	500C 410Ch	5000 510Ch
10Eh	16	EPWM_TZCTLDCB	5008 410Eh	500C 410Eh	5000 510Eh
11Ah	16	EPWM_TZEINT	5008 411Ah	500C 411Ah	5000 511Ah
126h	16	EPWM_TZFLG	5008 4126h	500C 4126h	5000 5126h
128h	16	EPWM_TZCBCFLG	5008 4128h	500C 4128h	5000 5128h
12Ah	16	EPWM_TZOSTFLG	5008 412Ah	500C 412Ah	5000 512Ah
12Eh	16	EPWM_TZCLR	5008 412Eh	500C 412Eh	5000 512Eh
130h	16	EPWM_TZCBCCLR	5008 4130h	500C 4130h	5000 5130h
132h	16	EPWM_TZOSTCLR	5008 4132h	500C 4132h	5000 5132h
136h	16	EPWM_TZFRC	5008 4136h	500C 4136h	5000 5136h
13Ah	16	EPWM_TZTRIPOUTSEL	5008 413Ah	500C 413Ah	5000 513Ah
148h	16	EPWM_ETSEL	5008 4148h	500C 4148h	5000 5148h
14Ch	16	EPWM_ETPS	5008 414Ch	500C 414Ch	5000 514Ch
150h	16	EPWM_ETFLG	5008 4150h	500C 4150h	5000 5150h
154h	16	EPWM_ETCLR	5008 4154h	500C 4154h	5000 5154h
158h	16	EPWM_ETFRC	5008 4158h	500C 4158h	5000 5158h
15Ch	16	EPWM_ETINTPS	5008 415Ch	500C 415Ch	5000 515Ch
160h	16	EPWM_ETSOCPS	5008 4160h	500C 4160h	5000 5160h
164h	16	EPWM_ETCNTINITCTL	5008 4164h	500C 4164h	5000 5164h
168h	16	EPWM_ETCNTINIT	5008 4168h	500C 4168h	5000 5168h
16Ch	16	EPWM_ETINTMIXEN	5008 416Ch	500C 416Ch	5000 516Ch
170h	16	EPWM_ETSOCAMIXEN	5008 4170h	500C 4170h	5000 5170h
174h	16	EPWM_ETSOCBMIXEN	5008 4174h	500C 4174h	5000 5174h
180h	16	EPWM_DCTRIPSEL	5008 4180h	500C 4180h	5000 5180h
186h	16	EPWM_DCACTL	5008 4186h	500C 4186h	5000 5186h
188h	16	EPWM_DCBCTL	5008 4188h	500C 4188h	5000 5188h
18Eh	16	EPWM_DCFCTL	5008 418Eh	500C 418Eh	5000 518Eh
190h	16	EPWM_DCCAPCTL	5008 4190h	500C 4190h	5000 5190h
192h	16	EPWM_DCFOFFSET	5008 4192h	500C 4192h	5000 5192h
194h	16	EPWM_DCFOFFSETCNT	5008 4194h	500C 4194h	5000 5194h
196h	16	EPWM_DCFWINDOW	5008 4196h	500C 4196h	5000 5196h
198h	16	EPWM_DCFWINDOWCNT	5008 4198h	500C 4198h	5000 5198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5008 419Ah	500C 419Ah	5000 519Ah
19Ch	16	EPWM_DCCAPMIXSEL	5008 419Ch	500C 419Ch	5000 519Ch
19Eh	16	EPWM_DCCAP	5008 419Eh	500C 419Eh	5000 519Eh
1A4h	16	EPWM_DCAHTRIPSEL	5008 41A4h	500C 41A4h	5000 51A4h
1A6h	16	EPWM_DCALTRIPSEL	5008 41A6h	500C 41A6h	5000 51A6h
1A8h	16	EPWM_DCBHTRIPSEL	5008 41A8h	500C 41A8h	5000 51A8h
1AAh	16	EPWM_DCBLTRIPSEL	5008 41AAh	500C 41AAh	5000 51AAh
1ACh	16	EPWM_CAPCTL	5008 41ACh	500C 41ACh	5000 51ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5008 41AEh	500C 41AEh	5000 51AEh
1B0h	16	EPWM_CAPINTRIPSEL	5008 41B0h	500C 41B0h	5000 51B0h

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Table 3-576. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM18_G0 Physical Address	EPWM19_G0 Physical Address	EPWM20_G0 Physical Address
1B2h	16	EPWM_CAPTRIPSEL	5008 41B2h	500C 41B2h	5000 51B2h
1F4h	32	EPWM_EPWMLOCK	5008 41F4h	500C 41F4h	5000 51F4h
1FAh	16	EPWM_HWVDELVAL	5008 41FAh	500C 41FAh	5000 51FAh
1FCh	16	EPWM_VCNTVAL	5008 41FCh	500C 41FCh	5000 51FCh
400h	32	EPWM_XCMPCTL1	5008 4400h	500C 4400h	5000 5400h
410h	32	EPWM_XLOADCTL	5008 4410h	500C 4410h	5000 5410h
418h	32	EPWM_XLOAD	5008 4418h	500C 4418h	5000 5418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5008 441Ch	500C 441Ch	5000 541Ch
420h	32	EPWM_XREGSHDW1STS	5008 4420h	500C 4420h	5000 5420h
428h	32	EPWM_XREGSHDW2STS	5008 4428h	500C 4428h	5000 5428h
430h	32	EPWM_XREGSHDW3STS	5008 4430h	500C 4430h	5000 5430h
600h	32	EPWM_XCMP1_ACTIVE	5008 4600h	500C 4600h	5000 5600h
604h	32	EPWM_XCMP2_ACTIVE	5008 4604h	500C 4604h	5000 5604h
608h	32	EPWM_XCMP3_ACTIVE	5008 4608h	500C 4608h	5000 5608h
60Ch	32	EPWM_XCMP4_ACTIVE	5008 460Ch	500C 460Ch	5000 560Ch
610h	32	EPWM_XCMP5_ACTIVE	5008 4610h	500C 4610h	5000 5610h
614h	32	EPWM_XCMP6_ACTIVE	5008 4614h	500C 4614h	5000 5614h
618h	32	EPWM_XCMP7_ACTIVE	5008 4618h	500C 4618h	5000 5618h
61Ch	32	EPWM_XCMP8_ACTIVE	5008 461Ch	500C 461Ch	5000 561Ch
620h	32	EPWM_XTBPRD_ACTIVE	5008 4620h	500C 4620h	5000 5620h
630h	16	EPWM_XAQCTLA_ACTIVE	5008 4630h	500C 4630h	5000 5630h
644h	32	EPWM_XMINMAX_ACTIVE	5008 4644h	500C 4644h	5000 5644h
680h	32	EPWM_XCMP1_SHDW1	5008 4680h	500C 4680h	5000 5680h
684h	32	EPWM_XCMP2_SHDW1	5008 4684h	500C 4684h	5000 5684h
688h	32	EPWM_XCMP3_SHDW1	5008 4688h	500C 4688h	5000 5688h
68Ch	32	EPWM_XCMP4_SHDW1	5008 468Ch	500C 468Ch	5000 568Ch
690h	32	EPWM_XCMP5_SHDW1	5008 4690h	500C 4690h	5000 5690h
694h	32	EPWM_XCMP6_SHDW1	5008 4694h	500C 4694h	5000 5694h
698h	32	EPWM_XCMP7_SHDW1	5008 4698h	500C 4698h	5000 5698h
69Ch	32	EPWM_XCMP8_SHDW1	5008 469Ch	500C 469Ch	5000 569Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5008 46A0h	500C 46A0h	5000 56A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5008 46B0h	500C 46B0h	5000 56B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5008 46B2h	500C 46B2h	5000 56B2h
6BAh	16	EPWM_CMPC_SHDW1	5008 46BAh	500C 46BAh	5000 56BAh
6BEh	16	EPWM_CMPD_SHDW1	5008 46BEh	500C 46BEh	5000 56BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5008 46C4h	500C 46C4h	5000 56C4h
700h	32	EPWM_XCMP1_SHDW2	5008 4700h	500C 4700h	5000 5700h
704h	32	EPWM_XCMP2_SHDW2	5008 4704h	500C 4704h	5000 5704h
708h	32	EPWM_XCMP3_SHDW2	5008 4708h	500C 4708h	5000 5708h
70Ch	32	EPWM_XCMP4_SHDW2	5008 470Ch	500C 470Ch	5000 570Ch
710h	32	EPWM_XCMP5_SHDW2	5008 4710h	500C 4710h	5000 5710h
714h	32	EPWM_XCMP6_SHDW2	5008 4714h	500C 4714h	5000 5714h
718h	32	EPWM_XCMP7_SHDW2	5008 4718h	500C 4718h	5000 5718h
71Ch	32	EPWM_XCMP8_SHDW2	5008 471Ch	500C 471Ch	5000 571Ch
720h	32	EPWM_XTBPRD_SHDW2	5008 4720h	500C 4720h	5000 5720h
730h	16	EPWM_XAQCTLA_SHDW2	5008 4730h	500C 4730h	5000 5730h

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Table 3-576. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM18_G0 Physical Address	EPWM19_G0 Physical Address	EPWM20_G0 Physical Address
732h	16	EPWM_XAQCTLB_SHDW2	5008 4732h	500C 4732h	5000 5732h
73Ah	16	EPWM_CMPC_SHDW2	5008 473Ah	500C 473Ah	5000 573Ah
73Eh	16	EPWM_CMPD_SHDW2	5008 473Eh	500C 473Eh	5000 573Eh
744h	32	EPWM_XMINMAX_SHDW2	5008 4744h	500C 4744h	5000 5744h
780h	32	EPWM_XCMP1_SHDW3	5008 4780h	500C 4780h	5000 5780h
784h	32	EPWM_XCMP2_SHDW3	5008 4784h	500C 4784h	5000 5784h
788h	32	EPWM_XCMP3_SHDW3	5008 4788h	500C 4788h	5000 5788h
78Ch	32	EPWM_XCMP4_SHDW3	5008 478Ch	500C 478Ch	5000 578Ch
790h	32	EPWM_XCMP5_SHDW3	5008 4790h	500C 4790h	5000 5790h
794h	32	EPWM_XCMP6_SHDW3	5008 4794h	500C 4794h	5000 5794h
798h	32	EPWM_XCMP7_SHDW3	5008 4798h	500C 4798h	5000 5798h
79Ch	32	EPWM_XCMP8_SHDW3	5008 479Ch	500C 479Ch	5000 579Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5008 47A0h	500C 47A0h	5000 57A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5008 47B0h	500C 47B0h	5000 57B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5008 47B2h	500C 47B2h	5000 57B2h
7BAh	16	EPWM_CMPC_SHDW3	5008 47BAh	500C 47BAh	5000 57BAh
7BEh	16	EPWM_CMPD_SHDW3	5008 47BEh	500C 47BEh	5000 57BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5008 47C4h	500C 47C4h	5000 57C4h
800h	32	EPWM_DECTL	5008 4800h	500C 4800h	5000 5800h
804h	32	EPWM_DECOMPSEL	5008 4804h	500C 4804h	5000 5804h
808h	32	EPWM_DEACTCTL	5008 4808h	500C 4808h	5000 5808h
80Ch	32	EPWM_DESTS	5008 480Ch	500C 480Ch	5000 580Ch
810h	32	EPWM_DEFRC	5008 4810h	500C 4810h	5000 5810h
814h	32	EPWM_DECLR	5008 4814h	500C 4814h	5000 5814h
820h	32	EPWM_DEMONCNT	5008 4820h	500C 4820h	5000 5820h
824h	32	EPWM_DEMONCTL	5008 4824h	500C 4824h	5000 5824h
828h	32	EPWM_DEMONSTEP	5008 4828h	500C 4828h	5000 5828h
82Ch	32	EPWM_DEMONTHRES	5008 482Ch	500C 482Ch	5000 582Ch
C00h	32	EPWM_MINDBCFG	5008 4C00h	500C 4C00h	5000 5C00h
C04h	32	EPWM_MINDBDLY	5008 4C04h	500C 4C04h	5000 5C04h
C20h	32	EPWM_LUTCTLA	5008 4C20h	500C 4C20h	5000 5C20h
C24h	32	EPWM_LUTCTLB	5008 4C24h	500C 4C24h	5000 5C24h

Table 3-577. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM21_G0 Physical Address	EPWM22_G0 Physical Address	EPWM23_G0 Physical Address
0h	16	EPWM_TBCTL	5004 5000h	5008 5000h	500C 5000h
2h	16	EPWM_TBCTL2	5004 5002h	5008 5002h	500C 5002h
6h	16	EPWM_EPWMSYNCINSEL	5004 5006h	5008 5006h	500C 5006h
8h	16	EPWM_TBCTR	5004 5008h	5008 5008h	500C 5008h
Ah	16	EPWM_TBSTS	5004 500Ah	5008 500Ah	500C 500Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5004 500Ch	5008 500Ch	500C 500Ch
Eh	16	EPWM_TBCTL3	5004 500Eh	5008 500Eh	500C 500Eh
10h	16	EPWM_CMPCTL	5004 5010h	5008 5010h	500C 5010h
12h	16	EPWM_CMPCTL2	5004 5012h	5008 5012h	500C 5012h
18h	16	EPWM_DBCTL	5004 5018h	5008 5018h	500C 5018h

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Table 3-577. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM21_G0 Physical Address	EPWM22_G0 Physical Address	EPWM23_G0 Physical Address
1Ah	16	EPWM_DBCTL2	5004 501Ah	5008 501Ah	500C 501Ah
20h	16	EPWM_AQCTL	5004 5020h	5008 5020h	500C 5020h
22h	16	EPWM_AQTSRCSEL	5004 5022h	5008 5022h	500C 5022h
28h	16	EPWM_PCCTL	5004 5028h	5008 5028h	500C 5028h
30h	16	EPWM_VCAPCTL	5004 5030h	5008 5030h	500C 5030h
32h	16	EPWM_VCNTCFG	5004 5032h	5008 5032h	500C 5032h
40h	16	EPWM_HRCNFG	5004 5040h	5008 5040h	500C 5040h
4Eh	16	EPWM_HRCNFG2	5004 504Eh	5008 504Eh	500C 504Eh
5Ah	16	EPWM_HRPCTL	5004 505Ah	5008 505Ah	500C 505Ah
5Ch	16	EPWM_TRREM	5004 505Ch	5008 505Ch	500C 505Ch
68h	16	EPWM_GLDCTL	5004 5068h	5008 5068h	500C 5068h
6Ah	16	EPWM_GLDCFG	5004 506Ah	5008 506Ah	500C 506Ah
70h	32	EPWM_EPWMXLINK	5004 5070h	5008 5070h	500C 5070h
74h	32	EPWM_EPWMXLINK2	5004 5074h	5008 5074h	500C 5074h
7Ah	16	EPWM_ETEST	5004 507Ah	5008 507Ah	500C 507Ah
7Ch	16	EPWM_EPWMREV	5004 507Ch	5008 507Ch	500C 507Ch
7Eh	16	EPWM_HRPWMREV	5004 507Eh	5008 507Eh	500C 507Eh
80h	16	EPWM_AQCTLA	5004 5080h	5008 5080h	500C 5080h
82h	16	EPWM_AQCTLA2	5004 5082h	5008 5082h	500C 5082h
84h	16	EPWM_AQCTLB	5004 5084h	5008 5084h	500C 5084h
86h	16	EPWM_AQCTLB2	5004 5086h	5008 5086h	500C 5086h
8Eh	16	EPWM_AQSFRC	5004 508Eh	5008 508Eh	500C 508Eh
92h	16	EPWM_AQCSFRC	5004 5092h	5008 5092h	500C 5092h
A0h	16	EPWM_DBREDHR	5004 50A0h	5008 50A0h	500C 50A0h
A2h	16	EPWM_DBRED	5004 50A2h	5008 50A2h	500C 50A2h
A4h	16	EPWM_DBFEDHR	5004 50A4h	5008 50A4h	500C 50A4h
A6h	16	EPWM_DBFED	5004 50A6h	5008 50A6h	500C 50A6h
C0h	32	EPWM_TBPHS	5004 50C0h	5008 50C0h	500C 50C0h
C4h	16	EPWM_TBPRDHR	5004 50C4h	5008 50C4h	500C 50C4h
C6h	16	EPWM_TBPRD	5004 50C6h	5008 50C6h	500C 50C6h
C8h	16	EPWM_TBPRDHRB	5004 50C8h	5008 50C8h	500C 50C8h
D4h	32	EPWM_CMPA	5004 50D4h	5008 50D4h	500C 50D4h
D8h	32	EPWM_CMPB	5004 50D8h	5008 50D8h	500C 50D8h
DEh	16	EPWM_CMPC	5004 50DEh	5008 50DEh	500C 50DEh
E2h	16	EPWM_CMPD	5004 50E2h	5008 50E2h	500C 50E2h
E8h	16	EPWM_GLDCTL2	5004 50E8h	5008 50E8h	500C 50E8h
EEh	16	EPWM_SWVDELVAL	5004 50EEh	5008 50EEh	500C 50EEh
100h	16	EPWM_TZSEL	5004 5100h	5008 5100h	500C 5100h
102h	16	EPWM_TZSEL2	5004 5102h	5008 5102h	500C 5102h
104h	16	EPWM_TZDCSEL	5004 5104h	5008 5104h	500C 5104h
108h	16	EPWM_TZCTL	5004 5108h	5008 5108h	500C 5108h
10Ah	16	EPWM_TZCTL2	5004 510Ah	5008 510Ah	500C 510Ah
10Ch	16	EPWM_TZCTLDCA	5004 510Ch	5008 510Ch	500C 510Ch
10Eh	16	EPWM_TZCTLDCB	5004 510Eh	5008 510Eh	500C 510Eh
11Ah	16	EPWM_TZEINT	5004 511Ah	5008 511Ah	500C 511Ah
126h	16	EPWM_TZFLG	5004 5126h	5008 5126h	500C 5126h

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Table 3-577. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM21_G0 Physical Address	EPWM22_G0 Physical Address	EPWM23_G0 Physical Address
128h	16	EPWM_TZCBCFLG	5004 5128h	5008 5128h	500C 5128h
12Ah	16	EPWM_TZOSTFLG	5004 512Ah	5008 512Ah	500C 512Ah
12Eh	16	EPWM_TZCLR	5004 512Eh	5008 512Eh	500C 512Eh
130h	16	EPWM_TZCBCCLR	5004 5130h	5008 5130h	500C 5130h
132h	16	EPWM_TZOSTCLR	5004 5132h	5008 5132h	500C 5132h
136h	16	EPWM_TZFRC	5004 5136h	5008 5136h	500C 5136h
13Ah	16	EPWM_TZTRIPOUTSEL	5004 513Ah	5008 513Ah	500C 513Ah
148h	16	EPWM_ETSEL	5004 5148h	5008 5148h	500C 5148h
14Ch	16	EPWM_ETPS	5004 514Ch	5008 514Ch	500C 514Ch
150h	16	EPWM_ETFLG	5004 5150h	5008 5150h	500C 5150h
154h	16	EPWM_ETCLR	5004 5154h	5008 5154h	500C 5154h
158h	16	EPWM_ETFRC	5004 5158h	5008 5158h	500C 5158h
15Ch	16	EPWM_ETINTPS	5004 515Ch	5008 515Ch	500C 515Ch
160h	16	EPWM_ETSOCPS	5004 5160h	5008 5160h	500C 5160h
164h	16	EPWM_ETCNTINITCTL	5004 5164h	5008 5164h	500C 5164h
168h	16	EPWM_ETCNTINIT	5004 5168h	5008 5168h	500C 5168h
16Ch	16	EPWM_ETINTMIXEN	5004 516Ch	5008 516Ch	500C 516Ch
170h	16	EPWM_ETSOCAMIXEN	5004 5170h	5008 5170h	500C 5170h
174h	16	EPWM_ETSOCBMIXEN	5004 5174h	5008 5174h	500C 5174h
180h	16	EPWM_DCTRIPSEL	5004 5180h	5008 5180h	500C 5180h
186h	16	EPWM_DCACTL	5004 5186h	5008 5186h	500C 5186h
188h	16	EPWM_DCBCTL	5004 5188h	5008 5188h	500C 5188h
18Eh	16	EPWM_DCFCTL	5004 518Eh	5008 518Eh	500C 518Eh
190h	16	EPWM_DCCAPCTL	5004 5190h	5008 5190h	500C 5190h
192h	16	EPWM_DCFOFFSET	5004 5192h	5008 5192h	500C 5192h
194h	16	EPWM_DCFOFFSETCNT	5004 5194h	5008 5194h	500C 5194h
196h	16	EPWM_DCFWINDOW	5004 5196h	5008 5196h	500C 5196h
198h	16	EPWM_DCFWINDOWCNT	5004 5198h	5008 5198h	500C 5198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5004 519Ah	5008 519Ah	500C 519Ah
19Ch	16	EPWM_DCCAPMIXSEL	5004 519Ch	5008 519Ch	500C 519Ch
19Eh	16	EPWM_DCCAP	5004 519Eh	5008 519Eh	500C 519Eh
1A4h	16	EPWM_DCAHTRIPSEL	5004 51A4h	5008 51A4h	500C 51A4h
1A6h	16	EPWM_DCALTRIPSEL	5004 51A6h	5008 51A6h	500C 51A6h
1A8h	16	EPWM_DCBHTRIPSEL	5004 51A8h	5008 51A8h	500C 51A8h
1AAh	16	EPWM_DCBLTRIPSEL	5004 51AAh	5008 51AAh	500C 51AAh
1ACh	16	EPWM_CAPCTL	5004 51ACh	5008 51ACh	500C 51ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5004 51AEh	5008 51AEh	500C 51AEh
1B0h	16	EPWM_CAPINTRIPSEL	5004 51B0h	5008 51B0h	500C 51B0h
1B2h	16	EPWM_CAPTRIPSEL	5004 51B2h	5008 51B2h	500C 51B2h
1F4h	32	EPWM_EPWMLOCK	5004 51F4h	5008 51F4h	500C 51F4h
1FAh	16	EPWM_HWVDELVAL	5004 51FAh	5008 51FAh	500C 51FAh
1FCh	16	EPWM_VCNTVAL	5004 51FCh	5008 51FCh	500C 51FCh
400h	32	EPWM_XCMPCTL1	5004 5400h	5008 5400h	500C 5400h
410h	32	EPWM_XLOADCTL	5004 5410h	5008 5410h	500C 5410h
418h	32	EPWM_XLOAD	5004 5418h	5008 5418h	500C 5418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5004 541Ch	5008 541Ch	500C 541Ch

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Table 3-577. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM21_G0 Physical Address	EPWM22_G0 Physical Address	EPWM23_G0 Physical Address
420h	32	EPWM_XREGSHDW1STS	5004 5420h	5008 5420h	500C 5420h
428h	32	EPWM_XREGSHDW2STS	5004 5428h	5008 5428h	500C 5428h
430h	32	EPWM_XREGSHDW3STS	5004 5430h	5008 5430h	500C 5430h
600h	32	EPWM_XCMP1_ACTIVE	5004 5600h	5008 5600h	500C 5600h
604h	32	EPWM_XCMP2_ACTIVE	5004 5604h	5008 5604h	500C 5604h
608h	32	EPWM_XCMP3_ACTIVE	5004 5608h	5008 5608h	500C 5608h
60Ch	32	EPWM_XCMP4_ACTIVE	5004 560Ch	5008 560Ch	500C 560Ch
610h	32	EPWM_XCMP5_ACTIVE	5004 5610h	5008 5610h	500C 5610h
614h	32	EPWM_XCMP6_ACTIVE	5004 5614h	5008 5614h	500C 5614h
618h	32	EPWM_XCMP7_ACTIVE	5004 5618h	5008 5618h	500C 5618h
61Ch	32	EPWM_XCMP8_ACTIVE	5004 561Ch	5008 561Ch	500C 561Ch
620h	32	EPWM_XTBPRD_ACTIVE	5004 5620h	5008 5620h	500C 5620h
630h	16	EPWM_XAQCTLA_ACTIVE	5004 5630h	5008 5630h	500C 5630h
644h	32	EPWM_XMINMAX_ACTIVE	5004 5644h	5008 5644h	500C 5644h
680h	32	EPWM_XCMP1_SHDW1	5004 5680h	5008 5680h	500C 5680h
684h	32	EPWM_XCMP2_SHDW1	5004 5684h	5008 5684h	500C 5684h
688h	32	EPWM_XCMP3_SHDW1	5004 5688h	5008 5688h	500C 5688h
68Ch	32	EPWM_XCMP4_SHDW1	5004 568Ch	5008 568Ch	500C 568Ch
690h	32	EPWM_XCMP5_SHDW1	5004 5690h	5008 5690h	500C 5690h
694h	32	EPWM_XCMP6_SHDW1	5004 5694h	5008 5694h	500C 5694h
698h	32	EPWM_XCMP7_SHDW1	5004 5698h	5008 5698h	500C 5698h
69Ch	32	EPWM_XCMP8_SHDW1	5004 569Ch	5008 569Ch	500C 569Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5004 56A0h	5008 56A0h	500C 56A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5004 56B0h	5008 56B0h	500C 56B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5004 56B2h	5008 56B2h	500C 56B2h
6BAh	16	EPWM_CMPC_SHDW1	5004 56BAh	5008 56BAh	500C 56BAh
6BEh	16	EPWM_CMPD_SHDW1	5004 56BEh	5008 56BEh	500C 56BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5004 56C4h	5008 56C4h	500C 56C4h
700h	32	EPWM_XCMP1_SHDW2	5004 5700h	5008 5700h	500C 5700h
704h	32	EPWM_XCMP2_SHDW2	5004 5704h	5008 5704h	500C 5704h
708h	32	EPWM_XCMP3_SHDW2	5004 5708h	5008 5708h	500C 5708h
70Ch	32	EPWM_XCMP4_SHDW2	5004 570Ch	5008 570Ch	500C 570Ch
710h	32	EPWM_XCMP5_SHDW2	5004 5710h	5008 5710h	500C 5710h
714h	32	EPWM_XCMP6_SHDW2	5004 5714h	5008 5714h	500C 5714h
718h	32	EPWM_XCMP7_SHDW2	5004 5718h	5008 5718h	500C 5718h
71Ch	32	EPWM_XCMP8_SHDW2	5004 571Ch	5008 571Ch	500C 571Ch
720h	32	EPWM_XTBPRD_SHDW2	5004 5720h	5008 5720h	500C 5720h
730h	16	EPWM_XAQCTLA_SHDW2	5004 5730h	5008 5730h	500C 5730h
732h	16	EPWM_XAQCTLB_SHDW2	5004 5732h	5008 5732h	500C 5732h
73Ah	16	EPWM_CMPC_SHDW2	5004 573Ah	5008 573Ah	500C 573Ah
73Eh	16	EPWM_CMPD_SHDW2	5004 573Eh	5008 573Eh	500C 573Eh
744h	32	EPWM_XMINMAX_SHDW2	5004 5744h	5008 5744h	500C 5744h
780h	32	EPWM_XCMP1_SHDW3	5004 5780h	5008 5780h	500C 5780h
784h	32	EPWM_XCMP2_SHDW3	5004 5784h	5008 5784h	500C 5784h
788h	32	EPWM_XCMP3_SHDW3	5004 5788h	5008 5788h	500C 5788h
78Ch	32	EPWM_XCMP4_SHDW3	5004 578Ch	5008 578Ch	500C 578Ch

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Table 3-577. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM21_G0 Physical Address	EPWM22_G0 Physical Address	EPWM23_G0 Physical Address
790h	32	EPWM_XCMP5_SHDW3	5004 5790h	5008 5790h	500C 5790h
794h	32	EPWM_XCMP6_SHDW3	5004 5794h	5008 5794h	500C 5794h
798h	32	EPWM_XCMP7_SHDW3	5004 5798h	5008 5798h	500C 5798h
79Ch	32	EPWM_XCMP8_SHDW3	5004 579Ch	5008 579Ch	500C 579Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5004 57A0h	5008 57A0h	500C 57A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5004 57B0h	5008 57B0h	500C 57B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5004 57B2h	5008 57B2h	500C 57B2h
7BAh	16	EPWM_CMPC_SHDW3	5004 57BAh	5008 57BAh	500C 57BAh
7BEh	16	EPWM_CMPD_SHDW3	5004 57BEh	5008 57BEh	500C 57BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5004 57C4h	5008 57C4h	500C 57C4h
800h	32	EPWM_DECTL	5004 5800h	5008 5800h	500C 5800h
804h	32	EPWM_DECOMPSEL	5004 5804h	5008 5804h	500C 5804h
808h	32	EPWM_DEACTCTL	5004 5808h	5008 5808h	500C 5808h
80Ch	32	EPWM_DESTS	5004 580Ch	5008 580Ch	500C 580Ch
810h	32	EPWM_DEFRC	5004 5810h	5008 5810h	500C 5810h
814h	32	EPWM_DECLR	5004 5814h	5008 5814h	500C 5814h
820h	32	EPWM_DEMONCNT	5004 5820h	5008 5820h	500C 5820h
824h	32	EPWM_DEMONCTL	5004 5824h	5008 5824h	500C 5824h
828h	32	EPWM_DEMONSTEP	5004 5828h	5008 5828h	500C 5828h
82Ch	32	EPWM_DEMONTHRES	5004 582Ch	5008 582Ch	500C 582Ch
C00h	32	EPWM_MINDBCFG	5004 5C00h	5008 5C00h	500C 5C00h
C04h	32	EPWM_MINDBDLY	5004 5C04h	5008 5C04h	500C 5C04h
C20h	32	EPWM_LUTCTLA	5004 5C20h	5008 5C20h	500C 5C20h
C24h	32	EPWM_LUTCTLB	5004 5C24h	5008 5C24h	500C 5C24h

Table 3-578. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM24_G0 Physical Address	EPWM25_G0 Physical Address	EPWM26_G0 Physical Address
0h	16	EPWM_TBCTL	5000 6000h	5004 6000h	5008 6000h
2h	16	EPWM_TBCTL2	5000 6002h	5004 6002h	5008 6002h
6h	16	EPWM_EPWMSYNCINSEL	5000 6006h	5004 6006h	5008 6006h
8h	16	EPWM_TBCTR	5000 6008h	5004 6008h	5008 6008h
Ah	16	EPWM_TBSTS	5000 600Ah	5004 600Ah	5008 600Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5000 600Ch	5004 600Ch	5008 600Ch
Eh	16	EPWM_TBCTL3	5000 600Eh	5004 600Eh	5008 600Eh
10h	16	EPWM_CMPCTL	5000 6010h	5004 6010h	5008 6010h
12h	16	EPWM_CMPCTL2	5000 6012h	5004 6012h	5008 6012h
18h	16	EPWM_DBCTL	5000 6018h	5004 6018h	5008 6018h
1Ah	16	EPWM_DBCTL2	5000 601Ah	5004 601Ah	5008 601Ah
20h	16	EPWM_AQCTL	5000 6020h	5004 6020h	5008 6020h
22h	16	EPWM_AQTSRCSEL	5000 6022h	5004 6022h	5008 6022h
28h	16	EPWM_PCCTL	5000 6028h	5004 6028h	5008 6028h
30h	16	EPWM_VCAPCTL	5000 6030h	5004 6030h	5008 6030h
32h	16	EPWM_VCNTCFG	5000 6032h	5004 6032h	5008 6032h
40h	16	EPWM_HRCNFG	5000 6040h	5004 6040h	5008 6040h
4Eh	16	EPWM_HRCNFG2	5000 604Eh	5004 604Eh	5008 604Eh

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Table 3-578. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM24_G0 Physical Address	EPWM25_G0 Physical Address	EPWM26_G0 Physical Address
5Ah	16	EPWM_HRPCTL	5000 605Ah	5004 605Ah	5008 605Ah
5Ch	16	EPWM_TRREM	5000 605Ch	5004 605Ch	5008 605Ch
68h	16	EPWM_GLDCTL	5000 6068h	5004 6068h	5008 6068h
6Ah	16	EPWM_GLDCFG	5000 606Ah	5004 606Ah	5008 606Ah
70h	32	EPWM_EPWMXLINK	5000 6070h	5004 6070h	5008 6070h
74h	32	EPWM_EPWMXLINK2	5000 6074h	5004 6074h	5008 6074h
7Ah	16	EPWM_ETEST	5000 607Ah	5004 607Ah	5008 607Ah
7Ch	16	EPWM_EPWMREV	5000 607Ch	5004 607Ch	5008 607Ch
7Eh	16	EPWM_HRPWMREV	5000 607Eh	5004 607Eh	5008 607Eh
80h	16	EPWM_AQCTLA	5000 6080h	5004 6080h	5008 6080h
82h	16	EPWM_AQCTLA2	5000 6082h	5004 6082h	5008 6082h
84h	16	EPWM_AQCTLB	5000 6084h	5004 6084h	5008 6084h
86h	16	EPWM_AQCTLB2	5000 6086h	5004 6086h	5008 6086h
8Eh	16	EPWM_AQSFRC	5000 608Eh	5004 608Eh	5008 608Eh
92h	16	EPWM_AQCSFRC	5000 6092h	5004 6092h	5008 6092h
A0h	16	EPWM_DBREDHR	5000 60A0h	5004 60A0h	5008 60A0h
A2h	16	EPWM_DBRED	5000 60A2h	5004 60A2h	5008 60A2h
A4h	16	EPWM_DBFEDHR	5000 60A4h	5004 60A4h	5008 60A4h
A6h	16	EPWM_DBFED	5000 60A6h	5004 60A6h	5008 60A6h
C0h	32	EPWM_TBPHS	5000 60C0h	5004 60C0h	5008 60C0h
C4h	16	EPWM_TBPRDHR	5000 60C4h	5004 60C4h	5008 60C4h
C6h	16	EPWM_TBPRD	5000 60C6h	5004 60C6h	5008 60C6h
C8h	16	EPWM_TBPRDHRB	5000 60C8h	5004 60C8h	5008 60C8h
D4h	32	EPWM_CMPA	5000 60D4h	5004 60D4h	5008 60D4h
D8h	32	EPWM_CMPB	5000 60D8h	5004 60D8h	5008 60D8h
DEh	16	EPWM_CMPC	5000 60DEh	5004 60DEh	5008 60DEh
E2h	16	EPWM_CMPD	5000 60E2h	5004 60E2h	5008 60E2h
E8h	16	EPWM_GLDCTL2	5000 60E8h	5004 60E8h	5008 60E8h
EEh	16	EPWM_SWVDELVAL	5000 60EEh	5004 60EEh	5008 60EEh
100h	16	EPWM_TZSEL	5000 6100h	5004 6100h	5008 6100h
102h	16	EPWM_TZSEL2	5000 6102h	5004 6102h	5008 6102h
104h	16	EPWM_TZDCSEL	5000 6104h	5004 6104h	5008 6104h
108h	16	EPWM_TZCTL	5000 6108h	5004 6108h	5008 6108h
10Ah	16	EPWM_TZCTL2	5000 610Ah	5004 610Ah	5008 610Ah
10Ch	16	EPWM_TZCTLDCA	5000 610Ch	5004 610Ch	5008 610Ch
10Eh	16	EPWM_TZCTLDCB	5000 610Eh	5004 610Eh	5008 610Eh
11Ah	16	EPWM_TZEINT	5000 611Ah	5004 611Ah	5008 611Ah
126h	16	EPWM_TZFLG	5000 6126h	5004 6126h	5008 6126h
128h	16	EPWM_TZCBCFLG	5000 6128h	5004 6128h	5008 6128h
12Ah	16	EPWM_TZOSTFLG	5000 612Ah	5004 612Ah	5008 612Ah
12Eh	16	EPWM_TZCLR	5000 612Eh	5004 612Eh	5008 612Eh
130h	16	EPWM_TZCBCCLR	5000 6130h	5004 6130h	5008 6130h
132h	16	EPWM_TZOSTCLR	5000 6132h	5004 6132h	5008 6132h
136h	16	EPWM_TZFRC	5000 6136h	5004 6136h	5008 6136h
13Ah	16	EPWM_TZTRIPOUTSEL	5000 613Ah	5004 613Ah	5008 613Ah
148h	16	EPWM_ETSEL	5000 6148h	5004 6148h	5008 6148h

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Table 3-578. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM24_G0 Physical Address	EPWM25_G0 Physical Address	EPWM26_G0 Physical Address
14Ch	16	EPWM_ETPS	5000 614Ch	5004 614Ch	5008 614Ch
150h	16	EPWM_ETFLG	5000 6150h	5004 6150h	5008 6150h
154h	16	EPWM_ETCLR	5000 6154h	5004 6154h	5008 6154h
158h	16	EPWM_ETFRC	5000 6158h	5004 6158h	5008 6158h
15Ch	16	EPWM_ETINTPS	5000 615Ch	5004 615Ch	5008 615Ch
160h	16	EPWM_ETSOCPS	5000 6160h	5004 6160h	5008 6160h
164h	16	EPWM_ETCNTINITCTL	5000 6164h	5004 6164h	5008 6164h
168h	16	EPWM_ETCNTINIT	5000 6168h	5004 6168h	5008 6168h
16Ch	16	EPWM_ETINTMIXEN	5000 616Ch	5004 616Ch	5008 616Ch
170h	16	EPWM_ETSOCAMIXEN	5000 6170h	5004 6170h	5008 6170h
174h	16	EPWM_ETSOCBMIXEN	5000 6174h	5004 6174h	5008 6174h
180h	16	EPWM_DCTRIPSEL	5000 6180h	5004 6180h	5008 6180h
186h	16	EPWM_DCACTL	5000 6186h	5004 6186h	5008 6186h
188h	16	EPWM_DCBCTL	5000 6188h	5004 6188h	5008 6188h
18Eh	16	EPWM_DCFCTL	5000 618Eh	5004 618Eh	5008 618Eh
190h	16	EPWM_DCCAPCTL	5000 6190h	5004 6190h	5008 6190h
192h	16	EPWM_DCFOFFSET	5000 6192h	5004 6192h	5008 6192h
194h	16	EPWM_DCFOFFSETCNT	5000 6194h	5004 6194h	5008 6194h
196h	16	EPWM_DCFWINDOW	5000 6196h	5004 6196h	5008 6196h
198h	16	EPWM_DCFWINDOWCNT	5000 6198h	5004 6198h	5008 6198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5000 619Ah	5004 619Ah	5008 619Ah
19Ch	16	EPWM_DCCAPMIXSEL	5000 619Ch	5004 619Ch	5008 619Ch
19Eh	16	EPWM_DCCAP	5000 619Eh	5004 619Eh	5008 619Eh
1A4h	16	EPWM_DCAHTRIPSEL	5000 61A4h	5004 61A4h	5008 61A4h
1A6h	16	EPWM_DCALTRIPSEL	5000 61A6h	5004 61A6h	5008 61A6h
1A8h	16	EPWM_DCBHTRIPSEL	5000 61A8h	5004 61A8h	5008 61A8h
1AAh	16	EPWM_DCBLTRIPSEL	5000 61AAh	5004 61AAh	5008 61AAh
1ACh	16	EPWM_CAPCTL	5000 61ACh	5004 61ACh	5008 61ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5000 61AEh	5004 61AEh	5008 61AEh
1B0h	16	EPWM_CAPINTRIPSEL	5000 61B0h	5004 61B0h	5008 61B0h
1B2h	16	EPWM_CAPTRIPSEL	5000 61B2h	5004 61B2h	5008 61B2h
1F4h	32	EPWM_EPWMLOCK	5000 61F4h	5004 61F4h	5008 61F4h
1FAh	16	EPWM_HWVDELVAL	5000 61FAh	5004 61FAh	5008 61FAh
1FCh	16	EPWM_VCNTVAL	5000 61FCh	5004 61FCh	5008 61FCh
400h	32	EPWM_XCMPCTL1	5000 6400h	5004 6400h	5008 6400h
410h	32	EPWM_XLOADCTL	5000 6410h	5004 6410h	5008 6410h
418h	32	EPWM_XLOAD	5000 6418h	5004 6418h	5008 6418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5000 641Ch	5004 641Ch	5008 641Ch
420h	32	EPWM_XREGSHDW1STS	5000 6420h	5004 6420h	5008 6420h
428h	32	EPWM_XREGSHDW2STS	5000 6428h	5004 6428h	5008 6428h
430h	32	EPWM_XREGSHDW3STS	5000 6430h	5004 6430h	5008 6430h
600h	32	EPWM_XCMP1_ACTIVE	5000 6600h	5004 6600h	5008 6600h
604h	32	EPWM_XCMP2_ACTIVE	5000 6604h	5004 6604h	5008 6604h
608h	32	EPWM_XCMP3_ACTIVE	5000 6608h	5004 6608h	5008 6608h
60Ch	32	EPWM_XCMP4_ACTIVE	5000 660Ch	5004 660Ch	5008 660Ch
610h	32	EPWM_XCMP5_ACTIVE	5000 6610h	5004 6610h	5008 6610h

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Table 3-578. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM24_G0 Physical Address	EPWM25_G0 Physical Address	EPWM26_G0 Physical Address
614h	32	EPWM_XCMP6_ACTIVE	5000 6614h	5004 6614h	5008 6614h
618h	32	EPWM_XCMP7_ACTIVE	5000 6618h	5004 6618h	5008 6618h
61Ch	32	EPWM_XCMP8_ACTIVE	5000 661Ch	5004 661Ch	5008 661Ch
620h	32	EPWM_XTBPRD_ACTIVE	5000 6620h	5004 6620h	5008 6620h
630h	16	EPWM_XAQCTLA_ACTIVE	5000 6630h	5004 6630h	5008 6630h
644h	32	EPWM_XMINMAX_ACTIVE	5000 6644h	5004 6644h	5008 6644h
680h	32	EPWM_XCMP1_SHDW1	5000 6680h	5004 6680h	5008 6680h
684h	32	EPWM_XCMP2_SHDW1	5000 6684h	5004 6684h	5008 6684h
688h	32	EPWM_XCMP3_SHDW1	5000 6688h	5004 6688h	5008 6688h
68Ch	32	EPWM_XCMP4_SHDW1	5000 668Ch	5004 668Ch	5008 668Ch
690h	32	EPWM_XCMP5_SHDW1	5000 6690h	5004 6690h	5008 6690h
694h	32	EPWM_XCMP6_SHDW1	5000 6694h	5004 6694h	5008 6694h
698h	32	EPWM_XCMP7_SHDW1	5000 6698h	5004 6698h	5008 6698h
69Ch	32	EPWM_XCMP8_SHDW1	5000 669Ch	5004 669Ch	5008 669Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5000 66A0h	5004 66A0h	5008 66A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5000 66B0h	5004 66B0h	5008 66B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5000 66B2h	5004 66B2h	5008 66B2h
6BAh	16	EPWM_CMPC_SHDW1	5000 66BAh	5004 66BAh	5008 66BAh
6BEh	16	EPWM_CMPD_SHDW1	5000 66BEh	5004 66BEh	5008 66BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5000 66C4h	5004 66C4h	5008 66C4h
700h	32	EPWM_XCMP1_SHDW2	5000 6700h	5004 6700h	5008 6700h
704h	32	EPWM_XCMP2_SHDW2	5000 6704h	5004 6704h	5008 6704h
708h	32	EPWM_XCMP3_SHDW2	5000 6708h	5004 6708h	5008 6708h
70Ch	32	EPWM_XCMP4_SHDW2	5000 670Ch	5004 670Ch	5008 670Ch
710h	32	EPWM_XCMP5_SHDW2	5000 6710h	5004 6710h	5008 6710h
714h	32	EPWM_XCMP6_SHDW2	5000 6714h	5004 6714h	5008 6714h
718h	32	EPWM_XCMP7_SHDW2	5000 6718h	5004 6718h	5008 6718h
71Ch	32	EPWM_XCMP8_SHDW2	5000 671Ch	5004 671Ch	5008 671Ch
720h	32	EPWM_XTBPRD_SHDW2	5000 6720h	5004 6720h	5008 6720h
730h	16	EPWM_XAQCTLA_SHDW2	5000 6730h	5004 6730h	5008 6730h
732h	16	EPWM_XAQCTLB_SHDW2	5000 6732h	5004 6732h	5008 6732h
73Ah	16	EPWM_CMPC_SHDW2	5000 673Ah	5004 673Ah	5008 673Ah
73Eh	16	EPWM_CMPD_SHDW2	5000 673Eh	5004 673Eh	5008 673Eh
744h	32	EPWM_XMINMAX_SHDW2	5000 6744h	5004 6744h	5008 6744h
780h	32	EPWM_XCMP1_SHDW3	5000 6780h	5004 6780h	5008 6780h
784h	32	EPWM_XCMP2_SHDW3	5000 6784h	5004 6784h	5008 6784h
788h	32	EPWM_XCMP3_SHDW3	5000 6788h	5004 6788h	5008 6788h
78Ch	32	EPWM_XCMP4_SHDW3	5000 678Ch	5004 678Ch	5008 678Ch
790h	32	EPWM_XCMP5_SHDW3	5000 6790h	5004 6790h	5008 6790h
794h	32	EPWM_XCMP6_SHDW3	5000 6794h	5004 6794h	5008 6794h
798h	32	EPWM_XCMP7_SHDW3	5000 6798h	5004 6798h	5008 6798h
79Ch	32	EPWM_XCMP8_SHDW3	5000 679Ch	5004 679Ch	5008 679Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5000 67A0h	5004 67A0h	5008 67A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5000 67B0h	5004 67B0h	5008 67B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5000 67B2h	5004 67B2h	5008 67B2h
7BAh	16	EPWM_CMPC_SHDW3	5000 67BAh	5004 67BAh	5008 67BAh

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Table 3-578. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM24_G0 Physical Address	EPWM25_G0 Physical Address	EPWM26_G0 Physical Address
7BEh	16	EPWM_CMPD_SHDW3	5000 67BEh	5004 67BEh	5008 67BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5000 67C4h	5004 67C4h	5008 67C4h
800h	32	EPWM_DECTL	5000 6800h	5004 6800h	5008 6800h
804h	32	EPWM_DECOMPSEL	5000 6804h	5004 6804h	5008 6804h
808h	32	EPWM_DEACTCTL	5000 6808h	5004 6808h	5008 6808h
80Ch	32	EPWM_DESTS	5000 680Ch	5004 680Ch	5008 680Ch
810h	32	EPWM_DEFRC	5000 6810h	5004 6810h	5008 6810h
814h	32	EPWM_DECLR	5000 6814h	5004 6814h	5008 6814h
820h	32	EPWM_DEMONCNT	5000 6820h	5004 6820h	5008 6820h
824h	32	EPWM_DEMONCTL	5000 6824h	5004 6824h	5008 6824h
828h	32	EPWM_DEMONSTEP	5000 6828h	5004 6828h	5008 6828h
82Ch	32	EPWM_DEMONTHRES	5000 682Ch	5004 682Ch	5008 682Ch
C00h	32	EPWM_MINDBCFG	5000 6C00h	5004 6C00h	5008 6C00h
C04h	32	EPWM_MINDBDLY	5000 6C04h	5004 6C04h	5008 6C04h
C20h	32	EPWM_LUTCTLA	5000 6C20h	5004 6C20h	5008 6C20h
C24h	32	EPWM_LUTCTLB	5000 6C24h	5004 6C24h	5008 6C24h

Table 3-579. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM27_G0 Physical Address	EPWM28_G0 Physical Address	EPWM29_G0 Physical Address
0h	16	EPWM_TBCTL	500C 6000h	5000 7000h	5004 7000h
2h	16	EPWM_TBCTL2	500C 6002h	5000 7002h	5004 7002h
6h	16	EPWM_EPWMSYNCINSEL	500C 6006h	5000 7006h	5004 7006h
8h	16	EPWM_TBCTR	500C 6008h	5000 7008h	5004 7008h
Ah	16	EPWM_TBSTS	500C 600Ah	5000 700Ah	5004 700Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500C 600Ch	5000 700Ch	5004 700Ch
Eh	16	EPWM_TBCTL3	500C 600Eh	5000 700Eh	5004 700Eh
10h	16	EPWM_CMPCTL	500C 6010h	5000 7010h	5004 7010h
12h	16	EPWM_CMPCTL2	500C 6012h	5000 7012h	5004 7012h
18h	16	EPWM_DBCTL	500C 6018h	5000 7018h	5004 7018h
1Ah	16	EPWM_DBCTL2	500C 601Ah	5000 701Ah	5004 701Ah
20h	16	EPWM_AQCTL	500C 6020h	5000 7020h	5004 7020h
22h	16	EPWM_AQTSRCSEL	500C 6022h	5000 7022h	5004 7022h
28h	16	EPWM_PCCTL	500C 6028h	5000 7028h	5004 7028h
30h	16	EPWM_VCAPCTL	500C 6030h	5000 7030h	5004 7030h
32h	16	EPWM_VCNTCFG	500C 6032h	5000 7032h	5004 7032h
40h	16	EPWM_HRCNFG	500C 6040h	5000 7040h	5004 7040h
4Eh	16	EPWM_HRCNFG2	500C 604Eh	5000 704Eh	5004 704Eh
5Ah	16	EPWM_HRPCTL	500C 605Ah	5000 705Ah	5004 705Ah
5Ch	16	EPWM_TRREM	500C 605Ch	5000 705Ch	5004 705Ch
68h	16	EPWM_GLDCTL	500C 6068h	5000 7068h	5004 7068h
6Ah	16	EPWM_GLDCFG	500C 606Ah	5000 706Ah	5004 706Ah
70h	32	EPWM_EPWMXLINK	500C 6070h	5000 7070h	5004 7070h
74h	32	EPWM_EPWMXLINK2	500C 6074h	5000 7074h	5004 7074h
7Ah	16	EPWM_ETEST	500C 607Ah	5000 707Ah	5004 707Ah
7Ch	16	EPWM_EPWMREV	500C 607Ch	5000 707Ch	5004 707Ch

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Table 3-579. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM27_G0 Physical Address	EPWM28_G0 Physical Address	EPWM29_G0 Physical Address
7Eh	16	EPWM_HRPWMREV	500C 607Eh	5000 707Eh	5004 707Eh
80h	16	EPWM_AQCTLA	500C 6080h	5000 7080h	5004 7080h
82h	16	EPWM_AQCTLA2	500C 6082h	5000 7082h	5004 7082h
84h	16	EPWM_AQCTLB	500C 6084h	5000 7084h	5004 7084h
86h	16	EPWM_AQCTLB2	500C 6086h	5000 7086h	5004 7086h
8Eh	16	EPWM_AQSFRC	500C 608Eh	5000 708Eh	5004 708Eh
92h	16	EPWM_AQCSFRC	500C 6092h	5000 7092h	5004 7092h
A0h	16	EPWM_DBREDHR	500C 60A0h	5000 70A0h	5004 70A0h
A2h	16	EPWM_DBRED	500C 60A2h	5000 70A2h	5004 70A2h
A4h	16	EPWM_DBFEDHR	500C 60A4h	5000 70A4h	5004 70A4h
A6h	16	EPWM_DBFED	500C 60A6h	5000 70A6h	5004 70A6h
C0h	32	EPWM_TBPHS	500C 60C0h	5000 70C0h	5004 70C0h
C4h	16	EPWM_TBPRDHR	500C 60C4h	5000 70C4h	5004 70C4h
C6h	16	EPWM_TBPRD	500C 60C6h	5000 70C6h	5004 70C6h
C8h	16	EPWM_TBPRDHRB	500C 60C8h	5000 70C8h	5004 70C8h
D4h	32	EPWM_CMPA	500C 60D4h	5000 70D4h	5004 70D4h
D8h	32	EPWM_CMPB	500C 60D8h	5000 70D8h	5004 70D8h
DEh	16	EPWM_CMPC	500C 60DEh	5000 70DEh	5004 70DEh
E2h	16	EPWM_CMPD	500C 60E2h	5000 70E2h	5004 70E2h
E8h	16	EPWM_GLDCTL2	500C 60E8h	5000 70E8h	5004 70E8h
EEh	16	EPWM_SWVDELVAL	500C 60EEh	5000 70EEh	5004 70EEh
100h	16	EPWM_TZSEL	500C 6100h	5000 7100h	5004 7100h
102h	16	EPWM_TZSEL2	500C 6102h	5000 7102h	5004 7102h
104h	16	EPWM_TZDCSEL	500C 6104h	5000 7104h	5004 7104h
108h	16	EPWM_TZCTL	500C 6108h	5000 7108h	5004 7108h
10Ah	16	EPWM_TZCTL2	500C 610Ah	5000 710Ah	5004 710Ah
10Ch	16	EPWM_TZCTLDCA	500C 610Ch	5000 710Ch	5004 710Ch
10Eh	16	EPWM_TZCTLDCB	500C 610Eh	5000 710Eh	5004 710Eh
11Ah	16	EPWM_TZEINT	500C 611Ah	5000 711Ah	5004 711Ah
126h	16	EPWM_TZFLG	500C 6126h	5000 7126h	5004 7126h
128h	16	EPWM_TZCBCFLG	500C 6128h	5000 7128h	5004 7128h
12Ah	16	EPWM_TZOSTFLG	500C 612Ah	5000 712Ah	5004 712Ah
12Eh	16	EPWM_TZCLR	500C 612Eh	5000 712Eh	5004 712Eh
130h	16	EPWM_TZCBCCLR	500C 6130h	5000 7130h	5004 7130h
132h	16	EPWM_TZOSTCLR	500C 6132h	5000 7132h	5004 7132h
136h	16	EPWM_TZFRC	500C 6136h	5000 7136h	5004 7136h
13Ah	16	EPWM_TZTRIPOUTSEL	500C 613Ah	5000 713Ah	5004 713Ah
148h	16	EPWM_ETSEL	500C 6148h	5000 7148h	5004 7148h
14Ch	16	EPWM_ETPS	500C 614Ch	5000 714Ch	5004 714Ch
150h	16	EPWM_ETFLG	500C 6150h	5000 7150h	5004 7150h
154h	16	EPWM_ETCLR	500C 6154h	5000 7154h	5004 7154h
158h	16	EPWM_ETFRC	500C 6158h	5000 7158h	5004 7158h
15Ch	16	EPWM_ETINTPS	500C 615Ch	5000 715Ch	5004 715Ch
160h	16	EPWM_ETSOCPS	500C 6160h	5000 7160h	5004 7160h
164h	16	EPWM_ETCNTINITCTL	500C 6164h	5000 7164h	5004 7164h
168h	16	EPWM_ETCNTINIT	500C 6168h	5000 7168h	5004 7168h

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Table 3-579. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM27_G0 Physical Address	EPWM28_G0 Physical Address	EPWM29_G0 Physical Address
16Ch	16	EPWM_ETINTMIXEN	500C 616Ch	5000 716Ch	5004 716Ch
170h	16	EPWM_ETSOCAMIXEN	500C 6170h	5000 7170h	5004 7170h
174h	16	EPWM_ETSOCBMIXEN	500C 6174h	5000 7174h	5004 7174h
180h	16	EPWM_DCTRIPSEL	500C 6180h	5000 7180h	5004 7180h
186h	16	EPWM_DCACTL	500C 6186h	5000 7186h	5004 7186h
188h	16	EPWM_DCBCTL	500C 6188h	5000 7188h	5004 7188h
18Eh	16	EPWM_DCFCTL	500C 618Eh	5000 718Eh	5004 718Eh
190h	16	EPWM_DCCAPCTL	500C 6190h	5000 7190h	5004 7190h
192h	16	EPWM_DCFOFFSET	500C 6192h	5000 7192h	5004 7192h
194h	16	EPWM_DCFOFFSETCNT	500C 6194h	5000 7194h	5004 7194h
196h	16	EPWM_DCFWINDOW	500C 6196h	5000 7196h	5004 7196h
198h	16	EPWM_DCFWINDOWCNT	500C 6198h	5000 7198h	5004 7198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500C 619Ah	5000 719Ah	5004 719Ah
19Ch	16	EPWM_DCCAPMIXSEL	500C 619Ch	5000 719Ch	5004 719Ch
19Eh	16	EPWM_DCCAP	500C 619Eh	5000 719Eh	5004 719Eh
1A4h	16	EPWM_DCAHTRIPSEL	500C 61A4h	5000 71A4h	5004 71A4h
1A6h	16	EPWM_DCALTRIPSEL	500C 61A6h	5000 71A6h	5004 71A6h
1A8h	16	EPWM_DCBHTRIPSEL	500C 61A8h	5000 71A8h	5004 71A8h
1AAh	16	EPWM_DCBLTRIPSEL	500C 61AAh	5000 71AAh	5004 71AAh
1ACh	16	EPWM_CAPCTL	500C 61ACh	5000 71ACh	5004 71ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500C 61AEh	5000 71AEh	5004 71AEh
1B0h	16	EPWM_CAPINTRIPSEL	500C 61B0h	5000 71B0h	5004 71B0h
1B2h	16	EPWM_CAPTRIPSEL	500C 61B2h	5000 71B2h	5004 71B2h
1F4h	32	EPWM_EPWMLOCK	500C 61F4h	5000 71F4h	5004 71F4h
1FAh	16	EPWM_HWVDELVAL	500C 61FAh	5000 71FAh	5004 71FAh
1FCh	16	EPWM_VCNTVAL	500C 61FCh	5000 71FCh	5004 71FCh
400h	32	EPWM_XCMPCTL1	500C 6400h	5000 7400h	5004 7400h
410h	32	EPWM_XLOADCTL	500C 6410h	5000 7410h	5004 7410h
418h	32	EPWM_XLOAD	500C 6418h	5000 7418h	5004 7418h
41Ch	32	EPWM_EPWMXLINKXLOAD	500C 641Ch	5000 741Ch	5004 741Ch
420h	32	EPWM_XREGSHDW1STS	500C 6420h	5000 7420h	5004 7420h
428h	32	EPWM_XREGSHDW2STS	500C 6428h	5000 7428h	5004 7428h
430h	32	EPWM_XREGSHDW3STS	500C 6430h	5000 7430h	5004 7430h
600h	32	EPWM_XCMP1_ACTIVE	500C 6600h	5000 7600h	5004 7600h
604h	32	EPWM_XCMP2_ACTIVE	500C 6604h	5000 7604h	5004 7604h
608h	32	EPWM_XCMP3_ACTIVE	500C 6608h	5000 7608h	5004 7608h
60Ch	32	EPWM_XCMP4_ACTIVE	500C 660Ch	5000 760Ch	5004 760Ch
610h	32	EPWM_XCMP5_ACTIVE	500C 6610h	5000 7610h	5004 7610h
614h	32	EPWM_XCMP6_ACTIVE	500C 6614h	5000 7614h	5004 7614h
618h	32	EPWM_XCMP7_ACTIVE	500C 6618h	5000 7618h	5004 7618h
61Ch	32	EPWM_XCMP8_ACTIVE	500C 661Ch	5000 761Ch	5004 761Ch
620h	32	EPWM_XTBPRD_ACTIVE	500C 6620h	5000 7620h	5004 7620h
630h	16	EPWM_XAQCTLA_ACTIVE	500C 6630h	5000 7630h	5004 7630h
644h	32	EPWM_XMINMAX_ACTIVE	500C 6644h	5000 7644h	5004 7644h
680h	32	EPWM_XCMP1_SHDW1	500C 6680h	5000 7680h	5004 7680h
684h	32	EPWM_XCMP2_SHDW1	500C 6684h	5000 7684h	5004 7684h

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Table 3-579. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM27_G0 Physical Address	EPWM28_G0 Physical Address	EPWM29_G0 Physical Address
688h	32	EPWM_XCMP3_SHDW1	500C 6688h	5000 7688h	5004 7688h
68Ch	32	EPWM_XCMP4_SHDW1	500C 668Ch	5000 768Ch	5004 768Ch
690h	32	EPWM_XCMP5_SHDW1	500C 6690h	5000 7690h	5004 7690h
694h	32	EPWM_XCMP6_SHDW1	500C 6694h	5000 7694h	5004 7694h
698h	32	EPWM_XCMP7_SHDW1	500C 6698h	5000 7698h	5004 7698h
69Ch	32	EPWM_XCMP8_SHDW1	500C 669Ch	5000 769Ch	5004 769Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500C 66A0h	5000 76A0h	5004 76A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500C 66B0h	5000 76B0h	5004 76B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500C 66B2h	5000 76B2h	5004 76B2h
6BAh	16	EPWM_CMPC_SHDW1	500C 66BAh	5000 76BAh	5004 76BAh
6BEh	16	EPWM_CMPD_SHDW1	500C 66BEh	5000 76BEh	5004 76BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500C 66C4h	5000 76C4h	5004 76C4h
700h	32	EPWM_XCMP1_SHDW2	500C 6700h	5000 7700h	5004 7700h
704h	32	EPWM_XCMP2_SHDW2	500C 6704h	5000 7704h	5004 7704h
708h	32	EPWM_XCMP3_SHDW2	500C 6708h	5000 7708h	5004 7708h
70Ch	32	EPWM_XCMP4_SHDW2	500C 670Ch	5000 770Ch	5004 770Ch
710h	32	EPWM_XCMP5_SHDW2	500C 6710h	5000 7710h	5004 7710h
714h	32	EPWM_XCMP6_SHDW2	500C 6714h	5000 7714h	5004 7714h
718h	32	EPWM_XCMP7_SHDW2	500C 6718h	5000 7718h	5004 7718h
71Ch	32	EPWM_XCMP8_SHDW2	500C 671Ch	5000 771Ch	5004 771Ch
720h	32	EPWM_XTBPRD_SHDW2	500C 6720h	5000 7720h	5004 7720h
730h	16	EPWM_XAQCTLA_SHDW2	500C 6730h	5000 7730h	5004 7730h
732h	16	EPWM_XAQCTLB_SHDW2	500C 6732h	5000 7732h	5004 7732h
73Ah	16	EPWM_CMPC_SHDW2	500C 673Ah	5000 773Ah	5004 773Ah
73Eh	16	EPWM_CMPD_SHDW2	500C 673Eh	5000 773Eh	5004 773Eh
744h	32	EPWM_XMINMAX_SHDW2	500C 6744h	5000 7744h	5004 7744h
780h	32	EPWM_XCMP1_SHDW3	500C 6780h	5000 7780h	5004 7780h
784h	32	EPWM_XCMP2_SHDW3	500C 6784h	5000 7784h	5004 7784h
788h	32	EPWM_XCMP3_SHDW3	500C 6788h	5000 7788h	5004 7788h
78Ch	32	EPWM_XCMP4_SHDW3	500C 678Ch	5000 778Ch	5004 778Ch
790h	32	EPWM_XCMP5_SHDW3	500C 6790h	5000 7790h	5004 7790h
794h	32	EPWM_XCMP6_SHDW3	500C 6794h	5000 7794h	5004 7794h
798h	32	EPWM_XCMP7_SHDW3	500C 6798h	5000 7798h	5004 7798h
79Ch	32	EPWM_XCMP8_SHDW3	500C 679Ch	5000 779Ch	5004 779Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500C 67A0h	5000 77A0h	5004 77A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500C 67B0h	5000 77B0h	5004 77B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500C 67B2h	5000 77B2h	5004 77B2h
7BAh	16	EPWM_CMPC_SHDW3	500C 67BAh	5000 77BAh	5004 77BAh
7BEh	16	EPWM_CMPD_SHDW3	500C 67BEh	5000 77BEh	5004 77BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500C 67C4h	5000 77C4h	5004 77C4h
800h	32	EPWM_DECTL	500C 6800h	5000 7800h	5004 7800h
804h	32	EPWM_DECOMPSEL	500C 6804h	5000 7804h	5004 7804h
808h	32	EPWM_DEACTCTL	500C 6808h	5000 7808h	5004 7808h
80Ch	32	EPWM_DESTS	500C 680Ch	5000 780Ch	5004 780Ch
810h	32	EPWM_DEFRC	500C 6810h	5000 7810h	5004 7810h
814h	32	EPWM_DECLR	500C 6814h	5000 7814h	5004 7814h

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Table 3-579. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM27_G0 Physical Address	EPWM28_G0 Physical Address	EPWM29_G0 Physical Address
820h	32	EPWM_DEMONCNT	500C 6820h	5000 7820h	5004 7820h
824h	32	EPWM_DEMONCTL	500C 6824h	5000 7824h	5004 7824h
828h	32	EPWM_DEMONSTEP	500C 6828h	5000 7828h	5004 7828h
82Ch	32	EPWM_DEMONTHRES	500C 682Ch	5000 782Ch	5004 782Ch
C00h	32	EPWM_MINDBCFG	500C 6C00h	5000 7C00h	5004 7C00h
C04h	32	EPWM_MINDBDLY	500C 6C04h	5000 7C04h	5004 7C04h
C20h	32	EPWM_LUTCTLA	500C 6C20h	5000 7C20h	5004 7C20h
C24h	32	EPWM_LUTCTLB	500C 6C24h	5000 7C24h	5004 7C24h

Table 3-580. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM30_G0 Physical Address	EPWM31_G0 Physical Address	EPWM00_G1 Physical Address
0h	16	EPWM_TBCTL	5008 7000h	500C 7000h	5000 8000h
2h	16	EPWM_TBCTL2	5008 7002h	500C 7002h	5000 8002h
6h	16	EPWM_EPWMSYNCINSEL	5008 7006h	500C 7006h	5000 8006h
8h	16	EPWM_TBCTR	5008 7008h	500C 7008h	5000 8008h
Ah	16	EPWM_TBSTS	5008 700Ah	500C 700Ah	5000 800Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5008 700Ch	500C 700Ch	5000 800Ch
Eh	16	EPWM_TBCTL3	5008 700Eh	500C 700Eh	5000 800Eh
10h	16	EPWM_CMPCTL	5008 7010h	500C 7010h	5000 8010h
12h	16	EPWM_CMPCTL2	5008 7012h	500C 7012h	5000 8012h
18h	16	EPWM_DBCTL	5008 7018h	500C 7018h	5000 8018h
1Ah	16	EPWM_DBCTL2	5008 701Ah	500C 701Ah	5000 801Ah
20h	16	EPWM_AQCTL	5008 7020h	500C 7020h	5000 8020h
22h	16	EPWM_AQTSRCSEL	5008 7022h	500C 7022h	5000 8022h
28h	16	EPWM_PCCTL	5008 7028h	500C 7028h	5000 8028h
30h	16	EPWM_VCAPCTL	5008 7030h	500C 7030h	5000 8030h
32h	16	EPWM_VCNTCFG	5008 7032h	500C 7032h	5000 8032h
40h	16	EPWM_HRCNFG	5008 7040h	500C 7040h	5000 8040h
4Eh	16	EPWM_HRCNFG2	5008 704Eh	500C 704Eh	5000 804Eh
5Ah	16	EPWM_HRPCTL	5008 705Ah	500C 705Ah	5000 805Ah
5Ch	16	EPWM_TRREM	5008 705Ch	500C 705Ch	5000 805Ch
68h	16	EPWM_GLDCTL	5008 7068h	500C 7068h	5000 8068h
6Ah	16	EPWM_GLDCFG	5008 706Ah	500C 706Ah	5000 806Ah
70h	32	EPWM_EPWMXLINK	5008 7070h	500C 7070h	5000 8070h
74h	32	EPWM_EPWMXLINK2	5008 7074h	500C 7074h	5000 8074h
7Ah	16	EPWM_ETEST	5008 707Ah	500C 707Ah	5000 807Ah
7Ch	16	EPWM_EPWMREV	5008 707Ch	500C 707Ch	5000 807Ch
7Eh	16	EPWM_HRPWMREV	5008 707Eh	500C 707Eh	5000 807Eh
80h	16	EPWM_AQCTLA	5008 7080h	500C 7080h	5000 8080h
82h	16	EPWM_AQCTLA2	5008 7082h	500C 7082h	5000 8082h
84h	16	EPWM_AQCTLB	5008 7084h	500C 7084h	5000 8084h
86h	16	EPWM_AQCTLB2	5008 7086h	500C 7086h	5000 8086h
8Eh	16	EPWM_AQSFRC	5008 708Eh	500C 708Eh	5000 808Eh
92h	16	EPWM_AQCSFRC	5008 7092h	500C 7092h	5000 8092h
A0h	16	EPWM_DBREDHR	5008 70A0h	500C 70A0h	5000 80A0h

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Table 3-580. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM30_G0 Physical Address	EPWM31_G0 Physical Address	EPWM00_G1 Physical Address
A2h	16	EPWM_DBRED	5008 70A2h	500C 70A2h	5000 80A2h
A4h	16	EPWM_DBFEDHR	5008 70A4h	500C 70A4h	5000 80A4h
A6h	16	EPWM_DBFED	5008 70A6h	500C 70A6h	5000 80A6h
C0h	32	EPWM_TBPHS	5008 70C0h	500C 70C0h	5000 80C0h
C4h	16	EPWM_TBPRDHR	5008 70C4h	500C 70C4h	5000 80C4h
C6h	16	EPWM_TBPRD	5008 70C6h	500C 70C6h	5000 80C6h
C8h	16	EPWM_TBPRDHRB	5008 70C8h	500C 70C8h	5000 80C8h
D4h	32	EPWM_CMPA	5008 70D4h	500C 70D4h	5000 80D4h
D8h	32	EPWM_CMPB	5008 70D8h	500C 70D8h	5000 80D8h
DEh	16	EPWM_CMPC	5008 70DEh	500C 70DEh	5000 80DEh
E2h	16	EPWM_CMPD	5008 70E2h	500C 70E2h	5000 80E2h
E8h	16	EPWM_GLDCTL2	5008 70E8h	500C 70E8h	5000 80E8h
EEh	16	EPWM_SWVDELVAL	5008 70EEh	500C 70EEh	5000 80EEh
100h	16	EPWM_TZSEL	5008 7100h	500C 7100h	5000 8100h
102h	16	EPWM_TZSEL2	5008 7102h	500C 7102h	5000 8102h
104h	16	EPWM_TZDCSEL	5008 7104h	500C 7104h	5000 8104h
108h	16	EPWM_TZCTL	5008 7108h	500C 7108h	5000 8108h
10Ah	16	EPWM_TZCTL2	5008 710Ah	500C 710Ah	5000 810Ah
10Ch	16	EPWM_TZCTLDCA	5008 710Ch	500C 710Ch	5000 810Ch
10Eh	16	EPWM_TZCTLDCB	5008 710Eh	500C 710Eh	5000 810Eh
11Ah	16	EPWM_TZEINT	5008 711Ah	500C 711Ah	5000 811Ah
126h	16	EPWM_TZFLG	5008 7126h	500C 7126h	5000 8126h
128h	16	EPWM_TZCBCFLG	5008 7128h	500C 7128h	5000 8128h
12Ah	16	EPWM_TZOSTFLG	5008 712Ah	500C 712Ah	5000 812Ah
12Eh	16	EPWM_TZCLR	5008 712Eh	500C 712Eh	5000 812Eh
130h	16	EPWM_TZCBCCLR	5008 7130h	500C 7130h	5000 8130h
132h	16	EPWM_TZOSTCLR	5008 7132h	500C 7132h	5000 8132h
136h	16	EPWM_TZFRC	5008 7136h	500C 7136h	5000 8136h
13Ah	16	EPWM_TZTRIPOUTSEL	5008 713Ah	500C 713Ah	5000 813Ah
148h	16	EPWM_ETSEL	5008 7148h	500C 7148h	5000 8148h
14Ch	16	EPWM_ETPS	5008 714Ch	500C 714Ch	5000 814Ch
150h	16	EPWM_ETFLG	5008 7150h	500C 7150h	5000 8150h
154h	16	EPWM_ETCLR	5008 7154h	500C 7154h	5000 8154h
158h	16	EPWM_ETFRC	5008 7158h	500C 7158h	5000 8158h
15Ch	16	EPWM_ETINTPS	5008 715Ch	500C 715Ch	5000 815Ch
160h	16	EPWM_ETSOCPS	5008 7160h	500C 7160h	5000 8160h
164h	16	EPWM_ETCNTINITCTL	5008 7164h	500C 7164h	5000 8164h
168h	16	EPWM_ETCNTINIT	5008 7168h	500C 7168h	5000 8168h
16Ch	16	EPWM_ETINTMIXEN	5008 716Ch	500C 716Ch	5000 816Ch
170h	16	EPWM_ETSOCAMIXEN	5008 7170h	500C 7170h	5000 8170h
174h	16	EPWM_ETSOCBMIXEN	5008 7174h	500C 7174h	5000 8174h
180h	16	EPWM_DCTRIPSEL	5008 7180h	500C 7180h	5000 8180h
186h	16	EPWM_DCACTL	5008 7186h	500C 7186h	5000 8186h
188h	16	EPWM_DCBCTL	5008 7188h	500C 7188h	5000 8188h
18Eh	16	EPWM_DCFCTL	5008 718Eh	500C 718Eh	5000 818Eh
190h	16	EPWM_DCCAPCTL	5008 7190h	500C 7190h	5000 8190h

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Table 3-580. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM30_G0 Physical Address	EPWM31_G0 Physical Address	EPWM00_G1 Physical Address
192h	16	EPWM_DCFOFFSET	5008 7192h	500C 7192h	5000 8192h
194h	16	EPWM_DCFOFFSETCNT	5008 7194h	500C 7194h	5000 8194h
196h	16	EPWM_DCFWINDOW	5008 7196h	500C 7196h	5000 8196h
198h	16	EPWM_DCFWINDOWCNT	5008 7198h	500C 7198h	5000 8198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5008 719Ah	500C 719Ah	5000 819Ah
19Ch	16	EPWM_DCCAPMIXSEL	5008 719Ch	500C 719Ch	5000 819Ch
19Eh	16	EPWM_DCCAP	5008 719Eh	500C 719Eh	5000 819Eh
1A4h	16	EPWM_DCAHTRIPSEL	5008 71A4h	500C 71A4h	5000 81A4h
1A6h	16	EPWM_DCALTRIPSEL	5008 71A6h	500C 71A6h	5000 81A6h
1A8h	16	EPWM_DCBHTRIPSEL	5008 71A8h	500C 71A8h	5000 81A8h
1AAh	16	EPWM_DCBLTRIPSEL	5008 71AAh	500C 71AAh	5000 81AAh
1ACh	16	EPWM_CAPCTL	5008 71ACh	500C 71ACh	5000 81ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5008 71AEh	500C 71AEh	5000 81AEh
1B0h	16	EPWM_CAPINTRIPSEL	5008 71B0h	500C 71B0h	5000 81B0h
1B2h	16	EPWM_CAPTRIPSEL	5008 71B2h	500C 71B2h	5000 81B2h
1F4h	32	EPWM_EPWMLOCK	5008 71F4h	500C 71F4h	5000 81F4h
1FAh	16	EPWM_HWVDELVAL	5008 71FAh	500C 71FAh	5000 81FAh
1FCh	16	EPWM_VCNTVAL	5008 71FCh	500C 71FCh	5000 81FCh
400h	32	EPWM_XCMPCTL1	5008 7400h	500C 7400h	5000 8400h
410h	32	EPWM_XLOADCTL	5008 7410h	500C 7410h	5000 8410h
418h	32	EPWM_XLOAD	5008 7418h	500C 7418h	5000 8418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5008 741Ch	500C 741Ch	5000 841Ch
420h	32	EPWM_XREGSHDW1STS	5008 7420h	500C 7420h	5000 8420h
428h	32	EPWM_XREGSHDW2STS	5008 7428h	500C 7428h	5000 8428h
430h	32	EPWM_XREGSHDW3STS	5008 7430h	500C 7430h	5000 8430h
600h	32	EPWM_XCMP1_ACTIVE	5008 7600h	500C 7600h	5000 8600h
604h	32	EPWM_XCMP2_ACTIVE	5008 7604h	500C 7604h	5000 8604h
608h	32	EPWM_XCMP3_ACTIVE	5008 7608h	500C 7608h	5000 8608h
60Ch	32	EPWM_XCMP4_ACTIVE	5008 760Ch	500C 760Ch	5000 860Ch
610h	32	EPWM_XCMP5_ACTIVE	5008 7610h	500C 7610h	5000 8610h
614h	32	EPWM_XCMP6_ACTIVE	5008 7614h	500C 7614h	5000 8614h
618h	32	EPWM_XCMP7_ACTIVE	5008 7618h	500C 7618h	5000 8618h
61Ch	32	EPWM_XCMP8_ACTIVE	5008 761Ch	500C 761Ch	5000 861Ch
620h	32	EPWM_XTBPRD_ACTIVE	5008 7620h	500C 7620h	5000 8620h
630h	16	EPWM_XAQCTLA_ACTIVE	5008 7630h	500C 7630h	5000 8630h
644h	32	EPWM_XMINMAX_ACTIVE	5008 7644h	500C 7644h	5000 8644h
680h	32	EPWM_XCMP1_SHDW1	5008 7680h	500C 7680h	5000 8680h
684h	32	EPWM_XCMP2_SHDW1	5008 7684h	500C 7684h	5000 8684h
688h	32	EPWM_XCMP3_SHDW1	5008 7688h	500C 7688h	5000 8688h
68Ch	32	EPWM_XCMP4_SHDW1	5008 768Ch	500C 768Ch	5000 868Ch
690h	32	EPWM_XCMP5_SHDW1	5008 7690h	500C 7690h	5000 8690h
694h	32	EPWM_XCMP6_SHDW1	5008 7694h	500C 7694h	5000 8694h
698h	32	EPWM_XCMP7_SHDW1	5008 7698h	500C 7698h	5000 8698h
69Ch	32	EPWM_XCMP8_SHDW1	5008 769Ch	500C 769Ch	5000 869Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5008 76A0h	500C 76A0h	5000 86A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5008 76B0h	500C 76B0h	5000 86B0h

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Table 3-580. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM30_G0 Physical Address	EPWM31_G0 Physical Address	EPWM00_G1 Physical Address
6B2h	16	EPWM_XAQCTLB_SHDW1	5008 76B2h	500C 76B2h	5000 86B2h
6BAh	16	EPWM_CMPC_SHDW1	5008 76BAh	500C 76BAh	5000 86BAh
6BEh	16	EPWM_CMPD_SHDW1	5008 76BEh	500C 76BEh	5000 86BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5008 76C4h	500C 76C4h	5000 86C4h
700h	32	EPWM_XCMP1_SHDW2	5008 7700h	500C 7700h	5000 8700h
704h	32	EPWM_XCMP2_SHDW2	5008 7704h	500C 7704h	5000 8704h
708h	32	EPWM_XCMP3_SHDW2	5008 7708h	500C 7708h	5000 8708h
70Ch	32	EPWM_XCMP4_SHDW2	5008 770Ch	500C 770Ch	5000 870Ch
710h	32	EPWM_XCMP5_SHDW2	5008 7710h	500C 7710h	5000 8710h
714h	32	EPWM_XCMP6_SHDW2	5008 7714h	500C 7714h	5000 8714h
718h	32	EPWM_XCMP7_SHDW2	5008 7718h	500C 7718h	5000 8718h
71Ch	32	EPWM_XCMP8_SHDW2	5008 771Ch	500C 771Ch	5000 871Ch
720h	32	EPWM_XTBPRD_SHDW2	5008 7720h	500C 7720h	5000 8720h
730h	16	EPWM_XAQCTLA_SHDW2	5008 7730h	500C 7730h	5000 8730h
732h	16	EPWM_XAQCTLB_SHDW2	5008 7732h	500C 7732h	5000 8732h
73Ah	16	EPWM_CMPC_SHDW2	5008 773Ah	500C 773Ah	5000 873Ah
73Eh	16	EPWM_CMPD_SHDW2	5008 773Eh	500C 773Eh	5000 873Eh
744h	32	EPWM_XMINMAX_SHDW2	5008 7744h	500C 7744h	5000 8744h
780h	32	EPWM_XCMP1_SHDW3	5008 7780h	500C 7780h	5000 8780h
784h	32	EPWM_XCMP2_SHDW3	5008 7784h	500C 7784h	5000 8784h
788h	32	EPWM_XCMP3_SHDW3	5008 7788h	500C 7788h	5000 8788h
78Ch	32	EPWM_XCMP4_SHDW3	5008 778Ch	500C 778Ch	5000 878Ch
790h	32	EPWM_XCMP5_SHDW3	5008 7790h	500C 7790h	5000 8790h
794h	32	EPWM_XCMP6_SHDW3	5008 7794h	500C 7794h	5000 8794h
798h	32	EPWM_XCMP7_SHDW3	5008 7798h	500C 7798h	5000 8798h
79Ch	32	EPWM_XCMP8_SHDW3	5008 779Ch	500C 779Ch	5000 879Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5008 77A0h	500C 77A0h	5000 87A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5008 77B0h	500C 77B0h	5000 87B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5008 77B2h	500C 77B2h	5000 87B2h
7BAh	16	EPWM_CMPC_SHDW3	5008 77BAh	500C 77BAh	5000 87BAh
7BEh	16	EPWM_CMPD_SHDW3	5008 77BEh	500C 77BEh	5000 87BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5008 77C4h	500C 77C4h	5000 87C4h
800h	32	EPWM_DECTL	5008 7800h	500C 7800h	5000 8800h
804h	32	EPWM_DECOMPSEL	5008 7804h	500C 7804h	5000 8804h
808h	32	EPWM_DEACTCTL	5008 7808h	500C 7808h	5000 8808h
80Ch	32	EPWM_DESTS	5008 780Ch	500C 780Ch	5000 880Ch
810h	32	EPWM_DEFRC	5008 7810h	500C 7810h	5000 8810h
814h	32	EPWM_DECLR	5008 7814h	500C 7814h	5000 8814h
820h	32	EPWM_DEMONCNT	5008 7820h	500C 7820h	5000 8820h
824h	32	EPWM_DEMONCTL	5008 7824h	500C 7824h	5000 8824h
828h	32	EPWM_DEMONSTEP	5008 7828h	500C 7828h	5000 8828h
82Ch	32	EPWM_DEMONTHRES	5008 782Ch	500C 782Ch	5000 882Ch
C00h	32	EPWM_MINDBCFG	5008 7C00h	500C 7C00h	5000 8C00h
C04h	32	EPWM_MINDBDLY	5008 7C04h	500C 7C04h	5000 8C04h
C20h	32	EPWM_LUTCTLA	5008 7C20h	500C 7C20h	5000 8C20h

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Table 3-580. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM30_G0 Physical Address	EPWM31_G0 Physical Address	EPWM00_G1 Physical Address
C24h	32	EPWM_LUTCTLB	5008 7C24h	500C 7C24h	5000 8C24h

Table 3-581. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM01_G1 Physical Address	EPWM02_G1 Physical Address	EPWM03_G1 Physical Address
0h	16	EPWM_TBCTL	5004 8000h	5008 8000h	500C 8000h
2h	16	EPWM_TBCTL2	5004 8002h	5008 8002h	500C 8002h
6h	16	EPWM_EPWMSYNCINSEL	5004 8006h	5008 8006h	500C 8006h
8h	16	EPWM_TBCTR	5004 8008h	5008 8008h	500C 8008h
Ah	16	EPWM_TBSTS	5004 800Ah	5008 800Ah	500C 800Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5004 800Ch	5008 800Ch	500C 800Ch
Eh	16	EPWM_TBCTL3	5004 800Eh	5008 800Eh	500C 800Eh
10h	16	EPWM_CMPCTL	5004 8010h	5008 8010h	500C 8010h
12h	16	EPWM_CMPCTL2	5004 8012h	5008 8012h	500C 8012h
18h	16	EPWM_DBCTL	5004 8018h	5008 8018h	500C 8018h
1Ah	16	EPWM_DBCTL2	5004 801Ah	5008 801Ah	500C 801Ah
20h	16	EPWM_AQCTL	5004 8020h	5008 8020h	500C 8020h
22h	16	EPWM_AQTSRCSEL	5004 8022h	5008 8022h	500C 8022h
28h	16	EPWM_PCCTL	5004 8028h	5008 8028h	500C 8028h
30h	16	EPWM_VCAPCTL	5004 8030h	5008 8030h	500C 8030h
32h	16	EPWM_VCNTCFG	5004 8032h	5008 8032h	500C 8032h
40h	16	EPWM_HRCNFG	5004 8040h	5008 8040h	500C 8040h
4Eh	16	EPWM_HRCNFG2	5004 804Eh	5008 804Eh	500C 804Eh
5Ah	16	EPWM_HRPCTL	5004 805Ah	5008 805Ah	500C 805Ah
5Ch	16	EPWM_TRREM	5004 805Ch	5008 805Ch	500C 805Ch
68h	16	EPWM_GLDCTL	5004 8068h	5008 8068h	500C 8068h
6Ah	16	EPWM_GLDCFG	5004 806Ah	5008 806Ah	500C 806Ah
70h	32	EPWM_EPWMXLINK	5004 8070h	5008 8070h	500C 8070h
74h	32	EPWM_EPWMXLINK2	5004 8074h	5008 8074h	500C 8074h
7Ah	16	EPWM_ETEST	5004 807Ah	5008 807Ah	500C 807Ah
7Ch	16	EPWM_EPWMREV	5004 807Ch	5008 807Ch	500C 807Ch
7Eh	16	EPWM_HRPWMREV	5004 807Eh	5008 807Eh	500C 807Eh
80h	16	EPWM_AQCTLA	5004 8080h	5008 8080h	500C 8080h
82h	16	EPWM_AQCTLA2	5004 8082h	5008 8082h	500C 8082h
84h	16	EPWM_AQCTLB	5004 8084h	5008 8084h	500C 8084h
86h	16	EPWM_AQCTLB2	5004 8086h	5008 8086h	500C 8086h
8Eh	16	EPWM_AQSFRC	5004 808Eh	5008 808Eh	500C 808Eh
92h	16	EPWM_AQCSFRC	5004 8092h	5008 8092h	500C 8092h
A0h	16	EPWM_DBREDHR	5004 80A0h	5008 80A0h	500C 80A0h
A2h	16	EPWM_DBRED	5004 80A2h	5008 80A2h	500C 80A2h
A4h	16	EPWM_DBFEDHR	5004 80A4h	5008 80A4h	500C 80A4h
A6h	16	EPWM_DBFED	5004 80A6h	5008 80A6h	500C 80A6h
C0h	32	EPWM_TBPHS	5004 80C0h	5008 80C0h	500C 80C0h
C4h	16	EPWM_TBPRDHR	5004 80C4h	5008 80C4h	500C 80C4h
C6h	16	EPWM_TBPRD	5004 80C6h	5008 80C6h	500C 80C6h
C8h	16	EPWM_TBPRDHRB	5004 80C8h	5008 80C8h	500C 80C8h

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Table 3-581. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM01_G1 Physical Address	EPWM02_G1 Physical Address	EPWM03_G1 Physical Address
D4h	32	EPWM_CMPA	5004 80D4h	5008 80D4h	500C 80D4h
D8h	32	EPWM_CMPB	5004 80D8h	5008 80D8h	500C 80D8h
DEh	16	EPWM_CMPC	5004 80DEh	5008 80DEh	500C 80DEh
E2h	16	EPWM_CMPD	5004 80E2h	5008 80E2h	500C 80E2h
E8h	16	EPWM_GLDCTL2	5004 80E8h	5008 80E8h	500C 80E8h
EEh	16	EPWM_SWVDELVAL	5004 80EEh	5008 80EEh	500C 80EEh
100h	16	EPWM_TZSEL	5004 8100h	5008 8100h	500C 8100h
102h	16	EPWM_TZSEL2	5004 8102h	5008 8102h	500C 8102h
104h	16	EPWM_TZDCSEL	5004 8104h	5008 8104h	500C 8104h
108h	16	EPWM_TZCTL	5004 8108h	5008 8108h	500C 8108h
10Ah	16	EPWM_TZCTL2	5004 810Ah	5008 810Ah	500C 810Ah
10Ch	16	EPWM_TZCTLDCA	5004 810Ch	5008 810Ch	500C 810Ch
10Eh	16	EPWM_TZCTLDCB	5004 810Eh	5008 810Eh	500C 810Eh
11Ah	16	EPWM_TZEINT	5004 811Ah	5008 811Ah	500C 811Ah
126h	16	EPWM_TZFLG	5004 8126h	5008 8126h	500C 8126h
128h	16	EPWM_TZCBCFLG	5004 8128h	5008 8128h	500C 8128h
12Ah	16	EPWM_TZOSTFLG	5004 812Ah	5008 812Ah	500C 812Ah
12Eh	16	EPWM_TZCLR	5004 812Eh	5008 812Eh	500C 812Eh
130h	16	EPWM_TZCBCCLR	5004 8130h	5008 8130h	500C 8130h
132h	16	EPWM_TZOSTCLR	5004 8132h	5008 8132h	500C 8132h
136h	16	EPWM_TZFRC	5004 8136h	5008 8136h	500C 8136h
13Ah	16	EPWM_TZTRIPOUTSEL	5004 813Ah	5008 813Ah	500C 813Ah
148h	16	EPWM_ETSEL	5004 8148h	5008 8148h	500C 8148h
14Ch	16	EPWM_ETPS	5004 814Ch	5008 814Ch	500C 814Ch
150h	16	EPWM_ETFLG	5004 8150h	5008 8150h	500C 8150h
154h	16	EPWM_ETCLR	5004 8154h	5008 8154h	500C 8154h
158h	16	EPWM_ETFRC	5004 8158h	5008 8158h	500C 8158h
15Ch	16	EPWM_ETINTPS	5004 815Ch	5008 815Ch	500C 815Ch
160h	16	EPWM_ETSOCPS	5004 8160h	5008 8160h	500C 8160h
164h	16	EPWM_ETCNTINITCTL	5004 8164h	5008 8164h	500C 8164h
168h	16	EPWM_ETCNTINIT	5004 8168h	5008 8168h	500C 8168h
16Ch	16	EPWM_ETINTMIXEN	5004 816Ch	5008 816Ch	500C 816Ch
170h	16	EPWM_ETSOCAMIXEN	5004 8170h	5008 8170h	500C 8170h
174h	16	EPWM_ETSOCBMIXEN	5004 8174h	5008 8174h	500C 8174h
180h	16	EPWM_DCTRIPSEL	5004 8180h	5008 8180h	500C 8180h
186h	16	EPWM_DCACTL	5004 8186h	5008 8186h	500C 8186h
188h	16	EPWM_DCBCTL	5004 8188h	5008 8188h	500C 8188h
18Eh	16	EPWM_DCFCTL	5004 818Eh	5008 818Eh	500C 818Eh
190h	16	EPWM_DCCAPCTL	5004 8190h	5008 8190h	500C 8190h
192h	16	EPWM_DCFOFFSET	5004 8192h	5008 8192h	500C 8192h
194h	16	EPWM_DCFOFFSETCNT	5004 8194h	5008 8194h	500C 8194h
196h	16	EPWM_DCFWINDOW	5004 8196h	5008 8196h	500C 8196h
198h	16	EPWM_DCFWINDOWCNT	5004 8198h	5008 8198h	500C 8198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5004 819Ah	5008 819Ah	500C 819Ah
19Ch	16	EPWM_DCCAPMIXSEL	5004 819Ch	5008 819Ch	500C 819Ch
19Eh	16	EPWM_DCCAP	5004 819Eh	5008 819Eh	500C 819Eh

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Table 3-581. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM01_G1 Physical Address	EPWM02_G1 Physical Address	EPWM03_G1 Physical Address
1A4h	16	EPWM_DCAHTRIPSEL	5004 81A4h	5008 81A4h	500C 81A4h
1A6h	16	EPWM_DCALTRIPSEL	5004 81A6h	5008 81A6h	500C 81A6h
1A8h	16	EPWM_DCBHTRIPSEL	5004 81A8h	5008 81A8h	500C 81A8h
1AAh	16	EPWM_DCBLTRIPSEL	5004 81AAh	5008 81AAh	500C 81AAh
1ACh	16	EPWM_CAPCTL	5004 81ACh	5008 81ACh	500C 81ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5004 81AEh	5008 81AEh	500C 81AEh
1B0h	16	EPWM_CAPINTRIPSEL	5004 81B0h	5008 81B0h	500C 81B0h
1B2h	16	EPWM_CAPTRIPSEL	5004 81B2h	5008 81B2h	500C 81B2h
1F4h	32	EPWM_EPWMLOCK	5004 81F4h	5008 81F4h	500C 81F4h
1FAh	16	EPWM_HWVDELVAL	5004 81FAh	5008 81FAh	500C 81FAh
1FCh	16	EPWM_VCNTVAL	5004 81FCh	5008 81FCh	500C 81FCh
400h	32	EPWM_XCMPCTL1	5004 8400h	5008 8400h	500C 8400h
410h	32	EPWM_XLOADCTL	5004 8410h	5008 8410h	500C 8410h
418h	32	EPWM_XLOAD	5004 8418h	5008 8418h	500C 8418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5004 841Ch	5008 841Ch	500C 841Ch
420h	32	EPWM_XREGSHDW1STS	5004 8420h	5008 8420h	500C 8420h
428h	32	EPWM_XREGSHDW2STS	5004 8428h	5008 8428h	500C 8428h
430h	32	EPWM_XREGSHDW3STS	5004 8430h	5008 8430h	500C 8430h
600h	32	EPWM_XCMP1_ACTIVE	5004 8600h	5008 8600h	500C 8600h
604h	32	EPWM_XCMP2_ACTIVE	5004 8604h	5008 8604h	500C 8604h
608h	32	EPWM_XCMP3_ACTIVE	5004 8608h	5008 8608h	500C 8608h
60Ch	32	EPWM_XCMP4_ACTIVE	5004 860Ch	5008 860Ch	500C 860Ch
610h	32	EPWM_XCMP5_ACTIVE	5004 8610h	5008 8610h	500C 8610h
614h	32	EPWM_XCMP6_ACTIVE	5004 8614h	5008 8614h	500C 8614h
618h	32	EPWM_XCMP7_ACTIVE	5004 8618h	5008 8618h	500C 8618h
61Ch	32	EPWM_XCMP8_ACTIVE	5004 861Ch	5008 861Ch	500C 861Ch
620h	32	EPWM_XTBPRD_ACTIVE	5004 8620h	5008 8620h	500C 8620h
630h	16	EPWM_XAQCTLA_ACTIVE	5004 8630h	5008 8630h	500C 8630h
644h	32	EPWM_XMINMAX_ACTIVE	5004 8644h	5008 8644h	500C 8644h
680h	32	EPWM_XCMP1_SHDW1	5004 8680h	5008 8680h	500C 8680h
684h	32	EPWM_XCMP2_SHDW1	5004 8684h	5008 8684h	500C 8684h
688h	32	EPWM_XCMP3_SHDW1	5004 8688h	5008 8688h	500C 8688h
68Ch	32	EPWM_XCMP4_SHDW1	5004 868Ch	5008 868Ch	500C 868Ch
690h	32	EPWM_XCMP5_SHDW1	5004 8690h	5008 8690h	500C 8690h
694h	32	EPWM_XCMP6_SHDW1	5004 8694h	5008 8694h	500C 8694h
698h	32	EPWM_XCMP7_SHDW1	5004 8698h	5008 8698h	500C 8698h
69Ch	32	EPWM_XCMP8_SHDW1	5004 869Ch	5008 869Ch	500C 869Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5004 86A0h	5008 86A0h	500C 86A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5004 86B0h	5008 86B0h	500C 86B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5004 86B2h	5008 86B2h	500C 86B2h
6BAh	16	EPWM_CMPC_SHDW1	5004 86BAh	5008 86BAh	500C 86BAh
6BEh	16	EPWM_CMPD_SHDW1	5004 86BEh	5008 86BEh	500C 86BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5004 86C4h	5008 86C4h	500C 86C4h
700h	32	EPWM_XCMP1_SHDW2	5004 8700h	5008 8700h	500C 8700h
704h	32	EPWM_XCMP2_SHDW2	5004 8704h	5008 8704h	500C 8704h
708h	32	EPWM_XCMP3_SHDW2	5004 8708h	5008 8708h	500C 8708h

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Table 3-581. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM01_G1 Physical Address	EPWM02_G1 Physical Address	EPWM03_G1 Physical Address
70Ch	32	EPWM_XCMP4_SHDW2	5004 870Ch	5008 870Ch	500C 870Ch
710h	32	EPWM_XCMP5_SHDW2	5004 8710h	5008 8710h	500C 8710h
714h	32	EPWM_XCMP6_SHDW2	5004 8714h	5008 8714h	500C 8714h
718h	32	EPWM_XCMP7_SHDW2	5004 8718h	5008 8718h	500C 8718h
71Ch	32	EPWM_XCMP8_SHDW2	5004 871Ch	5008 871Ch	500C 871Ch
720h	32	EPWM_XTBPRD_SHDW2	5004 8720h	5008 8720h	500C 8720h
730h	16	EPWM_XAQCTLA_SHDW2	5004 8730h	5008 8730h	500C 8730h
732h	16	EPWM_XAQCTLB_SHDW2	5004 8732h	5008 8732h	500C 8732h
73Ah	16	EPWM_CMPC_SHDW2	5004 873Ah	5008 873Ah	500C 873Ah
73Eh	16	EPWM_CMPD_SHDW2	5004 873Eh	5008 873Eh	500C 873Eh
744h	32	EPWM_XMINMAX_SHDW2	5004 8744h	5008 8744h	500C 8744h
780h	32	EPWM_XCMP1_SHDW3	5004 8780h	5008 8780h	500C 8780h
784h	32	EPWM_XCMP2_SHDW3	5004 8784h	5008 8784h	500C 8784h
788h	32	EPWM_XCMP3_SHDW3	5004 8788h	5008 8788h	500C 8788h
78Ch	32	EPWM_XCMP4_SHDW3	5004 878Ch	5008 878Ch	500C 878Ch
790h	32	EPWM_XCMP5_SHDW3	5004 8790h	5008 8790h	500C 8790h
794h	32	EPWM_XCMP6_SHDW3	5004 8794h	5008 8794h	500C 8794h
798h	32	EPWM_XCMP7_SHDW3	5004 8798h	5008 8798h	500C 8798h
79Ch	32	EPWM_XCMP8_SHDW3	5004 879Ch	5008 879Ch	500C 879Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5004 87A0h	5008 87A0h	500C 87A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5004 87B0h	5008 87B0h	500C 87B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5004 87B2h	5008 87B2h	500C 87B2h
7BAh	16	EPWM_CMPC_SHDW3	5004 87BAh	5008 87BAh	500C 87BAh
7BEh	16	EPWM_CMPD_SHDW3	5004 87BEh	5008 87BEh	500C 87BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5004 87C4h	5008 87C4h	500C 87C4h
800h	32	EPWM_DECTL	5004 8800h	5008 8800h	500C 8800h
804h	32	EPWM_DECOMPSEL	5004 8804h	5008 8804h	500C 8804h
808h	32	EPWM_DEACTCTL	5004 8808h	5008 8808h	500C 8808h
80Ch	32	EPWM_DESTS	5004 880Ch	5008 880Ch	500C 880Ch
810h	32	EPWM_DEFRC	5004 8810h	5008 8810h	500C 8810h
814h	32	EPWM_DECLR	5004 8814h	5008 8814h	500C 8814h
820h	32	EPWM_DEMONCNT	5004 8820h	5008 8820h	500C 8820h
824h	32	EPWM_DEMONCTL	5004 8824h	5008 8824h	500C 8824h
828h	32	EPWM_DEMONSTEP	5004 8828h	5008 8828h	500C 8828h
82Ch	32	EPWM_DEMONTHRES	5004 882Ch	5008 882Ch	500C 882Ch
C00h	32	EPWM_MINDBCFG	5004 8C00h	5008 8C00h	500C 8C00h
C04h	32	EPWM_MINDBDLY	5004 8C04h	5008 8C04h	500C 8C04h
C20h	32	EPWM_LUTCTLA	5004 8C20h	5008 8C20h	500C 8C20h
C24h	32	EPWM_LUTCTLB	5004 8C24h	5008 8C24h	500C 8C24h

Table 3-582. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM04_G1 Physical Address	EPWM05_G1 Physical Address	EPWM06_G1 Physical Address
0h	16	EPWM_TBCTL	5000 9000h	5004 9000h	5008 9000h
2h	16	EPWM_TBCTL2	5000 9002h	5004 9002h	5008 9002h
6h	16	EPWM_EPWMSYNCINSEL	5000 9006h	5004 9006h	5008 9006h

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Table 3-582. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM04_G1 Physical Address	EPWM05_G1 Physical Address	EPWM06_G1 Physical Address
8h	16	EPWM_TBCTR	5000 9008h	5004 9008h	5008 9008h
Ah	16	EPWM_TBSTS	5000 900Ah	5004 900Ah	5008 900Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5000 900Ch	5004 900Ch	5008 900Ch
Eh	16	EPWM_TBCTL3	5000 900Eh	5004 900Eh	5008 900Eh
10h	16	EPWM_CMPCTL	5000 9010h	5004 9010h	5008 9010h
12h	16	EPWM_CMPCTL2	5000 9012h	5004 9012h	5008 9012h
18h	16	EPWM_DBCTL	5000 9018h	5004 9018h	5008 9018h
1Ah	16	EPWM_DBCTL2	5000 901Ah	5004 901Ah	5008 901Ah
20h	16	EPWM_AQCTL	5000 9020h	5004 9020h	5008 9020h
22h	16	EPWM_AQTSRCSEL	5000 9022h	5004 9022h	5008 9022h
28h	16	EPWM_PCCTL	5000 9028h	5004 9028h	5008 9028h
30h	16	EPWM_VCAPCTL	5000 9030h	5004 9030h	5008 9030h
32h	16	EPWM_VCNTCFG	5000 9032h	5004 9032h	5008 9032h
40h	16	EPWM_HRCNFG	5000 9040h	5004 9040h	5008 9040h
4Eh	16	EPWM_HRCNFG2	5000 904Eh	5004 904Eh	5008 904Eh
5Ah	16	EPWM_HRPCTL	5000 905Ah	5004 905Ah	5008 905Ah
5Ch	16	EPWM_TRREM	5000 905Ch	5004 905Ch	5008 905Ch
68h	16	EPWM_GLDCTL	5000 9068h	5004 9068h	5008 9068h
6Ah	16	EPWM_GLDCFG	5000 906Ah	5004 906Ah	5008 906Ah
70h	32	EPWM_EPWMXLINK	5000 9070h	5004 9070h	5008 9070h
74h	32	EPWM_EPWMXLINK2	5000 9074h	5004 9074h	5008 9074h
7Ah	16	EPWM_ETEST	5000 907Ah	5004 907Ah	5008 907Ah
7Ch	16	EPWM_EPWMREV	5000 907Ch	5004 907Ch	5008 907Ch
7Eh	16	EPWM_HRPWMREV	5000 907Eh	5004 907Eh	5008 907Eh
80h	16	EPWM_AQCTLA	5000 9080h	5004 9080h	5008 9080h
82h	16	EPWM_AQCTLA2	5000 9082h	5004 9082h	5008 9082h
84h	16	EPWM_AQCTLB	5000 9084h	5004 9084h	5008 9084h
86h	16	EPWM_AQCTLB2	5000 9086h	5004 9086h	5008 9086h
8Eh	16	EPWM_AQSFRC	5000 908Eh	5004 908Eh	5008 908Eh
92h	16	EPWM_AQCSFRC	5000 9092h	5004 9092h	5008 9092h
A0h	16	EPWM_DBREDHR	5000 90A0h	5004 90A0h	5008 90A0h
A2h	16	EPWM_DBRED	5000 90A2h	5004 90A2h	5008 90A2h
A4h	16	EPWM_DBFEDHR	5000 90A4h	5004 90A4h	5008 90A4h
A6h	16	EPWM_DBFED	5000 90A6h	5004 90A6h	5008 90A6h
C0h	32	EPWM_TBPHS	5000 90C0h	5004 90C0h	5008 90C0h
C4h	16	EPWM_TBPRDHR	5000 90C4h	5004 90C4h	5008 90C4h
C6h	16	EPWM_TBPRD	5000 90C6h	5004 90C6h	5008 90C6h
C8h	16	EPWM_TBPRDHRB	5000 90C8h	5004 90C8h	5008 90C8h
D4h	32	EPWM_CMPA	5000 90D4h	5004 90D4h	5008 90D4h
D8h	32	EPWM_CMPB	5000 90D8h	5004 90D8h	5008 90D8h
DEh	16	EPWM_CMPC	5000 90DEh	5004 90DEh	5008 90DEh
E2h	16	EPWM_CMPD	5000 90E2h	5004 90E2h	5008 90E2h
E8h	16	EPWM_GLDCTL2	5000 90E8h	5004 90E8h	5008 90E8h
EEh	16	EPWM_SWVDELVAL	5000 90EEh	5004 90EEh	5008 90EEh
100h	16	EPWM_TZSEL	5000 9100h	5004 9100h	5008 9100h
102h	16	EPWM_TZSEL2	5000 9102h	5004 9102h	5008 9102h

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Table 3-582. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM04_G1 Physical Address	EPWM05_G1 Physical Address	EPWM06_G1 Physical Address
104h	16	EPWM_TZDCSEL	5000 9104h	5004 9104h	5008 9104h
108h	16	EPWM_TZCTL	5000 9108h	5004 9108h	5008 9108h
10Ah	16	EPWM_TZCTL2	5000 910Ah	5004 910Ah	5008 910Ah
10Ch	16	EPWM_TZCTLDCA	5000 910Ch	5004 910Ch	5008 910Ch
10Eh	16	EPWM_TZCTLDCB	5000 910Eh	5004 910Eh	5008 910Eh
11Ah	16	EPWM_TZEINT	5000 911Ah	5004 911Ah	5008 911Ah
126h	16	EPWM_TZFLG	5000 9126h	5004 9126h	5008 9126h
128h	16	EPWM_TZCBCFLG	5000 9128h	5004 9128h	5008 9128h
12Ah	16	EPWM_TZOSTFLG	5000 912Ah	5004 912Ah	5008 912Ah
12Eh	16	EPWM_TZCLR	5000 912Eh	5004 912Eh	5008 912Eh
130h	16	EPWM_TZCBCCLR	5000 9130h	5004 9130h	5008 9130h
132h	16	EPWM_TZOSTCLR	5000 9132h	5004 9132h	5008 9132h
136h	16	EPWM_TZFRC	5000 9136h	5004 9136h	5008 9136h
13Ah	16	EPWM_TZTRIPOUTSEL	5000 913Ah	5004 913Ah	5008 913Ah
148h	16	EPWM_ETSEL	5000 9148h	5004 9148h	5008 9148h
14Ch	16	EPWM_ETPS	5000 914Ch	5004 914Ch	5008 914Ch
150h	16	EPWM_ETFLG	5000 9150h	5004 9150h	5008 9150h
154h	16	EPWM_ETCLR	5000 9154h	5004 9154h	5008 9154h
158h	16	EPWM_ETFRC	5000 9158h	5004 9158h	5008 9158h
15Ch	16	EPWM_ETINTPS	5000 915Ch	5004 915Ch	5008 915Ch
160h	16	EPWM_ETSOCPS	5000 9160h	5004 9160h	5008 9160h
164h	16	EPWM_ETCNTINITCTL	5000 9164h	5004 9164h	5008 9164h
168h	16	EPWM_ETCNTINIT	5000 9168h	5004 9168h	5008 9168h
16Ch	16	EPWM_ETINTMIXEN	5000 916Ch	5004 916Ch	5008 916Ch
170h	16	EPWM_ETSOCAMIXEN	5000 9170h	5004 9170h	5008 9170h
174h	16	EPWM_ETSOCBMIXEN	5000 9174h	5004 9174h	5008 9174h
180h	16	EPWM_DCTRIPSEL	5000 9180h	5004 9180h	5008 9180h
186h	16	EPWM_DCACTL	5000 9186h	5004 9186h	5008 9186h
188h	16	EPWM_DCBCTL	5000 9188h	5004 9188h	5008 9188h
18Eh	16	EPWM_DCFCTL	5000 918Eh	5004 918Eh	5008 918Eh
190h	16	EPWM_DCCAPCTL	5000 9190h	5004 9190h	5008 9190h
192h	16	EPWM_DCFOFFSET	5000 9192h	5004 9192h	5008 9192h
194h	16	EPWM_DCFOFFSETCNT	5000 9194h	5004 9194h	5008 9194h
196h	16	EPWM_DCFWINDOW	5000 9196h	5004 9196h	5008 9196h
198h	16	EPWM_DCFWINDOWCNT	5000 9198h	5004 9198h	5008 9198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5000 919Ah	5004 919Ah	5008 919Ah
19Ch	16	EPWM_DCCAPMIXSEL	5000 919Ch	5004 919Ch	5008 919Ch
19Eh	16	EPWM_DCCAP	5000 919Eh	5004 919Eh	5008 919Eh
1A4h	16	EPWM_DCAHTRIPSEL	5000 91A4h	5004 91A4h	5008 91A4h
1A6h	16	EPWM_DCALTRIPSEL	5000 91A6h	5004 91A6h	5008 91A6h
1A8h	16	EPWM_DCBHTRIPSEL	5000 91A8h	5004 91A8h	5008 91A8h
1AAh	16	EPWM_DCBLTRIPSEL	5000 91AAh	5004 91AAh	5008 91AAh
1ACh	16	EPWM_CAPCTL	5000 91ACh	5004 91ACh	5008 91ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5000 91AEh	5004 91AEh	5008 91AEh
1B0h	16	EPWM_CAPINTRIPSEL	5000 91B0h	5004 91B0h	5008 91B0h
1B2h	16	EPWM_CAPTRIPSEL	5000 91B2h	5004 91B2h	5008 91B2h

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Table 3-582. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM04_G1 Physical Address	EPWM05_G1 Physical Address	EPWM06_G1 Physical Address
1F4h	32	EPWM_EPWMLOCK	5000 91F4h	5004 91F4h	5008 91F4h
1FAh	16	EPWM_HWVDELVAL	5000 91FAh	5004 91FAh	5008 91FAh
1FCh	16	EPWM_VCNTVAL	5000 91FCh	5004 91FCh	5008 91FCh
400h	32	EPWM_XCMPCTL1	5000 9400h	5004 9400h	5008 9400h
410h	32	EPWM_XLOADCTL	5000 9410h	5004 9410h	5008 9410h
418h	32	EPWM_XLOAD	5000 9418h	5004 9418h	5008 9418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5000 941Ch	5004 941Ch	5008 941Ch
420h	32	EPWM_XREGSHDW1STS	5000 9420h	5004 9420h	5008 9420h
428h	32	EPWM_XREGSHDW2STS	5000 9428h	5004 9428h	5008 9428h
430h	32	EPWM_XREGSHDW3STS	5000 9430h	5004 9430h	5008 9430h
600h	32	EPWM_XCMP1_ACTIVE	5000 9600h	5004 9600h	5008 9600h
604h	32	EPWM_XCMP2_ACTIVE	5000 9604h	5004 9604h	5008 9604h
608h	32	EPWM_XCMP3_ACTIVE	5000 9608h	5004 9608h	5008 9608h
60Ch	32	EPWM_XCMP4_ACTIVE	5000 960Ch	5004 960Ch	5008 960Ch
610h	32	EPWM_XCMP5_ACTIVE	5000 9610h	5004 9610h	5008 9610h
614h	32	EPWM_XCMP6_ACTIVE	5000 9614h	5004 9614h	5008 9614h
618h	32	EPWM_XCMP7_ACTIVE	5000 9618h	5004 9618h	5008 9618h
61Ch	32	EPWM_XCMP8_ACTIVE	5000 961Ch	5004 961Ch	5008 961Ch
620h	32	EPWM_XTBPRD_ACTIVE	5000 9620h	5004 9620h	5008 9620h
630h	16	EPWM_XAQCTLA_ACTIVE	5000 9630h	5004 9630h	5008 9630h
644h	32	EPWM_XMINMAX_ACTIVE	5000 9644h	5004 9644h	5008 9644h
680h	32	EPWM_XCMP1_SHDW1	5000 9680h	5004 9680h	5008 9680h
684h	32	EPWM_XCMP2_SHDW1	5000 9684h	5004 9684h	5008 9684h
688h	32	EPWM_XCMP3_SHDW1	5000 9688h	5004 9688h	5008 9688h
68Ch	32	EPWM_XCMP4_SHDW1	5000 968Ch	5004 968Ch	5008 968Ch
690h	32	EPWM_XCMP5_SHDW1	5000 9690h	5004 9690h	5008 9690h
694h	32	EPWM_XCMP6_SHDW1	5000 9694h	5004 9694h	5008 9694h
698h	32	EPWM_XCMP7_SHDW1	5000 9698h	5004 9698h	5008 9698h
69Ch	32	EPWM_XCMP8_SHDW1	5000 969Ch	5004 969Ch	5008 969Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5000 96A0h	5004 96A0h	5008 96A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5000 96B0h	5004 96B0h	5008 96B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5000 96B2h	5004 96B2h	5008 96B2h
6BAh	16	EPWM_CMPC_SHDW1	5000 96BAh	5004 96BAh	5008 96BAh
6BEh	16	EPWM_CMPD_SHDW1	5000 96BEh	5004 96BEh	5008 96BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5000 96C4h	5004 96C4h	5008 96C4h
700h	32	EPWM_XCMP1_SHDW2	5000 9700h	5004 9700h	5008 9700h
704h	32	EPWM_XCMP2_SHDW2	5000 9704h	5004 9704h	5008 9704h
708h	32	EPWM_XCMP3_SHDW2	5000 9708h	5004 9708h	5008 9708h
70Ch	32	EPWM_XCMP4_SHDW2	5000 970Ch	5004 970Ch	5008 970Ch
710h	32	EPWM_XCMP5_SHDW2	5000 9710h	5004 9710h	5008 9710h
714h	32	EPWM_XCMP6_SHDW2	5000 9714h	5004 9714h	5008 9714h
718h	32	EPWM_XCMP7_SHDW2	5000 9718h	5004 9718h	5008 9718h
71Ch	32	EPWM_XCMP8_SHDW2	5000 971Ch	5004 971Ch	5008 971Ch
720h	32	EPWM_XTBPRD_SHDW2	5000 9720h	5004 9720h	5008 9720h
730h	16	EPWM_XAQCTLA_SHDW2	5000 9730h	5004 9730h	5008 9730h
732h	16	EPWM_XAQCTLB_SHDW2	5000 9732h	5004 9732h	5008 9732h

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Table 3-582. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM04_G1 Physical Address	EPWM05_G1 Physical Address	EPWM06_G1 Physical Address
73Ah	16	EPWM_CMPC_SHDW2	5000 973Ah	5004 973Ah	5008 973Ah
73Eh	16	EPWM_CMPD_SHDW2	5000 973Eh	5004 973Eh	5008 973Eh
744h	32	EPWM_XMINMAX_SHDW2	5000 9744h	5004 9744h	5008 9744h
780h	32	EPWM_XCMP1_SHDW3	5000 9780h	5004 9780h	5008 9780h
784h	32	EPWM_XCMP2_SHDW3	5000 9784h	5004 9784h	5008 9784h
788h	32	EPWM_XCMP3_SHDW3	5000 9788h	5004 9788h	5008 9788h
78Ch	32	EPWM_XCMP4_SHDW3	5000 978Ch	5004 978Ch	5008 978Ch
790h	32	EPWM_XCMP5_SHDW3	5000 9790h	5004 9790h	5008 9790h
794h	32	EPWM_XCMP6_SHDW3	5000 9794h	5004 9794h	5008 9794h
798h	32	EPWM_XCMP7_SHDW3	5000 9798h	5004 9798h	5008 9798h
79Ch	32	EPWM_XCMP8_SHDW3	5000 979Ch	5004 979Ch	5008 979Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5000 97A0h	5004 97A0h	5008 97A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5000 97B0h	5004 97B0h	5008 97B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5000 97B2h	5004 97B2h	5008 97B2h
7BAh	16	EPWM_CMPC_SHDW3	5000 97BAh	5004 97BAh	5008 97BAh
7BEh	16	EPWM_CMPD_SHDW3	5000 97BEh	5004 97BEh	5008 97BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5000 97C4h	5004 97C4h	5008 97C4h
800h	32	EPWM_DECTL	5000 9800h	5004 9800h	5008 9800h
804h	32	EPWM_DECOMPSEL	5000 9804h	5004 9804h	5008 9804h
808h	32	EPWM_DEACTCTL	5000 9808h	5004 9808h	5008 9808h
80Ch	32	EPWM_DESTS	5000 980Ch	5004 980Ch	5008 980Ch
810h	32	EPWM_DEFRC	5000 9810h	5004 9810h	5008 9810h
814h	32	EPWM_DECLR	5000 9814h	5004 9814h	5008 9814h
820h	32	EPWM_DEMONCNT	5000 9820h	5004 9820h	5008 9820h
824h	32	EPWM_DEMONCTL	5000 9824h	5004 9824h	5008 9824h
828h	32	EPWM_DEMONSTEP	5000 9828h	5004 9828h	5008 9828h
82Ch	32	EPWM_DEMONTHRES	5000 982Ch	5004 982Ch	5008 982Ch
C00h	32	EPWM_MINDBCFG	5000 9C00h	5004 9C00h	5008 9C00h
C04h	32	EPWM_MINDBDLY	5000 9C04h	5004 9C04h	5008 9C04h
C20h	32	EPWM_LUTCTLA	5000 9C20h	5004 9C20h	5008 9C20h
C24h	32	EPWM_LUTCTLB	5000 9C24h	5004 9C24h	5008 9C24h

Table 3-583. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM07_G1 Physical Address	EPWM08_G1 Physical Address	EPWM09_G1 Physical Address
0h	16	EPWM_TBCTL	500C 9000h	5000 A000h	5004 A000h
2h	16	EPWM_TBCTL2	500C 9002h	5000 A002h	5004 A002h
6h	16	EPWM_EPWMSYNCINSEL	500C 9006h	5000 A006h	5004 A006h
8h	16	EPWM_TBCTR	500C 9008h	5000 A008h	5004 A008h
Ah	16	EPWM_TBSTS	500C 900Ah	5000 A00Ah	5004 A00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500C 900Ch	5000 A00Ch	5004 A00Ch
Eh	16	EPWM_TBCTL3	500C 900Eh	5000 A00Eh	5004 A00Eh
10h	16	EPWM_CMPCTL	500C 9010h	5000 A010h	5004 A010h
12h	16	EPWM_CMPCTL2	500C 9012h	5000 A012h	5004 A012h
18h	16	EPWM_DBCTL	500C 9018h	5000 A018h	5004 A018h
1Ah	16	EPWM_DBCTL2	500C 901Ah	5000 A01Ah	5004 A01Ah

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Table 3-583. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM07_G1 Physical Address	EPWM08_G1 Physical Address	EPWM09_G1 Physical Address
20h	16	EPWM_AQCTL	500C 9020h	5000 A020h	5004 A020h
22h	16	EPWM_AQTSRCSEL	500C 9022h	5000 A022h	5004 A022h
28h	16	EPWM_PCCTL	500C 9028h	5000 A028h	5004 A028h
30h	16	EPWM_VCAPCTL	500C 9030h	5000 A030h	5004 A030h
32h	16	EPWM_VCNTCFG	500C 9032h	5000 A032h	5004 A032h
40h	16	EPWM_HRCNFG	500C 9040h	5000 A040h	5004 A040h
4Eh	16	EPWM_HRCNFG2	500C 904Eh	5000 A04Eh	5004 A04Eh
5Ah	16	EPWM_HRPCTL	500C 905Ah	5000 A05Ah	5004 A05Ah
5Ch	16	EPWM_TRREM	500C 905Ch	5000 A05Ch	5004 A05Ch
68h	16	EPWM_GLDCTL	500C 9068h	5000 A068h	5004 A068h
6Ah	16	EPWM_GLDCFG	500C 906Ah	5000 A06Ah	5004 A06Ah
70h	32	EPWM_EPWMXLINK	500C 9070h	5000 A070h	5004 A070h
74h	32	EPWM_EPWMXLINK2	500C 9074h	5000 A074h	5004 A074h
7Ah	16	EPWM_ETEST	500C 907Ah	5000 A07Ah	5004 A07Ah
7Ch	16	EPWM_EPWMREV	500C 907Ch	5000 A07Ch	5004 A07Ch
7Eh	16	EPWM_HRPWMREV	500C 907Eh	5000 A07Eh	5004 A07Eh
80h	16	EPWM_AQCTLA	500C 9080h	5000 A080h	5004 A080h
82h	16	EPWM_AQCTLA2	500C 9082h	5000 A082h	5004 A082h
84h	16	EPWM_AQCTLB	500C 9084h	5000 A084h	5004 A084h
86h	16	EPWM_AQCTLB2	500C 9086h	5000 A086h	5004 A086h
8Eh	16	EPWM_AQSFRC	500C 908Eh	5000 A08Eh	5004 A08Eh
92h	16	EPWM_AQCSFRC	500C 9092h	5000 A092h	5004 A092h
A0h	16	EPWM_DBREDHR	500C 90A0h	5000 A0A0h	5004 A0A0h
A2h	16	EPWM_DBRED	500C 90A2h	5000 A0A2h	5004 A0A2h
A4h	16	EPWM_DBFEDHR	500C 90A4h	5000 A0A4h	5004 A0A4h
A6h	16	EPWM_DBFED	500C 90A6h	5000 A0A6h	5004 A0A6h
C0h	32	EPWM_TBPHS	500C 90C0h	5000 A0C0h	5004 A0C0h
C4h	16	EPWM_TBPRDHR	500C 90C4h	5000 A0C4h	5004 A0C4h
C6h	16	EPWM_TBPRD	500C 90C6h	5000 A0C6h	5004 A0C6h
C8h	16	EPWM_TBPRDHRB	500C 90C8h	5000 A0C8h	5004 A0C8h
D4h	32	EPWM_CMPA	500C 90D4h	5000 A0D4h	5004 A0D4h
D8h	32	EPWM_CMPB	500C 90D8h	5000 A0D8h	5004 A0D8h
DEh	16	EPWM_CMPC	500C 90DEh	5000 A0DEh	5004 A0DEh
E2h	16	EPWM_CMPD	500C 90E2h	5000 A0E2h	5004 A0E2h
E8h	16	EPWM_GLDCTL2	500C 90E8h	5000 A0E8h	5004 A0E8h
EEh	16	EPWM_SWVDELVAL	500C 90EEh	5000 A0EEh	5004 A0EEh
100h	16	EPWM_TZSEL	500C 9100h	5000 A100h	5004 A100h
102h	16	EPWM_TZSEL2	500C 9102h	5000 A102h	5004 A102h
104h	16	EPWM_TZDCSEL	500C 9104h	5000 A104h	5004 A104h
108h	16	EPWM_TZCTL	500C 9108h	5000 A108h	5004 A108h
10Ah	16	EPWM_TZCTL2	500C 910Ah	5000 A10Ah	5004 A10Ah
10Ch	16	EPWM_TZCTLDCA	500C 910Ch	5000 A10Ch	5004 A10Ch
10Eh	16	EPWM_TZCTLDCB	500C 910Eh	5000 A10Eh	5004 A10Eh
11Ah	16	EPWM_TZEINT	500C 911Ah	5000 A11Ah	5004 A11Ah
126h	16	EPWM_TZFLG	500C 9126h	5000 A126h	5004 A126h
128h	16	EPWM_TZCBCFLG	500C 9128h	5000 A128h	5004 A128h

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Table 3-583. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM07_G1 Physical Address	EPWM08_G1 Physical Address	EPWM09_G1 Physical Address
12Ah	16	EPWM_TZOSTFLG	500C 912Ah	5000 A12Ah	5004 A12Ah
12Eh	16	EPWM_TZCLR	500C 912Eh	5000 A12Eh	5004 A12Eh
130h	16	EPWM_TZCBCCLR	500C 9130h	5000 A130h	5004 A130h
132h	16	EPWM_TZOSTCLR	500C 9132h	5000 A132h	5004 A132h
136h	16	EPWM_TZFRC	500C 9136h	5000 A136h	5004 A136h
13Ah	16	EPWM_TZTRIPOUTSEL	500C 913Ah	5000 A13Ah	5004 A13Ah
148h	16	EPWM_ETSEL	500C 9148h	5000 A148h	5004 A148h
14Ch	16	EPWM_ETPS	500C 914Ch	5000 A14Ch	5004 A14Ch
150h	16	EPWM_ETFLG	500C 9150h	5000 A150h	5004 A150h
154h	16	EPWM_ETCLR	500C 9154h	5000 A154h	5004 A154h
158h	16	EPWM_ETFRC	500C 9158h	5000 A158h	5004 A158h
15Ch	16	EPWM_ETINTPS	500C 915Ch	5000 A15Ch	5004 A15Ch
160h	16	EPWM_ETSOCPS	500C 9160h	5000 A160h	5004 A160h
164h	16	EPWM_ETCNTINITCTL	500C 9164h	5000 A164h	5004 A164h
168h	16	EPWM_ETCNTINIT	500C 9168h	5000 A168h	5004 A168h
16Ch	16	EPWM_ETINTMIXEN	500C 916Ch	5000 A16Ch	5004 A16Ch
170h	16	EPWM_ETSOCAMIXEN	500C 9170h	5000 A170h	5004 A170h
174h	16	EPWM_ETSOCBMIXEN	500C 9174h	5000 A174h	5004 A174h
180h	16	EPWM_DCTRIPSEL	500C 9180h	5000 A180h	5004 A180h
186h	16	EPWM_DCACTL	500C 9186h	5000 A186h	5004 A186h
188h	16	EPWM_DCBCTL	500C 9188h	5000 A188h	5004 A188h
18Eh	16	EPWM_DCFCTL	500C 918Eh	5000 A18Eh	5004 A18Eh
190h	16	EPWM_DCCAPCTL	500C 9190h	5000 A190h	5004 A190h
192h	16	EPWM_DCFOFFSET	500C 9192h	5000 A192h	5004 A192h
194h	16	EPWM_DCFOFFSETCNT	500C 9194h	5000 A194h	5004 A194h
196h	16	EPWM_DCFWINDOW	500C 9196h	5000 A196h	5004 A196h
198h	16	EPWM_DCFWINDOWCNT	500C 9198h	5000 A198h	5004 A198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500C 919Ah	5000 A19Ah	5004 A19Ah
19Ch	16	EPWM_DCCAPMIXSEL	500C 919Ch	5000 A19Ch	5004 A19Ch
19Eh	16	EPWM_DCCAP	500C 919Eh	5000 A19Eh	5004 A19Eh
1A4h	16	EPWM_DCAHTRIPSEL	500C 91A4h	5000 A1A4h	5004 A1A4h
1A6h	16	EPWM_DCALTRIPSEL	500C 91A6h	5000 A1A6h	5004 A1A6h
1A8h	16	EPWM_DCBHTRIPSEL	500C 91A8h	5000 A1A8h	5004 A1A8h
1AAh	16	EPWM_DCBLTRIPSEL	500C 91AAh	5000 A1AAh	5004 A1AAh
1ACh	16	EPWM_CAPCTL	500C 91ACh	5000 A1ACh	5004 A1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500C 91AEh	5000 A1AEh	5004 A1AEh
1B0h	16	EPWM_CAPINTRIPSEL	500C 91B0h	5000 A1B0h	5004 A1B0h
1B2h	16	EPWM_CAPTRIPSEL	500C 91B2h	5000 A1B2h	5004 A1B2h
1F4h	32	EPWM_EPWMLOCK	500C 91F4h	5000 A1F4h	5004 A1F4h
1FAh	16	EPWM_HWVDELVAL	500C 91FAh	5000 A1FAh	5004 A1FAh
1FCh	16	EPWM_VCNTVAL	500C 91FCh	5000 A1FCh	5004 A1FCh
400h	32	EPWM_XCMPCTL1	500C 9400h	5000 A400h	5004 A400h
410h	32	EPWM_XLOADCTL	500C 9410h	5000 A410h	5004 A410h
418h	32	EPWM_XLOAD	500C 9418h	5000 A418h	5004 A418h
41Ch	32	EPWM_EPWMXLINKXLOAD	500C 941Ch	5000 A41Ch	5004 A41Ch
420h	32	EPWM_XREGSHDW1STS	500C 9420h	5000 A420h	5004 A420h

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Table 3-583. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM07_G1 Physical Address	EPWM08_G1 Physical Address	EPWM09_G1 Physical Address
428h	32	EPWM_XREGSHDW2STS	500C 9428h	5000 A428h	5004 A428h
430h	32	EPWM_XREGSHDW3STS	500C 9430h	5000 A430h	5004 A430h
600h	32	EPWM_XCMP1_ACTIVE	500C 9600h	5000 A600h	5004 A600h
604h	32	EPWM_XCMP2_ACTIVE	500C 9604h	5000 A604h	5004 A604h
608h	32	EPWM_XCMP3_ACTIVE	500C 9608h	5000 A608h	5004 A608h
60Ch	32	EPWM_XCMP4_ACTIVE	500C 960Ch	5000 A60Ch	5004 A60Ch
610h	32	EPWM_XCMP5_ACTIVE	500C 9610h	5000 A610h	5004 A610h
614h	32	EPWM_XCMP6_ACTIVE	500C 9614h	5000 A614h	5004 A614h
618h	32	EPWM_XCMP7_ACTIVE	500C 9618h	5000 A618h	5004 A618h
61Ch	32	EPWM_XCMP8_ACTIVE	500C 961Ch	5000 A61Ch	5004 A61Ch
620h	32	EPWM_XTBPRD_ACTIVE	500C 9620h	5000 A620h	5004 A620h
630h	16	EPWM_XAQCTLA_ACTIVE	500C 9630h	5000 A630h	5004 A630h
644h	32	EPWM_XMINMAX_ACTIVE	500C 9644h	5000 A644h	5004 A644h
680h	32	EPWM_XCMP1_SHDW1	500C 9680h	5000 A680h	5004 A680h
684h	32	EPWM_XCMP2_SHDW1	500C 9684h	5000 A684h	5004 A684h
688h	32	EPWM_XCMP3_SHDW1	500C 9688h	5000 A688h	5004 A688h
68Ch	32	EPWM_XCMP4_SHDW1	500C 968Ch	5000 A68Ch	5004 A68Ch
690h	32	EPWM_XCMP5_SHDW1	500C 9690h	5000 A690h	5004 A690h
694h	32	EPWM_XCMP6_SHDW1	500C 9694h	5000 A694h	5004 A694h
698h	32	EPWM_XCMP7_SHDW1	500C 9698h	5000 A698h	5004 A698h
69Ch	32	EPWM_XCMP8_SHDW1	500C 969Ch	5000 A69Ch	5004 A69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500C 96A0h	5000 A6A0h	5004 A6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500C 96B0h	5000 A6B0h	5004 A6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500C 96B2h	5000 A6B2h	5004 A6B2h
6BAh	16	EPWM_CMPC_SHDW1	500C 96BAh	5000 A6BAh	5004 A6BAh
6BEh	16	EPWM_CMPD_SHDW1	500C 96BEh	5000 A6BEh	5004 A6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500C 96C4h	5000 A6C4h	5004 A6C4h
700h	32	EPWM_XCMP1_SHDW2	500C 9700h	5000 A700h	5004 A700h
704h	32	EPWM_XCMP2_SHDW2	500C 9704h	5000 A704h	5004 A704h
708h	32	EPWM_XCMP3_SHDW2	500C 9708h	5000 A708h	5004 A708h
70Ch	32	EPWM_XCMP4_SHDW2	500C 970Ch	5000 A70Ch	5004 A70Ch
710h	32	EPWM_XCMP5_SHDW2	500C 9710h	5000 A710h	5004 A710h
714h	32	EPWM_XCMP6_SHDW2	500C 9714h	5000 A714h	5004 A714h
718h	32	EPWM_XCMP7_SHDW2	500C 9718h	5000 A718h	5004 A718h
71Ch	32	EPWM_XCMP8_SHDW2	500C 971Ch	5000 A71Ch	5004 A71Ch
720h	32	EPWM_XTBPRD_SHDW2	500C 9720h	5000 A720h	5004 A720h
730h	16	EPWM_XAQCTLA_SHDW2	500C 9730h	5000 A730h	5004 A730h
732h	16	EPWM_XAQCTLB_SHDW2	500C 9732h	5000 A732h	5004 A732h
73Ah	16	EPWM_CMPC_SHDW2	500C 973Ah	5000 A73Ah	5004 A73Ah
73Eh	16	EPWM_CMPD_SHDW2	500C 973Eh	5000 A73Eh	5004 A73Eh
744h	32	EPWM_XMINMAX_SHDW2	500C 9744h	5000 A744h	5004 A744h
780h	32	EPWM_XCMP1_SHDW3	500C 9780h	5000 A780h	5004 A780h
784h	32	EPWM_XCMP2_SHDW3	500C 9784h	5000 A784h	5004 A784h
788h	32	EPWM_XCMP3_SHDW3	500C 9788h	5000 A788h	5004 A788h
78Ch	32	EPWM_XCMP4_SHDW3	500C 978Ch	5000 A78Ch	5004 A78Ch
790h	32	EPWM_XCMP5_SHDW3	500C 9790h	5000 A790h	5004 A790h

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Table 3-583. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM07_G1 Physical Address	EPWM08_G1 Physical Address	EPWM09_G1 Physical Address
794h	32	EPWM_XCMP6_SHDW3	500C 9794h	5000 A794h	5004 A794h
798h	32	EPWM_XCMP7_SHDW3	500C 9798h	5000 A798h	5004 A798h
79Ch	32	EPWM_XCMP8_SHDW3	500C 979Ch	5000 A79Ch	5004 A79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500C 97A0h	5000 A7A0h	5004 A7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500C 97B0h	5000 A7B0h	5004 A7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500C 97B2h	5000 A7B2h	5004 A7B2h
7BAh	16	EPWM_CMPC_SHDW3	500C 97BAh	5000 A7BAh	5004 A7BAh
7BEh	16	EPWM_CMPD_SHDW3	500C 97BEh	5000 A7BEh	5004 A7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500C 97C4h	5000 A7C4h	5004 A7C4h
800h	32	EPWM_DECTL	500C 9800h	5000 A800h	5004 A800h
804h	32	EPWM_DECOMPSEL	500C 9804h	5000 A804h	5004 A804h
808h	32	EPWM_DEACTCTL	500C 9808h	5000 A808h	5004 A808h
80Ch	32	EPWM_DESTS	500C 980Ch	5000 A80Ch	5004 A80Ch
810h	32	EPWM_DEFRC	500C 9810h	5000 A810h	5004 A810h
814h	32	EPWM_DECLR	500C 9814h	5000 A814h	5004 A814h
820h	32	EPWM_DEMONCNT	500C 9820h	5000 A820h	5004 A820h
824h	32	EPWM_DEMONCTL	500C 9824h	5000 A824h	5004 A824h
828h	32	EPWM_DEMONSTEP	500C 9828h	5000 A828h	5004 A828h
82Ch	32	EPWM_DEMONTHRES	500C 982Ch	5000 A82Ch	5004 A82Ch
C00h	32	EPWM_MINDBCFG	500C 9C00h	5000 AC00h	5004 AC00h
C04h	32	EPWM_MINDBDLY	500C 9C04h	5000 AC04h	5004 AC04h
C20h	32	EPWM_LUTCTLA	500C 9C20h	5000 AC20h	5004 AC20h
C24h	32	EPWM_LUTCTLB	500C 9C24h	5000 AC24h	5004 AC24h

Table 3-584. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM10_G1 Physical Address	EPWM11_G1 Physical Address	EPWM12_G1 Physical Address
0h	16	EPWM_TBCTL	5008 A000h	500C A000h	5000 B000h
2h	16	EPWM_TBCTL2	5008 A002h	500C A002h	5000 B002h
6h	16	EPWM_EPWMSYNCINSEL	5008 A006h	500C A006h	5000 B006h
8h	16	EPWM_TBCTR	5008 A008h	500C A008h	5000 B008h
Ah	16	EPWM_TBSTS	5008 A00Ah	500C A00Ah	5000 B00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5008 A00Ch	500C A00Ch	5000 B00Ch
Eh	16	EPWM_TBCTL3	5008 A00Eh	500C A00Eh	5000 B00Eh
10h	16	EPWM_CMPCTL	5008 A010h	500C A010h	5000 B010h
12h	16	EPWM_CMPCTL2	5008 A012h	500C A012h	5000 B012h
18h	16	EPWM_DBCTL	5008 A018h	500C A018h	5000 B018h
1Ah	16	EPWM_DBCTL2	5008 A01Ah	500C A01Ah	5000 B01Ah
20h	16	EPWM_AQCTL	5008 A020h	500C A020h	5000 B020h
22h	16	EPWM_AQTSRCSEL	5008 A022h	500C A022h	5000 B022h
28h	16	EPWM_PCCTL	5008 A028h	500C A028h	5000 B028h
30h	16	EPWM_VCAPCTL	5008 A030h	500C A030h	5000 B030h
32h	16	EPWM_VCNTCFG	5008 A032h	500C A032h	5000 B032h
40h	16	EPWM_HRCNFG	5008 A040h	500C A040h	5000 B040h
4Eh	16	EPWM_HRCNFG2	5008 A04Eh	500C A04Eh	5000 B04Eh
5Ah	16	EPWM_HRPCTL	5008 A05Ah	500C A05Ah	5000 B05Ah

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Table 3-584. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM10_G1 Physical Address	EPWM11_G1 Physical Address	EPWM12_G1 Physical Address
5Ch	16	EPWM_TRREM	5008 A05Ch	500C A05Ch	5000 B05Ch
68h	16	EPWM_GLDCTL	5008 A068h	500C A068h	5000 B068h
6Ah	16	EPWM_GLDCFG	5008 A06Ah	500C A06Ah	5000 B06Ah
70h	32	EPWM_EPWMXLINK	5008 A070h	500C A070h	5000 B070h
74h	32	EPWM_EPWMXLINK2	5008 A074h	500C A074h	5000 B074h
7Ah	16	EPWM_ETEST	5008 A07Ah	500C A07Ah	5000 B07Ah
7Ch	16	EPWM_EPWMREV	5008 A07Ch	500C A07Ch	5000 B07Ch
7Eh	16	EPWM_HRPWMREV	5008 A07Eh	500C A07Eh	5000 B07Eh
80h	16	EPWM_AQCTLA	5008 A080h	500C A080h	5000 B080h
82h	16	EPWM_AQCTLA2	5008 A082h	500C A082h	5000 B082h
84h	16	EPWM_AQCTLB	5008 A084h	500C A084h	5000 B084h
86h	16	EPWM_AQCTLB2	5008 A086h	500C A086h	5000 B086h
8Eh	16	EPWM_AQSFRC	5008 A08Eh	500C A08Eh	5000 B08Eh
92h	16	EPWM_AQCSFRC	5008 A092h	500C A092h	5000 B092h
A0h	16	EPWM_DBREDHR	5008 A0A0h	500C A0A0h	5000 B0A0h
A2h	16	EPWM_DBRED	5008 A0A2h	500C A0A2h	5000 B0A2h
A4h	16	EPWM_DBFEDHR	5008 A0A4h	500C A0A4h	5000 B0A4h
A6h	16	EPWM_DBFED	5008 A0A6h	500C A0A6h	5000 B0A6h
C0h	32	EPWM_TBPHS	5008 A0C0h	500C A0C0h	5000 B0C0h
C4h	16	EPWM_TBPRDHR	5008 A0C4h	500C A0C4h	5000 B0C4h
C6h	16	EPWM_TBPRD	5008 A0C6h	500C A0C6h	5000 B0C6h
C8h	16	EPWM_TBPRDHRB	5008 A0C8h	500C A0C8h	5000 B0C8h
D4h	32	EPWM_CMPA	5008 A0D4h	500C A0D4h	5000 B0D4h
D8h	32	EPWM_CMPB	5008 A0D8h	500C A0D8h	5000 B0D8h
DEh	16	EPWM_CMPC	5008 A0DEh	500C A0DEh	5000 B0DEh
E2h	16	EPWM_CMPD	5008 A0E2h	500C A0E2h	5000 B0E2h
E8h	16	EPWM_GLDCTL2	5008 A0E8h	500C A0E8h	5000 B0E8h
EEh	16	EPWM_SWVDELVAL	5008 A0EEh	500C A0EEh	5000 B0EEh
100h	16	EPWM_TZSEL	5008 A100h	500C A100h	5000 B100h
102h	16	EPWM_TZSEL2	5008 A102h	500C A102h	5000 B102h
104h	16	EPWM_TZDCSEL	5008 A104h	500C A104h	5000 B104h
108h	16	EPWM_TZCTL	5008 A108h	500C A108h	5000 B108h
10Ah	16	EPWM_TZCTL2	5008 A10Ah	500C A10Ah	5000 B10Ah
10Ch	16	EPWM_TZCTLDCA	5008 A10Ch	500C A10Ch	5000 B10Ch
10Eh	16	EPWM_TZCTLDCB	5008 A10Eh	500C A10Eh	5000 B10Eh
11Ah	16	EPWM_TZEINT	5008 A11Ah	500C A11Ah	5000 B11Ah
126h	16	EPWM_TZFLG	5008 A126h	500C A126h	5000 B126h
128h	16	EPWM_TZCBCFLG	5008 A128h	500C A128h	5000 B128h
12Ah	16	EPWM_TZOSTFLG	5008 A12Ah	500C A12Ah	5000 B12Ah
12Eh	16	EPWM_TZCLR	5008 A12Eh	500C A12Eh	5000 B12Eh
130h	16	EPWM_TZCBCCLR	5008 A130h	500C A130h	5000 B130h
132h	16	EPWM_TZOSTCLR	5008 A132h	500C A132h	5000 B132h
136h	16	EPWM_TZFRC	5008 A136h	500C A136h	5000 B136h
13Ah	16	EPWM_TZTRIPOUTSEL	5008 A13Ah	500C A13Ah	5000 B13Ah
148h	16	EPWM_ETSEL	5008 A148h	500C A148h	5000 B148h
14Ch	16	EPWM_ETPS	5008 A14Ch	500C A14Ch	5000 B14Ch

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Table 3-584. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM10_G1 Physical Address	EPWM11_G1 Physical Address	EPWM12_G1 Physical Address
150h	16	EPWM_ETFLG	5008 A150h	500C A150h	5000 B150h
154h	16	EPWM_ETCLR	5008 A154h	500C A154h	5000 B154h
158h	16	EPWM_ETFRC	5008 A158h	500C A158h	5000 B158h
15Ch	16	EPWM_ETINTPS	5008 A15Ch	500C A15Ch	5000 B15Ch
160h	16	EPWM_ETSOCPS	5008 A160h	500C A160h	5000 B160h
164h	16	EPWM_ETCNTINITCTL	5008 A164h	500C A164h	5000 B164h
168h	16	EPWM_ETCNTINIT	5008 A168h	500C A168h	5000 B168h
16Ch	16	EPWM_ETINTMIXEN	5008 A16Ch	500C A16Ch	5000 B16Ch
170h	16	EPWM_ETSOCAMIXEN	5008 A170h	500C A170h	5000 B170h
174h	16	EPWM_ETSOCBMIXEN	5008 A174h	500C A174h	5000 B174h
180h	16	EPWM_DCTRIPSEL	5008 A180h	500C A180h	5000 B180h
186h	16	EPWM_DCACTL	5008 A186h	500C A186h	5000 B186h
188h	16	EPWM_DCBCTL	5008 A188h	500C A188h	5000 B188h
18Eh	16	EPWM_DCFCTL	5008 A18Eh	500C A18Eh	5000 B18Eh
190h	16	EPWM_DCCAPCTL	5008 A190h	500C A190h	5000 B190h
192h	16	EPWM_DCFOFFSET	5008 A192h	500C A192h	5000 B192h
194h	16	EPWM_DCFOFFSETCNT	5008 A194h	500C A194h	5000 B194h
196h	16	EPWM_DCFWINDOW	5008 A196h	500C A196h	5000 B196h
198h	16	EPWM_DCFWINDOWCNT	5008 A198h	500C A198h	5000 B198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5008 A19Ah	500C A19Ah	5000 B19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5008 A19Ch	500C A19Ch	5000 B19Ch
19Eh	16	EPWM_DCCAP	5008 A19Eh	500C A19Eh	5000 B19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5008 A1A4h	500C A1A4h	5000 B1A4h
1A6h	16	EPWM_DCALTRIPSEL	5008 A1A6h	500C A1A6h	5000 B1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5008 A1A8h	500C A1A8h	5000 B1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5008 A1AAh	500C A1AAh	5000 B1AAh
1ACh	16	EPWM_CAPCTL	5008 A1ACh	500C A1ACh	5000 B1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5008 A1AEh	500C A1AEh	5000 B1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5008 A1B0h	500C A1B0h	5000 B1B0h
1B2h	16	EPWM_CAPTRIPSEL	5008 A1B2h	500C A1B2h	5000 B1B2h
1F4h	32	EPWM_EPWMLOCK	5008 A1F4h	500C A1F4h	5000 B1F4h
1FAh	16	EPWM_HWVDELVAL	5008 A1FAh	500C A1FAh	5000 B1FAh
1FCh	16	EPWM_VCNTVAL	5008 A1FCh	500C A1FCh	5000 B1FCh
400h	32	EPWM_XCMPCTL1	5008 A400h	500C A400h	5000 B400h
410h	32	EPWM_XLOADCTL	5008 A410h	500C A410h	5000 B410h
418h	32	EPWM_XLOAD	5008 A418h	500C A418h	5000 B418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5008 A41Ch	500C A41Ch	5000 B41Ch
420h	32	EPWM_XREGSHDW1STS	5008 A420h	500C A420h	5000 B420h
428h	32	EPWM_XREGSHDW2STS	5008 A428h	500C A428h	5000 B428h
430h	32	EPWM_XREGSHDW3STS	5008 A430h	500C A430h	5000 B430h
600h	32	EPWM_XCMP1_ACTIVE	5008 A600h	500C A600h	5000 B600h
604h	32	EPWM_XCMP2_ACTIVE	5008 A604h	500C A604h	5000 B604h
608h	32	EPWM_XCMP3_ACTIVE	5008 A608h	500C A608h	5000 B608h
60Ch	32	EPWM_XCMP4_ACTIVE	5008 A60Ch	500C A60Ch	5000 B60Ch
610h	32	EPWM_XCMP5_ACTIVE	5008 A610h	500C A610h	5000 B610h
614h	32	EPWM_XCMP6_ACTIVE	5008 A614h	500C A614h	5000 B614h

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Table 3-584. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM10_G1 Physical Address	EPWM11_G1 Physical Address	EPWM12_G1 Physical Address
618h	32	EPWM_XCMP7_ACTIVE	5008 A618h	500C A618h	5000 B618h
61Ch	32	EPWM_XCMP8_ACTIVE	5008 A61Ch	500C A61Ch	5000 B61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5008 A620h	500C A620h	5000 B620h
630h	16	EPWM_XAQCTLA_ACTIVE	5008 A630h	500C A630h	5000 B630h
644h	32	EPWM_XMINMAX_ACTIVE	5008 A644h	500C A644h	5000 B644h
680h	32	EPWM_XCMP1_SHDW1	5008 A680h	500C A680h	5000 B680h
684h	32	EPWM_XCMP2_SHDW1	5008 A684h	500C A684h	5000 B684h
688h	32	EPWM_XCMP3_SHDW1	5008 A688h	500C A688h	5000 B688h
68Ch	32	EPWM_XCMP4_SHDW1	5008 A68Ch	500C A68Ch	5000 B68Ch
690h	32	EPWM_XCMP5_SHDW1	5008 A690h	500C A690h	5000 B690h
694h	32	EPWM_XCMP6_SHDW1	5008 A694h	500C A694h	5000 B694h
698h	32	EPWM_XCMP7_SHDW1	5008 A698h	500C A698h	5000 B698h
69Ch	32	EPWM_XCMP8_SHDW1	5008 A69Ch	500C A69Ch	5000 B69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5008 A6A0h	500C A6A0h	5000 B6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5008 A6B0h	500C A6B0h	5000 B6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5008 A6B2h	500C A6B2h	5000 B6B2h
6BAh	16	EPWM_CMPC_SHDW1	5008 A6BAh	500C A6BAh	5000 B6BAh
6BEh	16	EPWM_CMPD_SHDW1	5008 A6BEh	500C A6BEh	5000 B6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5008 A6C4h	500C A6C4h	5000 B6C4h
700h	32	EPWM_XCMP1_SHDW2	5008 A700h	500C A700h	5000 B700h
704h	32	EPWM_XCMP2_SHDW2	5008 A704h	500C A704h	5000 B704h
708h	32	EPWM_XCMP3_SHDW2	5008 A708h	500C A708h	5000 B708h
70Ch	32	EPWM_XCMP4_SHDW2	5008 A70Ch	500C A70Ch	5000 B70Ch
710h	32	EPWM_XCMP5_SHDW2	5008 A710h	500C A710h	5000 B710h
714h	32	EPWM_XCMP6_SHDW2	5008 A714h	500C A714h	5000 B714h
718h	32	EPWM_XCMP7_SHDW2	5008 A718h	500C A718h	5000 B718h
71Ch	32	EPWM_XCMP8_SHDW2	5008 A71Ch	500C A71Ch	5000 B71Ch
720h	32	EPWM_XTBPRD_SHDW2	5008 A720h	500C A720h	5000 B720h
730h	16	EPWM_XAQCTLA_SHDW2	5008 A730h	500C A730h	5000 B730h
732h	16	EPWM_XAQCTLB_SHDW2	5008 A732h	500C A732h	5000 B732h
73Ah	16	EPWM_CMPC_SHDW2	5008 A73Ah	500C A73Ah	5000 B73Ah
73Eh	16	EPWM_CMPD_SHDW2	5008 A73Eh	500C A73Eh	5000 B73Eh
744h	32	EPWM_XMINMAX_SHDW2	5008 A744h	500C A744h	5000 B744h
780h	32	EPWM_XCMP1_SHDW3	5008 A780h	500C A780h	5000 B780h
784h	32	EPWM_XCMP2_SHDW3	5008 A784h	500C A784h	5000 B784h
788h	32	EPWM_XCMP3_SHDW3	5008 A788h	500C A788h	5000 B788h
78Ch	32	EPWM_XCMP4_SHDW3	5008 A78Ch	500C A78Ch	5000 B78Ch
790h	32	EPWM_XCMP5_SHDW3	5008 A790h	500C A790h	5000 B790h
794h	32	EPWM_XCMP6_SHDW3	5008 A794h	500C A794h	5000 B794h
798h	32	EPWM_XCMP7_SHDW3	5008 A798h	500C A798h	5000 B798h
79Ch	32	EPWM_XCMP8_SHDW3	5008 A79Ch	500C A79Ch	5000 B79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5008 A7A0h	500C A7A0h	5000 B7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5008 A7B0h	500C A7B0h	5000 B7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5008 A7B2h	500C A7B2h	5000 B7B2h
7BAh	16	EPWM_CMPC_SHDW3	5008 A7BAh	500C A7BAh	5000 B7BAh
7BEh	16	EPWM_CMPD_SHDW3	5008 A7BEh	500C A7BEh	5000 B7BEh

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Table 3-584. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM10_G1 Physical Address	EPWM11_G1 Physical Address	EPWM12_G1 Physical Address
7C4h	32	EPWM_XMINMAX_SHDW3	5008 A7C4h	500C A7C4h	5000 B7C4h
800h	32	EPWM_DECTL	5008 A800h	500C A800h	5000 B800h
804h	32	EPWM_DECOMPSEL	5008 A804h	500C A804h	5000 B804h
808h	32	EPWM_DEACTCTL	5008 A808h	500C A808h	5000 B808h
80Ch	32	EPWM_DESTS	5008 A80Ch	500C A80Ch	5000 B80Ch
810h	32	EPWM_DEFRC	5008 A810h	500C A810h	5000 B810h
814h	32	EPWM_DECLR	5008 A814h	500C A814h	5000 B814h
820h	32	EPWM_DEMONCNT	5008 A820h	500C A820h	5000 B820h
824h	32	EPWM_DEMONCTL	5008 A824h	500C A824h	5000 B824h
828h	32	EPWM_DEMONSTEP	5008 A828h	500C A828h	5000 B828h
82Ch	32	EPWM_DEMONTHRES	5008 A82Ch	500C A82Ch	5000 B82Ch
C00h	32	EPWM_MINDBCFG	5008 AC00h	500C AC00h	5000 BC00h
C04h	32	EPWM_MINDBDLY	5008 AC04h	500C AC04h	5000 BC04h
C20h	32	EPWM_LUTCTLA	5008 AC20h	500C AC20h	5000 BC20h
C24h	32	EPWM_LUTCTLB	5008 AC24h	500C AC24h	5000 BC24h

Table 3-585. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM13_G1 Physical Address	EPWM14_G1 Physical Address	EPWM15_G1 Physical Address
0h	16	EPWM_TBCTL	5004 B000h	5008 B000h	500C B000h
2h	16	EPWM_TBCTL2	5004 B002h	5008 B002h	500C B002h
6h	16	EPWM_EPWMSYNCINSEL	5004 B006h	5008 B006h	500C B006h
8h	16	EPWM_TBCTR	5004 B008h	5008 B008h	500C B008h
Ah	16	EPWM_TBSTS	5004 B00Ah	5008 B00Ah	500C B00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5004 B00Ch	5008 B00Ch	500C B00Ch
Eh	16	EPWM_TBCTL3	5004 B00Eh	5008 B00Eh	500C B00Eh
10h	16	EPWM_CMPCTL	5004 B010h	5008 B010h	500C B010h
12h	16	EPWM_CMPCTL2	5004 B012h	5008 B012h	500C B012h
18h	16	EPWM_DBCTL	5004 B018h	5008 B018h	500C B018h
1Ah	16	EPWM_DBCTL2	5004 B01Ah	5008 B01Ah	500C B01Ah
20h	16	EPWM_AQCTL	5004 B020h	5008 B020h	500C B020h
22h	16	EPWM_AQTSRCSEL	5004 B022h	5008 B022h	500C B022h
28h	16	EPWM_PCCTL	5004 B028h	5008 B028h	500C B028h
30h	16	EPWM_VCAPCTL	5004 B030h	5008 B030h	500C B030h
32h	16	EPWM_VCNTCFG	5004 B032h	5008 B032h	500C B032h
40h	16	EPWM_HRCNFG	5004 B040h	5008 B040h	500C B040h
4Eh	16	EPWM_HRCNFG2	5004 B04Eh	5008 B04Eh	500C B04Eh
5Ah	16	EPWM_HRPCTL	5004 B05Ah	5008 B05Ah	500C B05Ah
5Ch	16	EPWM_TRREM	5004 B05Ch	5008 B05Ch	500C B05Ch
68h	16	EPWM_GLDCTL	5004 B068h	5008 B068h	500C B068h
6Ah	16	EPWM_GLDCFG	5004 B06Ah	5008 B06Ah	500C B06Ah
70h	32	EPWM_EPWMXLINK	5004 B070h	5008 B070h	500C B070h
74h	32	EPWM_EPWMXLINK2	5004 B074h	5008 B074h	500C B074h
7Ah	16	EPWM_ETEST	5004 B07Ah	5008 B07Ah	500C B07Ah
7Ch	16	EPWM_EPWMREV	5004 B07Ch	5008 B07Ch	500C B07Ch
7Eh	16	EPWM_HRPWMREV	5004 B07Eh	5008 B07Eh	500C B07Eh

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Table 3-585. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM13_G1 Physical Address	EPWM14_G1 Physical Address	EPWM15_G1 Physical Address
80h	16	EPWM_AQCTLA	5004 B080h	5008 B080h	500C B080h
82h	16	EPWM_AQCTLA2	5004 B082h	5008 B082h	500C B082h
84h	16	EPWM_AQCTLB	5004 B084h	5008 B084h	500C B084h
86h	16	EPWM_AQCTLB2	5004 B086h	5008 B086h	500C B086h
8Eh	16	EPWM_AQSFRC	5004 B08Eh	5008 B08Eh	500C B08Eh
92h	16	EPWM_AQCSFRC	5004 B092h	5008 B092h	500C B092h
A0h	16	EPWM_DBREDHR	5004 B0A0h	5008 B0A0h	500C B0A0h
A2h	16	EPWM_DBRED	5004 B0A2h	5008 B0A2h	500C B0A2h
A4h	16	EPWM_DBFEDHR	5004 B0A4h	5008 B0A4h	500C B0A4h
A6h	16	EPWM_DBFED	5004 B0A6h	5008 B0A6h	500C B0A6h
C0h	32	EPWM_TBPHS	5004 B0C0h	5008 B0C0h	500C B0C0h
C4h	16	EPWM_TBPRDHR	5004 B0C4h	5008 B0C4h	500C B0C4h
C6h	16	EPWM_TBPRD	5004 B0C6h	5008 B0C6h	500C B0C6h
C8h	16	EPWM_TBPRDHRB	5004 B0C8h	5008 B0C8h	500C B0C8h
D4h	32	EPWM_CMPA	5004 B0D4h	5008 B0D4h	500C B0D4h
D8h	32	EPWM_CMPB	5004 B0D8h	5008 B0D8h	500C B0D8h
DEh	16	EPWM_CMPC	5004 B0DEh	5008 B0DEh	500C B0DEh
E2h	16	EPWM_CMPD	5004 B0E2h	5008 B0E2h	500C B0E2h
E8h	16	EPWM_GLDCTL2	5004 B0E8h	5008 B0E8h	500C B0E8h
EEh	16	EPWM_SWVDELVAL	5004 B0EEh	5008 B0EEh	500C B0EEh
100h	16	EPWM_TZSEL	5004 B100h	5008 B100h	500C B100h
102h	16	EPWM_TZSEL2	5004 B102h	5008 B102h	500C B102h
104h	16	EPWM_TZDCSEL	5004 B104h	5008 B104h	500C B104h
108h	16	EPWM_TZCTL	5004 B108h	5008 B108h	500C B108h
10Ah	16	EPWM_TZCTL2	5004 B10Ah	5008 B10Ah	500C B10Ah
10Ch	16	EPWM_TZCTLDCA	5004 B10Ch	5008 B10Ch	500C B10Ch
10Eh	16	EPWM_TZCTLDCB	5004 B10Eh	5008 B10Eh	500C B10Eh
11Ah	16	EPWM_TZEINT	5004 B11Ah	5008 B11Ah	500C B11Ah
126h	16	EPWM_TZFLG	5004 B126h	5008 B126h	500C B126h
128h	16	EPWM_TZCBCFLG	5004 B128h	5008 B128h	500C B128h
12Ah	16	EPWM_TZOSTFLG	5004 B12Ah	5008 B12Ah	500C B12Ah
12Eh	16	EPWM_TZCLR	5004 B12Eh	5008 B12Eh	500C B12Eh
130h	16	EPWM_TZCBCCLR	5004 B130h	5008 B130h	500C B130h
132h	16	EPWM_TZOSTCLR	5004 B132h	5008 B132h	500C B132h
136h	16	EPWM_TZFRC	5004 B136h	5008 B136h	500C B136h
13Ah	16	EPWM_TZTRIPOUTSEL	5004 B13Ah	5008 B13Ah	500C B13Ah
148h	16	EPWM_ETSEL	5004 B148h	5008 B148h	500C B148h
14Ch	16	EPWM_ETPS	5004 B14Ch	5008 B14Ch	500C B14Ch
150h	16	EPWM_ETFLG	5004 B150h	5008 B150h	500C B150h
154h	16	EPWM_ETCLR	5004 B154h	5008 B154h	500C B154h
158h	16	EPWM_ETFRC	5004 B158h	5008 B158h	500C B158h
15Ch	16	EPWM_ETINTPS	5004 B15Ch	5008 B15Ch	500C B15Ch
160h	16	EPWM_ETSOCPS	5004 B160h	5008 B160h	500C B160h
164h	16	EPWM_ETCNTINITCTL	5004 B164h	5008 B164h	500C B164h
168h	16	EPWM_ETCNTINIT	5004 B168h	5008 B168h	500C B168h
16Ch	16	EPWM_ETINTMIXEN	5004 B16Ch	5008 B16Ch	500C B16Ch

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Table 3-585. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM13_G1 Physical Address	EPWM14_G1 Physical Address	EPWM15_G1 Physical Address
170h	16	EPWM_ETSOCAMIXEN	5004 B170h	5008 B170h	500C B170h
174h	16	EPWM_ETSOCBMIXEN	5004 B174h	5008 B174h	500C B174h
180h	16	EPWM_DCTRIPSEL	5004 B180h	5008 B180h	500C B180h
186h	16	EPWM_DCACTL	5004 B186h	5008 B186h	500C B186h
188h	16	EPWM_DCBCTL	5004 B188h	5008 B188h	500C B188h
18Eh	16	EPWM_DCFCTL	5004 B18Eh	5008 B18Eh	500C B18Eh
190h	16	EPWM_DCCAPCTL	5004 B190h	5008 B190h	500C B190h
192h	16	EPWM_DCFOFFSET	5004 B192h	5008 B192h	500C B192h
194h	16	EPWM_DCFOFFSETCNT	5004 B194h	5008 B194h	500C B194h
196h	16	EPWM_DCFWINDOW	5004 B196h	5008 B196h	500C B196h
198h	16	EPWM_DCFWINDOWCNT	5004 B198h	5008 B198h	500C B198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5004 B19Ah	5008 B19Ah	500C B19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5004 B19Ch	5008 B19Ch	500C B19Ch
19Eh	16	EPWM_DCCAP	5004 B19Eh	5008 B19Eh	500C B19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5004 B1A4h	5008 B1A4h	500C B1A4h
1A6h	16	EPWM_DCALTRIPSEL	5004 B1A6h	5008 B1A6h	500C B1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5004 B1A8h	5008 B1A8h	500C B1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5004 B1AAh	5008 B1AAh	500C B1AAh
1ACh	16	EPWM_CAPCTL	5004 B1ACh	5008 B1ACh	500C B1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5004 B1AEh	5008 B1AEh	500C B1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5004 B1B0h	5008 B1B0h	500C B1B0h
1B2h	16	EPWM_CAPTRIPSEL	5004 B1B2h	5008 B1B2h	500C B1B2h
1F4h	32	EPWM_EPWMLOCK	5004 B1F4h	5008 B1F4h	500C B1F4h
1FAh	16	EPWM_HWVDELVAL	5004 B1FAh	5008 B1FAh	500C B1FAh
1FCh	16	EPWM_VCNTVAL	5004 B1FCh	5008 B1FCh	500C B1FCh
400h	32	EPWM_XCMPCTL1	5004 B400h	5008 B400h	500C B400h
410h	32	EPWM_XLOADCTL	5004 B410h	5008 B410h	500C B410h
418h	32	EPWM_XLOAD	5004 B418h	5008 B418h	500C B418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5004 B41Ch	5008 B41Ch	500C B41Ch
420h	32	EPWM_XREGSHDW1STS	5004 B420h	5008 B420h	500C B420h
428h	32	EPWM_XREGSHDW2STS	5004 B428h	5008 B428h	500C B428h
430h	32	EPWM_XREGSHDW3STS	5004 B430h	5008 B430h	500C B430h
600h	32	EPWM_XCMP1_ACTIVE	5004 B600h	5008 B600h	500C B600h
604h	32	EPWM_XCMP2_ACTIVE	5004 B604h	5008 B604h	500C B604h
608h	32	EPWM_XCMP3_ACTIVE	5004 B608h	5008 B608h	500C B608h
60Ch	32	EPWM_XCMP4_ACTIVE	5004 B60Ch	5008 B60Ch	500C B60Ch
610h	32	EPWM_XCMP5_ACTIVE	5004 B610h	5008 B610h	500C B610h
614h	32	EPWM_XCMP6_ACTIVE	5004 B614h	5008 B614h	500C B614h
618h	32	EPWM_XCMP7_ACTIVE	5004 B618h	5008 B618h	500C B618h
61Ch	32	EPWM_XCMP8_ACTIVE	5004 B61Ch	5008 B61Ch	500C B61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5004 B620h	5008 B620h	500C B620h
630h	16	EPWM_XAQCTLA_ACTIVE	5004 B630h	5008 B630h	500C B630h
644h	32	EPWM_XMINMAX_ACTIVE	5004 B644h	5008 B644h	500C B644h
680h	32	EPWM_XCMP1_SHDW1	5004 B680h	5008 B680h	500C B680h
684h	32	EPWM_XCMP2_SHDW1	5004 B684h	5008 B684h	500C B684h
688h	32	EPWM_XCMP3_SHDW1	5004 B688h	5008 B688h	500C B688h

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Table 3-585. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM13_G1 Physical Address	EPWM14_G1 Physical Address	EPWM15_G1 Physical Address
68Ch	32	EPWM_XCMP4_SHDW1	5004 B68Ch	5008 B68Ch	500C B68Ch
690h	32	EPWM_XCMP5_SHDW1	5004 B690h	5008 B690h	500C B690h
694h	32	EPWM_XCMP6_SHDW1	5004 B694h	5008 B694h	500C B694h
698h	32	EPWM_XCMP7_SHDW1	5004 B698h	5008 B698h	500C B698h
69Ch	32	EPWM_XCMP8_SHDW1	5004 B69Ch	5008 B69Ch	500C B69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5004 B6A0h	5008 B6A0h	500C B6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5004 B6B0h	5008 B6B0h	500C B6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5004 B6B2h	5008 B6B2h	500C B6B2h
6BAh	16	EPWM_CMPC_SHDW1	5004 B6BAh	5008 B6BAh	500C B6BAh
6BEh	16	EPWM_CMPD_SHDW1	5004 B6BEh	5008 B6BEh	500C B6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5004 B6C4h	5008 B6C4h	500C B6C4h
700h	32	EPWM_XCMP1_SHDW2	5004 B700h	5008 B700h	500C B700h
704h	32	EPWM_XCMP2_SHDW2	5004 B704h	5008 B704h	500C B704h
708h	32	EPWM_XCMP3_SHDW2	5004 B708h	5008 B708h	500C B708h
70Ch	32	EPWM_XCMP4_SHDW2	5004 B70Ch	5008 B70Ch	500C B70Ch
710h	32	EPWM_XCMP5_SHDW2	5004 B710h	5008 B710h	500C B710h
714h	32	EPWM_XCMP6_SHDW2	5004 B714h	5008 B714h	500C B714h
718h	32	EPWM_XCMP7_SHDW2	5004 B718h	5008 B718h	500C B718h
71Ch	32	EPWM_XCMP8_SHDW2	5004 B71Ch	5008 B71Ch	500C B71Ch
720h	32	EPWM_XTBPRD_SHDW2	5004 B720h	5008 B720h	500C B720h
730h	16	EPWM_XAQCTLA_SHDW2	5004 B730h	5008 B730h	500C B730h
732h	16	EPWM_XAQCTLB_SHDW2	5004 B732h	5008 B732h	500C B732h
73Ah	16	EPWM_CMPC_SHDW2	5004 B73Ah	5008 B73Ah	500C B73Ah
73Eh	16	EPWM_CMPD_SHDW2	5004 B73Eh	5008 B73Eh	500C B73Eh
744h	32	EPWM_XMINMAX_SHDW2	5004 B744h	5008 B744h	500C B744h
780h	32	EPWM_XCMP1_SHDW3	5004 B780h	5008 B780h	500C B780h
784h	32	EPWM_XCMP2_SHDW3	5004 B784h	5008 B784h	500C B784h
788h	32	EPWM_XCMP3_SHDW3	5004 B788h	5008 B788h	500C B788h
78Ch	32	EPWM_XCMP4_SHDW3	5004 B78Ch	5008 B78Ch	500C B78Ch
790h	32	EPWM_XCMP5_SHDW3	5004 B790h	5008 B790h	500C B790h
794h	32	EPWM_XCMP6_SHDW3	5004 B794h	5008 B794h	500C B794h
798h	32	EPWM_XCMP7_SHDW3	5004 B798h	5008 B798h	500C B798h
79Ch	32	EPWM_XCMP8_SHDW3	5004 B79Ch	5008 B79Ch	500C B79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5004 B7A0h	5008 B7A0h	500C B7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5004 B7B0h	5008 B7B0h	500C B7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5004 B7B2h	5008 B7B2h	500C B7B2h
7BAh	16	EPWM_CMPC_SHDW3	5004 B7BAh	5008 B7BAh	500C B7BAh
7BEh	16	EPWM_CMPD_SHDW3	5004 B7BEh	5008 B7BEh	500C B7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5004 B7C4h	5008 B7C4h	500C B7C4h
800h	32	EPWM_DECTL	5004 B800h	5008 B800h	500C B800h
804h	32	EPWM_DECOMPSEL	5004 B804h	5008 B804h	500C B804h
808h	32	EPWM_DEACTCTL	5004 B808h	5008 B808h	500C B808h
80Ch	32	EPWM_DESTS	5004 B80Ch	5008 B80Ch	500C B80Ch
810h	32	EPWM_DEFRC	5004 B810h	5008 B810h	500C B810h
814h	32	EPWM_DECLR	5004 B814h	5008 B814h	500C B814h
820h	32	EPWM_DEMONCNT	5004 B820h	5008 B820h	500C B820h

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Table 3-585. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM13_G1 Physical Address	EPWM14_G1 Physical Address	EPWM15_G1 Physical Address
824h	32	EPWM_DEMONCTL	5004 B824h	5008 B824h	500C B824h
828h	32	EPWM_DEMONSTEP	5004 B828h	5008 B828h	500C B828h
82Ch	32	EPWM_DEMONTHRES	5004 B82Ch	5008 B82Ch	500C B82Ch
C00h	32	EPWM_MINDBCFG	5004 BC00h	5008 BC00h	500C BC00h
C04h	32	EPWM_MINDBDLY	5004 BC04h	5008 BC04h	500C BC04h
C20h	32	EPWM_LUTCTLA	5004 BC20h	5008 BC20h	500C BC20h
C24h	32	EPWM_LUTCTLB	5004 BC24h	5008 BC24h	500C BC24h

Table 3-586. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM16_G1 Physical Address	EPWM17_G1 Physical Address	EPWM18_G1 Physical Address
0h	16	EPWM_TBCTL	5000 C000h	5004 C000h	5008 C000h
2h	16	EPWM_TBCTL2	5000 C002h	5004 C002h	5008 C002h
6h	16	EPWM_EPWMSYNCINSEL	5000 C006h	5004 C006h	5008 C006h
8h	16	EPWM_TBCTR	5000 C008h	5004 C008h	5008 C008h
Ah	16	EPWM_TBSTS	5000 C00Ah	5004 C00Ah	5008 C00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5000 C00Ch	5004 C00Ch	5008 C00Ch
Eh	16	EPWM_TBCTL3	5000 C00Eh	5004 C00Eh	5008 C00Eh
10h	16	EPWM_CMPCTL	5000 C010h	5004 C010h	5008 C010h
12h	16	EPWM_CMPCTL2	5000 C012h	5004 C012h	5008 C012h
18h	16	EPWM_DBCTL	5000 C018h	5004 C018h	5008 C018h
1Ah	16	EPWM_DBCTL2	5000 C01Ah	5004 C01Ah	5008 C01Ah
20h	16	EPWM_AQCTL	5000 C020h	5004 C020h	5008 C020h
22h	16	EPWM_AQTSRCSEL	5000 C022h	5004 C022h	5008 C022h
28h	16	EPWM_PCCTL	5000 C028h	5004 C028h	5008 C028h
30h	16	EPWM_VCAPCTL	5000 C030h	5004 C030h	5008 C030h
32h	16	EPWM_VCNTCFG	5000 C032h	5004 C032h	5008 C032h
40h	16	EPWM_HRCNFG	5000 C040h	5004 C040h	5008 C040h
4Eh	16	EPWM_HRCNFG2	5000 C04Eh	5004 C04Eh	5008 C04Eh
5Ah	16	EPWM_HRPCTL	5000 C05Ah	5004 C05Ah	5008 C05Ah
5Ch	16	EPWM_TRREM	5000 C05Ch	5004 C05Ch	5008 C05Ch
68h	16	EPWM_GLDCTL	5000 C068h	5004 C068h	5008 C068h
6Ah	16	EPWM_GLDCFG	5000 C06Ah	5004 C06Ah	5008 C06Ah
70h	32	EPWM_EPWMXLINK	5000 C070h	5004 C070h	5008 C070h
74h	32	EPWM_EPWMXLINK2	5000 C074h	5004 C074h	5008 C074h
7Ah	16	EPWM_ETEST	5000 C07Ah	5004 C07Ah	5008 C07Ah
7Ch	16	EPWM_EPWMREV	5000 C07Ch	5004 C07Ch	5008 C07Ch
7Eh	16	EPWM_HRPWMREV	5000 C07Eh	5004 C07Eh	5008 C07Eh
80h	16	EPWM_AQCTLA	5000 C080h	5004 C080h	5008 C080h
82h	16	EPWM_AQCTLA2	5000 C082h	5004 C082h	5008 C082h
84h	16	EPWM_AQCTLB	5000 C084h	5004 C084h	5008 C084h
86h	16	EPWM_AQCTLB2	5000 C086h	5004 C086h	5008 C086h
8Eh	16	EPWM_AQSFRC	5000 C08Eh	5004 C08Eh	5008 C08Eh
92h	16	EPWM_AQCSFRC	5000 C092h	5004 C092h	5008 C092h
A0h	16	EPWM_DBREDHR	5000 C0A0h	5004 C0A0h	5008 C0A0h
A2h	16	EPWM_DBRED	5000 C0A2h	5004 C0A2h	5008 C0A2h

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Table 3-586. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM16_G1 Physical Address	EPWM17_G1 Physical Address	EPWM18_G1 Physical Address
A4h	16	EPWM_DBFEDHR	5000 C0A4h	5004 C0A4h	5008 C0A4h
A6h	16	EPWM_DBFED	5000 C0A6h	5004 C0A6h	5008 C0A6h
C0h	32	EPWM_TBPHS	5000 C0C0h	5004 C0C0h	5008 C0C0h
C4h	16	EPWM_TBPRDHR	5000 C0C4h	5004 C0C4h	5008 C0C4h
C6h	16	EPWM_TBPRD	5000 C0C6h	5004 C0C6h	5008 C0C6h
C8h	16	EPWM_TBPRDHRB	5000 C0C8h	5004 C0C8h	5008 C0C8h
D4h	32	EPWM_CMPA	5000 C0D4h	5004 C0D4h	5008 C0D4h
D8h	32	EPWM_CMPB	5000 C0D8h	5004 C0D8h	5008 C0D8h
DEh	16	EPWM_CMPC	5000 C0DEh	5004 C0DEh	5008 C0DEh
E2h	16	EPWM_CMPD	5000 C0E2h	5004 C0E2h	5008 C0E2h
E8h	16	EPWM_GLDCTL2	5000 C0E8h	5004 C0E8h	5008 C0E8h
EEh	16	EPWM_SWVDELVAL	5000 C0EEh	5004 C0EEh	5008 C0EEh
100h	16	EPWM_TZSEL	5000 C100h	5004 C100h	5008 C100h
102h	16	EPWM_TZSEL2	5000 C102h	5004 C102h	5008 C102h
104h	16	EPWM_TZDCSEL	5000 C104h	5004 C104h	5008 C104h
108h	16	EPWM_TZCTL	5000 C108h	5004 C108h	5008 C108h
10Ah	16	EPWM_TZCTL2	5000 C10Ah	5004 C10Ah	5008 C10Ah
10Ch	16	EPWM_TZCTLDCA	5000 C10Ch	5004 C10Ch	5008 C10Ch
10Eh	16	EPWM_TZCTLDCB	5000 C10Eh	5004 C10Eh	5008 C10Eh
11Ah	16	EPWM_TZEINT	5000 C11Ah	5004 C11Ah	5008 C11Ah
126h	16	EPWM_TZFLG	5000 C126h	5004 C126h	5008 C126h
128h	16	EPWM_TZCBCFLG	5000 C128h	5004 C128h	5008 C128h
12Ah	16	EPWM_TZOSTFLG	5000 C12Ah	5004 C12Ah	5008 C12Ah
12Eh	16	EPWM_TZCLR	5000 C12Eh	5004 C12Eh	5008 C12Eh
130h	16	EPWM_TZCBCCLR	5000 C130h	5004 C130h	5008 C130h
132h	16	EPWM_TZOSTCLR	5000 C132h	5004 C132h	5008 C132h
136h	16	EPWM_TZFRC	5000 C136h	5004 C136h	5008 C136h
13Ah	16	EPWM_TZTRIPOUTSEL	5000 C13Ah	5004 C13Ah	5008 C13Ah
148h	16	EPWM_ETSEL	5000 C148h	5004 C148h	5008 C148h
14Ch	16	EPWM_ETPS	5000 C14Ch	5004 C14Ch	5008 C14Ch
150h	16	EPWM_ETFLG	5000 C150h	5004 C150h	5008 C150h
154h	16	EPWM_ETCLR	5000 C154h	5004 C154h	5008 C154h
158h	16	EPWM_ETFRC	5000 C158h	5004 C158h	5008 C158h
15Ch	16	EPWM_ETINTPS	5000 C15Ch	5004 C15Ch	5008 C15Ch
160h	16	EPWM_ETSOCPS	5000 C160h	5004 C160h	5008 C160h
164h	16	EPWM_ETCNTINITCTL	5000 C164h	5004 C164h	5008 C164h
168h	16	EPWM_ETCNTINIT	5000 C168h	5004 C168h	5008 C168h
16Ch	16	EPWM_ETINTMIXEN	5000 C16Ch	5004 C16Ch	5008 C16Ch
170h	16	EPWM_ETSOCAMIXEN	5000 C170h	5004 C170h	5008 C170h
174h	16	EPWM_ETSOCBMIXEN	5000 C174h	5004 C174h	5008 C174h
180h	16	EPWM_DCTRIPSEL	5000 C180h	5004 C180h	5008 C180h
186h	16	EPWM_DCACTL	5000 C186h	5004 C186h	5008 C186h
188h	16	EPWM_DCBCTL	5000 C188h	5004 C188h	5008 C188h
18Eh	16	EPWM_DCFCTL	5000 C18Eh	5004 C18Eh	5008 C18Eh
190h	16	EPWM_DCCAPCTL	5000 C190h	5004 C190h	5008 C190h
192h	16	EPWM_DCFOFFSET	5000 C192h	5004 C192h	5008 C192h

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Table 3-586. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM16_G1 Physical Address	EPWM17_G1 Physical Address	EPWM18_G1 Physical Address
194h	16	EPWM_DCFOFFSETCNT	5000 C194h	5004 C194h	5008 C194h
196h	16	EPWM_DCFWINDOW	5000 C196h	5004 C196h	5008 C196h
198h	16	EPWM_DCFWINDOWCNT	5000 C198h	5004 C198h	5008 C198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5000 C19Ah	5004 C19Ah	5008 C19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5000 C19Ch	5004 C19Ch	5008 C19Ch
19Eh	16	EPWM_DCCAP	5000 C19Eh	5004 C19Eh	5008 C19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5000 C1A4h	5004 C1A4h	5008 C1A4h
1A6h	16	EPWM_DCALTRIPSEL	5000 C1A6h	5004 C1A6h	5008 C1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5000 C1A8h	5004 C1A8h	5008 C1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5000 C1AAh	5004 C1AAh	5008 C1AAh
1ACh	16	EPWM_CAPCTL	5000 C1ACh	5004 C1ACh	5008 C1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5000 C1AEh	5004 C1AEh	5008 C1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5000 C1B0h	5004 C1B0h	5008 C1B0h
1B2h	16	EPWM_CAPTRIPSEL	5000 C1B2h	5004 C1B2h	5008 C1B2h
1F4h	32	EPWM_EPWMLOCK	5000 C1F4h	5004 C1F4h	5008 C1F4h
1FAh	16	EPWM_HWVDELVAL	5000 C1FAh	5004 C1FAh	5008 C1FAh
1FCh	16	EPWM_VCNTVAL	5000 C1FCh	5004 C1FCh	5008 C1FCh
400h	32	EPWM_XCMPCTL1	5000 C400h	5004 C400h	5008 C400h
410h	32	EPWM_XLOADCTL	5000 C410h	5004 C410h	5008 C410h
418h	32	EPWM_XLOAD	5000 C418h	5004 C418h	5008 C418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5000 C41Ch	5004 C41Ch	5008 C41Ch
420h	32	EPWM_XREGSHDW1STS	5000 C420h	5004 C420h	5008 C420h
428h	32	EPWM_XREGSHDW2STS	5000 C428h	5004 C428h	5008 C428h
430h	32	EPWM_XREGSHDW3STS	5000 C430h	5004 C430h	5008 C430h
600h	32	EPWM_XCMP1_ACTIVE	5000 C600h	5004 C600h	5008 C600h
604h	32	EPWM_XCMP2_ACTIVE	5000 C604h	5004 C604h	5008 C604h
608h	32	EPWM_XCMP3_ACTIVE	5000 C608h	5004 C608h	5008 C608h
60Ch	32	EPWM_XCMP4_ACTIVE	5000 C60Ch	5004 C60Ch	5008 C60Ch
610h	32	EPWM_XCMP5_ACTIVE	5000 C610h	5004 C610h	5008 C610h
614h	32	EPWM_XCMP6_ACTIVE	5000 C614h	5004 C614h	5008 C614h
618h	32	EPWM_XCMP7_ACTIVE	5000 C618h	5004 C618h	5008 C618h
61Ch	32	EPWM_XCMP8_ACTIVE	5000 C61Ch	5004 C61Ch	5008 C61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5000 C620h	5004 C620h	5008 C620h
630h	16	EPWM_XAQCTLA_ACTIVE	5000 C630h	5004 C630h	5008 C630h
644h	32	EPWM_XMINMAX_ACTIVE	5000 C644h	5004 C644h	5008 C644h
680h	32	EPWM_XCMP1_SHDW1	5000 C680h	5004 C680h	5008 C680h
684h	32	EPWM_XCMP2_SHDW1	5000 C684h	5004 C684h	5008 C684h
688h	32	EPWM_XCMP3_SHDW1	5000 C688h	5004 C688h	5008 C688h
68Ch	32	EPWM_XCMP4_SHDW1	5000 C68Ch	5004 C68Ch	5008 C68Ch
690h	32	EPWM_XCMP5_SHDW1	5000 C690h	5004 C690h	5008 C690h
694h	32	EPWM_XCMP6_SHDW1	5000 C694h	5004 C694h	5008 C694h
698h	32	EPWM_XCMP7_SHDW1	5000 C698h	5004 C698h	5008 C698h
69Ch	32	EPWM_XCMP8_SHDW1	5000 C69Ch	5004 C69Ch	5008 C69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5000 C6A0h	5004 C6A0h	5008 C6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5000 C6B0h	5004 C6B0h	5008 C6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5000 C6B2h	5004 C6B2h	5008 C6B2h

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Table 3-586. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM16_G1 Physical Address	EPWM17_G1 Physical Address	EPWM18_G1 Physical Address
6BAh	16	EPWM_CMPC_SHDW1	5000 C6BAh	5004 C6BAh	5008 C6BAh
6BEh	16	EPWM_CMPD_SHDW1	5000 C6BEh	5004 C6BEh	5008 C6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5000 C6C4h	5004 C6C4h	5008 C6C4h
700h	32	EPWM_XCMP1_SHDW2	5000 C700h	5004 C700h	5008 C700h
704h	32	EPWM_XCMP2_SHDW2	5000 C704h	5004 C704h	5008 C704h
708h	32	EPWM_XCMP3_SHDW2	5000 C708h	5004 C708h	5008 C708h
70Ch	32	EPWM_XCMP4_SHDW2	5000 C70Ch	5004 C70Ch	5008 C70Ch
710h	32	EPWM_XCMP5_SHDW2	5000 C710h	5004 C710h	5008 C710h
714h	32	EPWM_XCMP6_SHDW2	5000 C714h	5004 C714h	5008 C714h
718h	32	EPWM_XCMP7_SHDW2	5000 C718h	5004 C718h	5008 C718h
71Ch	32	EPWM_XCMP8_SHDW2	5000 C71Ch	5004 C71Ch	5008 C71Ch
720h	32	EPWM_XTBPRD_SHDW2	5000 C720h	5004 C720h	5008 C720h
730h	16	EPWM_XAQCTLA_SHDW2	5000 C730h	5004 C730h	5008 C730h
732h	16	EPWM_XAQCTLB_SHDW2	5000 C732h	5004 C732h	5008 C732h
73Ah	16	EPWM_CMPC_SHDW2	5000 C73Ah	5004 C73Ah	5008 C73Ah
73Eh	16	EPWM_CMPD_SHDW2	5000 C73Eh	5004 C73Eh	5008 C73Eh
744h	32	EPWM_XMINMAX_SHDW2	5000 C744h	5004 C744h	5008 C744h
780h	32	EPWM_XCMP1_SHDW3	5000 C780h	5004 C780h	5008 C780h
784h	32	EPWM_XCMP2_SHDW3	5000 C784h	5004 C784h	5008 C784h
788h	32	EPWM_XCMP3_SHDW3	5000 C788h	5004 C788h	5008 C788h
78Ch	32	EPWM_XCMP4_SHDW3	5000 C78Ch	5004 C78Ch	5008 C78Ch
790h	32	EPWM_XCMP5_SHDW3	5000 C790h	5004 C790h	5008 C790h
794h	32	EPWM_XCMP6_SHDW3	5000 C794h	5004 C794h	5008 C794h
798h	32	EPWM_XCMP7_SHDW3	5000 C798h	5004 C798h	5008 C798h
79Ch	32	EPWM_XCMP8_SHDW3	5000 C79Ch	5004 C79Ch	5008 C79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5000 C7A0h	5004 C7A0h	5008 C7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5000 C7B0h	5004 C7B0h	5008 C7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5000 C7B2h	5004 C7B2h	5008 C7B2h
7BAh	16	EPWM_CMPC_SHDW3	5000 C7BAh	5004 C7BAh	5008 C7BAh
7BEh	16	EPWM_CMPD_SHDW3	5000 C7BEh	5004 C7BEh	5008 C7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5000 C7C4h	5004 C7C4h	5008 C7C4h
800h	32	EPWM_DECTL	5000 C800h	5004 C800h	5008 C800h
804h	32	EPWM_DECOMPSEL	5000 C804h	5004 C804h	5008 C804h
808h	32	EPWM_DEACTCTL	5000 C808h	5004 C808h	5008 C808h
80Ch	32	EPWM_DESTS	5000 C80Ch	5004 C80Ch	5008 C80Ch
810h	32	EPWM_DEFRC	5000 C810h	5004 C810h	5008 C810h
814h	32	EPWM_DECLR	5000 C814h	5004 C814h	5008 C814h
820h	32	EPWM_DEMONCNT	5000 C820h	5004 C820h	5008 C820h
824h	32	EPWM_DEMONCTL	5000 C824h	5004 C824h	5008 C824h
828h	32	EPWM_DEMONSTEP	5000 C828h	5004 C828h	5008 C828h
82Ch	32	EPWM_DEMONTHRES	5000 C82Ch	5004 C82Ch	5008 C82Ch
C00h	32	EPWM_MINDBCFG	5000 CC00h	5004 CC00h	5008 CC00h
C04h	32	EPWM_MINDBDLY	5000 CC04h	5004 CC04h	5008 CC04h
C20h	32	EPWM_LUTCTLA	5000 CC20h	5004 CC20h	5008 CC20h
C24h	32	EPWM_LUTCTLB	5000 CC24h	5004 CC24h	5008 CC24h

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Table 3-587. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM19_G1 Physical Address	EPWM20_G1 Physical Address	EPWM21_G1 Physical Address
0h	16	EPWM_TBCTL	500C C000h	5000 D000h	5004 D000h
2h	16	EPWM_TBCTL2	500C C002h	5000 D002h	5004 D002h
6h	16	EPWM_EPWMSYNCINSEL	500C C006h	5000 D006h	5004 D006h
8h	16	EPWM_TBCTR	500C C008h	5000 D008h	5004 D008h
Ah	16	EPWM_TBSTS	500C C00Ah	5000 D00Ah	5004 D00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500C C00Ch	5000 D00Ch	5004 D00Ch
Eh	16	EPWM_TBCTL3	500C C00Eh	5000 D00Eh	5004 D00Eh
10h	16	EPWM_CMPCTL	500C C010h	5000 D010h	5004 D010h
12h	16	EPWM_CMPCTL2	500C C012h	5000 D012h	5004 D012h
18h	16	EPWM_DBCTL	500C C018h	5000 D018h	5004 D018h
1Ah	16	EPWM_DBCTL2	500C C01Ah	5000 D01Ah	5004 D01Ah
20h	16	EPWM_AQCTL	500C C020h	5000 D020h	5004 D020h
22h	16	EPWM_AQTSRCSEL	500C C022h	5000 D022h	5004 D022h
28h	16	EPWM_PCCTL	500C C028h	5000 D028h	5004 D028h
30h	16	EPWM_VCAPCTL	500C C030h	5000 D030h	5004 D030h
32h	16	EPWM_VCNTCFG	500C C032h	5000 D032h	5004 D032h
40h	16	EPWM_HRCNFG	500C C040h	5000 D040h	5004 D040h
4Eh	16	EPWM_HRCNFG2	500C C04Eh	5000 D04Eh	5004 D04Eh
5Ah	16	EPWM_HRPCTL	500C C05Ah	5000 D05Ah	5004 D05Ah
5Ch	16	EPWM_TRREM	500C C05Ch	5000 D05Ch	5004 D05Ch
68h	16	EPWM_GLDCTL	500C C068h	5000 D068h	5004 D068h
6Ah	16	EPWM_GLDCFG	500C C06Ah	5000 D06Ah	5004 D06Ah
70h	32	EPWM_EPWMXLINK	500C C070h	5000 D070h	5004 D070h
74h	32	EPWM_EPWMXLINK2	500C C074h	5000 D074h	5004 D074h
7Ah	16	EPWM_ETEST	500C C07Ah	5000 D07Ah	5004 D07Ah
7Ch	16	EPWM_EPWMREV	500C C07Ch	5000 D07Ch	5004 D07Ch
7Eh	16	EPWM_HRPWMREV	500C C07Eh	5000 D07Eh	5004 D07Eh
80h	16	EPWM_AQCTLA	500C C080h	5000 D080h	5004 D080h
82h	16	EPWM_AQCTLA2	500C C082h	5000 D082h	5004 D082h
84h	16	EPWM_AQCTLB	500C C084h	5000 D084h	5004 D084h
86h	16	EPWM_AQCTLB2	500C C086h	5000 D086h	5004 D086h
8Eh	16	EPWM_AQSFRC	500C C08Eh	5000 D08Eh	5004 D08Eh
92h	16	EPWM_AQCSFRC	500C C092h	5000 D092h	5004 D092h
A0h	16	EPWM_DBREDHR	500C C0A0h	5000 D0A0h	5004 D0A0h
A2h	16	EPWM_DBRED	500C C0A2h	5000 D0A2h	5004 D0A2h
A4h	16	EPWM_DBFEDHR	500C C0A4h	5000 D0A4h	5004 D0A4h
A6h	16	EPWM_DBFED	500C C0A6h	5000 D0A6h	5004 D0A6h
C0h	32	EPWM_TBPHS	500C C0C0h	5000 D0C0h	5004 D0C0h
C4h	16	EPWM_TBPRDHR	500C C0C4h	5000 D0C4h	5004 D0C4h
C6h	16	EPWM_TBPRD	500C C0C6h	5000 D0C6h	5004 D0C6h
C8h	16	EPWM_TBPRDHRB	500C C0C8h	5000 D0C8h	5004 D0C8h
D4h	32	EPWM_CMPA	500C C0D4h	5000 D0D4h	5004 D0D4h
D8h	32	EPWM_CMPB	500C C0D8h	5000 D0D8h	5004 D0D8h
DEh	16	EPWM_CMPC	500C C0DEh	5000 D0DEh	5004 D0DEh
E2h	16	EPWM_CMPD	500C C0E2h	5000 D0E2h	5004 D0E2h

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Table 3-587. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM19_G1 Physical Address	EPWM20_G1 Physical Address	EPWM21_G1 Physical Address
E8h	16	EPWM_GLDCTL2	500C C0E8h	5000 D0E8h	5004 D0E8h
EEh	16	EPWM_SWVDELVAL	500C C0EEh	5000 D0EEh	5004 D0EEh
100h	16	EPWM_TZSEL	500C C100h	5000 D100h	5004 D100h
102h	16	EPWM_TZSEL2	500C C102h	5000 D102h	5004 D102h
104h	16	EPWM_TZDCSEL	500C C104h	5000 D104h	5004 D104h
108h	16	EPWM_TZCTL	500C C108h	5000 D108h	5004 D108h
10Ah	16	EPWM_TZCTL2	500C C10Ah	5000 D10Ah	5004 D10Ah
10Ch	16	EPWM_TZCTLDCA	500C C10Ch	5000 D10Ch	5004 D10Ch
10Eh	16	EPWM_TZCTLDCB	500C C10Eh	5000 D10Eh	5004 D10Eh
11Ah	16	EPWM_TZEINT	500C C11Ah	5000 D11Ah	5004 D11Ah
126h	16	EPWM_TZFLG	500C C126h	5000 D126h	5004 D126h
128h	16	EPWM_TZCBCFLG	500C C128h	5000 D128h	5004 D128h
12Ah	16	EPWM_TZOSTFLG	500C C12Ah	5000 D12Ah	5004 D12Ah
12Eh	16	EPWM_TZCLR	500C C12Eh	5000 D12Eh	5004 D12Eh
130h	16	EPWM_TZCBCCLR	500C C130h	5000 D130h	5004 D130h
132h	16	EPWM_TZOSTCLR	500C C132h	5000 D132h	5004 D132h
136h	16	EPWM_TZFRC	500C C136h	5000 D136h	5004 D136h
13Ah	16	EPWM_TZTRIPOUTSEL	500C C13Ah	5000 D13Ah	5004 D13Ah
148h	16	EPWM_ETSEL	500C C148h	5000 D148h	5004 D148h
14Ch	16	EPWM_ETPS	500C C14Ch	5000 D14Ch	5004 D14Ch
150h	16	EPWM_ETFLG	500C C150h	5000 D150h	5004 D150h
154h	16	EPWM_ETCLR	500C C154h	5000 D154h	5004 D154h
158h	16	EPWM_ETFRC	500C C158h	5000 D158h	5004 D158h
15Ch	16	EPWM_ETINTPS	500C C15Ch	5000 D15Ch	5004 D15Ch
160h	16	EPWM_ETSOCPS	500C C160h	5000 D160h	5004 D160h
164h	16	EPWM_ETCNTINITCTL	500C C164h	5000 D164h	5004 D164h
168h	16	EPWM_ETCNTINIT	500C C168h	5000 D168h	5004 D168h
16Ch	16	EPWM_ETINTMIXEN	500C C16Ch	5000 D16Ch	5004 D16Ch
170h	16	EPWM_ETSOCAMIXEN	500C C170h	5000 D170h	5004 D170h
174h	16	EPWM_ETSOCBMIXEN	500C C174h	5000 D174h	5004 D174h
180h	16	EPWM_DCTRIPSEL	500C C180h	5000 D180h	5004 D180h
186h	16	EPWM_DCACTL	500C C186h	5000 D186h	5004 D186h
188h	16	EPWM_DCBCTL	500C C188h	5000 D188h	5004 D188h
18Eh	16	EPWM_DCFCTL	500C C18Eh	5000 D18Eh	5004 D18Eh
190h	16	EPWM_DCCAPCTL	500C C190h	5000 D190h	5004 D190h
192h	16	EPWM_DCFOFFSET	500C C192h	5000 D192h	5004 D192h
194h	16	EPWM_DCFOFFSETCNT	500C C194h	5000 D194h	5004 D194h
196h	16	EPWM_DCFWINDOW	500C C196h	5000 D196h	5004 D196h
198h	16	EPWM_DCFWINDOWCNT	500C C198h	5000 D198h	5004 D198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500C C19Ah	5000 D19Ah	5004 D19Ah
19Ch	16	EPWM_DCCAPMIXSEL	500C C19Ch	5000 D19Ch	5004 D19Ch
19Eh	16	EPWM_DCCAP	500C C19Eh	5000 D19Eh	5004 D19Eh
1A4h	16	EPWM_DCAHTRIPSEL	500C C1A4h	5000 D1A4h	5004 D1A4h
1A6h	16	EPWM_DCALTRIPSEL	500C C1A6h	5000 D1A6h	5004 D1A6h
1A8h	16	EPWM_DCBHTRIPSEL	500C C1A8h	5000 D1A8h	5004 D1A8h
1AAh	16	EPWM_DCBLTRIPSEL	500C C1AAh	5000 D1AAh	5004 D1AAh

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Table 3-587. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM19_G1 Physical Address	EPWM20_G1 Physical Address	EPWM21_G1 Physical Address
1ACh	16	EPWM_CAPCTL	500C C1ACh	5000 D1ACh	5004 D1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500C C1AEh	5000 D1AEh	5004 D1AEh
1B0h	16	EPWM_CAPINTRIPSEL	500C C1B0h	5000 D1B0h	5004 D1B0h
1B2h	16	EPWM_CAPTRIPSEL	500C C1B2h	5000 D1B2h	5004 D1B2h
1F4h	32	EPWM_EPWMLOCK	500C C1F4h	5000 D1F4h	5004 D1F4h
1FAh	16	EPWM_HWVDELVAL	500C C1FAh	5000 D1FAh	5004 D1FAh
1FCh	16	EPWM_VCNTVAL	500C C1FCh	5000 D1FCh	5004 D1FCh
400h	32	EPWM_XCMPCTL1	500C C400h	5000 D400h	5004 D400h
410h	32	EPWM_XLOADCTL	500C C410h	5000 D410h	5004 D410h
418h	32	EPWM_XLOAD	500C C418h	5000 D418h	5004 D418h
41Ch	32	EPWM_EPWMXLINKXLOAD	500C C41Ch	5000 D41Ch	5004 D41Ch
420h	32	EPWM_XREGSHDW1STS	500C C420h	5000 D420h	5004 D420h
428h	32	EPWM_XREGSHDW2STS	500C C428h	5000 D428h	5004 D428h
430h	32	EPWM_XREGSHDW3STS	500C C430h	5000 D430h	5004 D430h
600h	32	EPWM_XCMP1_ACTIVE	500C C600h	5000 D600h	5004 D600h
604h	32	EPWM_XCMP2_ACTIVE	500C C604h	5000 D604h	5004 D604h
608h	32	EPWM_XCMP3_ACTIVE	500C C608h	5000 D608h	5004 D608h
60Ch	32	EPWM_XCMP4_ACTIVE	500C C60Ch	5000 D60Ch	5004 D60Ch
610h	32	EPWM_XCMP5_ACTIVE	500C C610h	5000 D610h	5004 D610h
614h	32	EPWM_XCMP6_ACTIVE	500C C614h	5000 D614h	5004 D614h
618h	32	EPWM_XCMP7_ACTIVE	500C C618h	5000 D618h	5004 D618h
61Ch	32	EPWM_XCMP8_ACTIVE	500C C61Ch	5000 D61Ch	5004 D61Ch
620h	32	EPWM_XTBPRD_ACTIVE	500C C620h	5000 D620h	5004 D620h
630h	16	EPWM_XAQCTLA_ACTIVE	500C C630h	5000 D630h	5004 D630h
644h	32	EPWM_XMINMAX_ACTIVE	500C C644h	5000 D644h	5004 D644h
680h	32	EPWM_XCMP1_SHDW1	500C C680h	5000 D680h	5004 D680h
684h	32	EPWM_XCMP2_SHDW1	500C C684h	5000 D684h	5004 D684h
688h	32	EPWM_XCMP3_SHDW1	500C C688h	5000 D688h	5004 D688h
68Ch	32	EPWM_XCMP4_SHDW1	500C C68Ch	5000 D68Ch	5004 D68Ch
690h	32	EPWM_XCMP5_SHDW1	500C C690h	5000 D690h	5004 D690h
694h	32	EPWM_XCMP6_SHDW1	500C C694h	5000 D694h	5004 D694h
698h	32	EPWM_XCMP7_SHDW1	500C C698h	5000 D698h	5004 D698h
69Ch	32	EPWM_XCMP8_SHDW1	500C C69Ch	5000 D69Ch	5004 D69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500C C6A0h	5000 D6A0h	5004 D6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500C C6B0h	5000 D6B0h	5004 D6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500C C6B2h	5000 D6B2h	5004 D6B2h
6BAh	16	EPWM_CMPC_SHDW1	500C C6BAh	5000 D6BAh	5004 D6BAh
6BEh	16	EPWM_CMPD_SHDW1	500C C6BEh	5000 D6BEh	5004 D6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500C C6C4h	5000 D6C4h	5004 D6C4h
700h	32	EPWM_XCMP1_SHDW2	500C C700h	5000 D700h	5004 D700h
704h	32	EPWM_XCMP2_SHDW2	500C C704h	5000 D704h	5004 D704h
708h	32	EPWM_XCMP3_SHDW2	500C C708h	5000 D708h	5004 D708h
70Ch	32	EPWM_XCMP4_SHDW2	500C C70Ch	5000 D70Ch	5004 D70Ch
710h	32	EPWM_XCMP5_SHDW2	500C C710h	5000 D710h	5004 D710h
714h	32	EPWM_XCMP6_SHDW2	500C C714h	5000 D714h	5004 D714h
718h	32	EPWM_XCMP7_SHDW2	500C C718h	5000 D718h	5004 D718h

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Table 3-587. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM19_G1 Physical Address	EPWM20_G1 Physical Address	EPWM21_G1 Physical Address
71Ch	32	EPWM_XCMP8_SHDW2	500C C71Ch	5000 D71Ch	5004 D71Ch
720h	32	EPWM_XTBPRD_SHDW2	500C C720h	5000 D720h	5004 D720h
730h	16	EPWM_XAQCTLA_SHDW2	500C C730h	5000 D730h	5004 D730h
732h	16	EPWM_XAQCTLB_SHDW2	500C C732h	5000 D732h	5004 D732h
73Ah	16	EPWM_CMPC_SHDW2	500C C73Ah	5000 D73Ah	5004 D73Ah
73Eh	16	EPWM_CMPD_SHDW2	500C C73Eh	5000 D73Eh	5004 D73Eh
744h	32	EPWM_XMINMAX_SHDW2	500C C744h	5000 D744h	5004 D744h
780h	32	EPWM_XCMP1_SHDW3	500C C780h	5000 D780h	5004 D780h
784h	32	EPWM_XCMP2_SHDW3	500C C784h	5000 D784h	5004 D784h
788h	32	EPWM_XCMP3_SHDW3	500C C788h	5000 D788h	5004 D788h
78Ch	32	EPWM_XCMP4_SHDW3	500C C78Ch	5000 D78Ch	5004 D78Ch
790h	32	EPWM_XCMP5_SHDW3	500C C790h	5000 D790h	5004 D790h
794h	32	EPWM_XCMP6_SHDW3	500C C794h	5000 D794h	5004 D794h
798h	32	EPWM_XCMP7_SHDW3	500C C798h	5000 D798h	5004 D798h
79Ch	32	EPWM_XCMP8_SHDW3	500C C79Ch	5000 D79Ch	5004 D79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500C C7A0h	5000 D7A0h	5004 D7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500C C7B0h	5000 D7B0h	5004 D7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500C C7B2h	5000 D7B2h	5004 D7B2h
7BAh	16	EPWM_CMPC_SHDW3	500C C7BAh	5000 D7BAh	5004 D7BAh
7BEh	16	EPWM_CMPD_SHDW3	500C C7BEh	5000 D7BEh	5004 D7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500C C7C4h	5000 D7C4h	5004 D7C4h
800h	32	EPWM_DECTL	500C C800h	5000 D800h	5004 D800h
804h	32	EPWM_DECOMPSEL	500C C804h	5000 D804h	5004 D804h
808h	32	EPWM_DEACTCTL	500C C808h	5000 D808h	5004 D808h
80Ch	32	EPWM_DESTS	500C C80Ch	5000 D80Ch	5004 D80Ch
810h	32	EPWM_DEFRC	500C C810h	5000 D810h	5004 D810h
814h	32	EPWM_DECLR	500C C814h	5000 D814h	5004 D814h
820h	32	EPWM_DEMONCNT	500C C820h	5000 D820h	5004 D820h
824h	32	EPWM_DEMONCTL	500C C824h	5000 D824h	5004 D824h
828h	32	EPWM_DEMONSTEP	500C C828h	5000 D828h	5004 D828h
82Ch	32	EPWM_DEMONTHRES	500C C82Ch	5000 D82Ch	5004 D82Ch
C00h	32	EPWM_MINDBCFG	500C CC00h	5000 DC00h	5004 DC00h
C04h	32	EPWM_MINDBDLY	500C CC04h	5000 DC04h	5004 DC04h
C20h	32	EPWM_LUTCTLA	500C CC20h	5000 DC20h	5004 DC20h
C24h	32	EPWM_LUTCTLB	500C CC24h	5000 DC24h	5004 DC24h

Table 3-588. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM22_G1 Physical Address	EPWM23_G1 Physical Address	EPWM24_G1 Physical Address
0h	16	EPWM_TBCTL	5008 D000h	500C D000h	5000 E000h
2h	16	EPWM_TBCTL2	5008 D002h	500C D002h	5000 E002h
6h	16	EPWM_EPWMSYNCINSEL	5008 D006h	500C D006h	5000 E006h
8h	16	EPWM_TBCTR	5008 D008h	500C D008h	5000 E008h
Ah	16	EPWM_TBSTS	5008 D00Ah	500C D00Ah	5000 E00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5008 D00Ch	500C D00Ch	5000 E00Ch
Eh	16	EPWM_TBCTL3	5008 D00Eh	500C D00Eh	5000 E00Eh

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Table 3-588. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM22_G1 Physical Address	EPWM23_G1 Physical Address	EPWM24_G1 Physical Address
10h	16	EPWM_CMPCTL	5008 D010h	500C D010h	5000 E010h
12h	16	EPWM_CMPCTL2	5008 D012h	500C D012h	5000 E012h
18h	16	EPWM_DBCTL	5008 D018h	500C D018h	5000 E018h
1Ah	16	EPWM_DBCTL2	5008 D01Ah	500C D01Ah	5000 E01Ah
20h	16	EPWM_AQCTL	5008 D020h	500C D020h	5000 E020h
22h	16	EPWM_AQTSRCSEL	5008 D022h	500C D022h	5000 E022h
28h	16	EPWM_PCCTL	5008 D028h	500C D028h	5000 E028h
30h	16	EPWM_VCAPCTL	5008 D030h	500C D030h	5000 E030h
32h	16	EPWM_VCNTCFG	5008 D032h	500C D032h	5000 E032h
40h	16	EPWM_HRCNFG	5008 D040h	500C D040h	5000 E040h
4Eh	16	EPWM_HRCNFG2	5008 D04Eh	500C D04Eh	5000 E04Eh
5Ah	16	EPWM_HRPCTL	5008 D05Ah	500C D05Ah	5000 E05Ah
5Ch	16	EPWM_TRREM	5008 D05Ch	500C D05Ch	5000 E05Ch
68h	16	EPWM_GLDCTL	5008 D068h	500C D068h	5000 E068h
6Ah	16	EPWM_GLDCFG	5008 D06Ah	500C D06Ah	5000 E06Ah
70h	32	EPWM_EPWMXLINK	5008 D070h	500C D070h	5000 E070h
74h	32	EPWM_EPWMXLINK2	5008 D074h	500C D074h	5000 E074h
7Ah	16	EPWM_ETEST	5008 D07Ah	500C D07Ah	5000 E07Ah
7Ch	16	EPWM_EPWMREV	5008 D07Ch	500C D07Ch	5000 E07Ch
7Eh	16	EPWM_HRPWMREV	5008 D07Eh	500C D07Eh	5000 E07Eh
80h	16	EPWM_AQCTLA	5008 D080h	500C D080h	5000 E080h
82h	16	EPWM_AQCTLA2	5008 D082h	500C D082h	5000 E082h
84h	16	EPWM_AQCTLB	5008 D084h	500C D084h	5000 E084h
86h	16	EPWM_AQCTLB2	5008 D086h	500C D086h	5000 E086h
8Eh	16	EPWM_AQSFRC	5008 D08Eh	500C D08Eh	5000 E08Eh
92h	16	EPWM_AQCSFRC	5008 D092h	500C D092h	5000 E092h
A0h	16	EPWM_DBREDHR	5008 D0A0h	500C D0A0h	5000 E0A0h
A2h	16	EPWM_DBRED	5008 D0A2h	500C D0A2h	5000 E0A2h
A4h	16	EPWM_DBFEDHR	5008 D0A4h	500C D0A4h	5000 E0A4h
A6h	16	EPWM_DBFED	5008 D0A6h	500C D0A6h	5000 E0A6h
C0h	32	EPWM_TBPHS	5008 D0C0h	500C D0C0h	5000 E0C0h
C4h	16	EPWM_TBPRDHR	5008 D0C4h	500C D0C4h	5000 E0C4h
C6h	16	EPWM_TBPRD	5008 D0C6h	500C D0C6h	5000 E0C6h
C8h	16	EPWM_TBPRDHRB	5008 D0C8h	500C D0C8h	5000 E0C8h
D4h	32	EPWM_CMPA	5008 D0D4h	500C D0D4h	5000 E0D4h
D8h	32	EPWM_CMPB	5008 D0D8h	500C D0D8h	5000 E0D8h
DEh	16	EPWM_CMPC	5008 D0DEh	500C D0DEh	5000 E0DEh
E2h	16	EPWM_CMPD	5008 D0E2h	500C D0E2h	5000 E0E2h
E8h	16	EPWM_GLDCTL2	5008 D0E8h	500C D0E8h	5000 E0E8h
EEh	16	EPWM_SWVDELVAL	5008 D0EEh	500C D0EEh	5000 E0EEh
100h	16	EPWM_TZSEL	5008 D100h	500C D100h	5000 E100h
102h	16	EPWM_TZSEL2	5008 D102h	500C D102h	5000 E102h
104h	16	EPWM_TZDCSEL	5008 D104h	500C D104h	5000 E104h
108h	16	EPWM_TZCTL	5008 D108h	500C D108h	5000 E108h
10Ah	16	EPWM_TZCTL2	5008 D10Ah	500C D10Ah	5000 E10Ah
10Ch	16	EPWM_TZCTLDCA	5008 D10Ch	500C D10Ch	5000 E10Ch

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Table 3-588. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM22_G1 Physical Address	EPWM23_G1 Physical Address	EPWM24_G1 Physical Address
10Eh	16	EPWM_TZCTLDCB	5008 D10Eh	500C D10Eh	5000 E10Eh
11Ah	16	EPWM_TZEINT	5008 D11Ah	500C D11Ah	5000 E11Ah
126h	16	EPWM_TZFLG	5008 D126h	500C D126h	5000 E126h
128h	16	EPWM_TZCBCFLG	5008 D128h	500C D128h	5000 E128h
12Ah	16	EPWM_TZOSTFLG	5008 D12Ah	500C D12Ah	5000 E12Ah
12Eh	16	EPWM_TZCLR	5008 D12Eh	500C D12Eh	5000 E12Eh
130h	16	EPWM_TZCBCCLR	5008 D130h	500C D130h	5000 E130h
132h	16	EPWM_TZOSTCLR	5008 D132h	500C D132h	5000 E132h
136h	16	EPWM_TZFRC	5008 D136h	500C D136h	5000 E136h
13Ah	16	EPWM_TZTRIPOUTSEL	5008 D13Ah	500C D13Ah	5000 E13Ah
148h	16	EPWM_ETSEL	5008 D148h	500C D148h	5000 E148h
14Ch	16	EPWM_ETPS	5008 D14Ch	500C D14Ch	5000 E14Ch
150h	16	EPWM_ETFLG	5008 D150h	500C D150h	5000 E150h
154h	16	EPWM_ETCLR	5008 D154h	500C D154h	5000 E154h
158h	16	EPWM_ETFRC	5008 D158h	500C D158h	5000 E158h
15Ch	16	EPWM_ETINTPS	5008 D15Ch	500C D15Ch	5000 E15Ch
160h	16	EPWM_ETSOCPS	5008 D160h	500C D160h	5000 E160h
164h	16	EPWM_ETCNTINITCTL	5008 D164h	500C D164h	5000 E164h
168h	16	EPWM_ETCNTINIT	5008 D168h	500C D168h	5000 E168h
16Ch	16	EPWM_ETINTMIXEN	5008 D16Ch	500C D16Ch	5000 E16Ch
170h	16	EPWM_ETSOCAMIXEN	5008 D170h	500C D170h	5000 E170h
174h	16	EPWM_ETSOCBMIXEN	5008 D174h	500C D174h	5000 E174h
180h	16	EPWM_DCTRIPSEL	5008 D180h	500C D180h	5000 E180h
186h	16	EPWM_DCACTL	5008 D186h	500C D186h	5000 E186h
188h	16	EPWM_DCBCTL	5008 D188h	500C D188h	5000 E188h
18Eh	16	EPWM_DCFCTL	5008 D18Eh	500C D18Eh	5000 E18Eh
190h	16	EPWM_DCCAPCTL	5008 D190h	500C D190h	5000 E190h
192h	16	EPWM_DCFOFFSET	5008 D192h	500C D192h	5000 E192h
194h	16	EPWM_DCFOFFSETCNT	5008 D194h	500C D194h	5000 E194h
196h	16	EPWM_DCFWINDOW	5008 D196h	500C D196h	5000 E196h
198h	16	EPWM_DCFWINDOWCNT	5008 D198h	500C D198h	5000 E198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5008 D19Ah	500C D19Ah	5000 E19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5008 D19Ch	500C D19Ch	5000 E19Ch
19Eh	16	EPWM_DCCAP	5008 D19Eh	500C D19Eh	5000 E19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5008 D1A4h	500C D1A4h	5000 E1A4h
1A6h	16	EPWM_DCALTRIPSEL	5008 D1A6h	500C D1A6h	5000 E1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5008 D1A8h	500C D1A8h	5000 E1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5008 D1AAh	500C D1AAh	5000 E1AAh
1ACh	16	EPWM_CAPCTL	5008 D1ACh	500C D1ACh	5000 E1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5008 D1AEh	500C D1AEh	5000 E1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5008 D1B0h	500C D1B0h	5000 E1B0h
1B2h	16	EPWM_CAPTRIPSEL	5008 D1B2h	500C D1B2h	5000 E1B2h
1F4h	32	EPWM_EPWMLOCK	5008 D1F4h	500C D1F4h	5000 E1F4h
1FAh	16	EPWM_HWVDELVAL	5008 D1FAh	500C D1FAh	5000 E1FAh
1FCh	16	EPWM_VCNTVAL	5008 D1FCh	500C D1FCh	5000 E1FCh
400h	32	EPWM_XCMPCTL1	5008 D400h	500C D400h	5000 E400h

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Table 3-588. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM22_G1 Physical Address	EPWM23_G1 Physical Address	EPWM24_G1 Physical Address
410h	32	EPWM_XLOADCTL	5008 D410h	500C D410h	5000 E410h
418h	32	EPWM_XLOAD	5008 D418h	500C D418h	5000 E418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5008 D41Ch	500C D41Ch	5000 E41Ch
420h	32	EPWM_XREGSHDW1STS	5008 D420h	500C D420h	5000 E420h
428h	32	EPWM_XREGSHDW2STS	5008 D428h	500C D428h	5000 E428h
430h	32	EPWM_XREGSHDW3STS	5008 D430h	500C D430h	5000 E430h
600h	32	EPWM_XCMP1_ACTIVE	5008 D600h	500C D600h	5000 E600h
604h	32	EPWM_XCMP2_ACTIVE	5008 D604h	500C D604h	5000 E604h
608h	32	EPWM_XCMP3_ACTIVE	5008 D608h	500C D608h	5000 E608h
60Ch	32	EPWM_XCMP4_ACTIVE	5008 D60Ch	500C D60Ch	5000 E60Ch
610h	32	EPWM_XCMP5_ACTIVE	5008 D610h	500C D610h	5000 E610h
614h	32	EPWM_XCMP6_ACTIVE	5008 D614h	500C D614h	5000 E614h
618h	32	EPWM_XCMP7_ACTIVE	5008 D618h	500C D618h	5000 E618h
61Ch	32	EPWM_XCMP8_ACTIVE	5008 D61Ch	500C D61Ch	5000 E61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5008 D620h	500C D620h	5000 E620h
630h	16	EPWM_XAQCTLA_ACTIVE	5008 D630h	500C D630h	5000 E630h
644h	32	EPWM_XMINMAX_ACTIVE	5008 D644h	500C D644h	5000 E644h
680h	32	EPWM_XCMP1_SHDW1	5008 D680h	500C D680h	5000 E680h
684h	32	EPWM_XCMP2_SHDW1	5008 D684h	500C D684h	5000 E684h
688h	32	EPWM_XCMP3_SHDW1	5008 D688h	500C D688h	5000 E688h
68Ch	32	EPWM_XCMP4_SHDW1	5008 D68Ch	500C D68Ch	5000 E68Ch
690h	32	EPWM_XCMP5_SHDW1	5008 D690h	500C D690h	5000 E690h
694h	32	EPWM_XCMP6_SHDW1	5008 D694h	500C D694h	5000 E694h
698h	32	EPWM_XCMP7_SHDW1	5008 D698h	500C D698h	5000 E698h
69Ch	32	EPWM_XCMP8_SHDW1	5008 D69Ch	500C D69Ch	5000 E69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5008 D6A0h	500C D6A0h	5000 E6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5008 D6B0h	500C D6B0h	5000 E6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5008 D6B2h	500C D6B2h	5000 E6B2h
6BAh	16	EPWM_CMPC_SHDW1	5008 D6BAh	500C D6BAh	5000 E6BAh
6BEh	16	EPWM_CMPD_SHDW1	5008 D6BEh	500C D6BEh	5000 E6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5008 D6C4h	500C D6C4h	5000 E6C4h
700h	32	EPWM_XCMP1_SHDW2	5008 D700h	500C D700h	5000 E700h
704h	32	EPWM_XCMP2_SHDW2	5008 D704h	500C D704h	5000 E704h
708h	32	EPWM_XCMP3_SHDW2	5008 D708h	500C D708h	5000 E708h
70Ch	32	EPWM_XCMP4_SHDW2	5008 D70Ch	500C D70Ch	5000 E70Ch
710h	32	EPWM_XCMP5_SHDW2	5008 D710h	500C D710h	5000 E710h
714h	32	EPWM_XCMP6_SHDW2	5008 D714h	500C D714h	5000 E714h
718h	32	EPWM_XCMP7_SHDW2	5008 D718h	500C D718h	5000 E718h
71Ch	32	EPWM_XCMP8_SHDW2	5008 D71Ch	500C D71Ch	5000 E71Ch
720h	32	EPWM_XTBPRD_SHDW2	5008 D720h	500C D720h	5000 E720h
730h	16	EPWM_XAQCTLA_SHDW2	5008 D730h	500C D730h	5000 E730h
732h	16	EPWM_XAQCTLB_SHDW2	5008 D732h	500C D732h	5000 E732h
73Ah	16	EPWM_CMPC_SHDW2	5008 D73Ah	500C D73Ah	5000 E73Ah
73Eh	16	EPWM_CMPD_SHDW2	5008 D73Eh	500C D73Eh	5000 E73Eh
744h	32	EPWM_XMINMAX_SHDW2	5008 D744h	500C D744h	5000 E744h
780h	32	EPWM_XCMP1_SHDW3	5008 D780h	500C D780h	5000 E780h

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Table 3-588. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM22_G1 Physical Address	EPWM23_G1 Physical Address	EPWM24_G1 Physical Address
784h	32	EPWM_XCMP2_SHDW3	5008 D784h	500C D784h	5000 E784h
788h	32	EPWM_XCMP3_SHDW3	5008 D788h	500C D788h	5000 E788h
78Ch	32	EPWM_XCMP4_SHDW3	5008 D78Ch	500C D78Ch	5000 E78Ch
790h	32	EPWM_XCMP5_SHDW3	5008 D790h	500C D790h	5000 E790h
794h	32	EPWM_XCMP6_SHDW3	5008 D794h	500C D794h	5000 E794h
798h	32	EPWM_XCMP7_SHDW3	5008 D798h	500C D798h	5000 E798h
79Ch	32	EPWM_XCMP8_SHDW3	5008 D79Ch	500C D79Ch	5000 E79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5008 D7A0h	500C D7A0h	5000 E7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5008 D7B0h	500C D7B0h	5000 E7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5008 D7B2h	500C D7B2h	5000 E7B2h
7BAh	16	EPWM_CMPC_SHDW3	5008 D7BAh	500C D7BAh	5000 E7BAh
7BEh	16	EPWM_CMPD_SHDW3	5008 D7BEh	500C D7BEh	5000 E7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5008 D7C4h	500C D7C4h	5000 E7C4h
800h	32	EPWM_DECTL	5008 D800h	500C D800h	5000 E800h
804h	32	EPWM_DECOMPSEL	5008 D804h	500C D804h	5000 E804h
808h	32	EPWM_DEACTCTL	5008 D808h	500C D808h	5000 E808h
80Ch	32	EPWM_DESTS	5008 D80Ch	500C D80Ch	5000 E80Ch
810h	32	EPWM_DEFRC	5008 D810h	500C D810h	5000 E810h
814h	32	EPWM_DECLR	5008 D814h	500C D814h	5000 E814h
820h	32	EPWM_DEMONCNT	5008 D820h	500C D820h	5000 E820h
824h	32	EPWM_DEMONCTL	5008 D824h	500C D824h	5000 E824h
828h	32	EPWM_DEMONSTEP	5008 D828h	500C D828h	5000 E828h
82Ch	32	EPWM_DEMONTHRES	5008 D82Ch	500C D82Ch	5000 E82Ch
C00h	32	EPWM_MINDBCFG	5008 DC00h	500C DC00h	5000 EC00h
C04h	32	EPWM_MINDBDLY	5008 DC04h	500C DC04h	5000 EC04h
C20h	32	EPWM_LUTCTLA	5008 DC20h	500C DC20h	5000 EC20h
C24h	32	EPWM_LUTCTLB	5008 DC24h	500C DC24h	5000 EC24h

Table 3-589. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM25_G1 Physical Address	EPWM26_G1 Physical Address	EPWM27_G1 Physical Address
0h	16	EPWM_TBCTL	5004 E000h	5008 E000h	500C E000h
2h	16	EPWM_TBCTL2	5004 E002h	5008 E002h	500C E002h
6h	16	EPWM_EPWMSYNCINSEL	5004 E006h	5008 E006h	500C E006h
8h	16	EPWM_TBCTR	5004 E008h	5008 E008h	500C E008h
Ah	16	EPWM_TBSTS	5004 E00Ah	5008 E00Ah	500C E00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5004 E00Ch	5008 E00Ch	500C E00Ch
Eh	16	EPWM_TBCTL3	5004 E00Eh	5008 E00Eh	500C E00Eh
10h	16	EPWM_CMPCTL	5004 E010h	5008 E010h	500C E010h
12h	16	EPWM_CMPCTL2	5004 E012h	5008 E012h	500C E012h
18h	16	EPWM_DBCTL	5004 E018h	5008 E018h	500C E018h
1Ah	16	EPWM_DBCTL2	5004 E01Ah	5008 E01Ah	500C E01Ah
20h	16	EPWM_AQCTL	5004 E020h	5008 E020h	500C E020h
22h	16	EPWM_AQTSRCSEL	5004 E022h	5008 E022h	500C E022h
28h	16	EPWM_PCCTL	5004 E028h	5008 E028h	500C E028h
30h	16	EPWM_VCAPCTL	5004 E030h	5008 E030h	500C E030h

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Table 3-589. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM25_G1 Physical Address	EPWM26_G1 Physical Address	EPWM27_G1 Physical Address
32h	16	EPWM_VCNTCFG	5004 E032h	5008 E032h	500C E032h
40h	16	EPWM_HRCNFG	5004 E040h	5008 E040h	500C E040h
4Eh	16	EPWM_HRCNFG2	5004 E04Eh	5008 E04Eh	500C E04Eh
5Ah	16	EPWM_HRPCTL	5004 E05Ah	5008 E05Ah	500C E05Ah
5Ch	16	EPWM_TRREM	5004 E05Ch	5008 E05Ch	500C E05Ch
68h	16	EPWM_GLDCTL	5004 E068h	5008 E068h	500C E068h
6Ah	16	EPWM_GLDCFG	5004 E06Ah	5008 E06Ah	500C E06Ah
70h	32	EPWM_EPWMXLINK	5004 E070h	5008 E070h	500C E070h
74h	32	EPWM_EPWMXLINK2	5004 E074h	5008 E074h	500C E074h
7Ah	16	EPWM_ETEST	5004 E07Ah	5008 E07Ah	500C E07Ah
7Ch	16	EPWM_EPWMREV	5004 E07Ch	5008 E07Ch	500C E07Ch
7Eh	16	EPWM_HRPWMREV	5004 E07Eh	5008 E07Eh	500C E07Eh
80h	16	EPWM_AQCTLA	5004 E080h	5008 E080h	500C E080h
82h	16	EPWM_AQCTLA2	5004 E082h	5008 E082h	500C E082h
84h	16	EPWM_AQCTLB	5004 E084h	5008 E084h	500C E084h
86h	16	EPWM_AQCTLB2	5004 E086h	5008 E086h	500C E086h
8Eh	16	EPWM_AQSFRC	5004 E08Eh	5008 E08Eh	500C E08Eh
92h	16	EPWM_AQCSFRC	5004 E092h	5008 E092h	500C E092h
A0h	16	EPWM_DBREDHR	5004 E0A0h	5008 E0A0h	500C E0A0h
A2h	16	EPWM_DBRED	5004 E0A2h	5008 E0A2h	500C E0A2h
A4h	16	EPWM_DBFEDHR	5004 E0A4h	5008 E0A4h	500C E0A4h
A6h	16	EPWM_DBFED	5004 E0A6h	5008 E0A6h	500C E0A6h
C0h	32	EPWM_TBPHS	5004 E0C0h	5008 E0C0h	500C E0C0h
C4h	16	EPWM_TBPRDHR	5004 E0C4h	5008 E0C4h	500C E0C4h
C6h	16	EPWM_TBPRD	5004 E0C6h	5008 E0C6h	500C E0C6h
C8h	16	EPWM_TBPRDHRB	5004 E0C8h	5008 E0C8h	500C E0C8h
D4h	32	EPWM_CMPA	5004 E0D4h	5008 E0D4h	500C E0D4h
D8h	32	EPWM_CMPB	5004 E0D8h	5008 E0D8h	500C E0D8h
DEh	16	EPWM_CMPC	5004 E0DEh	5008 E0DEh	500C E0DEh
E2h	16	EPWM_CMPD	5004 E0E2h	5008 E0E2h	500C E0E2h
E8h	16	EPWM_GLDCTL2	5004 E0E8h	5008 E0E8h	500C E0E8h
EEh	16	EPWM_SWVDELVAL	5004 E0EEh	5008 E0EEh	500C E0EEh
100h	16	EPWM_TZSEL	5004 E100h	5008 E100h	500C E100h
102h	16	EPWM_TZSEL2	5004 E102h	5008 E102h	500C E102h
104h	16	EPWM_TZDCSEL	5004 E104h	5008 E104h	500C E104h
108h	16	EPWM_TZCTL	5004 E108h	5008 E108h	500C E108h
10Ah	16	EPWM_TZCTL2	5004 E10Ah	5008 E10Ah	500C E10Ah
10Ch	16	EPWM_TZCTLDCA	5004 E10Ch	5008 E10Ch	500C E10Ch
10Eh	16	EPWM_TZCTLDCB	5004 E10Eh	5008 E10Eh	500C E10Eh
11Ah	16	EPWM_TZEINT	5004 E11Ah	5008 E11Ah	500C E11Ah
126h	16	EPWM_TZFLG	5004 E126h	5008 E126h	500C E126h
128h	16	EPWM_TZCBCFLG	5004 E128h	5008 E128h	500C E128h
12Ah	16	EPWM_TZOSTFLG	5004 E12Ah	5008 E12Ah	500C E12Ah
12Eh	16	EPWM_TZCLR	5004 E12Eh	5008 E12Eh	500C E12Eh
130h	16	EPWM_TZCBCCLR	5004 E130h	5008 E130h	500C E130h
132h	16	EPWM_TZOSTCLR	5004 E132h	5008 E132h	500C E132h

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Table 3-589. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM25_G1 Physical Address	EPWM26_G1 Physical Address	EPWM27_G1 Physical Address
136h	16	EPWM_TZFRC	5004 E136h	5008 E136h	500C E136h
13Ah	16	EPWM_TZTRIPOUTSEL	5004 E13Ah	5008 E13Ah	500C E13Ah
148h	16	EPWM_ETSEL	5004 E148h	5008 E148h	500C E148h
14Ch	16	EPWM_ETPS	5004 E14Ch	5008 E14Ch	500C E14Ch
150h	16	EPWM_ETFLG	5004 E150h	5008 E150h	500C E150h
154h	16	EPWM_ETCLR	5004 E154h	5008 E154h	500C E154h
158h	16	EPWM_ETFRC	5004 E158h	5008 E158h	500C E158h
15Ch	16	EPWM_ETINTPS	5004 E15Ch	5008 E15Ch	500C E15Ch
160h	16	EPWM_ETSOCPS	5004 E160h	5008 E160h	500C E160h
164h	16	EPWM_ETCNTINITCTL	5004 E164h	5008 E164h	500C E164h
168h	16	EPWM_ETCNTINIT	5004 E168h	5008 E168h	500C E168h
16Ch	16	EPWM_ETINTMIXEN	5004 E16Ch	5008 E16Ch	500C E16Ch
170h	16	EPWM_ETSOCAMIXEN	5004 E170h	5008 E170h	500C E170h
174h	16	EPWM_ETSOCBMIXEN	5004 E174h	5008 E174h	500C E174h
180h	16	EPWM_DCTRIPSEL	5004 E180h	5008 E180h	500C E180h
186h	16	EPWM_DCACTL	5004 E186h	5008 E186h	500C E186h
188h	16	EPWM_DCBCTL	5004 E188h	5008 E188h	500C E188h
18Eh	16	EPWM_DCFCTL	5004 E18Eh	5008 E18Eh	500C E18Eh
190h	16	EPWM_DCCAPCTL	5004 E190h	5008 E190h	500C E190h
192h	16	EPWM_DCFOFFSET	5004 E192h	5008 E192h	500C E192h
194h	16	EPWM_DCFOFFSETCNT	5004 E194h	5008 E194h	500C E194h
196h	16	EPWM_DCFWINDOW	5004 E196h	5008 E196h	500C E196h
198h	16	EPWM_DCFWINDOWCNT	5004 E198h	5008 E198h	500C E198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5004 E19Ah	5008 E19Ah	500C E19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5004 E19Ch	5008 E19Ch	500C E19Ch
19Eh	16	EPWM_DCCAP	5004 E19Eh	5008 E19Eh	500C E19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5004 E1A4h	5008 E1A4h	500C E1A4h
1A6h	16	EPWM_DCALTRIPSEL	5004 E1A6h	5008 E1A6h	500C E1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5004 E1A8h	5008 E1A8h	500C E1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5004 E1AAh	5008 E1AAh	500C E1AAh
1ACh	16	EPWM_CAPCTL	5004 E1ACh	5008 E1ACh	500C E1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5004 E1AEh	5008 E1AEh	500C E1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5004 E1B0h	5008 E1B0h	500C E1B0h
1B2h	16	EPWM_CAPTRIPSEL	5004 E1B2h	5008 E1B2h	500C E1B2h
1F4h	32	EPWM_EPWMLOCK	5004 E1F4h	5008 E1F4h	500C E1F4h
1FAh	16	EPWM_HWVDELVAL	5004 E1FAh	5008 E1FAh	500C E1FAh
1FCh	16	EPWM_VCNTVAL	5004 E1FCh	5008 E1FCh	500C E1FCh
400h	32	EPWM_XCMPCTL1	5004 E400h	5008 E400h	500C E400h
410h	32	EPWM_XLOADCTL	5004 E410h	5008 E410h	500C E410h
418h	32	EPWM_XLOAD	5004 E418h	5008 E418h	500C E418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5004 E41Ch	5008 E41Ch	500C E41Ch
420h	32	EPWM_XREGSHDW1STS	5004 E420h	5008 E420h	500C E420h
428h	32	EPWM_XREGSHDW2STS	5004 E428h	5008 E428h	500C E428h
430h	32	EPWM_XREGSHDW3STS	5004 E430h	5008 E430h	500C E430h
600h	32	EPWM_XCMP1_ACTIVE	5004 E600h	5008 E600h	500C E600h
604h	32	EPWM_XCMP2_ACTIVE	5004 E604h	5008 E604h	500C E604h

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Table 3-589. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM25_G1 Physical Address	EPWM26_G1 Physical Address	EPWM27_G1 Physical Address
608h	32	EPWM_XCMP3_ACTIVE	5004 E608h	5008 E608h	500C E608h
60Ch	32	EPWM_XCMP4_ACTIVE	5004 E60Ch	5008 E60Ch	500C E60Ch
610h	32	EPWM_XCMP5_ACTIVE	5004 E610h	5008 E610h	500C E610h
614h	32	EPWM_XCMP6_ACTIVE	5004 E614h	5008 E614h	500C E614h
618h	32	EPWM_XCMP7_ACTIVE	5004 E618h	5008 E618h	500C E618h
61Ch	32	EPWM_XCMP8_ACTIVE	5004 E61Ch	5008 E61Ch	500C E61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5004 E620h	5008 E620h	500C E620h
630h	16	EPWM_XAQCTLA_ACTIVE	5004 E630h	5008 E630h	500C E630h
644h	32	EPWM_XMINMAX_ACTIVE	5004 E644h	5008 E644h	500C E644h
680h	32	EPWM_XCMP1_SHDW1	5004 E680h	5008 E680h	500C E680h
684h	32	EPWM_XCMP2_SHDW1	5004 E684h	5008 E684h	500C E684h
688h	32	EPWM_XCMP3_SHDW1	5004 E688h	5008 E688h	500C E688h
68Ch	32	EPWM_XCMP4_SHDW1	5004 E68Ch	5008 E68Ch	500C E68Ch
690h	32	EPWM_XCMP5_SHDW1	5004 E690h	5008 E690h	500C E690h
694h	32	EPWM_XCMP6_SHDW1	5004 E694h	5008 E694h	500C E694h
698h	32	EPWM_XCMP7_SHDW1	5004 E698h	5008 E698h	500C E698h
69Ch	32	EPWM_XCMP8_SHDW1	5004 E69Ch	5008 E69Ch	500C E69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5004 E6A0h	5008 E6A0h	500C E6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5004 E6B0h	5008 E6B0h	500C E6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5004 E6B2h	5008 E6B2h	500C E6B2h
6BAh	16	EPWM_CMPC_SHDW1	5004 E6BAh	5008 E6BAh	500C E6BAh
6BEh	16	EPWM_CMPD_SHDW1	5004 E6BEh	5008 E6BEh	500C E6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5004 E6C4h	5008 E6C4h	500C E6C4h
700h	32	EPWM_XCMP1_SHDW2	5004 E700h	5008 E700h	500C E700h
704h	32	EPWM_XCMP2_SHDW2	5004 E704h	5008 E704h	500C E704h
708h	32	EPWM_XCMP3_SHDW2	5004 E708h	5008 E708h	500C E708h
70Ch	32	EPWM_XCMP4_SHDW2	5004 E70Ch	5008 E70Ch	500C E70Ch
710h	32	EPWM_XCMP5_SHDW2	5004 E710h	5008 E710h	500C E710h
714h	32	EPWM_XCMP6_SHDW2	5004 E714h	5008 E714h	500C E714h
718h	32	EPWM_XCMP7_SHDW2	5004 E718h	5008 E718h	500C E718h
71Ch	32	EPWM_XCMP8_SHDW2	5004 E71Ch	5008 E71Ch	500C E71Ch
720h	32	EPWM_XTBPRD_SHDW2	5004 E720h	5008 E720h	500C E720h
730h	16	EPWM_XAQCTLA_SHDW2	5004 E730h	5008 E730h	500C E730h
732h	16	EPWM_XAQCTLB_SHDW2	5004 E732h	5008 E732h	500C E732h
73Ah	16	EPWM_CMPC_SHDW2	5004 E73Ah	5008 E73Ah	500C E73Ah
73Eh	16	EPWM_CMPD_SHDW2	5004 E73Eh	5008 E73Eh	500C E73Eh
744h	32	EPWM_XMINMAX_SHDW2	5004 E744h	5008 E744h	500C E744h
780h	32	EPWM_XCMP1_SHDW3	5004 E780h	5008 E780h	500C E780h
784h	32	EPWM_XCMP2_SHDW3	5004 E784h	5008 E784h	500C E784h
788h	32	EPWM_XCMP3_SHDW3	5004 E788h	5008 E788h	500C E788h
78Ch	32	EPWM_XCMP4_SHDW3	5004 E78Ch	5008 E78Ch	500C E78Ch
790h	32	EPWM_XCMP5_SHDW3	5004 E790h	5008 E790h	500C E790h
794h	32	EPWM_XCMP6_SHDW3	5004 E794h	5008 E794h	500C E794h
798h	32	EPWM_XCMP7_SHDW3	5004 E798h	5008 E798h	500C E798h
79Ch	32	EPWM_XCMP8_SHDW3	5004 E79Ch	5008 E79Ch	500C E79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5004 E7A0h	5008 E7A0h	500C E7A0h

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Table 3-589. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM25_G1 Physical Address	EPWM26_G1 Physical Address	EPWM27_G1 Physical Address
7B0h	16	EPWM_XAQCTLA_SHDW3	5004 E7B0h	5008 E7B0h	500C E7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5004 E7B2h	5008 E7B2h	500C E7B2h
7BAh	16	EPWM_CMPC_SHDW3	5004 E7BAh	5008 E7BAh	500C E7BAh
7BEh	16	EPWM_CMPD_SHDW3	5004 E7BEh	5008 E7BEh	500C E7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5004 E7C4h	5008 E7C4h	500C E7C4h
800h	32	EPWM_DECTL	5004 E800h	5008 E800h	500C E800h
804h	32	EPWM_DECOMPSEL	5004 E804h	5008 E804h	500C E804h
808h	32	EPWM_DEACTCTL	5004 E808h	5008 E808h	500C E808h
80Ch	32	EPWM_DESTS	5004 E80Ch	5008 E80Ch	500C E80Ch
810h	32	EPWM_DEFRC	5004 E810h	5008 E810h	500C E810h
814h	32	EPWM_DECLR	5004 E814h	5008 E814h	500C E814h
820h	32	EPWM_DEMONCNT	5004 E820h	5008 E820h	500C E820h
824h	32	EPWM_DEMONCTL	5004 E824h	5008 E824h	500C E824h
828h	32	EPWM_DEMONSTEP	5004 E828h	5008 E828h	500C E828h
82Ch	32	EPWM_DEMONTHRES	5004 E82Ch	5008 E82Ch	500C E82Ch
C00h	32	EPWM_MINDBCFG	5004 EC00h	5008 EC00h	500C EC00h
C04h	32	EPWM_MINDBDLY	5004 EC04h	5008 EC04h	500C EC04h
C20h	32	EPWM_LUTCTLA	5004 EC20h	5008 EC20h	500C EC20h
C24h	32	EPWM_LUTCTLB	5004 EC24h	5008 EC24h	500C EC24h

Table 3-590. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM28_G1 Physical Address	EPWM29_G1 Physical Address	EPWM30_G1 Physical Address
0h	16	EPWM_TBCTL	5000 F000h	5004 F000h	5008 F000h
2h	16	EPWM_TBCTL2	5000 F002h	5004 F002h	5008 F002h
6h	16	EPWM_EPWMSYNCINSEL	5000 F006h	5004 F006h	5008 F006h
8h	16	EPWM_TBCTR	5000 F008h	5004 F008h	5008 F008h
Ah	16	EPWM_TBSTS	5000 F00Ah	5004 F00Ah	5008 F00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5000 F00Ch	5004 F00Ch	5008 F00Ch
Eh	16	EPWM_TBCTL3	5000 F00Eh	5004 F00Eh	5008 F00Eh
10h	16	EPWM_CMPCTL	5000 F010h	5004 F010h	5008 F010h
12h	16	EPWM_CMPCTL2	5000 F012h	5004 F012h	5008 F012h
18h	16	EPWM_DBCTL	5000 F018h	5004 F018h	5008 F018h
1Ah	16	EPWM_DBCTL2	5000 F01Ah	5004 F01Ah	5008 F01Ah
20h	16	EPWM_AQCTL	5000 F020h	5004 F020h	5008 F020h
22h	16	EPWM_AQTSRCSEL	5000 F022h	5004 F022h	5008 F022h
28h	16	EPWM_PCCTL	5000 F028h	5004 F028h	5008 F028h
30h	16	EPWM_VCAPCTL	5000 F030h	5004 F030h	5008 F030h
32h	16	EPWM_VCNTCFG	5000 F032h	5004 F032h	5008 F032h
40h	16	EPWM_HRCNFG	5000 F040h	5004 F040h	5008 F040h
4Eh	16	EPWM_HRCNFG2	5000 F04Eh	5004 F04Eh	5008 F04Eh
5Ah	16	EPWM_HRPCTL	5000 F05Ah	5004 F05Ah	5008 F05Ah
5Ch	16	EPWM_TRREM	5000 F05Ch	5004 F05Ch	5008 F05Ch
68h	16	EPWM_GLDCTL	5000 F068h	5004 F068h	5008 F068h
6Ah	16	EPWM_GLDCFG	5000 F06Ah	5004 F06Ah	5008 F06Ah
70h	32	EPWM_EPWMXLINK	5000 F070h	5004 F070h	5008 F070h

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Table 3-590. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM28_G1 Physical Address	EPWM29_G1 Physical Address	EPWM30_G1 Physical Address
74h	32	EPWM_EPWMXLINK2	5000 F074h	5004 F074h	5008 F074h
7Ah	16	EPWM_ETEST	5000 F07Ah	5004 F07Ah	5008 F07Ah
7Ch	16	EPWM_EPWMREV	5000 F07Ch	5004 F07Ch	5008 F07Ch
7Eh	16	EPWM_HRPWMREV	5000 F07Eh	5004 F07Eh	5008 F07Eh
80h	16	EPWM_AQCTLA	5000 F080h	5004 F080h	5008 F080h
82h	16	EPWM_AQCTLA2	5000 F082h	5004 F082h	5008 F082h
84h	16	EPWM_AQCTLB	5000 F084h	5004 F084h	5008 F084h
86h	16	EPWM_AQCTLB2	5000 F086h	5004 F086h	5008 F086h
8Eh	16	EPWM_AQSFRC	5000 F08Eh	5004 F08Eh	5008 F08Eh
92h	16	EPWM_AQCSFRC	5000 F092h	5004 F092h	5008 F092h
A0h	16	EPWM_DBREDHR	5000 F0A0h	5004 F0A0h	5008 F0A0h
A2h	16	EPWM_DBRED	5000 F0A2h	5004 F0A2h	5008 F0A2h
A4h	16	EPWM_DBFEDHR	5000 F0A4h	5004 F0A4h	5008 F0A4h
A6h	16	EPWM_DBFED	5000 F0A6h	5004 F0A6h	5008 F0A6h
C0h	32	EPWM_TBPHS	5000 F0C0h	5004 F0C0h	5008 F0C0h
C4h	16	EPWM_TBPRDHR	5000 F0C4h	5004 F0C4h	5008 F0C4h
C6h	16	EPWM_TBPRD	5000 F0C6h	5004 F0C6h	5008 F0C6h
C8h	16	EPWM_TBPRDHRB	5000 F0C8h	5004 F0C8h	5008 F0C8h
D4h	32	EPWM_CMPA	5000 F0D4h	5004 F0D4h	5008 F0D4h
D8h	32	EPWM_CMPB	5000 F0D8h	5004 F0D8h	5008 F0D8h
DEh	16	EPWM_CMPC	5000 F0DEh	5004 F0DEh	5008 F0DEh
E2h	16	EPWM_CMPD	5000 F0E2h	5004 F0E2h	5008 F0E2h
E8h	16	EPWM_GLDCTL2	5000 F0E8h	5004 F0E8h	5008 F0E8h
EEh	16	EPWM_SWVDELVAL	5000 F0EEh	5004 F0EEh	5008 F0EEh
100h	16	EPWM_TZSEL	5000 F100h	5004 F100h	5008 F100h
102h	16	EPWM_TZSEL2	5000 F102h	5004 F102h	5008 F102h
104h	16	EPWM_TZDCSEL	5000 F104h	5004 F104h	5008 F104h
108h	16	EPWM_TZCTL	5000 F108h	5004 F108h	5008 F108h
10Ah	16	EPWM_TZCTL2	5000 F10Ah	5004 F10Ah	5008 F10Ah
10Ch	16	EPWM_TZCTLDCA	5000 F10Ch	5004 F10Ch	5008 F10Ch
10Eh	16	EPWM_TZCTLDCB	5000 F10Eh	5004 F10Eh	5008 F10Eh
11Ah	16	EPWM_TZEINT	5000 F11Ah	5004 F11Ah	5008 F11Ah
126h	16	EPWM_TZFLG	5000 F126h	5004 F126h	5008 F126h
128h	16	EPWM_TZCBCFLG	5000 F128h	5004 F128h	5008 F128h
12Ah	16	EPWM_TZOSTFLG	5000 F12Ah	5004 F12Ah	5008 F12Ah
12Eh	16	EPWM_TZCLR	5000 F12Eh	5004 F12Eh	5008 F12Eh
130h	16	EPWM_TZCBCCLR	5000 F130h	5004 F130h	5008 F130h
132h	16	EPWM_TZOSTCLR	5000 F132h	5004 F132h	5008 F132h
136h	16	EPWM_TZFRC	5000 F136h	5004 F136h	5008 F136h
13Ah	16	EPWM_TZTRIPOUTSEL	5000 F13Ah	5004 F13Ah	5008 F13Ah
148h	16	EPWM_ETSEL	5000 F148h	5004 F148h	5008 F148h
14Ch	16	EPWM_ETPS	5000 F14Ch	5004 F14Ch	5008 F14Ch
150h	16	EPWM_ETFLG	5000 F150h	5004 F150h	5008 F150h
154h	16	EPWM_ETCLR	5000 F154h	5004 F154h	5008 F154h
158h	16	EPWM_ETFRC	5000 F158h	5004 F158h	5008 F158h
15Ch	16	EPWM_ETINTPS	5000 F15Ch	5004 F15Ch	5008 F15Ch

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Table 3-590. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM28_G1 Physical Address	EPWM29_G1 Physical Address	EPWM30_G1 Physical Address
160h	16	EPWM_ETSOCPS	5000 F160h	5004 F160h	5008 F160h
164h	16	EPWM_ETCNTINITCTL	5000 F164h	5004 F164h	5008 F164h
168h	16	EPWM_ETCNTINIT	5000 F168h	5004 F168h	5008 F168h
16Ch	16	EPWM_ETINTMIXEN	5000 F16Ch	5004 F16Ch	5008 F16Ch
170h	16	EPWM_ETSOCAMIXEN	5000 F170h	5004 F170h	5008 F170h
174h	16	EPWM_ETSOCBMIXEN	5000 F174h	5004 F174h	5008 F174h
180h	16	EPWM_DCTRIPSEL	5000 F180h	5004 F180h	5008 F180h
186h	16	EPWM_DCACTL	5000 F186h	5004 F186h	5008 F186h
188h	16	EPWM_DCBCTL	5000 F188h	5004 F188h	5008 F188h
18Eh	16	EPWM_DCFCTL	5000 F18Eh	5004 F18Eh	5008 F18Eh
190h	16	EPWM_DCCAPCTL	5000 F190h	5004 F190h	5008 F190h
192h	16	EPWM_DCFOFFSET	5000 F192h	5004 F192h	5008 F192h
194h	16	EPWM_DCFOFFSETCNT	5000 F194h	5004 F194h	5008 F194h
196h	16	EPWM_DCFWINDOW	5000 F196h	5004 F196h	5008 F196h
198h	16	EPWM_DCFWINDOWCNT	5000 F198h	5004 F198h	5008 F198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5000 F19Ah	5004 F19Ah	5008 F19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5000 F19Ch	5004 F19Ch	5008 F19Ch
19Eh	16	EPWM_DCCAP	5000 F19Eh	5004 F19Eh	5008 F19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5000 F1A4h	5004 F1A4h	5008 F1A4h
1A6h	16	EPWM_DCALTRIPSEL	5000 F1A6h	5004 F1A6h	5008 F1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5000 F1A8h	5004 F1A8h	5008 F1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5000 F1AAh	5004 F1AAh	5008 F1AAh
1ACh	16	EPWM_CAPCTL	5000 F1ACh	5004 F1ACh	5008 F1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5000 F1AEh	5004 F1AEh	5008 F1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5000 F1B0h	5004 F1B0h	5008 F1B0h
1B2h	16	EPWM_CAPTRIPSEL	5000 F1B2h	5004 F1B2h	5008 F1B2h
1F4h	32	EPWM_EPWMLOCK	5000 F1F4h	5004 F1F4h	5008 F1F4h
1FAh	16	EPWM_HWVDELVAL	5000 F1FAh	5004 F1FAh	5008 F1FAh
1FCh	16	EPWM_VCNTVAL	5000 F1FCh	5004 F1FCh	5008 F1FCh
400h	32	EPWM_XCMPCTL1	5000 F400h	5004 F400h	5008 F400h
410h	32	EPWM_XLOADCTL	5000 F410h	5004 F410h	5008 F410h
418h	32	EPWM_XLOAD	5000 F418h	5004 F418h	5008 F418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5000 F41Ch	5004 F41Ch	5008 F41Ch
420h	32	EPWM_XREGSHDW1STS	5000 F420h	5004 F420h	5008 F420h
428h	32	EPWM_XREGSHDW2STS	5000 F428h	5004 F428h	5008 F428h
430h	32	EPWM_XREGSHDW3STS	5000 F430h	5004 F430h	5008 F430h
600h	32	EPWM_XCMP1_ACTIVE	5000 F600h	5004 F600h	5008 F600h
604h	32	EPWM_XCMP2_ACTIVE	5000 F604h	5004 F604h	5008 F604h
608h	32	EPWM_XCMP3_ACTIVE	5000 F608h	5004 F608h	5008 F608h
60Ch	32	EPWM_XCMP4_ACTIVE	5000 F60Ch	5004 F60Ch	5008 F60Ch
610h	32	EPWM_XCMP5_ACTIVE	5000 F610h	5004 F610h	5008 F610h
614h	32	EPWM_XCMP6_ACTIVE	5000 F614h	5004 F614h	5008 F614h
618h	32	EPWM_XCMP7_ACTIVE	5000 F618h	5004 F618h	5008 F618h
61Ch	32	EPWM_XCMP8_ACTIVE	5000 F61Ch	5004 F61Ch	5008 F61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5000 F620h	5004 F620h	5008 F620h
630h	16	EPWM_XAQCTLA_ACTIVE	5000 F630h	5004 F630h	5008 F630h

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Table 3-590. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM28_G1 Physical Address	EPWM29_G1 Physical Address	EPWM30_G1 Physical Address
644h	32	EPWM_XMINMAX_ACTIVE	5000 F644h	5004 F644h	5008 F644h
680h	32	EPWM_XCMP1_SHDW1	5000 F680h	5004 F680h	5008 F680h
684h	32	EPWM_XCMP2_SHDW1	5000 F684h	5004 F684h	5008 F684h
688h	32	EPWM_XCMP3_SHDW1	5000 F688h	5004 F688h	5008 F688h
68Ch	32	EPWM_XCMP4_SHDW1	5000 F68Ch	5004 F68Ch	5008 F68Ch
690h	32	EPWM_XCMP5_SHDW1	5000 F690h	5004 F690h	5008 F690h
694h	32	EPWM_XCMP6_SHDW1	5000 F694h	5004 F694h	5008 F694h
698h	32	EPWM_XCMP7_SHDW1	5000 F698h	5004 F698h	5008 F698h
69Ch	32	EPWM_XCMP8_SHDW1	5000 F69Ch	5004 F69Ch	5008 F69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5000 F6A0h	5004 F6A0h	5008 F6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5000 F6B0h	5004 F6B0h	5008 F6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5000 F6B2h	5004 F6B2h	5008 F6B2h
6BAh	16	EPWM_CMPC_SHDW1	5000 F6BAh	5004 F6BAh	5008 F6BAh
6BEh	16	EPWM_CMPD_SHDW1	5000 F6BEh	5004 F6BEh	5008 F6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5000 F6C4h	5004 F6C4h	5008 F6C4h
700h	32	EPWM_XCMP1_SHDW2	5000 F700h	5004 F700h	5008 F700h
704h	32	EPWM_XCMP2_SHDW2	5000 F704h	5004 F704h	5008 F704h
708h	32	EPWM_XCMP3_SHDW2	5000 F708h	5004 F708h	5008 F708h
70Ch	32	EPWM_XCMP4_SHDW2	5000 F70Ch	5004 F70Ch	5008 F70Ch
710h	32	EPWM_XCMP5_SHDW2	5000 F710h	5004 F710h	5008 F710h
714h	32	EPWM_XCMP6_SHDW2	5000 F714h	5004 F714h	5008 F714h
718h	32	EPWM_XCMP7_SHDW2	5000 F718h	5004 F718h	5008 F718h
71Ch	32	EPWM_XCMP8_SHDW2	5000 F71Ch	5004 F71Ch	5008 F71Ch
720h	32	EPWM_XTBPRD_SHDW2	5000 F720h	5004 F720h	5008 F720h
730h	16	EPWM_XAQCTLA_SHDW2	5000 F730h	5004 F730h	5008 F730h
732h	16	EPWM_XAQCTLB_SHDW2	5000 F732h	5004 F732h	5008 F732h
73Ah	16	EPWM_CMPC_SHDW2	5000 F73Ah	5004 F73Ah	5008 F73Ah
73Eh	16	EPWM_CMPD_SHDW2	5000 F73Eh	5004 F73Eh	5008 F73Eh
744h	32	EPWM_XMINMAX_SHDW2	5000 F744h	5004 F744h	5008 F744h
780h	32	EPWM_XCMP1_SHDW3	5000 F780h	5004 F780h	5008 F780h
784h	32	EPWM_XCMP2_SHDW3	5000 F784h	5004 F784h	5008 F784h
788h	32	EPWM_XCMP3_SHDW3	5000 F788h	5004 F788h	5008 F788h
78Ch	32	EPWM_XCMP4_SHDW3	5000 F78Ch	5004 F78Ch	5008 F78Ch
790h	32	EPWM_XCMP5_SHDW3	5000 F790h	5004 F790h	5008 F790h
794h	32	EPWM_XCMP6_SHDW3	5000 F794h	5004 F794h	5008 F794h
798h	32	EPWM_XCMP7_SHDW3	5000 F798h	5004 F798h	5008 F798h
79Ch	32	EPWM_XCMP8_SHDW3	5000 F79Ch	5004 F79Ch	5008 F79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5000 F7A0h	5004 F7A0h	5008 F7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5000 F7B0h	5004 F7B0h	5008 F7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5000 F7B2h	5004 F7B2h	5008 F7B2h
7BAh	16	EPWM_CMPC_SHDW3	5000 F7BAh	5004 F7BAh	5008 F7BAh
7BEh	16	EPWM_CMPD_SHDW3	5000 F7BEh	5004 F7BEh	5008 F7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5000 F7C4h	5004 F7C4h	5008 F7C4h
800h	32	EPWM_DECTL	5000 F800h	5004 F800h	5008 F800h
804h	32	EPWM_DECOMPSEL	5000 F804h	5004 F804h	5008 F804h
808h	32	EPWM_DEACTCTL	5000 F808h	5004 F808h	5008 F808h

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Table 3-590. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM28_G1 Physical Address	EPWM29_G1 Physical Address	EPWM30_G1 Physical Address
80Ch	32	EPWM_DESTS	5000 F80Ch	5004 F80Ch	5008 F80Ch
810h	32	EPWM_DEFRC	5000 F810h	5004 F810h	5008 F810h
814h	32	EPWM_DECLR	5000 F814h	5004 F814h	5008 F814h
820h	32	EPWM_DEMONCNT	5000 F820h	5004 F820h	5008 F820h
824h	32	EPWM_DEMONCTL	5000 F824h	5004 F824h	5008 F824h
828h	32	EPWM_DEMONSTEP	5000 F828h	5004 F828h	5008 F828h
82Ch	32	EPWM_DEMONTHRES	5000 F82Ch	5004 F82Ch	5008 F82Ch
C00h	32	EPWM_MINDBCFG	5000 FC00h	5004 FC00h	5008 FC00h
C04h	32	EPWM_MINDBDLY	5000 FC04h	5004 FC04h	5008 FC04h
C20h	32	EPWM_LUTCTLA	5000 FC20h	5004 FC20h	5008 FC20h
C24h	32	EPWM_LUTCTLB	5000 FC24h	5004 FC24h	5008 FC24h

Table 3-591. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM31_G1 Physical Address	EPWM00_G2 Physical Address	EPWM01_G2 Physical Address
0h	16	EPWM_TBCTL	500C F000h	5001 0000h	5005 0000h
2h	16	EPWM_TBCTL2	500C F002h	5001 0002h	5005 0002h
6h	16	EPWM_EPWMSYNCINSEL	500C F006h	5001 0006h	5005 0006h
8h	16	EPWM_TBCTR	500C F008h	5001 0008h	5005 0008h
Ah	16	EPWM_TBSTS	500C F00Ah	5001 000Ah	5005 000Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500C F00Ch	5001 000Ch	5005 000Ch
Eh	16	EPWM_TBCTL3	500C F00Eh	5001 000Eh	5005 000Eh
10h	16	EPWM_CMPCTL	500C F010h	5001 0010h	5005 0010h
12h	16	EPWM_CMPCTL2	500C F012h	5001 0012h	5005 0012h
18h	16	EPWM_DBCTL	500C F018h	5001 0018h	5005 0018h
1Ah	16	EPWM_DBCTL2	500C F01Ah	5001 001Ah	5005 001Ah
20h	16	EPWM_AQCTL	500C F020h	5001 0020h	5005 0020h
22h	16	EPWM_AQTSRCSEL	500C F022h	5001 0022h	5005 0022h
28h	16	EPWM_PCCTL	500C F028h	5001 0028h	5005 0028h
30h	16	EPWM_VCAPCTL	500C F030h	5001 0030h	5005 0030h
32h	16	EPWM_VCNTCFG	500C F032h	5001 0032h	5005 0032h
40h	16	EPWM_HRCNFG	500C F040h	5001 0040h	5005 0040h
4Eh	16	EPWM_HRCNFG2	500C F04Eh	5001 004Eh	5005 004Eh
5Ah	16	EPWM_HRPCTL	500C F05Ah	5001 005Ah	5005 005Ah
5Ch	16	EPWM_TRREM	500C F05Ch	5001 005Ch	5005 005Ch
68h	16	EPWM_GLDCTL	500C F068h	5001 0068h	5005 0068h
6Ah	16	EPWM_GLDCFG	500C F06Ah	5001 006Ah	5005 006Ah
70h	32	EPWM_EPWMXLINK	500C F070h	5001 0070h	5005 0070h
74h	32	EPWM_EPWMXLINK2	500C F074h	5001 0074h	5005 0074h
7Ah	16	EPWM_ETEST	500C F07Ah	5001 007Ah	5005 007Ah
7Ch	16	EPWM_EPWMREV	500C F07Ch	5001 007Ch	5005 007Ch
7Eh	16	EPWM_HRPWMREV	500C F07Eh	5001 007Eh	5005 007Eh
80h	16	EPWM_AQCTLA	500C F080h	5001 0080h	5005 0080h
82h	16	EPWM_AQCTLA2	500C F082h	5001 0082h	5005 0082h
84h	16	EPWM_AQCTLB	500C F084h	5001 0084h	5005 0084h
86h	16	EPWM_AQCTLB2	500C F086h	5001 0086h	5005 0086h

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Table 3-591. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM31_G1 Physical Address	EPWM00_G2 Physical Address	EPWM01_G2 Physical Address
8Eh	16	EPWM_AQSFRC	500C F08Eh	5001 008Eh	5005 008Eh
92h	16	EPWM_AQCSFRC	500C F092h	5001 0092h	5005 0092h
A0h	16	EPWM_DBREDHR	500C F0A0h	5001 00A0h	5005 00A0h
A2h	16	EPWM_DBRED	500C F0A2h	5001 00A2h	5005 00A2h
A4h	16	EPWM_DBFEDHR	500C F0A4h	5001 00A4h	5005 00A4h
A6h	16	EPWM_DBFED	500C F0A6h	5001 00A6h	5005 00A6h
C0h	32	EPWM_TBPHS	500C F0C0h	5001 00C0h	5005 00C0h
C4h	16	EPWM_TBPRDHR	500C F0C4h	5001 00C4h	5005 00C4h
C6h	16	EPWM_TBPRD	500C F0C6h	5001 00C6h	5005 00C6h
C8h	16	EPWM_TBPRDHRB	500C F0C8h	5001 00C8h	5005 00C8h
D4h	32	EPWM_CMPA	500C F0D4h	5001 00D4h	5005 00D4h
D8h	32	EPWM_CMPB	500C F0D8h	5001 00D8h	5005 00D8h
DEh	16	EPWM_CMPC	500C F0DEh	5001 00DEh	5005 00DEh
E2h	16	EPWM_CMPD	500C F0E2h	5001 00E2h	5005 00E2h
E8h	16	EPWM_GLDCTL2	500C F0E8h	5001 00E8h	5005 00E8h
EEh	16	EPWM_SWVDELVAL	500C F0EEh	5001 00EEh	5005 00EEh
100h	16	EPWM_TZSEL	500C F100h	5001 0100h	5005 0100h
102h	16	EPWM_TZSEL2	500C F102h	5001 0102h	5005 0102h
104h	16	EPWM_TZDCSEL	500C F104h	5001 0104h	5005 0104h
108h	16	EPWM_TZCTL	500C F108h	5001 0108h	5005 0108h
10Ah	16	EPWM_TZCTL2	500C F10Ah	5001 010Ah	5005 010Ah
10Ch	16	EPWM_TZCTLDCA	500C F10Ch	5001 010Ch	5005 010Ch
10Eh	16	EPWM_TZCTLDCB	500C F10Eh	5001 010Eh	5005 010Eh
11Ah	16	EPWM_TZEINT	500C F11Ah	5001 011Ah	5005 011Ah
126h	16	EPWM_TZFLG	500C F126h	5001 0126h	5005 0126h
128h	16	EPWM_TZCBCFLG	500C F128h	5001 0128h	5005 0128h
12Ah	16	EPWM_TZOSTFLG	500C F12Ah	5001 012Ah	5005 012Ah
12Eh	16	EPWM_TZCLR	500C F12Eh	5001 012Eh	5005 012Eh
130h	16	EPWM_TZCBCCLR	500C F130h	5001 0130h	5005 0130h
132h	16	EPWM_TZOSTCLR	500C F132h	5001 0132h	5005 0132h
136h	16	EPWM_TZFRC	500C F136h	5001 0136h	5005 0136h
13Ah	16	EPWM_TZTRIPOUTSEL	500C F13Ah	5001 013Ah	5005 013Ah
148h	16	EPWM_ETSEL	500C F148h	5001 0148h	5005 0148h
14Ch	16	EPWM_ETPS	500C F14Ch	5001 014Ch	5005 014Ch
150h	16	EPWM_ETFLG	500C F150h	5001 0150h	5005 0150h
154h	16	EPWM_ETCLR	500C F154h	5001 0154h	5005 0154h
158h	16	EPWM_ETFRC	500C F158h	5001 0158h	5005 0158h
15Ch	16	EPWM_ETINTPS	500C F15Ch	5001 015Ch	5005 015Ch
160h	16	EPWM_ETSOCPS	500C F160h	5001 0160h	5005 0160h
164h	16	EPWM_ETCNTINITCTL	500C F164h	5001 0164h	5005 0164h
168h	16	EPWM_ETCNTINIT	500C F168h	5001 0168h	5005 0168h
16Ch	16	EPWM_ETINTMIXEN	500C F16Ch	5001 016Ch	5005 016Ch
170h	16	EPWM_ETSOCAMIXEN	500C F170h	5001 0170h	5005 0170h
174h	16	EPWM_ETSOCBMIXEN	500C F174h	5001 0174h	5005 0174h
180h	16	EPWM_DCTRIPSEL	500C F180h	5001 0180h	5005 0180h
186h	16	EPWM_DCACTL	500C F186h	5001 0186h	5005 0186h

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Table 3-591. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM31_G1 Physical Address	EPWM00_G2 Physical Address	EPWM01_G2 Physical Address
188h	16	EPWM_DCBCTL	500C F188h	5001 0188h	5005 0188h
18Eh	16	EPWM_DCFCTL	500C F18Eh	5001 018Eh	5005 018Eh
190h	16	EPWM_DCCAPCTL	500C F190h	5001 0190h	5005 0190h
192h	16	EPWM_DCFOFFSET	500C F192h	5001 0192h	5005 0192h
194h	16	EPWM_DCFOFFSETCNT	500C F194h	5001 0194h	5005 0194h
196h	16	EPWM_DCFWINDOW	500C F196h	5001 0196h	5005 0196h
198h	16	EPWM_DCFWINDOWCNT	500C F198h	5001 0198h	5005 0198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500C F19Ah	5001 019Ah	5005 019Ah
19Ch	16	EPWM_DCCAPMIXSEL	500C F19Ch	5001 019Ch	5005 019Ch
19Eh	16	EPWM_DCCAP	500C F19Eh	5001 019Eh	5005 019Eh
1A4h	16	EPWM_DCAHTRIPSEL	500C F1A4h	5001 01A4h	5005 01A4h
1A6h	16	EPWM_DCALTRIPSEL	500C F1A6h	5001 01A6h	5005 01A6h
1A8h	16	EPWM_DCBHTRIPSEL	500C F1A8h	5001 01A8h	5005 01A8h
1AAh	16	EPWM_DCBLTRIPSEL	500C F1AAh	5001 01AAh	5005 01AAh
1ACh	16	EPWM_CAPCTL	500C F1ACh	5001 01ACh	5005 01ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500C F1AEh	5001 01AEh	5005 01AEh
1B0h	16	EPWM_CAPINTRIPSEL	500C F1B0h	5001 01B0h	5005 01B0h
1B2h	16	EPWM_CAPTRIPSEL	500C F1B2h	5001 01B2h	5005 01B2h
1F4h	32	EPWM_EPWMLOCK	500C F1F4h	5001 01F4h	5005 01F4h
1FAh	16	EPWM_HWVDELVAL	500C F1FAh	5001 01FAh	5005 01FAh
1FCh	16	EPWM_VCNTVAL	500C F1FCh	5001 01FCh	5005 01FCh
400h	32	EPWM_XCMPCTL1	500C F400h	5001 0400h	5005 0400h
410h	32	EPWM_XLOADCTL	500C F410h	5001 0410h	5005 0410h
418h	32	EPWM_XLOAD	500C F418h	5001 0418h	5005 0418h
41Ch	32	EPWM_EPWMXLINKXLOAD	500C F41Ch	5001 041Ch	5005 041Ch
420h	32	EPWM_XREGSHDW1STS	500C F420h	5001 0420h	5005 0420h
428h	32	EPWM_XREGSHDW2STS	500C F428h	5001 0428h	5005 0428h
430h	32	EPWM_XREGSHDW3STS	500C F430h	5001 0430h	5005 0430h
600h	32	EPWM_XCMP1_ACTIVE	500C F600h	5001 0600h	5005 0600h
604h	32	EPWM_XCMP2_ACTIVE	500C F604h	5001 0604h	5005 0604h
608h	32	EPWM_XCMP3_ACTIVE	500C F608h	5001 0608h	5005 0608h
60Ch	32	EPWM_XCMP4_ACTIVE	500C F60Ch	5001 060Ch	5005 060Ch
610h	32	EPWM_XCMP5_ACTIVE	500C F610h	5001 0610h	5005 0610h
614h	32	EPWM_XCMP6_ACTIVE	500C F614h	5001 0614h	5005 0614h
618h	32	EPWM_XCMP7_ACTIVE	500C F618h	5001 0618h	5005 0618h
61Ch	32	EPWM_XCMP8_ACTIVE	500C F61Ch	5001 061Ch	5005 061Ch
620h	32	EPWM_XTBPRD_ACTIVE	500C F620h	5001 0620h	5005 0620h
630h	16	EPWM_XAQCTLA_ACTIVE	500C F630h	5001 0630h	5005 0630h
644h	32	EPWM_XMINMAX_ACTIVE	500C F644h	5001 0644h	5005 0644h
680h	32	EPWM_XCMP1_SHDW1	500C F680h	5001 0680h	5005 0680h
684h	32	EPWM_XCMP2_SHDW1	500C F684h	5001 0684h	5005 0684h
688h	32	EPWM_XCMP3_SHDW1	500C F688h	5001 0688h	5005 0688h
68Ch	32	EPWM_XCMP4_SHDW1	500C F68Ch	5001 068Ch	5005 068Ch
690h	32	EPWM_XCMP5_SHDW1	500C F690h	5001 0690h	5005 0690h
694h	32	EPWM_XCMP6_SHDW1	500C F694h	5001 0694h	5005 0694h
698h	32	EPWM_XCMP7_SHDW1	500C F698h	5001 0698h	5005 0698h

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Table 3-591. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM31_G1 Physical Address	EPWM00_G2 Physical Address	EPWM01_G2 Physical Address
69Ch	32	EPWM_XCMP8_SHDW1	500C F69Ch	5001 069Ch	5005 069Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500C F6A0h	5001 06A0h	5005 06A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500C F6B0h	5001 06B0h	5005 06B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500C F6B2h	5001 06B2h	5005 06B2h
6BAh	16	EPWM_CMPC_SHDW1	500C F6BAh	5001 06BAh	5005 06BAh
6BEh	16	EPWM_CMPD_SHDW1	500C F6BEh	5001 06BEh	5005 06BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500C F6C4h	5001 06C4h	5005 06C4h
700h	32	EPWM_XCMP1_SHDW2	500C F700h	5001 0700h	5005 0700h
704h	32	EPWM_XCMP2_SHDW2	500C F704h	5001 0704h	5005 0704h
708h	32	EPWM_XCMP3_SHDW2	500C F708h	5001 0708h	5005 0708h
70Ch	32	EPWM_XCMP4_SHDW2	500C F70Ch	5001 070Ch	5005 070Ch
710h	32	EPWM_XCMP5_SHDW2	500C F710h	5001 0710h	5005 0710h
714h	32	EPWM_XCMP6_SHDW2	500C F714h	5001 0714h	5005 0714h
718h	32	EPWM_XCMP7_SHDW2	500C F718h	5001 0718h	5005 0718h
71Ch	32	EPWM_XCMP8_SHDW2	500C F71Ch	5001 071Ch	5005 071Ch
720h	32	EPWM_XTBPRD_SHDW2	500C F720h	5001 0720h	5005 0720h
730h	16	EPWM_XAQCTLA_SHDW2	500C F730h	5001 0730h	5005 0730h
732h	16	EPWM_XAQCTLB_SHDW2	500C F732h	5001 0732h	5005 0732h
73Ah	16	EPWM_CMPC_SHDW2	500C F73Ah	5001 073Ah	5005 073Ah
73Eh	16	EPWM_CMPD_SHDW2	500C F73Eh	5001 073Eh	5005 073Eh
744h	32	EPWM_XMINMAX_SHDW2	500C F744h	5001 0744h	5005 0744h
780h	32	EPWM_XCMP1_SHDW3	500C F780h	5001 0780h	5005 0780h
784h	32	EPWM_XCMP2_SHDW3	500C F784h	5001 0784h	5005 0784h
788h	32	EPWM_XCMP3_SHDW3	500C F788h	5001 0788h	5005 0788h
78Ch	32	EPWM_XCMP4_SHDW3	500C F78Ch	5001 078Ch	5005 078Ch
790h	32	EPWM_XCMP5_SHDW3	500C F790h	5001 0790h	5005 0790h
794h	32	EPWM_XCMP6_SHDW3	500C F794h	5001 0794h	5005 0794h
798h	32	EPWM_XCMP7_SHDW3	500C F798h	5001 0798h	5005 0798h
79Ch	32	EPWM_XCMP8_SHDW3	500C F79Ch	5001 079Ch	5005 079Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500C F7A0h	5001 07A0h	5005 07A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500C F7B0h	5001 07B0h	5005 07B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500C F7B2h	5001 07B2h	5005 07B2h
7BAh	16	EPWM_CMPC_SHDW3	500C F7BAh	5001 07BAh	5005 07BAh
7BEh	16	EPWM_CMPD_SHDW3	500C F7BEh	5001 07BEh	5005 07BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500C F7C4h	5001 07C4h	5005 07C4h
800h	32	EPWM_DECTL	500C F800h	5001 0800h	5005 0800h
804h	32	EPWM_DECOMPSEL	500C F804h	5001 0804h	5005 0804h
808h	32	EPWM_DEACTCTL	500C F808h	5001 0808h	5005 0808h
80Ch	32	EPWM_DESTS	500C F80Ch	5001 080Ch	5005 080Ch
810h	32	EPWM_DEFRC	500C F810h	5001 0810h	5005 0810h
814h	32	EPWM_DECLR	500C F814h	5001 0814h	5005 0814h
820h	32	EPWM_DEMONCNT	500C F820h	5001 0820h	5005 0820h
824h	32	EPWM_DEMONCTL	500C F824h	5001 0824h	5005 0824h
828h	32	EPWM_DEMONSTEP	500C F828h	5001 0828h	5005 0828h
82Ch	32	EPWM_DEMONTHRES	500C F82Ch	5001 082Ch	5005 082Ch
C00h	32	EPWM_MINDBCFG	500C FC00h	5001 0C00h	5005 0C00h

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Table 3-591. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM31_G1 Physical Address	EPWM00_G2 Physical Address	EPWM01_G2 Physical Address
C04h	32	EPWM_MINDBDLY	500C FC04h	5001 0C04h	5005 0C04h
C20h	32	EPWM_LUTCTLA	500C FC20h	5001 0C20h	5005 0C20h
C24h	32	EPWM_LUTCTLB	500C FC24h	5001 0C24h	5005 0C24h

Table 3-592. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM02_G2 Physical Address	EPWM03_G2 Physical Address	EPWM04_G2 Physical Address
0h	16	EPWM_TBCTL	5009 0000h	500D 0000h	5001 1000h
2h	16	EPWM_TBCTL2	5009 0002h	500D 0002h	5001 1002h
6h	16	EPWM_EPWMSYNCINSEL	5009 0006h	500D 0006h	5001 1006h
8h	16	EPWM_TBCTR	5009 0008h	500D 0008h	5001 1008h
Ah	16	EPWM_TBSTS	5009 000Ah	500D 000Ah	5001 100Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5009 000Ch	500D 000Ch	5001 100Ch
Eh	16	EPWM_TBCTL3	5009 000Eh	500D 000Eh	5001 100Eh
10h	16	EPWM_CMPCTL	5009 0010h	500D 0010h	5001 1010h
12h	16	EPWM_CMPCTL2	5009 0012h	500D 0012h	5001 1012h
18h	16	EPWM_DBCTL	5009 0018h	500D 0018h	5001 1018h
1Ah	16	EPWM_DBCTL2	5009 001Ah	500D 001Ah	5001 101Ah
20h	16	EPWM_AQCTL	5009 0020h	500D 0020h	5001 1020h
22h	16	EPWM_AQTSRCSEL	5009 0022h	500D 0022h	5001 1022h
28h	16	EPWM_PCCTL	5009 0028h	500D 0028h	5001 1028h
30h	16	EPWM_VCAPCTL	5009 0030h	500D 0030h	5001 1030h
32h	16	EPWM_VCNTCFG	5009 0032h	500D 0032h	5001 1032h
40h	16	EPWM_HRCNFG	5009 0040h	500D 0040h	5001 1040h
4Eh	16	EPWM_HRCNFG2	5009 004Eh	500D 004Eh	5001 104Eh
5Ah	16	EPWM_HRPCTL	5009 005Ah	500D 005Ah	5001 105Ah
5Ch	16	EPWM_TRREM	5009 005Ch	500D 005Ch	5001 105Ch
68h	16	EPWM_GLDCTL	5009 0068h	500D 0068h	5001 1068h
6Ah	16	EPWM_GLDCFG	5009 006Ah	500D 006Ah	5001 106Ah
70h	32	EPWM_EPWMXLINK	5009 0070h	500D 0070h	5001 1070h
74h	32	EPWM_EPWMXLINK2	5009 0074h	500D 0074h	5001 1074h
7Ah	16	EPWM_ETEST	5009 007Ah	500D 007Ah	5001 107Ah
7Ch	16	EPWM_EPWMREV	5009 007Ch	500D 007Ch	5001 107Ch
7Eh	16	EPWM_HRPWMREV	5009 007Eh	500D 007Eh	5001 107Eh
80h	16	EPWM_AQCTLA	5009 0080h	500D 0080h	5001 1080h
82h	16	EPWM_AQCTLA2	5009 0082h	500D 0082h	5001 1082h
84h	16	EPWM_AQCTLB	5009 0084h	500D 0084h	5001 1084h
86h	16	EPWM_AQCTLB2	5009 0086h	500D 0086h	5001 1086h
8Eh	16	EPWM_AQSFRC	5009 008Eh	500D 008Eh	5001 108Eh
92h	16	EPWM_AQCSFRC	5009 0092h	500D 0092h	5001 1092h
A0h	16	EPWM_DBREDHR	5009 00A0h	500D 00A0h	5001 10A0h
A2h	16	EPWM_DBRED	5009 00A2h	500D 00A2h	5001 10A2h
A4h	16	EPWM_DBFEDHR	5009 00A4h	500D 00A4h	5001 10A4h
A6h	16	EPWM_DBFED	5009 00A6h	500D 00A6h	5001 10A6h
C0h	32	EPWM_TBPHS	5009 00C0h	500D 00C0h	5001 10C0h
C4h	16	EPWM_TBPRDHR	5009 00C4h	500D 00C4h	5001 10C4h

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Table 3-592. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM02_G2 Physical Address	EPWM03_G2 Physical Address	EPWM04_G2 Physical Address
C6h	16	EPWM_TBPRD	5009 00C6h	500D 00C6h	5001 10C6h
C8h	16	EPWM_TBPRDHRB	5009 00C8h	500D 00C8h	5001 10C8h
D4h	32	EPWM_CMPA	5009 00D4h	500D 00D4h	5001 10D4h
D8h	32	EPWM_CMPB	5009 00D8h	500D 00D8h	5001 10D8h
DEh	16	EPWM_CMPC	5009 00DEh	500D 00DEh	5001 10DEh
E2h	16	EPWM_CMPD	5009 00E2h	500D 00E2h	5001 10E2h
E8h	16	EPWM_GLDCTL2	5009 00E8h	500D 00E8h	5001 10E8h
EEh	16	EPWM_SWVDELVAL	5009 00EEh	500D 00EEh	5001 10EEh
100h	16	EPWM_TZSEL	5009 0100h	500D 0100h	5001 1100h
102h	16	EPWM_TZSEL2	5009 0102h	500D 0102h	5001 1102h
104h	16	EPWM_TZDCSEL	5009 0104h	500D 0104h	5001 1104h
108h	16	EPWM_TZCTL	5009 0108h	500D 0108h	5001 1108h
10Ah	16	EPWM_TZCTL2	5009 010Ah	500D 010Ah	5001 110Ah
10Ch	16	EPWM_TZCTLDCA	5009 010Ch	500D 010Ch	5001 110Ch
10Eh	16	EPWM_TZCTLDCB	5009 010Eh	500D 010Eh	5001 110Eh
11Ah	16	EPWM_TZEINT	5009 011Ah	500D 011Ah	5001 111Ah
126h	16	EPWM_TZFLG	5009 0126h	500D 0126h	5001 1126h
128h	16	EPWM_TZCBCFLG	5009 0128h	500D 0128h	5001 1128h
12Ah	16	EPWM_TZOSTFLG	5009 012Ah	500D 012Ah	5001 112Ah
12Eh	16	EPWM_TZCLR	5009 012Eh	500D 012Eh	5001 112Eh
130h	16	EPWM_TZCBCCLR	5009 0130h	500D 0130h	5001 1130h
132h	16	EPWM_TZOSTCLR	5009 0132h	500D 0132h	5001 1132h
136h	16	EPWM_TZFRC	5009 0136h	500D 0136h	5001 1136h
13Ah	16	EPWM_TZTRIPOUTSEL	5009 013Ah	500D 013Ah	5001 113Ah
148h	16	EPWM_ETSEL	5009 0148h	500D 0148h	5001 1148h
14Ch	16	EPWM_ETPS	5009 014Ch	500D 014Ch	5001 114Ch
150h	16	EPWM_ETFLG	5009 0150h	500D 0150h	5001 1150h
154h	16	EPWM_ETCLR	5009 0154h	500D 0154h	5001 1154h
158h	16	EPWM_ETFRC	5009 0158h	500D 0158h	5001 1158h
15Ch	16	EPWM_ETINTPS	5009 015Ch	500D 015Ch	5001 115Ch
160h	16	EPWM_ETSOCPS	5009 0160h	500D 0160h	5001 1160h
164h	16	EPWM_ETCNTINITCTL	5009 0164h	500D 0164h	5001 1164h
168h	16	EPWM_ETCNTINIT	5009 0168h	500D 0168h	5001 1168h
16Ch	16	EPWM_ETINTMIXEN	5009 016Ch	500D 016Ch	5001 116Ch
170h	16	EPWM_ETSOCAMIXEN	5009 0170h	500D 0170h	5001 1170h
174h	16	EPWM_ETSOCBMIXEN	5009 0174h	500D 0174h	5001 1174h
180h	16	EPWM_DCTRIPSEL	5009 0180h	500D 0180h	5001 1180h
186h	16	EPWM_DCACTL	5009 0186h	500D 0186h	5001 1186h
188h	16	EPWM_DCBCTL	5009 0188h	500D 0188h	5001 1188h
18Eh	16	EPWM_DCFCTL	5009 018Eh	500D 018Eh	5001 118Eh
190h	16	EPWM_DCCAPCTL	5009 0190h	500D 0190h	5001 1190h
192h	16	EPWM_DCFOFFSET	5009 0192h	500D 0192h	5001 1192h
194h	16	EPWM_DCFOFFSETCNT	5009 0194h	500D 0194h	5001 1194h
196h	16	EPWM_DCFWINDOW	5009 0196h	500D 0196h	5001 1196h
198h	16	EPWM_DCFWINDOWCNT	5009 0198h	500D 0198h	5001 1198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5009 019Ah	500D 019Ah	5001 119Ah

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Table 3-592. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM02_G2 Physical Address	EPWM03_G2 Physical Address	EPWM04_G2 Physical Address
19Ch	16	EPWM_DCCAPMIXSEL	5009 019Ch	500D 019Ch	5001 119Ch
19Eh	16	EPWM_DCCAP	5009 019Eh	500D 019Eh	5001 119Eh
1A4h	16	EPWM_DCAHTRIPSEL	5009 01A4h	500D 01A4h	5001 11A4h
1A6h	16	EPWM_DCALTRIPSEL	5009 01A6h	500D 01A6h	5001 11A6h
1A8h	16	EPWM_DCBHTRIPSEL	5009 01A8h	500D 01A8h	5001 11A8h
1AAh	16	EPWM_DCBLTRIPSEL	5009 01AAh	500D 01AAh	5001 11AAh
1ACh	16	EPWM_CAPCTL	5009 01ACh	500D 01ACh	5001 11ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5009 01AEh	500D 01AEh	5001 11AEh
1B0h	16	EPWM_CAPINTRIPSEL	5009 01B0h	500D 01B0h	5001 11B0h
1B2h	16	EPWM_CAPTRIPSEL	5009 01B2h	500D 01B2h	5001 11B2h
1F4h	32	EPWM_EPWMLOCK	5009 01F4h	500D 01F4h	5001 11F4h
1FAh	16	EPWM_HWVDELVAL	5009 01FAh	500D 01FAh	5001 11FAh
1FCh	16	EPWM_VCNTVAL	5009 01FCh	500D 01FCh	5001 11FCh
400h	32	EPWM_XCMPCTL1	5009 0400h	500D 0400h	5001 1400h
410h	32	EPWM_XLOADCTL	5009 0410h	500D 0410h	5001 1410h
418h	32	EPWM_XLOAD	5009 0418h	500D 0418h	5001 1418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5009 041Ch	500D 041Ch	5001 141Ch
420h	32	EPWM_XREGSHDW1STS	5009 0420h	500D 0420h	5001 1420h
428h	32	EPWM_XREGSHDW2STS	5009 0428h	500D 0428h	5001 1428h
430h	32	EPWM_XREGSHDW3STS	5009 0430h	500D 0430h	5001 1430h
600h	32	EPWM_XCMP1_ACTIVE	5009 0600h	500D 0600h	5001 1600h
604h	32	EPWM_XCMP2_ACTIVE	5009 0604h	500D 0604h	5001 1604h
608h	32	EPWM_XCMP3_ACTIVE	5009 0608h	500D 0608h	5001 1608h
60Ch	32	EPWM_XCMP4_ACTIVE	5009 060Ch	500D 060Ch	5001 160Ch
610h	32	EPWM_XCMP5_ACTIVE	5009 0610h	500D 0610h	5001 1610h
614h	32	EPWM_XCMP6_ACTIVE	5009 0614h	500D 0614h	5001 1614h
618h	32	EPWM_XCMP7_ACTIVE	5009 0618h	500D 0618h	5001 1618h
61Ch	32	EPWM_XCMP8_ACTIVE	5009 061Ch	500D 061Ch	5001 161Ch
620h	32	EPWM_XTBPRD_ACTIVE	5009 0620h	500D 0620h	5001 1620h
630h	16	EPWM_XAQCTLA_ACTIVE	5009 0630h	500D 0630h	5001 1630h
644h	32	EPWM_XMINMAX_ACTIVE	5009 0644h	500D 0644h	5001 1644h
680h	32	EPWM_XCMP1_SHDW1	5009 0680h	500D 0680h	5001 1680h
684h	32	EPWM_XCMP2_SHDW1	5009 0684h	500D 0684h	5001 1684h
688h	32	EPWM_XCMP3_SHDW1	5009 0688h	500D 0688h	5001 1688h
68Ch	32	EPWM_XCMP4_SHDW1	5009 068Ch	500D 068Ch	5001 168Ch
690h	32	EPWM_XCMP5_SHDW1	5009 0690h	500D 0690h	5001 1690h
694h	32	EPWM_XCMP6_SHDW1	5009 0694h	500D 0694h	5001 1694h
698h	32	EPWM_XCMP7_SHDW1	5009 0698h	500D 0698h	5001 1698h
69Ch	32	EPWM_XCMP8_SHDW1	5009 069Ch	500D 069Ch	5001 169Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5009 06A0h	500D 06A0h	5001 16A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5009 06B0h	500D 06B0h	5001 16B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5009 06B2h	500D 06B2h	5001 16B2h
6BAh	16	EPWM_CMPC_SHDW1	5009 06BAh	500D 06BAh	5001 16BAh
6BEh	16	EPWM_CMPD_SHDW1	5009 06BEh	500D 06BEh	5001 16BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5009 06C4h	500D 06C4h	5001 16C4h
700h	32	EPWM_XCMP1_SHDW2	5009 0700h	500D 0700h	5001 1700h

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Table 3-592. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM02_G2 Physical Address	EPWM03_G2 Physical Address	EPWM04_G2 Physical Address
704h	32	EPWM_XCMP2_SHDW2	5009 0704h	500D 0704h	5001 1704h
708h	32	EPWM_XCMP3_SHDW2	5009 0708h	500D 0708h	5001 1708h
70Ch	32	EPWM_XCMP4_SHDW2	5009 070Ch	500D 070Ch	5001 170Ch
710h	32	EPWM_XCMP5_SHDW2	5009 0710h	500D 0710h	5001 1710h
714h	32	EPWM_XCMP6_SHDW2	5009 0714h	500D 0714h	5001 1714h
718h	32	EPWM_XCMP7_SHDW2	5009 0718h	500D 0718h	5001 1718h
71Ch	32	EPWM_XCMP8_SHDW2	5009 071Ch	500D 071Ch	5001 171Ch
720h	32	EPWM_XTBPRD_SHDW2	5009 0720h	500D 0720h	5001 1720h
730h	16	EPWM_XAQCTLA_SHDW2	5009 0730h	500D 0730h	5001 1730h
732h	16	EPWM_XAQCTLB_SHDW2	5009 0732h	500D 0732h	5001 1732h
73Ah	16	EPWM_CMPC_SHDW2	5009 073Ah	500D 073Ah	5001 173Ah
73Eh	16	EPWM_CMPD_SHDW2	5009 073Eh	500D 073Eh	5001 173Eh
744h	32	EPWM_XMINMAX_SHDW2	5009 0744h	500D 0744h	5001 1744h
780h	32	EPWM_XCMP1_SHDW3	5009 0780h	500D 0780h	5001 1780h
784h	32	EPWM_XCMP2_SHDW3	5009 0784h	500D 0784h	5001 1784h
788h	32	EPWM_XCMP3_SHDW3	5009 0788h	500D 0788h	5001 1788h
78Ch	32	EPWM_XCMP4_SHDW3	5009 078Ch	500D 078Ch	5001 178Ch
790h	32	EPWM_XCMP5_SHDW3	5009 0790h	500D 0790h	5001 1790h
794h	32	EPWM_XCMP6_SHDW3	5009 0794h	500D 0794h	5001 1794h
798h	32	EPWM_XCMP7_SHDW3	5009 0798h	500D 0798h	5001 1798h
79Ch	32	EPWM_XCMP8_SHDW3	5009 079Ch	500D 079Ch	5001 179Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5009 07A0h	500D 07A0h	5001 17A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5009 07B0h	500D 07B0h	5001 17B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5009 07B2h	500D 07B2h	5001 17B2h
7BAh	16	EPWM_CMPC_SHDW3	5009 07BAh	500D 07BAh	5001 17BAh
7BEh	16	EPWM_CMPD_SHDW3	5009 07BEh	500D 07BEh	5001 17BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5009 07C4h	500D 07C4h	5001 17C4h
800h	32	EPWM_DECTL	5009 0800h	500D 0800h	5001 1800h
804h	32	EPWM_DECOMPSEL	5009 0804h	500D 0804h	5001 1804h
808h	32	EPWM_DEACTCTL	5009 0808h	500D 0808h	5001 1808h
80Ch	32	EPWM_DESTS	5009 080Ch	500D 080Ch	5001 180Ch
810h	32	EPWM_DEFRC	5009 0810h	500D 0810h	5001 1810h
814h	32	EPWM_DECLR	5009 0814h	500D 0814h	5001 1814h
820h	32	EPWM_DEMONCNT	5009 0820h	500D 0820h	5001 1820h
824h	32	EPWM_DEMONCTL	5009 0824h	500D 0824h	5001 1824h
828h	32	EPWM_DEMONSTEP	5009 0828h	500D 0828h	5001 1828h
82Ch	32	EPWM_DEMONTHRES	5009 082Ch	500D 082Ch	5001 182Ch
C00h	32	EPWM_MINDBCFG	5009 0C00h	500D 0C00h	5001 1C00h
C04h	32	EPWM_MINDBDLY	5009 0C04h	500D 0C04h	5001 1C04h
C20h	32	EPWM_LUTCTLA	5009 0C20h	500D 0C20h	5001 1C20h
C24h	32	EPWM_LUTCTLB	5009 0C24h	500D 0C24h	5001 1C24h

Table 3-593. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM05_G2 Physical Address	EPWM06_G2 Physical Address	EPWM07_G2 Physical Address
0h	16	EPWM_TBCTL	5005 1000h	5009 1000h	500D 1000h

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Table 3-593. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM05_G2 Physical Address	EPWM06_G2 Physical Address	EPWM07_G2 Physical Address
2h	16	EPWM_TBCTL2	5005 1002h	5009 1002h	500D 1002h
6h	16	EPWM_EPWMSYNCINSEL	5005 1006h	5009 1006h	500D 1006h
8h	16	EPWM_TBCTR	5005 1008h	5009 1008h	500D 1008h
Ah	16	EPWM_TBSTS	5005 100Ah	5009 100Ah	500D 100Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5005 100Ch	5009 100Ch	500D 100Ch
Eh	16	EPWM_TBCTL3	5005 100Eh	5009 100Eh	500D 100Eh
10h	16	EPWM_CMPCTL	5005 1010h	5009 1010h	500D 1010h
12h	16	EPWM_CMPCTL2	5005 1012h	5009 1012h	500D 1012h
18h	16	EPWM_DBCTL	5005 1018h	5009 1018h	500D 1018h
1Ah	16	EPWM_DBCTL2	5005 101Ah	5009 101Ah	500D 101Ah
20h	16	EPWM_AQCTL	5005 1020h	5009 1020h	500D 1020h
22h	16	EPWM_AQTSRCSEL	5005 1022h	5009 1022h	500D 1022h
28h	16	EPWM_PCCTL	5005 1028h	5009 1028h	500D 1028h
30h	16	EPWM_VCAPCTL	5005 1030h	5009 1030h	500D 1030h
32h	16	EPWM_VCNTCFG	5005 1032h	5009 1032h	500D 1032h
40h	16	EPWM_HRCNFG	5005 1040h	5009 1040h	500D 1040h
4Eh	16	EPWM_HRCNFG2	5005 104Eh	5009 104Eh	500D 104Eh
5Ah	16	EPWM_HRPCTL	5005 105Ah	5009 105Ah	500D 105Ah
5Ch	16	EPWM_TRREM	5005 105Ch	5009 105Ch	500D 105Ch
68h	16	EPWM_GLDCTL	5005 1068h	5009 1068h	500D 1068h
6Ah	16	EPWM_GLDCFG	5005 106Ah	5009 106Ah	500D 106Ah
70h	32	EPWM_EPWMXLINK	5005 1070h	5009 1070h	500D 1070h
74h	32	EPWM_EPWMXLINK2	5005 1074h	5009 1074h	500D 1074h
7Ah	16	EPWM_ETEST	5005 107Ah	5009 107Ah	500D 107Ah
7Ch	16	EPWM_EPWMREV	5005 107Ch	5009 107Ch	500D 107Ch
7Eh	16	EPWM_HRPWMREV	5005 107Eh	5009 107Eh	500D 107Eh
80h	16	EPWM_AQCTLA	5005 1080h	5009 1080h	500D 1080h
82h	16	EPWM_AQCTLA2	5005 1082h	5009 1082h	500D 1082h
84h	16	EPWM_AQCTLB	5005 1084h	5009 1084h	500D 1084h
86h	16	EPWM_AQCTLB2	5005 1086h	5009 1086h	500D 1086h
8Eh	16	EPWM_AQSFRC	5005 108Eh	5009 108Eh	500D 108Eh
92h	16	EPWM_AQCSFRC	5005 1092h	5009 1092h	500D 1092h
A0h	16	EPWM_DBREDHR	5005 10A0h	5009 10A0h	500D 10A0h
A2h	16	EPWM_DBRED	5005 10A2h	5009 10A2h	500D 10A2h
A4h	16	EPWM_DBFEDHR	5005 10A4h	5009 10A4h	500D 10A4h
A6h	16	EPWM_DBFED	5005 10A6h	5009 10A6h	500D 10A6h
C0h	32	EPWM_TBPHS	5005 10C0h	5009 10C0h	500D 10C0h
C4h	16	EPWM_TBPRDHR	5005 10C4h	5009 10C4h	500D 10C4h
C6h	16	EPWM_TBPRD	5005 10C6h	5009 10C6h	500D 10C6h
C8h	16	EPWM_TBPRDHRB	5005 10C8h	5009 10C8h	500D 10C8h
D4h	32	EPWM_CMPA	5005 10D4h	5009 10D4h	500D 10D4h
D8h	32	EPWM_CMPB	5005 10D8h	5009 10D8h	500D 10D8h
DEh	16	EPWM_CMPC	5005 10DEh	5009 10DEh	500D 10DEh
E2h	16	EPWM_CMPD	5005 10E2h	5009 10E2h	500D 10E2h
E8h	16	EPWM_GLDCTL2	5005 10E8h	5009 10E8h	500D 10E8h
EEh	16	EPWM_SWVDELVAL	5005 10EEh	5009 10EEh	500D 10EEh

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Table 3-593. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM05_G2 Physical Address	EPWM06_G2 Physical Address	EPWM07_G2 Physical Address
100h	16	EPWM_TZSEL	5005 1100h	5009 1100h	500D 1100h
102h	16	EPWM_TZSEL2	5005 1102h	5009 1102h	500D 1102h
104h	16	EPWM_TZDCSEL	5005 1104h	5009 1104h	500D 1104h
108h	16	EPWM_TZCTL	5005 1108h	5009 1108h	500D 1108h
10Ah	16	EPWM_TZCTL2	5005 110Ah	5009 110Ah	500D 110Ah
10Ch	16	EPWM_TZCTLDCA	5005 110Ch	5009 110Ch	500D 110Ch
10Eh	16	EPWM_TZCTLDCB	5005 110Eh	5009 110Eh	500D 110Eh
11Ah	16	EPWM_TZEINT	5005 111Ah	5009 111Ah	500D 111Ah
126h	16	EPWM_TZFLG	5005 1126h	5009 1126h	500D 1126h
128h	16	EPWM_TZCBCFLG	5005 1128h	5009 1128h	500D 1128h
12Ah	16	EPWM_TZOSTFLG	5005 112Ah	5009 112Ah	500D 112Ah
12Eh	16	EPWM_TZCLR	5005 112Eh	5009 112Eh	500D 112Eh
130h	16	EPWM_TZCBCCLR	5005 1130h	5009 1130h	500D 1130h
132h	16	EPWM_TZOSTCLR	5005 1132h	5009 1132h	500D 1132h
136h	16	EPWM_TZFRC	5005 1136h	5009 1136h	500D 1136h
13Ah	16	EPWM_TZTRIPOUTSEL	5005 113Ah	5009 113Ah	500D 113Ah
148h	16	EPWM_ETSEL	5005 1148h	5009 1148h	500D 1148h
14Ch	16	EPWM_ETPS	5005 114Ch	5009 114Ch	500D 114Ch
150h	16	EPWM_ETFLG	5005 1150h	5009 1150h	500D 1150h
154h	16	EPWM_ETCLR	5005 1154h	5009 1154h	500D 1154h
158h	16	EPWM_ETFRC	5005 1158h	5009 1158h	500D 1158h
15Ch	16	EPWM_ETINTPS	5005 115Ch	5009 115Ch	500D 115Ch
160h	16	EPWM_ETSOCPS	5005 1160h	5009 1160h	500D 1160h
164h	16	EPWM_ETCNTINITCTL	5005 1164h	5009 1164h	500D 1164h
168h	16	EPWM_ETCNTINIT	5005 1168h	5009 1168h	500D 1168h
16Ch	16	EPWM_ETINTMIXEN	5005 116Ch	5009 116Ch	500D 116Ch
170h	16	EPWM_ETSOCAMIXEN	5005 1170h	5009 1170h	500D 1170h
174h	16	EPWM_ETSOCBMIXEN	5005 1174h	5009 1174h	500D 1174h
180h	16	EPWM_DCTRIPSEL	5005 1180h	5009 1180h	500D 1180h
186h	16	EPWM_DCACTL	5005 1186h	5009 1186h	500D 1186h
188h	16	EPWM_DCBCTL	5005 1188h	5009 1188h	500D 1188h
18Eh	16	EPWM_DCFCTL	5005 118Eh	5009 118Eh	500D 118Eh
190h	16	EPWM_DCCAPCTL	5005 1190h	5009 1190h	500D 1190h
192h	16	EPWM_DCFOFFSET	5005 1192h	5009 1192h	500D 1192h
194h	16	EPWM_DCFOFFSETCNT	5005 1194h	5009 1194h	500D 1194h
196h	16	EPWM_DCFWINDOW	5005 1196h	5009 1196h	500D 1196h
198h	16	EPWM_DCFWINDOWCNT	5005 1198h	5009 1198h	500D 1198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5005 119Ah	5009 119Ah	500D 119Ah
19Ch	16	EPWM_DCCAPMIXSEL	5005 119Ch	5009 119Ch	500D 119Ch
19Eh	16	EPWM_DCCAP	5005 119Eh	5009 119Eh	500D 119Eh
1A4h	16	EPWM_DCAHTRIPSEL	5005 11A4h	5009 11A4h	500D 11A4h
1A6h	16	EPWM_DCALTRIPSEL	5005 11A6h	5009 11A6h	500D 11A6h
1A8h	16	EPWM_DCBHTRIPSEL	5005 11A8h	5009 11A8h	500D 11A8h
1AAh	16	EPWM_DCBLTRIPSEL	5005 11AAh	5009 11AAh	500D 11AAh
1ACh	16	EPWM_CAPCTL	5005 11ACh	5009 11ACh	500D 11ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5005 11AEh	5009 11AEh	500D 11AEh

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Table 3-593. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM05_G2 Physical Address	EPWM06_G2 Physical Address	EPWM07_G2 Physical Address
1B0h	16	EPWM_CAPINTRIPSEL	5005 11B0h	5009 11B0h	500D 11B0h
1B2h	16	EPWM_CAPTRIPSEL	5005 11B2h	5009 11B2h	500D 11B2h
1F4h	32	EPWM_EPWMLOCK	5005 11F4h	5009 11F4h	500D 11F4h
1FAh	16	EPWM_HWVDELVAL	5005 11FAh	5009 11FAh	500D 11FAh
1FCh	16	EPWM_VCNTVAL	5005 11FCh	5009 11FCh	500D 11FCh
400h	32	EPWM_XCMPCTL1	5005 1400h	5009 1400h	500D 1400h
410h	32	EPWM_XLOADCTL	5005 1410h	5009 1410h	500D 1410h
418h	32	EPWM_XLOAD	5005 1418h	5009 1418h	500D 1418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5005 141Ch	5009 141Ch	500D 141Ch
420h	32	EPWM_XREGSHDW1STS	5005 1420h	5009 1420h	500D 1420h
428h	32	EPWM_XREGSHDW2STS	5005 1428h	5009 1428h	500D 1428h
430h	32	EPWM_XREGSHDW3STS	5005 1430h	5009 1430h	500D 1430h
600h	32	EPWM_XCMP1_ACTIVE	5005 1600h	5009 1600h	500D 1600h
604h	32	EPWM_XCMP2_ACTIVE	5005 1604h	5009 1604h	500D 1604h
608h	32	EPWM_XCMP3_ACTIVE	5005 1608h	5009 1608h	500D 1608h
60Ch	32	EPWM_XCMP4_ACTIVE	5005 160Ch	5009 160Ch	500D 160Ch
610h	32	EPWM_XCMP5_ACTIVE	5005 1610h	5009 1610h	500D 1610h
614h	32	EPWM_XCMP6_ACTIVE	5005 1614h	5009 1614h	500D 1614h
618h	32	EPWM_XCMP7_ACTIVE	5005 1618h	5009 1618h	500D 1618h
61Ch	32	EPWM_XCMP8_ACTIVE	5005 161Ch	5009 161Ch	500D 161Ch
620h	32	EPWM_XTBPRD_ACTIVE	5005 1620h	5009 1620h	500D 1620h
630h	16	EPWM_XAQCTLA_ACTIVE	5005 1630h	5009 1630h	500D 1630h
644h	32	EPWM_XMINMAX_ACTIVE	5005 1644h	5009 1644h	500D 1644h
680h	32	EPWM_XCMP1_SHDW1	5005 1680h	5009 1680h	500D 1680h
684h	32	EPWM_XCMP2_SHDW1	5005 1684h	5009 1684h	500D 1684h
688h	32	EPWM_XCMP3_SHDW1	5005 1688h	5009 1688h	500D 1688h
68Ch	32	EPWM_XCMP4_SHDW1	5005 168Ch	5009 168Ch	500D 168Ch
690h	32	EPWM_XCMP5_SHDW1	5005 1690h	5009 1690h	500D 1690h
694h	32	EPWM_XCMP6_SHDW1	5005 1694h	5009 1694h	500D 1694h
698h	32	EPWM_XCMP7_SHDW1	5005 1698h	5009 1698h	500D 1698h
69Ch	32	EPWM_XCMP8_SHDW1	5005 169Ch	5009 169Ch	500D 169Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5005 16A0h	5009 16A0h	500D 16A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5005 16B0h	5009 16B0h	500D 16B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5005 16B2h	5009 16B2h	500D 16B2h
6BAh	16	EPWM_CMPC_SHDW1	5005 16BAh	5009 16BAh	500D 16BAh
6BEh	16	EPWM_CMPD_SHDW1	5005 16BEh	5009 16BEh	500D 16BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5005 16C4h	5009 16C4h	500D 16C4h
700h	32	EPWM_XCMP1_SHDW2	5005 1700h	5009 1700h	500D 1700h
704h	32	EPWM_XCMP2_SHDW2	5005 1704h	5009 1704h	500D 1704h
708h	32	EPWM_XCMP3_SHDW2	5005 1708h	5009 1708h	500D 1708h
70Ch	32	EPWM_XCMP4_SHDW2	5005 170Ch	5009 170Ch	500D 170Ch
710h	32	EPWM_XCMP5_SHDW2	5005 1710h	5009 1710h	500D 1710h
714h	32	EPWM_XCMP6_SHDW2	5005 1714h	5009 1714h	500D 1714h
718h	32	EPWM_XCMP7_SHDW2	5005 1718h	5009 1718h	500D 1718h
71Ch	32	EPWM_XCMP8_SHDW2	5005 171Ch	5009 171Ch	500D 171Ch
720h	32	EPWM_XTBPRD_SHDW2	5005 1720h	5009 1720h	500D 1720h

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Table 3-593. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM05_G2 Physical Address	EPWM06_G2 Physical Address	EPWM07_G2 Physical Address
730h	16	EPWM_XAQCTLA_SHDW2	5005 1730h	5009 1730h	500D 1730h
732h	16	EPWM_XAQCTLB_SHDW2	5005 1732h	5009 1732h	500D 1732h
73Ah	16	EPWM_CMPC_SHDW2	5005 173Ah	5009 173Ah	500D 173Ah
73Eh	16	EPWM_CMPD_SHDW2	5005 173Eh	5009 173Eh	500D 173Eh
744h	32	EPWM_XMINMAX_SHDW2	5005 1744h	5009 1744h	500D 1744h
780h	32	EPWM_XCMP1_SHDW3	5005 1780h	5009 1780h	500D 1780h
784h	32	EPWM_XCMP2_SHDW3	5005 1784h	5009 1784h	500D 1784h
788h	32	EPWM_XCMP3_SHDW3	5005 1788h	5009 1788h	500D 1788h
78Ch	32	EPWM_XCMP4_SHDW3	5005 178Ch	5009 178Ch	500D 178Ch
790h	32	EPWM_XCMP5_SHDW3	5005 1790h	5009 1790h	500D 1790h
794h	32	EPWM_XCMP6_SHDW3	5005 1794h	5009 1794h	500D 1794h
798h	32	EPWM_XCMP7_SHDW3	5005 1798h	5009 1798h	500D 1798h
79Ch	32	EPWM_XCMP8_SHDW3	5005 179Ch	5009 179Ch	500D 179Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5005 17A0h	5009 17A0h	500D 17A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5005 17B0h	5009 17B0h	500D 17B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5005 17B2h	5009 17B2h	500D 17B2h
7BAh	16	EPWM_CMPC_SHDW3	5005 17BAh	5009 17BAh	500D 17BAh
7BEh	16	EPWM_CMPD_SHDW3	5005 17BEh	5009 17BEh	500D 17BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5005 17C4h	5009 17C4h	500D 17C4h
800h	32	EPWM_DECTL	5005 1800h	5009 1800h	500D 1800h
804h	32	EPWM_DECOMPSEL	5005 1804h	5009 1804h	500D 1804h
808h	32	EPWM_DEACTCTL	5005 1808h	5009 1808h	500D 1808h
80Ch	32	EPWM_DESTS	5005 180Ch	5009 180Ch	500D 180Ch
810h	32	EPWM_DEFRC	5005 1810h	5009 1810h	500D 1810h
814h	32	EPWM_DECLR	5005 1814h	5009 1814h	500D 1814h
820h	32	EPWM_DEMONCNT	5005 1820h	5009 1820h	500D 1820h
824h	32	EPWM_DEMONCTL	5005 1824h	5009 1824h	500D 1824h
828h	32	EPWM_DEMONSTEP	5005 1828h	5009 1828h	500D 1828h
82Ch	32	EPWM_DEMONTHRES	5005 182Ch	5009 182Ch	500D 182Ch
C00h	32	EPWM_MINDBCFG	5005 1C00h	5009 1C00h	500D 1C00h
C04h	32	EPWM_MINDBDLY	5005 1C04h	5009 1C04h	500D 1C04h
C20h	32	EPWM_LUTCTLA	5005 1C20h	5009 1C20h	500D 1C20h
C24h	32	EPWM_LUTCTLB	5005 1C24h	5009 1C24h	500D 1C24h

Table 3-594. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM08_G2 Physical Address	EPWM09_G2 Physical Address	EPWM10_G2 Physical Address
0h	16	EPWM_TBCTL	5001 2000h	5005 2000h	5009 2000h
2h	16	EPWM_TBCTL2	5001 2002h	5005 2002h	5009 2002h
6h	16	EPWM_EPWMSYNCINSEL	5001 2006h	5005 2006h	5009 2006h
8h	16	EPWM_TBCTR	5001 2008h	5005 2008h	5009 2008h
Ah	16	EPWM_TBSTS	5001 200Ah	5005 200Ah	5009 200Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5001 200Ch	5005 200Ch	5009 200Ch
Eh	16	EPWM_TBCTL3	5001 200Eh	5005 200Eh	5009 200Eh
10h	16	EPWM_CMPCTL	5001 2010h	5005 2010h	5009 2010h
12h	16	EPWM_CMPCTL2	5001 2012h	5005 2012h	5009 2012h

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Table 3-594. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM08_G2 Physical Address	EPWM09_G2 Physical Address	EPWM10_G2 Physical Address
18h	16	EPWM_DBCTL	5001 2018h	5005 2018h	5009 2018h
1Ah	16	EPWM_DBCTL2	5001 201Ah	5005 201Ah	5009 201Ah
20h	16	EPWM_AQCTL	5001 2020h	5005 2020h	5009 2020h
22h	16	EPWM_AQTSRCSEL	5001 2022h	5005 2022h	5009 2022h
28h	16	EPWM_PCCTL	5001 2028h	5005 2028h	5009 2028h
30h	16	EPWM_VCAPCTL	5001 2030h	5005 2030h	5009 2030h
32h	16	EPWM_VCNTCFG	5001 2032h	5005 2032h	5009 2032h
40h	16	EPWM_HRCNFG	5001 2040h	5005 2040h	5009 2040h
4Eh	16	EPWM_HRCNFG2	5001 204Eh	5005 204Eh	5009 204Eh
5Ah	16	EPWM_HRPCTL	5001 205Ah	5005 205Ah	5009 205Ah
5Ch	16	EPWM_TRREM	5001 205Ch	5005 205Ch	5009 205Ch
68h	16	EPWM_GLDCTL	5001 2068h	5005 2068h	5009 2068h
6Ah	16	EPWM_GLDCFG	5001 206Ah	5005 206Ah	5009 206Ah
70h	32	EPWM_EPWMXLINK	5001 2070h	5005 2070h	5009 2070h
74h	32	EPWM_EPWMXLINK2	5001 2074h	5005 2074h	5009 2074h
7Ah	16	EPWM_ETEST	5001 207Ah	5005 207Ah	5009 207Ah
7Ch	16	EPWM_EPWMREV	5001 207Ch	5005 207Ch	5009 207Ch
7Eh	16	EPWM_HRPWMREV	5001 207Eh	5005 207Eh	5009 207Eh
80h	16	EPWM_AQCTLA	5001 2080h	5005 2080h	5009 2080h
82h	16	EPWM_AQCTLA2	5001 2082h	5005 2082h	5009 2082h
84h	16	EPWM_AQCTLB	5001 2084h	5005 2084h	5009 2084h
86h	16	EPWM_AQCTLB2	5001 2086h	5005 2086h	5009 2086h
8Eh	16	EPWM_AQSFRC	5001 208Eh	5005 208Eh	5009 208Eh
92h	16	EPWM_AQCSFRC	5001 2092h	5005 2092h	5009 2092h
A0h	16	EPWM_DBREDHR	5001 20A0h	5005 20A0h	5009 20A0h
A2h	16	EPWM_DBRED	5001 20A2h	5005 20A2h	5009 20A2h
A4h	16	EPWM_DBFEDHR	5001 20A4h	5005 20A4h	5009 20A4h
A6h	16	EPWM_DBFED	5001 20A6h	5005 20A6h	5009 20A6h
C0h	32	EPWM_TBPHS	5001 20C0h	5005 20C0h	5009 20C0h
C4h	16	EPWM_TBPRDHR	5001 20C4h	5005 20C4h	5009 20C4h
C6h	16	EPWM_TBPRD	5001 20C6h	5005 20C6h	5009 20C6h
C8h	16	EPWM_TBPRDHRB	5001 20C8h	5005 20C8h	5009 20C8h
D4h	32	EPWM_CMPA	5001 20D4h	5005 20D4h	5009 20D4h
D8h	32	EPWM_CMPB	5001 20D8h	5005 20D8h	5009 20D8h
DEh	16	EPWM_CMPC	5001 20DEh	5005 20DEh	5009 20DEh
E2h	16	EPWM_CMPD	5001 20E2h	5005 20E2h	5009 20E2h
E8h	16	EPWM_GLDCTL2	5001 20E8h	5005 20E8h	5009 20E8h
EEh	16	EPWM_SWVDELVAL	5001 20EEh	5005 20EEh	5009 20EEh
100h	16	EPWM_TZSEL	5001 2100h	5005 2100h	5009 2100h
102h	16	EPWM_TZSEL2	5001 2102h	5005 2102h	5009 2102h
104h	16	EPWM_TZDCSEL	5001 2104h	5005 2104h	5009 2104h
108h	16	EPWM_TZCTL	5001 2108h	5005 2108h	5009 2108h
10Ah	16	EPWM_TZCTL2	5001 210Ah	5005 210Ah	5009 210Ah
10Ch	16	EPWM_TZCTLDCA	5001 210Ch	5005 210Ch	5009 210Ch
10Eh	16	EPWM_TZCTLDCB	5001 210Eh	5005 210Eh	5009 210Eh
11Ah	16	EPWM_TZEINT	5001 211Ah	5005 211Ah	5009 211Ah

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Table 3-594. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM08_G2 Physical Address	EPWM09_G2 Physical Address	EPWM10_G2 Physical Address
126h	16	EPWM_TZFLG	5001 2126h	5005 2126h	5009 2126h
128h	16	EPWM_TZCBCFLG	5001 2128h	5005 2128h	5009 2128h
12Ah	16	EPWM_TZOSTFLG	5001 212Ah	5005 212Ah	5009 212Ah
12Eh	16	EPWM_TZCLR	5001 212Eh	5005 212Eh	5009 212Eh
130h	16	EPWM_TZCBCCLR	5001 2130h	5005 2130h	5009 2130h
132h	16	EPWM_TZOSTCLR	5001 2132h	5005 2132h	5009 2132h
136h	16	EPWM_TZFRC	5001 2136h	5005 2136h	5009 2136h
13Ah	16	EPWM_TZTRIPOUTSEL	5001 213Ah	5005 213Ah	5009 213Ah
148h	16	EPWM_ETSEL	5001 2148h	5005 2148h	5009 2148h
14Ch	16	EPWM_ETPS	5001 214Ch	5005 214Ch	5009 214Ch
150h	16	EPWM_ETFLG	5001 2150h	5005 2150h	5009 2150h
154h	16	EPWM_ETCLR	5001 2154h	5005 2154h	5009 2154h
158h	16	EPWM_ETFRC	5001 2158h	5005 2158h	5009 2158h
15Ch	16	EPWM_ETINTPS	5001 215Ch	5005 215Ch	5009 215Ch
160h	16	EPWM_ETSOCPS	5001 2160h	5005 2160h	5009 2160h
164h	16	EPWM_ETCNTINITCTL	5001 2164h	5005 2164h	5009 2164h
168h	16	EPWM_ETCNTINIT	5001 2168h	5005 2168h	5009 2168h
16Ch	16	EPWM_ETINTMIXEN	5001 216Ch	5005 216Ch	5009 216Ch
170h	16	EPWM_ETSOCAMIXEN	5001 2170h	5005 2170h	5009 2170h
174h	16	EPWM_ETSOCBMIXEN	5001 2174h	5005 2174h	5009 2174h
180h	16	EPWM_DCTRIPSEL	5001 2180h	5005 2180h	5009 2180h
186h	16	EPWM_DCACTL	5001 2186h	5005 2186h	5009 2186h
188h	16	EPWM_DCBCTL	5001 2188h	5005 2188h	5009 2188h
18Eh	16	EPWM_DCFCTL	5001 218Eh	5005 218Eh	5009 218Eh
190h	16	EPWM_DCCAPCTL	5001 2190h	5005 2190h	5009 2190h
192h	16	EPWM_DCFOFFSET	5001 2192h	5005 2192h	5009 2192h
194h	16	EPWM_DCFOFFSETCNT	5001 2194h	5005 2194h	5009 2194h
196h	16	EPWM_DCFWINDOW	5001 2196h	5005 2196h	5009 2196h
198h	16	EPWM_DCFWINDOWCNT	5001 2198h	5005 2198h	5009 2198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5001 219Ah	5005 219Ah	5009 219Ah
19Ch	16	EPWM_DCCAPMIXSEL	5001 219Ch	5005 219Ch	5009 219Ch
19Eh	16	EPWM_DCCAP	5001 219Eh	5005 219Eh	5009 219Eh
1A4h	16	EPWM_DCAHTRIPSEL	5001 21A4h	5005 21A4h	5009 21A4h
1A6h	16	EPWM_DCALTRIPSEL	5001 21A6h	5005 21A6h	5009 21A6h
1A8h	16	EPWM_DCBHTRIPSEL	5001 21A8h	5005 21A8h	5009 21A8h
1AAh	16	EPWM_DCBLTRIPSEL	5001 21AAh	5005 21AAh	5009 21AAh
1ACh	16	EPWM_CAPCTL	5001 21ACh	5005 21ACh	5009 21ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5001 21AEh	5005 21AEh	5009 21AEh
1B0h	16	EPWM_CAPINTRIPSEL	5001 21B0h	5005 21B0h	5009 21B0h
1B2h	16	EPWM_CAPTRIPSEL	5001 21B2h	5005 21B2h	5009 21B2h
1F4h	32	EPWM_EPWMLOCK	5001 21F4h	5005 21F4h	5009 21F4h
1FAh	16	EPWM_HWVDELVAL	5001 21FAh	5005 21FAh	5009 21FAh
1FCh	16	EPWM_VCNTVAL	5001 21FCh	5005 21FCh	5009 21FCh
400h	32	EPWM_XCMPCTL1	5001 2400h	5005 2400h	5009 2400h
410h	32	EPWM_XLOADCTL	5001 2410h	5005 2410h	5009 2410h
418h	32	EPWM_XLOAD	5001 2418h	5005 2418h	5009 2418h

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Table 3-594. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM08_G2 Physical Address	EPWM09_G2 Physical Address	EPWM10_G2 Physical Address
41Ch	32	EPWM_EPWMXLINKXLOAD	5001 241Ch	5005 241Ch	5009 241Ch
420h	32	EPWM_XREGSHDW1STS	5001 2420h	5005 2420h	5009 2420h
428h	32	EPWM_XREGSHDW2STS	5001 2428h	5005 2428h	5009 2428h
430h	32	EPWM_XREGSHDW3STS	5001 2430h	5005 2430h	5009 2430h
600h	32	EPWM_XCMP1_ACTIVE	5001 2600h	5005 2600h	5009 2600h
604h	32	EPWM_XCMP2_ACTIVE	5001 2604h	5005 2604h	5009 2604h
608h	32	EPWM_XCMP3_ACTIVE	5001 2608h	5005 2608h	5009 2608h
60Ch	32	EPWM_XCMP4_ACTIVE	5001 260Ch	5005 260Ch	5009 260Ch
610h	32	EPWM_XCMP5_ACTIVE	5001 2610h	5005 2610h	5009 2610h
614h	32	EPWM_XCMP6_ACTIVE	5001 2614h	5005 2614h	5009 2614h
618h	32	EPWM_XCMP7_ACTIVE	5001 2618h	5005 2618h	5009 2618h
61Ch	32	EPWM_XCMP8_ACTIVE	5001 261Ch	5005 261Ch	5009 261Ch
620h	32	EPWM_XTBPRD_ACTIVE	5001 2620h	5005 2620h	5009 2620h
630h	16	EPWM_XAQCTLA_ACTIVE	5001 2630h	5005 2630h	5009 2630h
644h	32	EPWM_XMINMAX_ACTIVE	5001 2644h	5005 2644h	5009 2644h
680h	32	EPWM_XCMP1_SHDW1	5001 2680h	5005 2680h	5009 2680h
684h	32	EPWM_XCMP2_SHDW1	5001 2684h	5005 2684h	5009 2684h
688h	32	EPWM_XCMP3_SHDW1	5001 2688h	5005 2688h	5009 2688h
68Ch	32	EPWM_XCMP4_SHDW1	5001 268Ch	5005 268Ch	5009 268Ch
690h	32	EPWM_XCMP5_SHDW1	5001 2690h	5005 2690h	5009 2690h
694h	32	EPWM_XCMP6_SHDW1	5001 2694h	5005 2694h	5009 2694h
698h	32	EPWM_XCMP7_SHDW1	5001 2698h	5005 2698h	5009 2698h
69Ch	32	EPWM_XCMP8_SHDW1	5001 269Ch	5005 269Ch	5009 269Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5001 26A0h	5005 26A0h	5009 26A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5001 26B0h	5005 26B0h	5009 26B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5001 26B2h	5005 26B2h	5009 26B2h
6BAh	16	EPWM_CMPC_SHDW1	5001 26BAh	5005 26BAh	5009 26BAh
6BEh	16	EPWM_CMPD_SHDW1	5001 26BEh	5005 26BEh	5009 26BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5001 26C4h	5005 26C4h	5009 26C4h
700h	32	EPWM_XCMP1_SHDW2	5001 2700h	5005 2700h	5009 2700h
704h	32	EPWM_XCMP2_SHDW2	5001 2704h	5005 2704h	5009 2704h
708h	32	EPWM_XCMP3_SHDW2	5001 2708h	5005 2708h	5009 2708h
70Ch	32	EPWM_XCMP4_SHDW2	5001 270Ch	5005 270Ch	5009 270Ch
710h	32	EPWM_XCMP5_SHDW2	5001 2710h	5005 2710h	5009 2710h
714h	32	EPWM_XCMP6_SHDW2	5001 2714h	5005 2714h	5009 2714h
718h	32	EPWM_XCMP7_SHDW2	5001 2718h	5005 2718h	5009 2718h
71Ch	32	EPWM_XCMP8_SHDW2	5001 271Ch	5005 271Ch	5009 271Ch
720h	32	EPWM_XTBPRD_SHDW2	5001 2720h	5005 2720h	5009 2720h
730h	16	EPWM_XAQCTLA_SHDW2	5001 2730h	5005 2730h	5009 2730h
732h	16	EPWM_XAQCTLB_SHDW2	5001 2732h	5005 2732h	5009 2732h
73Ah	16	EPWM_CMPC_SHDW2	5001 273Ah	5005 273Ah	5009 273Ah
73Eh	16	EPWM_CMPD_SHDW2	5001 273Eh	5005 273Eh	5009 273Eh
744h	32	EPWM_XMINMAX_SHDW2	5001 2744h	5005 2744h	5009 2744h
780h	32	EPWM_XCMP1_SHDW3	5001 2780h	5005 2780h	5009 2780h
784h	32	EPWM_XCMP2_SHDW3	5001 2784h	5005 2784h	5009 2784h
788h	32	EPWM_XCMP3_SHDW3	5001 2788h	5005 2788h	5009 2788h

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Table 3-594. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM08_G2 Physical Address	EPWM09_G2 Physical Address	EPWM10_G2 Physical Address
78Ch	32	EPWM_XCMP4_SHDW3	5001 278Ch	5005 278Ch	5009 278Ch
790h	32	EPWM_XCMP5_SHDW3	5001 2790h	5005 2790h	5009 2790h
794h	32	EPWM_XCMP6_SHDW3	5001 2794h	5005 2794h	5009 2794h
798h	32	EPWM_XCMP7_SHDW3	5001 2798h	5005 2798h	5009 2798h
79Ch	32	EPWM_XCMP8_SHDW3	5001 279Ch	5005 279Ch	5009 279Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5001 27A0h	5005 27A0h	5009 27A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5001 27B0h	5005 27B0h	5009 27B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5001 27B2h	5005 27B2h	5009 27B2h
7BAh	16	EPWM_CMPC_SHDW3	5001 27BAh	5005 27BAh	5009 27BAh
7BEh	16	EPWM_CMPD_SHDW3	5001 27BEh	5005 27BEh	5009 27BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5001 27C4h	5005 27C4h	5009 27C4h
800h	32	EPWM_DECTL	5001 2800h	5005 2800h	5009 2800h
804h	32	EPWM_DECOMPSEL	5001 2804h	5005 2804h	5009 2804h
808h	32	EPWM_DEACTCTL	5001 2808h	5005 2808h	5009 2808h
80Ch	32	EPWM_DESTS	5001 280Ch	5005 280Ch	5009 280Ch
810h	32	EPWM_DEFRC	5001 2810h	5005 2810h	5009 2810h
814h	32	EPWM_DECLR	5001 2814h	5005 2814h	5009 2814h
820h	32	EPWM_DEMONCNT	5001 2820h	5005 2820h	5009 2820h
824h	32	EPWM_DEMONCTL	5001 2824h	5005 2824h	5009 2824h
828h	32	EPWM_DEMONSTEP	5001 2828h	5005 2828h	5009 2828h
82Ch	32	EPWM_DEMONTHRES	5001 282Ch	5005 282Ch	5009 282Ch
C00h	32	EPWM_MINDBCFG	5001 2C00h	5005 2C00h	5009 2C00h
C04h	32	EPWM_MINDBDLY	5001 2C04h	5005 2C04h	5009 2C04h
C20h	32	EPWM_LUTCTLA	5001 2C20h	5005 2C20h	5009 2C20h
C24h	32	EPWM_LUTCTLB	5001 2C24h	5005 2C24h	5009 2C24h

Table 3-595. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM11_G2 Physical Address	EPWM12_G2 Physical Address	EPWM13_G2 Physical Address
0h	16	EPWM_TBCTL	500D 2000h	5001 3000h	5005 3000h
2h	16	EPWM_TBCTL2	500D 2002h	5001 3002h	5005 3002h
6h	16	EPWM_EPWMSYNCINSEL	500D 2006h	5001 3006h	5005 3006h
8h	16	EPWM_TBCTR	500D 2008h	5001 3008h	5005 3008h
Ah	16	EPWM_TBSTS	500D 200Ah	5001 300Ah	5005 300Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500D 200Ch	5001 300Ch	5005 300Ch
Eh	16	EPWM_TBCTL3	500D 200Eh	5001 300Eh	5005 300Eh
10h	16	EPWM_CMPCTL	500D 2010h	5001 3010h	5005 3010h
12h	16	EPWM_CMPCTL2	500D 2012h	5001 3012h	5005 3012h
18h	16	EPWM_DBCTL	500D 2018h	5001 3018h	5005 3018h
1Ah	16	EPWM_DBCTL2	500D 201Ah	5001 301Ah	5005 301Ah
20h	16	EPWM_AQCTL	500D 2020h	5001 3020h	5005 3020h
22h	16	EPWM_AQTSRCSEL	500D 2022h	5001 3022h	5005 3022h
28h	16	EPWM_PCCTL	500D 2028h	5001 3028h	5005 3028h
30h	16	EPWM_VCAPCTL	500D 2030h	5001 3030h	5005 3030h
32h	16	EPWM_VCNTCFG	500D 2032h	5001 3032h	5005 3032h
40h	16	EPWM_HRCNFG	500D 2040h	5001 3040h	5005 3040h

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Table 3-595. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM11_G2 Physical Address	EPWM12_G2 Physical Address	EPWM13_G2 Physical Address
4Eh	16	EPWM_HRCNFG2	500D 204Eh	5001 304Eh	5005 304Eh
5Ah	16	EPWM_HRPCTL	500D 205Ah	5001 305Ah	5005 305Ah
5Ch	16	EPWM_TRREM	500D 205Ch	5001 305Ch	5005 305Ch
68h	16	EPWM_GLDCTL	500D 2068h	5001 3068h	5005 3068h
6Ah	16	EPWM_GLDCFG	500D 206Ah	5001 306Ah	5005 306Ah
70h	32	EPWM_EPWMXLINK	500D 2070h	5001 3070h	5005 3070h
74h	32	EPWM_EPWMXLINK2	500D 2074h	5001 3074h	5005 3074h
7Ah	16	EPWM_ETEST	500D 207Ah	5001 307Ah	5005 307Ah
7Ch	16	EPWM_EPWMREV	500D 207Ch	5001 307Ch	5005 307Ch
7Eh	16	EPWM_HRPWMREV	500D 207Eh	5001 307Eh	5005 307Eh
80h	16	EPWM_AQCTLA	500D 2080h	5001 3080h	5005 3080h
82h	16	EPWM_AQCTLA2	500D 2082h	5001 3082h	5005 3082h
84h	16	EPWM_AQCTLB	500D 2084h	5001 3084h	5005 3084h
86h	16	EPWM_AQCTLB2	500D 2086h	5001 3086h	5005 3086h
8Eh	16	EPWM_AQSFRC	500D 208Eh	5001 308Eh	5005 308Eh
92h	16	EPWM_AQCSFRC	500D 2092h	5001 3092h	5005 3092h
A0h	16	EPWM_DBREDHR	500D 20A0h	5001 30A0h	5005 30A0h
A2h	16	EPWM_DBRED	500D 20A2h	5001 30A2h	5005 30A2h
A4h	16	EPWM_DBFEDHR	500D 20A4h	5001 30A4h	5005 30A4h
A6h	16	EPWM_DBFED	500D 20A6h	5001 30A6h	5005 30A6h
C0h	32	EPWM_TBPHS	500D 20C0h	5001 30C0h	5005 30C0h
C4h	16	EPWM_TBPRDHR	500D 20C4h	5001 30C4h	5005 30C4h
C6h	16	EPWM_TBPRD	500D 20C6h	5001 30C6h	5005 30C6h
C8h	16	EPWM_TBPRDHRB	500D 20C8h	5001 30C8h	5005 30C8h
D4h	32	EPWM_CMPA	500D 20D4h	5001 30D4h	5005 30D4h
D8h	32	EPWM_CMPB	500D 20D8h	5001 30D8h	5005 30D8h
DEh	16	EPWM_CMPC	500D 20DEh	5001 30DEh	5005 30DEh
E2h	16	EPWM_CMPD	500D 20E2h	5001 30E2h	5005 30E2h
E8h	16	EPWM_GLDCTL2	500D 20E8h	5001 30E8h	5005 30E8h
EEh	16	EPWM_SWVDELVAL	500D 20EEh	5001 30EEh	5005 30EEh
100h	16	EPWM_TZSEL	500D 2100h	5001 3100h	5005 3100h
102h	16	EPWM_TZSEL2	500D 2102h	5001 3102h	5005 3102h
104h	16	EPWM_TZDCSEL	500D 2104h	5001 3104h	5005 3104h
108h	16	EPWM_TZCTL	500D 2108h	5001 3108h	5005 3108h
10Ah	16	EPWM_TZCTL2	500D 210Ah	5001 310Ah	5005 310Ah
10Ch	16	EPWM_TZCTLDCA	500D 210Ch	5001 310Ch	5005 310Ch
10Eh	16	EPWM_TZCTLDCB	500D 210Eh	5001 310Eh	5005 310Eh
11Ah	16	EPWM_TZEINT	500D 211Ah	5001 311Ah	5005 311Ah
126h	16	EPWM_TZFLG	500D 2126h	5001 3126h	5005 3126h
128h	16	EPWM_TZCBCFLG	500D 2128h	5001 3128h	5005 3128h
12Ah	16	EPWM_TZOSTFLG	500D 212Ah	5001 312Ah	5005 312Ah
12Eh	16	EPWM_TZCLR	500D 212Eh	5001 312Eh	5005 312Eh
130h	16	EPWM_TZCBCCLR	500D 2130h	5001 3130h	5005 3130h
132h	16	EPWM_TZOSTCLR	500D 2132h	5001 3132h	5005 3132h
136h	16	EPWM_TZFRC	500D 2136h	5001 3136h	5005 3136h
13Ah	16	EPWM_TZTRIPOUTSEL	500D 213Ah	5001 313Ah	5005 313Ah

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Table 3-595. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM11_G2 Physical Address	EPWM12_G2 Physical Address	EPWM13_G2 Physical Address
148h	16	EPWM_ETSEL	500D 2148h	5001 3148h	5005 3148h
14Ch	16	EPWM_ETPS	500D 214Ch	5001 314Ch	5005 314Ch
150h	16	EPWM_ETFLG	500D 2150h	5001 3150h	5005 3150h
154h	16	EPWM_ETCLR	500D 2154h	5001 3154h	5005 3154h
158h	16	EPWM_ETFRC	500D 2158h	5001 3158h	5005 3158h
15Ch	16	EPWM_ETINTPS	500D 215Ch	5001 315Ch	5005 315Ch
160h	16	EPWM_ETSOCPS	500D 2160h	5001 3160h	5005 3160h
164h	16	EPWM_ETCNTINITCTL	500D 2164h	5001 3164h	5005 3164h
168h	16	EPWM_ETCNTINIT	500D 2168h	5001 3168h	5005 3168h
16Ch	16	EPWM_ETINTMIXEN	500D 216Ch	5001 316Ch	5005 316Ch
170h	16	EPWM_ETSOCAMIXEN	500D 2170h	5001 3170h	5005 3170h
174h	16	EPWM_ETSOCBMIXEN	500D 2174h	5001 3174h	5005 3174h
180h	16	EPWM_DCTRIPSEL	500D 2180h	5001 3180h	5005 3180h
186h	16	EPWM_DCACTL	500D 2186h	5001 3186h	5005 3186h
188h	16	EPWM_DCBCTL	500D 2188h	5001 3188h	5005 3188h
18Eh	16	EPWM_DCFCTL	500D 218Eh	5001 318Eh	5005 318Eh
190h	16	EPWM_DCCAPCTL	500D 2190h	5001 3190h	5005 3190h
192h	16	EPWM_DCFOFFSET	500D 2192h	5001 3192h	5005 3192h
194h	16	EPWM_DCFOFFSETCNT	500D 2194h	5001 3194h	5005 3194h
196h	16	EPWM_DCFWINDOW	500D 2196h	5001 3196h	5005 3196h
198h	16	EPWM_DCFWINDOWCNT	500D 2198h	5001 3198h	5005 3198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500D 219Ah	5001 319Ah	5005 319Ah
19Ch	16	EPWM_DCCAPMIXSEL	500D 219Ch	5001 319Ch	5005 319Ch
19Eh	16	EPWM_DCCAP	500D 219Eh	5001 319Eh	5005 319Eh
1A4h	16	EPWM_DCAHTRIPSEL	500D 21A4h	5001 31A4h	5005 31A4h
1A6h	16	EPWM_DCALTRIPSEL	500D 21A6h	5001 31A6h	5005 31A6h
1A8h	16	EPWM_DCBHTRIPSEL	500D 21A8h	5001 31A8h	5005 31A8h
1AAh	16	EPWM_DCBLTRIPSEL	500D 21AAh	5001 31AAh	5005 31AAh
1ACh	16	EPWM_CAPCTL	500D 21ACh	5001 31ACh	5005 31ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500D 21AEh	5001 31AEh	5005 31AEh
1B0h	16	EPWM_CAPINTRIPSEL	500D 21B0h	5001 31B0h	5005 31B0h
1B2h	16	EPWM_CAPTRIPSEL	500D 21B2h	5001 31B2h	5005 31B2h
1F4h	32	EPWM_EPWMLOCK	500D 21F4h	5001 31F4h	5005 31F4h
1FAh	16	EPWM_HWVDELVAL	500D 21FAh	5001 31FAh	5005 31FAh
1FCh	16	EPWM_VCNTVAL	500D 21FCh	5001 31FCh	5005 31FCh
400h	32	EPWM_XCMPCTL1	500D 2400h	5001 3400h	5005 3400h
410h	32	EPWM_XLOADCTL	500D 2410h	5001 3410h	5005 3410h
418h	32	EPWM_XLOAD	500D 2418h	5001 3418h	5005 3418h
41Ch	32	EPWM_EPWMXLINKXLOAD	500D 241Ch	5001 341Ch	5005 341Ch
420h	32	EPWM_XREGSHDW1STS	500D 2420h	5001 3420h	5005 3420h
428h	32	EPWM_XREGSHDW2STS	500D 2428h	5001 3428h	5005 3428h
430h	32	EPWM_XREGSHDW3STS	500D 2430h	5001 3430h	5005 3430h
600h	32	EPWM_XCMP1_ACTIVE	500D 2600h	5001 3600h	5005 3600h
604h	32	EPWM_XCMP2_ACTIVE	500D 2604h	5001 3604h	5005 3604h
608h	32	EPWM_XCMP3_ACTIVE	500D 2608h	5001 3608h	5005 3608h
60Ch	32	EPWM_XCMP4_ACTIVE	500D 260Ch	5001 360Ch	5005 360Ch

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Table 3-595. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM11_G2 Physical Address	EPWM12_G2 Physical Address	EPWM13_G2 Physical Address
610h	32	EPWM_XCMP5_ACTIVE	500D 2610h	5001 3610h	5005 3610h
614h	32	EPWM_XCMP6_ACTIVE	500D 2614h	5001 3614h	5005 3614h
618h	32	EPWM_XCMP7_ACTIVE	500D 2618h	5001 3618h	5005 3618h
61Ch	32	EPWM_XCMP8_ACTIVE	500D 261Ch	5001 361Ch	5005 361Ch
620h	32	EPWM_XTBPRD_ACTIVE	500D 2620h	5001 3620h	5005 3620h
630h	16	EPWM_XAQCTLA_ACTIVE	500D 2630h	5001 3630h	5005 3630h
644h	32	EPWM_XMINMAX_ACTIVE	500D 2644h	5001 3644h	5005 3644h
680h	32	EPWM_XCMP1_SHDW1	500D 2680h	5001 3680h	5005 3680h
684h	32	EPWM_XCMP2_SHDW1	500D 2684h	5001 3684h	5005 3684h
688h	32	EPWM_XCMP3_SHDW1	500D 2688h	5001 3688h	5005 3688h
68Ch	32	EPWM_XCMP4_SHDW1	500D 268Ch	5001 368Ch	5005 368Ch
690h	32	EPWM_XCMP5_SHDW1	500D 2690h	5001 3690h	5005 3690h
694h	32	EPWM_XCMP6_SHDW1	500D 2694h	5001 3694h	5005 3694h
698h	32	EPWM_XCMP7_SHDW1	500D 2698h	5001 3698h	5005 3698h
69Ch	32	EPWM_XCMP8_SHDW1	500D 269Ch	5001 369Ch	5005 369Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500D 26A0h	5001 36A0h	5005 36A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500D 26B0h	5001 36B0h	5005 36B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500D 26B2h	5001 36B2h	5005 36B2h
6BAh	16	EPWM_CMPC_SHDW1	500D 26BAh	5001 36BAh	5005 36BAh
6BEh	16	EPWM_CMPD_SHDW1	500D 26BEh	5001 36BEh	5005 36BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500D 26C4h	5001 36C4h	5005 36C4h
700h	32	EPWM_XCMP1_SHDW2	500D 2700h	5001 3700h	5005 3700h
704h	32	EPWM_XCMP2_SHDW2	500D 2704h	5001 3704h	5005 3704h
708h	32	EPWM_XCMP3_SHDW2	500D 2708h	5001 3708h	5005 3708h
70Ch	32	EPWM_XCMP4_SHDW2	500D 270Ch	5001 370Ch	5005 370Ch
710h	32	EPWM_XCMP5_SHDW2	500D 2710h	5001 3710h	5005 3710h
714h	32	EPWM_XCMP6_SHDW2	500D 2714h	5001 3714h	5005 3714h
718h	32	EPWM_XCMP7_SHDW2	500D 2718h	5001 3718h	5005 3718h
71Ch	32	EPWM_XCMP8_SHDW2	500D 271Ch	5001 371Ch	5005 371Ch
720h	32	EPWM_XTBPRD_SHDW2	500D 2720h	5001 3720h	5005 3720h
730h	16	EPWM_XAQCTLA_SHDW2	500D 2730h	5001 3730h	5005 3730h
732h	16	EPWM_XAQCTLB_SHDW2	500D 2732h	5001 3732h	5005 3732h
73Ah	16	EPWM_CMPC_SHDW2	500D 273Ah	5001 373Ah	5005 373Ah
73Eh	16	EPWM_CMPD_SHDW2	500D 273Eh	5001 373Eh	5005 373Eh
744h	32	EPWM_XMINMAX_SHDW2	500D 2744h	5001 3744h	5005 3744h
780h	32	EPWM_XCMP1_SHDW3	500D 2780h	5001 3780h	5005 3780h
784h	32	EPWM_XCMP2_SHDW3	500D 2784h	5001 3784h	5005 3784h
788h	32	EPWM_XCMP3_SHDW3	500D 2788h	5001 3788h	5005 3788h
78Ch	32	EPWM_XCMP4_SHDW3	500D 278Ch	5001 378Ch	5005 378Ch
790h	32	EPWM_XCMP5_SHDW3	500D 2790h	5001 3790h	5005 3790h
794h	32	EPWM_XCMP6_SHDW3	500D 2794h	5001 3794h	5005 3794h
798h	32	EPWM_XCMP7_SHDW3	500D 2798h	5001 3798h	5005 3798h
79Ch	32	EPWM_XCMP8_SHDW3	500D 279Ch	5001 379Ch	5005 379Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500D 27A0h	5001 37A0h	5005 37A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500D 27B0h	5001 37B0h	5005 37B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500D 27B2h	5001 37B2h	5005 37B2h

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Table 3-595. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM11_G2 Physical Address	EPWM12_G2 Physical Address	EPWM13_G2 Physical Address
7BAh	16	EPWM_CMPC_SHDW3	500D 27BAh	5001 37BAh	5005 37BAh
7BEh	16	EPWM_CMPD_SHDW3	500D 27BEh	5001 37BEh	5005 37BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500D 27C4h	5001 37C4h	5005 37C4h
800h	32	EPWM_DECTL	500D 2800h	5001 3800h	5005 3800h
804h	32	EPWM_DECOMPSEL	500D 2804h	5001 3804h	5005 3804h
808h	32	EPWM_DEACTCTL	500D 2808h	5001 3808h	5005 3808h
80Ch	32	EPWM_DESTS	500D 280Ch	5001 380Ch	5005 380Ch
810h	32	EPWM_DEFRC	500D 2810h	5001 3810h	5005 3810h
814h	32	EPWM_DECLR	500D 2814h	5001 3814h	5005 3814h
820h	32	EPWM_DEMONCNT	500D 2820h	5001 3820h	5005 3820h
824h	32	EPWM_DEMONCTL	500D 2824h	5001 3824h	5005 3824h
828h	32	EPWM_DEMONSTEP	500D 2828h	5001 3828h	5005 3828h
82Ch	32	EPWM_DEMONTHRES	500D 282Ch	5001 382Ch	5005 382Ch
C00h	32	EPWM_MINDBCFG	500D 2C00h	5001 3C00h	5005 3C00h
C04h	32	EPWM_MINDBDLY	500D 2C04h	5001 3C04h	5005 3C04h
C20h	32	EPWM_LUTCTLA	500D 2C20h	5001 3C20h	5005 3C20h
C24h	32	EPWM_LUTCTLB	500D 2C24h	5001 3C24h	5005 3C24h

Table 3-596. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM14_G2 Physical Address	EPWM15_G2 Physical Address	EPWM16_G2 Physical Address
0h	16	EPWM_TBCTL	5009 3000h	500D 3000h	5001 4000h
2h	16	EPWM_TBCTL2	5009 3002h	500D 3002h	5001 4002h
6h	16	EPWM_EPWMSYNCINSEL	5009 3006h	500D 3006h	5001 4006h
8h	16	EPWM_TBCTR	5009 3008h	500D 3008h	5001 4008h
Ah	16	EPWM_TBSTS	5009 300Ah	500D 300Ah	5001 400Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5009 300Ch	500D 300Ch	5001 400Ch
Eh	16	EPWM_TBCTL3	5009 300Eh	500D 300Eh	5001 400Eh
10h	16	EPWM_CMPCTL	5009 3010h	500D 3010h	5001 4010h
12h	16	EPWM_CMPCTL2	5009 3012h	500D 3012h	5001 4012h
18h	16	EPWM_DBCTL	5009 3018h	500D 3018h	5001 4018h
1Ah	16	EPWM_DBCTL2	5009 301Ah	500D 301Ah	5001 401Ah
20h	16	EPWM_AQCTL	5009 3020h	500D 3020h	5001 4020h
22h	16	EPWM_AQTSRCSEL	5009 3022h	500D 3022h	5001 4022h
28h	16	EPWM_PCCTL	5009 3028h	500D 3028h	5001 4028h
30h	16	EPWM_VCAPCTL	5009 3030h	500D 3030h	5001 4030h
32h	16	EPWM_VCNTCFG	5009 3032h	500D 3032h	5001 4032h
40h	16	EPWM_HRCNFG	5009 3040h	500D 3040h	5001 4040h
4Eh	16	EPWM_HRCNFG2	5009 304Eh	500D 304Eh	5001 404Eh
5Ah	16	EPWM_HRPCTL	5009 305Ah	500D 305Ah	5001 405Ah
5Ch	16	EPWM_TRREM	5009 305Ch	500D 305Ch	5001 405Ch
68h	16	EPWM_GLDCTL	5009 3068h	500D 3068h	5001 4068h
6Ah	16	EPWM_GLDCFG	5009 306Ah	500D 306Ah	5001 406Ah
70h	32	EPWM_EPWMXLINK	5009 3070h	500D 3070h	5001 4070h
74h	32	EPWM_EPWMXLINK2	5009 3074h	500D 3074h	5001 4074h
7Ah	16	EPWM_ETEST	5009 307Ah	500D 307Ah	5001 407Ah

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Table 3-596. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM14_G2 Physical Address	EPWM15_G2 Physical Address	EPWM16_G2 Physical Address
7Ch	16	EPWM_EPWMREV	5009 307Ch	500D 307Ch	5001 407Ch
7Eh	16	EPWM_HRPWMREV	5009 307Eh	500D 307Eh	5001 407Eh
80h	16	EPWM_AQCTLA	5009 3080h	500D 3080h	5001 4080h
82h	16	EPWM_AQCTLA2	5009 3082h	500D 3082h	5001 4082h
84h	16	EPWM_AQCTLB	5009 3084h	500D 3084h	5001 4084h
86h	16	EPWM_AQCTLB2	5009 3086h	500D 3086h	5001 4086h
8Eh	16	EPWM_AQSFRC	5009 308Eh	500D 308Eh	5001 408Eh
92h	16	EPWM_AQCSFRC	5009 3092h	500D 3092h	5001 4092h
A0h	16	EPWM_DBREDHR	5009 30A0h	500D 30A0h	5001 40A0h
A2h	16	EPWM_DBRED	5009 30A2h	500D 30A2h	5001 40A2h
A4h	16	EPWM_DBFEDHR	5009 30A4h	500D 30A4h	5001 40A4h
A6h	16	EPWM_DBFED	5009 30A6h	500D 30A6h	5001 40A6h
C0h	32	EPWM_TBPHS	5009 30C0h	500D 30C0h	5001 40C0h
C4h	16	EPWM_TBPRDHR	5009 30C4h	500D 30C4h	5001 40C4h
C6h	16	EPWM_TBPRD	5009 30C6h	500D 30C6h	5001 40C6h
C8h	16	EPWM_TBPRDHRB	5009 30C8h	500D 30C8h	5001 40C8h
D4h	32	EPWM_CMPA	5009 30D4h	500D 30D4h	5001 40D4h
D8h	32	EPWM_CMPB	5009 30D8h	500D 30D8h	5001 40D8h
DEh	16	EPWM_CMPC	5009 30DEh	500D 30DEh	5001 40DEh
E2h	16	EPWM_CMPD	5009 30E2h	500D 30E2h	5001 40E2h
E8h	16	EPWM_GLDCTL2	5009 30E8h	500D 30E8h	5001 40E8h
EEh	16	EPWM_SWVDELVAL	5009 30EEh	500D 30EEh	5001 40EEh
100h	16	EPWM_TZSEL	5009 3100h	500D 3100h	5001 4100h
102h	16	EPWM_TZSEL2	5009 3102h	500D 3102h	5001 4102h
104h	16	EPWM_TZDCSEL	5009 3104h	500D 3104h	5001 4104h
108h	16	EPWM_TZCTL	5009 3108h	500D 3108h	5001 4108h
10Ah	16	EPWM_TZCTL2	5009 310Ah	500D 310Ah	5001 410Ah
10Ch	16	EPWM_TZCTLDCA	5009 310Ch	500D 310Ch	5001 410Ch
10Eh	16	EPWM_TZCTLDCB	5009 310Eh	500D 310Eh	5001 410Eh
11Ah	16	EPWM_TZEINT	5009 311Ah	500D 311Ah	5001 411Ah
126h	16	EPWM_TZFLG	5009 3126h	500D 3126h	5001 4126h
128h	16	EPWM_TZCBCFLG	5009 3128h	500D 3128h	5001 4128h
12Ah	16	EPWM_TZOSTFLG	5009 312Ah	500D 312Ah	5001 412Ah
12Eh	16	EPWM_TZCLR	5009 312Eh	500D 312Eh	5001 412Eh
130h	16	EPWM_TZCBCCLR	5009 3130h	500D 3130h	5001 4130h
132h	16	EPWM_TZOSTCLR	5009 3132h	500D 3132h	5001 4132h
136h	16	EPWM_TZFRC	5009 3136h	500D 3136h	5001 4136h
13Ah	16	EPWM_TZTRIPOUTSEL	5009 313Ah	500D 313Ah	5001 413Ah
148h	16	EPWM_ETSEL	5009 3148h	500D 3148h	5001 4148h
14Ch	16	EPWM_ETPS	5009 314Ch	500D 314Ch	5001 414Ch
150h	16	EPWM_ETFLG	5009 3150h	500D 3150h	5001 4150h
154h	16	EPWM_ETCLR	5009 3154h	500D 3154h	5001 4154h
158h	16	EPWM_ETFRC	5009 3158h	500D 3158h	5001 4158h
15Ch	16	EPWM_ETINTPS	5009 315Ch	500D 315Ch	5001 415Ch
160h	16	EPWM_ETSOCPS	5009 3160h	500D 3160h	5001 4160h
164h	16	EPWM_ETCNTINITCTL	5009 3164h	500D 3164h	5001 4164h

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Table 3-596. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM14_G2 Physical Address	EPWM15_G2 Physical Address	EPWM16_G2 Physical Address
168h	16	EPWM_ETCNTINIT	5009 3168h	500D 3168h	5001 4168h
16Ch	16	EPWM_ETINTMIXEN	5009 316Ch	500D 316Ch	5001 416Ch
170h	16	EPWM_ETSOCAMIXEN	5009 3170h	500D 3170h	5001 4170h
174h	16	EPWM_ETSOCBMIXEN	5009 3174h	500D 3174h	5001 4174h
180h	16	EPWM_DCTRIPSEL	5009 3180h	500D 3180h	5001 4180h
186h	16	EPWM_DCACTL	5009 3186h	500D 3186h	5001 4186h
188h	16	EPWM_DCBCTL	5009 3188h	500D 3188h	5001 4188h
18Eh	16	EPWM_DCFCTL	5009 318Eh	500D 318Eh	5001 418Eh
190h	16	EPWM_DCCAPCTL	5009 3190h	500D 3190h	5001 4190h
192h	16	EPWM_DCFOFFSET	5009 3192h	500D 3192h	5001 4192h
194h	16	EPWM_DCFOFFSETCNT	5009 3194h	500D 3194h	5001 4194h
196h	16	EPWM_DCFWINDOW	5009 3196h	500D 3196h	5001 4196h
198h	16	EPWM_DCFWINDOWCNT	5009 3198h	500D 3198h	5001 4198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5009 319Ah	500D 319Ah	5001 419Ah
19Ch	16	EPWM_DCCAPMIXSEL	5009 319Ch	500D 319Ch	5001 419Ch
19Eh	16	EPWM_DCCAP	5009 319Eh	500D 319Eh	5001 419Eh
1A4h	16	EPWM_DCAHTRIPSEL	5009 31A4h	500D 31A4h	5001 41A4h
1A6h	16	EPWM_DCALTRIPSEL	5009 31A6h	500D 31A6h	5001 41A6h
1A8h	16	EPWM_DCBHTRIPSEL	5009 31A8h	500D 31A8h	5001 41A8h
1AAh	16	EPWM_DCBLTRIPSEL	5009 31AAh	500D 31AAh	5001 41AAh
1ACh	16	EPWM_CAPCTL	5009 31ACh	500D 31ACh	5001 41ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5009 31AEh	500D 31AEh	5001 41AEh
1B0h	16	EPWM_CAPINTRIPSEL	5009 31B0h	500D 31B0h	5001 41B0h
1B2h	16	EPWM_CAPTRIPSEL	5009 31B2h	500D 31B2h	5001 41B2h
1F4h	32	EPWM_EPWMLOCK	5009 31F4h	500D 31F4h	5001 41F4h
1FAh	16	EPWM_HWVDELVAL	5009 31FAh	500D 31FAh	5001 41FAh
1FCh	16	EPWM_VCNTVAL	5009 31FCh	500D 31FCh	5001 41FCh
400h	32	EPWM_XCMPCTL1	5009 3400h	500D 3400h	5001 4400h
410h	32	EPWM_XLOADCTL	5009 3410h	500D 3410h	5001 4410h
418h	32	EPWM_XLOAD	5009 3418h	500D 3418h	5001 4418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5009 341Ch	500D 341Ch	5001 441Ch
420h	32	EPWM_XREGSHDW1STS	5009 3420h	500D 3420h	5001 4420h
428h	32	EPWM_XREGSHDW2STS	5009 3428h	500D 3428h	5001 4428h
430h	32	EPWM_XREGSHDW3STS	5009 3430h	500D 3430h	5001 4430h
600h	32	EPWM_XCMP1_ACTIVE	5009 3600h	500D 3600h	5001 4600h
604h	32	EPWM_XCMP2_ACTIVE	5009 3604h	500D 3604h	5001 4604h
608h	32	EPWM_XCMP3_ACTIVE	5009 3608h	500D 3608h	5001 4608h
60Ch	32	EPWM_XCMP4_ACTIVE	5009 360Ch	500D 360Ch	5001 460Ch
610h	32	EPWM_XCMP5_ACTIVE	5009 3610h	500D 3610h	5001 4610h
614h	32	EPWM_XCMP6_ACTIVE	5009 3614h	500D 3614h	5001 4614h
618h	32	EPWM_XCMP7_ACTIVE	5009 3618h	500D 3618h	5001 4618h
61Ch	32	EPWM_XCMP8_ACTIVE	5009 361Ch	500D 361Ch	5001 461Ch
620h	32	EPWM_XTBPRD_ACTIVE	5009 3620h	500D 3620h	5001 4620h
630h	16	EPWM_XAQCTLA_ACTIVE	5009 3630h	500D 3630h	5001 4630h
644h	32	EPWM_XMINMAX_ACTIVE	5009 3644h	500D 3644h	5001 4644h
680h	32	EPWM_XCMP1_SHDW1	5009 3680h	500D 3680h	5001 4680h

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Table 3-596. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM14_G2 Physical Address	EPWM15_G2 Physical Address	EPWM16_G2 Physical Address
684h	32	EPWM_XCMP2_SHDW1	5009 3684h	500D 3684h	5001 4684h
688h	32	EPWM_XCMP3_SHDW1	5009 3688h	500D 3688h	5001 4688h
68Ch	32	EPWM_XCMP4_SHDW1	5009 368Ch	500D 368Ch	5001 468Ch
690h	32	EPWM_XCMP5_SHDW1	5009 3690h	500D 3690h	5001 4690h
694h	32	EPWM_XCMP6_SHDW1	5009 3694h	500D 3694h	5001 4694h
698h	32	EPWM_XCMP7_SHDW1	5009 3698h	500D 3698h	5001 4698h
69Ch	32	EPWM_XCMP8_SHDW1	5009 369Ch	500D 369Ch	5001 469Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5009 36A0h	500D 36A0h	5001 46A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5009 36B0h	500D 36B0h	5001 46B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5009 36B2h	500D 36B2h	5001 46B2h
6BAh	16	EPWM_CMPC_SHDW1	5009 36BAh	500D 36BAh	5001 46BAh
6BEh	16	EPWM_CMPD_SHDW1	5009 36BEh	500D 36BEh	5001 46BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5009 36C4h	500D 36C4h	5001 46C4h
700h	32	EPWM_XCMP1_SHDW2	5009 3700h	500D 3700h	5001 4700h
704h	32	EPWM_XCMP2_SHDW2	5009 3704h	500D 3704h	5001 4704h
708h	32	EPWM_XCMP3_SHDW2	5009 3708h	500D 3708h	5001 4708h
70Ch	32	EPWM_XCMP4_SHDW2	5009 370Ch	500D 370Ch	5001 470Ch
710h	32	EPWM_XCMP5_SHDW2	5009 3710h	500D 3710h	5001 4710h
714h	32	EPWM_XCMP6_SHDW2	5009 3714h	500D 3714h	5001 4714h
718h	32	EPWM_XCMP7_SHDW2	5009 3718h	500D 3718h	5001 4718h
71Ch	32	EPWM_XCMP8_SHDW2	5009 371Ch	500D 371Ch	5001 471Ch
720h	32	EPWM_XTBPRD_SHDW2	5009 3720h	500D 3720h	5001 4720h
730h	16	EPWM_XAQCTLA_SHDW2	5009 3730h	500D 3730h	5001 4730h
732h	16	EPWM_XAQCTLB_SHDW2	5009 3732h	500D 3732h	5001 4732h
73Ah	16	EPWM_CMPC_SHDW2	5009 373Ah	500D 373Ah	5001 473Ah
73Eh	16	EPWM_CMPD_SHDW2	5009 373Eh	500D 373Eh	5001 473Eh
744h	32	EPWM_XMINMAX_SHDW2	5009 3744h	500D 3744h	5001 4744h
780h	32	EPWM_XCMP1_SHDW3	5009 3780h	500D 3780h	5001 4780h
784h	32	EPWM_XCMP2_SHDW3	5009 3784h	500D 3784h	5001 4784h
788h	32	EPWM_XCMP3_SHDW3	5009 3788h	500D 3788h	5001 4788h
78Ch	32	EPWM_XCMP4_SHDW3	5009 378Ch	500D 378Ch	5001 478Ch
790h	32	EPWM_XCMP5_SHDW3	5009 3790h	500D 3790h	5001 4790h
794h	32	EPWM_XCMP6_SHDW3	5009 3794h	500D 3794h	5001 4794h
798h	32	EPWM_XCMP7_SHDW3	5009 3798h	500D 3798h	5001 4798h
79Ch	32	EPWM_XCMP8_SHDW3	5009 379Ch	500D 379Ch	5001 479Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5009 37A0h	500D 37A0h	5001 47A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5009 37B0h	500D 37B0h	5001 47B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5009 37B2h	500D 37B2h	5001 47B2h
7BAh	16	EPWM_CMPC_SHDW3	5009 37BAh	500D 37BAh	5001 47BAh
7BEh	16	EPWM_CMPD_SHDW3	5009 37BEh	500D 37BEh	5001 47BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5009 37C4h	500D 37C4h	5001 47C4h
800h	32	EPWM_DECTL	5009 3800h	500D 3800h	5001 4800h
804h	32	EPWM_DECOMPSEL	5009 3804h	500D 3804h	5001 4804h
808h	32	EPWM_DEACTCTL	5009 3808h	500D 3808h	5001 4808h
80Ch	32	EPWM_DESTS	5009 380Ch	500D 380Ch	5001 480Ch
810h	32	EPWM_DEFRC	5009 3810h	500D 3810h	5001 4810h

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Table 3-596. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM14_G2 Physical Address	EPWM15_G2 Physical Address	EPWM16_G2 Physical Address
814h	32	EPWM_DECLR	5009 3814h	500D 3814h	5001 4814h
820h	32	EPWM_DEMONCNT	5009 3820h	500D 3820h	5001 4820h
824h	32	EPWM_DEMONCTL	5009 3824h	500D 3824h	5001 4824h
828h	32	EPWM_DEMONSTEP	5009 3828h	500D 3828h	5001 4828h
82Ch	32	EPWM_DEMONTHRES	5009 382Ch	500D 382Ch	5001 482Ch
C00h	32	EPWM_MINDBCFG	5009 3C00h	500D 3C00h	5001 4C00h
C04h	32	EPWM_MINDBDLY	5009 3C04h	500D 3C04h	5001 4C04h
C20h	32	EPWM_LUTCTLA	5009 3C20h	500D 3C20h	5001 4C20h
C24h	32	EPWM_LUTCTLB	5009 3C24h	500D 3C24h	5001 4C24h

Table 3-597. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM17_G2 Physical Address	EPWM18_G2 Physical Address	EPWM19_G2 Physical Address
0h	16	EPWM_TBCTL	5005 4000h	5009 4000h	500D 4000h
2h	16	EPWM_TBCTL2	5005 4002h	5009 4002h	500D 4002h
6h	16	EPWM_EPWMSYNCINSEL	5005 4006h	5009 4006h	500D 4006h
8h	16	EPWM_TBCTR	5005 4008h	5009 4008h	500D 4008h
Ah	16	EPWM_TBSTS	5005 400Ah	5009 400Ah	500D 400Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5005 400Ch	5009 400Ch	500D 400Ch
Eh	16	EPWM_TBCTL3	5005 400Eh	5009 400Eh	500D 400Eh
10h	16	EPWM_CMPCTL	5005 4010h	5009 4010h	500D 4010h
12h	16	EPWM_CMPCTL2	5005 4012h	5009 4012h	500D 4012h
18h	16	EPWM_DBCTL	5005 4018h	5009 4018h	500D 4018h
1Ah	16	EPWM_DBCTL2	5005 401Ah	5009 401Ah	500D 401Ah
20h	16	EPWM_AQCTL	5005 4020h	5009 4020h	500D 4020h
22h	16	EPWM_AQTSRCSEL	5005 4022h	5009 4022h	500D 4022h
28h	16	EPWM_PCCTL	5005 4028h	5009 4028h	500D 4028h
30h	16	EPWM_VCAPCTL	5005 4030h	5009 4030h	500D 4030h
32h	16	EPWM_VCNTCFG	5005 4032h	5009 4032h	500D 4032h
40h	16	EPWM_HRCNFG	5005 4040h	5009 4040h	500D 4040h
4Eh	16	EPWM_HRCNFG2	5005 404Eh	5009 404Eh	500D 404Eh
5Ah	16	EPWM_HRPCTL	5005 405Ah	5009 405Ah	500D 405Ah
5Ch	16	EPWM_TRREM	5005 405Ch	5009 405Ch	500D 405Ch
68h	16	EPWM_GLDCTL	5005 4068h	5009 4068h	500D 4068h
6Ah	16	EPWM_GLDCFG	5005 406Ah	5009 406Ah	500D 406Ah
70h	32	EPWM_EPWMXLINK	5005 4070h	5009 4070h	500D 4070h
74h	32	EPWM_EPWMXLINK2	5005 4074h	5009 4074h	500D 4074h
7Ah	16	EPWM_ETEST	5005 407Ah	5009 407Ah	500D 407Ah
7Ch	16	EPWM_EPWMREV	5005 407Ch	5009 407Ch	500D 407Ch
7Eh	16	EPWM_HRPWMREV	5005 407Eh	5009 407Eh	500D 407Eh
80h	16	EPWM_AQCTLA	5005 4080h	5009 4080h	500D 4080h
82h	16	EPWM_AQCTLA2	5005 4082h	5009 4082h	500D 4082h
84h	16	EPWM_AQCTLB	5005 4084h	5009 4084h	500D 4084h
86h	16	EPWM_AQCTLB2	5005 4086h	5009 4086h	500D 4086h
8Eh	16	EPWM_AQSFRC	5005 408Eh	5009 408Eh	500D 408Eh
92h	16	EPWM_AQCSFRC	5005 4092h	5009 4092h	500D 4092h

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Table 3-597. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM17_G2 Physical Address	EPWM18_G2 Physical Address	EPWM19_G2 Physical Address
A0h	16	EPWM_DBREDHR	5005 40A0h	5009 40A0h	500D 40A0h
A2h	16	EPWM_DBRED	5005 40A2h	5009 40A2h	500D 40A2h
A4h	16	EPWM_DBFEDHR	5005 40A4h	5009 40A4h	500D 40A4h
A6h	16	EPWM_DBFED	5005 40A6h	5009 40A6h	500D 40A6h
C0h	32	EPWM_TBPHS	5005 40C0h	5009 40C0h	500D 40C0h
C4h	16	EPWM_TBPRDHR	5005 40C4h	5009 40C4h	500D 40C4h
C6h	16	EPWM_TBPRD	5005 40C6h	5009 40C6h	500D 40C6h
C8h	16	EPWM_TBPRDHRB	5005 40C8h	5009 40C8h	500D 40C8h
D4h	32	EPWM_CMPA	5005 40D4h	5009 40D4h	500D 40D4h
D8h	32	EPWM_CMPB	5005 40D8h	5009 40D8h	500D 40D8h
DEh	16	EPWM_CMPC	5005 40DEh	5009 40DEh	500D 40DEh
E2h	16	EPWM_CMPD	5005 40E2h	5009 40E2h	500D 40E2h
E8h	16	EPWM_GLDCTL2	5005 40E8h	5009 40E8h	500D 40E8h
EEh	16	EPWM_SWVDELVAL	5005 40EEh	5009 40EEh	500D 40EEh
100h	16	EPWM_TZSEL	5005 4100h	5009 4100h	500D 4100h
102h	16	EPWM_TZSEL2	5005 4102h	5009 4102h	500D 4102h
104h	16	EPWM_TZDCSEL	5005 4104h	5009 4104h	500D 4104h
108h	16	EPWM_TZCTL	5005 4108h	5009 4108h	500D 4108h
10Ah	16	EPWM_TZCTL2	5005 410Ah	5009 410Ah	500D 410Ah
10Ch	16	EPWM_TZCTLDCA	5005 410Ch	5009 410Ch	500D 410Ch
10Eh	16	EPWM_TZCTLDCB	5005 410Eh	5009 410Eh	500D 410Eh
11Ah	16	EPWM_TZEINT	5005 411Ah	5009 411Ah	500D 411Ah
126h	16	EPWM_TZFLG	5005 4126h	5009 4126h	500D 4126h
128h	16	EPWM_TZCBCFLG	5005 4128h	5009 4128h	500D 4128h
12Ah	16	EPWM_TZOSTFLG	5005 412Ah	5009 412Ah	500D 412Ah
12Eh	16	EPWM_TZCLR	5005 412Eh	5009 412Eh	500D 412Eh
130h	16	EPWM_TZCBCCLR	5005 4130h	5009 4130h	500D 4130h
132h	16	EPWM_TZOSTCLR	5005 4132h	5009 4132h	500D 4132h
136h	16	EPWM_TZFRC	5005 4136h	5009 4136h	500D 4136h
13Ah	16	EPWM_TZTRIPOUTSEL	5005 413Ah	5009 413Ah	500D 413Ah
148h	16	EPWM_ETSEL	5005 4148h	5009 4148h	500D 4148h
14Ch	16	EPWM_ETPS	5005 414Ch	5009 414Ch	500D 414Ch
150h	16	EPWM_ETFLG	5005 4150h	5009 4150h	500D 4150h
154h	16	EPWM_ETCLR	5005 4154h	5009 4154h	500D 4154h
158h	16	EPWM_ETFRC	5005 4158h	5009 4158h	500D 4158h
15Ch	16	EPWM_ETINTPS	5005 415Ch	5009 415Ch	500D 415Ch
160h	16	EPWM_ETSOCPS	5005 4160h	5009 4160h	500D 4160h
164h	16	EPWM_ETCNTINITCTL	5005 4164h	5009 4164h	500D 4164h
168h	16	EPWM_ETCNTINIT	5005 4168h	5009 4168h	500D 4168h
16Ch	16	EPWM_ETINTMIXEN	5005 416Ch	5009 416Ch	500D 416Ch
170h	16	EPWM_ETSOCAMIXEN	5005 4170h	5009 4170h	500D 4170h
174h	16	EPWM_ETSOCBMIXEN	5005 4174h	5009 4174h	500D 4174h
180h	16	EPWM_DCTRIPSEL	5005 4180h	5009 4180h	500D 4180h
186h	16	EPWM_DCACTL	5005 4186h	5009 4186h	500D 4186h
188h	16	EPWM_DCBCTL	5005 4188h	5009 4188h	500D 4188h
18Eh	16	EPWM_DCFCTL	5005 418Eh	5009 418Eh	500D 418Eh

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Table 3-597. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM17_G2 Physical Address	EPWM18_G2 Physical Address	EPWM19_G2 Physical Address
190h	16	EPWM_DCCAPCTL	5005 4190h	5009 4190h	500D 4190h
192h	16	EPWM_DCFOFFSET	5005 4192h	5009 4192h	500D 4192h
194h	16	EPWM_DCFOFFSETCNT	5005 4194h	5009 4194h	500D 4194h
196h	16	EPWM_DCFWINDOW	5005 4196h	5009 4196h	500D 4196h
198h	16	EPWM_DCFWINDOWCNT	5005 4198h	5009 4198h	500D 4198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5005 419Ah	5009 419Ah	500D 419Ah
19Ch	16	EPWM_DCCAPMIXSEL	5005 419Ch	5009 419Ch	500D 419Ch
19Eh	16	EPWM_DCCAP	5005 419Eh	5009 419Eh	500D 419Eh
1A4h	16	EPWM_DCAHTRIPSEL	5005 41A4h	5009 41A4h	500D 41A4h
1A6h	16	EPWM_DCALTRIPSEL	5005 41A6h	5009 41A6h	500D 41A6h
1A8h	16	EPWM_DCBHTRIPSEL	5005 41A8h	5009 41A8h	500D 41A8h
1AAh	16	EPWM_DCBLTRIPSEL	5005 41AAh	5009 41AAh	500D 41AAh
1ACh	16	EPWM_CAPCTL	5005 41ACh	5009 41ACh	500D 41ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5005 41AEh	5009 41AEh	500D 41AEh
1B0h	16	EPWM_CAPINTRIPSEL	5005 41B0h	5009 41B0h	500D 41B0h
1B2h	16	EPWM_CAPTRIPSEL	5005 41B2h	5009 41B2h	500D 41B2h
1F4h	32	EPWM_EPWMLOCK	5005 41F4h	5009 41F4h	500D 41F4h
1FAh	16	EPWM_HWVDELVAL	5005 41FAh	5009 41FAh	500D 41FAh
1FCh	16	EPWM_VCNTVAL	5005 41FCh	5009 41FCh	500D 41FCh
400h	32	EPWM_XCMPCTL1	5005 4400h	5009 4400h	500D 4400h
410h	32	EPWM_XLOADCTL	5005 4410h	5009 4410h	500D 4410h
418h	32	EPWM_XLOAD	5005 4418h	5009 4418h	500D 4418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5005 441Ch	5009 441Ch	500D 441Ch
420h	32	EPWM_XREGSHDW1STS	5005 4420h	5009 4420h	500D 4420h
428h	32	EPWM_XREGSHDW2STS	5005 4428h	5009 4428h	500D 4428h
430h	32	EPWM_XREGSHDW3STS	5005 4430h	5009 4430h	500D 4430h
600h	32	EPWM_XCMP1_ACTIVE	5005 4600h	5009 4600h	500D 4600h
604h	32	EPWM_XCMP2_ACTIVE	5005 4604h	5009 4604h	500D 4604h
608h	32	EPWM_XCMP3_ACTIVE	5005 4608h	5009 4608h	500D 4608h
60Ch	32	EPWM_XCMP4_ACTIVE	5005 460Ch	5009 460Ch	500D 460Ch
610h	32	EPWM_XCMP5_ACTIVE	5005 4610h	5009 4610h	500D 4610h
614h	32	EPWM_XCMP6_ACTIVE	5005 4614h	5009 4614h	500D 4614h
618h	32	EPWM_XCMP7_ACTIVE	5005 4618h	5009 4618h	500D 4618h
61Ch	32	EPWM_XCMP8_ACTIVE	5005 461Ch	5009 461Ch	500D 461Ch
620h	32	EPWM_XTBPRD_ACTIVE	5005 4620h	5009 4620h	500D 4620h
630h	16	EPWM_XAQCTLA_ACTIVE	5005 4630h	5009 4630h	500D 4630h
644h	32	EPWM_XMINMAX_ACTIVE	5005 4644h	5009 4644h	500D 4644h
680h	32	EPWM_XCMP1_SHDW1	5005 4680h	5009 4680h	500D 4680h
684h	32	EPWM_XCMP2_SHDW1	5005 4684h	5009 4684h	500D 4684h
688h	32	EPWM_XCMP3_SHDW1	5005 4688h	5009 4688h	500D 4688h
68Ch	32	EPWM_XCMP4_SHDW1	5005 468Ch	5009 468Ch	500D 468Ch
690h	32	EPWM_XCMP5_SHDW1	5005 4690h	5009 4690h	500D 4690h
694h	32	EPWM_XCMP6_SHDW1	5005 4694h	5009 4694h	500D 4694h
698h	32	EPWM_XCMP7_SHDW1	5005 4698h	5009 4698h	500D 4698h
69Ch	32	EPWM_XCMP8_SHDW1	5005 469Ch	5009 469Ch	500D 469Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5005 46A0h	5009 46A0h	500D 46A0h

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Table 3-597. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM17_G2 Physical Address	EPWM18_G2 Physical Address	EPWM19_G2 Physical Address
6B0h	16	EPWM_XAQCTLA_SHDW1	5005 46B0h	5009 46B0h	500D 46B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5005 46B2h	5009 46B2h	500D 46B2h
6BAh	16	EPWM_CMPC_SHDW1	5005 46BAh	5009 46BAh	500D 46BAh
6BEh	16	EPWM_CMPD_SHDW1	5005 46BEh	5009 46BEh	500D 46BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5005 46C4h	5009 46C4h	500D 46C4h
700h	32	EPWM_XCMP1_SHDW2	5005 4700h	5009 4700h	500D 4700h
704h	32	EPWM_XCMP2_SHDW2	5005 4704h	5009 4704h	500D 4704h
708h	32	EPWM_XCMP3_SHDW2	5005 4708h	5009 4708h	500D 4708h
70Ch	32	EPWM_XCMP4_SHDW2	5005 470Ch	5009 470Ch	500D 470Ch
710h	32	EPWM_XCMP5_SHDW2	5005 4710h	5009 4710h	500D 4710h
714h	32	EPWM_XCMP6_SHDW2	5005 4714h	5009 4714h	500D 4714h
718h	32	EPWM_XCMP7_SHDW2	5005 4718h	5009 4718h	500D 4718h
71Ch	32	EPWM_XCMP8_SHDW2	5005 471Ch	5009 471Ch	500D 471Ch
720h	32	EPWM_XTBPRD_SHDW2	5005 4720h	5009 4720h	500D 4720h
730h	16	EPWM_XAQCTLA_SHDW2	5005 4730h	5009 4730h	500D 4730h
732h	16	EPWM_XAQCTLB_SHDW2	5005 4732h	5009 4732h	500D 4732h
73Ah	16	EPWM_CMPC_SHDW2	5005 473Ah	5009 473Ah	500D 473Ah
73Eh	16	EPWM_CMPD_SHDW2	5005 473Eh	5009 473Eh	500D 473Eh
744h	32	EPWM_XMINMAX_SHDW2	5005 4744h	5009 4744h	500D 4744h
780h	32	EPWM_XCMP1_SHDW3	5005 4780h	5009 4780h	500D 4780h
784h	32	EPWM_XCMP2_SHDW3	5005 4784h	5009 4784h	500D 4784h
788h	32	EPWM_XCMP3_SHDW3	5005 4788h	5009 4788h	500D 4788h
78Ch	32	EPWM_XCMP4_SHDW3	5005 478Ch	5009 478Ch	500D 478Ch
790h	32	EPWM_XCMP5_SHDW3	5005 4790h	5009 4790h	500D 4790h
794h	32	EPWM_XCMP6_SHDW3	5005 4794h	5009 4794h	500D 4794h
798h	32	EPWM_XCMP7_SHDW3	5005 4798h	5009 4798h	500D 4798h
79Ch	32	EPWM_XCMP8_SHDW3	5005 479Ch	5009 479Ch	500D 479Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5005 47A0h	5009 47A0h	500D 47A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5005 47B0h	5009 47B0h	500D 47B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5005 47B2h	5009 47B2h	500D 47B2h
7BAh	16	EPWM_CMPC_SHDW3	5005 47BAh	5009 47BAh	500D 47BAh
7BEh	16	EPWM_CMPD_SHDW3	5005 47BEh	5009 47BEh	500D 47BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5005 47C4h	5009 47C4h	500D 47C4h
800h	32	EPWM_DECTL	5005 4800h	5009 4800h	500D 4800h
804h	32	EPWM_DECOMPSEL	5005 4804h	5009 4804h	500D 4804h
808h	32	EPWM_DEACTCTL	5005 4808h	5009 4808h	500D 4808h
80Ch	32	EPWM_DESTS	5005 480Ch	5009 480Ch	500D 480Ch
810h	32	EPWM_DEFRC	5005 4810h	5009 4810h	500D 4810h
814h	32	EPWM_DECLR	5005 4814h	5009 4814h	500D 4814h
820h	32	EPWM_DEMONCNT	5005 4820h	5009 4820h	500D 4820h
824h	32	EPWM_DEMONCTL	5005 4824h	5009 4824h	500D 4824h
828h	32	EPWM_DEMONSTEP	5005 4828h	5009 4828h	500D 4828h
82Ch	32	EPWM_DEMONTHRES	5005 482Ch	5009 482Ch	500D 482Ch
C00h	32	EPWM_MINDBCFG	5005 4C00h	5009 4C00h	500D 4C00h
C04h	32	EPWM_MINDBDLY	5005 4C04h	5009 4C04h	500D 4C04h
C20h	32	EPWM_LUTCTLA	5005 4C20h	5009 4C20h	500D 4C20h

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Table 3-597. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM17_G2 Physical Address	EPWM18_G2 Physical Address	EPWM19_G2 Physical Address
C24h	32	EPWM_LUTCTLB	5005 4C24h	5009 4C24h	500D 4C24h

Table 3-598. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM20_G2 Physical Address	EPWM21_G2 Physical Address	EPWM22_G2 Physical Address
0h	16	EPWM_TBCTL	5001 5000h	5005 5000h	5009 5000h
2h	16	EPWM_TBCTL2	5001 5002h	5005 5002h	5009 5002h
6h	16	EPWM_EPWMSYNCINSEL	5001 5006h	5005 5006h	5009 5006h
8h	16	EPWM_TBCTR	5001 5008h	5005 5008h	5009 5008h
Ah	16	EPWM_TBSTS	5001 500Ah	5005 500Ah	5009 500Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5001 500Ch	5005 500Ch	5009 500Ch
Eh	16	EPWM_TBCTL3	5001 500Eh	5005 500Eh	5009 500Eh
10h	16	EPWM_CMPCTL	5001 5010h	5005 5010h	5009 5010h
12h	16	EPWM_CMPCTL2	5001 5012h	5005 5012h	5009 5012h
18h	16	EPWM_DBCTL	5001 5018h	5005 5018h	5009 5018h
1Ah	16	EPWM_DBCTL2	5001 501Ah	5005 501Ah	5009 501Ah
20h	16	EPWM_AQCTL	5001 5020h	5005 5020h	5009 5020h
22h	16	EPWM_AQTSRCSEL	5001 5022h	5005 5022h	5009 5022h
28h	16	EPWM_PCCTL	5001 5028h	5005 5028h	5009 5028h
30h	16	EPWM_VCAPCTL	5001 5030h	5005 5030h	5009 5030h
32h	16	EPWM_VCNTCFG	5001 5032h	5005 5032h	5009 5032h
40h	16	EPWM_HRCNFG	5001 5040h	5005 5040h	5009 5040h
4Eh	16	EPWM_HRCNFG2	5001 504Eh	5005 504Eh	5009 504Eh
5Ah	16	EPWM_HRPCTL	5001 505Ah	5005 505Ah	5009 505Ah
5Ch	16	EPWM_TRREM	5001 505Ch	5005 505Ch	5009 505Ch
68h	16	EPWM_GLDCTL	5001 5068h	5005 5068h	5009 5068h
6Ah	16	EPWM_GLDCFG	5001 506Ah	5005 506Ah	5009 506Ah
70h	32	EPWM_EPWMXLINK	5001 5070h	5005 5070h	5009 5070h
74h	32	EPWM_EPWMXLINK2	5001 5074h	5005 5074h	5009 5074h
7Ah	16	EPWM_ETEST	5001 507Ah	5005 507Ah	5009 507Ah
7Ch	16	EPWM_EPWMREV	5001 507Ch	5005 507Ch	5009 507Ch
7Eh	16	EPWM_HRPWMREV	5001 507Eh	5005 507Eh	5009 507Eh
80h	16	EPWM_AQCTLA	5001 5080h	5005 5080h	5009 5080h
82h	16	EPWM_AQCTLA2	5001 5082h	5005 5082h	5009 5082h
84h	16	EPWM_AQCTLB	5001 5084h	5005 5084h	5009 5084h
86h	16	EPWM_AQCTLB2	5001 5086h	5005 5086h	5009 5086h
8Eh	16	EPWM_AQSFRC	5001 508Eh	5005 508Eh	5009 508Eh
92h	16	EPWM_AQCSFRC	5001 5092h	5005 5092h	5009 5092h
A0h	16	EPWM_DBREDHR	5001 50A0h	5005 50A0h	5009 50A0h
A2h	16	EPWM_DBRED	5001 50A2h	5005 50A2h	5009 50A2h
A4h	16	EPWM_DBFEDHR	5001 50A4h	5005 50A4h	5009 50A4h
A6h	16	EPWM_DBFED	5001 50A6h	5005 50A6h	5009 50A6h
C0h	32	EPWM_TBPHS	5001 50C0h	5005 50C0h	5009 50C0h
C4h	16	EPWM_TBPRDHR	5001 50C4h	5005 50C4h	5009 50C4h
C6h	16	EPWM_TBPRD	5001 50C6h	5005 50C6h	5009 50C6h
C8h	16	EPWM_TBPRDHRB	5001 50C8h	5005 50C8h	5009 50C8h

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Table 3-598. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM20_G2 Physical Address	EPWM21_G2 Physical Address	EPWM22_G2 Physical Address
D4h	32	EPWM_CMPA	5001 50D4h	5005 50D4h	5009 50D4h
D8h	32	EPWM_CMPB	5001 50D8h	5005 50D8h	5009 50D8h
DEh	16	EPWM_CMPC	5001 50DEh	5005 50DEh	5009 50DEh
E2h	16	EPWM_CMPD	5001 50E2h	5005 50E2h	5009 50E2h
E8h	16	EPWM_GLDCTL2	5001 50E8h	5005 50E8h	5009 50E8h
EEh	16	EPWM_SWVDELVAL	5001 50EEh	5005 50EEh	5009 50EEh
100h	16	EPWM_TZSEL	5001 5100h	5005 5100h	5009 5100h
102h	16	EPWM_TZSEL2	5001 5102h	5005 5102h	5009 5102h
104h	16	EPWM_TZDCSEL	5001 5104h	5005 5104h	5009 5104h
108h	16	EPWM_TZCTL	5001 5108h	5005 5108h	5009 5108h
10Ah	16	EPWM_TZCTL2	5001 510Ah	5005 510Ah	5009 510Ah
10Ch	16	EPWM_TZCTLDCA	5001 510Ch	5005 510Ch	5009 510Ch
10Eh	16	EPWM_TZCTLDCB	5001 510Eh	5005 510Eh	5009 510Eh
11Ah	16	EPWM_TZEINT	5001 511Ah	5005 511Ah	5009 511Ah
126h	16	EPWM_TZFLG	5001 5126h	5005 5126h	5009 5126h
128h	16	EPWM_TZCBCFLG	5001 5128h	5005 5128h	5009 5128h
12Ah	16	EPWM_TZOSTFLG	5001 512Ah	5005 512Ah	5009 512Ah
12Eh	16	EPWM_TZCLR	5001 512Eh	5005 512Eh	5009 512Eh
130h	16	EPWM_TZCBCCLR	5001 5130h	5005 5130h	5009 5130h
132h	16	EPWM_TZOSTCLR	5001 5132h	5005 5132h	5009 5132h
136h	16	EPWM_TZFRC	5001 5136h	5005 5136h	5009 5136h
13Ah	16	EPWM_TZTRIPOUTSEL	5001 513Ah	5005 513Ah	5009 513Ah
148h	16	EPWM_ETSEL	5001 5148h	5005 5148h	5009 5148h
14Ch	16	EPWM_ETPS	5001 514Ch	5005 514Ch	5009 514Ch
150h	16	EPWM_ETFLG	5001 5150h	5005 5150h	5009 5150h
154h	16	EPWM_ETCLR	5001 5154h	5005 5154h	5009 5154h
158h	16	EPWM_ETFRC	5001 5158h	5005 5158h	5009 5158h
15Ch	16	EPWM_ETINTPS	5001 515Ch	5005 515Ch	5009 515Ch
160h	16	EPWM_ETSOCPS	5001 5160h	5005 5160h	5009 5160h
164h	16	EPWM_ETCNTINITCTL	5001 5164h	5005 5164h	5009 5164h
168h	16	EPWM_ETCNTINIT	5001 5168h	5005 5168h	5009 5168h
16Ch	16	EPWM_ETINTMIXEN	5001 516Ch	5005 516Ch	5009 516Ch
170h	16	EPWM_ETSOCAMIXEN	5001 5170h	5005 5170h	5009 5170h
174h	16	EPWM_ETSOCBMIXEN	5001 5174h	5005 5174h	5009 5174h
180h	16	EPWM_DCTRIPSEL	5001 5180h	5005 5180h	5009 5180h
186h	16	EPWM_DCACTL	5001 5186h	5005 5186h	5009 5186h
188h	16	EPWM_DCBCTL	5001 5188h	5005 5188h	5009 5188h
18Eh	16	EPWM_DCFCTL	5001 518Eh	5005 518Eh	5009 518Eh
190h	16	EPWM_DCCAPCTL	5001 5190h	5005 5190h	5009 5190h
192h	16	EPWM_DCFOFFSET	5001 5192h	5005 5192h	5009 5192h
194h	16	EPWM_DCFOFFSETCNT	5001 5194h	5005 5194h	5009 5194h
196h	16	EPWM_DCFWINDOW	5001 5196h	5005 5196h	5009 5196h
198h	16	EPWM_DCFWINDOWCNT	5001 5198h	5005 5198h	5009 5198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5001 519Ah	5005 519Ah	5009 519Ah
19Ch	16	EPWM_DCCAPMIXSEL	5001 519Ch	5005 519Ch	5009 519Ch
19Eh	16	EPWM_DCCAP	5001 519Eh	5005 519Eh	5009 519Eh

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Table 3-598. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM20_G2 Physical Address	EPWM21_G2 Physical Address	EPWM22_G2 Physical Address
1A4h	16	EPWM_DCAHTRIPSEL	5001 51A4h	5005 51A4h	5009 51A4h
1A6h	16	EPWM_DCALTRIPSEL	5001 51A6h	5005 51A6h	5009 51A6h
1A8h	16	EPWM_DCBHTRIPSEL	5001 51A8h	5005 51A8h	5009 51A8h
1AAh	16	EPWM_DCBLTRIPSEL	5001 51AAh	5005 51AAh	5009 51AAh
1ACh	16	EPWM_CAPCTL	5001 51ACh	5005 51ACh	5009 51ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5001 51AEh	5005 51AEh	5009 51AEh
1B0h	16	EPWM_CAPINTRIPSEL	5001 51B0h	5005 51B0h	5009 51B0h
1B2h	16	EPWM_CAPTRIPSEL	5001 51B2h	5005 51B2h	5009 51B2h
1F4h	32	EPWM_EPWMLOCK	5001 51F4h	5005 51F4h	5009 51F4h
1FAh	16	EPWM_HWVDELVAL	5001 51FAh	5005 51FAh	5009 51FAh
1FCh	16	EPWM_VCNTVAL	5001 51FCh	5005 51FCh	5009 51FCh
400h	32	EPWM_XCMPCTL1	5001 5400h	5005 5400h	5009 5400h
410h	32	EPWM_XLOADCTL	5001 5410h	5005 5410h	5009 5410h
418h	32	EPWM_XLOAD	5001 5418h	5005 5418h	5009 5418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5001 541Ch	5005 541Ch	5009 541Ch
420h	32	EPWM_XREGSHDW1STS	5001 5420h	5005 5420h	5009 5420h
428h	32	EPWM_XREGSHDW2STS	5001 5428h	5005 5428h	5009 5428h
430h	32	EPWM_XREGSHDW3STS	5001 5430h	5005 5430h	5009 5430h
600h	32	EPWM_XCMP1_ACTIVE	5001 5600h	5005 5600h	5009 5600h
604h	32	EPWM_XCMP2_ACTIVE	5001 5604h	5005 5604h	5009 5604h
608h	32	EPWM_XCMP3_ACTIVE	5001 5608h	5005 5608h	5009 5608h
60Ch	32	EPWM_XCMP4_ACTIVE	5001 560Ch	5005 560Ch	5009 560Ch
610h	32	EPWM_XCMP5_ACTIVE	5001 5610h	5005 5610h	5009 5610h
614h	32	EPWM_XCMP6_ACTIVE	5001 5614h	5005 5614h	5009 5614h
618h	32	EPWM_XCMP7_ACTIVE	5001 5618h	5005 5618h	5009 5618h
61Ch	32	EPWM_XCMP8_ACTIVE	5001 561Ch	5005 561Ch	5009 561Ch
620h	32	EPWM_XTBPRD_ACTIVE	5001 5620h	5005 5620h	5009 5620h
630h	16	EPWM_XAQCTLA_ACTIVE	5001 5630h	5005 5630h	5009 5630h
644h	32	EPWM_XMINMAX_ACTIVE	5001 5644h	5005 5644h	5009 5644h
680h	32	EPWM_XCMP1_SHDW1	5001 5680h	5005 5680h	5009 5680h
684h	32	EPWM_XCMP2_SHDW1	5001 5684h	5005 5684h	5009 5684h
688h	32	EPWM_XCMP3_SHDW1	5001 5688h	5005 5688h	5009 5688h
68Ch	32	EPWM_XCMP4_SHDW1	5001 568Ch	5005 568Ch	5009 568Ch
690h	32	EPWM_XCMP5_SHDW1	5001 5690h	5005 5690h	5009 5690h
694h	32	EPWM_XCMP6_SHDW1	5001 5694h	5005 5694h	5009 5694h
698h	32	EPWM_XCMP7_SHDW1	5001 5698h	5005 5698h	5009 5698h
69Ch	32	EPWM_XCMP8_SHDW1	5001 569Ch	5005 569Ch	5009 569Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5001 56A0h	5005 56A0h	5009 56A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5001 56B0h	5005 56B0h	5009 56B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5001 56B2h	5005 56B2h	5009 56B2h
6BAh	16	EPWM_CMPC_SHDW1	5001 56BAh	5005 56BAh	5009 56BAh
6BEh	16	EPWM_CMPD_SHDW1	5001 56BEh	5005 56BEh	5009 56BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5001 56C4h	5005 56C4h	5009 56C4h
700h	32	EPWM_XCMP1_SHDW2	5001 5700h	5005 5700h	5009 5700h
704h	32	EPWM_XCMP2_SHDW2	5001 5704h	5005 5704h	5009 5704h
708h	32	EPWM_XCMP3_SHDW2	5001 5708h	5005 5708h	5009 5708h

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Table 3-598. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM20_G2 Physical Address	EPWM21_G2 Physical Address	EPWM22_G2 Physical Address
70Ch	32	EPWM_XCMP4_SHDW2	5001 570Ch	5005 570Ch	5009 570Ch
710h	32	EPWM_XCMP5_SHDW2	5001 5710h	5005 5710h	5009 5710h
714h	32	EPWM_XCMP6_SHDW2	5001 5714h	5005 5714h	5009 5714h
718h	32	EPWM_XCMP7_SHDW2	5001 5718h	5005 5718h	5009 5718h
71Ch	32	EPWM_XCMP8_SHDW2	5001 571Ch	5005 571Ch	5009 571Ch
720h	32	EPWM_XTBPRD_SHDW2	5001 5720h	5005 5720h	5009 5720h
730h	16	EPWM_XAQCTLA_SHDW2	5001 5730h	5005 5730h	5009 5730h
732h	16	EPWM_XAQCTLB_SHDW2	5001 5732h	5005 5732h	5009 5732h
73Ah	16	EPWM_CMPC_SHDW2	5001 573Ah	5005 573Ah	5009 573Ah
73Eh	16	EPWM_CMPD_SHDW2	5001 573Eh	5005 573Eh	5009 573Eh
744h	32	EPWM_XMINMAX_SHDW2	5001 5744h	5005 5744h	5009 5744h
780h	32	EPWM_XCMP1_SHDW3	5001 5780h	5005 5780h	5009 5780h
784h	32	EPWM_XCMP2_SHDW3	5001 5784h	5005 5784h	5009 5784h
788h	32	EPWM_XCMP3_SHDW3	5001 5788h	5005 5788h	5009 5788h
78Ch	32	EPWM_XCMP4_SHDW3	5001 578Ch	5005 578Ch	5009 578Ch
790h	32	EPWM_XCMP5_SHDW3	5001 5790h	5005 5790h	5009 5790h
794h	32	EPWM_XCMP6_SHDW3	5001 5794h	5005 5794h	5009 5794h
798h	32	EPWM_XCMP7_SHDW3	5001 5798h	5005 5798h	5009 5798h
79Ch	32	EPWM_XCMP8_SHDW3	5001 579Ch	5005 579Ch	5009 579Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5001 57A0h	5005 57A0h	5009 57A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5001 57B0h	5005 57B0h	5009 57B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5001 57B2h	5005 57B2h	5009 57B2h
7BAh	16	EPWM_CMPC_SHDW3	5001 57BAh	5005 57BAh	5009 57BAh
7BEh	16	EPWM_CMPD_SHDW3	5001 57BEh	5005 57BEh	5009 57BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5001 57C4h	5005 57C4h	5009 57C4h
800h	32	EPWM_DECTL	5001 5800h	5005 5800h	5009 5800h
804h	32	EPWM_DECOMPSEL	5001 5804h	5005 5804h	5009 5804h
808h	32	EPWM_DEACTCTL	5001 5808h	5005 5808h	5009 5808h
80Ch	32	EPWM_DESTS	5001 580Ch	5005 580Ch	5009 580Ch
810h	32	EPWM_DEFRC	5001 5810h	5005 5810h	5009 5810h
814h	32	EPWM_DECLR	5001 5814h	5005 5814h	5009 5814h
820h	32	EPWM_DEMONCNT	5001 5820h	5005 5820h	5009 5820h
824h	32	EPWM_DEMONCTL	5001 5824h	5005 5824h	5009 5824h
828h	32	EPWM_DEMONSTEP	5001 5828h	5005 5828h	5009 5828h
82Ch	32	EPWM_DEMONTHRES	5001 582Ch	5005 582Ch	5009 582Ch
C00h	32	EPWM_MINDBCFG	5001 5C00h	5005 5C00h	5009 5C00h
C04h	32	EPWM_MINDBDLY	5001 5C04h	5005 5C04h	5009 5C04h
C20h	32	EPWM_LUTCTLA	5001 5C20h	5005 5C20h	5009 5C20h
C24h	32	EPWM_LUTCTLB	5001 5C24h	5005 5C24h	5009 5C24h

Table 3-599. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM23_G2 Physical Address	EPWM24_G2 Physical Address	EPWM25_G2 Physical Address
0h	16	EPWM_TBCTL	500D 5000h	5001 6000h	5005 6000h
2h	16	EPWM_TBCTL2	500D 5002h	5001 6002h	5005 6002h
6h	16	EPWM_EPWMSYNCINSEL	500D 5006h	5001 6006h	5005 6006h

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Table 3-599. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM23_G2 Physical Address	EPWM24_G2 Physical Address	EPWM25_G2 Physical Address
8h	16	EPWM_TBCTR	500D 5008h	5001 6008h	5005 6008h
Ah	16	EPWM_TBSTS	500D 500Ah	5001 600Ah	5005 600Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500D 500Ch	5001 600Ch	5005 600Ch
Eh	16	EPWM_TBCTL3	500D 500Eh	5001 600Eh	5005 600Eh
10h	16	EPWM_CMPCTL	500D 5010h	5001 6010h	5005 6010h
12h	16	EPWM_CMPCTL2	500D 5012h	5001 6012h	5005 6012h
18h	16	EPWM_DBCTL	500D 5018h	5001 6018h	5005 6018h
1Ah	16	EPWM_DBCTL2	500D 501Ah	5001 601Ah	5005 601Ah
20h	16	EPWM_AQCTL	500D 5020h	5001 6020h	5005 6020h
22h	16	EPWM_AQTSRCSEL	500D 5022h	5001 6022h	5005 6022h
28h	16	EPWM_PCCTL	500D 5028h	5001 6028h	5005 6028h
30h	16	EPWM_VCAPCTL	500D 5030h	5001 6030h	5005 6030h
32h	16	EPWM_VCNTCFG	500D 5032h	5001 6032h	5005 6032h
40h	16	EPWM_HRCNFG	500D 5040h	5001 6040h	5005 6040h
4Eh	16	EPWM_HRCNFG2	500D 504Eh	5001 604Eh	5005 604Eh
5Ah	16	EPWM_HRPCTL	500D 505Ah	5001 605Ah	5005 605Ah
5Ch	16	EPWM_TRREM	500D 505Ch	5001 605Ch	5005 605Ch
68h	16	EPWM_GLDCTL	500D 5068h	5001 6068h	5005 6068h
6Ah	16	EPWM_GLDCFG	500D 506Ah	5001 606Ah	5005 606Ah
70h	32	EPWM_EPWMXLINK	500D 5070h	5001 6070h	5005 6070h
74h	32	EPWM_EPWMXLINK2	500D 5074h	5001 6074h	5005 6074h
7Ah	16	EPWM_ETEST	500D 507Ah	5001 607Ah	5005 607Ah
7Ch	16	EPWM_EPWMREV	500D 507Ch	5001 607Ch	5005 607Ch
7Eh	16	EPWM_HRPWMREV	500D 507Eh	5001 607Eh	5005 607Eh
80h	16	EPWM_AQCTLA	500D 5080h	5001 6080h	5005 6080h
82h	16	EPWM_AQCTLA2	500D 5082h	5001 6082h	5005 6082h
84h	16	EPWM_AQCTLB	500D 5084h	5001 6084h	5005 6084h
86h	16	EPWM_AQCTLB2	500D 5086h	5001 6086h	5005 6086h
8Eh	16	EPWM_AQSFRC	500D 508Eh	5001 608Eh	5005 608Eh
92h	16	EPWM_AQCSFRC	500D 5092h	5001 6092h	5005 6092h
A0h	16	EPWM_DBREDHR	500D 50A0h	5001 60A0h	5005 60A0h
A2h	16	EPWM_DBRED	500D 50A2h	5001 60A2h	5005 60A2h
A4h	16	EPWM_DBFEDHR	500D 50A4h	5001 60A4h	5005 60A4h
A6h	16	EPWM_DBFED	500D 50A6h	5001 60A6h	5005 60A6h
C0h	32	EPWM_TBPHS	500D 50C0h	5001 60C0h	5005 60C0h
C4h	16	EPWM_TBPRDHR	500D 50C4h	5001 60C4h	5005 60C4h
C6h	16	EPWM_TBPRD	500D 50C6h	5001 60C6h	5005 60C6h
C8h	16	EPWM_TBPRDHRB	500D 50C8h	5001 60C8h	5005 60C8h
D4h	32	EPWM_CMPA	500D 50D4h	5001 60D4h	5005 60D4h
D8h	32	EPWM_CMPB	500D 50D8h	5001 60D8h	5005 60D8h
DEh	16	EPWM_CMPC	500D 50DEh	5001 60DEh	5005 60DEh
E2h	16	EPWM_CMPD	500D 50E2h	5001 60E2h	5005 60E2h
E8h	16	EPWM_GLDCTL2	500D 50E8h	5001 60E8h	5005 60E8h
EEh	16	EPWM_SWVDELVAL	500D 50EEh	5001 60EEh	5005 60EEh
100h	16	EPWM_TZSEL	500D 5100h	5001 6100h	5005 6100h
102h	16	EPWM_TZSEL2	500D 5102h	5001 6102h	5005 6102h

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Table 3-599. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM23_G2 Physical Address	EPWM24_G2 Physical Address	EPWM25_G2 Physical Address
104h	16	EPWM_TZDCSEL	500D 5104h	5001 6104h	5005 6104h
108h	16	EPWM_TZCTL	500D 5108h	5001 6108h	5005 6108h
10Ah	16	EPWM_TZCTL2	500D 510Ah	5001 610Ah	5005 610Ah
10Ch	16	EPWM_TZCTLDCA	500D 510Ch	5001 610Ch	5005 610Ch
10Eh	16	EPWM_TZCTLDCB	500D 510Eh	5001 610Eh	5005 610Eh
11Ah	16	EPWM_TZEINT	500D 511Ah	5001 611Ah	5005 611Ah
126h	16	EPWM_TZFLG	500D 5126h	5001 6126h	5005 6126h
128h	16	EPWM_TZCBCFLG	500D 5128h	5001 6128h	5005 6128h
12Ah	16	EPWM_TZOSTFLG	500D 512Ah	5001 612Ah	5005 612Ah
12Eh	16	EPWM_TZCLR	500D 512Eh	5001 612Eh	5005 612Eh
130h	16	EPWM_TZCBCCLR	500D 5130h	5001 6130h	5005 6130h
132h	16	EPWM_TZOSTCLR	500D 5132h	5001 6132h	5005 6132h
136h	16	EPWM_TZFRC	500D 5136h	5001 6136h	5005 6136h
13Ah	16	EPWM_TZTRIPOUTSEL	500D 513Ah	5001 613Ah	5005 613Ah
148h	16	EPWM_ETSEL	500D 5148h	5001 6148h	5005 6148h
14Ch	16	EPWM_ETPS	500D 514Ch	5001 614Ch	5005 614Ch
150h	16	EPWM_ETFLG	500D 5150h	5001 6150h	5005 6150h
154h	16	EPWM_ETCLR	500D 5154h	5001 6154h	5005 6154h
158h	16	EPWM_ETFRC	500D 5158h	5001 6158h	5005 6158h
15Ch	16	EPWM_ETINTPS	500D 515Ch	5001 615Ch	5005 615Ch
160h	16	EPWM_ETSOCPS	500D 5160h	5001 6160h	5005 6160h
164h	16	EPWM_ETCNTINITCTL	500D 5164h	5001 6164h	5005 6164h
168h	16	EPWM_ETCNTINIT	500D 5168h	5001 6168h	5005 6168h
16Ch	16	EPWM_ETINTMIXEN	500D 516Ch	5001 616Ch	5005 616Ch
170h	16	EPWM_ETSOCAMIXEN	500D 5170h	5001 6170h	5005 6170h
174h	16	EPWM_ETSOCBMIXEN	500D 5174h	5001 6174h	5005 6174h
180h	16	EPWM_DCTRIPSEL	500D 5180h	5001 6180h	5005 6180h
186h	16	EPWM_DCACTL	500D 5186h	5001 6186h	5005 6186h
188h	16	EPWM_DCBCTL	500D 5188h	5001 6188h	5005 6188h
18Eh	16	EPWM_DCFCTL	500D 518Eh	5001 618Eh	5005 618Eh
190h	16	EPWM_DCCAPCTL	500D 5190h	5001 6190h	5005 6190h
192h	16	EPWM_DCFOFFSET	500D 5192h	5001 6192h	5005 6192h
194h	16	EPWM_DCFOFFSETCNT	500D 5194h	5001 6194h	5005 6194h
196h	16	EPWM_DCFWINDOW	500D 5196h	5001 6196h	5005 6196h
198h	16	EPWM_DCFWINDOWCNT	500D 5198h	5001 6198h	5005 6198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500D 519Ah	5001 619Ah	5005 619Ah
19Ch	16	EPWM_DCCAPMIXSEL	500D 519Ch	5001 619Ch	5005 619Ch
19Eh	16	EPWM_DCCAP	500D 519Eh	5001 619Eh	5005 619Eh
1A4h	16	EPWM_DCAHTRIPSEL	500D 51A4h	5001 61A4h	5005 61A4h
1A6h	16	EPWM_DCALTRIPSEL	500D 51A6h	5001 61A6h	5005 61A6h
1A8h	16	EPWM_DCBHTRIPSEL	500D 51A8h	5001 61A8h	5005 61A8h
1AAh	16	EPWM_DCBLTRIPSEL	500D 51AAh	5001 61AAh	5005 61AAh
1ACh	16	EPWM_CAPCTL	500D 51ACh	5001 61ACh	5005 61ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500D 51AEh	5001 61AEh	5005 61AEh
1B0h	16	EPWM_CAPINTRIPSEL	500D 51B0h	5001 61B0h	5005 61B0h
1B2h	16	EPWM_CAPTRIPSEL	500D 51B2h	5001 61B2h	5005 61B2h

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Table 3-599. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM23_G2 Physical Address	EPWM24_G2 Physical Address	EPWM25_G2 Physical Address
1F4h	32	EPWM_EPWMLOCK	500D 51F4h	5001 61F4h	5005 61F4h
1FAh	16	EPWM_HWVDELVAL	500D 51FAh	5001 61FAh	5005 61FAh
1FCh	16	EPWM_VCNTVAL	500D 51FCh	5001 61FCh	5005 61FCh
400h	32	EPWM_XCMPCTL1	500D 5400h	5001 6400h	5005 6400h
410h	32	EPWM_XLOADCTL	500D 5410h	5001 6410h	5005 6410h
418h	32	EPWM_XLOAD	500D 5418h	5001 6418h	5005 6418h
41Ch	32	EPWM_EPWMXLINKXLOAD	500D 541Ch	5001 641Ch	5005 641Ch
420h	32	EPWM_XREGSHDW1STS	500D 5420h	5001 6420h	5005 6420h
428h	32	EPWM_XREGSHDW2STS	500D 5428h	5001 6428h	5005 6428h
430h	32	EPWM_XREGSHDW3STS	500D 5430h	5001 6430h	5005 6430h
600h	32	EPWM_XCMP1_ACTIVE	500D 5600h	5001 6600h	5005 6600h
604h	32	EPWM_XCMP2_ACTIVE	500D 5604h	5001 6604h	5005 6604h
608h	32	EPWM_XCMP3_ACTIVE	500D 5608h	5001 6608h	5005 6608h
60Ch	32	EPWM_XCMP4_ACTIVE	500D 560Ch	5001 660Ch	5005 660Ch
610h	32	EPWM_XCMP5_ACTIVE	500D 5610h	5001 6610h	5005 6610h
614h	32	EPWM_XCMP6_ACTIVE	500D 5614h	5001 6614h	5005 6614h
618h	32	EPWM_XCMP7_ACTIVE	500D 5618h	5001 6618h	5005 6618h
61Ch	32	EPWM_XCMP8_ACTIVE	500D 561Ch	5001 661Ch	5005 661Ch
620h	32	EPWM_XTBPRD_ACTIVE	500D 5620h	5001 6620h	5005 6620h
630h	16	EPWM_XAQCTLA_ACTIVE	500D 5630h	5001 6630h	5005 6630h
644h	32	EPWM_XMINMAX_ACTIVE	500D 5644h	5001 6644h	5005 6644h
680h	32	EPWM_XCMP1_SHDW1	500D 5680h	5001 6680h	5005 6680h
684h	32	EPWM_XCMP2_SHDW1	500D 5684h	5001 6684h	5005 6684h
688h	32	EPWM_XCMP3_SHDW1	500D 5688h	5001 6688h	5005 6688h
68Ch	32	EPWM_XCMP4_SHDW1	500D 568Ch	5001 668Ch	5005 668Ch
690h	32	EPWM_XCMP5_SHDW1	500D 5690h	5001 6690h	5005 6690h
694h	32	EPWM_XCMP6_SHDW1	500D 5694h	5001 6694h	5005 6694h
698h	32	EPWM_XCMP7_SHDW1	500D 5698h	5001 6698h	5005 6698h
69Ch	32	EPWM_XCMP8_SHDW1	500D 569Ch	5001 669Ch	5005 669Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500D 56A0h	5001 66A0h	5005 66A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500D 56B0h	5001 66B0h	5005 66B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500D 56B2h	5001 66B2h	5005 66B2h
6BAh	16	EPWM_CMPC_SHDW1	500D 56BAh	5001 66BAh	5005 66BAh
6BEh	16	EPWM_CMPD_SHDW1	500D 56BEh	5001 66BEh	5005 66BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500D 56C4h	5001 66C4h	5005 66C4h
700h	32	EPWM_XCMP1_SHDW2	500D 5700h	5001 6700h	5005 6700h
704h	32	EPWM_XCMP2_SHDW2	500D 5704h	5001 6704h	5005 6704h
708h	32	EPWM_XCMP3_SHDW2	500D 5708h	5001 6708h	5005 6708h
70Ch	32	EPWM_XCMP4_SHDW2	500D 570Ch	5001 670Ch	5005 670Ch
710h	32	EPWM_XCMP5_SHDW2	500D 5710h	5001 6710h	5005 6710h
714h	32	EPWM_XCMP6_SHDW2	500D 5714h	5001 6714h	5005 6714h
718h	32	EPWM_XCMP7_SHDW2	500D 5718h	5001 6718h	5005 6718h
71Ch	32	EPWM_XCMP8_SHDW2	500D 571Ch	5001 671Ch	5005 671Ch
720h	32	EPWM_XTBPRD_SHDW2	500D 5720h	5001 6720h	5005 6720h
730h	16	EPWM_XAQCTLA_SHDW2	500D 5730h	5001 6730h	5005 6730h
732h	16	EPWM_XAQCTLB_SHDW2	500D 5732h	5001 6732h	5005 6732h

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Table 3-599. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM23_G2 Physical Address	EPWM24_G2 Physical Address	EPWM25_G2 Physical Address
73Ah	16	EPWM_CMPC_SHDW2	500D 573Ah	5001 673Ah	5005 673Ah
73Eh	16	EPWM_CMPD_SHDW2	500D 573Eh	5001 673Eh	5005 673Eh
744h	32	EPWM_XMINMAX_SHDW2	500D 5744h	5001 6744h	5005 6744h
780h	32	EPWM_XCMP1_SHDW3	500D 5780h	5001 6780h	5005 6780h
784h	32	EPWM_XCMP2_SHDW3	500D 5784h	5001 6784h	5005 6784h
788h	32	EPWM_XCMP3_SHDW3	500D 5788h	5001 6788h	5005 6788h
78Ch	32	EPWM_XCMP4_SHDW3	500D 578Ch	5001 678Ch	5005 678Ch
790h	32	EPWM_XCMP5_SHDW3	500D 5790h	5001 6790h	5005 6790h
794h	32	EPWM_XCMP6_SHDW3	500D 5794h	5001 6794h	5005 6794h
798h	32	EPWM_XCMP7_SHDW3	500D 5798h	5001 6798h	5005 6798h
79Ch	32	EPWM_XCMP8_SHDW3	500D 579Ch	5001 679Ch	5005 679Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500D 57A0h	5001 67A0h	5005 67A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500D 57B0h	5001 67B0h	5005 67B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500D 57B2h	5001 67B2h	5005 67B2h
7BAh	16	EPWM_CMPC_SHDW3	500D 57BAh	5001 67BAh	5005 67BAh
7BEh	16	EPWM_CMPD_SHDW3	500D 57BEh	5001 67BEh	5005 67BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500D 57C4h	5001 67C4h	5005 67C4h
800h	32	EPWM_DECTL	500D 5800h	5001 6800h	5005 6800h
804h	32	EPWM_DECOMPSEL	500D 5804h	5001 6804h	5005 6804h
808h	32	EPWM_DEACTCTL	500D 5808h	5001 6808h	5005 6808h
80Ch	32	EPWM_DESTS	500D 580Ch	5001 680Ch	5005 680Ch
810h	32	EPWM_DEFRC	500D 5810h	5001 6810h	5005 6810h
814h	32	EPWM_DECLR	500D 5814h	5001 6814h	5005 6814h
820h	32	EPWM_DEMONCNT	500D 5820h	5001 6820h	5005 6820h
824h	32	EPWM_DEMONCTL	500D 5824h	5001 6824h	5005 6824h
828h	32	EPWM_DEMONSTEP	500D 5828h	5001 6828h	5005 6828h
82Ch	32	EPWM_DEMONTHRES	500D 582Ch	5001 682Ch	5005 682Ch
C00h	32	EPWM_MINDBCFG	500D 5C00h	5001 6C00h	5005 6C00h
C04h	32	EPWM_MINDBDLY	500D 5C04h	5001 6C04h	5005 6C04h
C20h	32	EPWM_LUTCTLA	500D 5C20h	5001 6C20h	5005 6C20h
C24h	32	EPWM_LUTCTLB	500D 5C24h	5001 6C24h	5005 6C24h

Table 3-600. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM26_G2 Physical Address	EPWM27_G2 Physical Address	EPWM28_G2 Physical Address
0h	16	EPWM_TBCTL	5009 6000h	500D 6000h	5001 7000h
2h	16	EPWM_TBCTL2	5009 6002h	500D 6002h	5001 7002h
6h	16	EPWM_EPWMSYNCINSEL	5009 6006h	500D 6006h	5001 7006h
8h	16	EPWM_TBCTR	5009 6008h	500D 6008h	5001 7008h
Ah	16	EPWM_TBSTS	5009 600Ah	500D 600Ah	5001 700Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5009 600Ch	500D 600Ch	5001 700Ch
Eh	16	EPWM_TBCTL3	5009 600Eh	500D 600Eh	5001 700Eh
10h	16	EPWM_CMPCTL	5009 6010h	500D 6010h	5001 7010h
12h	16	EPWM_CMPCTL2	5009 6012h	500D 6012h	5001 7012h
18h	16	EPWM_DBCTL	5009 6018h	500D 6018h	5001 7018h
1Ah	16	EPWM_DBCTL2	5009 601Ah	500D 601Ah	5001 701Ah

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Table 3-600. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM26_G2 Physical Address	EPWM27_G2 Physical Address	EPWM28_G2 Physical Address
20h	16	EPWM_AQCTL	5009 6020h	500D 6020h	5001 7020h
22h	16	EPWM_AQTSRCSEL	5009 6022h	500D 6022h	5001 7022h
28h	16	EPWM_PCCTL	5009 6028h	500D 6028h	5001 7028h
30h	16	EPWM_VCAPCTL	5009 6030h	500D 6030h	5001 7030h
32h	16	EPWM_VCNTCFG	5009 6032h	500D 6032h	5001 7032h
40h	16	EPWM_HRCNFG	5009 6040h	500D 6040h	5001 7040h
4Eh	16	EPWM_HRCNFG2	5009 604Eh	500D 604Eh	5001 704Eh
5Ah	16	EPWM_HRPCTL	5009 605Ah	500D 605Ah	5001 705Ah
5Ch	16	EPWM_TRREM	5009 605Ch	500D 605Ch	5001 705Ch
68h	16	EPWM_GLDCTL	5009 6068h	500D 6068h	5001 7068h
6Ah	16	EPWM_GLDCFG	5009 606Ah	500D 606Ah	5001 706Ah
70h	32	EPWM_EPWMXLINK	5009 6070h	500D 6070h	5001 7070h
74h	32	EPWM_EPWMXLINK2	5009 6074h	500D 6074h	5001 7074h
7Ah	16	EPWM_ETEST	5009 607Ah	500D 607Ah	5001 707Ah
7Ch	16	EPWM_EPWMREV	5009 607Ch	500D 607Ch	5001 707Ch
7Eh	16	EPWM_HRPWMREV	5009 607Eh	500D 607Eh	5001 707Eh
80h	16	EPWM_AQCTLA	5009 6080h	500D 6080h	5001 7080h
82h	16	EPWM_AQCTLA2	5009 6082h	500D 6082h	5001 7082h
84h	16	EPWM_AQCTLB	5009 6084h	500D 6084h	5001 7084h
86h	16	EPWM_AQCTLB2	5009 6086h	500D 6086h	5001 7086h
8Eh	16	EPWM_AQSFRC	5009 608Eh	500D 608Eh	5001 708Eh
92h	16	EPWM_AQCSFRC	5009 6092h	500D 6092h	5001 7092h
A0h	16	EPWM_DBREDHR	5009 60A0h	500D 60A0h	5001 70A0h
A2h	16	EPWM_DBRED	5009 60A2h	500D 60A2h	5001 70A2h
A4h	16	EPWM_DBFEDHR	5009 60A4h	500D 60A4h	5001 70A4h
A6h	16	EPWM_DBFED	5009 60A6h	500D 60A6h	5001 70A6h
C0h	32	EPWM_TBPHS	5009 60C0h	500D 60C0h	5001 70C0h
C4h	16	EPWM_TBPRDHR	5009 60C4h	500D 60C4h	5001 70C4h
C6h	16	EPWM_TBPRD	5009 60C6h	500D 60C6h	5001 70C6h
C8h	16	EPWM_TBPRDHRB	5009 60C8h	500D 60C8h	5001 70C8h
D4h	32	EPWM_CMPA	5009 60D4h	500D 60D4h	5001 70D4h
D8h	32	EPWM_CMPB	5009 60D8h	500D 60D8h	5001 70D8h
DEh	16	EPWM_CMPC	5009 60DEh	500D 60DEh	5001 70DEh
E2h	16	EPWM_CMPD	5009 60E2h	500D 60E2h	5001 70E2h
E8h	16	EPWM_GLDCTL2	5009 60E8h	500D 60E8h	5001 70E8h
EEh	16	EPWM_SWVDELVAL	5009 60EEh	500D 60EEh	5001 70EEh
100h	16	EPWM_TZSEL	5009 6100h	500D 6100h	5001 7100h
102h	16	EPWM_TZSEL2	5009 6102h	500D 6102h	5001 7102h
104h	16	EPWM_TZDCSEL	5009 6104h	500D 6104h	5001 7104h
108h	16	EPWM_TZCTL	5009 6108h	500D 6108h	5001 7108h
10Ah	16	EPWM_TZCTL2	5009 610Ah	500D 610Ah	5001 710Ah
10Ch	16	EPWM_TZCTLDCA	5009 610Ch	500D 610Ch	5001 710Ch
10Eh	16	EPWM_TZCTLDCB	5009 610Eh	500D 610Eh	5001 710Eh
11Ah	16	EPWM_TZEINT	5009 611Ah	500D 611Ah	5001 711Ah
126h	16	EPWM_TZFLG	5009 6126h	500D 6126h	5001 7126h
128h	16	EPWM_TZCBCFLG	5009 6128h	500D 6128h	5001 7128h

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Table 3-600. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM26_G2 Physical Address	EPWM27_G2 Physical Address	EPWM28_G2 Physical Address
12Ah	16	EPWM_TZOSTFLG	5009 612Ah	500D 612Ah	5001 712Ah
12Eh	16	EPWM_TZCLR	5009 612Eh	500D 612Eh	5001 712Eh
130h	16	EPWM_TZCBCCLR	5009 6130h	500D 6130h	5001 7130h
132h	16	EPWM_TZOSTCLR	5009 6132h	500D 6132h	5001 7132h
136h	16	EPWM_TZFRC	5009 6136h	500D 6136h	5001 7136h
13Ah	16	EPWM_TZTRIPOUTSEL	5009 613Ah	500D 613Ah	5001 713Ah
148h	16	EPWM_ETSEL	5009 6148h	500D 6148h	5001 7148h
14Ch	16	EPWM_ETPS	5009 614Ch	500D 614Ch	5001 714Ch
150h	16	EPWM_ETFLG	5009 6150h	500D 6150h	5001 7150h
154h	16	EPWM_ETCLR	5009 6154h	500D 6154h	5001 7154h
158h	16	EPWM_ETFRC	5009 6158h	500D 6158h	5001 7158h
15Ch	16	EPWM_ETINTPS	5009 615Ch	500D 615Ch	5001 715Ch
160h	16	EPWM_ETSOCPS	5009 6160h	500D 6160h	5001 7160h
164h	16	EPWM_ETCNTINITCTL	5009 6164h	500D 6164h	5001 7164h
168h	16	EPWM_ETCNTINIT	5009 6168h	500D 6168h	5001 7168h
16Ch	16	EPWM_ETINTMIXEN	5009 616Ch	500D 616Ch	5001 716Ch
170h	16	EPWM_ETSOCAMIXEN	5009 6170h	500D 6170h	5001 7170h
174h	16	EPWM_ETSOCBMIXEN	5009 6174h	500D 6174h	5001 7174h
180h	16	EPWM_DCTRIPSEL	5009 6180h	500D 6180h	5001 7180h
186h	16	EPWM_DCACTL	5009 6186h	500D 6186h	5001 7186h
188h	16	EPWM_DCBCTL	5009 6188h	500D 6188h	5001 7188h
18Eh	16	EPWM_DCFCTL	5009 618Eh	500D 618Eh	5001 718Eh
190h	16	EPWM_DCCAPCTL	5009 6190h	500D 6190h	5001 7190h
192h	16	EPWM_DCFOFFSET	5009 6192h	500D 6192h	5001 7192h
194h	16	EPWM_DCFOFFSETCNT	5009 6194h	500D 6194h	5001 7194h
196h	16	EPWM_DCFWINDOW	5009 6196h	500D 6196h	5001 7196h
198h	16	EPWM_DCFWINDOWCNT	5009 6198h	500D 6198h	5001 7198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5009 619Ah	500D 619Ah	5001 719Ah
19Ch	16	EPWM_DCCAPMIXSEL	5009 619Ch	500D 619Ch	5001 719Ch
19Eh	16	EPWM_DCCAP	5009 619Eh	500D 619Eh	5001 719Eh
1A4h	16	EPWM_DCAHTRIPSEL	5009 61A4h	500D 61A4h	5001 71A4h
1A6h	16	EPWM_DCALTRIPSEL	5009 61A6h	500D 61A6h	5001 71A6h
1A8h	16	EPWM_DCBHTRIPSEL	5009 61A8h	500D 61A8h	5001 71A8h
1AAh	16	EPWM_DCBLTRIPSEL	5009 61AAh	500D 61AAh	5001 71AAh
1ACh	16	EPWM_CAPCTL	5009 61ACh	500D 61ACh	5001 71ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5009 61AEh	500D 61AEh	5001 71AEh
1B0h	16	EPWM_CAPINTRIPSEL	5009 61B0h	500D 61B0h	5001 71B0h
1B2h	16	EPWM_CAPTRIPSEL	5009 61B2h	500D 61B2h	5001 71B2h
1F4h	32	EPWM_EPWMLOCK	5009 61F4h	500D 61F4h	5001 71F4h
1FAh	16	EPWM_HWVDELVAL	5009 61FAh	500D 61FAh	5001 71FAh
1FCh	16	EPWM_VCNTVAL	5009 61FCh	500D 61FCh	5001 71FCh
400h	32	EPWM_XCMPCTL1	5009 6400h	500D 6400h	5001 7400h
410h	32	EPWM_XLOADCTL	5009 6410h	500D 6410h	5001 7410h
418h	32	EPWM_XLOAD	5009 6418h	500D 6418h	5001 7418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5009 641Ch	500D 641Ch	5001 741Ch
420h	32	EPWM_XREGSHDW1STS	5009 6420h	500D 6420h	5001 7420h

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Table 3-600. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM26_G2 Physical Address	EPWM27_G2 Physical Address	EPWM28_G2 Physical Address
428h	32	EPWM_XREGSHDW2STS	5009 6428h	500D 6428h	5001 7428h
430h	32	EPWM_XREGSHDW3STS	5009 6430h	500D 6430h	5001 7430h
600h	32	EPWM_XCMP1_ACTIVE	5009 6600h	500D 6600h	5001 7600h
604h	32	EPWM_XCMP2_ACTIVE	5009 6604h	500D 6604h	5001 7604h
608h	32	EPWM_XCMP3_ACTIVE	5009 6608h	500D 6608h	5001 7608h
60Ch	32	EPWM_XCMP4_ACTIVE	5009 660Ch	500D 660Ch	5001 760Ch
610h	32	EPWM_XCMP5_ACTIVE	5009 6610h	500D 6610h	5001 7610h
614h	32	EPWM_XCMP6_ACTIVE	5009 6614h	500D 6614h	5001 7614h
618h	32	EPWM_XCMP7_ACTIVE	5009 6618h	500D 6618h	5001 7618h
61Ch	32	EPWM_XCMP8_ACTIVE	5009 661Ch	500D 661Ch	5001 761Ch
620h	32	EPWM_XTBPRD_ACTIVE	5009 6620h	500D 6620h	5001 7620h
630h	16	EPWM_XAQCTLA_ACTIVE	5009 6630h	500D 6630h	5001 7630h
644h	32	EPWM_XMINMAX_ACTIVE	5009 6644h	500D 6644h	5001 7644h
680h	32	EPWM_XCMP1_SHDW1	5009 6680h	500D 6680h	5001 7680h
684h	32	EPWM_XCMP2_SHDW1	5009 6684h	500D 6684h	5001 7684h
688h	32	EPWM_XCMP3_SHDW1	5009 6688h	500D 6688h	5001 7688h
68Ch	32	EPWM_XCMP4_SHDW1	5009 668Ch	500D 668Ch	5001 768Ch
690h	32	EPWM_XCMP5_SHDW1	5009 6690h	500D 6690h	5001 7690h
694h	32	EPWM_XCMP6_SHDW1	5009 6694h	500D 6694h	5001 7694h
698h	32	EPWM_XCMP7_SHDW1	5009 6698h	500D 6698h	5001 7698h
69Ch	32	EPWM_XCMP8_SHDW1	5009 669Ch	500D 669Ch	5001 769Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5009 66A0h	500D 66A0h	5001 76A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5009 66B0h	500D 66B0h	5001 76B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5009 66B2h	500D 66B2h	5001 76B2h
6BAh	16	EPWM_CMPC_SHDW1	5009 66BAh	500D 66BAh	5001 76BAh
6BEh	16	EPWM_CMPD_SHDW1	5009 66BEh	500D 66BEh	5001 76BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5009 66C4h	500D 66C4h	5001 76C4h
700h	32	EPWM_XCMP1_SHDW2	5009 6700h	500D 6700h	5001 7700h
704h	32	EPWM_XCMP2_SHDW2	5009 6704h	500D 6704h	5001 7704h
708h	32	EPWM_XCMP3_SHDW2	5009 6708h	500D 6708h	5001 7708h
70Ch	32	EPWM_XCMP4_SHDW2	5009 670Ch	500D 670Ch	5001 770Ch
710h	32	EPWM_XCMP5_SHDW2	5009 6710h	500D 6710h	5001 7710h
714h	32	EPWM_XCMP6_SHDW2	5009 6714h	500D 6714h	5001 7714h
718h	32	EPWM_XCMP7_SHDW2	5009 6718h	500D 6718h	5001 7718h
71Ch	32	EPWM_XCMP8_SHDW2	5009 671Ch	500D 671Ch	5001 771Ch
720h	32	EPWM_XTBPRD_SHDW2	5009 6720h	500D 6720h	5001 7720h
730h	16	EPWM_XAQCTLA_SHDW2	5009 6730h	500D 6730h	5001 7730h
732h	16	EPWM_XAQCTLB_SHDW2	5009 6732h	500D 6732h	5001 7732h
73Ah	16	EPWM_CMPC_SHDW2	5009 673Ah	500D 673Ah	5001 773Ah
73Eh	16	EPWM_CMPD_SHDW2	5009 673Eh	500D 673Eh	5001 773Eh
744h	32	EPWM_XMINMAX_SHDW2	5009 6744h	500D 6744h	5001 7744h
780h	32	EPWM_XCMP1_SHDW3	5009 6780h	500D 6780h	5001 7780h
784h	32	EPWM_XCMP2_SHDW3	5009 6784h	500D 6784h	5001 7784h
788h	32	EPWM_XCMP3_SHDW3	5009 6788h	500D 6788h	5001 7788h
78Ch	32	EPWM_XCMP4_SHDW3	5009 678Ch	500D 678Ch	5001 778Ch
790h	32	EPWM_XCMP5_SHDW3	5009 6790h	500D 6790h	5001 7790h

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Table 3-600. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM26_G2 Physical Address	EPWM27_G2 Physical Address	EPWM28_G2 Physical Address
794h	32	EPWM_XCMP6_SHDW3	5009 6794h	500D 6794h	5001 7794h
798h	32	EPWM_XCMP7_SHDW3	5009 6798h	500D 6798h	5001 7798h
79Ch	32	EPWM_XCMP8_SHDW3	5009 679Ch	500D 679Ch	5001 779Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5009 67A0h	500D 67A0h	5001 77A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5009 67B0h	500D 67B0h	5001 77B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5009 67B2h	500D 67B2h	5001 77B2h
7BAh	16	EPWM_CMPC_SHDW3	5009 67BAh	500D 67BAh	5001 77BAh
7BEh	16	EPWM_CMPD_SHDW3	5009 67BEh	500D 67BEh	5001 77BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5009 67C4h	500D 67C4h	5001 77C4h
800h	32	EPWM_DECTL	5009 6800h	500D 6800h	5001 7800h
804h	32	EPWM_DECOMPSEL	5009 6804h	500D 6804h	5001 7804h
808h	32	EPWM_DEACTCTL	5009 6808h	500D 6808h	5001 7808h
80Ch	32	EPWM_DESTS	5009 680Ch	500D 680Ch	5001 780Ch
810h	32	EPWM_DEFRC	5009 6810h	500D 6810h	5001 7810h
814h	32	EPWM_DECLR	5009 6814h	500D 6814h	5001 7814h
820h	32	EPWM_DEMONCNT	5009 6820h	500D 6820h	5001 7820h
824h	32	EPWM_DEMONCTL	5009 6824h	500D 6824h	5001 7824h
828h	32	EPWM_DEMONSTEP	5009 6828h	500D 6828h	5001 7828h
82Ch	32	EPWM_DEMONTHRES	5009 682Ch	500D 682Ch	5001 782Ch
C00h	32	EPWM_MINDBCFG	5009 6C00h	500D 6C00h	5001 7C00h
C04h	32	EPWM_MINDBDLY	5009 6C04h	500D 6C04h	5001 7C04h
C20h	32	EPWM_LUTCTLA	5009 6C20h	500D 6C20h	5001 7C20h
C24h	32	EPWM_LUTCTLB	5009 6C24h	500D 6C24h	5001 7C24h

Table 3-601. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM29_G2 Physical Address	EPWM30_G2 Physical Address	EPWM31_G2 Physical Address
0h	16	EPWM_TBCTL	5005 7000h	5009 7000h	500D 7000h
2h	16	EPWM_TBCTL2	5005 7002h	5009 7002h	500D 7002h
6h	16	EPWM_EPWMSYNCINSEL	5005 7006h	5009 7006h	500D 7006h
8h	16	EPWM_TBCTR	5005 7008h	5009 7008h	500D 7008h
Ah	16	EPWM_TBSTS	5005 700Ah	5009 700Ah	500D 700Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5005 700Ch	5009 700Ch	500D 700Ch
Eh	16	EPWM_TBCTL3	5005 700Eh	5009 700Eh	500D 700Eh
10h	16	EPWM_CMPCTL	5005 7010h	5009 7010h	500D 7010h
12h	16	EPWM_CMPCTL2	5005 7012h	5009 7012h	500D 7012h
18h	16	EPWM_DBCTL	5005 7018h	5009 7018h	500D 7018h
1Ah	16	EPWM_DBCTL2	5005 701Ah	5009 701Ah	500D 701Ah
20h	16	EPWM_AQCTL	5005 7020h	5009 7020h	500D 7020h
22h	16	EPWM_AQTSRCSEL	5005 7022h	5009 7022h	500D 7022h
28h	16	EPWM_PCCTL	5005 7028h	5009 7028h	500D 7028h
30h	16	EPWM_VCAPCTL	5005 7030h	5009 7030h	500D 7030h
32h	16	EPWM_VCNTCFG	5005 7032h	5009 7032h	500D 7032h
40h	16	EPWM_HRCNFG	5005 7040h	5009 7040h	500D 7040h
4Eh	16	EPWM_HRCNFG2	5005 704Eh	5009 704Eh	500D 704Eh
5Ah	16	EPWM_HRPCTL	5005 705Ah	5009 705Ah	500D 705Ah

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Table 3-601. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM29_G2 Physical Address	EPWM30_G2 Physical Address	EPWM31_G2 Physical Address
5Ch	16	EPWM_TRREM	5005 705Ch	5009 705Ch	500D 705Ch
68h	16	EPWM_GLDCTL	5005 7068h	5009 7068h	500D 7068h
6Ah	16	EPWM_GLDCFG	5005 706Ah	5009 706Ah	500D 706Ah
70h	32	EPWM_EPWMXLINK	5005 7070h	5009 7070h	500D 7070h
74h	32	EPWM_EPWMXLINK2	5005 7074h	5009 7074h	500D 7074h
7Ah	16	EPWM_ETEST	5005 707Ah	5009 707Ah	500D 707Ah
7Ch	16	EPWM_EPWMREV	5005 707Ch	5009 707Ch	500D 707Ch
7Eh	16	EPWM_HRPWMREV	5005 707Eh	5009 707Eh	500D 707Eh
80h	16	EPWM_AQCTLA	5005 7080h	5009 7080h	500D 7080h
82h	16	EPWM_AQCTLA2	5005 7082h	5009 7082h	500D 7082h
84h	16	EPWM_AQCTLB	5005 7084h	5009 7084h	500D 7084h
86h	16	EPWM_AQCTLB2	5005 7086h	5009 7086h	500D 7086h
8Eh	16	EPWM_AQSFRC	5005 708Eh	5009 708Eh	500D 708Eh
92h	16	EPWM_AQCSFRC	5005 7092h	5009 7092h	500D 7092h
A0h	16	EPWM_DBREDHR	5005 70A0h	5009 70A0h	500D 70A0h
A2h	16	EPWM_DBRED	5005 70A2h	5009 70A2h	500D 70A2h
A4h	16	EPWM_DBFEDHR	5005 70A4h	5009 70A4h	500D 70A4h
A6h	16	EPWM_DBFED	5005 70A6h	5009 70A6h	500D 70A6h
C0h	32	EPWM_TBPHS	5005 70C0h	5009 70C0h	500D 70C0h
C4h	16	EPWM_TBPRDHR	5005 70C4h	5009 70C4h	500D 70C4h
C6h	16	EPWM_TBPRD	5005 70C6h	5009 70C6h	500D 70C6h
C8h	16	EPWM_TBPRDHRB	5005 70C8h	5009 70C8h	500D 70C8h
D4h	32	EPWM_CMPA	5005 70D4h	5009 70D4h	500D 70D4h
D8h	32	EPWM_CMPB	5005 70D8h	5009 70D8h	500D 70D8h
DEh	16	EPWM_CMPC	5005 70DEh	5009 70DEh	500D 70DEh
E2h	16	EPWM_CMPD	5005 70E2h	5009 70E2h	500D 70E2h
E8h	16	EPWM_GLDCTL2	5005 70E8h	5009 70E8h	500D 70E8h
EEh	16	EPWM_SWVDELVAL	5005 70EEh	5009 70EEh	500D 70EEh
100h	16	EPWM_TZSEL	5005 7100h	5009 7100h	500D 7100h
102h	16	EPWM_TZSEL2	5005 7102h	5009 7102h	500D 7102h
104h	16	EPWM_TZDCSEL	5005 7104h	5009 7104h	500D 7104h
108h	16	EPWM_TZCTL	5005 7108h	5009 7108h	500D 7108h
10Ah	16	EPWM_TZCTL2	5005 710Ah	5009 710Ah	500D 710Ah
10Ch	16	EPWM_TZCTLDCA	5005 710Ch	5009 710Ch	500D 710Ch
10Eh	16	EPWM_TZCTLDCB	5005 710Eh	5009 710Eh	500D 710Eh
11Ah	16	EPWM_TZEINT	5005 711Ah	5009 711Ah	500D 711Ah
126h	16	EPWM_TZFLG	5005 7126h	5009 7126h	500D 7126h
128h	16	EPWM_TZCBCFLG	5005 7128h	5009 7128h	500D 7128h
12Ah	16	EPWM_TZOSTFLG	5005 712Ah	5009 712Ah	500D 712Ah
12Eh	16	EPWM_TZCLR	5005 712Eh	5009 712Eh	500D 712Eh
130h	16	EPWM_TZCBCCLR	5005 7130h	5009 7130h	500D 7130h
132h	16	EPWM_TZOSTCLR	5005 7132h	5009 7132h	500D 7132h
136h	16	EPWM_TZFRC	5005 7136h	5009 7136h	500D 7136h
13Ah	16	EPWM_TZTRIPOUTSEL	5005 713Ah	5009 713Ah	500D 713Ah
148h	16	EPWM_ETSEL	5005 7148h	5009 7148h	500D 7148h
14Ch	16	EPWM_ETPS	5005 714Ch	5009 714Ch	500D 714Ch

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Table 3-601. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM29_G2 Physical Address	EPWM30_G2 Physical Address	EPWM31_G2 Physical Address
150h	16	EPWM_ETFLG	5005 7150h	5009 7150h	500D 7150h
154h	16	EPWM_ETCLR	5005 7154h	5009 7154h	500D 7154h
158h	16	EPWM_ETFRC	5005 7158h	5009 7158h	500D 7158h
15Ch	16	EPWM_ETINTPS	5005 715Ch	5009 715Ch	500D 715Ch
160h	16	EPWM_ETSOCPS	5005 7160h	5009 7160h	500D 7160h
164h	16	EPWM_ETCNTINITCTL	5005 7164h	5009 7164h	500D 7164h
168h	16	EPWM_ETCNTINIT	5005 7168h	5009 7168h	500D 7168h
16Ch	16	EPWM_ETINTMIXEN	5005 716Ch	5009 716Ch	500D 716Ch
170h	16	EPWM_ETSOCAMIXEN	5005 7170h	5009 7170h	500D 7170h
174h	16	EPWM_ETSOCBMIXEN	5005 7174h	5009 7174h	500D 7174h
180h	16	EPWM_DCTRIPSEL	5005 7180h	5009 7180h	500D 7180h
186h	16	EPWM_DCACTL	5005 7186h	5009 7186h	500D 7186h
188h	16	EPWM_DCBCTL	5005 7188h	5009 7188h	500D 7188h
18Eh	16	EPWM_DCFCTL	5005 718Eh	5009 718Eh	500D 718Eh
190h	16	EPWM_DCCAPCTL	5005 7190h	5009 7190h	500D 7190h
192h	16	EPWM_DCFOFFSET	5005 7192h	5009 7192h	500D 7192h
194h	16	EPWM_DCFOFFSETCNT	5005 7194h	5009 7194h	500D 7194h
196h	16	EPWM_DCFWINDOW	5005 7196h	5009 7196h	500D 7196h
198h	16	EPWM_DCFWINDOWCNT	5005 7198h	5009 7198h	500D 7198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5005 719Ah	5009 719Ah	500D 719Ah
19Ch	16	EPWM_DCCAPMIXSEL	5005 719Ch	5009 719Ch	500D 719Ch
19Eh	16	EPWM_DCCAP	5005 719Eh	5009 719Eh	500D 719Eh
1A4h	16	EPWM_DCAHTRIPSEL	5005 71A4h	5009 71A4h	500D 71A4h
1A6h	16	EPWM_DCALTRIPSEL	5005 71A6h	5009 71A6h	500D 71A6h
1A8h	16	EPWM_DCBHTRIPSEL	5005 71A8h	5009 71A8h	500D 71A8h
1AAh	16	EPWM_DCBLTRIPSEL	5005 71AAh	5009 71AAh	500D 71AAh
1ACh	16	EPWM_CAPCTL	5005 71ACh	5009 71ACh	500D 71ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5005 71AEh	5009 71AEh	500D 71AEh
1B0h	16	EPWM_CAPINTRIPSEL	5005 71B0h	5009 71B0h	500D 71B0h
1B2h	16	EPWM_CAPTRIPSEL	5005 71B2h	5009 71B2h	500D 71B2h
1F4h	32	EPWM_EPWMLOCK	5005 71F4h	5009 71F4h	500D 71F4h
1FAh	16	EPWM_HWVDELVAL	5005 71FAh	5009 71FAh	500D 71FAh
1FCh	16	EPWM_VCNTVAL	5005 71FCh	5009 71FCh	500D 71FCh
400h	32	EPWM_XCMPCTL1	5005 7400h	5009 7400h	500D 7400h
410h	32	EPWM_XLOADCTL	5005 7410h	5009 7410h	500D 7410h
418h	32	EPWM_XLOAD	5005 7418h	5009 7418h	500D 7418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5005 741Ch	5009 741Ch	500D 741Ch
420h	32	EPWM_XREGSHDW1STS	5005 7420h	5009 7420h	500D 7420h
428h	32	EPWM_XREGSHDW2STS	5005 7428h	5009 7428h	500D 7428h
430h	32	EPWM_XREGSHDW3STS	5005 7430h	5009 7430h	500D 7430h
600h	32	EPWM_XCMP1_ACTIVE	5005 7600h	5009 7600h	500D 7600h
604h	32	EPWM_XCMP2_ACTIVE	5005 7604h	5009 7604h	500D 7604h
608h	32	EPWM_XCMP3_ACTIVE	5005 7608h	5009 7608h	500D 7608h
60Ch	32	EPWM_XCMP4_ACTIVE	5005 760Ch	5009 760Ch	500D 760Ch
610h	32	EPWM_XCMP5_ACTIVE	5005 7610h	5009 7610h	500D 7610h
614h	32	EPWM_XCMP6_ACTIVE	5005 7614h	5009 7614h	500D 7614h

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Table 3-601. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM29_G2 Physical Address	EPWM30_G2 Physical Address	EPWM31_G2 Physical Address
618h	32	EPWM_XCMP7_ACTIVE	5005 7618h	5009 7618h	500D 7618h
61Ch	32	EPWM_XCMP8_ACTIVE	5005 761Ch	5009 761Ch	500D 761Ch
620h	32	EPWM_XTBPRD_ACTIVE	5005 7620h	5009 7620h	500D 7620h
630h	16	EPWM_XAQCTLA_ACTIVE	5005 7630h	5009 7630h	500D 7630h
644h	32	EPWM_XMINMAX_ACTIVE	5005 7644h	5009 7644h	500D 7644h
680h	32	EPWM_XCMP1_SHDW1	5005 7680h	5009 7680h	500D 7680h
684h	32	EPWM_XCMP2_SHDW1	5005 7684h	5009 7684h	500D 7684h
688h	32	EPWM_XCMP3_SHDW1	5005 7688h	5009 7688h	500D 7688h
68Ch	32	EPWM_XCMP4_SHDW1	5005 768Ch	5009 768Ch	500D 768Ch
690h	32	EPWM_XCMP5_SHDW1	5005 7690h	5009 7690h	500D 7690h
694h	32	EPWM_XCMP6_SHDW1	5005 7694h	5009 7694h	500D 7694h
698h	32	EPWM_XCMP7_SHDW1	5005 7698h	5009 7698h	500D 7698h
69Ch	32	EPWM_XCMP8_SHDW1	5005 769Ch	5009 769Ch	500D 769Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5005 76A0h	5009 76A0h	500D 76A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5005 76B0h	5009 76B0h	500D 76B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5005 76B2h	5009 76B2h	500D 76B2h
6BAh	16	EPWM_CMPC_SHDW1	5005 76BAh	5009 76BAh	500D 76BAh
6BEh	16	EPWM_CMPD_SHDW1	5005 76BEh	5009 76BEh	500D 76BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5005 76C4h	5009 76C4h	500D 76C4h
700h	32	EPWM_XCMP1_SHDW2	5005 7700h	5009 7700h	500D 7700h
704h	32	EPWM_XCMP2_SHDW2	5005 7704h	5009 7704h	500D 7704h
708h	32	EPWM_XCMP3_SHDW2	5005 7708h	5009 7708h	500D 7708h
70Ch	32	EPWM_XCMP4_SHDW2	5005 770Ch	5009 770Ch	500D 770Ch
710h	32	EPWM_XCMP5_SHDW2	5005 7710h	5009 7710h	500D 7710h
714h	32	EPWM_XCMP6_SHDW2	5005 7714h	5009 7714h	500D 7714h
718h	32	EPWM_XCMP7_SHDW2	5005 7718h	5009 7718h	500D 7718h
71Ch	32	EPWM_XCMP8_SHDW2	5005 771Ch	5009 771Ch	500D 771Ch
720h	32	EPWM_XTBPRD_SHDW2	5005 7720h	5009 7720h	500D 7720h
730h	16	EPWM_XAQCTLA_SHDW2	5005 7730h	5009 7730h	500D 7730h
732h	16	EPWM_XAQCTLB_SHDW2	5005 7732h	5009 7732h	500D 7732h
73Ah	16	EPWM_CMPC_SHDW2	5005 773Ah	5009 773Ah	500D 773Ah
73Eh	16	EPWM_CMPD_SHDW2	5005 773Eh	5009 773Eh	500D 773Eh
744h	32	EPWM_XMINMAX_SHDW2	5005 7744h	5009 7744h	500D 7744h
780h	32	EPWM_XCMP1_SHDW3	5005 7780h	5009 7780h	500D 7780h
784h	32	EPWM_XCMP2_SHDW3	5005 7784h	5009 7784h	500D 7784h
788h	32	EPWM_XCMP3_SHDW3	5005 7788h	5009 7788h	500D 7788h
78Ch	32	EPWM_XCMP4_SHDW3	5005 778Ch	5009 778Ch	500D 778Ch
790h	32	EPWM_XCMP5_SHDW3	5005 7790h	5009 7790h	500D 7790h
794h	32	EPWM_XCMP6_SHDW3	5005 7794h	5009 7794h	500D 7794h
798h	32	EPWM_XCMP7_SHDW3	5005 7798h	5009 7798h	500D 7798h
79Ch	32	EPWM_XCMP8_SHDW3	5005 779Ch	5009 779Ch	500D 779Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5005 77A0h	5009 77A0h	500D 77A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5005 77B0h	5009 77B0h	500D 77B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5005 77B2h	5009 77B2h	500D 77B2h
7BAh	16	EPWM_CMPC_SHDW3	5005 77BAh	5009 77BAh	500D 77BAh
7BEh	16	EPWM_CMPD_SHDW3	5005 77BEh	5009 77BEh	500D 77BEh

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Table 3-601. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM29_G2 Physical Address	EPWM30_G2 Physical Address	EPWM31_G2 Physical Address
7C4h	32	EPWM_XMINMAX_SHDW3	5005 77C4h	5009 77C4h	500D 77C4h
800h	32	EPWM_DECTL	5005 7800h	5009 7800h	500D 7800h
804h	32	EPWM_DECOMPSEL	5005 7804h	5009 7804h	500D 7804h
808h	32	EPWM_DEACTCTL	5005 7808h	5009 7808h	500D 7808h
80Ch	32	EPWM_DESTS	5005 780Ch	5009 780Ch	500D 780Ch
810h	32	EPWM_DEFRC	5005 7810h	5009 7810h	500D 7810h
814h	32	EPWM_DECLR	5005 7814h	5009 7814h	500D 7814h
820h	32	EPWM_DEMONCNT	5005 7820h	5009 7820h	500D 7820h
824h	32	EPWM_DEMONCTL	5005 7824h	5009 7824h	500D 7824h
828h	32	EPWM_DEMONSTEP	5005 7828h	5009 7828h	500D 7828h
82Ch	32	EPWM_DEMONTHRES	5005 782Ch	5009 782Ch	500D 782Ch
C00h	32	EPWM_MINDBCFG	5005 7C00h	5009 7C00h	500D 7C00h
C04h	32	EPWM_MINDBDLY	5005 7C04h	5009 7C04h	500D 7C04h
C20h	32	EPWM_LUTCTLA	5005 7C20h	5009 7C20h	500D 7C20h
C24h	32	EPWM_LUTCTLB	5005 7C24h	5009 7C24h	500D 7C24h

Table 3-602. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM00_G3 Physical Address	EPWM01_G3 Physical Address	EPWM02_G3 Physical Address
0h	16	EPWM_TBCTL	5001 8000h	5005 8000h	5009 8000h
2h	16	EPWM_TBCTL2	5001 8002h	5005 8002h	5009 8002h
6h	16	EPWM_EPWMSYNCINSEL	5001 8006h	5005 8006h	5009 8006h
8h	16	EPWM_TBCTR	5001 8008h	5005 8008h	5009 8008h
Ah	16	EPWM_TBSTS	5001 800Ah	5005 800Ah	5009 800Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5001 800Ch	5005 800Ch	5009 800Ch
Eh	16	EPWM_TBCTL3	5001 800Eh	5005 800Eh	5009 800Eh
10h	16	EPWM_CMPCTL	5001 8010h	5005 8010h	5009 8010h
12h	16	EPWM_CMPCTL2	5001 8012h	5005 8012h	5009 8012h
18h	16	EPWM_DBCTL	5001 8018h	5005 8018h	5009 8018h
1Ah	16	EPWM_DBCTL2	5001 801Ah	5005 801Ah	5009 801Ah
20h	16	EPWM_AQCTL	5001 8020h	5005 8020h	5009 8020h
22h	16	EPWM_AQTSRCSEL	5001 8022h	5005 8022h	5009 8022h
28h	16	EPWM_PCCTL	5001 8028h	5005 8028h	5009 8028h
30h	16	EPWM_VCAPCTL	5001 8030h	5005 8030h	5009 8030h
32h	16	EPWM_VCNTCFG	5001 8032h	5005 8032h	5009 8032h
40h	16	EPWM_HRCNFG	5001 8040h	5005 8040h	5009 8040h
4Eh	16	EPWM_HRCNFG2	5001 804Eh	5005 804Eh	5009 804Eh
5Ah	16	EPWM_HRPCTL	5001 805Ah	5005 805Ah	5009 805Ah
5Ch	16	EPWM_TRREM	5001 805Ch	5005 805Ch	5009 805Ch
68h	16	EPWM_GLDCTL	5001 8068h	5005 8068h	5009 8068h
6Ah	16	EPWM_GLDCFG	5001 806Ah	5005 806Ah	5009 806Ah
70h	32	EPWM_EPWMXLINK	5001 8070h	5005 8070h	5009 8070h
74h	32	EPWM_EPWMXLINK2	5001 8074h	5005 8074h	5009 8074h
7Ah	16	EPWM_ETEST	5001 807Ah	5005 807Ah	5009 807Ah
7Ch	16	EPWM_EPWMREV	5001 807Ch	5005 807Ch	5009 807Ch
7Eh	16	EPWM_HRPWMREV	5001 807Eh	5005 807Eh	5009 807Eh

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Table 3-602. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM00_G3 Physical Address	EPWM01_G3 Physical Address	EPWM02_G3 Physical Address
80h	16	EPWM_AQCTLA	5001 8080h	5005 8080h	5009 8080h
82h	16	EPWM_AQCTLA2	5001 8082h	5005 8082h	5009 8082h
84h	16	EPWM_AQCTLB	5001 8084h	5005 8084h	5009 8084h
86h	16	EPWM_AQCTLB2	5001 8086h	5005 8086h	5009 8086h
8Eh	16	EPWM_AQSFRC	5001 808Eh	5005 808Eh	5009 808Eh
92h	16	EPWM_AQCSFRC	5001 8092h	5005 8092h	5009 8092h
A0h	16	EPWM_DBREDHR	5001 80A0h	5005 80A0h	5009 80A0h
A2h	16	EPWM_DBRED	5001 80A2h	5005 80A2h	5009 80A2h
A4h	16	EPWM_DBFEDHR	5001 80A4h	5005 80A4h	5009 80A4h
A6h	16	EPWM_DBFED	5001 80A6h	5005 80A6h	5009 80A6h
C0h	32	EPWM_TBPHS	5001 80C0h	5005 80C0h	5009 80C0h
C4h	16	EPWM_TBPRDHR	5001 80C4h	5005 80C4h	5009 80C4h
C6h	16	EPWM_TBPRD	5001 80C6h	5005 80C6h	5009 80C6h
C8h	16	EPWM_TBPRDHRB	5001 80C8h	5005 80C8h	5009 80C8h
D4h	32	EPWM_CMPA	5001 80D4h	5005 80D4h	5009 80D4h
D8h	32	EPWM_CMPB	5001 80D8h	5005 80D8h	5009 80D8h
DEh	16	EPWM_CMPC	5001 80DEh	5005 80DEh	5009 80DEh
E2h	16	EPWM_CMPD	5001 80E2h	5005 80E2h	5009 80E2h
E8h	16	EPWM_GLDCTL2	5001 80E8h	5005 80E8h	5009 80E8h
EEh	16	EPWM_SWVDELVAL	5001 80EEh	5005 80EEh	5009 80EEh
100h	16	EPWM_TZSEL	5001 8100h	5005 8100h	5009 8100h
102h	16	EPWM_TZSEL2	5001 8102h	5005 8102h	5009 8102h
104h	16	EPWM_TZDCSEL	5001 8104h	5005 8104h	5009 8104h
108h	16	EPWM_TZCTL	5001 8108h	5005 8108h	5009 8108h
10Ah	16	EPWM_TZCTL2	5001 810Ah	5005 810Ah	5009 810Ah
10Ch	16	EPWM_TZCTLDCA	5001 810Ch	5005 810Ch	5009 810Ch
10Eh	16	EPWM_TZCTLDCB	5001 810Eh	5005 810Eh	5009 810Eh
11Ah	16	EPWM_TZEINT	5001 811Ah	5005 811Ah	5009 811Ah
126h	16	EPWM_TZFLG	5001 8126h	5005 8126h	5009 8126h
128h	16	EPWM_TZCBCFLG	5001 8128h	5005 8128h	5009 8128h
12Ah	16	EPWM_TZOSTFLG	5001 812Ah	5005 812Ah	5009 812Ah
12Eh	16	EPWM_TZCLR	5001 812Eh	5005 812Eh	5009 812Eh
130h	16	EPWM_TZCBCCLR	5001 8130h	5005 8130h	5009 8130h
132h	16	EPWM_TZOSTCLR	5001 8132h	5005 8132h	5009 8132h
136h	16	EPWM_TZFRC	5001 8136h	5005 8136h	5009 8136h
13Ah	16	EPWM_TZTRIPOUTSEL	5001 813Ah	5005 813Ah	5009 813Ah
148h	16	EPWM_ETSEL	5001 8148h	5005 8148h	5009 8148h
14Ch	16	EPWM_ETPS	5001 814Ch	5005 814Ch	5009 814Ch
150h	16	EPWM_ETFLG	5001 8150h	5005 8150h	5009 8150h
154h	16	EPWM_ETCLR	5001 8154h	5005 8154h	5009 8154h
158h	16	EPWM_ETFRC	5001 8158h	5005 8158h	5009 8158h
15Ch	16	EPWM_ETINTPS	5001 815Ch	5005 815Ch	5009 815Ch
160h	16	EPWM_ETSOCPS	5001 8160h	5005 8160h	5009 8160h
164h	16	EPWM_ETCNTINITCTL	5001 8164h	5005 8164h	5009 8164h
168h	16	EPWM_ETCNTINIT	5001 8168h	5005 8168h	5009 8168h
16Ch	16	EPWM_ETINTMIXEN	5001 816Ch	5005 816Ch	5009 816Ch

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Table 3-602. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM00_G3 Physical Address	EPWM01_G3 Physical Address	EPWM02_G3 Physical Address
170h	16	EPWM_ETSOCAMIXEN	5001 8170h	5005 8170h	5009 8170h
174h	16	EPWM_ETSOCBMIXEN	5001 8174h	5005 8174h	5009 8174h
180h	16	EPWM_DCTRIPSEL	5001 8180h	5005 8180h	5009 8180h
186h	16	EPWM_DCACTL	5001 8186h	5005 8186h	5009 8186h
188h	16	EPWM_DCBCTL	5001 8188h	5005 8188h	5009 8188h
18Eh	16	EPWM_DCFCTL	5001 818Eh	5005 818Eh	5009 818Eh
190h	16	EPWM_DCCAPCTL	5001 8190h	5005 8190h	5009 8190h
192h	16	EPWM_DCFOFFSET	5001 8192h	5005 8192h	5009 8192h
194h	16	EPWM_DCFOFFSETCNT	5001 8194h	5005 8194h	5009 8194h
196h	16	EPWM_DCFWINDOW	5001 8196h	5005 8196h	5009 8196h
198h	16	EPWM_DCFWINDOWCNT	5001 8198h	5005 8198h	5009 8198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5001 819Ah	5005 819Ah	5009 819Ah
19Ch	16	EPWM_DCCAPMIXSEL	5001 819Ch	5005 819Ch	5009 819Ch
19Eh	16	EPWM_DCCAP	5001 819Eh	5005 819Eh	5009 819Eh
1A4h	16	EPWM_DCAHTRIPSEL	5001 81A4h	5005 81A4h	5009 81A4h
1A6h	16	EPWM_DCALTRIPSEL	5001 81A6h	5005 81A6h	5009 81A6h
1A8h	16	EPWM_DCBHTRIPSEL	5001 81A8h	5005 81A8h	5009 81A8h
1AAh	16	EPWM_DCBLTRIPSEL	5001 81AAh	5005 81AAh	5009 81AAh
1ACh	16	EPWM_CAPCTL	5001 81ACh	5005 81ACh	5009 81ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5001 81AEh	5005 81AEh	5009 81AEh
1B0h	16	EPWM_CAPINTRIPSEL	5001 81B0h	5005 81B0h	5009 81B0h
1B2h	16	EPWM_CAPTRIPSEL	5001 81B2h	5005 81B2h	5009 81B2h
1F4h	32	EPWM_EPWMLOCK	5001 81F4h	5005 81F4h	5009 81F4h
1FAh	16	EPWM_HWVDELVAL	5001 81FAh	5005 81FAh	5009 81FAh
1FCh	16	EPWM_VCNTVAL	5001 81FCh	5005 81FCh	5009 81FCh
400h	32	EPWM_XCMPCTL1	5001 8400h	5005 8400h	5009 8400h
410h	32	EPWM_XLOADCTL	5001 8410h	5005 8410h	5009 8410h
418h	32	EPWM_XLOAD	5001 8418h	5005 8418h	5009 8418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5001 841Ch	5005 841Ch	5009 841Ch
420h	32	EPWM_XREGSHDW1STS	5001 8420h	5005 8420h	5009 8420h
428h	32	EPWM_XREGSHDW2STS	5001 8428h	5005 8428h	5009 8428h
430h	32	EPWM_XREGSHDW3STS	5001 8430h	5005 8430h	5009 8430h
600h	32	EPWM_XCMP1_ACTIVE	5001 8600h	5005 8600h	5009 8600h
604h	32	EPWM_XCMP2_ACTIVE	5001 8604h	5005 8604h	5009 8604h
608h	32	EPWM_XCMP3_ACTIVE	5001 8608h	5005 8608h	5009 8608h
60Ch	32	EPWM_XCMP4_ACTIVE	5001 860Ch	5005 860Ch	5009 860Ch
610h	32	EPWM_XCMP5_ACTIVE	5001 8610h	5005 8610h	5009 8610h
614h	32	EPWM_XCMP6_ACTIVE	5001 8614h	5005 8614h	5009 8614h
618h	32	EPWM_XCMP7_ACTIVE	5001 8618h	5005 8618h	5009 8618h
61Ch	32	EPWM_XCMP8_ACTIVE	5001 861Ch	5005 861Ch	5009 861Ch
620h	32	EPWM_XTBPRD_ACTIVE	5001 8620h	5005 8620h	5009 8620h
630h	16	EPWM_XAQCTLA_ACTIVE	5001 8630h	5005 8630h	5009 8630h
644h	32	EPWM_XMINMAX_ACTIVE	5001 8644h	5005 8644h	5009 8644h
680h	32	EPWM_XCMP1_SHDW1	5001 8680h	5005 8680h	5009 8680h
684h	32	EPWM_XCMP2_SHDW1	5001 8684h	5005 8684h	5009 8684h
688h	32	EPWM_XCMP3_SHDW1	5001 8688h	5005 8688h	5009 8688h

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Table 3-602. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM00_G3 Physical Address	EPWM01_G3 Physical Address	EPWM02_G3 Physical Address
68Ch	32	EPWM_XCMP4_SHDW1	5001 868Ch	5005 868Ch	5009 868Ch
690h	32	EPWM_XCMP5_SHDW1	5001 8690h	5005 8690h	5009 8690h
694h	32	EPWM_XCMP6_SHDW1	5001 8694h	5005 8694h	5009 8694h
698h	32	EPWM_XCMP7_SHDW1	5001 8698h	5005 8698h	5009 8698h
69Ch	32	EPWM_XCMP8_SHDW1	5001 869Ch	5005 869Ch	5009 869Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5001 86A0h	5005 86A0h	5009 86A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5001 86B0h	5005 86B0h	5009 86B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5001 86B2h	5005 86B2h	5009 86B2h
6BAh	16	EPWM_CMPC_SHDW1	5001 86BAh	5005 86BAh	5009 86BAh
6BEh	16	EPWM_CMPD_SHDW1	5001 86BEh	5005 86BEh	5009 86BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5001 86C4h	5005 86C4h	5009 86C4h
700h	32	EPWM_XCMP1_SHDW2	5001 8700h	5005 8700h	5009 8700h
704h	32	EPWM_XCMP2_SHDW2	5001 8704h	5005 8704h	5009 8704h
708h	32	EPWM_XCMP3_SHDW2	5001 8708h	5005 8708h	5009 8708h
70Ch	32	EPWM_XCMP4_SHDW2	5001 870Ch	5005 870Ch	5009 870Ch
710h	32	EPWM_XCMP5_SHDW2	5001 8710h	5005 8710h	5009 8710h
714h	32	EPWM_XCMP6_SHDW2	5001 8714h	5005 8714h	5009 8714h
718h	32	EPWM_XCMP7_SHDW2	5001 8718h	5005 8718h	5009 8718h
71Ch	32	EPWM_XCMP8_SHDW2	5001 871Ch	5005 871Ch	5009 871Ch
720h	32	EPWM_XTBPRD_SHDW2	5001 8720h	5005 8720h	5009 8720h
730h	16	EPWM_XAQCTLA_SHDW2	5001 8730h	5005 8730h	5009 8730h
732h	16	EPWM_XAQCTLB_SHDW2	5001 8732h	5005 8732h	5009 8732h
73Ah	16	EPWM_CMPC_SHDW2	5001 873Ah	5005 873Ah	5009 873Ah
73Eh	16	EPWM_CMPD_SHDW2	5001 873Eh	5005 873Eh	5009 873Eh
744h	32	EPWM_XMINMAX_SHDW2	5001 8744h	5005 8744h	5009 8744h
780h	32	EPWM_XCMP1_SHDW3	5001 8780h	5005 8780h	5009 8780h
784h	32	EPWM_XCMP2_SHDW3	5001 8784h	5005 8784h	5009 8784h
788h	32	EPWM_XCMP3_SHDW3	5001 8788h	5005 8788h	5009 8788h
78Ch	32	EPWM_XCMP4_SHDW3	5001 878Ch	5005 878Ch	5009 878Ch
790h	32	EPWM_XCMP5_SHDW3	5001 8790h	5005 8790h	5009 8790h
794h	32	EPWM_XCMP6_SHDW3	5001 8794h	5005 8794h	5009 8794h
798h	32	EPWM_XCMP7_SHDW3	5001 8798h	5005 8798h	5009 8798h
79Ch	32	EPWM_XCMP8_SHDW3	5001 879Ch	5005 879Ch	5009 879Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5001 87A0h	5005 87A0h	5009 87A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5001 87B0h	5005 87B0h	5009 87B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5001 87B2h	5005 87B2h	5009 87B2h
7BAh	16	EPWM_CMPC_SHDW3	5001 87BAh	5005 87BAh	5009 87BAh
7BEh	16	EPWM_CMPD_SHDW3	5001 87BEh	5005 87BEh	5009 87BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5001 87C4h	5005 87C4h	5009 87C4h
800h	32	EPWM_DECTL	5001 8800h	5005 8800h	5009 8800h
804h	32	EPWM_DECOMPSEL	5001 8804h	5005 8804h	5009 8804h
808h	32	EPWM_DEACTCTL	5001 8808h	5005 8808h	5009 8808h
80Ch	32	EPWM_DESTS	5001 880Ch	5005 880Ch	5009 880Ch
810h	32	EPWM_DEFRC	5001 8810h	5005 8810h	5009 8810h
814h	32	EPWM_DECLR	5001 8814h	5005 8814h	5009 8814h
820h	32	EPWM_DEMONCNT	5001 8820h	5005 8820h	5009 8820h

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Table 3-602. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM00_G3 Physical Address	EPWM01_G3 Physical Address	EPWM02_G3 Physical Address
824h	32	EPWM_DEMONCTL	5001 8824h	5005 8824h	5009 8824h
828h	32	EPWM_DEMONSTEP	5001 8828h	5005 8828h	5009 8828h
82Ch	32	EPWM_DEMONTHRES	5001 882Ch	5005 882Ch	5009 882Ch
C00h	32	EPWM_MINDBCFG	5001 8C00h	5005 8C00h	5009 8C00h
C04h	32	EPWM_MINDBDLY	5001 8C04h	5005 8C04h	5009 8C04h
C20h	32	EPWM_LUTCTLA	5001 8C20h	5005 8C20h	5009 8C20h
C24h	32	EPWM_LUTCTLB	5001 8C24h	5005 8C24h	5009 8C24h

Table 3-603. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM03_G3 Physical Address	EPWM04_G3 Physical Address	EPWM05_G3 Physical Address
0h	16	EPWM_TBCTL	500D 8000h	5001 9000h	5005 9000h
2h	16	EPWM_TBCTL2	500D 8002h	5001 9002h	5005 9002h
6h	16	EPWM_EPWMSYNCINSEL	500D 8006h	5001 9006h	5005 9006h
8h	16	EPWM_TBCTR	500D 8008h	5001 9008h	5005 9008h
Ah	16	EPWM_TBSTS	500D 800Ah	5001 900Ah	5005 900Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500D 800Ch	5001 900Ch	5005 900Ch
Eh	16	EPWM_TBCTL3	500D 800Eh	5001 900Eh	5005 900Eh
10h	16	EPWM_CMPCTL	500D 8010h	5001 9010h	5005 9010h
12h	16	EPWM_CMPCTL2	500D 8012h	5001 9012h	5005 9012h
18h	16	EPWM_DBCTL	500D 8018h	5001 9018h	5005 9018h
1Ah	16	EPWM_DBCTL2	500D 801Ah	5001 901Ah	5005 901Ah
20h	16	EPWM_AQCTL	500D 8020h	5001 9020h	5005 9020h
22h	16	EPWM_AQTSRCSEL	500D 8022h	5001 9022h	5005 9022h
28h	16	EPWM_PCCTL	500D 8028h	5001 9028h	5005 9028h
30h	16	EPWM_VCAPCTL	500D 8030h	5001 9030h	5005 9030h
32h	16	EPWM_VCNTCFG	500D 8032h	5001 9032h	5005 9032h
40h	16	EPWM_HRCNFG	500D 8040h	5001 9040h	5005 9040h
4Eh	16	EPWM_HRCNFG2	500D 804Eh	5001 904Eh	5005 904Eh
5Ah	16	EPWM_HRPCTL	500D 805Ah	5001 905Ah	5005 905Ah
5Ch	16	EPWM_TRREM	500D 805Ch	5001 905Ch	5005 905Ch
68h	16	EPWM_GLDCTL	500D 8068h	5001 9068h	5005 9068h
6Ah	16	EPWM_GLDCFG	500D 806Ah	5001 906Ah	5005 906Ah
70h	32	EPWM_EPWMXLINK	500D 8070h	5001 9070h	5005 9070h
74h	32	EPWM_EPWMXLINK2	500D 8074h	5001 9074h	5005 9074h
7Ah	16	EPWM_ETEST	500D 807Ah	5001 907Ah	5005 907Ah
7Ch	16	EPWM_EPWMREV	500D 807Ch	5001 907Ch	5005 907Ch
7Eh	16	EPWM_HRPWMREV	500D 807Eh	5001 907Eh	5005 907Eh
80h	16	EPWM_AQCTLA	500D 8080h	5001 9080h	5005 9080h
82h	16	EPWM_AQCTLA2	500D 8082h	5001 9082h	5005 9082h
84h	16	EPWM_AQCTLB	500D 8084h	5001 9084h	5005 9084h
86h	16	EPWM_AQCTLB2	500D 8086h	5001 9086h	5005 9086h
8Eh	16	EPWM_AQSFRC	500D 808Eh	5001 908Eh	5005 908Eh
92h	16	EPWM_AQCSFRC	500D 8092h	5001 9092h	5005 9092h
A0h	16	EPWM_DBREDHR	500D 80A0h	5001 90A0h	5005 90A0h
A2h	16	EPWM_DBRED	500D 80A2h	5001 90A2h	5005 90A2h

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Table 3-603. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM03_G3 Physical Address	EPWM04_G3 Physical Address	EPWM05_G3 Physical Address
A4h	16	EPWM_DBFEDHR	500D 80A4h	5001 90A4h	5005 90A4h
A6h	16	EPWM_DBFED	500D 80A6h	5001 90A6h	5005 90A6h
C0h	32	EPWM_TBPHS	500D 80C0h	5001 90C0h	5005 90C0h
C4h	16	EPWM_TBPRDHR	500D 80C4h	5001 90C4h	5005 90C4h
C6h	16	EPWM_TBPRD	500D 80C6h	5001 90C6h	5005 90C6h
C8h	16	EPWM_TBPRDHRB	500D 80C8h	5001 90C8h	5005 90C8h
D4h	32	EPWM_CMPA	500D 80D4h	5001 90D4h	5005 90D4h
D8h	32	EPWM_CMPB	500D 80D8h	5001 90D8h	5005 90D8h
DEh	16	EPWM_CMPC	500D 80DEh	5001 90DEh	5005 90DEh
E2h	16	EPWM_CMPD	500D 80E2h	5001 90E2h	5005 90E2h
E8h	16	EPWM_GLDCTL2	500D 80E8h	5001 90E8h	5005 90E8h
EEh	16	EPWM_SWVDELVAL	500D 80EEh	5001 90EEh	5005 90EEh
100h	16	EPWM_TZSEL	500D 8100h	5001 9100h	5005 9100h
102h	16	EPWM_TZSEL2	500D 8102h	5001 9102h	5005 9102h
104h	16	EPWM_TZDCSEL	500D 8104h	5001 9104h	5005 9104h
108h	16	EPWM_TZCTL	500D 8108h	5001 9108h	5005 9108h
10Ah	16	EPWM_TZCTL2	500D 810Ah	5001 910Ah	5005 910Ah
10Ch	16	EPWM_TZCTLDCA	500D 810Ch	5001 910Ch	5005 910Ch
10Eh	16	EPWM_TZCTLDCB	500D 810Eh	5001 910Eh	5005 910Eh
11Ah	16	EPWM_TZEINT	500D 811Ah	5001 911Ah	5005 911Ah
126h	16	EPWM_TZFLG	500D 8126h	5001 9126h	5005 9126h
128h	16	EPWM_TZCBCFLG	500D 8128h	5001 9128h	5005 9128h
12Ah	16	EPWM_TZOSTFLG	500D 812Ah	5001 912Ah	5005 912Ah
12Eh	16	EPWM_TZCLR	500D 812Eh	5001 912Eh	5005 912Eh
130h	16	EPWM_TZCBCCLR	500D 8130h	5001 9130h	5005 9130h
132h	16	EPWM_TZOSTCLR	500D 8132h	5001 9132h	5005 9132h
136h	16	EPWM_TZFRC	500D 8136h	5001 9136h	5005 9136h
13Ah	16	EPWM_TZTRIPOUTSEL	500D 813Ah	5001 913Ah	5005 913Ah
148h	16	EPWM_ETSEL	500D 8148h	5001 9148h	5005 9148h
14Ch	16	EPWM_ETPS	500D 814Ch	5001 914Ch	5005 914Ch
150h	16	EPWM_ETFLG	500D 8150h	5001 9150h	5005 9150h
154h	16	EPWM_ETCLR	500D 8154h	5001 9154h	5005 9154h
158h	16	EPWM_ETFRC	500D 8158h	5001 9158h	5005 9158h
15Ch	16	EPWM_ETINTPS	500D 815Ch	5001 915Ch	5005 915Ch
160h	16	EPWM_ETSOCPS	500D 8160h	5001 9160h	5005 9160h
164h	16	EPWM_ETCNTINITCTL	500D 8164h	5001 9164h	5005 9164h
168h	16	EPWM_ETCNTINIT	500D 8168h	5001 9168h	5005 9168h
16Ch	16	EPWM_ETINTMIXEN	500D 816Ch	5001 916Ch	5005 916Ch
170h	16	EPWM_ETSOCAMIXEN	500D 8170h	5001 9170h	5005 9170h
174h	16	EPWM_ETSOCBMIXEN	500D 8174h	5001 9174h	5005 9174h
180h	16	EPWM_DCTRIPSEL	500D 8180h	5001 9180h	5005 9180h
186h	16	EPWM_DCACTL	500D 8186h	5001 9186h	5005 9186h
188h	16	EPWM_DCBCTL	500D 8188h	5001 9188h	5005 9188h
18Eh	16	EPWM_DCFCTL	500D 818Eh	5001 918Eh	5005 918Eh
190h	16	EPWM_DCCAPCTL	500D 8190h	5001 9190h	5005 9190h
192h	16	EPWM_DCFOFFSET	500D 8192h	5001 9192h	5005 9192h

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Table 3-603. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM03_G3 Physical Address	EPWM04_G3 Physical Address	EPWM05_G3 Physical Address
194h	16	EPWM_DCFOFFSETCNT	500D 8194h	5001 9194h	5005 9194h
196h	16	EPWM_DCFWINDOW	500D 8196h	5001 9196h	5005 9196h
198h	16	EPWM_DCFWINDOWCNT	500D 8198h	5001 9198h	5005 9198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500D 819Ah	5001 919Ah	5005 919Ah
19Ch	16	EPWM_DCCAPMIXSEL	500D 819Ch	5001 919Ch	5005 919Ch
19Eh	16	EPWM_DCCAP	500D 819Eh	5001 919Eh	5005 919Eh
1A4h	16	EPWM_DCAHTRIPSEL	500D 81A4h	5001 91A4h	5005 91A4h
1A6h	16	EPWM_DCALTRIPSEL	500D 81A6h	5001 91A6h	5005 91A6h
1A8h	16	EPWM_DCBHTRIPSEL	500D 81A8h	5001 91A8h	5005 91A8h
1AAh	16	EPWM_DCBLTRIPSEL	500D 81AAh	5001 91AAh	5005 91AAh
1ACh	16	EPWM_CAPCTL	500D 81ACh	5001 91ACh	5005 91ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500D 81AEh	5001 91AEh	5005 91AEh
1B0h	16	EPWM_CAPINTRIPSEL	500D 81B0h	5001 91B0h	5005 91B0h
1B2h	16	EPWM_CAPTRIPSEL	500D 81B2h	5001 91B2h	5005 91B2h
1F4h	32	EPWM_EPWMLOCK	500D 81F4h	5001 91F4h	5005 91F4h
1FAh	16	EPWM_HWVDELVAL	500D 81FAh	5001 91FAh	5005 91FAh
1FCh	16	EPWM_VCNTVAL	500D 81FCh	5001 91FCh	5005 91FCh
400h	32	EPWM_XCMPCTL1	500D 8400h	5001 9400h	5005 9400h
410h	32	EPWM_XLOADCTL	500D 8410h	5001 9410h	5005 9410h
418h	32	EPWM_XLOAD	500D 8418h	5001 9418h	5005 9418h
41Ch	32	EPWM_EPWMXLINKXLOAD	500D 841Ch	5001 941Ch	5005 941Ch
420h	32	EPWM_XREGSHDW1STS	500D 8420h	5001 9420h	5005 9420h
428h	32	EPWM_XREGSHDW2STS	500D 8428h	5001 9428h	5005 9428h
430h	32	EPWM_XREGSHDW3STS	500D 8430h	5001 9430h	5005 9430h
600h	32	EPWM_XCMP1_ACTIVE	500D 8600h	5001 9600h	5005 9600h
604h	32	EPWM_XCMP2_ACTIVE	500D 8604h	5001 9604h	5005 9604h
608h	32	EPWM_XCMP3_ACTIVE	500D 8608h	5001 9608h	5005 9608h
60Ch	32	EPWM_XCMP4_ACTIVE	500D 860Ch	5001 960Ch	5005 960Ch
610h	32	EPWM_XCMP5_ACTIVE	500D 8610h	5001 9610h	5005 9610h
614h	32	EPWM_XCMP6_ACTIVE	500D 8614h	5001 9614h	5005 9614h
618h	32	EPWM_XCMP7_ACTIVE	500D 8618h	5001 9618h	5005 9618h
61Ch	32	EPWM_XCMP8_ACTIVE	500D 861Ch	5001 961Ch	5005 961Ch
620h	32	EPWM_XTBPRD_ACTIVE	500D 8620h	5001 9620h	5005 9620h
630h	16	EPWM_XAQCTLA_ACTIVE	500D 8630h	5001 9630h	5005 9630h
644h	32	EPWM_XMINMAX_ACTIVE	500D 8644h	5001 9644h	5005 9644h
680h	32	EPWM_XCMP1_SHDW1	500D 8680h	5001 9680h	5005 9680h
684h	32	EPWM_XCMP2_SHDW1	500D 8684h	5001 9684h	5005 9684h
688h	32	EPWM_XCMP3_SHDW1	500D 8688h	5001 9688h	5005 9688h
68Ch	32	EPWM_XCMP4_SHDW1	500D 868Ch	5001 968Ch	5005 968Ch
690h	32	EPWM_XCMP5_SHDW1	500D 8690h	5001 9690h	5005 9690h
694h	32	EPWM_XCMP6_SHDW1	500D 8694h	5001 9694h	5005 9694h
698h	32	EPWM_XCMP7_SHDW1	500D 8698h	5001 9698h	5005 9698h
69Ch	32	EPWM_XCMP8_SHDW1	500D 869Ch	5001 969Ch	5005 969Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500D 86A0h	5001 96A0h	5005 96A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500D 86B0h	5001 96B0h	5005 96B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500D 86B2h	5001 96B2h	5005 96B2h

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Table 3-603. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM03_G3 Physical Address	EPWM04_G3 Physical Address	EPWM05_G3 Physical Address
6BAh	16	EPWM_CMPC_SHDW1	500D 86BAh	5001 96BAh	5005 96BAh
6BEh	16	EPWM_CMPD_SHDW1	500D 86BEh	5001 96BEh	5005 96BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500D 86C4h	5001 96C4h	5005 96C4h
700h	32	EPWM_XCMP1_SHDW2	500D 8700h	5001 9700h	5005 9700h
704h	32	EPWM_XCMP2_SHDW2	500D 8704h	5001 9704h	5005 9704h
708h	32	EPWM_XCMP3_SHDW2	500D 8708h	5001 9708h	5005 9708h
70Ch	32	EPWM_XCMP4_SHDW2	500D 870Ch	5001 970Ch	5005 970Ch
710h	32	EPWM_XCMP5_SHDW2	500D 8710h	5001 9710h	5005 9710h
714h	32	EPWM_XCMP6_SHDW2	500D 8714h	5001 9714h	5005 9714h
718h	32	EPWM_XCMP7_SHDW2	500D 8718h	5001 9718h	5005 9718h
71Ch	32	EPWM_XCMP8_SHDW2	500D 871Ch	5001 971Ch	5005 971Ch
720h	32	EPWM_XTBPRD_SHDW2	500D 8720h	5001 9720h	5005 9720h
730h	16	EPWM_XAQCTLA_SHDW2	500D 8730h	5001 9730h	5005 9730h
732h	16	EPWM_XAQCTLB_SHDW2	500D 8732h	5001 9732h	5005 9732h
73Ah	16	EPWM_CMPC_SHDW2	500D 873Ah	5001 973Ah	5005 973Ah
73Eh	16	EPWM_CMPD_SHDW2	500D 873Eh	5001 973Eh	5005 973Eh
744h	32	EPWM_XMINMAX_SHDW2	500D 8744h	5001 9744h	5005 9744h
780h	32	EPWM_XCMP1_SHDW3	500D 8780h	5001 9780h	5005 9780h
784h	32	EPWM_XCMP2_SHDW3	500D 8784h	5001 9784h	5005 9784h
788h	32	EPWM_XCMP3_SHDW3	500D 8788h	5001 9788h	5005 9788h
78Ch	32	EPWM_XCMP4_SHDW3	500D 878Ch	5001 978Ch	5005 978Ch
790h	32	EPWM_XCMP5_SHDW3	500D 8790h	5001 9790h	5005 9790h
794h	32	EPWM_XCMP6_SHDW3	500D 8794h	5001 9794h	5005 9794h
798h	32	EPWM_XCMP7_SHDW3	500D 8798h	5001 9798h	5005 9798h
79Ch	32	EPWM_XCMP8_SHDW3	500D 879Ch	5001 979Ch	5005 979Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500D 87A0h	5001 97A0h	5005 97A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500D 87B0h	5001 97B0h	5005 97B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500D 87B2h	5001 97B2h	5005 97B2h
7BAh	16	EPWM_CMPC_SHDW3	500D 87BAh	5001 97BAh	5005 97BAh
7BEh	16	EPWM_CMPD_SHDW3	500D 87BEh	5001 97BEh	5005 97BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500D 87C4h	5001 97C4h	5005 97C4h
800h	32	EPWM_DECTL	500D 8800h	5001 9800h	5005 9800h
804h	32	EPWM_DECOMPSEL	500D 8804h	5001 9804h	5005 9804h
808h	32	EPWM_DEACTCTL	500D 8808h	5001 9808h	5005 9808h
80Ch	32	EPWM_DESTS	500D 880Ch	5001 980Ch	5005 980Ch
810h	32	EPWM_DEFRC	500D 8810h	5001 9810h	5005 9810h
814h	32	EPWM_DECLR	500D 8814h	5001 9814h	5005 9814h
820h	32	EPWM_DEMONCNT	500D 8820h	5001 9820h	5005 9820h
824h	32	EPWM_DEMONCTL	500D 8824h	5001 9824h	5005 9824h
828h	32	EPWM_DEMONSTEP	500D 8828h	5001 9828h	5005 9828h
82Ch	32	EPWM_DEMONTHRES	500D 882Ch	5001 982Ch	5005 982Ch
C00h	32	EPWM_MINDBCFG	500D 8C00h	5001 9C00h	5005 9C00h
C04h	32	EPWM_MINDBDLY	500D 8C04h	5001 9C04h	5005 9C04h
C20h	32	EPWM_LUTCTLA	500D 8C20h	5001 9C20h	5005 9C20h
C24h	32	EPWM_LUTCTLB	500D 8C24h	5001 9C24h	5005 9C24h

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Table 3-604. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM06_G3 Physical Address	EPWM07_G3 Physical Address	EPWM08_G3 Physical Address
0h	16	EPWM_TBCTL	5009 9000h	500D 9000h	5001 A000h
2h	16	EPWM_TBCTL2	5009 9002h	500D 9002h	5001 A002h
6h	16	EPWM_EPWMSYNCINSEL	5009 9006h	500D 9006h	5001 A006h
8h	16	EPWM_TBCTR	5009 9008h	500D 9008h	5001 A008h
Ah	16	EPWM_TBSTS	5009 900Ah	500D 900Ah	5001 A00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5009 900Ch	500D 900Ch	5001 A00Ch
Eh	16	EPWM_TBCTL3	5009 900Eh	500D 900Eh	5001 A00Eh
10h	16	EPWM_CMPCTL	5009 9010h	500D 9010h	5001 A010h
12h	16	EPWM_CMPCTL2	5009 9012h	500D 9012h	5001 A012h
18h	16	EPWM_DBCTL	5009 9018h	500D 9018h	5001 A018h
1Ah	16	EPWM_DBCTL2	5009 901Ah	500D 901Ah	5001 A01Ah
20h	16	EPWM_AQCTL	5009 9020h	500D 9020h	5001 A020h
22h	16	EPWM_AQTSRCSEL	5009 9022h	500D 9022h	5001 A022h
28h	16	EPWM_PCCTL	5009 9028h	500D 9028h	5001 A028h
30h	16	EPWM_VCAPCTL	5009 9030h	500D 9030h	5001 A030h
32h	16	EPWM_VCNTCFG	5009 9032h	500D 9032h	5001 A032h
40h	16	EPWM_HRCNFG	5009 9040h	500D 9040h	5001 A040h
4Eh	16	EPWM_HRCNFG2	5009 904Eh	500D 904Eh	5001 A04Eh
5Ah	16	EPWM_HRPCTL	5009 905Ah	500D 905Ah	5001 A05Ah
5Ch	16	EPWM_TRREM	5009 905Ch	500D 905Ch	5001 A05Ch
68h	16	EPWM_GLDCTL	5009 9068h	500D 9068h	5001 A068h
6Ah	16	EPWM_GLDCFG	5009 906Ah	500D 906Ah	5001 A06Ah
70h	32	EPWM_EPWMXLINK	5009 9070h	500D 9070h	5001 A070h
74h	32	EPWM_EPWMXLINK2	5009 9074h	500D 9074h	5001 A074h
7Ah	16	EPWM_ETEST	5009 907Ah	500D 907Ah	5001 A07Ah
7Ch	16	EPWM_EPWMREV	5009 907Ch	500D 907Ch	5001 A07Ch
7Eh	16	EPWM_HRPWMREV	5009 907Eh	500D 907Eh	5001 A07Eh
80h	16	EPWM_AQCTLA	5009 9080h	500D 9080h	5001 A080h
82h	16	EPWM_AQCTLA2	5009 9082h	500D 9082h	5001 A082h
84h	16	EPWM_AQCTLB	5009 9084h	500D 9084h	5001 A084h
86h	16	EPWM_AQCTLB2	5009 9086h	500D 9086h	5001 A086h
8Eh	16	EPWM_AQSFRC	5009 908Eh	500D 908Eh	5001 A08Eh
92h	16	EPWM_AQCSFRC	5009 9092h	500D 9092h	5001 A092h
A0h	16	EPWM_DBREDHR	5009 90A0h	500D 90A0h	5001 A0A0h
A2h	16	EPWM_DBRED	5009 90A2h	500D 90A2h	5001 A0A2h
A4h	16	EPWM_DBFEDHR	5009 90A4h	500D 90A4h	5001 A0A4h
A6h	16	EPWM_DBFED	5009 90A6h	500D 90A6h	5001 A0A6h
C0h	32	EPWM_TBPHS	5009 90C0h	500D 90C0h	5001 A0C0h
C4h	16	EPWM_TBPRDHR	5009 90C4h	500D 90C4h	5001 A0C4h
C6h	16	EPWM_TBPRD	5009 90C6h	500D 90C6h	5001 A0C6h
C8h	16	EPWM_TBPRDHRB	5009 90C8h	500D 90C8h	5001 A0C8h
D4h	32	EPWM_CMPA	5009 90D4h	500D 90D4h	5001 A0D4h
D8h	32	EPWM_CMPB	5009 90D8h	500D 90D8h	5001 A0D8h
DEh	16	EPWM_CMPC	5009 90DEh	500D 90DEh	5001 A0DEh
E2h	16	EPWM_CMPD	5009 90E2h	500D 90E2h	5001 A0E2h

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Table 3-604. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM06_G3 Physical Address	EPWM07_G3 Physical Address	EPWM08_G3 Physical Address
E8h	16	EPWM_GLDCTL2	5009 90E8h	500D 90E8h	5001 A0E8h
EEh	16	EPWM_SWVDELVAL	5009 90EEh	500D 90EEh	5001 A0EEh
100h	16	EPWM_TZSEL	5009 9100h	500D 9100h	5001 A100h
102h	16	EPWM_TZSEL2	5009 9102h	500D 9102h	5001 A102h
104h	16	EPWM_TZDCSEL	5009 9104h	500D 9104h	5001 A104h
108h	16	EPWM_TZCTL	5009 9108h	500D 9108h	5001 A108h
10Ah	16	EPWM_TZCTL2	5009 910Ah	500D 910Ah	5001 A10Ah
10Ch	16	EPWM_TZCTLDCA	5009 910Ch	500D 910Ch	5001 A10Ch
10Eh	16	EPWM_TZCTLDCB	5009 910Eh	500D 910Eh	5001 A10Eh
11Ah	16	EPWM_TZEINT	5009 911Ah	500D 911Ah	5001 A11Ah
126h	16	EPWM_TZFLG	5009 9126h	500D 9126h	5001 A126h
128h	16	EPWM_TZCBCFLG	5009 9128h	500D 9128h	5001 A128h
12Ah	16	EPWM_TZOSTFLG	5009 912Ah	500D 912Ah	5001 A12Ah
12Eh	16	EPWM_TZCLR	5009 912Eh	500D 912Eh	5001 A12Eh
130h	16	EPWM_TZCBCCLR	5009 9130h	500D 9130h	5001 A130h
132h	16	EPWM_TZOSTCLR	5009 9132h	500D 9132h	5001 A132h
136h	16	EPWM_TZFRC	5009 9136h	500D 9136h	5001 A136h
13Ah	16	EPWM_TZTRIPOUTSEL	5009 913Ah	500D 913Ah	5001 A13Ah
148h	16	EPWM_ETSEL	5009 9148h	500D 9148h	5001 A148h
14Ch	16	EPWM_ETPS	5009 914Ch	500D 914Ch	5001 A14Ch
150h	16	EPWM_ETFLG	5009 9150h	500D 9150h	5001 A150h
154h	16	EPWM_ETCLR	5009 9154h	500D 9154h	5001 A154h
158h	16	EPWM_ETFRC	5009 9158h	500D 9158h	5001 A158h
15Ch	16	EPWM_ETINTPS	5009 915Ch	500D 915Ch	5001 A15Ch
160h	16	EPWM_ETSOCPS	5009 9160h	500D 9160h	5001 A160h
164h	16	EPWM_ETCNTINITCTL	5009 9164h	500D 9164h	5001 A164h
168h	16	EPWM_ETCNTINIT	5009 9168h	500D 9168h	5001 A168h
16Ch	16	EPWM_ETINTMIXEN	5009 916Ch	500D 916Ch	5001 A16Ch
170h	16	EPWM_ETSOCAMIXEN	5009 9170h	500D 9170h	5001 A170h
174h	16	EPWM_ETSOCBMIXEN	5009 9174h	500D 9174h	5001 A174h
180h	16	EPWM_DCTRIPSEL	5009 9180h	500D 9180h	5001 A180h
186h	16	EPWM_DCACTL	5009 9186h	500D 9186h	5001 A186h
188h	16	EPWM_DCBCTL	5009 9188h	500D 9188h	5001 A188h
18Eh	16	EPWM_DCFCTL	5009 918Eh	500D 918Eh	5001 A18Eh
190h	16	EPWM_DCCAPCTL	5009 9190h	500D 9190h	5001 A190h
192h	16	EPWM_DCFOFFSET	5009 9192h	500D 9192h	5001 A192h
194h	16	EPWM_DCFOFFSETCNT	5009 9194h	500D 9194h	5001 A194h
196h	16	EPWM_DCFWINDOW	5009 9196h	500D 9196h	5001 A196h
198h	16	EPWM_DCFWINDOWCNT	5009 9198h	500D 9198h	5001 A198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5009 919Ah	500D 919Ah	5001 A19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5009 919Ch	500D 919Ch	5001 A19Ch
19Eh	16	EPWM_DCCAP	5009 919Eh	500D 919Eh	5001 A19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5009 91A4h	500D 91A4h	5001 A1A4h
1A6h	16	EPWM_DCALTRIPSEL	5009 91A6h	500D 91A6h	5001 A1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5009 91A8h	500D 91A8h	5001 A1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5009 91AAh	500D 91AAh	5001 A1AAh

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Table 3-604. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM06_G3 Physical Address	EPWM07_G3 Physical Address	EPWM08_G3 Physical Address
1ACh	16	EPWM_CAPCTL	5009 91ACh	500D 91ACh	5001 A1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5009 91AEh	500D 91AEh	5001 A1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5009 91B0h	500D 91B0h	5001 A1B0h
1B2h	16	EPWM_CAPTRIPSEL	5009 91B2h	500D 91B2h	5001 A1B2h
1F4h	32	EPWM_EPWMLOCK	5009 91F4h	500D 91F4h	5001 A1F4h
1FAh	16	EPWM_HWVDELVAL	5009 91FAh	500D 91FAh	5001 A1FAh
1FCh	16	EPWM_VCNTVAL	5009 91FCh	500D 91FCh	5001 A1FCh
400h	32	EPWM_XCMPCTL1	5009 9400h	500D 9400h	5001 A400h
410h	32	EPWM_XLOADCTL	5009 9410h	500D 9410h	5001 A410h
418h	32	EPWM_XLOAD	5009 9418h	500D 9418h	5001 A418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5009 941Ch	500D 941Ch	5001 A41Ch
420h	32	EPWM_XREGSHDW1STS	5009 9420h	500D 9420h	5001 A420h
428h	32	EPWM_XREGSHDW2STS	5009 9428h	500D 9428h	5001 A428h
430h	32	EPWM_XREGSHDW3STS	5009 9430h	500D 9430h	5001 A430h
600h	32	EPWM_XCMP1_ACTIVE	5009 9600h	500D 9600h	5001 A600h
604h	32	EPWM_XCMP2_ACTIVE	5009 9604h	500D 9604h	5001 A604h
608h	32	EPWM_XCMP3_ACTIVE	5009 9608h	500D 9608h	5001 A608h
60Ch	32	EPWM_XCMP4_ACTIVE	5009 960Ch	500D 960Ch	5001 A60Ch
610h	32	EPWM_XCMP5_ACTIVE	5009 9610h	500D 9610h	5001 A610h
614h	32	EPWM_XCMP6_ACTIVE	5009 9614h	500D 9614h	5001 A614h
618h	32	EPWM_XCMP7_ACTIVE	5009 9618h	500D 9618h	5001 A618h
61Ch	32	EPWM_XCMP8_ACTIVE	5009 961Ch	500D 961Ch	5001 A61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5009 9620h	500D 9620h	5001 A620h
630h	16	EPWM_XAQCTLA_ACTIVE	5009 9630h	500D 9630h	5001 A630h
644h	32	EPWM_XMINMAX_ACTIVE	5009 9644h	500D 9644h	5001 A644h
680h	32	EPWM_XCMP1_SHDW1	5009 9680h	500D 9680h	5001 A680h
684h	32	EPWM_XCMP2_SHDW1	5009 9684h	500D 9684h	5001 A684h
688h	32	EPWM_XCMP3_SHDW1	5009 9688h	500D 9688h	5001 A688h
68Ch	32	EPWM_XCMP4_SHDW1	5009 968Ch	500D 968Ch	5001 A68Ch
690h	32	EPWM_XCMP5_SHDW1	5009 9690h	500D 9690h	5001 A690h
694h	32	EPWM_XCMP6_SHDW1	5009 9694h	500D 9694h	5001 A694h
698h	32	EPWM_XCMP7_SHDW1	5009 9698h	500D 9698h	5001 A698h
69Ch	32	EPWM_XCMP8_SHDW1	5009 969Ch	500D 969Ch	5001 A69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5009 96A0h	500D 96A0h	5001 A6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5009 96B0h	500D 96B0h	5001 A6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5009 96B2h	500D 96B2h	5001 A6B2h
6BAh	16	EPWM_CMPC_SHDW1	5009 96BAh	500D 96BAh	5001 A6BAh
6BEh	16	EPWM_CMPD_SHDW1	5009 96BEh	500D 96BEh	5001 A6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5009 96C4h	500D 96C4h	5001 A6C4h
700h	32	EPWM_XCMP1_SHDW2	5009 9700h	500D 9700h	5001 A700h
704h	32	EPWM_XCMP2_SHDW2	5009 9704h	500D 9704h	5001 A704h
708h	32	EPWM_XCMP3_SHDW2	5009 9708h	500D 9708h	5001 A708h
70Ch	32	EPWM_XCMP4_SHDW2	5009 970Ch	500D 970Ch	5001 A70Ch
710h	32	EPWM_XCMP5_SHDW2	5009 9710h	500D 9710h	5001 A710h
714h	32	EPWM_XCMP6_SHDW2	5009 9714h	500D 9714h	5001 A714h
718h	32	EPWM_XCMP7_SHDW2	5009 9718h	500D 9718h	5001 A718h

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Table 3-604. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM06_G3 Physical Address	EPWM07_G3 Physical Address	EPWM08_G3 Physical Address
71Ch	32	EPWM_XCMP8_SHDW2	5009 971Ch	500D 971Ch	5001 A71Ch
720h	32	EPWM_XTBPRD_SHDW2	5009 9720h	500D 9720h	5001 A720h
730h	16	EPWM_XAQCTLA_SHDW2	5009 9730h	500D 9730h	5001 A730h
732h	16	EPWM_XAQCTLB_SHDW2	5009 9732h	500D 9732h	5001 A732h
73Ah	16	EPWM_CMPC_SHDW2	5009 973Ah	500D 973Ah	5001 A73Ah
73Eh	16	EPWM_CMPD_SHDW2	5009 973Eh	500D 973Eh	5001 A73Eh
744h	32	EPWM_XMINMAX_SHDW2	5009 9744h	500D 9744h	5001 A744h
780h	32	EPWM_XCMP1_SHDW3	5009 9780h	500D 9780h	5001 A780h
784h	32	EPWM_XCMP2_SHDW3	5009 9784h	500D 9784h	5001 A784h
788h	32	EPWM_XCMP3_SHDW3	5009 9788h	500D 9788h	5001 A788h
78Ch	32	EPWM_XCMP4_SHDW3	5009 978Ch	500D 978Ch	5001 A78Ch
790h	32	EPWM_XCMP5_SHDW3	5009 9790h	500D 9790h	5001 A790h
794h	32	EPWM_XCMP6_SHDW3	5009 9794h	500D 9794h	5001 A794h
798h	32	EPWM_XCMP7_SHDW3	5009 9798h	500D 9798h	5001 A798h
79Ch	32	EPWM_XCMP8_SHDW3	5009 979Ch	500D 979Ch	5001 A79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5009 97A0h	500D 97A0h	5001 A7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5009 97B0h	500D 97B0h	5001 A7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5009 97B2h	500D 97B2h	5001 A7B2h
7BAh	16	EPWM_CMPC_SHDW3	5009 97BAh	500D 97BAh	5001 A7BAh
7BEh	16	EPWM_CMPD_SHDW3	5009 97BEh	500D 97BEh	5001 A7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5009 97C4h	500D 97C4h	5001 A7C4h
800h	32	EPWM_DECTL	5009 9800h	500D 9800h	5001 A800h
804h	32	EPWM_DECOMPSEL	5009 9804h	500D 9804h	5001 A804h
808h	32	EPWM_DEACTCTL	5009 9808h	500D 9808h	5001 A808h
80Ch	32	EPWM_DESTS	5009 980Ch	500D 980Ch	5001 A80Ch
810h	32	EPWM_DEFRC	5009 9810h	500D 9810h	5001 A810h
814h	32	EPWM_DECLR	5009 9814h	500D 9814h	5001 A814h
820h	32	EPWM_DEMONCNT	5009 9820h	500D 9820h	5001 A820h
824h	32	EPWM_DEMONCTL	5009 9824h	500D 9824h	5001 A824h
828h	32	EPWM_DEMONSTEP	5009 9828h	500D 9828h	5001 A828h
82Ch	32	EPWM_DEMONTHRES	5009 982Ch	500D 982Ch	5001 A82Ch
C00h	32	EPWM_MINDBCFG	5009 9C00h	500D 9C00h	5001 AC00h
C04h	32	EPWM_MINDBDLY	5009 9C04h	500D 9C04h	5001 AC04h
C20h	32	EPWM_LUTCTLA	5009 9C20h	500D 9C20h	5001 AC20h
C24h	32	EPWM_LUTCTLB	5009 9C24h	500D 9C24h	5001 AC24h

Table 3-605. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM09_G3 Physical Address	EPWM10_G3 Physical Address	EPWM11_G3 Physical Address
0h	16	EPWM_TBCTL	5005 A000h	5009 A000h	500D A000h
2h	16	EPWM_TBCTL2	5005 A002h	5009 A002h	500D A002h
6h	16	EPWM_EPWMSYNCINSEL	5005 A006h	5009 A006h	500D A006h
8h	16	EPWM_TBCTR	5005 A008h	5009 A008h	500D A008h
Ah	16	EPWM_TBSTS	5005 A00Ah	5009 A00Ah	500D A00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5005 A00Ch	5009 A00Ch	500D A00Ch
Eh	16	EPWM_TBCTL3	5005 A00Eh	5009 A00Eh	500D A00Eh

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Table 3-605. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM09_G3 Physical Address	EPWM10_G3 Physical Address	EPWM11_G3 Physical Address
10h	16	EPWM_CMPCTL	5005 A010h	5009 A010h	500D A010h
12h	16	EPWM_CMPCTL2	5005 A012h	5009 A012h	500D A012h
18h	16	EPWM_DBCTL	5005 A018h	5009 A018h	500D A018h
1Ah	16	EPWM_DBCTL2	5005 A01Ah	5009 A01Ah	500D A01Ah
20h	16	EPWM_AQCTL	5005 A020h	5009 A020h	500D A020h
22h	16	EPWM_AQTSRCSEL	5005 A022h	5009 A022h	500D A022h
28h	16	EPWM_PCCTL	5005 A028h	5009 A028h	500D A028h
30h	16	EPWM_VCAPCTL	5005 A030h	5009 A030h	500D A030h
32h	16	EPWM_VCNTCFG	5005 A032h	5009 A032h	500D A032h
40h	16	EPWM_HRCNFG	5005 A040h	5009 A040h	500D A040h
4Eh	16	EPWM_HRCNFG2	5005 A04Eh	5009 A04Eh	500D A04Eh
5Ah	16	EPWM_HRPCTL	5005 A05Ah	5009 A05Ah	500D A05Ah
5Ch	16	EPWM_TRREM	5005 A05Ch	5009 A05Ch	500D A05Ch
68h	16	EPWM_GLDCTL	5005 A068h	5009 A068h	500D A068h
6Ah	16	EPWM_GLDCFG	5005 A06Ah	5009 A06Ah	500D A06Ah
70h	32	EPWM_EPWMXLINK	5005 A070h	5009 A070h	500D A070h
74h	32	EPWM_EPWMXLINK2	5005 A074h	5009 A074h	500D A074h
7Ah	16	EPWM_ETEST	5005 A07Ah	5009 A07Ah	500D A07Ah
7Ch	16	EPWM_EPWMREV	5005 A07Ch	5009 A07Ch	500D A07Ch
7Eh	16	EPWM_HRPWMREV	5005 A07Eh	5009 A07Eh	500D A07Eh
80h	16	EPWM_AQCTLA	5005 A080h	5009 A080h	500D A080h
82h	16	EPWM_AQCTLA2	5005 A082h	5009 A082h	500D A082h
84h	16	EPWM_AQCTLB	5005 A084h	5009 A084h	500D A084h
86h	16	EPWM_AQCTLB2	5005 A086h	5009 A086h	500D A086h
8Eh	16	EPWM_AQSFRC	5005 A08Eh	5009 A08Eh	500D A08Eh
92h	16	EPWM_AQCSFRC	5005 A092h	5009 A092h	500D A092h
A0h	16	EPWM_DBREDHR	5005 A0A0h	5009 A0A0h	500D A0A0h
A2h	16	EPWM_DBRED	5005 A0A2h	5009 A0A2h	500D A0A2h
A4h	16	EPWM_DBFEDHR	5005 A0A4h	5009 A0A4h	500D A0A4h
A6h	16	EPWM_DBFED	5005 A0A6h	5009 A0A6h	500D A0A6h
C0h	32	EPWM_TBPHS	5005 A0C0h	5009 A0C0h	500D A0C0h
C4h	16	EPWM_TBPRDHR	5005 A0C4h	5009 A0C4h	500D A0C4h
C6h	16	EPWM_TBPRD	5005 A0C6h	5009 A0C6h	500D A0C6h
C8h	16	EPWM_TBPRDHRB	5005 A0C8h	5009 A0C8h	500D A0C8h
D4h	32	EPWM_CMPA	5005 A0D4h	5009 A0D4h	500D A0D4h
D8h	32	EPWM_CMPB	5005 A0D8h	5009 A0D8h	500D A0D8h
DEh	16	EPWM_CMPC	5005 A0DEh	5009 A0DEh	500D A0DEh
E2h	16	EPWM_CMPD	5005 A0E2h	5009 A0E2h	500D A0E2h
E8h	16	EPWM_GLDCTL2	5005 A0E8h	5009 A0E8h	500D A0E8h
EEh	16	EPWM_SWVDELVAL	5005 A0EEh	5009 A0EEh	500D A0EEh
100h	16	EPWM_TZSEL	5005 A100h	5009 A100h	500D A100h
102h	16	EPWM_TZSEL2	5005 A102h	5009 A102h	500D A102h
104h	16	EPWM_TZDCSEL	5005 A104h	5009 A104h	500D A104h
108h	16	EPWM_TZCTL	5005 A108h	5009 A108h	500D A108h
10Ah	16	EPWM_TZCTL2	5005 A10Ah	5009 A10Ah	500D A10Ah
10Ch	16	EPWM_TZCTLDCA	5005 A10Ch	5009 A10Ch	500D A10Ch

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Table 3-605. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM09_G3 Physical Address	EPWM10_G3 Physical Address	EPWM11_G3 Physical Address
10Eh	16	EPWM_TZCTLDCB	5005 A10Eh	5009 A10Eh	500D A10Eh
11Ah	16	EPWM_TZEINT	5005 A11Ah	5009 A11Ah	500D A11Ah
126h	16	EPWM_TZFLG	5005 A126h	5009 A126h	500D A126h
128h	16	EPWM_TZCBCFLG	5005 A128h	5009 A128h	500D A128h
12Ah	16	EPWM_TZOSTFLG	5005 A12Ah	5009 A12Ah	500D A12Ah
12Eh	16	EPWM_TZCLR	5005 A12Eh	5009 A12Eh	500D A12Eh
130h	16	EPWM_TZCBCCLR	5005 A130h	5009 A130h	500D A130h
132h	16	EPWM_TZOSTCLR	5005 A132h	5009 A132h	500D A132h
136h	16	EPWM_TZFRC	5005 A136h	5009 A136h	500D A136h
13Ah	16	EPWM_TZTRIPOUTSEL	5005 A13Ah	5009 A13Ah	500D A13Ah
148h	16	EPWM_ETSEL	5005 A148h	5009 A148h	500D A148h
14Ch	16	EPWM_ETPS	5005 A14Ch	5009 A14Ch	500D A14Ch
150h	16	EPWM_ETFLG	5005 A150h	5009 A150h	500D A150h
154h	16	EPWM_ETCLR	5005 A154h	5009 A154h	500D A154h
158h	16	EPWM_ETFRC	5005 A158h	5009 A158h	500D A158h
15Ch	16	EPWM_ETINTPS	5005 A15Ch	5009 A15Ch	500D A15Ch
160h	16	EPWM_ETSOCPS	5005 A160h	5009 A160h	500D A160h
164h	16	EPWM_ETCNTINITCTL	5005 A164h	5009 A164h	500D A164h
168h	16	EPWM_ETCNTINIT	5005 A168h	5009 A168h	500D A168h
16Ch	16	EPWM_ETINTMIXEN	5005 A16Ch	5009 A16Ch	500D A16Ch
170h	16	EPWM_ETSOCAMIXEN	5005 A170h	5009 A170h	500D A170h
174h	16	EPWM_ETSOCBMIXEN	5005 A174h	5009 A174h	500D A174h
180h	16	EPWM_DCTRIPSEL	5005 A180h	5009 A180h	500D A180h
186h	16	EPWM_DCACTL	5005 A186h	5009 A186h	500D A186h
188h	16	EPWM_DCBCTL	5005 A188h	5009 A188h	500D A188h
18Eh	16	EPWM_DCFCTL	5005 A18Eh	5009 A18Eh	500D A18Eh
190h	16	EPWM_DCCAPCTL	5005 A190h	5009 A190h	500D A190h
192h	16	EPWM_DCFOFFSET	5005 A192h	5009 A192h	500D A192h
194h	16	EPWM_DCFOFFSETCNT	5005 A194h	5009 A194h	500D A194h
196h	16	EPWM_DCFWINDOW	5005 A196h	5009 A196h	500D A196h
198h	16	EPWM_DCFWINDOWCNT	5005 A198h	5009 A198h	500D A198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5005 A19Ah	5009 A19Ah	500D A19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5005 A19Ch	5009 A19Ch	500D A19Ch
19Eh	16	EPWM_DCCAP	5005 A19Eh	5009 A19Eh	500D A19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5005 A1A4h	5009 A1A4h	500D A1A4h
1A6h	16	EPWM_DCALTRIPSEL	5005 A1A6h	5009 A1A6h	500D A1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5005 A1A8h	5009 A1A8h	500D A1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5005 A1AAh	5009 A1AAh	500D A1AAh
1ACh	16	EPWM_CAPCTL	5005 A1ACh	5009 A1ACh	500D A1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5005 A1AEh	5009 A1AEh	500D A1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5005 A1B0h	5009 A1B0h	500D A1B0h
1B2h	16	EPWM_CAPTRIPSEL	5005 A1B2h	5009 A1B2h	500D A1B2h
1F4h	32	EPWM_EPWMLOCK	5005 A1F4h	5009 A1F4h	500D A1F4h
1FAh	16	EPWM_HWVDELVAL	5005 A1FAh	5009 A1FAh	500D A1FAh
1FCh	16	EPWM_VCNTVAL	5005 A1FCh	5009 A1FCh	500D A1FCh
400h	32	EPWM_XCMPCTL1	5005 A400h	5009 A400h	500D A400h

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Table 3-605. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM09_G3 Physical Address	EPWM10_G3 Physical Address	EPWM11_G3 Physical Address
410h	32	EPWM_XLOADCTL	5005 A410h	5009 A410h	500D A410h
418h	32	EPWM_XLOAD	5005 A418h	5009 A418h	500D A418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5005 A41Ch	5009 A41Ch	500D A41Ch
420h	32	EPWM_XREGSHDW1STS	5005 A420h	5009 A420h	500D A420h
428h	32	EPWM_XREGSHDW2STS	5005 A428h	5009 A428h	500D A428h
430h	32	EPWM_XREGSHDW3STS	5005 A430h	5009 A430h	500D A430h
600h	32	EPWM_XCMP1_ACTIVE	5005 A600h	5009 A600h	500D A600h
604h	32	EPWM_XCMP2_ACTIVE	5005 A604h	5009 A604h	500D A604h
608h	32	EPWM_XCMP3_ACTIVE	5005 A608h	5009 A608h	500D A608h
60Ch	32	EPWM_XCMP4_ACTIVE	5005 A60Ch	5009 A60Ch	500D A60Ch
610h	32	EPWM_XCMP5_ACTIVE	5005 A610h	5009 A610h	500D A610h
614h	32	EPWM_XCMP6_ACTIVE	5005 A614h	5009 A614h	500D A614h
618h	32	EPWM_XCMP7_ACTIVE	5005 A618h	5009 A618h	500D A618h
61Ch	32	EPWM_XCMP8_ACTIVE	5005 A61Ch	5009 A61Ch	500D A61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5005 A620h	5009 A620h	500D A620h
630h	16	EPWM_XAQCTLA_ACTIVE	5005 A630h	5009 A630h	500D A630h
644h	32	EPWM_XMINMAX_ACTIVE	5005 A644h	5009 A644h	500D A644h
680h	32	EPWM_XCMP1_SHDW1	5005 A680h	5009 A680h	500D A680h
684h	32	EPWM_XCMP2_SHDW1	5005 A684h	5009 A684h	500D A684h
688h	32	EPWM_XCMP3_SHDW1	5005 A688h	5009 A688h	500D A688h
68Ch	32	EPWM_XCMP4_SHDW1	5005 A68Ch	5009 A68Ch	500D A68Ch
690h	32	EPWM_XCMP5_SHDW1	5005 A690h	5009 A690h	500D A690h
694h	32	EPWM_XCMP6_SHDW1	5005 A694h	5009 A694h	500D A694h
698h	32	EPWM_XCMP7_SHDW1	5005 A698h	5009 A698h	500D A698h
69Ch	32	EPWM_XCMP8_SHDW1	5005 A69Ch	5009 A69Ch	500D A69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5005 A6A0h	5009 A6A0h	500D A6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5005 A6B0h	5009 A6B0h	500D A6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5005 A6B2h	5009 A6B2h	500D A6B2h
6BAh	16	EPWM_CMPC_SHDW1	5005 A6BAh	5009 A6BAh	500D A6BAh
6BEh	16	EPWM_CMPD_SHDW1	5005 A6BEh	5009 A6BEh	500D A6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5005 A6C4h	5009 A6C4h	500D A6C4h
700h	32	EPWM_XCMP1_SHDW2	5005 A700h	5009 A700h	500D A700h
704h	32	EPWM_XCMP2_SHDW2	5005 A704h	5009 A704h	500D A704h
708h	32	EPWM_XCMP3_SHDW2	5005 A708h	5009 A708h	500D A708h
70Ch	32	EPWM_XCMP4_SHDW2	5005 A70Ch	5009 A70Ch	500D A70Ch
710h	32	EPWM_XCMP5_SHDW2	5005 A710h	5009 A710h	500D A710h
714h	32	EPWM_XCMP6_SHDW2	5005 A714h	5009 A714h	500D A714h
718h	32	EPWM_XCMP7_SHDW2	5005 A718h	5009 A718h	500D A718h
71Ch	32	EPWM_XCMP8_SHDW2	5005 A71Ch	5009 A71Ch	500D A71Ch
720h	32	EPWM_XTBPRD_SHDW2	5005 A720h	5009 A720h	500D A720h
730h	16	EPWM_XAQCTLA_SHDW2	5005 A730h	5009 A730h	500D A730h
732h	16	EPWM_XAQCTLB_SHDW2	5005 A732h	5009 A732h	500D A732h
73Ah	16	EPWM_CMPC_SHDW2	5005 A73Ah	5009 A73Ah	500D A73Ah
73Eh	16	EPWM_CMPD_SHDW2	5005 A73Eh	5009 A73Eh	500D A73Eh
744h	32	EPWM_XMINMAX_SHDW2	5005 A744h	5009 A744h	500D A744h
780h	32	EPWM_XCMP1_SHDW3	5005 A780h	5009 A780h	500D A780h

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Table 3-605. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM09_G3 Physical Address	EPWM10_G3 Physical Address	EPWM11_G3 Physical Address
784h	32	EPWM_XCMP2_SHDW3	5005 A784h	5009 A784h	500D A784h
788h	32	EPWM_XCMP3_SHDW3	5005 A788h	5009 A788h	500D A788h
78Ch	32	EPWM_XCMP4_SHDW3	5005 A78Ch	5009 A78Ch	500D A78Ch
790h	32	EPWM_XCMP5_SHDW3	5005 A790h	5009 A790h	500D A790h
794h	32	EPWM_XCMP6_SHDW3	5005 A794h	5009 A794h	500D A794h
798h	32	EPWM_XCMP7_SHDW3	5005 A798h	5009 A798h	500D A798h
79Ch	32	EPWM_XCMP8_SHDW3	5005 A79Ch	5009 A79Ch	500D A79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5005 A7A0h	5009 A7A0h	500D A7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5005 A7B0h	5009 A7B0h	500D A7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5005 A7B2h	5009 A7B2h	500D A7B2h
7BAh	16	EPWM_CMPC_SHDW3	5005 A7BAh	5009 A7BAh	500D A7BAh
7BEh	16	EPWM_CMPD_SHDW3	5005 A7BEh	5009 A7BEh	500D A7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5005 A7C4h	5009 A7C4h	500D A7C4h
800h	32	EPWM_DECTL	5005 A800h	5009 A800h	500D A800h
804h	32	EPWM_DECOMPSEL	5005 A804h	5009 A804h	500D A804h
808h	32	EPWM_DEACTCTL	5005 A808h	5009 A808h	500D A808h
80Ch	32	EPWM_DESTS	5005 A80Ch	5009 A80Ch	500D A80Ch
810h	32	EPWM_DEFRC	5005 A810h	5009 A810h	500D A810h
814h	32	EPWM_DECLR	5005 A814h	5009 A814h	500D A814h
820h	32	EPWM_DEMONCNT	5005 A820h	5009 A820h	500D A820h
824h	32	EPWM_DEMONCTL	5005 A824h	5009 A824h	500D A824h
828h	32	EPWM_DEMONSTEP	5005 A828h	5009 A828h	500D A828h
82Ch	32	EPWM_DEMONTHRES	5005 A82Ch	5009 A82Ch	500D A82Ch
C00h	32	EPWM_MINDBCFG	5005 AC00h	5009 AC00h	500D AC00h
C04h	32	EPWM_MINDBDLY	5005 AC04h	5009 AC04h	500D AC04h
C20h	32	EPWM_LUTCTLA	5005 AC20h	5009 AC20h	500D AC20h
C24h	32	EPWM_LUTCTLB	5005 AC24h	5009 AC24h	500D AC24h

Table 3-606. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM12_G3 Physical Address	EPWM13_G3 Physical Address	EPWM14_G3 Physical Address
0h	16	EPWM_TBCTL	5001 B000h	5005 B000h	5009 B000h
2h	16	EPWM_TBCTL2	5001 B002h	5005 B002h	5009 B002h
6h	16	EPWM_EPWMSYNCINSEL	5001 B006h	5005 B006h	5009 B006h
8h	16	EPWM_TBCTR	5001 B008h	5005 B008h	5009 B008h
Ah	16	EPWM_TBSTS	5001 B00Ah	5005 B00Ah	5009 B00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5001 B00Ch	5005 B00Ch	5009 B00Ch
Eh	16	EPWM_TBCTL3	5001 B00Eh	5005 B00Eh	5009 B00Eh
10h	16	EPWM_CMPCTL	5001 B010h	5005 B010h	5009 B010h
12h	16	EPWM_CMPCTL2	5001 B012h	5005 B012h	5009 B012h
18h	16	EPWM_DBCTL	5001 B018h	5005 B018h	5009 B018h
1Ah	16	EPWM_DBCTL2	5001 B01Ah	5005 B01Ah	5009 B01Ah
20h	16	EPWM_AQCTL	5001 B020h	5005 B020h	5009 B020h
22h	16	EPWM_AQTSRCSEL	5001 B022h	5005 B022h	5009 B022h
28h	16	EPWM_PCCTL	5001 B028h	5005 B028h	5009 B028h
30h	16	EPWM_VCAPCTL	5001 B030h	5005 B030h	5009 B030h

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Table 3-606. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM12_G3 Physical Address	EPWM13_G3 Physical Address	EPWM14_G3 Physical Address
32h	16	EPWM_VCNTCFG	5001 B032h	5005 B032h	5009 B032h
40h	16	EPWM_HRCNFG	5001 B040h	5005 B040h	5009 B040h
4Eh	16	EPWM_HRCNFG2	5001 B04Eh	5005 B04Eh	5009 B04Eh
5Ah	16	EPWM_HRPCTL	5001 B05Ah	5005 B05Ah	5009 B05Ah
5Ch	16	EPWM_TRREM	5001 B05Ch	5005 B05Ch	5009 B05Ch
68h	16	EPWM_GLDCTL	5001 B068h	5005 B068h	5009 B068h
6Ah	16	EPWM_GLDCFG	5001 B06Ah	5005 B06Ah	5009 B06Ah
70h	32	EPWM_EPWMXLINK	5001 B070h	5005 B070h	5009 B070h
74h	32	EPWM_EPWMXLINK2	5001 B074h	5005 B074h	5009 B074h
7Ah	16	EPWM_ETEST	5001 B07Ah	5005 B07Ah	5009 B07Ah
7Ch	16	EPWM_EPWMREV	5001 B07Ch	5005 B07Ch	5009 B07Ch
7Eh	16	EPWM_HRPWMREV	5001 B07Eh	5005 B07Eh	5009 B07Eh
80h	16	EPWM_AQCTLA	5001 B080h	5005 B080h	5009 B080h
82h	16	EPWM_AQCTLA2	5001 B082h	5005 B082h	5009 B082h
84h	16	EPWM_AQCTLB	5001 B084h	5005 B084h	5009 B084h
86h	16	EPWM_AQCTLB2	5001 B086h	5005 B086h	5009 B086h
8Eh	16	EPWM_AQSFRC	5001 B08Eh	5005 B08Eh	5009 B08Eh
92h	16	EPWM_AQCSFRC	5001 B092h	5005 B092h	5009 B092h
A0h	16	EPWM_DBREDHR	5001 B0A0h	5005 B0A0h	5009 B0A0h
A2h	16	EPWM_DBRED	5001 B0A2h	5005 B0A2h	5009 B0A2h
A4h	16	EPWM_DBFEDHR	5001 B0A4h	5005 B0A4h	5009 B0A4h
A6h	16	EPWM_DBFED	5001 B0A6h	5005 B0A6h	5009 B0A6h
C0h	32	EPWM_TBPHS	5001 B0C0h	5005 B0C0h	5009 B0C0h
C4h	16	EPWM_TBPRDHR	5001 B0C4h	5005 B0C4h	5009 B0C4h
C6h	16	EPWM_TBPRD	5001 B0C6h	5005 B0C6h	5009 B0C6h
C8h	16	EPWM_TBPRDHRB	5001 B0C8h	5005 B0C8h	5009 B0C8h
D4h	32	EPWM_CMPA	5001 B0D4h	5005 B0D4h	5009 B0D4h
D8h	32	EPWM_CMPB	5001 B0D8h	5005 B0D8h	5009 B0D8h
DEh	16	EPWM_CMPC	5001 B0DEh	5005 B0DEh	5009 B0DEh
E2h	16	EPWM_CMPD	5001 B0E2h	5005 B0E2h	5009 B0E2h
E8h	16	EPWM_GLDCTL2	5001 B0E8h	5005 B0E8h	5009 B0E8h
EEh	16	EPWM_SWVDELVAL	5001 B0EEh	5005 B0EEh	5009 B0EEh
100h	16	EPWM_TZSEL	5001 B100h	5005 B100h	5009 B100h
102h	16	EPWM_TZSEL2	5001 B102h	5005 B102h	5009 B102h
104h	16	EPWM_TZDCSEL	5001 B104h	5005 B104h	5009 B104h
108h	16	EPWM_TZCTL	5001 B108h	5005 B108h	5009 B108h
10Ah	16	EPWM_TZCTL2	5001 B10Ah	5005 B10Ah	5009 B10Ah
10Ch	16	EPWM_TZCTLDCA	5001 B10Ch	5005 B10Ch	5009 B10Ch
10Eh	16	EPWM_TZCTLDCB	5001 B10Eh	5005 B10Eh	5009 B10Eh
11Ah	16	EPWM_TZEINT	5001 B11Ah	5005 B11Ah	5009 B11Ah
126h	16	EPWM_TZFLG	5001 B126h	5005 B126h	5009 B126h
128h	16	EPWM_TZCBCFLG	5001 B128h	5005 B128h	5009 B128h
12Ah	16	EPWM_TZOSTFLG	5001 B12Ah	5005 B12Ah	5009 B12Ah
12Eh	16	EPWM_TZCLR	5001 B12Eh	5005 B12Eh	5009 B12Eh
130h	16	EPWM_TZCBCCLR	5001 B130h	5005 B130h	5009 B130h
132h	16	EPWM_TZOSTCLR	5001 B132h	5005 B132h	5009 B132h

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Table 3-606. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM12_G3 Physical Address	EPWM13_G3 Physical Address	EPWM14_G3 Physical Address
136h	16	EPWM_TZFRC	5001 B136h	5005 B136h	5009 B136h
13Ah	16	EPWM_TZTRIPOUTSEL	5001 B13Ah	5005 B13Ah	5009 B13Ah
148h	16	EPWM_ETSEL	5001 B148h	5005 B148h	5009 B148h
14Ch	16	EPWM_ETPS	5001 B14Ch	5005 B14Ch	5009 B14Ch
150h	16	EPWM_ETFLG	5001 B150h	5005 B150h	5009 B150h
154h	16	EPWM_ETCLR	5001 B154h	5005 B154h	5009 B154h
158h	16	EPWM_ETFRC	5001 B158h	5005 B158h	5009 B158h
15Ch	16	EPWM_ETINTPS	5001 B15Ch	5005 B15Ch	5009 B15Ch
160h	16	EPWM_ETSOCPS	5001 B160h	5005 B160h	5009 B160h
164h	16	EPWM_ETCNTINITCTL	5001 B164h	5005 B164h	5009 B164h
168h	16	EPWM_ETCNTINIT	5001 B168h	5005 B168h	5009 B168h
16Ch	16	EPWM_ETINTMIXEN	5001 B16Ch	5005 B16Ch	5009 B16Ch
170h	16	EPWM_ETSOCAMIXEN	5001 B170h	5005 B170h	5009 B170h
174h	16	EPWM_ETSOCBMIXEN	5001 B174h	5005 B174h	5009 B174h
180h	16	EPWM_DCTRIPSEL	5001 B180h	5005 B180h	5009 B180h
186h	16	EPWM_DCACTL	5001 B186h	5005 B186h	5009 B186h
188h	16	EPWM_DCBCTL	5001 B188h	5005 B188h	5009 B188h
18Eh	16	EPWM_DCFCTL	5001 B18Eh	5005 B18Eh	5009 B18Eh
190h	16	EPWM_DCCAPCTL	5001 B190h	5005 B190h	5009 B190h
192h	16	EPWM_DCFOFFSET	5001 B192h	5005 B192h	5009 B192h
194h	16	EPWM_DCFOFFSETCNT	5001 B194h	5005 B194h	5009 B194h
196h	16	EPWM_DCFWINDOW	5001 B196h	5005 B196h	5009 B196h
198h	16	EPWM_DCFWINDOWCNT	5001 B198h	5005 B198h	5009 B198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5001 B19Ah	5005 B19Ah	5009 B19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5001 B19Ch	5005 B19Ch	5009 B19Ch
19Eh	16	EPWM_DCCAP	5001 B19Eh	5005 B19Eh	5009 B19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5001 B1A4h	5005 B1A4h	5009 B1A4h
1A6h	16	EPWM_DCALTRIPSEL	5001 B1A6h	5005 B1A6h	5009 B1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5001 B1A8h	5005 B1A8h	5009 B1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5001 B1AAh	5005 B1AAh	5009 B1AAh
1ACh	16	EPWM_CAPCTL	5001 B1ACh	5005 B1ACh	5009 B1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5001 B1AEh	5005 B1AEh	5009 B1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5001 B1B0h	5005 B1B0h	5009 B1B0h
1B2h	16	EPWM_CAPTRIPSEL	5001 B1B2h	5005 B1B2h	5009 B1B2h
1F4h	32	EPWM_EPWMLOCK	5001 B1F4h	5005 B1F4h	5009 B1F4h
1FAh	16	EPWM_HWVDELVAL	5001 B1FAh	5005 B1FAh	5009 B1FAh
1FCh	16	EPWM_VCNTVAL	5001 B1FCh	5005 B1FCh	5009 B1FCh
400h	32	EPWM_XCMPCTL1	5001 B400h	5005 B400h	5009 B400h
410h	32	EPWM_XLOADCTL	5001 B410h	5005 B410h	5009 B410h
418h	32	EPWM_XLOAD	5001 B418h	5005 B418h	5009 B418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5001 B41Ch	5005 B41Ch	5009 B41Ch
420h	32	EPWM_XREGSHDW1STS	5001 B420h	5005 B420h	5009 B420h
428h	32	EPWM_XREGSHDW2STS	5001 B428h	5005 B428h	5009 B428h
430h	32	EPWM_XREGSHDW3STS	5001 B430h	5005 B430h	5009 B430h
600h	32	EPWM_XCMP1_ACTIVE	5001 B600h	5005 B600h	5009 B600h
604h	32	EPWM_XCMP2_ACTIVE	5001 B604h	5005 B604h	5009 B604h

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Table 3-606. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM12_G3 Physical Address	EPWM13_G3 Physical Address	EPWM14_G3 Physical Address
608h	32	EPWM_XCMP3_ACTIVE	5001 B608h	5005 B608h	5009 B608h
60Ch	32	EPWM_XCMP4_ACTIVE	5001 B60Ch	5005 B60Ch	5009 B60Ch
610h	32	EPWM_XCMP5_ACTIVE	5001 B610h	5005 B610h	5009 B610h
614h	32	EPWM_XCMP6_ACTIVE	5001 B614h	5005 B614h	5009 B614h
618h	32	EPWM_XCMP7_ACTIVE	5001 B618h	5005 B618h	5009 B618h
61Ch	32	EPWM_XCMP8_ACTIVE	5001 B61Ch	5005 B61Ch	5009 B61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5001 B620h	5005 B620h	5009 B620h
630h	16	EPWM_XAQCTLA_ACTIVE	5001 B630h	5005 B630h	5009 B630h
644h	32	EPWM_XMINMAX_ACTIVE	5001 B644h	5005 B644h	5009 B644h
680h	32	EPWM_XCMP1_SHDW1	5001 B680h	5005 B680h	5009 B680h
684h	32	EPWM_XCMP2_SHDW1	5001 B684h	5005 B684h	5009 B684h
688h	32	EPWM_XCMP3_SHDW1	5001 B688h	5005 B688h	5009 B688h
68Ch	32	EPWM_XCMP4_SHDW1	5001 B68Ch	5005 B68Ch	5009 B68Ch
690h	32	EPWM_XCMP5_SHDW1	5001 B690h	5005 B690h	5009 B690h
694h	32	EPWM_XCMP6_SHDW1	5001 B694h	5005 B694h	5009 B694h
698h	32	EPWM_XCMP7_SHDW1	5001 B698h	5005 B698h	5009 B698h
69Ch	32	EPWM_XCMP8_SHDW1	5001 B69Ch	5005 B69Ch	5009 B69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5001 B6A0h	5005 B6A0h	5009 B6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5001 B6B0h	5005 B6B0h	5009 B6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5001 B6B2h	5005 B6B2h	5009 B6B2h
6BAh	16	EPWM_CMPC_SHDW1	5001 B6BAh	5005 B6BAh	5009 B6BAh
6BEh	16	EPWM_CMPD_SHDW1	5001 B6BEh	5005 B6BEh	5009 B6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5001 B6C4h	5005 B6C4h	5009 B6C4h
700h	32	EPWM_XCMP1_SHDW2	5001 B700h	5005 B700h	5009 B700h
704h	32	EPWM_XCMP2_SHDW2	5001 B704h	5005 B704h	5009 B704h
708h	32	EPWM_XCMP3_SHDW2	5001 B708h	5005 B708h	5009 B708h
70Ch	32	EPWM_XCMP4_SHDW2	5001 B70Ch	5005 B70Ch	5009 B70Ch
710h	32	EPWM_XCMP5_SHDW2	5001 B710h	5005 B710h	5009 B710h
714h	32	EPWM_XCMP6_SHDW2	5001 B714h	5005 B714h	5009 B714h
718h	32	EPWM_XCMP7_SHDW2	5001 B718h	5005 B718h	5009 B718h
71Ch	32	EPWM_XCMP8_SHDW2	5001 B71Ch	5005 B71Ch	5009 B71Ch
720h	32	EPWM_XTBPRD_SHDW2	5001 B720h	5005 B720h	5009 B720h
730h	16	EPWM_XAQCTLA_SHDW2	5001 B730h	5005 B730h	5009 B730h
732h	16	EPWM_XAQCTLB_SHDW2	5001 B732h	5005 B732h	5009 B732h
73Ah	16	EPWM_CMPC_SHDW2	5001 B73Ah	5005 B73Ah	5009 B73Ah
73Eh	16	EPWM_CMPD_SHDW2	5001 B73Eh	5005 B73Eh	5009 B73Eh
744h	32	EPWM_XMINMAX_SHDW2	5001 B744h	5005 B744h	5009 B744h
780h	32	EPWM_XCMP1_SHDW3	5001 B780h	5005 B780h	5009 B780h
784h	32	EPWM_XCMP2_SHDW3	5001 B784h	5005 B784h	5009 B784h
788h	32	EPWM_XCMP3_SHDW3	5001 B788h	5005 B788h	5009 B788h
78Ch	32	EPWM_XCMP4_SHDW3	5001 B78Ch	5005 B78Ch	5009 B78Ch
790h	32	EPWM_XCMP5_SHDW3	5001 B790h	5005 B790h	5009 B790h
794h	32	EPWM_XCMP6_SHDW3	5001 B794h	5005 B794h	5009 B794h
798h	32	EPWM_XCMP7_SHDW3	5001 B798h	5005 B798h	5009 B798h
79Ch	32	EPWM_XCMP8_SHDW3	5001 B79Ch	5005 B79Ch	5009 B79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5001 B7A0h	5005 B7A0h	5009 B7A0h

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Table 3-606. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM12_G3 Physical Address	EPWM13_G3 Physical Address	EPWM14_G3 Physical Address
7B0h	16	EPWM_XAQCTLA_SHDW3	5001 B7B0h	5005 B7B0h	5009 B7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5001 B7B2h	5005 B7B2h	5009 B7B2h
7BAh	16	EPWM_CMPC_SHDW3	5001 B7BAh	5005 B7BAh	5009 B7BAh
7BEh	16	EPWM_CMPD_SHDW3	5001 B7BEh	5005 B7BEh	5009 B7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5001 B7C4h	5005 B7C4h	5009 B7C4h
800h	32	EPWM_DECTL	5001 B800h	5005 B800h	5009 B800h
804h	32	EPWM_DECOMPSEL	5001 B804h	5005 B804h	5009 B804h
808h	32	EPWM_DEACTCTL	5001 B808h	5005 B808h	5009 B808h
80Ch	32	EPWM_DESTS	5001 B80Ch	5005 B80Ch	5009 B80Ch
810h	32	EPWM_DEFRC	5001 B810h	5005 B810h	5009 B810h
814h	32	EPWM_DECLR	5001 B814h	5005 B814h	5009 B814h
820h	32	EPWM_DEMONCNT	5001 B820h	5005 B820h	5009 B820h
824h	32	EPWM_DEMONCTL	5001 B824h	5005 B824h	5009 B824h
828h	32	EPWM_DEMONSTEP	5001 B828h	5005 B828h	5009 B828h
82Ch	32	EPWM_DEMONTHRES	5001 B82Ch	5005 B82Ch	5009 B82Ch
C00h	32	EPWM_MINDBCFG	5001 BC00h	5005 BC00h	5009 BC00h
C04h	32	EPWM_MINDBDLY	5001 BC04h	5005 BC04h	5009 BC04h
C20h	32	EPWM_LUTCTLA	5001 BC20h	5005 BC20h	5009 BC20h
C24h	32	EPWM_LUTCTLB	5001 BC24h	5005 BC24h	5009 BC24h

Table 3-607. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM15_G3 Physical Address	EPWM16_G3 Physical Address	EPWM17_G3 Physical Address
0h	16	EPWM_TBCTL	500D B000h	5001 C000h	5005 C000h
2h	16	EPWM_TBCTL2	500D B002h	5001 C002h	5005 C002h
6h	16	EPWM_EPWMSYNCINSEL	500D B006h	5001 C006h	5005 C006h
8h	16	EPWM_TBCTR	500D B008h	5001 C008h	5005 C008h
Ah	16	EPWM_TBSTS	500D B00Ah	5001 C00Ah	5005 C00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500D B00Ch	5001 C00Ch	5005 C00Ch
Eh	16	EPWM_TBCTL3	500D B00Eh	5001 C00Eh	5005 C00Eh
10h	16	EPWM_CMPCTL	500D B010h	5001 C010h	5005 C010h
12h	16	EPWM_CMPCTL2	500D B012h	5001 C012h	5005 C012h
18h	16	EPWM_DBCTL	500D B018h	5001 C018h	5005 C018h
1Ah	16	EPWM_DBCTL2	500D B01Ah	5001 C01Ah	5005 C01Ah
20h	16	EPWM_AQCTL	500D B020h	5001 C020h	5005 C020h
22h	16	EPWM_AQTSRCSEL	500D B022h	5001 C022h	5005 C022h
28h	16	EPWM_PCCTL	500D B028h	5001 C028h	5005 C028h
30h	16	EPWM_VCAPCTL	500D B030h	5001 C030h	5005 C030h
32h	16	EPWM_VCNTCFG	500D B032h	5001 C032h	5005 C032h
40h	16	EPWM_HRCNFG	500D B040h	5001 C040h	5005 C040h
4Eh	16	EPWM_HRCNFG2	500D B04Eh	5001 C04Eh	5005 C04Eh
5Ah	16	EPWM_HRPCTL	500D B05Ah	5001 C05Ah	5005 C05Ah
5Ch	16	EPWM_TRREM	500D B05Ch	5001 C05Ch	5005 C05Ch
68h	16	EPWM_GLDCTL	500D B068h	5001 C068h	5005 C068h
6Ah	16	EPWM_GLDCFG	500D B06Ah	5001 C06Ah	5005 C06Ah
70h	32	EPWM_EPWMXLINK	500D B070h	5001 C070h	5005 C070h

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Table 3-607. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM15_G3 Physical Address	EPWM16_G3 Physical Address	EPWM17_G3 Physical Address
74h	32	EPWM_EPWMXLINK2	500D B074h	5001 C074h	5005 C074h
7Ah	16	EPWM_ETEST	500D B07Ah	5001 C07Ah	5005 C07Ah
7Ch	16	EPWM_EPWMREV	500D B07Ch	5001 C07Ch	5005 C07Ch
7Eh	16	EPWM_HRPWMREV	500D B07Eh	5001 C07Eh	5005 C07Eh
80h	16	EPWM_AQCTLA	500D B080h	5001 C080h	5005 C080h
82h	16	EPWM_AQCTLA2	500D B082h	5001 C082h	5005 C082h
84h	16	EPWM_AQCTLB	500D B084h	5001 C084h	5005 C084h
86h	16	EPWM_AQCTLB2	500D B086h	5001 C086h	5005 C086h
8Eh	16	EPWM_AQSFRC	500D B08Eh	5001 C08Eh	5005 C08Eh
92h	16	EPWM_AQCSFRC	500D B092h	5001 C092h	5005 C092h
A0h	16	EPWM_DBREDHR	500D B0A0h	5001 C0A0h	5005 C0A0h
A2h	16	EPWM_DBRED	500D B0A2h	5001 C0A2h	5005 C0A2h
A4h	16	EPWM_DBFEDHR	500D B0A4h	5001 C0A4h	5005 C0A4h
A6h	16	EPWM_DBFED	500D B0A6h	5001 C0A6h	5005 C0A6h
C0h	32	EPWM_TBPHS	500D B0C0h	5001 C0C0h	5005 C0C0h
C4h	16	EPWM_TBPRDHR	500D B0C4h	5001 C0C4h	5005 C0C4h
C6h	16	EPWM_TBPRD	500D B0C6h	5001 C0C6h	5005 C0C6h
C8h	16	EPWM_TBPRDHRB	500D B0C8h	5001 C0C8h	5005 C0C8h
D4h	32	EPWM_CMPA	500D B0D4h	5001 C0D4h	5005 C0D4h
D8h	32	EPWM_CMPB	500D B0D8h	5001 C0D8h	5005 C0D8h
DEh	16	EPWM_CMPC	500D B0DEh	5001 C0DEh	5005 C0DEh
E2h	16	EPWM_CMPD	500D B0E2h	5001 C0E2h	5005 C0E2h
E8h	16	EPWM_GLDCTL2	500D B0E8h	5001 C0E8h	5005 C0E8h
EEh	16	EPWM_SWVDELVAL	500D B0EEh	5001 C0EEh	5005 C0EEh
100h	16	EPWM_TZSEL	500D B100h	5001 C100h	5005 C100h
102h	16	EPWM_TZSEL2	500D B102h	5001 C102h	5005 C102h
104h	16	EPWM_TZDCSEL	500D B104h	5001 C104h	5005 C104h
108h	16	EPWM_TZCTL	500D B108h	5001 C108h	5005 C108h
10Ah	16	EPWM_TZCTL2	500D B10Ah	5001 C10Ah	5005 C10Ah
10Ch	16	EPWM_TZCTLDCA	500D B10Ch	5001 C10Ch	5005 C10Ch
10Eh	16	EPWM_TZCTLDCB	500D B10Eh	5001 C10Eh	5005 C10Eh
11Ah	16	EPWM_TZEINT	500D B11Ah	5001 C11Ah	5005 C11Ah
126h	16	EPWM_TZFLG	500D B126h	5001 C126h	5005 C126h
128h	16	EPWM_TZCBCFLG	500D B128h	5001 C128h	5005 C128h
12Ah	16	EPWM_TZOSTFLG	500D B12Ah	5001 C12Ah	5005 C12Ah
12Eh	16	EPWM_TZCLR	500D B12Eh	5001 C12Eh	5005 C12Eh
130h	16	EPWM_TZCBCCLR	500D B130h	5001 C130h	5005 C130h
132h	16	EPWM_TZOSTCLR	500D B132h	5001 C132h	5005 C132h
136h	16	EPWM_TZFRC	500D B136h	5001 C136h	5005 C136h
13Ah	16	EPWM_TZTRIPOUTSEL	500D B13Ah	5001 C13Ah	5005 C13Ah
148h	16	EPWM_ETSEL	500D B148h	5001 C148h	5005 C148h
14Ch	16	EPWM_ETPS	500D B14Ch	5001 C14Ch	5005 C14Ch
150h	16	EPWM_ETFLG	500D B150h	5001 C150h	5005 C150h
154h	16	EPWM_ETCLR	500D B154h	5001 C154h	5005 C154h
158h	16	EPWM_ETFRC	500D B158h	5001 C158h	5005 C158h
15Ch	16	EPWM_ETINTPS	500D B15Ch	5001 C15Ch	5005 C15Ch

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Table 3-607. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM15_G3 Physical Address	EPWM16_G3 Physical Address	EPWM17_G3 Physical Address
160h	16	EPWM_ETSOCPS	500D B160h	5001 C160h	5005 C160h
164h	16	EPWM_ETCNTINITCTL	500D B164h	5001 C164h	5005 C164h
168h	16	EPWM_ETCNTINIT	500D B168h	5001 C168h	5005 C168h
16Ch	16	EPWM_ETINTMIXEN	500D B16Ch	5001 C16Ch	5005 C16Ch
170h	16	EPWM_ETSOCAMIXEN	500D B170h	5001 C170h	5005 C170h
174h	16	EPWM_ETSOCBMIXEN	500D B174h	5001 C174h	5005 C174h
180h	16	EPWM_DCTRIPSEL	500D B180h	5001 C180h	5005 C180h
186h	16	EPWM_DCACTL	500D B186h	5001 C186h	5005 C186h
188h	16	EPWM_DCBCTL	500D B188h	5001 C188h	5005 C188h
18Eh	16	EPWM_DCFCTL	500D B18Eh	5001 C18Eh	5005 C18Eh
190h	16	EPWM_DCCAPCTL	500D B190h	5001 C190h	5005 C190h
192h	16	EPWM_DCFOFFSET	500D B192h	5001 C192h	5005 C192h
194h	16	EPWM_DCFOFFSETCNT	500D B194h	5001 C194h	5005 C194h
196h	16	EPWM_DCFWINDOW	500D B196h	5001 C196h	5005 C196h
198h	16	EPWM_DCFWINDOWCNT	500D B198h	5001 C198h	5005 C198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500D B19Ah	5001 C19Ah	5005 C19Ah
19Ch	16	EPWM_DCCAPMIXSEL	500D B19Ch	5001 C19Ch	5005 C19Ch
19Eh	16	EPWM_DCCAP	500D B19Eh	5001 C19Eh	5005 C19Eh
1A4h	16	EPWM_DCAHTRIPSEL	500D B1A4h	5001 C1A4h	5005 C1A4h
1A6h	16	EPWM_DCALTRIPSEL	500D B1A6h	5001 C1A6h	5005 C1A6h
1A8h	16	EPWM_DCBHTRIPSEL	500D B1A8h	5001 C1A8h	5005 C1A8h
1AAh	16	EPWM_DCBLTRIPSEL	500D B1AAh	5001 C1AAh	5005 C1AAh
1ACh	16	EPWM_CAPCTL	500D B1ACh	5001 C1ACh	5005 C1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500D B1AEh	5001 C1AEh	5005 C1AEh
1B0h	16	EPWM_CAPINTRIPSEL	500D B1B0h	5001 C1B0h	5005 C1B0h
1B2h	16	EPWM_CAPTRIPSEL	500D B1B2h	5001 C1B2h	5005 C1B2h
1F4h	32	EPWM_EPWMLOCK	500D B1F4h	5001 C1F4h	5005 C1F4h
1FAh	16	EPWM_HWVDELVAL	500D B1FAh	5001 C1FAh	5005 C1FAh
1FCh	16	EPWM_VCNTVAL	500D B1FCh	5001 C1FCh	5005 C1FCh
400h	32	EPWM_XCMPCTL1	500D B400h	5001 C400h	5005 C400h
410h	32	EPWM_XLOADCTL	500D B410h	5001 C410h	5005 C410h
418h	32	EPWM_XLOAD	500D B418h	5001 C418h	5005 C418h
41Ch	32	EPWM_EPWMXLINKXLOAD	500D B41Ch	5001 C41Ch	5005 C41Ch
420h	32	EPWM_XREGSHDW1STS	500D B420h	5001 C420h	5005 C420h
428h	32	EPWM_XREGSHDW2STS	500D B428h	5001 C428h	5005 C428h
430h	32	EPWM_XREGSHDW3STS	500D B430h	5001 C430h	5005 C430h
600h	32	EPWM_XCMP1_ACTIVE	500D B600h	5001 C600h	5005 C600h
604h	32	EPWM_XCMP2_ACTIVE	500D B604h	5001 C604h	5005 C604h
608h	32	EPWM_XCMP3_ACTIVE	500D B608h	5001 C608h	5005 C608h
60Ch	32	EPWM_XCMP4_ACTIVE	500D B60Ch	5001 C60Ch	5005 C60Ch
610h	32	EPWM_XCMP5_ACTIVE	500D B610h	5001 C610h	5005 C610h
614h	32	EPWM_XCMP6_ACTIVE	500D B614h	5001 C614h	5005 C614h
618h	32	EPWM_XCMP7_ACTIVE	500D B618h	5001 C618h	5005 C618h
61Ch	32	EPWM_XCMP8_ACTIVE	500D B61Ch	5001 C61Ch	5005 C61Ch
620h	32	EPWM_XTBPRD_ACTIVE	500D B620h	5001 C620h	5005 C620h
630h	16	EPWM_XAQCTLA_ACTIVE	500D B630h	5001 C630h	5005 C630h

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Table 3-607. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM15_G3 Physical Address	EPWM16_G3 Physical Address	EPWM17_G3 Physical Address
644h	32	EPWM_XMINMAX_ACTIVE	500D B644h	5001 C644h	5005 C644h
680h	32	EPWM_XCMP1_SHDW1	500D B680h	5001 C680h	5005 C680h
684h	32	EPWM_XCMP2_SHDW1	500D B684h	5001 C684h	5005 C684h
688h	32	EPWM_XCMP3_SHDW1	500D B688h	5001 C688h	5005 C688h
68Ch	32	EPWM_XCMP4_SHDW1	500D B68Ch	5001 C68Ch	5005 C68Ch
690h	32	EPWM_XCMP5_SHDW1	500D B690h	5001 C690h	5005 C690h
694h	32	EPWM_XCMP6_SHDW1	500D B694h	5001 C694h	5005 C694h
698h	32	EPWM_XCMP7_SHDW1	500D B698h	5001 C698h	5005 C698h
69Ch	32	EPWM_XCMP8_SHDW1	500D B69Ch	5001 C69Ch	5005 C69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500D B6A0h	5001 C6A0h	5005 C6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500D B6B0h	5001 C6B0h	5005 C6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500D B6B2h	5001 C6B2h	5005 C6B2h
6BAh	16	EPWM_CMPC_SHDW1	500D B6BAh	5001 C6BAh	5005 C6BAh
6BEh	16	EPWM_CMPD_SHDW1	500D B6BEh	5001 C6BEh	5005 C6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500D B6C4h	5001 C6C4h	5005 C6C4h
700h	32	EPWM_XCMP1_SHDW2	500D B700h	5001 C700h	5005 C700h
704h	32	EPWM_XCMP2_SHDW2	500D B704h	5001 C704h	5005 C704h
708h	32	EPWM_XCMP3_SHDW2	500D B708h	5001 C708h	5005 C708h
70Ch	32	EPWM_XCMP4_SHDW2	500D B70Ch	5001 C70Ch	5005 C70Ch
710h	32	EPWM_XCMP5_SHDW2	500D B710h	5001 C710h	5005 C710h
714h	32	EPWM_XCMP6_SHDW2	500D B714h	5001 C714h	5005 C714h
718h	32	EPWM_XCMP7_SHDW2	500D B718h	5001 C718h	5005 C718h
71Ch	32	EPWM_XCMP8_SHDW2	500D B71Ch	5001 C71Ch	5005 C71Ch
720h	32	EPWM_XTBPRD_SHDW2	500D B720h	5001 C720h	5005 C720h
730h	16	EPWM_XAQCTLA_SHDW2	500D B730h	5001 C730h	5005 C730h
732h	16	EPWM_XAQCTLB_SHDW2	500D B732h	5001 C732h	5005 C732h
73Ah	16	EPWM_CMPC_SHDW2	500D B73Ah	5001 C73Ah	5005 C73Ah
73Eh	16	EPWM_CMPD_SHDW2	500D B73Eh	5001 C73Eh	5005 C73Eh
744h	32	EPWM_XMINMAX_SHDW2	500D B744h	5001 C744h	5005 C744h
780h	32	EPWM_XCMP1_SHDW3	500D B780h	5001 C780h	5005 C780h
784h	32	EPWM_XCMP2_SHDW3	500D B784h	5001 C784h	5005 C784h
788h	32	EPWM_XCMP3_SHDW3	500D B788h	5001 C788h	5005 C788h
78Ch	32	EPWM_XCMP4_SHDW3	500D B78Ch	5001 C78Ch	5005 C78Ch
790h	32	EPWM_XCMP5_SHDW3	500D B790h	5001 C790h	5005 C790h
794h	32	EPWM_XCMP6_SHDW3	500D B794h	5001 C794h	5005 C794h
798h	32	EPWM_XCMP7_SHDW3	500D B798h	5001 C798h	5005 C798h
79Ch	32	EPWM_XCMP8_SHDW3	500D B79Ch	5001 C79Ch	5005 C79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500D B7A0h	5001 C7A0h	5005 C7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500D B7B0h	5001 C7B0h	5005 C7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500D B7B2h	5001 C7B2h	5005 C7B2h
7BAh	16	EPWM_CMPC_SHDW3	500D B7BAh	5001 C7BAh	5005 C7BAh
7BEh	16	EPWM_CMPD_SHDW3	500D B7BEh	5001 C7BEh	5005 C7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500D B7C4h	5001 C7C4h	5005 C7C4h
800h	32	EPWM_DECTL	500D B800h	5001 C800h	5005 C800h
804h	32	EPWM_DECOMPSEL	500D B804h	5001 C804h	5005 C804h
808h	32	EPWM_DEACTCTL	500D B808h	5001 C808h	5005 C808h

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Table 3-607. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM15_G3 Physical Address	EPWM16_G3 Physical Address	EPWM17_G3 Physical Address
80Ch	32	EPWM_DESTS	500D B80Ch	5001 C80Ch	5005 C80Ch
810h	32	EPWM_DEFRC	500D B810h	5001 C810h	5005 C810h
814h	32	EPWM_DECLR	500D B814h	5001 C814h	5005 C814h
820h	32	EPWM_DEMONCNT	500D B820h	5001 C820h	5005 C820h
824h	32	EPWM_DEMONCTL	500D B824h	5001 C824h	5005 C824h
828h	32	EPWM_DEMONSTEP	500D B828h	5001 C828h	5005 C828h
82Ch	32	EPWM_DEMONTHRES	500D B82Ch	5001 C82Ch	5005 C82Ch
C00h	32	EPWM_MINDBCFG	500D BC00h	5001 CC00h	5005 CC00h
C04h	32	EPWM_MINDBDLY	500D BC04h	5001 CC04h	5005 CC04h
C20h	32	EPWM_LUTCTLA	500D BC20h	5001 CC20h	5005 CC20h
C24h	32	EPWM_LUTCTLB	500D BC24h	5001 CC24h	5005 CC24h

Table 3-608. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM18_G3 Physical Address	EPWM19_G3 Physical Address	EPWM20_G3 Physical Address
0h	16	EPWM_TBCTL	5009 C000h	500D C000h	5001 D000h
2h	16	EPWM_TBCTL2	5009 C002h	500D C002h	5001 D002h
6h	16	EPWM_EPWMSYNCINSEL	5009 C006h	500D C006h	5001 D006h
8h	16	EPWM_TBCTR	5009 C008h	500D C008h	5001 D008h
Ah	16	EPWM_TBSTS	5009 C00Ah	500D C00Ah	5001 D00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5009 C00Ch	500D C00Ch	5001 D00Ch
Eh	16	EPWM_TBCTL3	5009 C00Eh	500D C00Eh	5001 D00Eh
10h	16	EPWM_CMPCTL	5009 C010h	500D C010h	5001 D010h
12h	16	EPWM_CMPCTL2	5009 C012h	500D C012h	5001 D012h
18h	16	EPWM_DBCTL	5009 C018h	500D C018h	5001 D018h
1Ah	16	EPWM_DBCTL2	5009 C01Ah	500D C01Ah	5001 D01Ah
20h	16	EPWM_AQCTL	5009 C020h	500D C020h	5001 D020h
22h	16	EPWM_AQTSRCSEL	5009 C022h	500D C022h	5001 D022h
28h	16	EPWM_PCCTL	5009 C028h	500D C028h	5001 D028h
30h	16	EPWM_VCAPCTL	5009 C030h	500D C030h	5001 D030h
32h	16	EPWM_VCNTCFG	5009 C032h	500D C032h	5001 D032h
40h	16	EPWM_HRCNFG	5009 C040h	500D C040h	5001 D040h
4Eh	16	EPWM_HRCNFG2	5009 C04Eh	500D C04Eh	5001 D04Eh
5Ah	16	EPWM_HRPCTL	5009 C05Ah	500D C05Ah	5001 D05Ah
5Ch	16	EPWM_TRREM	5009 C05Ch	500D C05Ch	5001 D05Ch
68h	16	EPWM_GLDCTL	5009 C068h	500D C068h	5001 D068h
6Ah	16	EPWM_GLDCFG	5009 C06Ah	500D C06Ah	5001 D06Ah
70h	32	EPWM_EPWMXLINK	5009 C070h	500D C070h	5001 D070h
74h	32	EPWM_EPWMXLINK2	5009 C074h	500D C074h	5001 D074h
7Ah	16	EPWM_ETEST	5009 C07Ah	500D C07Ah	5001 D07Ah
7Ch	16	EPWM_EPWMREV	5009 C07Ch	500D C07Ch	5001 D07Ch
7Eh	16	EPWM_HRPWMREV	5009 C07Eh	500D C07Eh	5001 D07Eh
80h	16	EPWM_AQCTLA	5009 C080h	500D C080h	5001 D080h
82h	16	EPWM_AQCTLA2	5009 C082h	500D C082h	5001 D082h
84h	16	EPWM_AQCTLB	5009 C084h	500D C084h	5001 D084h
86h	16	EPWM_AQCTLB2	5009 C086h	500D C086h	5001 D086h

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Table 3-608. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM18_G3 Physical Address	EPWM19_G3 Physical Address	EPWM20_G3 Physical Address
8Eh	16	EPWM_AQSFRC	5009 C08Eh	500D C08Eh	5001 D08Eh
92h	16	EPWM_AQCSFRC	5009 C092h	500D C092h	5001 D092h
A0h	16	EPWM_DBREDHR	5009 C0A0h	500D C0A0h	5001 D0A0h
A2h	16	EPWM_DBRED	5009 C0A2h	500D C0A2h	5001 D0A2h
A4h	16	EPWM_DBFEDHR	5009 C0A4h	500D C0A4h	5001 D0A4h
A6h	16	EPWM_DBFED	5009 C0A6h	500D C0A6h	5001 D0A6h
C0h	32	EPWM_TBPHS	5009 C0C0h	500D C0C0h	5001 D0C0h
C4h	16	EPWM_TBPRDHR	5009 C0C4h	500D C0C4h	5001 D0C4h
C6h	16	EPWM_TBPRD	5009 C0C6h	500D C0C6h	5001 D0C6h
C8h	16	EPWM_TBPRDHRB	5009 C0C8h	500D C0C8h	5001 D0C8h
D4h	32	EPWM_CMPA	5009 C0D4h	500D C0D4h	5001 D0D4h
D8h	32	EPWM_CMPB	5009 C0D8h	500D C0D8h	5001 D0D8h
DEh	16	EPWM_CMPC	5009 C0DEh	500D C0DEh	5001 D0DEh
E2h	16	EPWM_CMPD	5009 C0E2h	500D C0E2h	5001 D0E2h
E8h	16	EPWM_GLDCTL2	5009 C0E8h	500D C0E8h	5001 D0E8h
EEh	16	EPWM_SWVDELVAL	5009 C0EEh	500D C0EEh	5001 D0EEh
100h	16	EPWM_TZSEL	5009 C100h	500D C100h	5001 D100h
102h	16	EPWM_TZSEL2	5009 C102h	500D C102h	5001 D102h
104h	16	EPWM_TZDCSEL	5009 C104h	500D C104h	5001 D104h
108h	16	EPWM_TZCTL	5009 C108h	500D C108h	5001 D108h
10Ah	16	EPWM_TZCTL2	5009 C10Ah	500D C10Ah	5001 D10Ah
10Ch	16	EPWM_TZCTLDCA	5009 C10Ch	500D C10Ch	5001 D10Ch
10Eh	16	EPWM_TZCTLDCB	5009 C10Eh	500D C10Eh	5001 D10Eh
11Ah	16	EPWM_TZEINT	5009 C11Ah	500D C11Ah	5001 D11Ah
126h	16	EPWM_TZFLG	5009 C126h	500D C126h	5001 D126h
128h	16	EPWM_TZCBCFLG	5009 C128h	500D C128h	5001 D128h
12Ah	16	EPWM_TZOSTFLG	5009 C12Ah	500D C12Ah	5001 D12Ah
12Eh	16	EPWM_TZCLR	5009 C12Eh	500D C12Eh	5001 D12Eh
130h	16	EPWM_TZCBCCLR	5009 C130h	500D C130h	5001 D130h
132h	16	EPWM_TZOSTCLR	5009 C132h	500D C132h	5001 D132h
136h	16	EPWM_TZFRC	5009 C136h	500D C136h	5001 D136h
13Ah	16	EPWM_TZTRIPOUTSEL	5009 C13Ah	500D C13Ah	5001 D13Ah
148h	16	EPWM_ETSEL	5009 C148h	500D C148h	5001 D148h
14Ch	16	EPWM_ETPS	5009 C14Ch	500D C14Ch	5001 D14Ch
150h	16	EPWM_ETFLG	5009 C150h	500D C150h	5001 D150h
154h	16	EPWM_ETCLR	5009 C154h	500D C154h	5001 D154h
158h	16	EPWM_ETFRC	5009 C158h	500D C158h	5001 D158h
15Ch	16	EPWM_ETINTPS	5009 C15Ch	500D C15Ch	5001 D15Ch
160h	16	EPWM_ETSOCPS	5009 C160h	500D C160h	5001 D160h
164h	16	EPWM_ETCNTINITCTL	5009 C164h	500D C164h	5001 D164h
168h	16	EPWM_ETCNTINIT	5009 C168h	500D C168h	5001 D168h
16Ch	16	EPWM_ETINTMIXEN	5009 C16Ch	500D C16Ch	5001 D16Ch
170h	16	EPWM_ETSOCAMIXEN	5009 C170h	500D C170h	5001 D170h
174h	16	EPWM_ETSOCBMIXEN	5009 C174h	500D C174h	5001 D174h
180h	16	EPWM_DCTRIPSEL	5009 C180h	500D C180h	5001 D180h
186h	16	EPWM_DCACTL	5009 C186h	500D C186h	5001 D186h

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Table 3-608. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM18_G3 Physical Address	EPWM19_G3 Physical Address	EPWM20_G3 Physical Address
188h	16	EPWM_DCBCTL	5009 C188h	500D C188h	5001 D188h
18Eh	16	EPWM_DCFCTL	5009 C18Eh	500D C18Eh	5001 D18Eh
190h	16	EPWM_DCCAPCTL	5009 C190h	500D C190h	5001 D190h
192h	16	EPWM_DCFOFFSET	5009 C192h	500D C192h	5001 D192h
194h	16	EPWM_DCFOFFSETCNT	5009 C194h	500D C194h	5001 D194h
196h	16	EPWM_DCFWINDOW	5009 C196h	500D C196h	5001 D196h
198h	16	EPWM_DCFWINDOWCNT	5009 C198h	500D C198h	5001 D198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5009 C19Ah	500D C19Ah	5001 D19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5009 C19Ch	500D C19Ch	5001 D19Ch
19Eh	16	EPWM_DCCAP	5009 C19Eh	500D C19Eh	5001 D19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5009 C1A4h	500D C1A4h	5001 D1A4h
1A6h	16	EPWM_DCALTRIPSEL	5009 C1A6h	500D C1A6h	5001 D1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5009 C1A8h	500D C1A8h	5001 D1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5009 C1AAh	500D C1AAh	5001 D1AAh
1ACh	16	EPWM_CAPCTL	5009 C1ACh	500D C1ACh	5001 D1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5009 C1AEh	500D C1AEh	5001 D1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5009 C1B0h	500D C1B0h	5001 D1B0h
1B2h	16	EPWM_CAPTRIPSEL	5009 C1B2h	500D C1B2h	5001 D1B2h
1F4h	32	EPWM_EPWMLOCK	5009 C1F4h	500D C1F4h	5001 D1F4h
1FAh	16	EPWM_HWVDELVAL	5009 C1FAh	500D C1FAh	5001 D1FAh
1FCh	16	EPWM_VCNTVAL	5009 C1FCh	500D C1FCh	5001 D1FCh
400h	32	EPWM_XCMPCTL1	5009 C400h	500D C400h	5001 D400h
410h	32	EPWM_XLOADCTL	5009 C410h	500D C410h	5001 D410h
418h	32	EPWM_XLOAD	5009 C418h	500D C418h	5001 D418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5009 C41Ch	500D C41Ch	5001 D41Ch
420h	32	EPWM_XREGSHDW1STS	5009 C420h	500D C420h	5001 D420h
428h	32	EPWM_XREGSHDW2STS	5009 C428h	500D C428h	5001 D428h
430h	32	EPWM_XREGSHDW3STS	5009 C430h	500D C430h	5001 D430h
600h	32	EPWM_XCMP1_ACTIVE	5009 C600h	500D C600h	5001 D600h
604h	32	EPWM_XCMP2_ACTIVE	5009 C604h	500D C604h	5001 D604h
608h	32	EPWM_XCMP3_ACTIVE	5009 C608h	500D C608h	5001 D608h
60Ch	32	EPWM_XCMP4_ACTIVE	5009 C60Ch	500D C60Ch	5001 D60Ch
610h	32	EPWM_XCMP5_ACTIVE	5009 C610h	500D C610h	5001 D610h
614h	32	EPWM_XCMP6_ACTIVE	5009 C614h	500D C614h	5001 D614h
618h	32	EPWM_XCMP7_ACTIVE	5009 C618h	500D C618h	5001 D618h
61Ch	32	EPWM_XCMP8_ACTIVE	5009 C61Ch	500D C61Ch	5001 D61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5009 C620h	500D C620h	5001 D620h
630h	16	EPWM_XAQCTLA_ACTIVE	5009 C630h	500D C630h	5001 D630h
644h	32	EPWM_XMINMAX_ACTIVE	5009 C644h	500D C644h	5001 D644h
680h	32	EPWM_XCMP1_SHDW1	5009 C680h	500D C680h	5001 D680h
684h	32	EPWM_XCMP2_SHDW1	5009 C684h	500D C684h	5001 D684h
688h	32	EPWM_XCMP3_SHDW1	5009 C688h	500D C688h	5001 D688h
68Ch	32	EPWM_XCMP4_SHDW1	5009 C68Ch	500D C68Ch	5001 D68Ch
690h	32	EPWM_XCMP5_SHDW1	5009 C690h	500D C690h	5001 D690h
694h	32	EPWM_XCMP6_SHDW1	5009 C694h	500D C694h	5001 D694h
698h	32	EPWM_XCMP7_SHDW1	5009 C698h	500D C698h	5001 D698h

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Table 3-608. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM18_G3 Physical Address	EPWM19_G3 Physical Address	EPWM20_G3 Physical Address
69Ch	32	EPWM_XCMP8_SHDW1	5009 C69Ch	500D C69Ch	5001 D69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5009 C6A0h	500D C6A0h	5001 D6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5009 C6B0h	500D C6B0h	5001 D6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5009 C6B2h	500D C6B2h	5001 D6B2h
6BAh	16	EPWM_CMPC_SHDW1	5009 C6BAh	500D C6BAh	5001 D6BAh
6BEh	16	EPWM_CMPD_SHDW1	5009 C6BEh	500D C6BEh	5001 D6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5009 C6C4h	500D C6C4h	5001 D6C4h
700h	32	EPWM_XCMP1_SHDW2	5009 C700h	500D C700h	5001 D700h
704h	32	EPWM_XCMP2_SHDW2	5009 C704h	500D C704h	5001 D704h
708h	32	EPWM_XCMP3_SHDW2	5009 C708h	500D C708h	5001 D708h
70Ch	32	EPWM_XCMP4_SHDW2	5009 C70Ch	500D C70Ch	5001 D70Ch
710h	32	EPWM_XCMP5_SHDW2	5009 C710h	500D C710h	5001 D710h
714h	32	EPWM_XCMP6_SHDW2	5009 C714h	500D C714h	5001 D714h
718h	32	EPWM_XCMP7_SHDW2	5009 C718h	500D C718h	5001 D718h
71Ch	32	EPWM_XCMP8_SHDW2	5009 C71Ch	500D C71Ch	5001 D71Ch
720h	32	EPWM_XTBPRD_SHDW2	5009 C720h	500D C720h	5001 D720h
730h	16	EPWM_XAQCTLA_SHDW2	5009 C730h	500D C730h	5001 D730h
732h	16	EPWM_XAQCTLB_SHDW2	5009 C732h	500D C732h	5001 D732h
73Ah	16	EPWM_CMPC_SHDW2	5009 C73Ah	500D C73Ah	5001 D73Ah
73Eh	16	EPWM_CMPD_SHDW2	5009 C73Eh	500D C73Eh	5001 D73Eh
744h	32	EPWM_XMINMAX_SHDW2	5009 C744h	500D C744h	5001 D744h
780h	32	EPWM_XCMP1_SHDW3	5009 C780h	500D C780h	5001 D780h
784h	32	EPWM_XCMP2_SHDW3	5009 C784h	500D C784h	5001 D784h
788h	32	EPWM_XCMP3_SHDW3	5009 C788h	500D C788h	5001 D788h
78Ch	32	EPWM_XCMP4_SHDW3	5009 C78Ch	500D C78Ch	5001 D78Ch
790h	32	EPWM_XCMP5_SHDW3	5009 C790h	500D C790h	5001 D790h
794h	32	EPWM_XCMP6_SHDW3	5009 C794h	500D C794h	5001 D794h
798h	32	EPWM_XCMP7_SHDW3	5009 C798h	500D C798h	5001 D798h
79Ch	32	EPWM_XCMP8_SHDW3	5009 C79Ch	500D C79Ch	5001 D79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5009 C7A0h	500D C7A0h	5001 D7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5009 C7B0h	500D C7B0h	5001 D7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5009 C7B2h	500D C7B2h	5001 D7B2h
7BAh	16	EPWM_CMPC_SHDW3	5009 C7BAh	500D C7BAh	5001 D7BAh
7BEh	16	EPWM_CMPD_SHDW3	5009 C7BEh	500D C7BEh	5001 D7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5009 C7C4h	500D C7C4h	5001 D7C4h
800h	32	EPWM_DECTL	5009 C800h	500D C800h	5001 D800h
804h	32	EPWM_DECOMPSEL	5009 C804h	500D C804h	5001 D804h
808h	32	EPWM_DEACTCTL	5009 C808h	500D C808h	5001 D808h
80Ch	32	EPWM_DESTS	5009 C80Ch	500D C80Ch	5001 D80Ch
810h	32	EPWM_DEFRC	5009 C810h	500D C810h	5001 D810h
814h	32	EPWM_DECLR	5009 C814h	500D C814h	5001 D814h
820h	32	EPWM_DEMONCNT	5009 C820h	500D C820h	5001 D820h
824h	32	EPWM_DEMONCTL	5009 C824h	500D C824h	5001 D824h
828h	32	EPWM_DEMONSTEP	5009 C828h	500D C828h	5001 D828h
82Ch	32	EPWM_DEMONTHRES	5009 C82Ch	500D C82Ch	5001 D82Ch
C00h	32	EPWM_MINDBCFG	5009 CC00h	500D CC00h	5001 DC00h

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Table 3-608. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM18_G3 Physical Address	EPWM19_G3 Physical Address	EPWM20_G3 Physical Address
C04h	32	EPWM_MINDBDLY	5009 CC04h	500D CC04h	5001 DC04h
C20h	32	EPWM_LUTCTLA	5009 CC20h	500D CC20h	5001 DC20h
C24h	32	EPWM_LUTCTLB	5009 CC24h	500D CC24h	5001 DC24h

Table 3-609. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM21_G3 Physical Address	EPWM22_G3 Physical Address	EPWM23_G3 Physical Address
0h	16	EPWM_TBCTL	5005 D000h	5009 D000h	500D D000h
2h	16	EPWM_TBCTL2	5005 D002h	5009 D002h	500D D002h
6h	16	EPWM_EPWMSYNCINSEL	5005 D006h	5009 D006h	500D D006h
8h	16	EPWM_TBCTR	5005 D008h	5009 D008h	500D D008h
Ah	16	EPWM_TBSTS	5005 D00Ah	5009 D00Ah	500D D00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5005 D00Ch	5009 D00Ch	500D D00Ch
Eh	16	EPWM_TBCTL3	5005 D00Eh	5009 D00Eh	500D D00Eh
10h	16	EPWM_CMPCTL	5005 D010h	5009 D010h	500D D010h
12h	16	EPWM_CMPCTL2	5005 D012h	5009 D012h	500D D012h
18h	16	EPWM_DBCTL	5005 D018h	5009 D018h	500D D018h
1Ah	16	EPWM_DBCTL2	5005 D01Ah	5009 D01Ah	500D D01Ah
20h	16	EPWM_AQCTL	5005 D020h	5009 D020h	500D D020h
22h	16	EPWM_AQTSRCSEL	5005 D022h	5009 D022h	500D D022h
28h	16	EPWM_PCCTL	5005 D028h	5009 D028h	500D D028h
30h	16	EPWM_VCAPCTL	5005 D030h	5009 D030h	500D D030h
32h	16	EPWM_VCNTCFG	5005 D032h	5009 D032h	500D D032h
40h	16	EPWM_HRCNFG	5005 D040h	5009 D040h	500D D040h
4Eh	16	EPWM_HRCNFG2	5005 D04Eh	5009 D04Eh	500D D04Eh
5Ah	16	EPWM_HRPCTL	5005 D05Ah	5009 D05Ah	500D D05Ah
5Ch	16	EPWM_TRREM	5005 D05Ch	5009 D05Ch	500D D05Ch
68h	16	EPWM_GLDCTL	5005 D068h	5009 D068h	500D D068h
6Ah	16	EPWM_GLDCFG	5005 D06Ah	5009 D06Ah	500D D06Ah
70h	32	EPWM_EPWMXLINK	5005 D070h	5009 D070h	500D D070h
74h	32	EPWM_EPWMXLINK2	5005 D074h	5009 D074h	500D D074h
7Ah	16	EPWM_ETEST	5005 D07Ah	5009 D07Ah	500D D07Ah
7Ch	16	EPWM_EPWMREV	5005 D07Ch	5009 D07Ch	500D D07Ch
7Eh	16	EPWM_HRPWMREV	5005 D07Eh	5009 D07Eh	500D D07Eh
80h	16	EPWM_AQCTLA	5005 D080h	5009 D080h	500D D080h
82h	16	EPWM_AQCTLA2	5005 D082h	5009 D082h	500D D082h
84h	16	EPWM_AQCTLB	5005 D084h	5009 D084h	500D D084h
86h	16	EPWM_AQCTLB2	5005 D086h	5009 D086h	500D D086h
8Eh	16	EPWM_AQSFRC	5005 D08Eh	5009 D08Eh	500D D08Eh
92h	16	EPWM_AQCSFRC	5005 D092h	5009 D092h	500D D092h
A0h	16	EPWM_DBREDHR	5005 D0A0h	5009 D0A0h	500D D0A0h
A2h	16	EPWM_DBRED	5005 D0A2h	5009 D0A2h	500D D0A2h
A4h	16	EPWM_DBFEDHR	5005 D0A4h	5009 D0A4h	500D D0A4h
A6h	16	EPWM_DBFED	5005 D0A6h	5009 D0A6h	500D D0A6h
C0h	32	EPWM_TBPHS	5005 D0C0h	5009 D0C0h	500D D0C0h
C4h	16	EPWM_TBPRDHR	5005 D0C4h	5009 D0C4h	500D D0C4h

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Table 3-609. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM21_G3 Physical Address	EPWM22_G3 Physical Address	EPWM23_G3 Physical Address
C6h	16	EPWM_TBPRD	5005 D0C6h	5009 D0C6h	500D D0C6h
C8h	16	EPWM_TBPRDHRB	5005 D0C8h	5009 D0C8h	500D D0C8h
D4h	32	EPWM_CMPA	5005 D0D4h	5009 D0D4h	500D D0D4h
D8h	32	EPWM_CMPB	5005 D0D8h	5009 D0D8h	500D D0D8h
DEh	16	EPWM_CMPC	5005 D0DEh	5009 D0DEh	500D D0DEh
E2h	16	EPWM_CMPD	5005 D0E2h	5009 D0E2h	500D D0E2h
E8h	16	EPWM_GLDCTL2	5005 D0E8h	5009 D0E8h	500D D0E8h
EEh	16	EPWM_SWVDELVAL	5005 D0EEh	5009 D0EEh	500D D0EEh
100h	16	EPWM_TZSEL	5005 D100h	5009 D100h	500D D100h
102h	16	EPWM_TZSEL2	5005 D102h	5009 D102h	500D D102h
104h	16	EPWM_TZDCSEL	5005 D104h	5009 D104h	500D D104h
108h	16	EPWM_TZCTL	5005 D108h	5009 D108h	500D D108h
10Ah	16	EPWM_TZCTL2	5005 D10Ah	5009 D10Ah	500D D10Ah
10Ch	16	EPWM_TZCTLDCA	5005 D10Ch	5009 D10Ch	500D D10Ch
10Eh	16	EPWM_TZCTLDCB	5005 D10Eh	5009 D10Eh	500D D10Eh
11Ah	16	EPWM_TZEINT	5005 D11Ah	5009 D11Ah	500D D11Ah
126h	16	EPWM_TZFLG	5005 D126h	5009 D126h	500D D126h
128h	16	EPWM_TZCBCFLG	5005 D128h	5009 D128h	500D D128h
12Ah	16	EPWM_TZOSTFLG	5005 D12Ah	5009 D12Ah	500D D12Ah
12Eh	16	EPWM_TZCLR	5005 D12Eh	5009 D12Eh	500D D12Eh
130h	16	EPWM_TZCBCCLR	5005 D130h	5009 D130h	500D D130h
132h	16	EPWM_TZOSTCLR	5005 D132h	5009 D132h	500D D132h
136h	16	EPWM_TZFRC	5005 D136h	5009 D136h	500D D136h
13Ah	16	EPWM_TZTRIPOUTSEL	5005 D13Ah	5009 D13Ah	500D D13Ah
148h	16	EPWM_ETSEL	5005 D148h	5009 D148h	500D D148h
14Ch	16	EPWM_ETPS	5005 D14Ch	5009 D14Ch	500D D14Ch
150h	16	EPWM_ETFLG	5005 D150h	5009 D150h	500D D150h
154h	16	EPWM_ETCLR	5005 D154h	5009 D154h	500D D154h
158h	16	EPWM_ETFRC	5005 D158h	5009 D158h	500D D158h
15Ch	16	EPWM_ETINTPS	5005 D15Ch	5009 D15Ch	500D D15Ch
160h	16	EPWM_ETSOCPS	5005 D160h	5009 D160h	500D D160h
164h	16	EPWM_ETCNTINITCTL	5005 D164h	5009 D164h	500D D164h
168h	16	EPWM_ETCNTINIT	5005 D168h	5009 D168h	500D D168h
16Ch	16	EPWM_ETINTMIXEN	5005 D16Ch	5009 D16Ch	500D D16Ch
170h	16	EPWM_ETSOCAMIXEN	5005 D170h	5009 D170h	500D D170h
174h	16	EPWM_ETSOCBMIXEN	5005 D174h	5009 D174h	500D D174h
180h	16	EPWM_DCTRIPSEL	5005 D180h	5009 D180h	500D D180h
186h	16	EPWM_DCACTL	5005 D186h	5009 D186h	500D D186h
188h	16	EPWM_DCBCTL	5005 D188h	5009 D188h	500D D188h
18Eh	16	EPWM_DCFCTL	5005 D18Eh	5009 D18Eh	500D D18Eh
190h	16	EPWM_DCCAPCTL	5005 D190h	5009 D190h	500D D190h
192h	16	EPWM_DCFOFFSET	5005 D192h	5009 D192h	500D D192h
194h	16	EPWM_DCFOFFSETCNT	5005 D194h	5009 D194h	500D D194h
196h	16	EPWM_DCFWINDOW	5005 D196h	5009 D196h	500D D196h
198h	16	EPWM_DCFWINDOWCNT	5005 D198h	5009 D198h	500D D198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5005 D19Ah	5009 D19Ah	500D D19Ah

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Table 3-609. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM21_G3 Physical Address	EPWM22_G3 Physical Address	EPWM23_G3 Physical Address
19Ch	16	EPWM_DCCAPMIXSEL	5005 D19Ch	5009 D19Ch	500D D19Ch
19Eh	16	EPWM_DCCAP	5005 D19Eh	5009 D19Eh	500D D19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5005 D1A4h	5009 D1A4h	500D D1A4h
1A6h	16	EPWM_DCALTRIPSEL	5005 D1A6h	5009 D1A6h	500D D1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5005 D1A8h	5009 D1A8h	500D D1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5005 D1AAh	5009 D1AAh	500D D1AAh
1ACh	16	EPWM_CAPCTL	5005 D1ACh	5009 D1ACh	500D D1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5005 D1AEh	5009 D1AEh	500D D1AEh
1B0h	16	EPWM_CAPINTRIPSEL	5005 D1B0h	5009 D1B0h	500D D1B0h
1B2h	16	EPWM_CAPTRIPSEL	5005 D1B2h	5009 D1B2h	500D D1B2h
1F4h	32	EPWM_EPWMLOCK	5005 D1F4h	5009 D1F4h	500D D1F4h
1FAh	16	EPWM_HWVDELVAL	5005 D1FAh	5009 D1FAh	500D D1FAh
1FCh	16	EPWM_VCNTVAL	5005 D1FCh	5009 D1FCh	500D D1FCh
400h	32	EPWM_XCMPCTL1	5005 D400h	5009 D400h	500D D400h
410h	32	EPWM_XLOADCTL	5005 D410h	5009 D410h	500D D410h
418h	32	EPWM_XLOAD	5005 D418h	5009 D418h	500D D418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5005 D41Ch	5009 D41Ch	500D D41Ch
420h	32	EPWM_XREGSHDW1STS	5005 D420h	5009 D420h	500D D420h
428h	32	EPWM_XREGSHDW2STS	5005 D428h	5009 D428h	500D D428h
430h	32	EPWM_XREGSHDW3STS	5005 D430h	5009 D430h	500D D430h
600h	32	EPWM_XCMP1_ACTIVE	5005 D600h	5009 D600h	500D D600h
604h	32	EPWM_XCMP2_ACTIVE	5005 D604h	5009 D604h	500D D604h
608h	32	EPWM_XCMP3_ACTIVE	5005 D608h	5009 D608h	500D D608h
60Ch	32	EPWM_XCMP4_ACTIVE	5005 D60Ch	5009 D60Ch	500D D60Ch
610h	32	EPWM_XCMP5_ACTIVE	5005 D610h	5009 D610h	500D D610h
614h	32	EPWM_XCMP6_ACTIVE	5005 D614h	5009 D614h	500D D614h
618h	32	EPWM_XCMP7_ACTIVE	5005 D618h	5009 D618h	500D D618h
61Ch	32	EPWM_XCMP8_ACTIVE	5005 D61Ch	5009 D61Ch	500D D61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5005 D620h	5009 D620h	500D D620h
630h	16	EPWM_XAQCTLA_ACTIVE	5005 D630h	5009 D630h	500D D630h
644h	32	EPWM_XMINMAX_ACTIVE	5005 D644h	5009 D644h	500D D644h
680h	32	EPWM_XCMP1_SHDW1	5005 D680h	5009 D680h	500D D680h
684h	32	EPWM_XCMP2_SHDW1	5005 D684h	5009 D684h	500D D684h
688h	32	EPWM_XCMP3_SHDW1	5005 D688h	5009 D688h	500D D688h
68Ch	32	EPWM_XCMP4_SHDW1	5005 D68Ch	5009 D68Ch	500D D68Ch
690h	32	EPWM_XCMP5_SHDW1	5005 D690h	5009 D690h	500D D690h
694h	32	EPWM_XCMP6_SHDW1	5005 D694h	5009 D694h	500D D694h
698h	32	EPWM_XCMP7_SHDW1	5005 D698h	5009 D698h	500D D698h
69Ch	32	EPWM_XCMP8_SHDW1	5005 D69Ch	5009 D69Ch	500D D69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5005 D6A0h	5009 D6A0h	500D D6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5005 D6B0h	5009 D6B0h	500D D6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5005 D6B2h	5009 D6B2h	500D D6B2h
6BAh	16	EPWM_CMPC_SHDW1	5005 D6BAh	5009 D6BAh	500D D6BAh
6BEh	16	EPWM_CMPD_SHDW1	5005 D6BEh	5009 D6BEh	500D D6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5005 D6C4h	5009 D6C4h	500D D6C4h
700h	32	EPWM_XCMP1_SHDW2	5005 D700h	5009 D700h	500D D700h

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Table 3-609. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM21_G3 Physical Address	EPWM22_G3 Physical Address	EPWM23_G3 Physical Address
704h	32	EPWM_XCMP2_SHDW2	5005 D704h	5009 D704h	500D D704h
708h	32	EPWM_XCMP3_SHDW2	5005 D708h	5009 D708h	500D D708h
70Ch	32	EPWM_XCMP4_SHDW2	5005 D70Ch	5009 D70Ch	500D D70Ch
710h	32	EPWM_XCMP5_SHDW2	5005 D710h	5009 D710h	500D D710h
714h	32	EPWM_XCMP6_SHDW2	5005 D714h	5009 D714h	500D D714h
718h	32	EPWM_XCMP7_SHDW2	5005 D718h	5009 D718h	500D D718h
71Ch	32	EPWM_XCMP8_SHDW2	5005 D71Ch	5009 D71Ch	500D D71Ch
720h	32	EPWM_XTBPRD_SHDW2	5005 D720h	5009 D720h	500D D720h
730h	16	EPWM_XAQCTLA_SHDW2	5005 D730h	5009 D730h	500D D730h
732h	16	EPWM_XAQCTLB_SHDW2	5005 D732h	5009 D732h	500D D732h
73Ah	16	EPWM_CMPC_SHDW2	5005 D73Ah	5009 D73Ah	500D D73Ah
73Eh	16	EPWM_CMPD_SHDW2	5005 D73Eh	5009 D73Eh	500D D73Eh
744h	32	EPWM_XMINMAX_SHDW2	5005 D744h	5009 D744h	500D D744h
780h	32	EPWM_XCMP1_SHDW3	5005 D780h	5009 D780h	500D D780h
784h	32	EPWM_XCMP2_SHDW3	5005 D784h	5009 D784h	500D D784h
788h	32	EPWM_XCMP3_SHDW3	5005 D788h	5009 D788h	500D D788h
78Ch	32	EPWM_XCMP4_SHDW3	5005 D78Ch	5009 D78Ch	500D D78Ch
790h	32	EPWM_XCMP5_SHDW3	5005 D790h	5009 D790h	500D D790h
794h	32	EPWM_XCMP6_SHDW3	5005 D794h	5009 D794h	500D D794h
798h	32	EPWM_XCMP7_SHDW3	5005 D798h	5009 D798h	500D D798h
79Ch	32	EPWM_XCMP8_SHDW3	5005 D79Ch	5009 D79Ch	500D D79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5005 D7A0h	5009 D7A0h	500D D7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5005 D7B0h	5009 D7B0h	500D D7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5005 D7B2h	5009 D7B2h	500D D7B2h
7BAh	16	EPWM_CMPC_SHDW3	5005 D7BAh	5009 D7BAh	500D D7BAh
7BEh	16	EPWM_CMPD_SHDW3	5005 D7BEh	5009 D7BEh	500D D7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5005 D7C4h	5009 D7C4h	500D D7C4h
800h	32	EPWM_DECTL	5005 D800h	5009 D800h	500D D800h
804h	32	EPWM_DECOMPSEL	5005 D804h	5009 D804h	500D D804h
808h	32	EPWM_DEACTCTL	5005 D808h	5009 D808h	500D D808h
80Ch	32	EPWM_DESTS	5005 D80Ch	5009 D80Ch	500D D80Ch
810h	32	EPWM_DEFRC	5005 D810h	5009 D810h	500D D810h
814h	32	EPWM_DECLR	5005 D814h	5009 D814h	500D D814h
820h	32	EPWM_DEMONCNT	5005 D820h	5009 D820h	500D D820h
824h	32	EPWM_DEMONCTL	5005 D824h	5009 D824h	500D D824h
828h	32	EPWM_DEMONSTEP	5005 D828h	5009 D828h	500D D828h
82Ch	32	EPWM_DEMONTHRES	5005 D82Ch	5009 D82Ch	500D D82Ch
C00h	32	EPWM_MINDBCFG	5005 DC00h	5009 DC00h	500D DC00h
C04h	32	EPWM_MINDBDLY	5005 DC04h	5009 DC04h	500D DC04h
C20h	32	EPWM_LUTCTLA	5005 DC20h	5009 DC20h	500D DC20h
C24h	32	EPWM_LUTCTLB	5005 DC24h	5009 DC24h	500D DC24h

Table 3-610. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM24_G3 Physical Address	EPWM25_G3 Physical Address	EPWM26_G3 Physical Address
0h	16	EPWM_TBCTL	5001 E000h	5005 E000h	5009 E000h

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Table 3-610. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM24_G3 Physical Address	EPWM25_G3 Physical Address	EPWM26_G3 Physical Address
2h	16	EPWM_TBCTL2	5001 E002h	5005 E002h	5009 E002h
6h	16	EPWM_EPWMSYNCINSEL	5001 E006h	5005 E006h	5009 E006h
8h	16	EPWM_TBCTR	5001 E008h	5005 E008h	5009 E008h
Ah	16	EPWM_TBSTS	5001 E00Ah	5005 E00Ah	5009 E00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5001 E00Ch	5005 E00Ch	5009 E00Ch
Eh	16	EPWM_TBCTL3	5001 E00Eh	5005 E00Eh	5009 E00Eh
10h	16	EPWM_CMPCTL	5001 E010h	5005 E010h	5009 E010h
12h	16	EPWM_CMPCTL2	5001 E012h	5005 E012h	5009 E012h
18h	16	EPWM_DBCTL	5001 E018h	5005 E018h	5009 E018h
1Ah	16	EPWM_DBCTL2	5001 E01Ah	5005 E01Ah	5009 E01Ah
20h	16	EPWM_AQCTL	5001 E020h	5005 E020h	5009 E020h
22h	16	EPWM_AQTSRCSEL	5001 E022h	5005 E022h	5009 E022h
28h	16	EPWM_PCCTL	5001 E028h	5005 E028h	5009 E028h
30h	16	EPWM_VCAPCTL	5001 E030h	5005 E030h	5009 E030h
32h	16	EPWM_VCNTCFG	5001 E032h	5005 E032h	5009 E032h
40h	16	EPWM_HRCNFG	5001 E040h	5005 E040h	5009 E040h
4Eh	16	EPWM_HRCNFG2	5001 E04Eh	5005 E04Eh	5009 E04Eh
5Ah	16	EPWM_HRPCTL	5001 E05Ah	5005 E05Ah	5009 E05Ah
5Ch	16	EPWM_TRREM	5001 E05Ch	5005 E05Ch	5009 E05Ch
68h	16	EPWM_GLDCTL	5001 E068h	5005 E068h	5009 E068h
6Ah	16	EPWM_GLDCFG	5001 E06Ah	5005 E06Ah	5009 E06Ah
70h	32	EPWM_EPWMXLINK	5001 E070h	5005 E070h	5009 E070h
74h	32	EPWM_EPWMXLINK2	5001 E074h	5005 E074h	5009 E074h
7Ah	16	EPWM_ETEST	5001 E07Ah	5005 E07Ah	5009 E07Ah
7Ch	16	EPWM_EPWMREV	5001 E07Ch	5005 E07Ch	5009 E07Ch
7Eh	16	EPWM_HRPWMREV	5001 E07Eh	5005 E07Eh	5009 E07Eh
80h	16	EPWM_AQCTLA	5001 E080h	5005 E080h	5009 E080h
82h	16	EPWM_AQCTLA2	5001 E082h	5005 E082h	5009 E082h
84h	16	EPWM_AQCTLB	5001 E084h	5005 E084h	5009 E084h
86h	16	EPWM_AQCTLB2	5001 E086h	5005 E086h	5009 E086h
8Eh	16	EPWM_AQSFRC	5001 E08Eh	5005 E08Eh	5009 E08Eh
92h	16	EPWM_AQCSFRC	5001 E092h	5005 E092h	5009 E092h
A0h	16	EPWM_DBREDHR	5001 E0A0h	5005 E0A0h	5009 E0A0h
A2h	16	EPWM_DBRED	5001 E0A2h	5005 E0A2h	5009 E0A2h
A4h	16	EPWM_DBFEDHR	5001 E0A4h	5005 E0A4h	5009 E0A4h
A6h	16	EPWM_DBFED	5001 E0A6h	5005 E0A6h	5009 E0A6h
C0h	32	EPWM_TBPHS	5001 E0C0h	5005 E0C0h	5009 E0C0h
C4h	16	EPWM_TBPRDHR	5001 E0C4h	5005 E0C4h	5009 E0C4h
C6h	16	EPWM_TBPRD	5001 E0C6h	5005 E0C6h	5009 E0C6h
C8h	16	EPWM_TBPRDHRB	5001 E0C8h	5005 E0C8h	5009 E0C8h
D4h	32	EPWM_CMPA	5001 E0D4h	5005 E0D4h	5009 E0D4h
D8h	32	EPWM_CMPB	5001 E0D8h	5005 E0D8h	5009 E0D8h
DEh	16	EPWM_CMPC	5001 E0DEh	5005 E0DEh	5009 E0DEh
E2h	16	EPWM_CMPD	5001 E0E2h	5005 E0E2h	5009 E0E2h
E8h	16	EPWM_GLDCTL2	5001 E0E8h	5005 E0E8h	5009 E0E8h
EEh	16	EPWM_SWVDELVAL	5001 E0EEh	5005 E0EEh	5009 E0EEh

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Table 3-610. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM24_G3 Physical Address	EPWM25_G3 Physical Address	EPWM26_G3 Physical Address
100h	16	EPWM_TZSEL	5001 E100h	5005 E100h	5009 E100h
102h	16	EPWM_TZSEL2	5001 E102h	5005 E102h	5009 E102h
104h	16	EPWM_TZDCSEL	5001 E104h	5005 E104h	5009 E104h
108h	16	EPWM_TZCTL	5001 E108h	5005 E108h	5009 E108h
10Ah	16	EPWM_TZCTL2	5001 E10Ah	5005 E10Ah	5009 E10Ah
10Ch	16	EPWM_TZCTLDCA	5001 E10Ch	5005 E10Ch	5009 E10Ch
10Eh	16	EPWM_TZCTLDCB	5001 E10Eh	5005 E10Eh	5009 E10Eh
11Ah	16	EPWM_TZEINT	5001 E11Ah	5005 E11Ah	5009 E11Ah
126h	16	EPWM_TZFLG	5001 E126h	5005 E126h	5009 E126h
128h	16	EPWM_TZCBCFLG	5001 E128h	5005 E128h	5009 E128h
12Ah	16	EPWM_TZOSTFLG	5001 E12Ah	5005 E12Ah	5009 E12Ah
12Eh	16	EPWM_TZCLR	5001 E12Eh	5005 E12Eh	5009 E12Eh
130h	16	EPWM_TZCBCCLR	5001 E130h	5005 E130h	5009 E130h
132h	16	EPWM_TZOSTCLR	5001 E132h	5005 E132h	5009 E132h
136h	16	EPWM_TZFRC	5001 E136h	5005 E136h	5009 E136h
13Ah	16	EPWM_TZTRIPOUTSEL	5001 E13Ah	5005 E13Ah	5009 E13Ah
148h	16	EPWM_ETSEL	5001 E148h	5005 E148h	5009 E148h
14Ch	16	EPWM_ETPS	5001 E14Ch	5005 E14Ch	5009 E14Ch
150h	16	EPWM_ETFLG	5001 E150h	5005 E150h	5009 E150h
154h	16	EPWM_ETCLR	5001 E154h	5005 E154h	5009 E154h
158h	16	EPWM_ETFRC	5001 E158h	5005 E158h	5009 E158h
15Ch	16	EPWM_ETINTPS	5001 E15Ch	5005 E15Ch	5009 E15Ch
160h	16	EPWM_ETSOCPS	5001 E160h	5005 E160h	5009 E160h
164h	16	EPWM_ETCNTINITCTL	5001 E164h	5005 E164h	5009 E164h
168h	16	EPWM_ETCNTINIT	5001 E168h	5005 E168h	5009 E168h
16Ch	16	EPWM_ETINTMIXEN	5001 E16Ch	5005 E16Ch	5009 E16Ch
170h	16	EPWM_ETSOCAMIXEN	5001 E170h	5005 E170h	5009 E170h
174h	16	EPWM_ETSOCBMIXEN	5001 E174h	5005 E174h	5009 E174h
180h	16	EPWM_DCTRIPSEL	5001 E180h	5005 E180h	5009 E180h
186h	16	EPWM_DCACTL	5001 E186h	5005 E186h	5009 E186h
188h	16	EPWM_DCBCTL	5001 E188h	5005 E188h	5009 E188h
18Eh	16	EPWM_DCFCTL	5001 E18Eh	5005 E18Eh	5009 E18Eh
190h	16	EPWM_DCCAPCTL	5001 E190h	5005 E190h	5009 E190h
192h	16	EPWM_DCFOFFSET	5001 E192h	5005 E192h	5009 E192h
194h	16	EPWM_DCFOFFSETCNT	5001 E194h	5005 E194h	5009 E194h
196h	16	EPWM_DCFWINDOW	5001 E196h	5005 E196h	5009 E196h
198h	16	EPWM_DCFWINDOWCNT	5001 E198h	5005 E198h	5009 E198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5001 E19Ah	5005 E19Ah	5009 E19Ah
19Ch	16	EPWM_DCCAPMIXSEL	5001 E19Ch	5005 E19Ch	5009 E19Ch
19Eh	16	EPWM_DCCAP	5001 E19Eh	5005 E19Eh	5009 E19Eh
1A4h	16	EPWM_DCAHTRIPSEL	5001 E1A4h	5005 E1A4h	5009 E1A4h
1A6h	16	EPWM_DCALTRIPSEL	5001 E1A6h	5005 E1A6h	5009 E1A6h
1A8h	16	EPWM_DCBHTRIPSEL	5001 E1A8h	5005 E1A8h	5009 E1A8h
1AAh	16	EPWM_DCBLTRIPSEL	5001 E1AAh	5005 E1AAh	5009 E1AAh
1ACh	16	EPWM_CAPCTL	5001 E1ACh	5005 E1ACh	5009 E1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5001 E1AEh	5005 E1AEh	5009 E1AEh

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Table 3-610. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM24_G3 Physical Address	EPWM25_G3 Physical Address	EPWM26_G3 Physical Address
1B0h	16	EPWM_CAPINTRIPSEL	5001 E1B0h	5005 E1B0h	5009 E1B0h
1B2h	16	EPWM_CAPTRIPSEL	5001 E1B2h	5005 E1B2h	5009 E1B2h
1F4h	32	EPWM_EPWMLOCK	5001 E1F4h	5005 E1F4h	5009 E1F4h
1FAh	16	EPWM_HWVDELVAL	5001 E1FAh	5005 E1FAh	5009 E1FAh
1FCh	16	EPWM_VCNTVAL	5001 E1FCh	5005 E1FCh	5009 E1FCh
400h	32	EPWM_XCMPCTL1	5001 E400h	5005 E400h	5009 E400h
410h	32	EPWM_XLOADCTL	5001 E410h	5005 E410h	5009 E410h
418h	32	EPWM_XLOAD	5001 E418h	5005 E418h	5009 E418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5001 E41Ch	5005 E41Ch	5009 E41Ch
420h	32	EPWM_XREGSHDW1STS	5001 E420h	5005 E420h	5009 E420h
428h	32	EPWM_XREGSHDW2STS	5001 E428h	5005 E428h	5009 E428h
430h	32	EPWM_XREGSHDW3STS	5001 E430h	5005 E430h	5009 E430h
600h	32	EPWM_XCMP1_ACTIVE	5001 E600h	5005 E600h	5009 E600h
604h	32	EPWM_XCMP2_ACTIVE	5001 E604h	5005 E604h	5009 E604h
608h	32	EPWM_XCMP3_ACTIVE	5001 E608h	5005 E608h	5009 E608h
60Ch	32	EPWM_XCMP4_ACTIVE	5001 E60Ch	5005 E60Ch	5009 E60Ch
610h	32	EPWM_XCMP5_ACTIVE	5001 E610h	5005 E610h	5009 E610h
614h	32	EPWM_XCMP6_ACTIVE	5001 E614h	5005 E614h	5009 E614h
618h	32	EPWM_XCMP7_ACTIVE	5001 E618h	5005 E618h	5009 E618h
61Ch	32	EPWM_XCMP8_ACTIVE	5001 E61Ch	5005 E61Ch	5009 E61Ch
620h	32	EPWM_XTBPRD_ACTIVE	5001 E620h	5005 E620h	5009 E620h
630h	16	EPWM_XAQCTLA_ACTIVE	5001 E630h	5005 E630h	5009 E630h
644h	32	EPWM_XMINMAX_ACTIVE	5001 E644h	5005 E644h	5009 E644h
680h	32	EPWM_XCMP1_SHDW1	5001 E680h	5005 E680h	5009 E680h
684h	32	EPWM_XCMP2_SHDW1	5001 E684h	5005 E684h	5009 E684h
688h	32	EPWM_XCMP3_SHDW1	5001 E688h	5005 E688h	5009 E688h
68Ch	32	EPWM_XCMP4_SHDW1	5001 E68Ch	5005 E68Ch	5009 E68Ch
690h	32	EPWM_XCMP5_SHDW1	5001 E690h	5005 E690h	5009 E690h
694h	32	EPWM_XCMP6_SHDW1	5001 E694h	5005 E694h	5009 E694h
698h	32	EPWM_XCMP7_SHDW1	5001 E698h	5005 E698h	5009 E698h
69Ch	32	EPWM_XCMP8_SHDW1	5001 E69Ch	5005 E69Ch	5009 E69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5001 E6A0h	5005 E6A0h	5009 E6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5001 E6B0h	5005 E6B0h	5009 E6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5001 E6B2h	5005 E6B2h	5009 E6B2h
6BAh	16	EPWM_CMPC_SHDW1	5001 E6BAh	5005 E6BAh	5009 E6BAh
6BEh	16	EPWM_CMPD_SHDW1	5001 E6BEh	5005 E6BEh	5009 E6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5001 E6C4h	5005 E6C4h	5009 E6C4h
700h	32	EPWM_XCMP1_SHDW2	5001 E700h	5005 E700h	5009 E700h
704h	32	EPWM_XCMP2_SHDW2	5001 E704h	5005 E704h	5009 E704h
708h	32	EPWM_XCMP3_SHDW2	5001 E708h	5005 E708h	5009 E708h
70Ch	32	EPWM_XCMP4_SHDW2	5001 E70Ch	5005 E70Ch	5009 E70Ch
710h	32	EPWM_XCMP5_SHDW2	5001 E710h	5005 E710h	5009 E710h
714h	32	EPWM_XCMP6_SHDW2	5001 E714h	5005 E714h	5009 E714h
718h	32	EPWM_XCMP7_SHDW2	5001 E718h	5005 E718h	5009 E718h
71Ch	32	EPWM_XCMP8_SHDW2	5001 E71Ch	5005 E71Ch	5009 E71Ch
720h	32	EPWM_XTBPRD_SHDW2	5001 E720h	5005 E720h	5009 E720h

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Table 3-610. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM24_G3 Physical Address	EPWM25_G3 Physical Address	EPWM26_G3 Physical Address
730h	16	EPWM_XAQCTLA_SHDW2	5001 E730h	5005 E730h	5009 E730h
732h	16	EPWM_XAQCTLB_SHDW2	5001 E732h	5005 E732h	5009 E732h
73Ah	16	EPWM_CMPC_SHDW2	5001 E73Ah	5005 E73Ah	5009 E73Ah
73Eh	16	EPWM_CMPD_SHDW2	5001 E73Eh	5005 E73Eh	5009 E73Eh
744h	32	EPWM_XMINMAX_SHDW2	5001 E744h	5005 E744h	5009 E744h
780h	32	EPWM_XCMP1_SHDW3	5001 E780h	5005 E780h	5009 E780h
784h	32	EPWM_XCMP2_SHDW3	5001 E784h	5005 E784h	5009 E784h
788h	32	EPWM_XCMP3_SHDW3	5001 E788h	5005 E788h	5009 E788h
78Ch	32	EPWM_XCMP4_SHDW3	5001 E78Ch	5005 E78Ch	5009 E78Ch
790h	32	EPWM_XCMP5_SHDW3	5001 E790h	5005 E790h	5009 E790h
794h	32	EPWM_XCMP6_SHDW3	5001 E794h	5005 E794h	5009 E794h
798h	32	EPWM_XCMP7_SHDW3	5001 E798h	5005 E798h	5009 E798h
79Ch	32	EPWM_XCMP8_SHDW3	5001 E79Ch	5005 E79Ch	5009 E79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5001 E7A0h	5005 E7A0h	5009 E7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5001 E7B0h	5005 E7B0h	5009 E7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5001 E7B2h	5005 E7B2h	5009 E7B2h
7BAh	16	EPWM_CMPC_SHDW3	5001 E7BAh	5005 E7BAh	5009 E7BAh
7BEh	16	EPWM_CMPD_SHDW3	5001 E7BEh	5005 E7BEh	5009 E7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5001 E7C4h	5005 E7C4h	5009 E7C4h
800h	32	EPWM_DECTL	5001 E800h	5005 E800h	5009 E800h
804h	32	EPWM_DECOMPSEL	5001 E804h	5005 E804h	5009 E804h
808h	32	EPWM_DEACTCTL	5001 E808h	5005 E808h	5009 E808h
80Ch	32	EPWM_DESTS	5001 E80Ch	5005 E80Ch	5009 E80Ch
810h	32	EPWM_DEFRC	5001 E810h	5005 E810h	5009 E810h
814h	32	EPWM_DECLR	5001 E814h	5005 E814h	5009 E814h
820h	32	EPWM_DEMONCNT	5001 E820h	5005 E820h	5009 E820h
824h	32	EPWM_DEMONCTL	5001 E824h	5005 E824h	5009 E824h
828h	32	EPWM_DEMONSTEP	5001 E828h	5005 E828h	5009 E828h
82Ch	32	EPWM_DEMONTHRES	5001 E82Ch	5005 E82Ch	5009 E82Ch
C00h	32	EPWM_MINDBCFG	5001 EC00h	5005 EC00h	5009 EC00h
C04h	32	EPWM_MINDBDLY	5001 EC04h	5005 EC04h	5009 EC04h
C20h	32	EPWM_LUTCTLA	5001 EC20h	5005 EC20h	5009 EC20h
C24h	32	EPWM_LUTCTLB	5001 EC24h	5005 EC24h	5009 EC24h

Table 3-611. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM27_G3 Physical Address	EPWM28_G3 Physical Address	EPWM29_G3 Physical Address
0h	16	EPWM_TBCTL	500D E000h	5001 F000h	5005 F000h
2h	16	EPWM_TBCTL2	500D E002h	5001 F002h	5005 F002h
6h	16	EPWM_EPWMSYNCINSEL	500D E006h	5001 F006h	5005 F006h
8h	16	EPWM_TBCTR	500D E008h	5001 F008h	5005 F008h
Ah	16	EPWM_TBSTS	500D E00Ah	5001 F00Ah	5005 F00Ah
Ch	16	EPWM_EPWMSYNCOUTEN	500D E00Ch	5001 F00Ch	5005 F00Ch
Eh	16	EPWM_TBCTL3	500D E00Eh	5001 F00Eh	5005 F00Eh
10h	16	EPWM_CMPCTL	500D E010h	5001 F010h	5005 F010h
12h	16	EPWM_CMPCTL2	500D E012h	5001 F012h	5005 F012h

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Table 3-611. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM27_G3 Physical Address	EPWM28_G3 Physical Address	EPWM29_G3 Physical Address
18h	16	EPWM_DBCTL	500D E018h	5001 F018h	5005 F018h
1Ah	16	EPWM_DBCTL2	500D E01Ah	5001 F01Ah	5005 F01Ah
20h	16	EPWM_AQCTL	500D E020h	5001 F020h	5005 F020h
22h	16	EPWM_AQTSRCSEL	500D E022h	5001 F022h	5005 F022h
28h	16	EPWM_PCCTL	500D E028h	5001 F028h	5005 F028h
30h	16	EPWM_VCAPCTL	500D E030h	5001 F030h	5005 F030h
32h	16	EPWM_VCNTCFG	500D E032h	5001 F032h	5005 F032h
40h	16	EPWM_HRCNFG	500D E040h	5001 F040h	5005 F040h
4Eh	16	EPWM_HRCNFG2	500D E04Eh	5001 F04Eh	5005 F04Eh
5Ah	16	EPWM_HRPCTL	500D E05Ah	5001 F05Ah	5005 F05Ah
5Ch	16	EPWM_TRREM	500D E05Ch	5001 F05Ch	5005 F05Ch
68h	16	EPWM_GLDCTL	500D E068h	5001 F068h	5005 F068h
6Ah	16	EPWM_GLDCFG	500D E06Ah	5001 F06Ah	5005 F06Ah
70h	32	EPWM_EPWMXLINK	500D E070h	5001 F070h	5005 F070h
74h	32	EPWM_EPWMXLINK2	500D E074h	5001 F074h	5005 F074h
7Ah	16	EPWM_ETEST	500D E07Ah	5001 F07Ah	5005 F07Ah
7Ch	16	EPWM_EPWMREV	500D E07Ch	5001 F07Ch	5005 F07Ch
7Eh	16	EPWM_HRPWMREV	500D E07Eh	5001 F07Eh	5005 F07Eh
80h	16	EPWM_AQCTLA	500D E080h	5001 F080h	5005 F080h
82h	16	EPWM_AQCTLA2	500D E082h	5001 F082h	5005 F082h
84h	16	EPWM_AQCTLB	500D E084h	5001 F084h	5005 F084h
86h	16	EPWM_AQCTLB2	500D E086h	5001 F086h	5005 F086h
8Eh	16	EPWM_AQSFRC	500D E08Eh	5001 F08Eh	5005 F08Eh
92h	16	EPWM_AQCSFRC	500D E092h	5001 F092h	5005 F092h
A0h	16	EPWM_DBREDHR	500D E0A0h	5001 F0A0h	5005 F0A0h
A2h	16	EPWM_DBRED	500D E0A2h	5001 F0A2h	5005 F0A2h
A4h	16	EPWM_DBFEDHR	500D E0A4h	5001 F0A4h	5005 F0A4h
A6h	16	EPWM_DBFED	500D E0A6h	5001 F0A6h	5005 F0A6h
C0h	32	EPWM_TBPHS	500D E0C0h	5001 F0C0h	5005 F0C0h
C4h	16	EPWM_TBPRDHR	500D E0C4h	5001 F0C4h	5005 F0C4h
C6h	16	EPWM_TBPRD	500D E0C6h	5001 F0C6h	5005 F0C6h
C8h	16	EPWM_TBPRDHRB	500D E0C8h	5001 F0C8h	5005 F0C8h
D4h	32	EPWM_CMPA	500D E0D4h	5001 F0D4h	5005 F0D4h
D8h	32	EPWM_CMPB	500D E0D8h	5001 F0D8h	5005 F0D8h
DEh	16	EPWM_CMPC	500D E0DEh	5001 F0DEh	5005 F0DEh
E2h	16	EPWM_CMPD	500D E0E2h	5001 F0E2h	5005 F0E2h
E8h	16	EPWM_GLDCTL2	500D E0E8h	5001 F0E8h	5005 F0E8h
EEh	16	EPWM_SWVDELVAL	500D E0EEh	5001 F0EEh	5005 F0EEh
100h	16	EPWM_TZSEL	500D E100h	5001 F100h	5005 F100h
102h	16	EPWM_TZSEL2	500D E102h	5001 F102h	5005 F102h
104h	16	EPWM_TZDCSEL	500D E104h	5001 F104h	5005 F104h
108h	16	EPWM_TZCTL	500D E108h	5001 F108h	5005 F108h
10Ah	16	EPWM_TZCTL2	500D E10Ah	5001 F10Ah	5005 F10Ah
10Ch	16	EPWM_TZCTLDCA	500D E10Ch	5001 F10Ch	5005 F10Ch
10Eh	16	EPWM_TZCTLDCB	500D E10Eh	5001 F10Eh	5005 F10Eh
11Ah	16	EPWM_TZEINT	500D E11Ah	5001 F11Ah	5005 F11Ah

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Table 3-611. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM27_G3 Physical Address	EPWM28_G3 Physical Address	EPWM29_G3 Physical Address
126h	16	EPWM_TZFLG	500D E126h	5001 F126h	5005 F126h
128h	16	EPWM_TZCBCFLG	500D E128h	5001 F128h	5005 F128h
12Ah	16	EPWM_TZOSTFLG	500D E12Ah	5001 F12Ah	5005 F12Ah
12Eh	16	EPWM_TZCLR	500D E12Eh	5001 F12Eh	5005 F12Eh
130h	16	EPWM_TZCBCCLR	500D E130h	5001 F130h	5005 F130h
132h	16	EPWM_TZOSTCLR	500D E132h	5001 F132h	5005 F132h
136h	16	EPWM_TZFRC	500D E136h	5001 F136h	5005 F136h
13Ah	16	EPWM_TZTRIPOUTSEL	500D E13Ah	5001 F13Ah	5005 F13Ah
148h	16	EPWM_ETSEL	500D E148h	5001 F148h	5005 F148h
14Ch	16	EPWM_ETPS	500D E14Ch	5001 F14Ch	5005 F14Ch
150h	16	EPWM_ETFLG	500D E150h	5001 F150h	5005 F150h
154h	16	EPWM_ETCLR	500D E154h	5001 F154h	5005 F154h
158h	16	EPWM_ETFRC	500D E158h	5001 F158h	5005 F158h
15Ch	16	EPWM_ETINTPS	500D E15Ch	5001 F15Ch	5005 F15Ch
160h	16	EPWM_ETSOCPS	500D E160h	5001 F160h	5005 F160h
164h	16	EPWM_ETCNTINITCTL	500D E164h	5001 F164h	5005 F164h
168h	16	EPWM_ETCNTINIT	500D E168h	5001 F168h	5005 F168h
16Ch	16	EPWM_ETINTMIXEN	500D E16Ch	5001 F16Ch	5005 F16Ch
170h	16	EPWM_ETSOCAMIXEN	500D E170h	5001 F170h	5005 F170h
174h	16	EPWM_ETSOCBMIXEN	500D E174h	5001 F174h	5005 F174h
180h	16	EPWM_DCTRIPSEL	500D E180h	5001 F180h	5005 F180h
186h	16	EPWM_DCACTL	500D E186h	5001 F186h	5005 F186h
188h	16	EPWM_DCBCTL	500D E188h	5001 F188h	5005 F188h
18Eh	16	EPWM_DCFCTL	500D E18Eh	5001 F18Eh	5005 F18Eh
190h	16	EPWM_DCCAPCTL	500D E190h	5001 F190h	5005 F190h
192h	16	EPWM_DCFOFFSET	500D E192h	5001 F192h	5005 F192h
194h	16	EPWM_DCFOFFSETCNT	500D E194h	5001 F194h	5005 F194h
196h	16	EPWM_DCFWINDOW	500D E196h	5001 F196h	5005 F196h
198h	16	EPWM_DCFWINDOWCNT	500D E198h	5001 F198h	5005 F198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500D E19Ah	5001 F19Ah	5005 F19Ah
19Ch	16	EPWM_DCCAPMIXSEL	500D E19Ch	5001 F19Ch	5005 F19Ch
19Eh	16	EPWM_DCCAP	500D E19Eh	5001 F19Eh	5005 F19Eh
1A4h	16	EPWM_DCAHTRIPSEL	500D E1A4h	5001 F1A4h	5005 F1A4h
1A6h	16	EPWM_DCALTRIPSEL	500D E1A6h	5001 F1A6h	5005 F1A6h
1A8h	16	EPWM_DCBHTRIPSEL	500D E1A8h	5001 F1A8h	5005 F1A8h
1AAh	16	EPWM_DCBLTRIPSEL	500D E1AAh	5001 F1AAh	5005 F1AAh
1ACh	16	EPWM_CAPCTL	500D E1ACh	5001 F1ACh	5005 F1ACh
1AEh	16	EPWM_CAPGATETRIPSEL	500D E1AEh	5001 F1AEh	5005 F1AEh
1B0h	16	EPWM_CAPINTRIPSEL	500D E1B0h	5001 F1B0h	5005 F1B0h
1B2h	16	EPWM_CAPTRIPSEL	500D E1B2h	5001 F1B2h	5005 F1B2h
1F4h	32	EPWM_EPWMLOCK	500D E1F4h	5001 F1F4h	5005 F1F4h
1FAh	16	EPWM_HWVDELVAL	500D E1FAh	5001 F1FAh	5005 F1FAh
1FCh	16	EPWM_VCNTVAL	500D E1FCh	5001 F1FCh	5005 F1FCh
400h	32	EPWM_XCMPCTL1	500D E400h	5001 F400h	5005 F400h
410h	32	EPWM_XLOADCTL	500D E410h	5001 F410h	5005 F410h
418h	32	EPWM_XLOAD	500D E418h	5001 F418h	5005 F418h

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Table 3-611. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM27_G3 Physical Address	EPWM28_G3 Physical Address	EPWM29_G3 Physical Address
41Ch	32	EPWM_EPWMXLINKXLOAD	500D E41Ch	5001 F41Ch	5005 F41Ch
420h	32	EPWM_XREGSHDW1STS	500D E420h	5001 F420h	5005 F420h
428h	32	EPWM_XREGSHDW2STS	500D E428h	5001 F428h	5005 F428h
430h	32	EPWM_XREGSHDW3STS	500D E430h	5001 F430h	5005 F430h
600h	32	EPWM_XCMP1_ACTIVE	500D E600h	5001 F600h	5005 F600h
604h	32	EPWM_XCMP2_ACTIVE	500D E604h	5001 F604h	5005 F604h
608h	32	EPWM_XCMP3_ACTIVE	500D E608h	5001 F608h	5005 F608h
60Ch	32	EPWM_XCMP4_ACTIVE	500D E60Ch	5001 F60Ch	5005 F60Ch
610h	32	EPWM_XCMP5_ACTIVE	500D E610h	5001 F610h	5005 F610h
614h	32	EPWM_XCMP6_ACTIVE	500D E614h	5001 F614h	5005 F614h
618h	32	EPWM_XCMP7_ACTIVE	500D E618h	5001 F618h	5005 F618h
61Ch	32	EPWM_XCMP8_ACTIVE	500D E61Ch	5001 F61Ch	5005 F61Ch
620h	32	EPWM_XTBPRD_ACTIVE	500D E620h	5001 F620h	5005 F620h
630h	16	EPWM_XAQCTLA_ACTIVE	500D E630h	5001 F630h	5005 F630h
644h	32	EPWM_XMINMAX_ACTIVE	500D E644h	5001 F644h	5005 F644h
680h	32	EPWM_XCMP1_SHDW1	500D E680h	5001 F680h	5005 F680h
684h	32	EPWM_XCMP2_SHDW1	500D E684h	5001 F684h	5005 F684h
688h	32	EPWM_XCMP3_SHDW1	500D E688h	5001 F688h	5005 F688h
68Ch	32	EPWM_XCMP4_SHDW1	500D E68Ch	5001 F68Ch	5005 F68Ch
690h	32	EPWM_XCMP5_SHDW1	500D E690h	5001 F690h	5005 F690h
694h	32	EPWM_XCMP6_SHDW1	500D E694h	5001 F694h	5005 F694h
698h	32	EPWM_XCMP7_SHDW1	500D E698h	5001 F698h	5005 F698h
69Ch	32	EPWM_XCMP8_SHDW1	500D E69Ch	5001 F69Ch	5005 F69Ch
6A0h	32	EPWM_XTBPRD_SHDW1	500D E6A0h	5001 F6A0h	5005 F6A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	500D E6B0h	5001 F6B0h	5005 F6B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	500D E6B2h	5001 F6B2h	5005 F6B2h
6BAh	16	EPWM_CMPC_SHDW1	500D E6BAh	5001 F6BAh	5005 F6BAh
6BEh	16	EPWM_CMPD_SHDW1	500D E6BEh	5001 F6BEh	5005 F6BEh
6C4h	32	EPWM_XMINMAX_SHDW1	500D E6C4h	5001 F6C4h	5005 F6C4h
700h	32	EPWM_XCMP1_SHDW2	500D E700h	5001 F700h	5005 F700h
704h	32	EPWM_XCMP2_SHDW2	500D E704h	5001 F704h	5005 F704h
708h	32	EPWM_XCMP3_SHDW2	500D E708h	5001 F708h	5005 F708h
70Ch	32	EPWM_XCMP4_SHDW2	500D E70Ch	5001 F70Ch	5005 F70Ch
710h	32	EPWM_XCMP5_SHDW2	500D E710h	5001 F710h	5005 F710h
714h	32	EPWM_XCMP6_SHDW2	500D E714h	5001 F714h	5005 F714h
718h	32	EPWM_XCMP7_SHDW2	500D E718h	5001 F718h	5005 F718h
71Ch	32	EPWM_XCMP8_SHDW2	500D E71Ch	5001 F71Ch	5005 F71Ch
720h	32	EPWM_XTBPRD_SHDW2	500D E720h	5001 F720h	5005 F720h
730h	16	EPWM_XAQCTLA_SHDW2	500D E730h	5001 F730h	5005 F730h
732h	16	EPWM_XAQCTLB_SHDW2	500D E732h	5001 F732h	5005 F732h
73Ah	16	EPWM_CMPC_SHDW2	500D E73Ah	5001 F73Ah	5005 F73Ah
73Eh	16	EPWM_CMPD_SHDW2	500D E73Eh	5001 F73Eh	5005 F73Eh
744h	32	EPWM_XMINMAX_SHDW2	500D E744h	5001 F744h	5005 F744h
780h	32	EPWM_XCMP1_SHDW3	500D E780h	5001 F780h	5005 F780h
784h	32	EPWM_XCMP2_SHDW3	500D E784h	5001 F784h	5005 F784h
788h	32	EPWM_XCMP3_SHDW3	500D E788h	5001 F788h	5005 F788h

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Table 3-611. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM27_G3 Physical Address	EPWM28_G3 Physical Address	EPWM29_G3 Physical Address
78Ch	32	EPWM_XCMP4_SHDW3	500D E78Ch	5001 F78Ch	5005 F78Ch
790h	32	EPWM_XCMP5_SHDW3	500D E790h	5001 F790h	5005 F790h
794h	32	EPWM_XCMP6_SHDW3	500D E794h	5001 F794h	5005 F794h
798h	32	EPWM_XCMP7_SHDW3	500D E798h	5001 F798h	5005 F798h
79Ch	32	EPWM_XCMP8_SHDW3	500D E79Ch	5001 F79Ch	5005 F79Ch
7A0h	32	EPWM_XTBPRD_SHDW3	500D E7A0h	5001 F7A0h	5005 F7A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	500D E7B0h	5001 F7B0h	5005 F7B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	500D E7B2h	5001 F7B2h	5005 F7B2h
7BAh	16	EPWM_CMPC_SHDW3	500D E7BAh	5001 F7BAh	5005 F7BAh
7BEh	16	EPWM_CMPD_SHDW3	500D E7BEh	5001 F7BEh	5005 F7BEh
7C4h	32	EPWM_XMINMAX_SHDW3	500D E7C4h	5001 F7C4h	5005 F7C4h
800h	32	EPWM_DECTL	500D E800h	5001 F800h	5005 F800h
804h	32	EPWM_DECOMPSEL	500D E804h	5001 F804h	5005 F804h
808h	32	EPWM_DEACTCTL	500D E808h	5001 F808h	5005 F808h
80Ch	32	EPWM_DESTS	500D E80Ch	5001 F80Ch	5005 F80Ch
810h	32	EPWM_DEFRC	500D E810h	5001 F810h	5005 F810h
814h	32	EPWM_DECLR	500D E814h	5001 F814h	5005 F814h
820h	32	EPWM_DEMONCNT	500D E820h	5001 F820h	5005 F820h
824h	32	EPWM_DEMONCTL	500D E824h	5001 F824h	5005 F824h
828h	32	EPWM_DEMONSTEP	500D E828h	5001 F828h	5005 F828h
82Ch	32	EPWM_DEMONTHRES	500D E82Ch	5001 F82Ch	5005 F82Ch
C00h	32	EPWM_MINDBCFG	500D EC00h	5001 FC00h	5005 FC00h
C04h	32	EPWM_MINDBDLY	500D EC04h	5001 FC04h	5005 FC04h
C20h	32	EPWM_LUTCTLA	500D EC20h	5001 FC20h	5005 FC20h
C24h	32	EPWM_LUTCTLB	500D EC24h	5001 FC24h	5005 FC24h

Table 3-612. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM30_G3 Physical Address	EPWM31_G3 Physical Address	EPWM_WLINK_G0 Physical Address
0h	16	EPWM_TBCTL	5009 F000h	500D F000h	5002 0000h
2h	16	EPWM_TBCTL2	5009 F002h	500D F002h	5002 0002h
6h	16	EPWM_EPWMSYNCINSEL	5009 F006h	500D F006h	5002 0006h
8h	16	EPWM_TBCTR	5009 F008h	500D F008h	5002 0008h
Ah	16	EPWM_TBSTS	5009 F00Ah	500D F00Ah	5002 000Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5009 F00Ch	500D F00Ch	5002 000Ch
Eh	16	EPWM_TBCTL3	5009 F00Eh	500D F00Eh	5002 000Eh
10h	16	EPWM_CMPCTL	5009 F010h	500D F010h	5002 0010h
12h	16	EPWM_CMPCTL2	5009 F012h	500D F012h	5002 0012h
18h	16	EPWM_DBCTL	5009 F018h	500D F018h	5002 0018h
1Ah	16	EPWM_DBCTL2	5009 F01Ah	500D F01Ah	5002 001Ah
20h	16	EPWM_AQCTL	5009 F020h	500D F020h	5002 0020h
22h	16	EPWM_AQTSRCSEL	5009 F022h	500D F022h	5002 0022h
28h	16	EPWM_PCCTL	5009 F028h	500D F028h	5002 0028h
30h	16	EPWM_VCAPCTL	5009 F030h	500D F030h	5002 0030h
32h	16	EPWM_VCNTCFG	5009 F032h	500D F032h	5002 0032h
40h	16	EPWM_HRCNFG	5009 F040h	500D F040h	5002 0040h

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Table 3-612. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM30_G3 Physical Address	EPWM31_G3 Physical Address	EPWM_WLINK_G0 Physical Address
4Eh	16	EPWM_HRCNFG2	5009 F04Eh	500D F04Eh	5002 004Eh
5Ah	16	EPWM_HRPCTL	5009 F05Ah	500D F05Ah	5002 005Ah
5Ch	16	EPWM_TRREM	5009 F05Ch	500D F05Ch	5002 005Ch
68h	16	EPWM_GLDCTL	5009 F068h	500D F068h	5002 0068h
6Ah	16	EPWM_GLDCFG	5009 F06Ah	500D F06Ah	5002 006Ah
70h	32	EPWM_EPWMXLINK	5009 F070h	500D F070h	5002 0070h
74h	32	EPWM_EPWMXLINK2	5009 F074h	500D F074h	5002 0074h
7Ah	16	EPWM_ETEST	5009 F07Ah	500D F07Ah	5002 007Ah
7Ch	16	EPWM_EPWMREV	5009 F07Ch	500D F07Ch	5002 007Ch
7Eh	16	EPWM_HRPWMREV	5009 F07Eh	500D F07Eh	5002 007Eh
80h	16	EPWM_AQCTLA	5009 F080h	500D F080h	5002 0080h
82h	16	EPWM_AQCTLA2	5009 F082h	500D F082h	5002 0082h
84h	16	EPWM_AQCTLB	5009 F084h	500D F084h	5002 0084h
86h	16	EPWM_AQCTLB2	5009 F086h	500D F086h	5002 0086h
8Eh	16	EPWM_AQSFRC	5009 F08Eh	500D F08Eh	5002 008Eh
92h	16	EPWM_AQCSFRC	5009 F092h	500D F092h	5002 0092h
A0h	16	EPWM_DBREDHR	5009 F0A0h	500D F0A0h	5002 00A0h
A2h	16	EPWM_DBRED	5009 F0A2h	500D F0A2h	5002 00A2h
A4h	16	EPWM_DBFEDHR	5009 F0A4h	500D F0A4h	5002 00A4h
A6h	16	EPWM_DBFED	5009 F0A6h	500D F0A6h	5002 00A6h
C0h	32	EPWM_TBPHS	5009 F0C0h	500D F0C0h	5002 00C0h
C4h	16	EPWM_TBPRDHR	5009 F0C4h	500D F0C4h	5002 00C4h
C6h	16	EPWM_TBPRD	5009 F0C6h	500D F0C6h	5002 00C6h
C8h	16	EPWM_TBPRDHRB	5009 F0C8h	500D F0C8h	5002 00C8h
D4h	32	EPWM_CMPA	5009 F0D4h	500D F0D4h	5002 00D4h
D8h	32	EPWM_CMPB	5009 F0D8h	500D F0D8h	5002 00D8h
DEh	16	EPWM_CMPC	5009 F0DEh	500D F0DEh	5002 00DEh
E2h	16	EPWM_CMPD	5009 F0E2h	500D F0E2h	5002 00E2h
E8h	16	EPWM_GLDCTL2	5009 F0E8h	500D F0E8h	5002 00E8h
EEh	16	EPWM_SWVDELVAL	5009 F0EEh	500D F0EEh	5002 00EEh
100h	16	EPWM_TZSEL	5009 F100h	500D F100h	5002 0100h
102h	16	EPWM_TZSEL2	5009 F102h	500D F102h	5002 0102h
104h	16	EPWM_TZDCSEL	5009 F104h	500D F104h	5002 0104h
108h	16	EPWM_TZCTL	5009 F108h	500D F108h	5002 0108h
10Ah	16	EPWM_TZCTL2	5009 F10Ah	500D F10Ah	5002 010Ah
10Ch	16	EPWM_TZCTLDCA	5009 F10Ch	500D F10Ch	5002 010Ch
10Eh	16	EPWM_TZCTLDCB	5009 F10Eh	500D F10Eh	5002 010Eh
11Ah	16	EPWM_TZEINT	5009 F11Ah	500D F11Ah	5002 011Ah
126h	16	EPWM_TZFLG	5009 F126h	500D F126h	5002 0126h
128h	16	EPWM_TZCBCFLG	5009 F128h	500D F128h	5002 0128h
12Ah	16	EPWM_TZOSTFLG	5009 F12Ah	500D F12Ah	5002 012Ah
12Eh	16	EPWM_TZCLR	5009 F12Eh	500D F12Eh	5002 012Eh
130h	16	EPWM_TZCBCCLR	5009 F130h	500D F130h	5002 0130h
132h	16	EPWM_TZOSTCLR	5009 F132h	500D F132h	5002 0132h
136h	16	EPWM_TZFRC	5009 F136h	500D F136h	5002 0136h
13Ah	16	EPWM_TZTRIPOUTSEL	5009 F13Ah	500D F13Ah	5002 013Ah

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Table 3-612. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM30_G3 Physical Address	EPWM31_G3 Physical Address	EPWM_WLINK_G0 Physical Address
148h	16	EPWM_ETSEL	5009 F148h	500D F148h	5002 0148h
14Ch	16	EPWM_ETPS	5009 F14Ch	500D F14Ch	5002 014Ch
150h	16	EPWM_ETFLG	5009 F150h	500D F150h	5002 0150h
154h	16	EPWM_ETCLR	5009 F154h	500D F154h	5002 0154h
158h	16	EPWM_ETFRC	5009 F158h	500D F158h	5002 0158h
15Ch	16	EPWM_ETINTPS	5009 F15Ch	500D F15Ch	5002 015Ch
160h	16	EPWM_ETSOCPS	5009 F160h	500D F160h	5002 0160h
164h	16	EPWM_ETCNTINITCTL	5009 F164h	500D F164h	5002 0164h
168h	16	EPWM_ETCNTINIT	5009 F168h	500D F168h	5002 0168h
16Ch	16	EPWM_ETINTMIXEN	5009 F16Ch	500D F16Ch	5002 016Ch
170h	16	EPWM_ETSOCAMIXEN	5009 F170h	500D F170h	5002 0170h
174h	16	EPWM_ETSOCBMIXEN	5009 F174h	500D F174h	5002 0174h
180h	16	EPWM_DCTRIPSEL	5009 F180h	500D F180h	5002 0180h
186h	16	EPWM_DCACTL	5009 F186h	500D F186h	5002 0186h
188h	16	EPWM_DCBCTL	5009 F188h	500D F188h	5002 0188h
18Eh	16	EPWM_DCFCTL	5009 F18Eh	500D F18Eh	5002 018Eh
190h	16	EPWM_DCCAPCTL	5009 F190h	500D F190h	5002 0190h
192h	16	EPWM_DCFOFFSET	5009 F192h	500D F192h	5002 0192h
194h	16	EPWM_DCFOFFSETCNT	5009 F194h	500D F194h	5002 0194h
196h	16	EPWM_DCFWINDOW	5009 F196h	500D F196h	5002 0196h
198h	16	EPWM_DCFWINDOWCNT	5009 F198h	500D F198h	5002 0198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5009 F19Ah	500D F19Ah	5002 019Ah
19Ch	16	EPWM_DCCAPMIXSEL	5009 F19Ch	500D F19Ch	5002 019Ch
19Eh	16	EPWM_DCCAP	5009 F19Eh	500D F19Eh	5002 019Eh
1A4h	16	EPWM_DCAHTRIPSEL	5009 F1A4h	500D F1A4h	5002 01A4h
1A6h	16	EPWM_DCALTRIPSEL	5009 F1A6h	500D F1A6h	5002 01A6h
1A8h	16	EPWM_DCBHTRIPSEL	5009 F1A8h	500D F1A8h	5002 01A8h
1AAh	16	EPWM_DCBLTRIPSEL	5009 F1AAh	500D F1AAh	5002 01AAh
1ACh	16	EPWM_CAPCTL	5009 F1ACh	500D F1ACh	5002 01ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5009 F1AEh	500D F1AEh	5002 01AEh
1B0h	16	EPWM_CAPINTRIPSEL	5009 F1B0h	500D F1B0h	5002 01B0h
1B2h	16	EPWM_CAPTRIPSEL	5009 F1B2h	500D F1B2h	5002 01B2h
1F4h	32	EPWM_EPWMLOCK	5009 F1F4h	500D F1F4h	5002 01F4h
1FAh	16	EPWM_HWVDELVAL	5009 F1FAh	500D F1FAh	5002 01FAh
1FCh	16	EPWM_VCNTVAL	5009 F1FCh	500D F1FCh	5002 01FCh
400h	32	EPWM_XCMPCTL1	5009 F400h	500D F400h	5002 0400h
410h	32	EPWM_XLOADCTL	5009 F410h	500D F410h	5002 0410h
418h	32	EPWM_XLOAD	5009 F418h	500D F418h	5002 0418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5009 F41Ch	500D F41Ch	5002 041Ch
420h	32	EPWM_XREGSHDW1STS	5009 F420h	500D F420h	5002 0420h
428h	32	EPWM_XREGSHDW2STS	5009 F428h	500D F428h	5002 0428h
430h	32	EPWM_XREGSHDW3STS	5009 F430h	500D F430h	5002 0430h
600h	32	EPWM_XCMP1_ACTIVE	5009 F600h	500D F600h	5002 0600h
604h	32	EPWM_XCMP2_ACTIVE	5009 F604h	500D F604h	5002 0604h
608h	32	EPWM_XCMP3_ACTIVE	5009 F608h	500D F608h	5002 0608h
60Ch	32	EPWM_XCMP4_ACTIVE	5009 F60Ch	500D F60Ch	5002 060Ch

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Table 3-612. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM30_G3 Physical Address	EPWM31_G3 Physical Address	EPWM_WLINK_G0 Physical Address
610h	32	EPWM_XCMP5_ACTIVE	5009 F610h	500D F610h	5002 0610h
614h	32	EPWM_XCMP6_ACTIVE	5009 F614h	500D F614h	5002 0614h
618h	32	EPWM_XCMP7_ACTIVE	5009 F618h	500D F618h	5002 0618h
61Ch	32	EPWM_XCMP8_ACTIVE	5009 F61Ch	500D F61Ch	5002 061Ch
620h	32	EPWM_XTBPRD_ACTIVE	5009 F620h	500D F620h	5002 0620h
630h	16	EPWM_XAQCTLA_ACTIVE	5009 F630h	500D F630h	5002 0630h
644h	32	EPWM_XMINMAX_ACTIVE	5009 F644h	500D F644h	5002 0644h
680h	32	EPWM_XCMP1_SHDW1	5009 F680h	500D F680h	5002 0680h
684h	32	EPWM_XCMP2_SHDW1	5009 F684h	500D F684h	5002 0684h
688h	32	EPWM_XCMP3_SHDW1	5009 F688h	500D F688h	5002 0688h
68Ch	32	EPWM_XCMP4_SHDW1	5009 F68Ch	500D F68Ch	5002 068Ch
690h	32	EPWM_XCMP5_SHDW1	5009 F690h	500D F690h	5002 0690h
694h	32	EPWM_XCMP6_SHDW1	5009 F694h	500D F694h	5002 0694h
698h	32	EPWM_XCMP7_SHDW1	5009 F698h	500D F698h	5002 0698h
69Ch	32	EPWM_XCMP8_SHDW1	5009 F69Ch	500D F69Ch	5002 069Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5009 F6A0h	500D F6A0h	5002 06A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5009 F6B0h	500D F6B0h	5002 06B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5009 F6B2h	500D F6B2h	5002 06B2h
6BAh	16	EPWM_CMPC_SHDW1	5009 F6BAh	500D F6BAh	5002 06BAh
6BEh	16	EPWM_CMPD_SHDW1	5009 F6BEh	500D F6BEh	5002 06BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5009 F6C4h	500D F6C4h	5002 06C4h
700h	32	EPWM_XCMP1_SHDW2	5009 F700h	500D F700h	5002 0700h
704h	32	EPWM_XCMP2_SHDW2	5009 F704h	500D F704h	5002 0704h
708h	32	EPWM_XCMP3_SHDW2	5009 F708h	500D F708h	5002 0708h
70Ch	32	EPWM_XCMP4_SHDW2	5009 F70Ch	500D F70Ch	5002 070Ch
710h	32	EPWM_XCMP5_SHDW2	5009 F710h	500D F710h	5002 0710h
714h	32	EPWM_XCMP6_SHDW2	5009 F714h	500D F714h	5002 0714h
718h	32	EPWM_XCMP7_SHDW2	5009 F718h	500D F718h	5002 0718h
71Ch	32	EPWM_XCMP8_SHDW2	5009 F71Ch	500D F71Ch	5002 071Ch
720h	32	EPWM_XTBPRD_SHDW2	5009 F720h	500D F720h	5002 0720h
730h	16	EPWM_XAQCTLA_SHDW2	5009 F730h	500D F730h	5002 0730h
732h	16	EPWM_XAQCTLB_SHDW2	5009 F732h	500D F732h	5002 0732h
73Ah	16	EPWM_CMPC_SHDW2	5009 F73Ah	500D F73Ah	5002 073Ah
73Eh	16	EPWM_CMPD_SHDW2	5009 F73Eh	500D F73Eh	5002 073Eh
744h	32	EPWM_XMINMAX_SHDW2	5009 F744h	500D F744h	5002 0744h
780h	32	EPWM_XCMP1_SHDW3	5009 F780h	500D F780h	5002 0780h
784h	32	EPWM_XCMP2_SHDW3	5009 F784h	500D F784h	5002 0784h
788h	32	EPWM_XCMP3_SHDW3	5009 F788h	500D F788h	5002 0788h
78Ch	32	EPWM_XCMP4_SHDW3	5009 F78Ch	500D F78Ch	5002 078Ch
790h	32	EPWM_XCMP5_SHDW3	5009 F790h	500D F790h	5002 0790h
794h	32	EPWM_XCMP6_SHDW3	5009 F794h	500D F794h	5002 0794h
798h	32	EPWM_XCMP7_SHDW3	5009 F798h	500D F798h	5002 0798h
79Ch	32	EPWM_XCMP8_SHDW3	5009 F79Ch	500D F79Ch	5002 079Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5009 F7A0h	500D F7A0h	5002 07A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5009 F7B0h	500D F7B0h	5002 07B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5009 F7B2h	500D F7B2h	5002 07B2h

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Table 3-612. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM30_G3 Physical Address	EPWM31_G3 Physical Address	EPWM_WLINK_G0 Physical Address
7BAh	16	EPWM_CMPC_SHDW3	5009 F7BAh	500D F7BAh	5002 07BAh
7BEh	16	EPWM_CMPD_SHDW3	5009 F7BEh	500D F7BEh	5002 07BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5009 F7C4h	500D F7C4h	5002 07C4h
800h	32	EPWM_DECTL	5009 F800h	500D F800h	5002 0800h
804h	32	EPWM_DECOMPSEL	5009 F804h	500D F804h	5002 0804h
808h	32	EPWM_DEACTCTL	5009 F808h	500D F808h	5002 0808h
80Ch	32	EPWM_DESTS	5009 F80Ch	500D F80Ch	5002 080Ch
810h	32	EPWM_DEFRC	5009 F810h	500D F810h	5002 0810h
814h	32	EPWM_DECLR	5009 F814h	500D F814h	5002 0814h
820h	32	EPWM_DEMONCNT	5009 F820h	500D F820h	5002 0820h
824h	32	EPWM_DEMONCTL	5009 F824h	500D F824h	5002 0824h
828h	32	EPWM_DEMONSTEP	5009 F828h	500D F828h	5002 0828h
82Ch	32	EPWM_DEMONTHRES	5009 F82Ch	500D F82Ch	5002 082Ch
C00h	32	EPWM_MINDBCFG	5009 FC00h	500D FC00h	5002 0C00h
C04h	32	EPWM_MINDBDLY	5009 FC04h	500D FC04h	5002 0C04h
C20h	32	EPWM_LUTCTLA	5009 FC20h	500D FC20h	5002 0C20h
C24h	32	EPWM_LUTCTLB	5009 FC24h	500D FC24h	5002 0C24h

Table 3-613. EPWM Registers, Base Address=5000 0000h, Length=4096

Offset	Length	Register Name	EPWM_WLINK_G1 Physical Address	EPWM_WLINK_G2 Physical Address	EPWM_WLINK_G3 Physical Address
0h	16	EPWM_TBCTL	5006 0000h	500A 0000h	500E 0000h
2h	16	EPWM_TBCTL2	5006 0002h	500A 0002h	500E 0002h
6h	16	EPWM_EPWMSYNCINSEL	5006 0006h	500A 0006h	500E 0006h
8h	16	EPWM_TBCTR	5006 0008h	500A 0008h	500E 0008h
Ah	16	EPWM_TBSTS	5006 000Ah	500A 000Ah	500E 000Ah
Ch	16	EPWM_EPWMSYNCOUTEN	5006 000Ch	500A 000Ch	500E 000Ch
Eh	16	EPWM_TBCTL3	5006 000Eh	500A 000Eh	500E 000Eh
10h	16	EPWM_CMPCTL	5006 0010h	500A 0010h	500E 0010h
12h	16	EPWM_CMPCTL2	5006 0012h	500A 0012h	500E 0012h
18h	16	EPWM_DBCTL	5006 0018h	500A 0018h	500E 0018h
1Ah	16	EPWM_DBCTL2	5006 001Ah	500A 001Ah	500E 001Ah
20h	16	EPWM_AQCTL	5006 0020h	500A 0020h	500E 0020h
22h	16	EPWM_AQTSRCSEL	5006 0022h	500A 0022h	500E 0022h
28h	16	EPWM_PCCTL	5006 0028h	500A 0028h	500E 0028h
30h	16	EPWM_VCAPCTL	5006 0030h	500A 0030h	500E 0030h
32h	16	EPWM_VCNTCFG	5006 0032h	500A 0032h	500E 0032h
40h	16	EPWM_HRCNFG	5006 0040h	500A 0040h	500E 0040h
4Eh	16	EPWM_HRCNFG2	5006 004Eh	500A 004Eh	500E 004Eh
5Ah	16	EPWM_HRPCTL	5006 005Ah	500A 005Ah	500E 005Ah
5Ch	16	EPWM_TRREM	5006 005Ch	500A 005Ch	500E 005Ch
68h	16	EPWM_GLDCTL	5006 0068h	500A 0068h	500E 0068h
6Ah	16	EPWM_GLDCFG	5006 006Ah	500A 006Ah	500E 006Ah
70h	32	EPWM_EPWMXLINK	5006 0070h	500A 0070h	500E 0070h
74h	32	EPWM_EPWMXLINK2	5006 0074h	500A 0074h	500E 0074h
7Ah	16	EPWM_ETEST	5006 007Ah	500A 007Ah	500E 007Ah

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Table 3-613. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM_WLINK_G1 Physical Address	EPWM_WLINK_G2 Physical Address	EPWM_WLINK_G3 Physical Address
7Ch	16	EPWM_EPWMREV	5006 007Ch	500A 007Ch	500E 007Ch
7Eh	16	EPWM_HRPWMREV	5006 007Eh	500A 007Eh	500E 007Eh
80h	16	EPWM_AQCTLA	5006 0080h	500A 0080h	500E 0080h
82h	16	EPWM_AQCTLA2	5006 0082h	500A 0082h	500E 0082h
84h	16	EPWM_AQCTLB	5006 0084h	500A 0084h	500E 0084h
86h	16	EPWM_AQCTLB2	5006 0086h	500A 0086h	500E 0086h
8Eh	16	EPWM_AQSFRC	5006 008Eh	500A 008Eh	500E 008Eh
92h	16	EPWM_AQCSFRC	5006 0092h	500A 0092h	500E 0092h
A0h	16	EPWM_DBREDHR	5006 00A0h	500A 00A0h	500E 00A0h
A2h	16	EPWM_DBRED	5006 00A2h	500A 00A2h	500E 00A2h
A4h	16	EPWM_DBFEDHR	5006 00A4h	500A 00A4h	500E 00A4h
A6h	16	EPWM_DBFED	5006 00A6h	500A 00A6h	500E 00A6h
C0h	32	EPWM_TBPHS	5006 00C0h	500A 00C0h	500E 00C0h
C4h	16	EPWM_TBPRDHR	5006 00C4h	500A 00C4h	500E 00C4h
C6h	16	EPWM_TBPRD	5006 00C6h	500A 00C6h	500E 00C6h
C8h	16	EPWM_TBPRDHRB	5006 00C8h	500A 00C8h	500E 00C8h
D4h	32	EPWM_CMPA	5006 00D4h	500A 00D4h	500E 00D4h
D8h	32	EPWM_CMPB	5006 00D8h	500A 00D8h	500E 00D8h
DEh	16	EPWM_CMPC	5006 00DEh	500A 00DEh	500E 00DEh
E2h	16	EPWM_CMPD	5006 00E2h	500A 00E2h	500E 00E2h
E8h	16	EPWM_GLDCTL2	5006 00E8h	500A 00E8h	500E 00E8h
EEh	16	EPWM_SWVDELVAL	5006 00EEh	500A 00EEh	500E 00EEh
100h	16	EPWM_TZSEL	5006 0100h	500A 0100h	500E 0100h
102h	16	EPWM_TZSEL2	5006 0102h	500A 0102h	500E 0102h
104h	16	EPWM_TZDCSEL	5006 0104h	500A 0104h	500E 0104h
108h	16	EPWM_TZCTL	5006 0108h	500A 0108h	500E 0108h
10Ah	16	EPWM_TZCTL2	5006 010Ah	500A 010Ah	500E 010Ah
10Ch	16	EPWM_TZCTLDCA	5006 010Ch	500A 010Ch	500E 010Ch
10Eh	16	EPWM_TZCTLDCB	5006 010Eh	500A 010Eh	500E 010Eh
11Ah	16	EPWM_TZEINT	5006 011Ah	500A 011Ah	500E 011Ah
126h	16	EPWM_TZFLG	5006 0126h	500A 0126h	500E 0126h
128h	16	EPWM_TZCBCFLG	5006 0128h	500A 0128h	500E 0128h
12Ah	16	EPWM_TZOSTFLG	5006 012Ah	500A 012Ah	500E 012Ah
12Eh	16	EPWM_TZCLR	5006 012Eh	500A 012Eh	500E 012Eh
130h	16	EPWM_TZCBCCLR	5006 0130h	500A 0130h	500E 0130h
132h	16	EPWM_TZOSTCLR	5006 0132h	500A 0132h	500E 0132h
136h	16	EPWM_TZFRC	5006 0136h	500A 0136h	500E 0136h
13Ah	16	EPWM_TZTRIPOUTSEL	5006 013Ah	500A 013Ah	500E 013Ah
148h	16	EPWM_ETSEL	5006 0148h	500A 0148h	500E 0148h
14Ch	16	EPWM_ETPS	5006 014Ch	500A 014Ch	500E 014Ch
150h	16	EPWM_ETFLG	5006 0150h	500A 0150h	500E 0150h
154h	16	EPWM_ETCLR	5006 0154h	500A 0154h	500E 0154h
158h	16	EPWM_ETFRC	5006 0158h	500A 0158h	500E 0158h
15Ch	16	EPWM_ETINTPS	5006 015Ch	500A 015Ch	500E 015Ch
160h	16	EPWM_ETSOCPS	5006 0160h	500A 0160h	500E 0160h
164h	16	EPWM_ETCNTINITCTL	5006 0164h	500A 0164h	500E 0164h

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Table 3-613. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM_WLINK_G1 Physical Address	EPWM_WLINK_G2 Physical Address	EPWM_WLINK_G3 Physical Address
168h	16	EPWM_ETCNTINIT	5006 0168h	500A 0168h	500E 0168h
16Ch	16	EPWM_ETINTMIXEN	5006 016Ch	500A 016Ch	500E 016Ch
170h	16	EPWM_ETSOCAMIXEN	5006 0170h	500A 0170h	500E 0170h
174h	16	EPWM_ETSOCBMIXEN	5006 0174h	500A 0174h	500E 0174h
180h	16	EPWM_DCTRIPSEL	5006 0180h	500A 0180h	500E 0180h
186h	16	EPWM_DCACTL	5006 0186h	500A 0186h	500E 0186h
188h	16	EPWM_DCBCTL	5006 0188h	500A 0188h	500E 0188h
18Eh	16	EPWM_DCFCTL	5006 018Eh	500A 018Eh	500E 018Eh
190h	16	EPWM_DCCAPCTL	5006 0190h	500A 0190h	500E 0190h
192h	16	EPWM_DCFOFFSET	5006 0192h	500A 0192h	500E 0192h
194h	16	EPWM_DCFOFFSETCNT	5006 0194h	500A 0194h	500E 0194h
196h	16	EPWM_DCFWINDOW	5006 0196h	500A 0196h	500E 0196h
198h	16	EPWM_DCFWINDOWCNT	5006 0198h	500A 0198h	500E 0198h
19Ah	16	EPWM_BLANKPULSEMIXSEL	5006 019Ah	500A 019Ah	500E 019Ah
19Ch	16	EPWM_DCCAPMIXSEL	5006 019Ch	500A 019Ch	500E 019Ch
19Eh	16	EPWM_DCCAP	5006 019Eh	500A 019Eh	500E 019Eh
1A4h	16	EPWM_DCAHTRIPSEL	5006 01A4h	500A 01A4h	500E 01A4h
1A6h	16	EPWM_DCALTRIPSEL	5006 01A6h	500A 01A6h	500E 01A6h
1A8h	16	EPWM_DCBHTRIPSEL	5006 01A8h	500A 01A8h	500E 01A8h
1AAh	16	EPWM_DCBLTRIPSEL	5006 01AAh	500A 01AAh	500E 01AAh
1ACh	16	EPWM_CAPCTL	5006 01ACh	500A 01ACh	500E 01ACh
1AEh	16	EPWM_CAPGATETRIPSEL	5006 01AEh	500A 01AEh	500E 01AEh
1B0h	16	EPWM_CAPINTRIPSEL	5006 01B0h	500A 01B0h	500E 01B0h
1B2h	16	EPWM_CAPTRIPSEL	5006 01B2h	500A 01B2h	500E 01B2h
1F4h	32	EPWM_EPWMLOCK	5006 01F4h	500A 01F4h	500E 01F4h
1FAh	16	EPWM_HWVDELVAL	5006 01FAh	500A 01FAh	500E 01FAh
1FCh	16	EPWM_VCNTVAL	5006 01FCh	500A 01FCh	500E 01FCh
400h	32	EPWM_XCMPCTL1	5006 0400h	500A 0400h	500E 0400h
410h	32	EPWM_XLOADCTL	5006 0410h	500A 0410h	500E 0410h
418h	32	EPWM_XLOAD	5006 0418h	500A 0418h	500E 0418h
41Ch	32	EPWM_EPWMXLINKXLOAD	5006 041Ch	500A 041Ch	500E 041Ch
420h	32	EPWM_XREGSHDW1STS	5006 0420h	500A 0420h	500E 0420h
428h	32	EPWM_XREGSHDW2STS	5006 0428h	500A 0428h	500E 0428h
430h	32	EPWM_XREGSHDW3STS	5006 0430h	500A 0430h	500E 0430h
600h	32	EPWM_XCMP1_ACTIVE	5006 0600h	500A 0600h	500E 0600h
604h	32	EPWM_XCMP2_ACTIVE	5006 0604h	500A 0604h	500E 0604h
608h	32	EPWM_XCMP3_ACTIVE	5006 0608h	500A 0608h	500E 0608h
60Ch	32	EPWM_XCMP4_ACTIVE	5006 060Ch	500A 060Ch	500E 060Ch
610h	32	EPWM_XCMP5_ACTIVE	5006 0610h	500A 0610h	500E 0610h
614h	32	EPWM_XCMP6_ACTIVE	5006 0614h	500A 0614h	500E 0614h
618h	32	EPWM_XCMP7_ACTIVE	5006 0618h	500A 0618h	500E 0618h
61Ch	32	EPWM_XCMP8_ACTIVE	5006 061Ch	500A 061Ch	500E 061Ch
620h	32	EPWM_XTBPRD_ACTIVE	5006 0620h	500A 0620h	500E 0620h
630h	16	EPWM_XAQCTLA_ACTIVE	5006 0630h	500A 0630h	500E 0630h
644h	32	EPWM_XMINMAX_ACTIVE	5006 0644h	500A 0644h	500E 0644h
680h	32	EPWM_XCMP1_SHDW1	5006 0680h	500A 0680h	500E 0680h

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Table 3-613. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM_WLINK_G1 Physical Address	EPWM_WLINK_G2 Physical Address	EPWM_WLINK_G3 Physical Address
684h	32	EPWM_XCMP2_SHDW1	5006 0684h	500A 0684h	500E 0684h
688h	32	EPWM_XCMP3_SHDW1	5006 0688h	500A 0688h	500E 0688h
68Ch	32	EPWM_XCMP4_SHDW1	5006 068Ch	500A 068Ch	500E 068Ch
690h	32	EPWM_XCMP5_SHDW1	5006 0690h	500A 0690h	500E 0690h
694h	32	EPWM_XCMP6_SHDW1	5006 0694h	500A 0694h	500E 0694h
698h	32	EPWM_XCMP7_SHDW1	5006 0698h	500A 0698h	500E 0698h
69Ch	32	EPWM_XCMP8_SHDW1	5006 069Ch	500A 069Ch	500E 069Ch
6A0h	32	EPWM_XTBPRD_SHDW1	5006 06A0h	500A 06A0h	500E 06A0h
6B0h	16	EPWM_XAQCTLA_SHDW1	5006 06B0h	500A 06B0h	500E 06B0h
6B2h	16	EPWM_XAQCTLB_SHDW1	5006 06B2h	500A 06B2h	500E 06B2h
6BAh	16	EPWM_CMPC_SHDW1	5006 06BAh	500A 06BAh	500E 06BAh
6BEh	16	EPWM_CMPD_SHDW1	5006 06BEh	500A 06BEh	500E 06BEh
6C4h	32	EPWM_XMINMAX_SHDW1	5006 06C4h	500A 06C4h	500E 06C4h
700h	32	EPWM_XCMP1_SHDW2	5006 0700h	500A 0700h	500E 0700h
704h	32	EPWM_XCMP2_SHDW2	5006 0704h	500A 0704h	500E 0704h
708h	32	EPWM_XCMP3_SHDW2	5006 0708h	500A 0708h	500E 0708h
70Ch	32	EPWM_XCMP4_SHDW2	5006 070Ch	500A 070Ch	500E 070Ch
710h	32	EPWM_XCMP5_SHDW2	5006 0710h	500A 0710h	500E 0710h
714h	32	EPWM_XCMP6_SHDW2	5006 0714h	500A 0714h	500E 0714h
718h	32	EPWM_XCMP7_SHDW2	5006 0718h	500A 0718h	500E 0718h
71Ch	32	EPWM_XCMP8_SHDW2	5006 071Ch	500A 071Ch	500E 071Ch
720h	32	EPWM_XTBPRD_SHDW2	5006 0720h	500A 0720h	500E 0720h
730h	16	EPWM_XAQCTLA_SHDW2	5006 0730h	500A 0730h	500E 0730h
732h	16	EPWM_XAQCTLB_SHDW2	5006 0732h	500A 0732h	500E 0732h
73Ah	16	EPWM_CMPC_SHDW2	5006 073Ah	500A 073Ah	500E 073Ah
73Eh	16	EPWM_CMPD_SHDW2	5006 073Eh	500A 073Eh	500E 073Eh
744h	32	EPWM_XMINMAX_SHDW2	5006 0744h	500A 0744h	500E 0744h
780h	32	EPWM_XCMP1_SHDW3	5006 0780h	500A 0780h	500E 0780h
784h	32	EPWM_XCMP2_SHDW3	5006 0784h	500A 0784h	500E 0784h
788h	32	EPWM_XCMP3_SHDW3	5006 0788h	500A 0788h	500E 0788h
78Ch	32	EPWM_XCMP4_SHDW3	5006 078Ch	500A 078Ch	500E 078Ch
790h	32	EPWM_XCMP5_SHDW3	5006 0790h	500A 0790h	500E 0790h
794h	32	EPWM_XCMP6_SHDW3	5006 0794h	500A 0794h	500E 0794h
798h	32	EPWM_XCMP7_SHDW3	5006 0798h	500A 0798h	500E 0798h
79Ch	32	EPWM_XCMP8_SHDW3	5006 079Ch	500A 079Ch	500E 079Ch
7A0h	32	EPWM_XTBPRD_SHDW3	5006 07A0h	500A 07A0h	500E 07A0h
7B0h	16	EPWM_XAQCTLA_SHDW3	5006 07B0h	500A 07B0h	500E 07B0h
7B2h	16	EPWM_XAQCTLB_SHDW3	5006 07B2h	500A 07B2h	500E 07B2h
7BAh	16	EPWM_CMPC_SHDW3	5006 07BAh	500A 07BAh	500E 07BAh
7BEh	16	EPWM_CMPD_SHDW3	5006 07BEh	500A 07BEh	500E 07BEh
7C4h	32	EPWM_XMINMAX_SHDW3	5006 07C4h	500A 07C4h	500E 07C4h
800h	32	EPWM_DECTL	5006 0800h	500A 0800h	500E 0800h
804h	32	EPWM_DECOMPSEL	5006 0804h	500A 0804h	500E 0804h
808h	32	EPWM_DEACTCTL	5006 0808h	500A 0808h	500E 0808h
80Ch	32	EPWM_DESTS	5006 080Ch	500A 080Ch	500E 080Ch
810h	32	EPWM_DEFRC	5006 0810h	500A 0810h	500E 0810h

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Table 3-613. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)

Offset	Length	Register Name	EPWM_WLINK_G1 Physical Address	EPWM_WLINK_G2 Physical Address	EPWM_WLINK_G3 Physical Address
814h	32	EPWM_DECLR	5006 0814h	500A 0814h	500E 0814h
820h	32	EPWM_DEMONCNT	5006 0820h	500A 0820h	500E 0820h
824h	32	EPWM_DEMONCTL	5006 0824h	500A 0824h	500E 0824h
828h	32	EPWM_DEMONSTEP	5006 0828h	500A 0828h	500E 0828h
82Ch	32	EPWM_DEMONTHRES	5006 082Ch	500A 082Ch	500E 082Ch
C00h	32	EPWM_MINDBCFG	5006 0C00h	500A 0C00h	500E 0C00h
C04h	32	EPWM_MINDBDLY	5006 0C04h	500A 0C04h	500E 0C04h
C20h	32	EPWM_LUTCTLA	5006 0C20h	500A 0C20h	500E 0C20h
C24h	32	EPWM_LUTCTLB	5006 0C24h	500A 0C24h	500E 0C24h

3.8.2 EPWM Registers

EPWM Registers

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3.8.2.1 EPWM_TBCTL Register

3.8.2.1.1 EPWM_TBCTL Register (Offset = 0h) [reset = 83h]

Time Base Control Register.

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Figure 3-273. EPWM_TBCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PHSDIR	CLKDIV			HSPCLKDIV	
R/W		R/W	R/W			R/W	
0h		0h	0h			1h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HSPCLKDIV	SWFSYNC	RESERVED_1		PRDLD	PHSEN	CTRMODE	
R/W	R/W1TS	R		R/W	R/W	R/W	
1h	0h	0h		0h	0h	3h	

Table 3-614. EPWM_TBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation Mode Bits. These bits select the behavior of the EPWM time-base counter during emulation events 00:Stop after the next time-base counter increment or decrement 01:Stop when counter completes a whole cycle: - Up-count mode: stop when the time-base counter = period [TBCTR = TBPRD] - Down-count mode: stop when the time-base counter = 0x00 [TBCTR = 0x00] - Up-down-count mode: stop when the time-base counter = 0x00 [TBCTR = 0x00] 1x: Free run
13	PHSDIR	R/W	0h	Phase Direction Bit This bit is only used when the time-base counter is configured in the up-down-count mode. The PHSDIR bit indicates the direction the time-base counter [TBCTR] will count after a synchronization event occurs and a new phase value is loaded from the phase [TBPHS] register. This is irrespective of the direction of the counter before the synchronization event.. In the up-count and down-count modes this bit is ignored. 0:Count down after the synchronization event. 1:Count up after the synchronization event.
12:10	CLKDIV	R/W	0h	Time Base Clock Pre-Scale Bits These bits select the time base clock pre-scale value [TBCLK = EPWMCLK/[HSPCLKDIV * CLKDIV]: 000:/1 [default on reset] 001:/2 010:/4 011:/8 100:/16 101:/32 110:/64 111:/128

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Table 3-614. EPWM_TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:7	HSPCLKDIV	R/W	1h	High Speed Time Base Clock Pre-Scale Bits These bits determine part of the time-base clock prescale value. TBCLK = EPWMCLK / [HSPCLKDIV x CLKDIV]. This divisor emulates the HSPCLK in the TMS320x281x system as used on the Event Manager [EV] peripheral. 000:/1 001:/2 [default on reset] 010:/4 011:/6 100:/8 101:/10 110:/12 111:/14
6	SWFSYNC	R/W1TS	0h	Software Forced Sync Pulse 0:Writing a 0 has no effect and reads always return a 0. 1:Writing a 1 forces a one-time synchronization pulse to be generated. SWFSYNC can be enabled to effect EPWMxSYNCO by setting the EPWMSYNCOUTEN.SWEN bit.
5:4	RESERVED_1	R	0h	Reserved
3	PRDLD	R/W	0h	Active Period Reg Load from Shadow Select 0:The period register [TBPRD] is loaded from its shadow register when the time-base counter, TBCTR, is equal to zero and/or a sync event as determined by the TBCTL2[PRDLDSYNC] bit. A write/read to the TBPRD register accesses the shadow register. 1: Immediate Mode [Shadow register bypassed]: A write or read to the TBPRD register accesses the active register.
2	PHSEN	R/W	0h	Counter Reg Load from Phase Reg Enable 0:Do not load the time-base counter [TBCTR] from the time-base phase register [TBPHS]. 1:Allow Counter to be loaded from the Phase register [TBPHS] and shadow to active load events when an EPWMxSYNCI input signal occurs or a software-forced sync signal, see bit 6.
1:0	CTRMODE	R/W	3h	Counter Mode The time-base counter mode is normally configured once and not changed during normal operation. If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change. These bits set the time-base counter mode of operation as follows: 00:Up-count mode 01:Down-count mode 10:Up-down count mode 11:Freeze counter operation [default on reset]

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3.8.2.2 EPWM_TBCTL2 Register

3.8.2.2.1 EPWM_TBCTL2 Register (Offset = 2h) [reset = 0h]

Time Base Control Register 2

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Figure 3-274. EPWM_TBCTL2 Name Register

15	14	13	12	11	10	9	8
PRDLDSYNC		RESERVED_3		RESERVED_2			
R/W		R		R			
0h		0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OSHTSYNC	OSHTSYNCMODE	SELFCLRTRREM	RESERVED_1				
R/W1TS	R/W	R/W	R				
0h	0h	0h	0h				

Table 3-615. EPWM_TBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	PRDLDSYNC	R/W	0h	Shadow to Active Period Register Load on SYNC event 00:Shadow to Active Load of TBPRD occurs only when TBCTR = 0 [same as legacy]. 01:Shadow to Active Load of TBPRD occurs both when TBCTR = 0 and when SYNC occurs. 10:Shadow to Active Load of TBPRD occurs only when a SYNC is received. 11:Reserved Note: This bit selection is valid only if TBCTL[PRDLD]=0.
13:12	RESERVED_3	R	0h	Reserved
11:8	RESERVED_2	R	0h	Reserved
7	OSHTSYNC	R/W1TS	0h	Oneshot sync bit 0:Writing a '0' has no effect. 1:Allow one sync pulse to propogate.
6	OSHTSYNCMODE	R/W	0h	Oneshot sync enable bit 0:Oneshot sync mode disabled 1:Oneshot sync mode enabled
5	SELFCLRTRREM	R/W	0h	Loop back sync pulse to enable self sync operation 0:Self clear function of TRREM disabled. 1:Self clear function of TRREM enabled
4:0	RESERVED_1	R	0h	Reserved

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3.8.2.3 EPWM_EPWMSYNCINSEL Register

3.8.2.3.1 EPWM_EPWMSYNCINSEL Register (Offset = 6h) [reset = 1h]

EPWMxSYNCIN Source Select Register.

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Figure 3-275. EPWM_EPWMSYNCINSEL Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED_1</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED_1</td><td colspan="7">SEL</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">1h</td></tr>
</table>

Table 3-616. EPWM_EPWMSYNCINSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved

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Table 3-616. EPWM_EPWMSYNCINSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	SEL	R/W	1h	These bits determine the source of the EPWMxSYNCI signal 0x0: Disabled 0x01: EPWM0.SYNCOUT . 0x10: EPWM15.SYNCOUT 0x11:EPWM16.SYNCOUT . 0x20: EPWM31.SYNCOUT 0x21: Reserved . 0x40: ECAP0.SYNCOUT . 0x49: ECAP9.SYNCOUT 0x4A: Reserved . 0x4F: Reserved 0x50: InputXBAR.Out[4] 0x51: InputXBAR.Out[20] 0x52: Reserved . 0x57: Reserved 0x58: SOC_TIMESYNC_XBAR0.SYNCPWMOut0 0x59: SOC_TIMESYNC_XBAR0.SYNCPWMOut1 0x5A: Reserved 0x5F: Reserved 0x60: FSIRX0.RXTRIG[0] 0x61: FSIRX0.RXTRIG[1] 0x62: FSIRX0.RXTRIG[2] 0x63: FSIRX0.RXTRIG[3] 0x64: FSIRX1.RXTRIG[0] 0x65: FSIRX1.RXTRIG[1] 0x66: FSIRX1.RXTRIG[2] 0x67: FSIRX1.RXTRIG[3] 0x68: FSIRX2.RXTRIG[0] 0x69: FSIRX2.RXTRIG[1] 0x6A: FSIRX2.RXTRIG[2] 0x6B: FSIRX2.RXTRIG[3] 0x6C: FSIRX3.RXTRIG[0] 0x6D: FSIRX3.RXTRIG[1] 0x6E: FSIRX3.RXTRIG[2] 0x6F: FSIRX3.RXTRIG[3] 0x70: Reserved . 0x7F: Reserved

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3.8.2.4 EPWM_TBCTR Register

3.8.2.4.1 EPWM_TBCTR Register (Offset = 8h) [reset = 0h]

Time Base Counter Register.

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Figure 3-276. EPWM_TBCTR Name Register

15	14	13	12	11	10	9	8
TBCTR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBCTR							
R/W							
0h							

Table 3-617. EPWM_TBCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBCTR	R/W	0h	Time Base Counter Register

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3.8.2.5 EPWM_TBSTS Register

3.8.2.5.1 EPWM_TBSTS Register (Offset = Ah) [reset = 1h]

Time Base Status Register.

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Figure 3-277. EPWM_TBSTS Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1					CTRMAX	SYNCI	CTRDIR
R					R/W1TC	R/W1TC	R
0h					0h	0h	1h

Table 3-618. EPWM_TBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED_1	R	0h	Reserved
2	CTRMAX	R/W1TC	0h	Time-Base Counter Max Latched Status Bit 0:Reading a 0 indicates the time-base counter never reached its maximum value. Writing a 0 will have no effect. 1:Reading a 1 on this bit indicates that the time-base counter reached the max value 0xFFFF. Writing a 1 to this bit will clear the latched event.
1	SYNCI	R/W1TC	0h	Input Synchronization Latched Status Bit 0:Writing a 0 will have no effect. Reading a 0 indicates no external synchronization event has occurred. 1:Reading a 1 on this bit indicates that an external synchronization event has occurred [EPWMxSYNCI]. Writing a 1 to this bit will clear the latched event.
0	CTRDIR	R	1h	Time Base Counter Direction Status Bit 0:Time-Base Counter is currently counting down. 1:Time-Base Counter is currently counting up. Note: This bit is only valid when the counter is not frozen.

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3.8.2.6 EPWM_EPWMSYNCOUTEN Register

3.8.2.6.1 EPWM_EPWMSYNCOUTEN Register (Offset = Ch) [reset = 1h]

EPWMxSYNCOUT Source Enable Register.

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Figure 3-278. EPWM_EPWMSYNCOUTEN Name Register

15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	DCBEVT1EN	DCAEVT1EN	CMPDEN	CMPCEN	CMPBEN	ZEROEN	SWEN
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	1h

Table 3-619. EPWM_EPWMSYNCOUTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_2	R	0h	Reserved
7	RESERVED_1	R	0h	Reserved
6	DCBEVT1EN	R/W	0h	This bit enables the DCBEVT1.sync event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a DCBEVT1.sync event
5	DCAEVT1EN	R/W	0h	This bit enables the DCAEVT1.sync event to set the EPWMxSYNCOUT signal. 0 Disabled 1 The EPWMxSYNCOUT signal is pulsed for one PWM clock period upon a DCAEVT1.sync event
4	CMPDEN	R/W	0h	This bit enables the TBCTR = CMPD event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare D event [TBCTR = CMPD]
3	CMPCEN	R/W	0h	This bit enables the TBCTR = CMPC event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare C event [TBCTR = CMPC]
2	CMPBEN	R/W	0h	This bit enables the TBCTR = CMPB event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare B event [TBCTR = CMPB]
1	ZEROEN	R/W	0h	This bit enables the TBCTR = 0x0000 event to set the EPWMxSYNCOUT signal. 0 Disabled 1 The EPWMxSYNCOUT signal is pulsed for one PWM clock period upon the value of TBCTR changing to 0x0000

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Table 3-619. EPWM_EPWMSYNCOUTEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SWEN	R/W	1h	This bit enables the TBCTL.SWFSYNC bit to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period when the TBCTL.SWFSYNC bit is set

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3.8.2.7 EPWM_TBCTL3 Register

3.8.2.7.1 EPWM_TBCTL3 Register (Offset = Eh) [reset = 0h]

Time Base Control Register 3

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Figure 3-279. EPWM_TBCTL3 Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							OSSFRCEN
R							R/W
0h							0h

Table 3-620. EPWM_TBCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	OSSFRCEN	R/W	0h	This bit determines which bit sets the EPWMxSYNCOUT One Shot Latch. 0 TBCTL2[OSHTSYNC] sets the One Shot Latch 1 GLDCTL2[OSHTLD] sets the One Shot Latch

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3.8.2.8 EPWM_CMPCTL Register

3.8.2.8.1 EPWM_CMPCTL Register (Offset = 10h) [reset = 0h]

Counter Compare Control Register.

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Figure 3-280. EPWM_CMPCTL Name Register

15	14	13	12	11	10	9	8
LINKDUTYHR	RESERVED_3	LOADBSYNC		LOADASYNC		SHDWBFULL	SHDWAFULL
R/W	R	R/W		R/W		R	R
0h	0h	0h		0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2	SHDWBMODE	RESERVED_1	SHDWAMODE	LOADBMODE		LOADAMODE	
R	R/W	R	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

Table 3-621. EPWM_CMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LINKDUTYHR	R/W	0h	CMPAHR, CMPBHR Register Linking: 0 PWMA and PWMB outputs generated independently and CMPAHR, CMPBHR are independent values as on Type-4 1 When this bit is set CMPBHR assumes the same value as CMPAHR. This is typically used in complimentary PWM output generation [Section 7 details of the operation]
14	RESERVED_3	R	0h	Reserved
13:12	LOADBSYNC	R/W	0h	Shadow to Active CMPB Register Load on SYNC event 00:Shadow to Active Load of CMPB:CMPBHR occurs according to LOADBMODE [bits 2'b10] [same as legacy] 01:Shadow to Active Load of CMPB:CMPBHR occurs both according to LOADBMODE bits and when SYNC occurs 10:Shadow to Active Load of CMPB:CMPBHR occurs only when a SYNC is received 11:Reserved Note: This bit is valid only if CMPCTL[SHDWBMODE] = 0.
11:10	LOADASYNC	R/W	0h	Shadow to Active CMPA Register Load on SYNC event 00:Shadow to Active Load of CMPA:CMPAHR occurs according to LOADAMODE [bits 2'b10] [same as legacy] 01:Shadow to Active Load of CMPA:CMPAHR occurs both according to LOADAMODE bits and when SYNC occurs 10:Shadow to Active Load of CMPA:CMPAHR occurs only when a SYNC is received 11:Reserved Note: This bit is valid only if CMPCTL[SHDWAMODE] = 0.
9	SHDWBFULL	R	0h	Counter-compare B [CMPB] Shadow Register Full Status Flag This bit self clears once a loadstrobe occurs. 0:CMPB shadow FIFO not full yet 1:Indicates the CMPB shadow FIFO is full a CPU write will overwrite current shadow value
8	SHDWAFULL	R	0h	Counter-compare A [CMPA] Shadow Register Full Status Flag The flag bit is set when a 32-bit write to CMPA:CMPAHR register or a 16-bit write to CMPA register is made. A 16-bit write to CMPAHR register will not effect the flag. This bit self clears once a load-strobe occurs. 0:CMPA shadow FIFO not full yet 1:Indicates the CMPA shadow FIFO is full, a CPU write will overwrite the current shadow value
7	RESERVED_2	R	0h	Reserved

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Table 3-621. EPWM_CMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SHDWBMODE	R/W	0h	Counter-compare B [CMPB] Register Operating Mode 0:Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register 1:Immediate mode. Only the active compare B register is used. All writes and reads directly access the active register for immediate compare action
5	RESERVED_1	R	0h	Reserved
4	SHDWAMODE	R/W	0h	Counter-compare A [CMPA] Register Operating Mode 0:Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register 1:Immediate mode. Only the active compare register is used. All writes and reads directly access the active register for immediate compare action
3:2	LOADBMODE	R/W	0h	Active Counter-Compare B [CMPB] Load From Shadow Select Mode This bit has no effect in immediate mode [CMPCTL[SHDWBMODE] = 1]. 00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10:Load on either CTR = Zero or CTR = PRD 11:Freeze [no loads possible]
1:0	LOADAMODE	R/W	0h	Active Counter-Compare A [CMPA] Load From Shadow Select Mode This bit has no effect in immediate mode [CMPCTL[SHDWAMODE] = 1]. 00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10:Load on either CTR = Zero or CTR = PRD 11:Freeze [no loads possible]

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3.8.2.9 EPWM_CMPCTL2 Register

3.8.2.9.1 EPWM_CMPCTL2 Register (Offset = 12h) [reset = 0h]

Counter Compare Control Register 2

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Figure 3-281. EPWM_CMPCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_3		LOADDSYNC		LOADCSYNC		RESERVED_2	
R		R/W		R/W		R	
0h		0h		0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2	SHDWDMODE	RESERVED_1	SHDWCMODE	LOADDMODE		LOADCMODE	
R	R/W	R	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

Table 3-622. EPWM_CMPCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED_3	R	0h	Reserved
13:12	LOADDSYNC	R/W	0h	Shadow to Active CMPD Register Load on SYNC event 00:Shadow to Active Load of CMPD occurs according to LOADDMODE 01:Shadow to Active Load of CMPD occurs both according to LOADDMODE bits and when SYNC occurs 10:Shadow to Active Load of CMPD occurs only when a SYNC is received 11:Reserved Note: This bit is valid only if CMPCTL2[SHDWDMODE] = 0.
11:10	LOADCSYNC	R/W	0h	Shadow to Active CMPC Register Load on SYNC event 00:Shadow to Active Load of CMPC occurs according to LOADCMODE 01:Shadow to Active Load of CMPC occurs both according to LOADCMODE bits and when SYNC occurs 10:Shadow to Active Load of CMPC occurs only when a SYNC is received 11:Reserved Note: This bit is valid only if CMPCTL2[SHDWCMODE] = 0.
9:7	RESERVED_2	R	0h	Reserved
6	SHDWDMODE	R/W	0h	Counter-Compare D Register Operating Mode 0:Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 1:Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action.
5	RESERVED_1	R	0h	Reserved
4	SHDWCMODE	R/W	0h	Counter-Compare C Register Operating Mode 0:Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 1:Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action.

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Table 3-622. EPWM_CMPCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	LOADDMODE	R/W	0h	Active Counter-Compare D [CMPD] Load from Shadow Select Mode 00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10:Load on either CTR = Zero or CTR = PRD 11:Freeze [no loads possible] Note: Has no effect in Immediate mode.
1:0	LOADCMODE	R/W	0h	Active Counter-Compare C [CMPC] Load from Shadow Select Mode 00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10:Load on either CTR = Zero or CTR = PRD 11:Freeze [no loads possible] Note: Has no effect in Immediate mode.

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3.8.2.10 EPWM_DBCTL Register

3.8.2.10.1 EPWM_DBCTL Register (Offset = 18h) [reset = 0h]

Dead-Band Generator Control Register.

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Figure 3-282. EPWM_DBCTL Name Register

15	14	13	12	11	10	9	8
HALFCYCLE	DEDB_MODE	OUTSWAP		SHDWDBFED MODE	SHDWDBRED MODE	LOADFEDMODE	
R/W	R/W	R/W		R/W	R/W	R/W	
0h	0h	0h		0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOADREDMODE		IN_MODE		POLSEL		OUT_MODE	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-623. EPWM_DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	HALFCYCLE	R/W	0h	Half Cycle Clocking Enable Bit 0:Full cycle clocking enabled. The dead-band counters are clocked at the TBCLK rate. 1:Half cycle clocking enabled. The dead-band counters are clocked at TBCLK*2.
14	DEDB_MODE	R/W	0h	Dead Band Dual-Edge B Mode Control [S8 switch] 0:Rising edge delay applied to InA/InB as selected by S4 switch [IN-MODE bits] on A signal path only. Falling edge delay applied to InA/InB as selected by S5 switch [INMODE bits] on B signal path only. 1:Rising edge delay and falling edge delay applied to source selected by S4 switch [INMODE bits] and output to B signal path only. Note: When this bit is set to 1, user should always either set OUT_MODE bits such that Apath = InA OR OUTSWAP bits such that OutA=Bpath otherwise, OutA will be invalid.
13:12	OUTSWAP	R/W	0h	Dead Band Output Swap Control Bit 13 controls the S6 switch and bit 12 controls the S7 switch. 00:OutA and OutB signals are as defined by OUT-MODE bits. 01:OutA = A-path as defined by OUT-MODE bits. OutB = A-path as defined by OUT-MODE bits [rising edge delay or delay-bypassed A signal path]. 10:OutA = B-path as defined by OUT-MODE bits [falling edge delay or delay-bypassed B signal path]. OutB = B-path as defined by OUT-MODE bits. 11:OutA = B-path as defined by OUT-MODE bits [falling edge delay or delay-bypassed B signal path]. OutB = A-path as defined by OUT-MODE bits [rising edge delay or delay-bypassed A signal path].
11	SHDWDBFEDMODE	R/W	0h	FED Dead-Band Load Mode 0:Immediate mode. Only the active DBFED register is used. All writes/reads via the CPU directly access the active register for immediate "FED dead-band action." 1:Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode [for compatibility with legacy].

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Table 3-623. EPWM_DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SHDWDBREDMODE	R/W	0h	RED Dead-Band Load Mode 0:Immediate mode. Only the active DBRED register is used. All writes/reads via the CPU directly access the active register for immediate "RED dead-band action." 1:Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode [for compatibility with legacy].
9:8	LOADFEDMODE	R/W	0h	Active DBFED Load from Shadow Select Mode 00:Load on Counter = 0 [CNT_eq] 01:Load on Counter = Period [PRD_eq] 10:Load on either Counter = 0, or Counter = Period 11:Freeze [no loads possible] Note: has no effect in Immediate mode.
7:6	LOADREDMODE	R/W	0h	Active DBRED Load from Shadow Select Mode 00:Load on Counter = 0 [CNT_eq] 01:Load on Counter = Period [PRD_eq] 10:Load on either Counter = 0, or Counter = Period 11:Freeze [no loads possible] Note: has no effect in Immediate mode.
5:4	IN_MODE	R/W	0h	Dead-Band Input Mode Control Bit 5 controls the S5 switch and bit 4 controls the S4 switch shown. This allows you to select the input source to the falling-edge and rising-edge delay. To produce classical dead-band waveforms the default is EPWMxA In is the source for both falling and rising-edge delays. 00:EPWMxA In [from the action-qualifier] is the source for both falling-edge and rising-edge delay. 01:EPWMxB In [from the action-qualifier] is the source for rising-edge delayed signal. EPWMxA In [from the action-qualifier] is the source for falling-edge delayed signal. 10:EPWMxA In [from the action-qualifier] is the source for rising-edge delayed signal. EPWMxB In [from the action-qualifier] is the source for falling-edge delayed signal. 11:EPWMxB In [from the action-qualifier] is the source for both rising-edge delay and falling-edge delayed signal.
3:2	POLSEL	R/W	0h	Polarity Select Control Bit 3 controls the S3 switch and bit 2 controls the S2 switch. This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule. The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter. These assume that DBCTL[OUT_MODE] = 2'b11 and DBCTL[IN_MODE] = 0x0. Other enhanced modes are also possible, but not regarded as typical usage modes. 00:Active high [AH] mode. Neither EPWMxA nor EPWMxB is inverted [default]. 01:Active low complementary [ALC] mode. EPWMxA is inverted. 10:Active high complementary [AHC]. EPWMxB is inverted. 11:Active low [AL] mode. Both EPWMxA and EPWMxB are inverted.
1:0	OUT_MODE	R/W	0h	Dead-Band Output Mode Control Bit 1 controls the S1 switch and bit 0 controls the S0 switch. 00:DBM is fully disabled or by-passed. In this mode the POLSEL and IN-MODE bits have no effect. 01:Apath = InA [delay is by-passed for A signal path] Bpath = FED [Falling Edge Delay in B signal path] 10:Apath = RED [Rising Edge Delay in A signal path] Bpath = InB [delay is by-passed for B signal path] 11:DBM is fully enabled [i.e. both RED and FED active]

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3.8.2.11 EPWM_DBCTL2 Register

3.8.2.11.1 EPWM_DBCTL2 Register (Offset = 1Ah) [reset = 0h]

Dead-Band Generator Control Register 2

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Figure 3-283. EPWM_DBCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1					SHDWDBCTLMODE	LOADDBCTLMODE	
R					R/W	R/W	
0h					0h	0h	

Table 3-624. EPWM_DBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED_1	R	0h	Reserved
2	SHDWDBCTLMODE	R/W	0h	DBCTL Load Mode 0:Immediate mode - only the Active DBCTL register is used. All writes/reads via the CPU directly access the Active register. 1:Shadow mode - All writes and reads to bits [5:0] of the DBCTL register are shadowed. All other bits still access the active register.
1:0	LOADDBCTLMODE	R/W	0h	Active DBCTL Load from Shadow Select Mode 00:Load on Counter = 0 [CNT_eq] 01:Load on Counter = Period [PRD_eq] 10:Load on either Counter = 0, or Counter = Period 11:Freeze [no loads possible] Note: has no effect in Immediate mode

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3.8.2.12 EPWM_AQCTL Register

3.8.2.12.1 EPWM_AQCTL Register (Offset = 20h) [reset = 0h]

Action Qualifier Control Register.

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Figure 3-284. EPWM_AQCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_3				LDAQBSYNC		LDAQASYNC	
R				R/W		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2	SHDWAQBMODE	RESERVED_1	SHDWAQAMODE	LDAQBMODE		LDAQAMODE	
R	R/W	R	R/W	R/W		R/W	
0h	0h	0h	0h	0h		0h	

Table 3-625. EPWM_AQCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_3	R	0h	Reserved
11:10	LDAQBSYNC	R/W	0h	Shadow to Active AQCTLB Register Load on SYNC event 00:Shadow to Active Load of AQCTLB occurs according to LDAQBMODE 01:Shadow to Active Load of AQCTLB occurs both according to LDAQBMODE bits and when SYNC occurs. 10:Shadow to Active Load of AQCTLB occurs only when a SYNC is received. 11:Reserved Note: This bit is valid only if AQCTL[SHDWAQBMODE] = 1.
9:8	LDAQASYNC	R/W	0h	Shadow to Active AQCTLA Register Load on SYNC event 00:Shadow to Active Load of AQCTLA occurs according to LDAQAMODE 01:Shadow to Active Load of AQCTLA occurs both according to LDAQAMODE bits and when SYNC occurs. 10:Shadow to Active Load of AQCTLA occurs only when a SYNC is received. 11:Reserved Note: This bit is valid only if AQCTL[SHDWAQAMODE] = 1.
7	RESERVED_2	R	0h	Reserved
6	SHDWAQBMODE	R/W	0h	Action Qualifier B Register operating mode 1:Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 0:Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register.
5	RESERVED_1	R	0h	Reserved
4	SHDWAQAMODE	R/W	0h	Action Qualifier A Register operating mode 1:Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 0:Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register.
3:2	LDAQBMODE	R/W	0h	Active Action Qualifier B Load from Shadow Select Mode 00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10:Load on either CTR = Zero or CTR = PRD 11:Freeze [no loads possible] Note: has no effect in Immediate mode.

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Table 3-625. EPWM_AQCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	LDAQAMODE	R/W	0h	Active Action Qualifier A Load from Shadow Select Mode 00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10:Load on either CTR = Zero or CTR = PRD 11:Freeze [no loads possible] Note: has no effect in Immediate mode.

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3.8.2.13 EPWM_AQTSRCSEL Register

3.8.2.13.1 EPWM_AQTSRCSEL Register (Offset = 22h) [reset = 0h]

Action Qualifier Trigger Event Source Select Register.

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Figure 3-285. EPWM_AQTSRCSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
T2SEL				T1SEL			
R/W				R/W			
0h				0h			

Table 3-626. EPWM_AQTSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7:4	T2SEL	R/W	0h	T2 Event Source Select Bits 0000 DCAEVT1 0001 DCAEVT2 0010 DCBEVT1 0011 DCBEVT2 0100 TZ1 0101 TZ2 0110 TZ3 0111 EPWMxSYNCI 1000 DCEVTFILT Others: Reserved
3:0	T1SEL	R/W	0h	T1 Event Source Select Bits 0000 DCAEVT1 0001 DCAEVT2 0010 DCBEVT1 0011 DCBEVT2 0100 TZ1 0101 TZ2 0110 TZ3 0111 EPWMxSYNCI 1000 DCEVTFILT Others: Reserved

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3.8.2.14 EPWM_PCCTL Register

3.8.2.14.1 EPWM_PCCTL Register (Offset = 28h) [reset = 0h]

PWM Chopper Control Register.

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Figure 3-286. EPWM_PCCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1					CHPDUTY		
R					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHPFREQ			OSHTWTH				CHPEN
R/W			R/W				R/W
0h			0h				0h

Table 3-627. EPWM_PCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10:8	CHPDUTY	R/W	0h	Chopping Clock Duty Cycle 000:Duty = 1/8 [12.5%] 001:Duty = 2/8 [25.0%] 010:Duty = 3/8 [37.5%] 011:Duty = 4/8 [50.0%] 100:Duty = 5/8 [62.5%] 101:Duty = 6/8 [75.0%] 110:Duty = 7/8 [87.5%] 111:Reserved
7:5	CHPFREQ	R/W	0h	Chopping Clock Frequency 000:Divide by 1 [no prescale, = 12.5 MHz at 100 MHz TBCLK] 001:Divide by 2 [6.25 MHz at 100 MHz TBCLK] 010:Divide by 3 [4.16 MHz at 100 MHz TBCLK] 011:Divide by 4 [3.12 MHz at 100 MHz TBCLK] 100:Divide by 5 [2.50 MHz at 100 MHz TBCLK] 101:Divide by 6 [2.08 MHz at 100 MHz TBCLK] 110:Divide by 7 [1.78 MHz at 100 MHz TBCLK] 111:Divide by 8 [1.56 MHz at 100 MHz TBCLK]
4:1	OSHTWTH	R/W	0h	One-Shot Pulse Width 0000 1 x EPWMCLK / 8 wide [= 80 ns at 100 MHz EPWMCLK] 0001 2 x EPWMCLK / 8 wide [= 160 ns at 100 MHz EPWMCLK] 0010 3 x EPWMCLK / 8 wide [= 240 ns at 100 MHz EPWMCLK] 0011 4 x EPWMCLK / 8 wide [= 320 ns at 100 MHz EPWMCLK] 0100 5 x EPWMCLK / 8 wide [= 400 ns at 100 MHz EPWMCLK] 0101 6 x EPWMCLK / 8 wide [= 480 ns at 100 MHz EPWMCLK] 0110 7 x EPWMCLK / 8 wide [= 560 ns at 100 MHz EPWMCLK] 0111 8 x EPWMCLK / 8 wide [= 640 ns at 100 MHz EPWMCLK] 1000 9 x EPWMCLK / 8 wide [= 720 ns at 100 MHz EPWMCLK] 1001 10 x EPWMCLK / 8 wide [= 800 ns at 100 MHz EPWMCLK] 1010 11 x EPWMCLK / 8 wide [= 880 ns at 100 MHz EPWMCLK] 1011 12 x EPWMCLK / 8 wide [= 960 ns at 100 MHz EPWMCLK] 1100 13 x EPWMCLK / 8 wide [= 1040ns at 100 MHz EPWMCLK] 1101 14 x EPWMCLK / 8 wide [= 1120ns at 100 MHz EPWMCLK] 1110 15 x EPWMCLK / 8 wide [= 1200ns at 100 MHz EPWMCLK] 1111 16 x EPWMCLK / 8 wide [= 1280ns at 100 MHz EPWMCLK]

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Table 3-627. EPWM_PCCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CHPEN	R/W	0h	PWM-Chopping Enable 0:Disable [bypass] PWM chopping function 1:Enable chopping function

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3.8.2.15 EPWM_VCAPCTL Register

3.8.2.15.1 EPWM_VCAPCTL Register (Offset = 30h) [reset = 0h]

Valley Capture Control Register.

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Figure 3-287. EPWM_VCAPCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_2					EDGEFILTDLYSEL	VDELAYDIV	
R					R/W	R/W	
0h					0h	0h	

7	6	5	4	3	2	1	0
VDELAYDIV	RESERVED_1		TRIGSEL			VCAPSTART	VCAPE
R/W	R		R/W			R/W1TS	R/W
0h	0h		0h			0h	0h

Table 3-628. EPWM_VCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_2	R	0h	Reserved
10	EDGEFILTDLYSEL	R/W	0h	Valley Switching Mode Delay Selection 0:No delay applied to the edge filter output 1:HWDELAYVAL delay applied to the edge filter output
9:7	VDELAYDIV	R/W	0h	Valley Delay Mode Divide Enable 000:HWVDELVAL = SWVDELVAL 001:HWVDELVAL = VCNTVAL+SWVDELVAL 010:HWVDELVAL = VCNTVAL>>1+SWVDELVAL 011:HWVDELVAL = VCNTVAL>>2+SWVDELVAL 100:HWVDELVAL = VCNTVAL>>4+SWVDELVAL Note: Delay value between the consecutive edge captures can optionally be divided by using these bits.
6:5	RESERVED_1	R	0h	Reserved
4:2	TRIGSEL	R/W	0h	Status of Numbered of Captured Events 000:Capture sequence is triggered by software via writes to VCAPCTL[VCAPSTART]. 001:Capture sequence is triggered by CNT_zero event. 010:Capture sequence is triggered by PRD_eq event. 011:Capture sequence is triggered by CNT_zero or PRD_eq event. 100:Capture sequence is triggered by DCAEVT1 event. 101:Capture sequence is triggered by DCAEVT2 event. 110:Capture sequence is triggered by DCBEVT1 event. 111:Capture sequence is triggered by DCBEVT2 event. Note: Valley capture sequence triggered by the selected event in this register field. Once the chosen event occurs the capture sequence is armed. Event captures occur based of the event chosen in DCFCTL[SRCSEL] register. Note: Same event may not be chosen in both DCFCTL[SRCSEL] and VCAPCTL[TRIGSEL] registers. Note: Once the chosen event in VCAPCTL[TRIGSEL] occurs, irrespective of the current capture status, capture sequence is retriggered.
1	VCAPSTART	R/W1TS	0h	Valley Capture Start 0:Writing a 0 has no effect 1:Trigger the capture sequence once if VCAPCTL[TRIGSEL]=0x0 Note: This bit is used to start valley capture sequence through software. VCAPCTL[TRIGSEL] has to be chosen for software trigger for this bit to have any effect. Writing of 1 will result in one capture sequence trigger.

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Table 3-628. EPWM_VCAPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	VCAPE	R/W	0h	Valley Capture Enable/Disable 0:Disabled 1:Enabled

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3.8.2.16 EPWM_VCNTCFG Register

3.8.2.16.1 EPWM_VCNTCFG Register (Offset = 32h) [reset = 0h]

Valley Counter Config Register.

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Figure 3-288. EPWM_VCNTCFG Name Register

15	14	13	12	11	10	9	8
STOPEDGESTS	RESERVED_2			STOPEDGE			
R	R			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STARTEDGESTS	RESERVED_1			STARTEDGE			
R	R			R/W			
0h	0h			0h			

Table 3-629. EPWM_VCNTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	STOPEDGESTS	R	0h	Stop Edge Status Bit 0:Stop edge has not occurred 1:Stop edge occurred Note: This bit is set only after the trigger sequence is armed [upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL]] and STOPEDGE occurs. Note:This bit is reset by the occurrence of the trigger pulse selected through VCAPCTL[TRIGSEL]
14:12	RESERVED_2	R	0h	Reserved
11:8	STOPEDGE	R/W	0h	Counter Stop Edge Selection Once the counter operation is armed, upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL] pulse - valley counter would stop counting upon the occurrence of chosen number of events thorough this bit field. Stop counting on occurrence of: 0000 Do not stop 0001 1st edge 0010 2nd edge 0011 3rd edge ... 1111 15th edge
7	STARTEDGESTS	R	0h	Start Edge Status Bit 0:Start edge has not occurred 1:Start edge occurred Note: This bit is set only after the trigger sequence is armed [upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL]] and STARTEDGE occurs. Note:This bit is reset by the occurrence of the trigger pulse selected through VCAPCTL[TRIGSEL]
6:4	RESERVED_1	R	0h	Reserved

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Table 3-629. EPWM_VCNTCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	STARTEDGE	R/W	0h	Counter Start Edge Selection Once the counter operation is armed, upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL] pulse - valley counter would start counting upon the occurrence of chosen number of events thorough this bit field. Start counting on occurrence of 0000 Do not start 0001 1st edge 0010 2nd edge 0011 3rd edge ... 1111 15th edge

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3.8.2.17 EPWM_HRCNFG Register

3.8.2.17.1 EPWM_HRCNFG Register (Offset = 40h) [reset = 0h]

HRPWM Configuration Register
This register is only accessible on EPWM modules with HRPWM capabilities.

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Figure 3-289. EPWM_HRCNFG Name Register

15	14	13	12	11	10	9	8
LINESEL		RESERVED_1	HRLOADB		CTLMODEB	EDGMODEB	
R/W		R	R/W		R/W	R/W	
0h		0h	0h		0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SWAPAB	AUTOCONV	SELOUTB	HRLOAD		CTLMODE	EDGMODE	
R/W	R/W	R/W	R/W		R/W	R/W	
0h	0h	0h	0h		0h	0h	

Table 3-630. EPWM_HRCNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	LINESEL	R/W	0h	Delay Line Selection Bits: Selects which of the 4 delay lines for a particular EPWM/EPWM module to send to CALIN for calibration.
13	RESERVED_1	R	0h	Reserved
12:11	HRLOADB	R/W	0h	Shadow Mode Bit Selects the time event that loads the CMPBHR shadow value into the active register. 00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10:Load on either CTR = Zero or CTR = PRD 11:Load on CMPB_EQ [Translator Event CMPB-3]
10	CTLMODEB	R/W	0h	Control Mode Bits Selects the register [CMP/TBPRD or TBPHS] that controls the MEP: 0:CMPBHR[8] or TBPRDHR[8] Register controls the edge position [i.e., this is duty or period control mode]. [Default on Reset] 1:TBPHSHR[8] Register controls the edge position [i.e., this is phase control mode].
9:8	EDGMODEB	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position [MEP] logic: 00:HRPWM capability is disabled [default on reset] 01:MEP control of rising edge [CMPBHR] 10:MEP control of falling edge [CMPBHR] 11:MEP control of both edges [TBPHSHR or TBPRDHR]
7	SWAPAB	R/W	0h	Swap EPWM A & B Output Signals This bit enables the swapping of the A & B signal outputs. The selection is as follows: 0:EPWMxA and EPWMxB outputs are unchanged. 1:EPWMxA signal appears on EPWMxB output and EPWMxB signal appears on EPWMxA output.

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Table 3-630. EPWM_HRCNFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AUTOCONV	R/W	0h	Auto Convert Delay Line Value Selects whether the fractional duty cycle/period/phase in the CMPAHR/TBPRDHR/TBPHSHR register is automatically scaled by the MEP scale factor in the HRMSTEP register or manually scaled by calculations in application software. The SFO library function automatically updates the HRMSTEP register with the appropriate MEP scale factor. 0:Automatic HRMSTEP scaling is disabled. 1:Automatic HRMSTEP scaling is enabled. If application software is manually scaling the fractional duty cycle, or phase [i.e. software sets CMPAHR = [fraction[PWMduty * PWMperiod] * MEP Scale Factor]<<8 + 0x080 for duty cycle], then this mode must be disabled.
5	SELOUTB	R/W	0h	EPWMxB Output Select Bit This bit selects which signal is output on the EPWMxB channel output. The inversion will take the high resolution mode into account and the inverted signal will contain any high resolution modification. The inversion takes place as the last step in modifying the EPWMxB signal. 0:EPWMxB output is normal. 1:EPWMxB output is inverted version of EPWMxA signal.
4:3	HRLOAD	R/W	0h	Shadow Mode Bit Selects the time event that loads the CMPAHR shadow value into the active register. 00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10:Load on either CTR = Zero or CTR = PRD 11:Load on CMPA_EQ [Translator Event CMPA-3]
2	CTLMODE	R/W	0h	Control Mode Bits Selects the register [CMP/TBPRD or TBPHS] that controls the MEP: 0:CMPAHR[8] or TBPRDHR[8] Register controls the edge position [i.e., this is duty or period control mode]. [Default on Reset] 1:TBPHSHR[8] Register controls the edge position [i.e., this is phase control mode].
1:0	EDGMODE	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position [MEP] logic: 00:HRPWM capability is disabled [default on reset] 01:MEP control of rising edge [CMPAHR] 10:MEP control of falling edge [CMPAHR] 11:MEP control of both edges [TBPHSHR or TBPRDHR]

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3.8.2.18 EPWM_HRCNFG2 Register

3.8.2.18.1 EPWM_HRCNFG2 Register (Offset = 4Eh) [reset = 0h]

HRPWM Configuration 2 Register
This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

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Figure 3-290. EPWM_HRCNFG2 Name Register

15	14	13	12	11	10	9	8
NOBYPASS	DELLOADFRC	RESERVED_1					
R/W	R/W1TS	R					
0h	0h	0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1		CTLMODEDBFED		CTLMODEDBRED		EDGMODEDB	
R		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-631. EPWM_HRCNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NOBYPASS	R/W	0h	No Bypass Delay Line Update Bit: For internal test purposes, this bit disables the 1 SYSCLK cycle bypass before delay line is updated.
14	DELLOADFRC	R/W1TS	0h	Delay Line Load Software Force: For internal test purposes, software force generates a pulse which forces a delay line update [similar to PRD_eq/CNT_zero strobe].
13:6	RESERVED_1	R	0h	Reserved
5:4	CTLMODEDBFED	R/W	0h	Shadow Mode Bit - selection should match DBCTL[LOADFEDMODE] Selects the time event that loads the DBFEDHR shadow value into the active register. 00 Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01 Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10 Load on either CTR = Zero or CTR = PRD 11 Reserved
3:2	CTLMODEDBRED	R/W	0h	Shadow Mode Bit - selection should match DBCTL[LOADREDMODE] Selects the time event that loads the DBREDHR shadow value into the active register. 00 Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000] 01 Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 10 Load on either CTR = Zero or CTR = PRD 11 Reserved
1:0	EDGMODEDB	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position [MEP] logic: 00 HRPWM capability is disabled [default on reset] 01 MEP control of rising edge [DBREDHR] 10 MEP control of falling edge [DBFEDHR] 11 MEP control of both edges [rising edge of DBREDHR or falling edge of DBFEDHR]

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3.8.2.19 EPWM_HRPCTL Register

3.8.2.19.1 EPWM_HRPCTL Register (Offset = 5Ah) [reset = 0h]

High Resolution Period Control Register
This register is only accessible on EPWM modules with HRPWM capabilities.

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Figure 3-291. EPWM_HRPCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1	PWMSYNCSELX			HRPSYNCE	TBPHSHRLOADE	PWMSYNCSEL	HRPE
R	R/W			R/W	R/W	R/W	R/W
0h	0h			0h	0h	0h	0h

Table 3-632. EPWM_HRPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6:4	PWMSYNCSELX	R/W	0h	Extended selection bits for EPWMSYNCPER 000:EPWMSYNCPER is defined by PWMSYNCSEL - > default condition [compatible with previous EPWM versions] 001:Reserved 010:Reserved 011:Reserved 100:CTR = CMPC, Count direction Up 101:CTR = CMPC, Count direction Down 110:CTR = CMPD, Count direction Up 111:CTR = CMPD, Count direction Down
3	HRPSYNCE	R/W	0h	SYNC Enable Bit [TRSYNCE]/High Resolution Period SYNC Enable Bit [HRPSYNCE]
2	TBPHSHRLOADE	R/W	0h	TBPHSHR Load Enable This bit allows you to synchronize EPWM modules with a high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event. This allows for multiple EPWM modules operating at the same frequency to be phase aligned with high-resolution. 0:Disables synchronization of high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event: 1:Synchronize the high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital comparator synchronization event. The phase is synchronized using the contents of the high-resolution phase TBPHSHR register. The TBCTL[PHSEN] bit which enables the loading of the TBCTR register with TBPHS register value on a SYNCIN or TBCTL[SWFSYNC] event works independently. However, users need to enable this bit also if they want to control phase in conjunction with the high-resolution period feature. This bit and the TBCTL[PHSEN] bit must be set to 1 when high-resolution period is enabled for up-down count mode even if TBPHSHR = 0x0000. This bit does not need to be set when only high-resolution duty is enabled.
1	PWMSYNCSEL	R/W	0h	PWMSYNC Source Select Bit: This bit selects the source for the EPWMSYNCPER signal that goes to the CMPSS and GPDAC: 0 CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD] 1 CTR = zero: Time-base counter equal to zero [TBCTR = 0x00]

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Table 3-632. EPWM_HRPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HRPE	R/W	0h	High Resolution Period Enable Bit 0:High resolution period feature disabled. In this mode the EPWM behaves as a Type 0 EPWM. 1:High resolution period enabled. In this mode the HRPWM module can control high-resolution of both the duty and frequency. When high-resolution period is enabled, TBCTL[CTRMODE] = 2'b01 [down-count mode] is not supported.

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3.8.2.20 EPWM_TRREM Register

3.8.2.20.1 EPWM_TRREM Register (Offset = 5Ch) [reset = 0h]

HRPWM High Resolution Remainder Register
This register is only accessible on EPWM modules with HRPWM capabilities.

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Figure 3-292. EPWM_TRREM Name Register

15	14	13	12	11	10	9	8
RESERVED_1					TRREM		
R					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRREM							
R/W							
0h							

Table 3-633. EPWM_TRREM Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10:0	TRREM	R/W	0h	HRPWM Remainder Bits: This 11-bit value keeps track of the remainder portion of the HRPWM algorithm calculations. This value keeps track of the remainder portion of the HRPWM hardware calculations. Notes: 1. The lower 8-bits of the TRREM register can be automatically initialized with the TBPHSHR value on a SYNCIN or TBCTL[SWFSYNC] event or DC event [if enabled]. The user can also write a value with the CPU. 2. Priority of TRREM register updates: Sync [software or hardware] TBPHSHR copied to TRREM : Highest Priority HRPWM Hardware [updates TRREM register]: Next priority CPU Write To TRREM Register: Lowest Priority 3. Bit 10 of TRREM register is not used in asymmetrical mode. This bit can be forced to zero. TRREM will be initialized to 0x0 and 0x100 in Up and Up-down modes respectively. Asymmetrical Mode: TRREM[7:0] = TBPHSHR[15:8] TRREM[10,9,8] = 3'b000 Symmetrical Mode: TRREM[7:0] = TBPHSHR[15:8] TRREM[10,9,8] = 3'b001

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3.8.2.21 EPWM_GLDCTL Register

3.8.2.21.1 EPWM_GLDCTL Register (Offset = 68h) [reset = 0h]

Global PWM Load Control Register.

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Figure 3-293. EPWM_GLDCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_2			GLDCNT			GLDPRD	
R			R			R/W	
0h			0h			0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GLDPRD	RESERVED_1	OSHTMODE	GLDMODE				GLD
R/W	R	R/W	R/W				R/W
0h	0h	0h	0h				0h

Table 3-634. EPWM_GLDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12:10	GLDCNT	R	0h	Global Load Strobe Counter Register These bits indicate how many selected events have occurred: 000:No events 001:1 event 010:2 events 011:3 events 100:4 events 101:5 events 110:6 events 111:7 events
9:7	GLDPRD	R/W	0h	Global Load Strobe Period Select Register These bits select how many selected events need to occur before a load strobe is generated 000:Disable counter 001:Generate strobe on GLDCNT = 001 [1st event] 010:Generate strobe on GLDCNT = 010 [2nd event] 011:Generate strobe on GLDCNT = 011 [3rd event] 100:Generate strobe on GLDCNT = 011 [4th event] 101:Generate strobe on GLDCNT = 001 [5th event] 110:Generate strobe on GLDCNT = 010 [6th event] 111:Generate strobe on GLDCNT = 011 [7th event]
6	RESERVED_1	R	0h	Reserved
5	OSHTMODE	R/W	0h	One Shot Load Mode Control Bit 0:One shot load mode is disabled and shadow to active loading happens continuously on all the chosen load strobes. 1:One shot mode is active. All load strobes are blocked until GLDCTL2[OSHTLD] is written with 1. Note: One Shot mode can only be used with global shadow to active load mode enabled [GLDCTL[GLD]=1]

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Table 3-634. EPWM_GLDCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:1	GLDMODE	R/W	0h	Global Load Pulse selection for Shadow to Active Mode Reloads 0000 Load on Counter = 0 [CNT_ZRO] 0001 Load on Counter = Period [PRD_EQ] 0010 Load on either Counter = 0, or Counter = Period 0011 Load on SYNCEVT - this is logical OR of DCAEVT1.sync, DCBEVT1.sync, EPWMxSYNCI and TBCTL[SWFSYNC] 0100 Load on SYNCEVT or CNT_ZRO 0101 Load on SYNCEVT or PRD_EQ 0110 Load on SYNCEVT or CNT_ZRO or PRD_EQ 1000 Load on Counter = CMPCU [CMPC_EQ counter incrementing] 1001 Load on Counter = CMPCD [CMPC_EQ counter decrementing] 1010 Load on Counter = CMPDU [CMPD_EQ counter incrementing] 1011 Load on Counter = CMPDD [CMPD_EQ counter decrementing] 1100 Reserved ... 1110 Reserved 1111 Load on GLDCTL2[GFRCLD] write
0	GLD	R/W	0h	Global Shadow to Active Load Event Control 0:Shadow to active reload for all shadowed registers happens as per the individual reload control bits specified [Compatible with previous EPWM versions]. 1:When set, all the shadow to active reload events are defined by GLDMODE bits in GLDCTL register. All the shadow registers use same reload pulse from shadow to active reloading. Individual LOADMODE bits are ignored.

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3.8.2.22 EPWM_GLDCFG Register

3.8.2.22.1 EPWM_GLDCFG Register (Offset = 6Ah) [reset = 0h]

Global PWM Load Config Register .

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Figure 3-294. EPWM_GLDCFG Name Register

15	14	13	12	11	10	9	8
RESERVED_1					AQCSFRC	AQCTLB_AQCTLB2	AQCTLA_AQCTLA2
R					R/W	R/W	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBCTL	DBFED_DBFEDHR	DBRED_DBREDHR	CMPD	CMPC	CMPB_CMPBHR	CMPA_CMPAHR	TBPRD_TBPRDHR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-635. EPWM_GLDCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10	AQCSFRC	R/W	0h	Global load event configuration for AQCSFRC 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1
9	AQCTLB_AQCTLB2	R/W	0h	Global load event configuration for AQCTLB_AQCTLB2 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1
8	AQCTLA_AQCTLA2	R/W	0h	Global load event configuration for AQCTLA_AQCTLA2 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1
7	DBCTL	R/W	0h	Global load event configuration for DBCTL 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1
6	DBFED_DBFEDHR	R/W	0h	Global load event configuration for DBFED_DBFEDHR 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1
5	DBRED_DBREDHR	R/W	0h	Global load event configuration for DBRED_DBREDHR 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1
4	CMPD	R/W	0h	Global load event configuration for CMPD 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1

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Table 3-635. EPWM_GLDCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMPC	R/W	0h	Global load event configuration for CMPC 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1
2	CMPB_CMPBHR	R/W	0h	Global load event configuration for CMPB_CMPBHR 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1
1	CMPA_CMPAHR	R/W	0h	Global load event configuration for CMPA_CMPAHR 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1
0	TBPRD_TBPRDHR	R/W	0h	Global load event configuration for TBPRD_TBPRDHR 0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs] 1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1

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3.8.2.23 EPWM_EPWMXLINK Register

3.8.2.23.1 EPWM_EPWMXLINK Register (Offset = 70h) [reset = 0h]

EPWMx Link Register
This register controls which EPWMs are linked to other EPWM modules. The default reset value will vary for each module. The reset value will link each EPWM module to itself to prevent unintentional linking of modules.

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Figure 3-295. EPWM_EPWMXLINK Name Register

31	30	29	28	27	26	25	24
RESERVED_2	GLDCTL2LINK					CMPDLINK	
R	R/W					R/W	
0h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CMPDLINK			CMPCLINK				
R/W			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1	CMPBLINK					CMPALINK	
R	R/W					R/W	
0h	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPALINK			TBPRDLINK				
R/W			R/W				
0h			0h				

Table 3-636. EPWM_EPWMXLINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_2	R	0h	Reserved
30:26	GLDCTL2LINK	R/W	0h	GLDCTL2 Link Bits Writes to the GLDCTL2 registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's GLDCTL2 registers. 5'b00000: EPWM0 5'b00001: EPWM1 5'b00010: EPWM2 5'b00011: EPWM3 5'b00100: EPWM4 5'b00101: EPWM5 5'b00110: EPWM6 5'b00111: EPWM7 5'b01000: EPWM8 5'b01001: EPWM9 5'b01010: EPWM10 5'b01011: EPWM11 5'b01100: EPWM12 ... 5'b11111: EPWM31

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Table 3-636. EPWM_EPWMXLINK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:21	CMPDLINK	R/W	0h	CMPD Link Bits Writes to the CMPD registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's CMPD registers. 5'b00000: EPWM0 5'b00001: EPWM1 5'b00010: EPWM2 5'b00011: EPWM3 5'b00100: EPWM4 5'b00101: EPWM5 5'b00110: EPWM6 5'b00111: EPWM7 5'b01000: EPWM8 5'b01001: EPWM9 5'b01010: EPWM10 5'b01011: EPWM11 5'b01100: EPWM12 ... 5'b11111: EPWM31
20:16	CMPCLINK	R/W	0h	CMPC Link Bits Writes to the CMPC registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's CMPC registers. 5'b00000: EPWM0 5'b00001: EPWM1 5'b00010: EPWM2 5'b00011: EPWM3 5'b00100: EPWM4 5'b00101: EPWM5 5'b00110: EPWM6 5'b00111: EPWM7 5'b01000: EPWM8 5'b01001: EPWM9 5'b01010: EPWM10 5'b01011: EPWM11 5'b01100: EPWM12 ... 5'b11111: EPWM31
15	RESERVED_1	R	0h	Reserved
14:10	CMPBLINK	R/W	0h	CMPB_CMPBHR Link Bits Writes to the CMPB_CMPBHR registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's CMPB_CMPBHR registers. 5'b00000: EPWM0 5'b00001: EPWM1 5'b00010: EPWM2 5'b00011: EPWM3 5'b00100: EPWM4 5'b00101: EPWM5 5'b00110: EPWM6 5'b00111: EPWM7 5'b01000: EPWM8 5'b01001: EPWM9 5'b01010: EPWM10 5'b01011: EPWM11 5'b01100: EPWM12 ... 5'b11111: EPWM31

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Table 3-636. EPWM_EPWMXLINK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:5	CMPALINK	R/W	0h	CMPA_CMPAHR Link Bits Writes to the CMPA_CMPAHR registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's CMPA_CMPAHR registers. 5'b00000: EPWM0 5'b00001: EPWM1 5'b00010: EPWM2 5'b00011: EPWM3 5'b00100: EPWM4 5'b00101: EPWM5 5'b00110: EPWM6 5'b00111: EPWM7 5'b01000: EPWM8 5'b01001: EPWM9 5'b01010: EPWM10 5'b01011: EPWM11 5'b01100: EPWM12 ... 5'b11111: EPWM31
4:0	TBPRDLINK	R/W	0h	TBPRD_TBPRDHR Link Bits Writes to the TBPRD:TBPRDHR registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's TBPRD_TBPRDHR registers. 5'b00000: EPWM0 5'b00001: EPWM1 5'b00010: EPWM2 5'b00011: EPWM3 5'b00100: EPWM4 5'b00101: EPWM5 5'b00110: EPWM6 5'b00111: EPWM7 5'b01000: EPWM8 5'b01001: EPWM9 5'b01010: EPWM10 5'b01011: EPWM11 5'b01100: EPWM12 ... 5'b11111: EPWM31

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3.8.2.24 EPWM_EPWMXLINK2 Register

3.8.2.24.1 EPWM_EPWMXLINK2 Register (Offset = 74h) [reset = 0h]

EPWMx Link 2 Register
This register controls which EPWMs are linked to other EPWM modules. The default reset value will vary for each module. The reset value will link each EPWM module to itself to prevent unintentional linking of modules.

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Figure 3-296. EPWM_EPWMXLINK2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1						DBFEDLINK	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBFEDLINK			DBREDLINK				
R/W			R/W				
0h			0h				

Table 3-637. EPWM_EPWMXLINK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_1	R	0h	Reserved
9:5	DBFEDLINK	R/W	0h	DBFED_DBFEDHR Link Bits Writes to the DBFED:DBFEDHR registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's DBFED_DBFEDHR registers. 5'b00000: EPWM0 5'b00001: EPWM1 5'b00010: EPWM2 5'b00011: EPWM3 5'b00100: EPWM4 5'b00101: EPWM5 5'b00110: EPWM6 5'b00111: EPWM7 5'b01000: EPWM8 5'b01001: EPWM9 5'b01010: EPWM10 5'b01011: EPWM11 5'b01100: EPWM12 ... 5'b11111: EPWM31

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Table 3-637. EPWM_EPWMXLINK2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	DBREDLINK	R/W	0h	DBRED_DBREDHR Link Bits Writes to the DBRED:DBREDHR registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's DBRED_DBREDHR registers. 5'b00000: EPWM0 5'b00001: EPWM1 5'b00010: EPWM2 5'b00011: EPWM3 5'b00100: EPWM4 5'b00101: EPWM5 5'b00110: EPWM6 5'b00111: EPWM7 5'b01000: EPWM8 5'b01001: EPWM9 5'b01010: EPWM10 5'b01011: EPWM11 5'b01100: EPWM12 ... 5'b11111: EPWM31

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3.8.2.25 EPWM_ETEST Register

3.8.2.25.1 EPWM_ETEST Register (Offset = 7Ah) [reset = 1h]

EPWM Test Register.

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Figure 3-297. EPWM_ETEST Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							CMPFIX_OVERRIDE
R							R/W
0h							1h

Table 3-638. EPWM_ETEST Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	CMPFIX_OVERRIDE	R/W	1h	0: Bug fix overriden 1:Bug fix takes effect

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3.8.2.26 EPWM_EPWMREV Register

3.8.2.26.1 EPWM_EPWMREV Register (Offset = 7Ch) [reset = 500h]

EPWM Revision Register.

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Figure 3-298. EPWM_EPWMREV Name Register

15	14	13	12	11	10	9	8
TYPE							
R							
5h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REV							
R							
0h							

Table 3-639. EPWM_EPWMREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	TYPE	R	5h	EPWM Type Bits: These bits specify the EPWM type. These bits are changed if the functionality of the EPWM is changed or any feature is added or removed:
7:0	REV	R	0h	EPWM Silicon Revision Bits: These bits specify the EPWM revision. These bits are changed if any bug fixes are performed:

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3.8.2.27 EPWM_HRPWMREV Register

3.8.2.27.1 EPWM_HRPWMREV Register (Offset = 7Eh) [reset = 300h]

High Resolution Revision Register.

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Figure 3-299. EPWM_HRPWMREV Name Register

15	14	13	12	11	10	9	8
TYPE							
R							
3h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REV							
R							
0h							

Table 3-640. EPWM_HRPWMREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	TYPE	R	3h	HRPWM Type Bits: These bits specify the HRPWM type. These bits are changed if the functionality of the HRPWM is changed or any feature is added or removed:
7:0	REV	R	0h	HRPWM Silicon Revision Bits: These bits specify the HRPWM revision. These bits are changed if any bug fixes are performed:

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3.8.2.28 EPWM_AQCTLA Register

3.8.2.28.1 EPWM_AQCTLA Register (Offset = 80h) [reset = 0h]

Action Qualifier Control Register For Output A .

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Figure 3-300. EPWM_AQCTLA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				CBD		CBU	
R				R/W		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAD		CAU		PRD		ZRO	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-641. EPWM_AQCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:10	CBD	R/W	0h	Action When TBCTR = CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxA output low. 10:Set: force EPWMxA output high. 11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
9:8	CBU	R/W	0h	Action When TBCTR = CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxA output low. 10:Set: force EPWMxA output high. 11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
7:6	CAD	R/W	0h	Action When TBCTR = CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxA output low. 10:Set: force EPWMxA output high. 11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
5:4	CAU	R/W	0h	Action When TBCTR = CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxA output low. 10:Set: force EPWMxA output high. 11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
3:2	PRD	R/W	0h	Action When TBCTR = TBPRD Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxA output low. 10:Set: force EPWMxA output high. 11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.

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Table 3-641. EPWM_AQCTLA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	ZRO	R/W	0h	Action When TBCTR = 0 Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxA output low. 10:Set: force EPWMxA output high. 11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.

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3.8.2.29 EPWM_AQCTLA2 Register

3.8.2.29.1 EPWM_AQCTLA2 Register (Offset = 82h) [reset = 0h]

Additional Action Qualifier Control Register For Output A .

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Figure 3-301. EPWM_AQCTLA2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
T2D		T2U		T1D		T1U	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-642. EPWM_AQCTLA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7:6	T2D	R/W	0h	Action when event occurs on T2 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxA output low. 10:Set: force EPWMxA output high. 11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
5:4	T2U	R/W	0h	Action when event occurs on T2 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxA output low. 10:Set: force EPWMxA output high. 11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
3:2	T1D	R/W	0h	Action when event occurs on T1 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxA output low. 10:Set: force EPWMxA output high. 11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
1:0	T1U	R/W	0h	Action when event occurs on T1 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxA output low. 10:Set: force EPWMxA output high. 11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.

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3.8.2.30 EPWM_AQCTLB Register

3.8.2.30.1 EPWM_AQCTLB Register (Offset = 84h) [reset = 0h]

Action Qualifier Control Register For Output B .

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Figure 3-302. EPWM_AQCTLB Name Register

15	14	13	12	11	10	9	8
RESERVED_1				CBD		CBU	
R				R/W		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAD		CAU		PRD		ZRO	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-643. EPWM_AQCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:10	CBD	R/W	0h	Action When TBCTR = CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxB output low. 10:Set: force EPWMxB output high. 11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
9:8	CBU	R/W	0h	Action When TBCTR = CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxB output low. 10:Set: force EPWMxB output high. 11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
7:6	CAD	R/W	0h	Action When TBCTR = CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxB output low. 10:Set: force EPWMxB output high. 11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
5:4	CAU	R/W	0h	Action When TBCTR = CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxB output low. 10:Set: force EPWMxB output high. 11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
3:2	PRD	R/W	0h	Action When TBCTR = TBPRD Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxB output low. 10:Set: force EPWMxB output high. 11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.

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Table 3-643. EPWM_AQCTLB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	ZRO	R/W	0h	Action When TBCTR = 0 Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxB output low. 10:Set: force EPWMxB output high. 11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.

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3.8.2.31 EPWM_AQCTLB2 Register

3.8.2.31.1 EPWM_AQCTLB2 Register (Offset = 86h) [reset = 0h]

Additional Action Qualifier Control Register For Output B .

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Figure 3-303. EPWM_AQCTLB2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
T2D		T2U		T1D		T1U	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-644. EPWM_AQCTLB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7:6	T2D	R/W	0h	Action when event occurs on T2 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxB output low. 10:Set: force EPWMxB output high. 11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
5:4	T2U	R/W	0h	Action when event occurs on T2 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxB output low. 10:Set: force EPWMxB output high. 11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
3:2	T1D	R/W	0h	Action when event occurs on T1 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxB output low. 10:Set: force EPWMxB output high. 11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
1:0	T1U	R/W	0h	Action when event occurs on T1 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00:Do nothing [action disabled] 01:Clear: force EPWMxB output low. 10:Set: force EPWMxB output high. 11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.

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3.8.2.32 EPWM_AQSFRC Register

3.8.2.32.1 EPWM_AQSFRC Register (Offset = 8Eh) [reset = 0h]

Action Qualifier Software Force Register.

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Figure 3-304. EPWM_AQSFRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RLDCSF		OTSFB	ACTSFB		OTSFA	ACTSFA	
R/W		R/W1TS	R/W		R/W1TS	R/W	
0h		0h	0h		0h	0h	

Table 3-645. EPWM_AQSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7:6	RLDCSF	R/W	0h	AQCSFRC Active Register Reload From Shadow Options 00:Load on event counter equals zero 01:Load on event counter equals period 10:Load on event counter equals zero or counter equals period 11:Load immediately [the active register is directly accessed by the CPU and is not loaded from the shadow register].
5	OTSFB	R/W1TS	0h	One-Time Software Forced Event on Output B 0:Writing a 0 [zero] has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete [i.e., a forced event is initiated.]. This is a one-shot forced event. It can be overridden by another subsequent event on output B. 1:Initiates a single software forced event
4:3	ACTSFB	R/W	0h	Action When One-Time Software Force B is Invoked 00:Does nothing [action disabled] 01:Clear [low] 10:Set [high] 11:Toggle [Low -> High, High -> Low] Note: This action is not qualified by counter direction [CNT_dir]
2	OTSFA	R/W1TS	0h	One-Time Software Forced Event on Output A 0:Writing a 0 [zero] has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete [i.e., a forced event is initiated]. This is a one-shot forced event. It can be overridden by another subsequent event on output A. 1:Initiates a single software forced event
1:0	ACTSFA	R/W	0h	Action When One-Time Software Force A Is Invoked 00:Does nothing [action disabled] 01:Clear [low] 10:Set [high] 11:Toggle [Low -> High, High -> Low] Note: This action is not qualified by counter direction [CNT_dir]

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3.8.2.33 EPWM_AQCSFRC Register

3.8.2.33.1 EPWM_AQCSFRC Register (Offset = 92h) [reset = 0h]

Action Qualifier Continuous S/W Force Register .

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Figure 3-305. EPWM_AQCSFRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				CSFB		CSFA	
R				R/W		R/W	
0h				0h		0h	

Table 3-646. EPWM_AQCSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3:2	CSFB	R/W	0h	Continuous Software Force on Output B In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register. To configure shadow mode, use AQSFRC[RLDCSF]. 00:Software forcing is disabled and has no effect 01:Forces a continuous low on output B 10:Forces a continuous high on output B 11:Software forcing is disabled and has no effect
1:0	CSFA	R/W	0h	Continuous Software Force on Output A In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register. 00:Software forcing is disabled and has no effect 01:Forces a continuous low on output A 10:Forces a continuous high on output A 11:Software forcing is disabled and has no effect

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3.8.2.34 EPWM_DBREDHR Register

3.8.2.34.1 EPWM_DBREDHR Register (Offset = A0h) [reset = 0h]

Dead-Band Generator Rising Edge Delay High Resolution Mirror Register .

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Figure 3-306. EPWM_DBREDHR Name Register

15	14	13	12	11	10	9	8
DBREDHR							RESERVED_2
R/W							R
0h							0h
7	6	5	4	3	2	1	0
DBREDHR_DELAY							RESERVED_1
R							R
0h							0h

Table 3-647. EPWM_DBREDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	DBREDHR	R/W	0h	Dead Band Rising Edge Delay High Resolution Bits
8	RESERVED_2	R	0h	Reserved
7:1	DBREDHR_DELAY	R	0h	These 7-bits contain the results of OTTO calculation [if auto-conversion is enabled]
0	RESERVED_1	R	0h	Reserved

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3.8.2.35 EPWM_DBRED Register

3.8.2.35.1 EPWM_DBRED Register (Offset = A2h) [reset = 0h]

Dead-Band Generator Rising Edge Delay High Resolution Mirror Register .

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Figure 3-307. EPWM_DBRED Name Register

15	14	13	12	11	10	9	8
RESERVED_1		DBRED					
R		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBRED							
R/W							
0h							

Table 3-648. EPWM_DBRED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED_1	R	0h	Reserved
13:0	DBRED	R/W	0h	Rising edge delay value

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3.8.2.36 EPWM_DBFEDHR Register

3.8.2.36.1 EPWM_DBFEDHR Register (Offset = A4h) [reset = 0h]

Dead-Band Generator Falling Edge Delay High Resolution Register .

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Figure 3-308. EPWM_DBFEDHR Name Register

15	14	13	12	11	10	9	8
DBFEDHR							RESERVED_2
R/W							R
0h							0h
7	6	5	4	3	2	1	0
DBFEDHR_DELAY							RESERVED_1
R							R
0h							0h

Table 3-649. EPWM_DBFEDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	DBFEDHR	R/W	0h	Dead Band Falling Edge Delay High Resolution Bits
8	RESERVED_2	R	0h	Reserved
7:1	DBFEDHR_DELAY	R	0h	These 7-bits contain the results of OTTO calculation [if auto-conversion is enabled]
0	RESERVED_1	R	0h	Reserved

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3.8.2.37 EPWM_DBFED Register

3.8.2.37.1 EPWM_DBFED Register (Offset = A6h) [reset = 0h]

Dead-Band Generator Falling Edge Delay Count Register.

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Figure 3-309. EPWM_DBFED Name Register

15	14	13	12	11	10	9	8
RESERVED_1		DBFED					
R		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DBFED							
R/W							
0h							

Table 3-650. EPWM_DBFED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED_1	R	0h	Reserved
13:0	DBFED	R/W	0h	Falling Edge Delay Count 14-bit counter

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3.8.2.38 EPWM_TBPHS Register

3.8.2.38.1 EPWM_TBPHS Register (Offset = C0h) [reset = 0h]

Time Base Phase High.

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Figure 3-310. EPWM_TBPHS Name Register

31	30	29	28	27	26	25	24
TBPHS							
R/W							
0h							
23	22	21	20	19	18	17	16
TBPHS							
R/W							
0h							
15	14	13	12	11	10	9	8
TBPHSHR							
R/W							
0h							
7	6	5	4	3	2	1	0
TBPHSHR							
R/W							
0h							

Table 3-651. EPWM_TBPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TBPHS	R/W	0h	Phase Offset Register These bits set time-base counter phase of the selected EPWM relative to the time-base that is supplying the synchronization input signal. - If TBCTL[PHSEN] = 0, then the synchronization event is ignored and the time-base counter is not loaded with the phase. - If TBCTL[PHSEN] = 1, then the time-base counter [TBCTR] will be loaded with the phase [TBPHS] when a synchronization event occurs. The synchronization event can be initiated by the input synchronization signal [EPWMxSYNCI] or by a software forced synchronization.
15:0	TBPHSHR	R/W	0h	Phase Offset [High Resolution] Register. TBPHSHR must not be used. Instead TRREM [HRPWM remainder register] must be used to mimic the functionality of TBPHSHR. The lower 8 bits in this register are ignored - writes are ignored and reads return zero

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3.8.2.39 EPWM_TBPRDHR Register

3.8.2.39.1 EPWM_TBPRDHR Register (Offset = C4h) [reset = 0h]

Time Base Period High Resolution Register .

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Figure 3-311. EPWM_TBPRDHR Name Register

15	14	13	12	11	10	9	8
TBPRDHR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBPRDHR							
R/W							
0h							

Table 3-652. EPWM_TBPRDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBPRDHR	R/W	0h	Period High Resolution Bits The upper 8-bits contain the high-resolution portion of the period value. The TBPRDHR register is not affected by the TBCTL[PRDLD] bit. Reads from this register always reflect the shadow register. Likewise writes are also to the shadow register. The TBPRDHR register is only used when the high resolution period feature is enabled. This register is only available with EPWM modules which support high-resolution period control. The lower 8 bits in this register are ignored - writes are ignored and reads return zero

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3.8.2.40 EPWM_TBPRD Register

3.8.2.40.1 EPWM_TBPRD Register (Offset = C6h) [reset = 0h]

Time Base Period Register .

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Figure 3-312. EPWM_TBPRD Name Register

15	14	13	12	11	10	9	8
TBPRD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TBPRD							
R/W							
0h							

Table 3-653. EPWM_TBPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TBPRD	R/W	0h	Time Base Period Register These bits determine the period of the time-base counter. This sets the PWM frequency. Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit. By default this register is shadowed. - If TBCTL[PRDLD] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the active register will be loaded from the shadow register when the time-base counter equals zero. - If TBCTL[PRDLD] = 1, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - The active and shadow registers share the same memory map address.

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3.8.2.41 EPWM_TBPRDHRB Register

3.8.2.41.1 EPWM_TBPRDHRB Register (Offset = C8h) [reset = 0h]

Calculation Result for EPWMxB.

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Figure 3-313. EPWM_TBPRDHRB Name Register

15	14	13	12	11	10	9	8
TBPRDHRB							
R/W							
0h							
7	6	5	4	3	2	1	0
TBPRDHRB_DELAY							
R/W							
0h							

Table 3-654. EPWM_TBPRDHRB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	TBPRDHRB	R/W	0h	TBPRD High Resolution Calculation [2] Results for EPWMxB HRPWM Equations
7:0	TBPRDHRB_DELAY	R/W	0h	TBPRDHRB Delay

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3.8.2.42 EPWM_CMPA Register

3.8.2.42.1 EPWM_CMPA Register (Offset = D4h) [reset = 0h]

Counter Compare A Register .

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Figure 3-314. EPWM_CMPA Name Register

31	30	29	28	27	26	25	24
CMPA							
R/W							
0h							
23	22	21	20	19	18	17	16
CMPA							
R/W							
0h							
15	14	13	12	11	10	9	8
CMPAHR							
R/W							
0h							
7	6	5	4	3	2	1	0
CMPAHR							
R/W							
0h							

Table 3-655. EPWM_CMPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CMPA	R/W	0h	Compare A Register The value in the active CMPA register is continuously compared to the time-base counter [TBCTR]. When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare A" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include: - Do nothing the event is ignored. - Clear: Pull the EPWMxA and/or EPWMxB signal low - Set: Pull the EPWMxA and/or EPWMxB signal high - Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWAMODE] bit. By default this register is shadowed. - If CMPCTL[SHDWAMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL[LOADAMODE] bit field determines which event will load the active register from the shadow register. - Before a write, the CMPCTL[SHDWAFULL] bit can be read to determine if the shadow register is currently full. - If CMPCTL[SHDWAMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.

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Table 3-655. EPWM_CMPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	CMPAHR	R/W	0h	Compare A HRPWM Extension Register The UPPER 8-bits contain the high-resolution portion [most significant 8-bits] of the counter-compare A value. CMPA:CMPAHR can be accessed in a single 32-bit read/write. Shadowing is enabled and disabled by the CMPCTL[SHDWAMODE] bit as described for the CMPA register. The lower 8 bits in this register are ignored

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3.8.2.43 EPWM_CMPB Register

3.8.2.43.1 EPWM_CMPB Register (Offset = D8h) [reset = 0h]

Compare B Register .

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Figure 3-315. EPWM_CMPB Name Register

31	30	29	28	27	26	25	24
CMPB							
R/W							
0h							
23	22	21	20	19	18	17	16
CMPB							
R/W							
0h							
15	14	13	12	11	10	9	8
CMPBHR							
R/W							
0h							
7	6	5	4	3	2	1	0
CMPBHR							
R/W							
0h							

Table 3-656. EPWM_CMPB Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CMPB	R/W	0h	Compare B Register The value in the active CMPB register is continuously compared to the time-base counter [TBCTR]. When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare B" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include: - Do nothing the event is ignored. - Clear: Pull the EPWMxA and/or EPWMxB signal low - Set: Pull the EPWMxA and/or EPWMxB signal high - Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWBMODE] bit. By default this register is shadowed. - If CMPCTL[SHDWBMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL[LOADBMODE] bit field determines which event will load the active register from the shadow register. - Before a write, the CMPCTL[SHDWBFULL] bit can be read to determine if the shadow register is currently full. - If CMPCTL[SHDWBMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.
15:0	CMPBHR	R/W	0h	Compare B High Resolution Bits The lower 8 bits in this register are ignored

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3.8.2.44 EPWM_CMPC Register

3.8.2.44.1 EPWM_CMPC Register (Offset = DEh) [reset = 0h]

Counter Compare C Register
LINK feature access should always be 16-bit.

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Figure 3-316. EPWM_CMPC Name Register

15	14	13	12	11	10	9	8
CMPC							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPC							
R/W							
0h							

Table 3-657. EPWM_CMPC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPC	R/W	0h	Compare C Register The value in the active CMPC register is continuously compared to the time-base counter [TBCTR]. When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare C" event. Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWCMODE] bit. By default this register is shadowed. - If CMPCTL2[SHDWCMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL2[LOADCMODE] bit field determines which event will load the active register from the shadow register: - If CMPCTL2[SHDWCMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register that is, the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.

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3.8.2.45 EPWM_CMPD Register

3.8.2.45.1 EPWM_CMPD Register (Offset = E2h) [reset = 0h]

Counter Compare D Register
LINK feature access should always be 16-bit.

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Figure 3-317. EPWM_CMPD Name Register

15	14	13	12	11	10	9	8
CMPD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPD							
R/W							
0h							

Table 3-658. EPWM_CMPD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPD	R/W	0h	Compare D Register The value in the active CMPD register is continuously compared to the time-base counter [TBCTR]. When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare D" event. Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWDMODE] bit. By default this register is shadowed. - If CMPCTL2[SHDWDMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL2[LOADDMODE] bit field determines which event will load the active register from the shadow register: - If CMPCTL2[SHDWDMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register that is, the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.

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3.8.2.46 EPWM_GLDCTL2 Register

3.8.2.46.1 EPWM_GLDCTL2 Register (Offset = E8h) [reset = 0h]

Global PWM Load Control Register 2

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Figure 3-318. EPWM_GLDCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						GFRCLD	OSHTLD
R						R/W1TS	R/W1TS
0h						0h	0h

Table 3-659. EPWM_GLDCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED_1	R	0h	Reserved
1	GFRCLD	R/W1TS	0h	Force Load Event in One Shot Mode 0:Writing of 0 will be ignored. Always reads back a 0. 1:Force one load event at the input of the event pre-scale counter as shown in the diagram below. This bit is intended to be used for testing and/or software force loading of the events in global load mode.
0	OSHTLD	R/W1TS	0h	Enable Reload Event in One Shot Mode 0:Writing of 0 will be ignored. Always reads back a 0. 1:Turns the one shot latch condition ON. Upon occurrence of a chosen load strobe, one shadow to active reload occurs and the latch will be cleared. Hence Writing 1 to this bit would allow one load strobe event to pass through and block further strobe events.

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3.8.2.47 EPWM_SWVDELVAL Register

3.8.2.47.1 EPWM_SWVDELVAL Register (Offset = EEh) [reset = 0h]

Software Valley Mode Delay Register.

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Figure 3-319. EPWM_SWVDELVAL Name Register

15	14	13	12	11	10	9	8
SWVDELVAL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SWVDELVAL							
R/W							
0h							

Table 3-660. EPWM_SWVDELVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SWVDELVAL	R/W	0h	Software Valley Delay Value Register This register can be optionally used define offset value for the hardware calculated delay HWDELAYVAL as defined in VCAPCTL[VDELAYDIV] bits.

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3.8.2.48 EPWM_TZSEL Register

3.8.2.48.1 EPWM_TZSEL Register (Offset = 100h) [reset = 0h]

Trip Zone Select Register .

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Figure 3-320. EPWM_TZSEL Name Register

15	14	13	12	11	10	9	8
DCBEVT1	DCAEVT1	OSHT6	OSHT5	OSHT4	OSHT3	OSHT2	OSHT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-661. EPWM_TZSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Select 0:Disable DCBEVT1 as one-shot-trip source for this EPWM module. 1:Enable DCBEVT1 as one-shot-trip source for this EPWM module.
14	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Select 0:Disable DCAEVT1 as one-shot-trip source for this EPWM module. 1:Enable DCAEVT1 as one-shot-trip source for this EPWM module.
13	OSHT6	R/W	0h	Trip-Zone 6 [TZ6] Select 0:Disable TZ6 as a one-shot trip source for this EPWM module 1:Enable TZ6 as a one-shot trip source for this EPWM module
12	OSHT5	R/W	0h	Trip-Zone 5 [TZ5] Select 0:Disable TZ5 as a one-shot trip source for this EPWM module 1:Enable TZ5 as a one-shot trip source for this EPWM module
11	OSHT4	R/W	0h	Trip-Zone 4 [TZ4] Select 0:Disable TZ4 as a one-shot trip source for this EPWM module 1:Enable TZ4 as a one-shot trip source for this EPWM module
10	OSHT3	R/W	0h	Trip-Zone 3 [TZ3] Select 0:Disable TZ3 as a one-shot trip source for this EPWM module 1:Enable TZ3 as a one-shot trip source for this EPWM module
9	OSHT2	R/W	0h	Trip-Zone 2 [TZ2] Select 0:Disable TZ2 as a one-shot trip source for this EPWM module 1:Enable TZ2 as a one-shot trip source for this EPWM module
8	OSHT1	R/W	0h	Trip-Zone 1 [TZ1] Select 0:Disable TZ1 as a one-shot trip source for this EPWM module 1:Enable TZ1 as a one-shot trip source for this EPWM module
7	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Select 0:Disable DCBEVT2 as a CBC trip source for this EPWM module 1:Enable DCBEVT2 as a CBC trip source for this EPWM module
6	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Select 0:Disable DCAEVT2 as a CBC trip source for this EPWM module 1:Enable DCAEVT2 as a CBC trip source for this EPWM module
5	CBC6	R/W	0h	Trip-Zone 6 [TZ6] Select 0:Disable TZ6 as a CBC trip source for this EPWM module 1:Enable TZ6 as a CBC trip source for this EPWM module
4	CBC5	R/W	0h	Trip-Zone 5 [TZ5] Select 0:Disable TZ5 as a CBC trip source for this EPWM module 1:Enable TZ5 as a CBC trip source for this EPWM module

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Table 3-661. EPWM_TZSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CBC4	R/W	0h	Trip-Zone 4 [TZ4] Select 0:Disable TZ4 as a CBC trip source for this EPWM module 1:Enable TZ4 as a CBC trip source for this EPWM module
2	CBC3	R/W	0h	Trip-Zone 3 [TZ3] Select 0:Disable TZ3 as a CBC trip source for this EPWM module 1:Enable TZ3 as a CBC trip source for this EPWM module
1	CBC2	R/W	0h	Trip-Zone 2 [TZ2] Select 0:Disable TZ2 as a CBC trip source for this EPWM module 1:Enable TZ2 as a CBC trip source for this EPWM module
0	CBC1	R/W	0h	Trip-Zone 1 [TZ1] Select 0:Disable TZ1 as a CBC trip source for this EPWM module 1:Enable TZ1 as a CBC trip source for this EPWM module

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3.8.2.49 EPWM_TZSEL2 Register

3.8.2.49.1 EPWM_TZSEL2 Register (Offset = 102h) [reset = 0h]

Trip Zone Select Register 2

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Figure 3-321. EPWM_TZSEL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_2							CAPEVTOST
R							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED_1							CAPEVTCBC
R							R/W
0h							0h

Table 3-662. EPWM_TZSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_2	R	0h	Reserved
8	CAPEVTOST	R/W	0h	CAPEVT OST Select 0:Disable CAPEVT as a one-shot trip source for this EPWM module 1:Enable CAPEVT as a one-shot trip source for this EPWM module
7:1	RESERVED_1	R	0h	Reserved
0	CAPEVTCBC	R/W	0h	CAPEVT CBC mode Select 0:Disable CAPEVT as a CBC trip source for this EPWM module 1:Enable CAPEVT as a CBC trip source for this EPWM module

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3.8.2.50 EPWM_TZDCSEL Register

3.8.2.50.1 EPWM_TZDCSEL Register (Offset = 104h) [reset = 0h]

Trip Zone Digital Comparator Select Register.

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Figure 3-322. EPWM_TZDCSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DCBEVT2			DCBEVT1
R				R/W			R/W
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCBEVT1		DCAEVT2			DCAEVT1		
R/W		R/W			R/W		
0h		0h			0h		

Table 3-663. EPWM_TZDCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:9	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Selection 000:Event disabled 001:DCBH = low, DCBL = don't care 010:DCBH = high, DCBL = don't care 011:DCBL = low, DCBH = don't care 100:DCBL = high, DCBH = don't care 101:DCBL = high, DCBH = low 110:Reserved 111:Reserved
8:6	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Selection 000:Event disabled 001:DCBH = low, DCBL = don't care 010:DCBH = high, DCBL = don't care 011:DCBL = low, DCBH = don't care 100:DCBL = high, DCBH = don't care 101:DCBL = high, DCBH = low 110:Reserved 111:Reserved
5:3	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Selection 000:Event disabled 001:DCAH = low, DCAL = don't care 010:DCAH = high, DCAL = don't care 011:DCAL = low, DCAH = don't care 100:DCAL = high, DCAH = don't care 101:DCAL = high, DCAH = low 110:Reserved 111:Reserved
2:0	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Selection 000:Event disabled 001:DCAH = low, DCAL = don't care 010:DCAH = high, DCAL = don't care 011:DCAL = low, DCAH = don't care 100:DCAL = high, DCAH = don't care 101:DCAL = high, DCAH = low 110:Reserved 111:Reserved

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3.8.2.51 EPWM_TZCTL Register

3.8.2.51.1 EPWM_TZCTL Register (Offset = 108h) [reset = 0h]

Trip Zone Control Register.

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Figure 3-323. EPWM_TZCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DCBEVT2		DCBEVT1	
R				R/W		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCAEVT2		DCAEVT1		TZB		TZA	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-664. EPWM_TZCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:10	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Action On EPWMxB 00:High-impedance [EPWMxB = High-impedance state] 01:Force EPWMxB to a high state. 10:Force EPWMxB to a low state. 11:Do Nothing, trip action is disabled
9:8	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Action On EPWMxB 00:High-impedance [EPWMxB = High-impedance state] 01:Force EPWMxB to a high state. 10:Force EPWMxB to a low state. 11:Do Nothing, trip action is disabled
7:6	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA 00:High-impedance [EPWMxA = High-impedance state] 01:Force EPWMxA to a high state. 10:Force EPWMxA to a low state. 11:Do Nothing, trip action is disabled
5:4	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA 00:High-impedance [EPWMxA = High-impedance state] 01:Force EPWMxA to a high state. 10:Force EPWMxA to a low state. 11:Do Nothing, trip action is disabled
3:2	TZB	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2Trip Action On EPWMxB When a trip event occurs the following action is taken on output EPWMxB. Which trip-zone pins can cause an event is defined in the TZSEL register. 00:High-impedance [EPWMxB = High-impedance state] 01:Force EPWMxB to a high state 10:Force EPWMxB to a low state 11:Do nothing, no action is taken on EPWMxB.
1:0	TZA	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA When a trip event occurs the following action is taken on output EPWMxA. Which trip-zone pins can cause an event is defined in the TZSEL register. 00:High-impedance [EPWMxA = High-impedance state] 01:Force EPWMxA to a high state 10:Force EPWMxA to a low state 11:Do nothing, no action is taken on EPWMxA.

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3.8.2.52 EPWM_TZCTL2 Register

3.8.2.52.1 EPWM_TZCTL2 Register (Offset = 10Ah) [reset = 0h]

Additional Trip Zone Control Register.

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Figure 3-324. EPWM_TZCTL2 Name Register

15	14	13	12	11	10	9	8
ETZE	RESERVED_1			TZBD			TZBU
R/W	R			R/W			R/W
0h	0h			0h			0h

7	6	5	4	3	2	1	0
TZBU		TZAD			TZAU		
R/W		R/W			R/W		
0h		0h			0h		

Table 3-665. EPWM_TZCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ETZE	R/W	0h	TZCTL2 Enable 0:Use trip action from TZCTL [legacy EPWM compatibility] 1:Use trip action defined in TZCTL2, TZCTLDCA and TZCTLDCB. Settings in TZCTL are ignored
14:12	RESERVED_1	R	0h	Reserved
11:9	TZBD	R/W	0h	TZ1 to TZ6 Trip Action On EPWMxB while Count direction is DOWN 000:HiZ [EPWMxB = HiZ state] 001:Forced Hi [EPWMxB = High state] 010:Forced Lo [EPWMxB = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled
8:6	TZBU	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxB while Count direction is UP 000:HiZ [EPWMxB = HiZ state] 001:Forced Hi [EPWMxB = High state] 010:Forced Lo [EPWMxB = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled
5:3	TZAD	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA while Count direction is DOWN 000:HiZ [EPWMxA = HiZ state] 001:Forced Hi [EPWMxA = High state] 010:Forced Lo [EPWMxA = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled

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Table 3-665. EPWM_TZCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	TZAU	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA while Count direction is UP 000:HiZ [EPWMxA = HiZ state] 001:Forced Hi [EPWMxA = High state] 010:Forced Lo [EPWMxA = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled

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3.8.2.53 EPWM_TZCTLDCA Register

3.8.2.53.1 EPWM_TZCTLDCA Register (Offset = 10Ch) [reset = 0h]

Trip Zone Control Register Digital Compare A .

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Figure 3-325. EPWM_TZCTLDCA Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DCAEVT2D			DCAEVT2U
R				R/W			R/W
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCAEVT2U		DCAEVT1D			DCAEVT1U		
R/W		R/W			R/W		
0h		0h			0h		

Table 3-666. EPWM_TZCTLDCA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:9	DCAEVT2D	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA while Count direction is DOWN 000:HiZ [EPWMxA = HiZ state] 001:Forced Hi [EPWMxA = High state] 010:Forced Lo [EPWMxA = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled
8:6	DCAEVT2U	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA while Count direction is UP 000:HiZ [EPWMxA = HiZ state] 001:Forced Hi [EPWMxA = High state] 010:Forced Lo [EPWMxA = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled
5:3	DCAEVT1D	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA while Count direction is DOWN 000:HiZ [EPWMxA = HiZ state] 001:Forced Hi [EPWMxA = High state] 010:Forced Lo [EPWMxA = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled

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Table 3-666. EPWM_TZCTLDCA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DCAEVT1U	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA while Count direction is UP 000:HiZ [EPWMxA = HiZ state] 001:Forced Hi [EPWMxA = High state] 010:Forced Lo [EPWMxA = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled

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3.8.2.54 EPWM_TZCTLDCB Register

3.8.2.54.1 EPWM_TZCTLDCB Register (Offset = 10Eh) [reset = 0h]

Trip Zone Control Register Digital Compare B .

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Figure 3-326. EPWM_TZCTLDCB Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DCBEVT2D			DCBEVT2U
R				R/W			R/W
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCBEVT2U		DCBEVT1D			DCBEVT1U		
R/W		R/W			R/W		
0h		0h			0h		

Table 3-667. EPWM_TZCTLDCB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:9	DCBEVT2D	R/W	0h	Digital Compare Output B Event 2 Action On EPWMxB while Count direction is DOWN 000:HiZ [EPWMxB = HiZ state] 001:Forced Hi [EPWMxB = High state] 010:Forced Lo [EPWMxB = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled
8:6	DCBEVT2U	R/W	0h	Digital Compare Output B Event 2 Action On EPWMxB while Count direction is UP 000:HiZ [EPWMxB = HiZ state] 001:Forced Hi [EPWMxB = High state] 010:Forced Lo [EPWMxB = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled
5:3	DCBEVT1D	R/W	0h	Digital Compare Output B Event 1 Action On EPWMxB while Count direction is DOWN 000:HiZ [EPWMxB = HiZ state] 001:Forced Hi [EPWMxB = High state] 010:Forced Lo [EPWMxB = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled

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Table 3-667. EPWM_TZCTLDCB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DCBEVT1U	R/W	0h	Digital Compare Output B Event 1 Action On EPWMxB while Count direction is UP 000:HiZ [EPWMxB = HiZ state] 001:Forced Hi [EPWMxB = High state] 010:Forced Lo [EPWMxB = Lo state] 011:Toggle [Low -> High, High -> Low] 100:Reserved 101:Reserved 110:Reserved 111:Do Nothing, trip action is disabled

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3.8.2.55 EPWM_TZEINT Register

3.8.2.55.1 EPWM_TZEINT Register (Offset = 11Ah) [reset = 0h]

Trip Zone Enable Interrupt Register.

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Figure 3-327. EPWM_TZEINT Name Register

15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAPEVT	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-668. EPWM_TZEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_2	R	0h	Reserved
7	CAPEVT	R/W	0h	Capture Event Interrupt Enable 0:Disabled 1:Enabled
6	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Interrupt Enable 0:Disabled 1:Enabled
5	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Interrupt Enable 0:Disabled 1:Enabled
4	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Interrupt Enable 0:Disabled 1:Enabled
3	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Interrupt Enable 0:Disabled 1:Enabled
2	OST	R/W	0h	Trip-Zone One-Shot Interrupt Enable 0:Disable one-shot interrupt generation 1:Enable Interrupt generation a one-shot trip event will cause a EPWMx_TZINT VIM interrupt.
1	CBC	R/W	0h	Trip-Zone Cycle-by-Cycle Interrupt Enable 0:Disable cycle-by-cycle interrupt generation. 1:Enable interrupt generation A cycle-by-cycle trip event will cause an EPWMx_TZINT VIM interrupt.
0	RESERVED_1	R	0h	Reserved

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3.8.2.56 EPWM_TZFLG Register

3.8.2.56.1 EPWM_TZFLG Register (Offset = 126h) [reset = 0h]

Trip Zone Flag Register.

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Figure 3-328. EPWM_TZFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPEVT	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	INT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-669. EPWM_TZFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7	CAPEVT	R	0h	Latched Status Flag for Capture Event 0:Indicates no trip event has occurred on CAPEVT 1:Indicates a trip event has occurred for the event defined for CAPEVT
6	DCBEVT2	R	0h	Latched Status Flag for Digital Compare Output B Event 2 0:Indicates no trip event has occurred on DCBEVT2 1:Indicates a trip event has occurred for the event defined for DCBEVT2
5	DCBEVT1	R	0h	Latched Status Flag for Digital Compare Output B Event 1 0:Indicates no trip event has occurred on DCBEVT1 1:Indicates a trip event has occurred for the event defined for DCBEVT1
4	DCAEVT2	R	0h	Latched Status Flag for Digital Compare Output A Event 2 0:Indicates no trip event has occurred on DCAEVT2 1:Indicates a trip event has occurred for the event defined for DCAEVT2
3	DCAEVT1	R	0h	Latched Status Flag for Digital Compare Output A Event 1 0:Indicates no trip event has occurred on DCAEVT1 1:Indicates a trip event has occurred for the event defined for DCAEVT1
2	OST	R	0h	Latched Status Flag for A One-Shot Trip Event 0:No one-shot trip event has occurred. 1:Indicates a trip event has occurred on a pin selected as a one-shot trip source. This bit is cleared by Writing the appropriate value to the TZCLR register.

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Table 3-669. EPWM_TZFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CBC	R	0h	Latched Status Flag for Cycle-By-Cycle Trip Event 0:No cycle-by-cycle trip event has occurred. 1:Indicates a trip event has occurred on a signal selected as a cycle-by-cycle trip source. The TZFLG[CBC] bit will remain set until it is manually cleared by the user. If the cycle-by-cycle trip event is still present when the CBC bit is cleared, then CBC will be immediately set again. The specified condition on the signal is automatically cleared when the EPWM time-base counter reaches zero [TBCTR = 0x00] if the trip condition is no longer present. The condition on the signal is only cleared when the TBCTR = 0x00 no matter where in the cycle the CBC flag is cleared. This bit is cleared by Writing the appropriate value to the TZCLR register.
0	INT	R	0h	Latched Trip Interrupt Status Flag 0:Indicates no interrupt has been generated. 1:Indicates an EPWMx_TZINT VIM interrupt was generated because of a trip condition. No further EPWMx_TZINT VIM interrupts will be generated until this flag is cleared. If the interrupt flag is cleared when either CBC or OST is set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. This bit is cleared by Writing the appropriate value to the TZCLR register.

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3.8.2.57 EPWM_TZCBCFLG Register

3.8.2.57.1 EPWM_TZCBCFLG Register (Offset = 128h) [reset = 0h]

Trip Zone CBC Flag Register.

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Figure 3-329. EPWM_TZCBCFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							CAPEVT
R							R
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-670. EPWM_TZCBCFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_1	R	0h	Reserved
8	CAPEVT	R	0h	Latched Status Flag for Capture Event 0:Indicates no trip event has occurred on CAPEVT 1:Indicates a trip event has occurred for the event defined for CAPEVT
7	DCBEVT2	R	0h	Latched Status Flag for Digital Compare B Output Event 2 Trip Latch 0:Reading a 0 indicates that no trip has occurred on DCBEVT2. 1:Reading a 1 indicates a trip has occured on the DCBEVT2 selected event.
6	DCAEVT2	R	0h	Latched Status Flag for Digital Compare A Output Event 2 Trip Latch 0:Reading a 0 indicates that no trip has occurred on DCAEVT2. 1:Reading a 1 indicates a trip has occured on the DCAEVT2 selected event.
5	CBC6	R	0h	Latched Status Flag for CBC6 Trip Latch 0:Reading a 0 indicates that no trip has occurred on CBC6. 1:Reading a 1 indicates a trip has occured on the CBC6 selected event.
4	CBC5	R	0h	Latched Status Flag for CBC5 Trip Latch 0:Reading a 0 indicates that no trip has occurred on CBC5. 1:Reading a 1 indicates a trip has occured on the CBC5 selected event.
3	CBC4	R	0h	Latched Status Flag for CBC4 Trip Latch 0:Reading a 0 indicates that no trip has occurred on CBC4. 1:Reading a 1 indicates a trip has occured on the CBC4 selected event.
2	CBC3	R	0h	Latched Status Flag for CBC3 Trip Latch 0:Reading a 0 indicates that no trip has occurred on CBC3. 1:Reading a 1 indicates a trip has occured on the CBC3 selected event.
1	CBC2	R	0h	Latched Status Flag for CBC2 Trip Latch 0:Reading a 0 indicates that no trip has occurred on CBC2. 1:Reading a 1 indicates a trip has occured on the CBC2 selected event.
0	CBC1	R	0h	Latched Status Flag for CBC1 Trip Latch 0:Reading a 0 indicates that no trip has occurred on CBC1. 1:Reading a 1 indicates a trip has occured on the CBC1 selected event.

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3.8.2.58 EPWM_TZOSTFLG Register

3.8.2.58.1 EPWM_TZOSTFLG Register (Offset = 12Ah) [reset = 0h]

Trip Zone OST Flag Register.

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Figure 3-330. EPWM_TZOSTFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							CAPEVT
R							R
0h							0h
7	6	5	4	3	2	1	0
DCBEVT1	DCAEVT1	OST6	OST5	OST4	OST3	OST2	OST1
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-671. EPWM_TZOSTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_1	R	0h	Reserved
8	CAPEVT	R	0h	Latched Status Flag for Capture Event 0:Indicates no trip event has occurred on CAPEVT 1:Indicates a trip event has occurred for the event defined for CAPEVT
7	DCBEVT1	R	0h	Latched Status Flag for Digital Compare B Output Event 1 Trip Latch 0:Reading a 0 indicates that no trip has occurred on DCBEVT1. 1:Reading a 1 indicates a trip has occured on the DCBEVT1 selected event.
6	DCAEVT1	R	0h	Latched Status Flag for Digital Compare A Output Event 1 Trip Latch 0:Reading a 0 indicates that no trip has occurred on DCAEVT1. 1:Reading a 1 indicates a trip has occured on the DCAEVT1 selected event.
5	OST6	R	0h	Latched Status Flag for OST6 Trip Latch 0:Reading a 0 indicates that no trip has occurred on OST6. 1:Reading a 1 indicates a trip has occured on the OST6 selected event.
4	OST5	R	0h	Latched Status Flag for OST5 Trip Latch 0:Reading a 0 indicates that no trip has occurred on OST5. 1:Reading a 1 indicates a trip has occured on the OST5 selected event.
3	OST4	R	0h	Latched Status Flag for OST4 Trip Latch 0:Reading a 0 indicates that no trip has occurred on OST4. 1:Reading a 1 indicates a trip has occured on the OST4 selected event.
2	OST3	R	0h	Latched Status Flag for OST3 Trip Latch 0:Reading a 0 indicates that no trip has occurred on OST3. 1:Reading a 1 indicates a trip has occured on the OST3 selected event.
1	OST2	R	0h	Latched Status Flag for OST2 Trip Latch 0:Reading a 0 indicates that no trip has occurred on OST2. 1:Reading a 1 indicates a trip has occured on the OST2 selected event.
0	OST1	R	0h	Latched Status Flag for OST1 Trip Latch 0:Reading a 0 indicates that no trip has occurred on OST1. 1:Reading a 1 indicates a trip has occured on the OST1 selected event.

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3.8.2.59 EPWM_TZCLR Register

3.8.2.59.1 EPWM_TZCLR Register (Offset = 12Eh) [reset = 0h]

Trip Zone Clear Register.

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Figure 3-331. EPWM_TZCLR Name Register

15	14	13	12	11	10	9	8
CBCPULSE		RESERVED_1					
R/W		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAPEVT	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	INT
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-672. EPWM_TZCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CBCPULSE	R/W	0h	Clear Pulse for Cycle-By-Cycle [CBC] Trip Latch This bit field determines which pulse clears the CBC trip latch. 00:CTR = zero pulse clears CBC trip latch. [Same as legacy designs.] 01:CTR = PRD pulse clears CBC trip latch. 10:CTR = zero or CTR = PRD pulse clears CBC trip latch. 11:CBC trip latch is not cleared
13:8	RESERVED_1	R	0h	Reserved
7	CAPEVT	R/W1TS	0h	Clear Flag for Capture Event 0:Writing 0 has no effect. This bit always reads back 0. 1:Writing 1 clears the CAPEVT event trip condition.
6	DCBEVT2	R/W1TS	0h	Clear Flag for Digital Compare Output B Event 2 0:Writing 0 has no effect. This bit always reads back 0. 1:Writing 1 clears the DCBEVT2 event trip condition.
5	DCBEVT1	R/W1TS	0h	Clear Flag for Digital Compare Output B Event 1 0:Writing 0 has no effect. This bit always reads back 0. 1:Writing 1 clears the DCBEVT1 event trip condition.
4	DCAEVT2	R/W1TS	0h	Clear Flag for Digital Compare Output A Event 2 0:Writing 0 has no effect. This bit always reads back 0. 1:Writing 1 clears the DCAEVT2 event trip condition.
3	DCAEVT1	R/W1TS	0h	Clear Flag for Digital Compare Output A Event 1 0:Writing 0 has no effect. This bit always reads back 0. 1:Writing 1 clears the DCAEVT1 event trip condition.
2	OST	R/W1TS	0h	Clear Flag for One-Shot Trip [OST] Latch 0:Has no effect. Always reads back a 0. 1:Clears this Trip [set] condition.
1	CBC	R/W1TS	0h	Clear Flag for Cycle-By-Cycle [CBC] Trip Latch 0:Has no effect. Always reads back a 0. 1:Clears this Trip [set] condition.
0	INT	R/W1TS	0h	Global Interrupt Clear Flag 0:Has no effect. Always reads back a 0. 1:Clears the trip-interrupt flag for this EPWM module [TZFLG[INT]]. NOTE: No further EPWMx_TZINT VIM interrupts will be generated until the flag is cleared. If the TZFLG[INT] bit is cleared and any of the other flag bits are set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts.

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3.8.2.60 EPWM_TZCBCCLR Register

3.8.2.60.1 EPWM_TZCBCCLR Register (Offset = 130h) [reset = 0h]

Trip Zone CBC Clear Register.

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Figure 3-332. EPWM_TZCBCCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1							CAPEVT
R							R/W1TS
0h							0h
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-673. EPWM_TZCBCCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_1	R	0h	Reserved
8	CAPEVT	R/W1TS	0h	Clear Flag for CAPEVT selected for CBC 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZCBCFLG[CAPEVT] bit.
7	DCBEVT2	R/W1TS	0h	Clear Flag for Digital Compare Output B Event 2 selected for CBC 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZCBCFLG[DCBEVT2] bit.
6	DCAEVT2	R/W1TS	0h	Clear Flag for Digital Compare Output A Event 2 selected for CBC 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZCBCFLG[DCAEVT2] bit.
5	CBC6	R/W1TS	0h	Clear Flag for Cycle-By-Cycle [CBC6] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZCBCFLG[CBC6] bit.
4	CBC5	R/W1TS	0h	Clear Flag for Cycle-By-Cycle [CBC5] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZCBCFLG[CBC5] bit.
3	CBC4	R/W1TS	0h	Clear Flag for Cycle-By-Cycle [CBC4] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZCBCFLG[CBC4] bit.
2	CBC3	R/W1TS	0h	Clear Flag for Cycle-By-Cycle [CBC3] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZCBCFLG[CBC3] bit.
1	CBC2	R/W1TS	0h	Clear Flag for Cycle-By-Cycle [CBC2] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZCBCFLG[CBC2] bit.
0	CBC1	R/W1TS	0h	Clear Flag for Cycle-By-Cycle [CBC1] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZCBCFLG[CBC1] bit.

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3.8.2.61 EPWM_TZOSTCLR Register

3.8.2.61.1 EPWM_TZOSTCLR Register (Offset = 132h) [reset = 0h]

Trip Zone OST Clear Register.

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Figure 3-333. EPWM_TZOSTCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1							CAPEVT
R							R/W1TS
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCBEVT1	DCAEVT1	OST6	OST5	OST4	OST3	OST2	OST1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-674. EPWM_TZOSTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_1	R	0h	Reserved
8	CAPEVT	R/W1TS	0h	Clear Flag for CAPEVT selected for OST 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZOSTFLG[CAPEVT] bit.
7	DCBEVT1	R/W1TS	0h	Clear Flag for Digital Compare Output B Event 1 selected for OST 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZOSTFLG[DCBEVT1] bit.
6	DCAEVT1	R/W1TS	0h	Clear Flag for Digital Compare Output A Event 1 selected for OST 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZOSTFLG[DCAEVT1] bit.
5	OST6	R/W1TS	0h	Clear Flag for Oneshot [OST6] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZOSTFLG[OST6] bit.
4	OST5	R/W1TS	0h	Clear Flag for Oneshot [OST5] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZOSTFLG[OST5] bit.
3	OST4	R/W1TS	0h	Clear Flag for Oneshot [OST4] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZOSTFLG[OST4] bit.
2	OST3	R/W1TS	0h	Clear Flag for Oneshot [OST3] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZOSTFLG[OST3] bit.
1	OST2	R/W1TS	0h	Clear Flag for Oneshot [OST2] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZOSTFLG[OST2] bit.
0	OST1	R/W1TS	0h	Clear Flag for Oneshot [OST1] Trip Latch 0:Writing a 0 has no effect. 1:Writing a 1 will clear the TZOSTFLG[OST1] bit.

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3.8.2.62 EPWM_TZFRC Register

3.8.2.62.1 EPWM_TZFRC Register (Offset = 136h) [reset = 0h]

Trip Zone Force Register.

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Figure 3-334. EPWM_TZFRC Name Register

15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAPEVT	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	RESERVED_1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-675. EPWM_TZFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_2	R	0h	Reserved
7	CAPEVT	R/W1TS	0h	Force Flag for Capture Event Output 0:Writing 0 has no effect. This bit always reads back 0. 1:Writing 1 forces the CAPEVT event trip condition and sets the TZFLG[CAPEVT] bit.
6	DCBEVT2	R/W1TS	0h	Force Flag for Digital Compare Output B Event 2 0:Writing 0 has no effect. This bit always reads back 0. 1:Writing 1 forces the DCBEVT2 event trip condition and sets the TZFLG[DCBEVT2] bit.
5	DCBEVT1	R/W1TS	0h	Force Flag for Digital Compare Output B Event 1 0:Writing 0 has no effect. This bit always reads back 0. 1:Writing 1 forces the DCBEVT1 event trip condition and sets the TZFLG[DCBEVT1] bit.
4	DCAEVT2	R/W1TS	0h	Force Flag for Digital Compare Output A Event 2 0:Writing 0 has no effect. This bit always reads back 0. 1:Writing 1 forces the DCAEVT2 event trip condition and sets the TZFLG[DCAEVT2] bit.
3	DCAEVT1	R/W1TS	0h	Force Flag for Digital Compare Output A Event 1 0:Writing 0 has no effect. This bit always reads back 0 1:Writing 1 forces the DCAEVT1 event trip condition and sets the TZFLG[DCAEVT1] bit.
2	OST	R/W1TS	0h	Force a One-Shot Trip Event via Software 0:Writing of 0 is ignored. Always reads back a 0. 1:Forces a one-shot trip event and sets the TZFLG[OST] bit.
1	CBC	R/W1TS	0h	Force a Cycle-by-Cycle Trip Event via Software 0:Writing of 0 is ignored. Always reads back a 0. 1:Forces a cycle-by-cycle trip event and sets the TZFLG[CBC] bit.
0	RESERVED_1	R	0h	Reserved

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3.8.2.63 EPWM_TZTRIPOUTSEL Register

3.8.2.63.1 EPWM_TZTRIPOUTSEL Register (Offset = 13Ah) [reset = 0h]

Trip Zone Force Register.

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Figure 3-335. EPWM_TZTRIPOUTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1			CAPEVT	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TZ6	TZ5	TZ4	TZ3	TZ2	TZ1	CBC	OST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-676. EPWM_TZTRIPOUTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	CAPEVT	R/W	0h	CAPEVT Select 0:Disable TZ6 as a TRIPOUT source for this EPWM module 1:Enable TZ6 as a TRIPOUT source for this EPWM module
11	DCBEVT2	R/W	0h	DCBEVT2 Select 0:Disable TZ6 as a TRIPOUT source for this EPWM module 1:Enable TZ6 as a TRIPOUT source for this EPWM module
10	DCBEVT1	R/W	0h	DCBEVT1 Select 0:Disable TZ6 as a TRIPOUT source for this EPWM module 1:Enable TZ6 as a TRIPOUT source for this EPWM module
9	DCAEVT2	R/W	0h	DCAEVT2 Select 0:Disable TZ6 as a TRIPOUT source for this EPWM module 1:Enable TZ6 as a TRIPOUT source for this EPWM module
8	DCAEVT1	R/W	0h	DCAEVT1 Select 0:Disable TZ6 as a TRIPOUT source for this EPWM module 1:Enable TZ6 as a TRIPOUT source for this EPWM module
7	TZ6	R/W	0h	Trip-Zone 6 [TZ6] Select 0:Disable TZ6 as a TRIPOUT source for this EPWM module 1:Enable TZ6 as a TRIPOUT source for this EPWM module
6	TZ5	R/W	0h	Trip-Zone 5 [TZ5] Select 0:Disable TZ5 as a TRIPOUT source for this EPWM module 1:Enable TZ5 as a TRIPOUT source for this EPWM module
5	TZ4	R/W	0h	Trip-Zone 4 [TZ4] Select 0:Disable TZ4 as a TRIPOUT source for this EPWM module 1:Enable TZ4 as a TRIPOUT source for this EPWM module
4	TZ3	R/W	0h	Trip-Zone 3 [TZ3] Select 0:Disable TZ3 as a TRIPOUT source for this EPWM module 1:Enable TZ3 as a TRIPOUT source for this EPWM module
3	TZ2	R/W	0h	Trip-Zone 2 [TZ2] Select 0:Disable TZ2 as a TRIPOUT source for this EPWM module 1:Enable TZ2 as a TRIPOUT source for this EPWM module
2	TZ1	R/W	0h	Trip-Zone 1 [TZ1] Select 0:Disable TZ1 as a TRIPOUT source for this EPWM module 1:Enable TZ1 as a TRIPOUT source for this EPWM module
1	CBC	R/W	0h	CBC Select 0:Disable TZ1 as a TRIPOUT source for this EPWM module 1:Enable TZ1 as a TRIPOUT source for this EPWM module

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Table 3-676. EPWM_TZTRIPOUTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OST	R/W	0h	OST Select 0:Disable TZ1 as a TRIPOUT source for this EPWM module 1:Enable TZ1 as a TRIPOUT source for this EPWM module

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3.8.2.64 EPWM_ETSEL Register

3.8.2.64.1 EPWM_ETSEL Register (Offset = 148h) [reset = 0h]

Event Trigger Selection Register.

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Figure 3-336. EPWM_ETSEL Name Register

15	14	13	12	11	10	9	8
SOCBEN	SOCBSEL			SOCAEN	SOCASEL		
R/W	R/W			R/W	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	INTSELCMP	SOCBSELCMP	SOCASELCMP	INTEN	INTSEL		
R	R/W	R/W	R/W	R/W	R/W		
0h	0h	0h	0h	0h	0h		

Table 3-677. EPWM_ETSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOCBEN	R/W	0h	Enable the ADC Start of Conversion B [EPWMxSOCB] Pulse 0:Disable EPWMxSOCB. 1:Enable EPWMxSOCB pulse.
14:12	SOCBSEL	R/W	0h	EPWMxSOCB Selection Options These bits determine when a EPWMxSOCB pulse will be generated. 000:Enable DCBEVT1.soc event 001:Enable event time-base counter equal to zero. [TBCTR = 0x00] 010:Enable event time-base counter equal to period [TBCTR = TBPRD] 011:Enable event time-base counter based on mixed events [ETSOCBMIX]. ETSOCBMIX is configured in the ETSOCBMIXEN register. 100:Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101:Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110:Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111:Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing [*] Event selected is determined by SOCBSELCMP bit.
11	SOCAEN	R/W	0h	Enable the ADC Start of Conversion A [EPWMxSOCA] Pulse 0:Disable EPWMxSOCA. 1:Enable EPWMxSOCA pulse.
10:8	SOCASEL	R/W	0h	EPWMxSOCA Selection Options These bits determine when a EPWMxSOCA pulse will be generated. 000:Enable DCAEVT1.soc event 001:Enable event time-base counter equal to zero. [TBCTR = 0x00] 010:Enable event time-base counter equal to period [TBCTR = TBPRD] 011:Enable event time-base counter based on mixed events [ETSOCAMIX]. ETSOCAMIX is configured in the ETSOCAMIXEN register. 100:Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101:Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110:Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111:Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing [*] Event selected is determined by SOCASELCMP bit.

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Table 3-677. EPWM_ETSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED_1	R	0h	Reserved
6	INTSELCMP	R/W	0h	EPWMxINT Compare Register Selection Options 0:Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to INTSEL selection mux. 1:Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to INTSEL selection mux.
5	SOCBSELCMP	R/W	0h	EPWMxSOCB Compare Register Selection Options 0:Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to SOCBSEL selection mux. 1:Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to SOCBSEL selection mux.
4	SOCASELCMP	R/W	0h	EPWMxSOCA Compare Register Selection Options 0:Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to SOCASEL selection mux. 1:Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to SOCASEL selection mux.
3	INTEN	R/W	0h	Enable EPWM Interrupt [EPWMx_INT] Generation 0:Disable EPWMx_INT generation 1:Enable EPWMx_INT generation
2:0	INTSEL	R/W	0h	EPWM Interrupt [EPWMx_INT] Selection Options 000:Reserved 001:Enable event time-base counter equal to zero. [TBCTR = 0x00] 010:Enable event time-base counter equal to period [TBCTR = TBPRD] 011:Enable event time-base counter based on mixed events [ETINTMIX]. ETINTMIX is configured in the ETINTMIXEN register. 100:Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101:Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110:Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111:Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing [*] Event selected is determined by INTSELCMP bit.

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3.8.2.65 EPWM_ETPS Register

3.8.2.65.1 EPWM_ETPS Register (Offset = 14Ch) [reset = 0h]

Event Trigger Pre-Scale Register.

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Figure 3-337. EPWM_ETPS Name Register

15	14	13	12	11	10	9	8
SOCBCNT		SOCBPRD		SOCACNT		SOCAPRD	
R		R/W		R		R/W	
0h		0h		0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1		SOCPSSEL	INTPSSEL	INTCNT		INTPRD	
R		R/W	R/W	R		R/W	
0h		0h	0h	0h		0h	

Table 3-678. EPWM_ETPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SOCBCNT	R	0h	EPWM ADC Start-of-Conversion B Event [EPWMxSOCB] Counter Register These bits indicate how many selected ETSEL[SOCBSEL] events have occurred: 00:No events have occurred. 01:1 event has occurred. 10:2 events have occurred. 11:3 events have occurred.
13:12	SOCBPRD	R/W	0h	EPWM ADC Start-of-Conversion B Event [EPWMxSOCB] Period Select These bits determine how many selected ETSEL[SOCBSEL] events need to occur before an EPWMxSOCB pulse is generated. To be generated, the pulse must be enabled [ETSEL[SOCBEN] = 1]. The SOCB pulse will be generated even if the status flag is set from a previous start of conversion [ETFLG[SOCB] = 1]. Once the SOCB pulse is generated, the ETPS[SOCBCNT] bits will automatically be cleared. 00:Disable the SOCB event counter. No EPWMxSOCB pulse will be generated 01:Generate the EPWMxSOCB pulse on the first event: ETPS[SOCBCNT] = 2'b01 10:Generate the EPWMxSOCB pulse on the second event: ETPS[SOCBCNT] = 2'b10 11:Generate the EPWMxSOCB pulse on the third event: ETPS[SOCBCNT] = 2'b11
11:10	SOCACNT	R	0h	EPWM ADC Start-of-Conversion A Event [EPWMxSOCA] Counter Register These bits indicate how many selected ETSEL[SOCASEL] events have occurred: 00:No events have occurred. 01:1 event has occurred. 10:2 events have occurred. 11:3 events have occurred.

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Table 3-678. EPWM_ETPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	SOCAPRD	R/W	0h	EPWM ADC Start-of-Conversion A Event [EPWMxSOCA] Period Select These bits determine how many selected ETSEL[SOCASEL] events need to occur before an EPWMxSOCA pulse is generated. To be generated, the pulse must be enabled [ETSEL[SOCAEN] = 1]. The SOCA pulse will be generated even if the status flag is set from a previous start of conversion [ETFLG[SOCA] = 1]. Once the SOCA pulse is generated, the ETPS[SOCACNT] bits will automatically be cleared. 00:Disable the SOCA event counter. No EPWMxSOCA pulse will be generated 01:Generate the EPWMxSOCA pulse on the first event: ETPS[SOCACNT] = 2'b01 10:Generate the EPWMxSOCA pulse on the second event: ETPS[SOCACNT] = 2'b10 11:Generate the EPWMxSOCA pulse on the third event: ETPS[SOCACNT] = 2'b11
7:6	RESERVED_1	R	0h	Reserved
5	SOCPSSEL	R/W	0h	EPWMxSOC A/B Pre-Scale Selection Bits 0:Selects ETPS [SOCACNT/SOCBCNT] and [SOCAPRD/SOCBPRD] registers to determine frequency of events [interrupt once every 0-3 events]. 1:Selects ETSOCPS [SOCACNT2/SOCBCNT2] and [SOCAPRD2/SOCBPRD2] registers to determine frequency of events [interrupt once every 0-15 events].
4	INTPSSEL	R/W	0h	EPWMxINTn Pre-Scale Selection Bits 0:Selects ETPS [INTCNT, and INTPRD] registers to determine frequency of events [interrupt once every 0-3 events]. 1:Selects ETINTPS [INTCNT2, and INTPRD2] registers to determine frequency of events [interrupt once every 0-15 events].
3:2	INTCNT	R	0h	EPWM Interrupt Event [EPWMx_INT] Counter Register These bits indicate how many selected ETSEL[INTSEL] events have occurred. These bits are automatically cleared when an interrupt pulse is generated. If interrupts are disabled, ETSEL[INT] = 0 or the interrupt flag is set, ETFLG[INT] = 1, the counter will stop counting events when it reaches the period value ETPS[INTCNT] = ETPS[INTPRD]. 00:No events have occurred. 01:1 event has occurred. 10:2 events have occurred. 11:3 events have occurred.
1:0	INTPRD	R/W	0h	EPWM Interrupt [EPWMx_INT] Period Select These bits determine how many selected ETSEL[INTSEL] events need to occur before an interrupt is generated. To be generated, the interrupt must be enabled [ETSEL[INT] = 1]. If the interrupt status flag is set from a previous interrupt [ETFLG[INT] = 1] then no interrupt will be generated until the flag is cleared via the ETCLR[INT] bit. This allows for one interrupt to be pending while another is still being serviced. Once the interrupt is generated, the ETPS[INTCNT] bits will automatically be cleared. Writing a INTPRD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear. Writing a INTPRD value that is less than the current counter value will result in an undefined state. If a counter event occurs at the same instant as a new zero or non-zero INTPRD value is written, the counter is incremented. 00:Disable the interrupt event counter. No interrupt will be generated and ETFRC[INT] is ignored. 01:Generate an interrupt on the first event INTCNT = 01 [first event] 10:Generate interrupt on ETPS[INTCNT] = 2'b10 [second event] 11:Generate interrupt on ETPS[INTCNT] = 2'b11 [third event]

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3.8.2.66 EPWM_ETFLG Register

3.8.2.66.1 EPWM_ETFLG Register (Offset = 150h) [reset = 0h]

Event Trigger Flag Register.

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Figure 3-338. EPWM_ETFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_2				SOCB	SOCA	RESERVED_1	INT
R				R	R	R	R
0h				0h	0h	0h	0h

Table 3-679. EPWM_ETFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_2	R	0h	Reserved
3	SOCB	R	0h	Latched EPWM ADC Start-of-Conversion A [EPWMxSOCB] Status Flag Unlike the ETFLG[INT] flag, the EPWMxSOCB output will continue to pulse even if the flag bit is set. 0:Indicates no event occurred 1:Indicates that a start of conversion pulse was generated on EPWMxSOCB. The EPWMxSOCB output will continue to be generated even if the flag bit is set.
2	SOCA	R	0h	Latched EPWM ADC Start-of-Conversion A [EPWMxSOCA] Status Flag Unlike the ETFLG[INT] flag, the EPWMxSOCA output will continue to pulse even if the flag bit is set. 0:Indicates no event occurred 1:Indicates that a start of conversion pulse was generated on EPWMxSOCA. The EPWMxSOCA output will continue to be generated even if the flag bit is set.
1	RESERVED_1	R	0h	Reserved
0	INT	R	0h	Latched EPWM Interrupt [EPWMx_INT] Status Flag 0:Indicates no event occurred 1:Indicates that an EPWMx interrupt [EPWMx_INT] was generated. No further interrupts will be generated until the flag bit is cleared. Up to one interrupt can be pending while the ETFLG[INT] bit is still set. If an interrupt is pending, it will not be generated until after the ETFLG[INT] bit is cleared.

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3.8.2.67 EPWM_ETCLR Register

3.8.2.67.1 EPWM_ETCLR Register (Offset = 154h) [reset = 0h]

Event Trigger Clear Register.

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Figure 3-339. EPWM_ETCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2				SOCB	SOCA	RESERVED_1	INT
R				R/W1TS	R/W1TS	R	R/W1TS
0h				0h	0h	0h	0h

Table 3-680. EPWM_ETCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_2	R	0h	Reserved
3	SOCB	R/W1TS	0h	EPWM ADC Start-of-Conversion A [EPWMxSOCB] Flag Clear Bit 0:Writing a 0 has no effect. Always reads back a 0 1:Clears the ETFLG[SOCB] flag bit
2	SOCA	R/W1TS	0h	EPWM ADC Start-of-Conversion A [EPWMxSOCA] Flag Clear Bit 0:Writing a 0 has no effect. Always reads back a 0 1:Clears the ETFLG[SOCA] flag bit
1	RESERVED_1	R	0h	Reserved
0	INT	R/W1TS	0h	EPWM Interrupt [EPWMx_INT] Flag Clear Bit 0:Writing a 0 has no effect. Always reads back a 0 1:Clears the ETFLG[INT] flag bit and enable further interrupts pulses to be generated

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3.8.2.68 EPWM_ETFRC Register

3.8.2.68.1 EPWM_ETFRC Register (Offset = 158h) [reset = 0h]

Event Trigger Force Register.

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Figure 3-340. EPWM_ETFRC Name Register

15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2				SOCB	SOCA	RESERVED_1	INT
R				R/W1TS	R/W1TS	R	R/W1TS
0h				0h	0h	0h	0h

Table 3-681. EPWM_ETFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_2	R	0h	Reserved
3	SOCB	R/W1TS	0h	SOCB Force Bit The SOCB pulse will only be generated if the event is enabled in the ETSEL register. The ETFLG[SOCB] flag bit will be set regardless. 0:Writing 0 to this bit will be ignored. Always reads back a 0. 1:Generates a pulse on EPWMxSOCB and set the SOCBFLG bit. This bit is used for test purposes.
2	SOCA	R/W1TS	0h	SOCA Force Bit The SOCA pulse will only be generated if the event is enabled in the ETSEL register. The ETFLG[SOCA] flag bit will be set regardless. 0:Writing 0 to this bit will be ignored. Always reads back a 0. 1:Generates a pulse on EPWMxSOCA and set the SOCAFLG bit. This bit is used for test purposes.
1	RESERVED_1	R	0h	Reserved
0	INT	R/W1TS	0h	INT Force Bit The interrupt will only be generated if the event is enabled in the ETSEL register. The INT flag bit will be set regardless. 0:Writing 0 to this bit will be ignored. Always reads back a 0. 1:Generates an interrupt on EPWMxINT and set the INT flag bit. This bit is used for test purposes.

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3.8.2.69 EPWM_ETINTPS Register

3.8.2.69.1 EPWM_ETINTPS Register (Offset = 15Ch) [reset = 0h]

Event-Trigger Interrupt Pre-Scale Register.

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Figure 3-341. EPWM_ETINTPS Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTCNT2				INTPRD2			
R				R/W			
0h				0h			

Table 3-682. EPWM_ETINTPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7:4	INTCNT2	R	0h	EPWMxINT Counter 2 When ETPS[INTPSSEL]=1, these bits indicate how many selected events have occurred: 0000 No events 0001 1 event 0010 2 events 0011 3 events 0100 4 events ... 1111 15 events
3:0	INTPRD2	R/W	0h	EPWMxINT Period 2 Select When ETPS[INTPSSEL] = 1, these bits select how many selected events need to occur before an interrupt is generated: 0000 Disable counter 0001 Generate interrupt on INTCNT = 1 [first event] 0010 Generate interrupt on INTCNT = 2 [second event] 0011 Generate interrupt on INTCNT = 3 [third event] 0100 Generate interrupt on INTCNT = 4 [fourth event] ... 1111 Generate interrupt on INTCNT = 15 [fifteenth event]

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3.8.2.70 EPWM_ETSOCPS Register

3.8.2.70.1 EPWM_ETSOCPS Register (Offset = 160h) [reset = 0h]

Event-Trigger SOC Pre-Scale Register.

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Figure 3-342. EPWM_ETSOCPS Name Register

15	14	13	12	11	10	9	8
SOCBCNT2				SOCBPRD2			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SOCACNT2				SOCAPRD2			
R				R/W			
0h				0h			

Table 3-683. EPWM_ETSOCPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	SOCBCNT2	R	0h	EPWMxSOCB Counter 2 When ETPS[SOCPSSEL] = 1, these bits indicate how many selected events have occurred: 0000 No events 0001 1 event 0010 2 events 0011 3 events 0100 4 events ... 1111 15 events
11:8	SOCBPRD2	R/W	0h	EPWMxSOCB Period 2 Select When ETPS[SOCPSSEL] = 1, these bits select how many selected event need to occur before an SOCB pulse is generated: 0000 Disable counter 0001 Generate interrupt on SOCBCNT2 = 1 [first event] 0010 Generate interrupt on SOCBCNT2 = 2 [second event] 0011 Generate interrupt on SOCBCNT2 = 3 [third event] 0100 Generate interrupt on SOCBCNT2 = 4 [fourth event] ... 1111 Generate interrupt on SOCBCNT2 = 15 [fifteenth event]
7:4	SOCACNT2	R	0h	EPWMxSOCA Counter 2 When ETPS[SOCPSSEL] = 1, these bits indicate how many selected events have occurred: 0000 No events 0001 1 event 0010 2 events 0011 3 events 0100 4 events ... 1111 15 events
3:0	SOCAPRD2	R/W	0h	EPWMxSOCA Period 2 Select When ETPS[SOCPSSEL] = 1, these bits select how many selected event need to occur before an SOCA pulse is generated: 0000 Disable counter 0001 Generate interrupt on SOCACNT2 = 1 [first event] 0010 Generate interrupt on SOCACNT2 = 2 [second event] 0011 Generate interrupt on SOCACNT2 = 3 [third event] 0100 Generate interrupt on SOCACNT2 = 4 [fourth event] ... 1111 Generate interrupt on SOCACNT2 = 15 [fifteenth event]

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3.8.2.71 EPWM_ETCNTINITCTL Register

3.8.2.71.1 EPWM_ETCNTINITCTL Register (Offset = 164h) [reset = 0h]

Event-Trigger Counter Initialization Control Register.

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Figure 3-343. EPWM_ETCNTINITCTL Name Register

15	14	13	12	11	10	9	8
SOCBINITEN	SOCAINITEN	INTINITEN	SOCBINITFRC	SOCAINITFRC	INTINITFRC	RESERVED_1	
R/W	R/W	R/W	R/W1TS	R/W1TS	R/W1TS	R	
0h	0h	0h	0h	0h	0h	0h	
7	6	5	4	3	2	1	0
RESERVED_1							
R							
0h							

Table 3-684. EPWM_ETCNTINITCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOCBINITEN	R/W	0h	EPWMxSOCB Counter 2 Initialization Enable 0:Has no effect. 1:Enable initialization of EPWMxSOCB counter with contents of ETCNTINIT[SOCBINIT] on a SYNC event or software force.
14	SOCAINITEN	R/W	0h	EPWMxSOCA Counter 2 Initialization Enable 0:Has no effect. 1:Enable initialization of EPWMxSOCA counter with contents of ETCNTINIT[SOCAINIT] on a SYNC event or software force.
13	INTINITEN	R/W	0h	EPWMxINT Counter 2 Initialization Enable 0:Has no effect. 1:Enable initialization of EPWMxINT counter 2 with contents of ETCNTINIT[INTINIT] on a SYNC event or software force.
12	SOCBINITFRC	R/W1TS	0h	EPWMxSOCB Counter 2 Initialization Force 0:Has no effect. 1:This bit forces the ET EPWMxSOCB counter to be initialized with the contents of ETCNTINIT[SOCBINIT].
11	SOCAINITFRC	R/W1TS	0h	EPWMxSOCA Counter 2 Initialization Force 0:Has no effect. 1:This bit forces the ET EPWMxSOCA counter to be initialized with the contents of ETCNTINIT[SOCAINIT].
10	INTINITFRC	R/W1TS	0h	EPWMxINT Counter 2 Initialization Force 0:Has no effect. 1:This bit forces the ET EPWMxINT counter to be initialized with the contents of ETCNTINIT[INTINIT].
9:0	RESERVED_1	R	0h	Reserved

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3.8.2.72 EPWM_ETCNTINIT Register

3.8.2.72.1 EPWM_ETCNTINIT Register (Offset = 168h) [reset = 0h]

Event-Trigger Counter Initialization Register.

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Figure 3-344. EPWM_ETCNTINIT Name Register

15	14	13	12	11	10	9	8
RESERVED_1				SOCBINIT			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
SOCAINIT				INTINIT			
R/W				R/W			
0h				0h			

Table 3-685. EPWM_ETCNTINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:8	SOCBINIT	R/W	0h	EPWMxSOCB Counter 2 Initialization Bits The ET EPWMxSOCB counter is initialized with the contents of this register on an EPWM SYNC event or a software force.
7:4	SOCAINIT	R/W	0h	EPWMxSOCA Counter 2 Initialization Bits The ET EPWMxSOCA counter is initialized with the contents of this register on an EPWM SYNC event or a software force.
3:0	INTINIT	R/W	0h	EPWMxINT Counter 2 Initialization Bits The ET EPWMxINT counter is initialized with the contents of this register on an EPWM SYNC event or a software force.

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3.8.2.73 EPWM_ETINTMIXEN Register

3.8.2.73.1 EPWM_ETINTMIXEN Register (Offset = 16Ch) [reset = 3h]

Event-Trigger Mixed INT Selection.

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Figure 3-345. EPWM_ETINTMIXEN Name Register

15	14	13	12	11	10	9	8
RESERVED_1					DCAEVT1	CDD	CDU
R					R/W	R/W	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	1h	1h

Table 3-686. EPWM_ETINTMIXEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10	DCAEVT1	R/W	0h	Enable DCAEVT1.inter to the mixed ET interrupt trigger signal [ETINTMIX]. 0:DCAEVT1.soc event is not enabled 1:Enable DCAEVT1.soc event
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the mixed ET interrupt trigger signal [ETINTMIX]. 0:CMPD down-count match enable event is not enabled 1:Enable CMPD down-count match enable event
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the mixed ET interrupt trigger signal [ETINTMIX]. 0:CMPD up-count match enable event is not enabled 1:Enable CMPD up-count match enable event
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the mixed ET interrupt trigger signal [ETINTMIX]. 0:CMPC down-count match enable event is not enabled 1:Enable CMPC down-count match enable event
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the mixed ET interrupt trigger signal [ETINTMIX]. 0:CMPC up-count match enable event is not enabled 1:Enable CMPC up-count match enable event
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the mixed ET interrupt trigger signal [ETINTMIX]. 0:CMPB down-count match enable event is not enabled 1:Enable CMPB down-count match enable event
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET interrupt trigger signal [ETINTMIX]. 0:CMPB up-count match enable event is not enabled 1:Enable CMPB up-count match enable event
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the mixed ET interrupt trigger signal [ETINTMIX]. 0:CMPA down-count match enable event is not enabled 1:Enable CMPA down-count match enable event
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the mixed ET interrupt trigger signal [ETINTMIX]. 0:CMPA up-count match enable event is not enabled 1:Enable CMPA up-count match enable event

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Table 3-686. EPWM_ETINTMIXEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PRD	R/W	1h	Enable event time-base counter equal to period [TBCTR = TBPRD] to the mixed ET interrupt trigger signal [ETINTMIX]. 0:Period match event is not enabled 1:Enable period match event
0	ZRO	R/W	1h	Enable event time-base counter equal to zero [TBCTR = 0x00] to the mixed ET interrupt trigger signal [ETINTMIX]. 0:Zero match event is not enabled 1:Enable zero match event

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3.8.2.74 EPWM_ETSOCAMIXEN Register

3.8.2.74.1 EPWM_ETSOCAMIXEN Register (Offset = 170h) [reset = 3h]

Event-Trigger Mixed SOCA Selection.

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Figure 3-346. EPWM_ETSOCAMIXEN Name Register

15	14	13	12	11	10	9	8
RESERVED_1					DCAEVT1	CDD	CDU
R					R/W	R/W	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	1h	1h

Table 3-687. EPWM_ETSOCAMIXEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10	DCAEVT1	R/W	0h	Enable DCAEVT1.inter to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:DCAEVT1.soc event is not enabled 1:Enable DCAEVT1.soc event
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:CMPD down-count match enable event is not enabled 1:Enable CMPD down-count match enable event
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:CMPD up-count match enable event is not enabled 1:Enable CMPD up-count match enable event
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:CMPC down-count match enable event is not enabled 1:Enable CMPC down-count match enable event
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:CMPC up-count match enable event is not enabled 1:Enable CMPC up-count match enable event
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:CMPB down-count match enable event is not enabled 1:Enable CMPB down-count match enable event
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:CMPB up-count match enable event is not enabled 1:Enable CMPB up-count match enable event
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:CMPA down-count match enable event is not enabled 1:Enable CMPA down-count match enable event
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:CMPA up-count match enable event is not enabled 1:Enable CMPA up-count match enable event

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Table 3-687. EPWM_ETSOCAMIXEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PRD	R/W	1h	Enable event time-base counter equal to period [TBCTR = TBPRD] to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:Period match event is not enabled 1:Enable period match event
0	ZRO	R/W	1h	Enable event time-base counter equal to zero [TBCTR = 0x00] to the mixed ET SOCA trigger signal [ETSOCAMIX]. 0:Zero match event is not enabled 1:Enable zero match event

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3.8.2.75 EPWM_ETSOCBMIXEN Register

3.8.2.75.1 EPWM_ETSOCBMIXEN Register (Offset = 174h) [reset = 3h]

Event-Trigger Mixed SOCB Selection.

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Figure 3-347. EPWM_ETSOCBMIXEN Name Register

15	14	13	12	11	10	9	8
RESERVED_1					DCBEVT1	CDD	CDU
R					R/W	R/W	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	1h	1h

Table 3-688. EPWM_ETSOCBMIXEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10	DCBEVT1	R/W	0h	Enable DCBEVT1.inter to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:DCBEVT1.soc event is not enabled 1:Enable DCBEVT1.soc event
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:CMPD down-count match enable event is not enabled 1:Enable CMPD down-count match enable event
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:CMPD up-count match enable event is not enabled 1:Enable CMPD up-count match enable event
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:CMPC down-count match enable event is not enabled 1:Enable CMPC down-count match enable event
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:CMPC up-count match enable event is not enabled 1:Enable CMPC up-count match enable event
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:CMPB down-count match enable event is not enabled 1:Enable CMPB down-count match enable event
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:CMPB up-count match enable event is not enabled 1:Enable CMPB up-count match enable event
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:CMPA down-count match enable event is not enabled 1:Enable CMPA down-count match enable event
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:CMPA up-count match enable event is not enabled 1:Enable CMPA up-count match enable event

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Table 3-688. EPWM_ETSOCBMIXEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PRD	R/W	1h	Enable event time-base counter equal to period [TBCTR = TBPRD] to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:Period match event is not enabled 1:Enable period match event
0	ZRO	R/W	1h	Enable event time-base counter equal to zero [TBCTR = 0x00] to the mixed ET SOCB trigger signal [ETSOCBMIX]. 0:Zero match event is not enabled 1:Enable zero match event

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3.8.2.76 EPWM_DCTRIPSEL Register

3.8.2.76.1 EPWM_DCTRIPSEL Register (Offset = 180h) [reset = 0h]

Digital Compare Trip Select Register.

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Figure 3-348. EPWM_DCTRIPSEL Name Register

15	14	13	12	11	10	9	8
DCBLCOMPSEL				DCBHCOMPSEL			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCALCOMPSEL				DCAHCOMPSEL			
R/W				R/W			
0h				0h			

Table 3-689. EPWM_DCTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	DCBLCOMPSEL	R/W	0h	Digital Compare B Low Input Select Bits 0000 TRIPIN1 0001 TRIPIN2 0010 TRIPIN3 0011 TRIPIN4 ... 1011 TRIPIN12 1100 Reserved 1101 TRIPIN14 1110 TRIPIN15 1111 Trip combination input [all trip inputs selected by DCBLTRIPSEL register ORed together]
11:8	DCBHCOMPSEL	R/W	0h	Digital Compare B High Input Select Bits 0000 TRIPIN1 0001 TRIPIN2 0010 TRIPIN3 0011 TRIPIN4 ... 1011 TRIPIN12 1100 Reserved 1101 TRIPIN14 1110 TRIPIN15 1111 Trip combination input [all trip inputs selected by DCBHTRIPSEL register ORed together]
7:4	DCALCOMPSEL	R/W	0h	Digital Compare A Low Input Select Bits 0000 TRIPIN1 0001 TRIPIN2 0010 TRIPIN3 0011 TRIPIN4 ... 1011 TRIPIN12 1100 Reserved 1101 TRIPIN14 1110 TRIPIN15 1111 Trip combination input [all trip inputs selected by DCALTRIPSEL register ORed together]

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Table 3-689. EPWM_DCTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	DCAHCOMPSEL	R/W	0h	Digital Compare A High Input Select Bits 0000 TRIPIN1 0001 TRIPIN2 0010 TRIPIN3 0011 TRIPIN4 ... 1011 TRIPIN12 1100 Reserved 1101 TRIPIN14 1110 TRIPIN15 1111 Trip combination input [all trip inputs selected by DCAHTRIPSEL register ORed together]

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3.8.2.77 EPWM_DCACTL Register

3.8.2.77.1 EPWM_DCACTL Register (Offset = 186h) [reset = 0h]

Digital Compare A Control Register.

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Figure 3-349. EPWM_DCACTL Name Register

15	14	13	12	11	10	9	8
EVT2LAT	EVT2LATCLRSEL		EVT2LATSEL	RESERVED_1		EVT2FRCSYNCSEL	EVT2SRCSEL
R	R/W		R/W	R		R/W	R/W
0h	0h		0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVT1LAT	EVT1LATCLRSEL		EVT1LATSEL	EVT1SYNCE	EVT1SOCE	EVT1FRCSYNCSEL	EVT1SRCSEL
R	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h

Table 3-690. EPWM_DCACTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EVT2LAT	R	0h	Indicates the status of DCAEVT2LAT signal. 0 The DCAEVT2LAT latch is cleared. 1 The DCAEVT2LAT latch is set.
14:13	EVT2LATCLRSEL	R/W	0h	DCAEVT2 Latched clear source select: 00 CNT_ZERO event clears DCAEVT2 latch. 01 PRD_EQ event clears DCAEVT2 latch. 10 CNT_ZERO event or PRD_EQ event clears DCAEVT2 latch. 11 Reserved.
12	EVT2LATSEL	R/W	0h	DCAEVT2 Latched signal select: 0 Does not select the DCAEVT2 latched signal as source of DCAEVT2.force. 1 Selects the DCAEVT2 latched signal as source of DCAEVT2.force.
11:10	RESERVED_1	R	0h	Reserved
9	EVT2FRCSYNCSEL	R/W	0h	DCAEVT2 Force Synchronization Signal Select 0:Source is synchronized with EPWMCLK 1:Source is passed through asynchronously
8	EVT2SRCSEL	R/W	0h	DCAEVT2 Source Signal Select 0:Source Is DCAEVT2 Signal 1:Source Is DCEVTFILT Signal
7	EVT1LAT	R	0h	Indicates the status of DCAEVT1LAT signal. 0 The DCAEVT1LAT latch is cleared. 1 The DCAEVT1LAT latch is set.
6:5	EVT1LATCLRSEL	R/W	0h	DCAEVT1 Latched clear source select: 00 CNT_ZERO event clears DCAEVT1 latch. 01 PRD_EQ event clears DCAEVT1 latch. 10 CNT_ZERO event or PRD_EQ event clears DCAEVT1 latch. 11 Reserved.
4	EVT1LATSEL	R/W	0h	DCAEVT1 Latched signal select: 0 Does not select the DCAEVT1 latched signal as source of DCAEVT1.force. 1 Selects the DCAEVT1 latched signal as source of DCAEVT1.force.
3	EVT1SYNCE	R/W	0h	DCAEVT1 SYNC, Enable/Disable 0:SYNC Generation Disabled 1:SYNC Generation Enabled
2	EVT1SOCE	R/W	0h	DCAEVT1 SOC, Enable/Disable 0:SOC Generation Disabled 1:SOC Generation Enabled

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Table 3-690. EPWM_DCACTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EVT1FRCSYNCSEL	R/W	0h	DCAEVT1 Force Synchronization Signal Select 0:Source is synchronized with EPWMCLK 1:Source is passed through asynchronously
0	EVT1SRCSEL	R/W	0h	DCAEVT1 Source Signal Select 0:Source Is DCAEVT1 Signal 1:Source Is DCEVTFILT Signal

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3.8.2.78 EPWM_DCBCTL Register

3.8.2.78.1 EPWM_DCBCTL Register (Offset = 188h) [reset = 0h]

Digital Compare B Control Register.

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Figure 3-350. EPWM_DCBCTL Name Register

15	14	13	12	11	10	9	8
EVT2LAT	EVT2LATCLRSEL		EVT2LATSEL	RESERVED_1		EVT2FRCSYNCSEL	EVT2SRCSEL
R	R/W		R/W	R		R/W	R/W
0h	0h		0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVT1LAT	EVT1LATCLRSEL		EVT1LATSEL	EVT1SYNCE	EVT1SOCE	EVT1FRCSYNCSEL	EVT1SRCSEL
R	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	0h	0h	0h

Table 3-691. EPWM_DCBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EVT2LAT	R	0h	Indicates the status of DCBEVT2LAT signal. 0 The DCBEVT2LAT latch is cleared. 1 The DCBEVT2LAT latch is set.
14:13	EVT2LATCLRSEL	R/W	0h	DCBEVT2 Latched clear source select: 00 CNT_ZERO event clears DCBEVT2 latch. 01 PRD_EQ event clears DCBEVT2 latch. 10 CNT_ZERO event or PRD_EQ event clears DCBEVT2 latch. 11 Reserved.
12	EVT2LATSEL	R/W	0h	DCBEVT2 Latched signal select: 0 Does not select the DCBEVT2 latched signal as source of DCBEVT2.force. 1 Selects the DCBEVT2 latched signal as source of DCBEVT2.force.
11:10	RESERVED_1	R	0h	Reserved
9	EVT2FRCSYNCSEL	R/W	0h	DCBEVT2 Force Synchronization Signal Select 0:Source is synchronized with EPWMCLK 1:Source is passed through asynchronously
8	EVT2SRCSEL	R/W	0h	DCBEVT2 Source Signal Select 0:Source Is DCBEVT2 Signal 1:Source Is DCEVTFILT Signal
7	EVT1LAT	R	0h	Indicates the status of DCBEVT1LAT signal. 0 The DCBEVT1LAT latch is cleared. 1 The DCBEVT1LAT latch is set.
6:5	EVT1LATCLRSEL	R/W	0h	DCBEVT1 Latched clear source select: 00 CNT_ZERO event clears DCBEVT1 latch. 01 PRD_EQ event clears DCBEVT1 latch. 10 CNT_ZERO event or PRD_EQ event clears DCBEVT1 latch. 11 Reserved.
4	EVT1LATSEL	R/W	0h	DCBEVT1 Latched signal select: 0 Does not select the DCBEVT1 latched signal as source of DCBEVT1.force. 1 Selects the DCBEVT1 latched signal as source of DCBEVT1.force.
3	EVT1SYNCE	R/W	0h	DCBEVT1 SYNC, Enable/Disable 0:SYNC Generation Disabled 1:SYNC Generation Enabled
2	EVT1SOCE	R/W	0h	DCBEVT1 SOC, Enable/Disable 0:SOC Generation Disabled 1:SOC Generation Enabled

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Table 3-691. EPWM_DCBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EVT1FRCSYNCSEL	R/W	0h	DCBEVT1 Force Synchronization Signal Select 0:Source is synchronized with EPWMCLK 1:Source is passed through asynchronously
0	EVT1SRCSEL	R/W	0h	DCBEVT1 Source Signal Select 0:Source Is DCBEVT1 Signal 1:Source Is DCEVTFILT Signal

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3.8.2.79 EPWM_DCFCTL Register

3.8.2.79.1 EPWM_DCFCTL Register (Offset = 18Eh) [reset = 0h]

Digital Compare Filter Control Register.

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Figure 3-351. EPWM_DCFCTL Name Register

15	14	13	12	11	10	9	8
EDGESTATUS			EDGECOUNT			EDGEMODE	
R			R/W			R/W	
0h			0h			0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	EDGEFILTSEL	PULSESEL		BLANKINV	BLANKE	SRCSEL	
R	R/W	R/W		R/W	R/W	R/W	
0h	0h	0h		0h	0h	0h	

Table 3-692. EPWM_DCFCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	EDGESTATUS	R	0h	Edge Status: These bits reflect the total number of edges currently captured. When the value matches the EDGECOUNT, the status bits are set to zero. and a TBCLK wide pulse is generated which can then be output on the DCEVTFILT signal. The edge counter can be reset by Writing 000 to the EDGECOUNT value:
12:10	EDGECOUNT	R/W	0h	Edge Count: These bits select how many edges to count before generating a TBCLK wide pulse on the DCEVTFILT signal: 000:no edges, reset current EDGESTATUS bits to 3'b000 001:1 edge 010:2 edges 011:3 edges 100:4 edges 101:5 edges 110:6 edges 111:7 edges
9:8	EDGEMODE	R/W	0h	Edge Mode Select: 00:Low To High Edge 01:High To Low Edge 10:Both Edges 11:Reserved
7	RESERVED_1	R	0h	Reserved
6	EDGEFILTSEL	R/W	0h	Edge Filter Select: 0:Edge Filter Not Selected 1:Edge Filter Selected
5:4	PULSESEL	R/W	0h	Pulse Select For Blanking & Capture Alignment 00:Time-base counter equal to period [TBCTR = TBPRD] 01:Time-base counter equal to zero [TBCTR = 0x00] 10:Time-base counter equal to zero [TBCTR = 0x00] or period [TBCTR = TBPRD] 11:Blank Pulse Mix
3	BLANKINV	R/W	0h	Blanking Window Inversion 0:Blanking window not inverted 1:Blanking window inverted
2	BLANKE	R/W	0h	Blanking Window Enable/Disable 0:Blanking window is disabled 1:Blanking window is enabled

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Table 3-692. EPWM_DCFCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	SRCSEL	R/W	0h	Filter Block Signal Source Select 00:Source Is DCAEVT1 Signal 01:Source Is DCAEVT2 Signal 10:Source Is DCBEVT1 Signal 11:Source Is DCBEVT2 Signal

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3.8.2.80 EPWM_DCCAPCTL Register

3.8.2.80.1 EPWM_DCCAPCTL Register (Offset = 190h) [reset = 0h]

Digital Compare Capture Control Register.

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Figure 3-352. EPWM_DCCAPCTL Name Register

15	14	13	12	11	10	9	8
CAPMODE	CAPCLR	CAPSTS	RESERVED_1				
R/W	R/W1TS	R	R				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						SHDWMODE	CAPE
R						R/W	R/W
0h						0h	0h

Table 3-693. EPWM_DCCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CAPMODE	R/W	0h	Counter Capture Mode 0:When a DCEVTFILT occurs and the counter capture is enabled, then the current TBCNT value is captured in the active register. When the respective trip event occurs, further trip [capture] events are ignored until the next PRD_eq or CNT_zero event [as selected by the PULSESEL bit in the DCFCTL register] re-triggers the capture mechanism. If active mode is enabled, via SHDWMODE bit in DCC0PCTL register, CPU reads of this register will return the active register value. If shadow mode is enabled, via SHDWMODE bit in DCC0PCTL register, the active register is copied to the shadow register on the PRD_eq or CNT_zero event [whichever is selected by PULSESEL bit in DCFCTL register]. CPU reads of this register will return the shadow register value. 1:When a DCEVTFILT occurs and the counter capture is enabled, then the current TBCNT value is captured in the active register. When the respective trip event occurs - it will set the CAPSTS flag and further trip [capture] events are ignored until this bit is cleared. CAPSTS can be cleared by writing to CAPCLR bit in DCC0PCTL register and it re-triggers the capture mechanism. If active mode is enabled, via SHDWMODE bit in DCC0PCTL register, CPU reads of this register will return the active register value. If shadow mode is enabled, via SHDWMODE bit in DCC0PCTL register, the active register is copied to the shadow register on the PRD_eq or CNT_zero event [whichever is selected by PULSESEL bit in DCFCTL register]. CPU reads of this register will return the shadow register value.
14	CAPCLR	R/W1TS	0h	DC Capture Latched Status Clear Flag 0:Writing a 0 has no effect. 1:Writing a 1 will clear this CAPSTS [set] condition.
13	CAPSTS	R	0h	Latched Status Flag for Capture Event 0:No DC capture event occurred. 1:A DC capture event has occurred.
12:2	RESERVED_1	R	0h	Reserved

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Table 3-693. EPWM_DCCAPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SHDWMODE	R/W	0h	TBCTR Counter Capture Shadow Select Mode 0:Enable shadow mode. The DCC0P active register is copied to shadow register on a TBCTR = TBPRD or TBCTR = zero event as defined by the DCFCTL[PULSESEL] bit. CPU reads of the DCC0P register will return the shadow register contents. 1:Active Mode. In this mode the shadow register is disabled. CPU reads from the DCC0P register will always return the active register contents.
0	CAPE	R/W	0h	TBCTR Counter Capture Enable/Disable 0:Disable the time-base counter capture. 1:Enable the time-base counter capture.

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3.8.2.81 EPWM_DCFOFFSET Register

3.8.2.81.1 EPWM_DCFOFFSET Register (Offset = 192h) [reset = 0h]

Digital Compare Filter Offset Register .

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Figure 3-353. EPWM_DCFOFFSET Name Register

15	14	13	12	11	10	9	8
DCFOFFSET							
R/W							
0h							
7	6	5	4	3	2	1	0
DCFOFFSET							
R/W							
0h							

Table 3-694. EPWM_DCFOFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DCFOFFSET	R/W	0h	Blanking Window Offset These 16-bits specify the number of TBCLK cycles from the blanking window reference to the point when the blanking window is applied. The blanking window reference is either period or zero as defined by the DCFCTL[PULSESEL] bit. This offset register is shadowed and the active register is loaded at the reference point defined by DCFCTL[PULSESEL]. The offset counter is also initialized and begins to count down when the active register is loaded. When the counter expires, the blanking window is applied. If the blanking window is currently active, then the blanking window counter is restarted.

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3.8.2.82 EPWM_DCFOFFSETCNT Register

3.8.2.82.1 EPWM_DCFOFFSETCNT Register (Offset = 194h) [reset = 0h]

Digital Compare Filter Offset Counter Register.

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Figure 3-354. EPWM_DCFOFFSETCNT Name Register

15	14	13	12	11	10	9	8
DCFOFFSETCNT							
R							
0h							
7	6	5	4	3	2	1	0
DCFOFFSETCNT							
R							
0h							

Table 3-695. EPWM_DCFOFFSETCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DCFOFFSETCNT	R	0h	Blanking Offset Counter These 16-bits are read only and indicate the current value of the offset counter. The counter counts down to zero and then stops until it is re-loaded on the next period or zero event as defined by the DCFCTL[PULSESEL] bit. The offset counter is not affected by the free/soft emulation bits. That is, it will always continue to count down if the device is halted by a emulation stop.

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3.8.2.83 EPWM_DCFWINDOW Register

3.8.2.83.1 EPWM_DCFWINDOW Register (Offset = 196h) [reset = 0h]

Digital Compare Filter Window Register.

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Figure 3-355. EPWM_DCFWINDOW Name Register

15	14	13	12	11	10	9	8
DCFWINDOW							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCFWINDOW							
R/W							
0h							

Table 3-696. EPWM_DCFWINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DCFWINDOW	R/W	0h	Blanking Window Width 00h No blanking window is generated. 01-FFFFh: Specifies the width of the blanking window in TBCLK cycles. The blanking window begins when the offset counter expires. When this occurs, the window counter is loaded and begins to count down. If the blanking window is currently active and the offset counter expires, the blanking window counter is not restarted and the blanking window is cut short prematurely. Care should be taken to avoid this situation. The blanking window can cross a PWM period boundary.

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3.8.2.84 EPWM_DCFWINDOWCNT Register

3.8.2.84.1 EPWM_DCFWINDOWCNT Register (Offset = 198h) [reset = 0h]

Digital Compare Filter Window Counter Register.

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Figure 3-356. EPWM_DCFWINDOWCNT Name Register

15	14	13	12	11	10	9	8
DCFWINDOWCNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCFWINDOWCNT							
R							
0h							

Table 3-697. EPWM_DCFWINDOWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DCFWINDOWCNT	R	0h	Blanking Window Counter These 16 bits are read only and indicate the current value of the window counter. The counter counts down to zero and then stops until it is re-loaded when the offset counter reaches zero again.

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3.8.2.85 EPWM_BLANKPULSEMIXSEL Register

3.8.2.85.1 EPWM_BLANKPULSEMIXSEL Register (Offset = 19Ah) [reset = 0h]

Blanking window trigger pulse select register.

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Figure 3-357. EPWM_BLANKPULSEMIXSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CDD	CDU
R						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-698. EPWM_BLANKPULSEMIXSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the blanking window trigger [BLANKPULSEMIX]. 0:CMPD down-count match enable event is not enabled 1:Enable CMPD down-count match enable event
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the blanking window trigger [BLANKPULSEMIX]. 0:CMPD up-count match enable event is not enabled 1:Enable CMPD up-count match enable event
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the blanking window trigger [BLANKPULSEMIX]. 0:CMPC down-count match enable event is not enabled 1:Enable CMPC down-count match enable event
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the blanking window trigger [BLANKPULSEMIX]. 0:CMPC up-count match enable event is not enabled 1:Enable CMPC up-count match enable event
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the blanking window trigger [BLANKPULSEMIX]. 0:CMPB down-count match enable event is not enabled 1:Enable CMPB down-count match enable event
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET interrupt trigger signal [BLANKPULSEMIX]. 0:CMPB up-count match enable event is not enabled 1:Enable CMPB up-count match enable event
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the blanking window trigger [BLANKPULSEMIX]. 0:CMPA down-count match enable event is not enabled 1:Enable CMPA down-count match enable event
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the blanking window trigger [BLANKPULSEMIX]. 0:CMPA up-count match enable event is not enabled 1:Enable CMPA up-count match enable event
1	PRD	R/W	0h	Enable event time-base counter equal to period [TBCTR = TBPRD] to the blanking window trigger [BLANKPULSEMIX]. 0:Period match event is not enabled 1:Enable period match event

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Table 3-698. EPWM_BLANKPULSEMIXSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ZRO	R/W	0h	Enable event time-base counter equal to zero [TBCTR = 0x00] to the blanking window trigger [BLANKPULSEMIX]. 0:Zero match event is not enabled 1:Enable zero match event

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3.8.2.86 EPWM_DCCAPMIXSEL Register

3.8.2.86.1 EPWM_DCCAPMIXSEL Register (Offset = 19Ch) [reset = 0h]

Capture Event pulse select register.

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Figure 3-358. EPWM_DCCAPMIXSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CDD	CDU
R						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-699. EPWM_DCCAPMIXSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the blanking window trigger [DCC0PMIX]. 0:CMPD down-count match enable event is not enabled 1:Enable CMPD down-count match enable event
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the blanking window trigger [DCC0PMIX]. 0:CMPD up-count match enable event is not enabled 1:Enable CMPD up-count match enable event
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the blanking window trigger [DCC0PMIX]. 0:CMPC down-count match enable event is not enabled 1:Enable CMPC down-count match enable event
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the blanking window trigger [DCC0PMIX]. 0:CMPC up-count match enable event is not enabled 1:Enable CMPC up-count match enable event
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the blanking window trigger [DCC0PMIX]. 0:CMPB down-count match enable event is not enabled 1:Enable CMPB down-count match enable event
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET interrupt trigger signal [DCC0PMIX]. 0:CMPB up-count match enable event is not enabled 1:Enable CMPB up-count match enable event
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the blanking window trigger [DCC0PMIX]. 0:CMPA down-count match enable event is not enabled 1:Enable CMPA down-count match enable event
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the blanking window trigger [DCC0PMIX]. 0:CMPA up-count match enable event is not enabled 1:Enable CMPA up-count match enable event
1	PRD	R/W	0h	Enable event time-base counter equal to period [TBCTR = TBPRD] to the blanking window trigger [DCC0PMIX]. 0:Period match event is not enabled 1:Enable period match event

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Table 3-699. EPWM_DCCAPMIXSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ZRO	R/W	0h	Enable event time-base counter equal to zero [TBCTR = 0x00] to the blanking window trigger [DCC0PMIX]. 0:Zero match event is not enabled 1:Enable zero match event

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3.8.2.87 EPWM_DCCAP Register

3.8.2.87.1 EPWM_DCCAP Register (Offset = 19Eh) [reset = 0h]

Digital Compare Counter Capture Register .

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Figure 3-359. EPWM_DCCAP Name Register

15	14	13	12	11	10	9	8
DCCAP							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCCAP							
R							
0h							

Table 3-700. EPWM_DCCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DCCAP	R	0h	Digital Compare Time-Base Counter Capture To enable time-base counter capture, set the DCC0PCLT[CAPE] bit to 1. If enabled, reflects the value of the time-base counter [TBCTR] on the low to high edge transition of a filtered [DCEVTFLT] event. Further capture events are ignored until the next period or zero as selected by the DCFCTL[PULSESEL] bit. Shadowing of DCC0P is enabled and disabled by the DCC0PCTL[SHDWMODE] bit. By default this register is shadowed. - If DCC0PCTL[SHDWMODE] = 0, then the shadow is enabled. In this mode, the active register is copied to the shadow register on the TBCTR = TBPRD or TBCTR = zero as defined by the DCFCTL[PULSESEL] bit. CPU reads of this register will return the shadow register value. - If DCC0PCTL[SHDWMODE] = 1, then the shadow register is disabled. In this mode, CPU reads will return the active register value. The active and shadow registers share the same memory map address.

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3.8.2.88 EPWM_DCAHTRIPSEL Register

3.8.2.88.1 EPWM_DCAHTRIPSEL Register (Offset = 1A4h) [reset = 0h]

Digital Compare AH Trip Select .

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Figure 3-360. EPWM_DCAHTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-701. EPWM_DCAHTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0:Trip Input 15 not selected as combinational ORed input 1:Trip Input 15 selected as combinational ORed input to DCAH mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0:Trip Input 14 not selected as combinational ORed input 1:Trip Input 14 selected as combinational ORed input to DCAH mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0:Trip Input 13 not selected as combinational ORed input 1:Trip Input 13 selected as combinational ORed input to DCAH mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0:Trip Input 12 not selected as combinational ORed input 1:Trip Input 12 selected as combinational ORed input to DCAH mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0:Trip Input 11 not selected as combinational ORed input 1:Trip Input 11 selected as combinational ORed input to DCAH mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0:Trip Input 10 not selected as combinational ORed input 1:Trip Input 10 selected as combinational ORed input to DCAH mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0:Trip Input 9 not selected as combinational ORed input 1:Trip Input 9 selected as combinational ORed input to DCAH mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0:Trip Input 8 not selected as combinational ORed input 1:Trip Input 8 selected as combinational ORed input to DCAH mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0:Trip Input 7 not selected as combinational ORed input 1:Trip Input 7 selected as combinational ORed input to DCAH mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0:Trip Input 6 not selected as combinational ORed input 1:Trip Input 6 selected as combinational ORed input to DCAH mux
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0:Trip Input 5 not selected as combinational ORed input 1:Trip Input 5 selected as combinational ORed input to DCAH mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0:Trip Input 4 not selected as combinational ORed input 1:Trip Input 4 selected as combinational ORed input to DCAH mux

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Table 3-701. EPWM_DCAHTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0:Trip Input 3 not selected as combinational ORed input 1:Trip Input 3 selected as combinational ORed input to DCAH mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0:Trip Input 2 not selected as combinational ORed input 1:Trip Input 2 selected as combinational ORed input to DCAH mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0:Trip Input 1 not selected as combinational ORed input 1:Trip Input 1 selected as combinational ORed input to DCAH mux

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3.8.2.89 EPWM_DCALTRIPSEL Register

3.8.2.89.1 EPWM_DCALTRIPSEL Register (Offset = 1A6h) [reset = 0h]

Digital Compare AL Trip Select .

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Figure 3-361. EPWM_DCALTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-702. EPWM_DCALTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0:Trip Input 15 not selected as combinational ORed input 1:Trip Input 15 selected as combinational ORed input to DCAL mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0:Trip Input 14 not selected as combinational ORed input 1:Trip Input 14 selected as combinational ORed input to DCAL mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0:Trip Input 13 not selected as combinational ORed input 1:Trip Input 13 selected as combinational ORed input to DCAL mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0:Trip Input 12 not selected as combinational ORed input 1:Trip Input 12 selected as combinational ORed input to DCAL mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0:Trip Input 11 not selected as combinational ORed input 1:Trip Input 11 selected as combinational ORed input to DCAL mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0:Trip Input 10 not selected as combinational ORed input 1:Trip Input 10 selected as combinational ORed input to DCAL mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0:Trip Input 9 not selected as combinational ORed input 1:Trip Input 9 selected as combinational ORed input to DCAL mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0:Trip Input 8 not selected as combinational ORed input 1:Trip Input 8 selected as combinational ORed input to DCAL mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0:Trip Input 7 not selected as combinational ORed input 1:Trip Input 7 selected as combinational ORed input to DCAL mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0:Trip Input 6 not selected as combinational ORed input 1:Trip Input 6 selected as combinational ORed input to DCAL mux
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0:Trip Input 5 not selected as combinational ORed input 1:Trip Input 5 selected as combinational ORed input to DCAL mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0:Trip Input 4 not selected as combinational ORed input 1:Trip Input 4 selected as combinational ORed input to DCAL mux

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Table 3-702. EPWM_DCALTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0:Trip Input 3 not selected as combinational ORed input 1:Trip Input 3 selected as combinational ORed input to DCAL mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0:Trip Input 2 not selected as combinational ORed input 1:Trip Input 2 selected as combinational ORed input to DCAL mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0:Trip Input 1 not selected as combinational ORed input 1:Trip Input 1 selected as combinational ORed input to DCAL mux

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3.8.2.90 EPWM_DCBHTRIPSEL Register

3.8.2.90.1 EPWM_DCBHTRIPSEL Register (Offset = 1A8h) [reset = 0h]

Digital Compare BH Trip Select .

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Figure 3-362. EPWM_DCBHTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-703. EPWM_DCBHTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0:Trip Input 15 not selected as combinational ORed input 1:Trip Input 15 selected as combinational ORed input to DCBH mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0:Trip Input 14 not selected as combinational ORed input 1:Trip Input 14 selected as combinational ORed input to DCBH mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0:Trip Input 13 not selected as combinational ORed input 1:Trip Input 13 selected as combinational ORed input to DCBH mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0:Trip Input 12 not selected as combinational ORed input 1:Trip Input 12 selected as combinational ORed input to DCBH mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0:Trip Input 11 not selected as combinational ORed input 1:Trip Input 11 selected as combinational ORed input to DCBH mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0:Trip Input 10 not selected as combinational ORed input 1:Trip Input 10 selected as combinational ORed input to DCBH mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0:Trip Input 9 not selected as combinational ORed input 1:Trip Input 9 selected as combinational ORed input to DCBH mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0:Trip Input 8 not selected as combinational ORed input 1:Trip Input 8 selected as combinational ORed input to DCBH mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0:Trip Input 7 not selected as combinational ORed input 1:Trip Input 7 selected as combinational ORed input to DCBH mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0:Trip Input 6 not selected as combinational ORed input 1:Trip Input 6 selected as combinational ORed input to DCBH mux
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0:Trip Input 5 not selected as combinational ORed input 1:Trip Input 5 selected as combinational ORed input to DCBH mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0:Trip Input 4 not selected as combinational ORed input 1:Trip Input 4 selected as combinational ORed input to DCBH mux

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Table 3-703. EPWM_DCBHTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0:Trip Input 3 not selected as combinational ORed input 1:Trip Input 3 selected as combinational ORed input to DCBH mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0:Trip Input 2 not selected as combinational ORed input 1:Trip Input 2 selected as combinational ORed input to DCBH mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0:Trip Input 1 not selected as combinational ORed input 1:Trip Input 1 selected as combinational ORed input to DCBH mux

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3.8.2.91 EPWM_DCBLTRIPSEL Register

3.8.2.91.1 EPWM_DCBLTRIPSEL Register (Offset = 1AAh) [reset = 0h]

Digital Compare BL Trip Select .

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Figure 3-363. EPWM_DCBLTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-704. EPWM_DCBLTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0:Trip Input 15 not selected as combinational ORed input 1:Trip Input 15 selected as combinational ORed input to DCAL mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0:Trip Input 14 not selected as combinational ORed input 1:Trip Input 14 selected as combinational ORed input to DCAL mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0:Trip Input 13 not selected as combinational ORed input 1:Trip Input 13 selected as combinational ORed input to DCAL mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0:Trip Input 12 not selected as combinational ORed input 1:Trip Input 12 selected as combinational ORed input to DCAL mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0:Trip Input 11 not selected as combinational ORed input 1:Trip Input 11 selected as combinational ORed input to DCAL mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0:Trip Input 10 not selected as combinational ORed input 1:Trip Input 10 selected as combinational ORed input to DCAL mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0:Trip Input 9 not selected as combinational ORed input 1:Trip Input 9 selected as combinational ORed input to DCAL mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0:Trip Input 8 not selected as combinational ORed input 1:Trip Input 8 selected as combinational ORed input to DCAL mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0:Trip Input 7 not selected as combinational ORed input 1:Trip Input 7 selected as combinational ORed input to DCAL mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0:Trip Input 6 not selected as combinational ORed input 1:Trip Input 6 selected as combinational ORed input to DCAL mux
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0:Trip Input 5 not selected as combinational ORed input 1:Trip Input 5 selected as combinational ORed input to DCAL mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0:Trip Input 4 not selected as combinational ORed input 1:Trip Input 4 selected as combinational ORed input to DCAL mux

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Table 3-704. EPWM_DCBLTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0:Trip Input 3 not selected as combinational ORed input 1:Trip Input 3 selected as combinational ORed input to DCAL mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0:Trip Input 2 not selected as combinational ORed input 1:Trip Input 2 selected as combinational ORed input to DCAL mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0:Trip Input 1 not selected as combinational ORed input 1:Trip Input 1 selected as combinational ORed input to DCAL mux

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3.8.2.92 EPWM_CAPCTL Register

3.8.2.92.1 EPWM_CAPCTL Register (Offset = 1ACh) [reset = 0h]

Event Capture Control Register.

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Figure 3-364. EPWM_CAPCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_2							FRCLOAD
R							R/W1TS
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1			PULSECTL	CAPINPOL	CAPGATEPOL		SRCSEL
R			R/W	R/W	R/W		R/W
0h			0h	0h	0h		0h

Table 3-705. EPWM_CAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_2	R	0h	Reserved
8	FRCLOAD	R/W1TS	0h	0:Writing of 0 is ignored. Always reads back a 0. 1:Forces a LOAD to occur on the DCC0P - an equivalent LOAD.active pulse
7:5	RESERVED_1	R	0h	Reserved
4	PULSECTL	R/W	0h	Capture Input Polarity Select Mux: 0:Pulse selection determined by PULSESEL bits [common pulse selection for Blanking and Capture logic] 1:Pulse selection determined by CAPMIXSEL register [independent pulse selection for Blaning and Capture logic]
3	CAPINPOL	R/W	0h	Capture Input Polarity Select Mux: 0:CAPIN.sync not inverted 1:CAPIN.sync Inverted Default state assumption for these inputs can be active high. If the user is providing active low signal then invert option can be configured
2:1	CAPGATEPOL	R/W	0h	Capture Gate Input Polarity Select Mux: 00:Set to 1 - Gate is always ON 01:Set to 0 - Gate is always OFF 10:CAPGATE.sync 11:CAPGATE.sync Inverted Default state assumption for these inputs can be active high. If the user is providing active low signal then invert option can be configured
0	SRCSEL	R/W	0h	Capture Logic Input Select Mux: 0:DCEVTFILT [Sync] - same as Type-4 1:CAPIN.sync

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3.8.2.93 EPWM_CAPGATETRIPSEL Register

3.8.2.93.1 EPWM_CAPGATETRIPSEL Register (Offset = 1AEh) [reset = 0h]

Event Capture Gate Trip input select.

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Figure 3-365. EPWM_CAPGATETRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-706. EPWM_CAPGATETRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0:Trip Input 15 not selected as combinational ORed input 1:Trip Input 15 selected as combinational ORed input to CAPGATE mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0:Trip Input 14 not selected as combinational ORed input 1:Trip Input 14 selected as combinational ORed input to CAPGATE mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0:Trip Input 13 not selected as combinational ORed input 1:Trip Input 13 selected as combinational ORed input to CAPGATE mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0:Trip Input 12 not selected as combinational ORed input 1:Trip Input 12 selected as combinational ORed input to CAPGATE mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0:Trip Input 11 not selected as combinational ORed input 1:Trip Input 11 selected as combinational ORed input to CAPGATE mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0:Trip Input 10 not selected as combinational ORed input 1:Trip Input 10 selected as combinational ORed input to CAPGATE mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0:Trip Input 9 not selected as combinational ORed input 1:Trip Input 9 selected as combinational ORed input to CAPGATE mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0:Trip Input 8 not selected as combinational ORed input 1:Trip Input 8 selected as combinational ORed input to CAPGATE mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0:Trip Input 7 not selected as combinational ORed input 1:Trip Input 7 selected as combinational ORed input to CAPGATE mux

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Table 3-706. EPWM_CAPGATETRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0:Trip Input 6 not selected as combinational ORed input 1:Trip Input 6 selected as combinational ORed input to CAPGATE mux
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0:Trip Input 5 not selected as combinational ORed input 1:Trip Input 5 selected as combinational ORed input to CAPGATE mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0:Trip Input 4 not selected as combinational ORed input 1:Trip Input 4 selected as combinational ORed input to CAPGATE mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0:Trip Input 3 not selected as combinational ORed input 1:Trip Input 3 selected as combinational ORed input to CAPGATE mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0:Trip Input 2 not selected as combinational ORed input 1:Trip Input 2 selected as combinational ORed input to CAPGATE mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0:Trip Input 1 not selected as combinational ORed input 1:Trip Input 1 selected as combinational ORed input to CAPGATE mux

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3.8.2.94 EPWM_CAPINTRIPSEL Register

3.8.2.94.1 EPWM_CAPINTRIPSEL Register (Offset = 1B0h) [reset = 0h]

Event Capture Trip input select.

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Figure 3-366. EPWM_CAPINTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-707. EPWM_CAPINTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0:Trip Input 15 not selected as combinational ORed input 1:Trip Input 15 selected as combinational ORed input to CAPIN mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0:Trip Input 14 not selected as combinational ORed input 1:Trip Input 14 selected as combinational ORed input to CAPIN mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0:Trip Input 13 not selected as combinational ORed input 1:Trip Input 13 selected as combinational ORed input to CAPIN mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0:Trip Input 12 not selected as combinational ORed input 1:Trip Input 12 selected as combinational ORed input to CAPIN mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0:Trip Input 11 not selected as combinational ORed input 1:Trip Input 11 selected as combinational ORed input to CAPIN mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0:Trip Input 10 not selected as combinational ORed input 1:Trip Input 10 selected as combinational ORed input to CAPIN mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0:Trip Input 9 not selected as combinational ORed input 1:Trip Input 9 selected as combinational ORed input to CAPIN mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0:Trip Input 8 not selected as combinational ORed input 1:Trip Input 8 selected as combinational ORed input to CAPIN mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0:Trip Input 7 not selected as combinational ORed input 1:Trip Input 7 selected as combinational ORed input to CAPIN mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0:Trip Input 6 not selected as combinational ORed input 1:Trip Input 6 selected as combinational ORed input to CAPIN mux
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0:Trip Input 5 not selected as combinational ORed input 1:Trip Input 5 selected as combinational ORed input to CAPIN mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0:Trip Input 4 not selected as combinational ORed input 1:Trip Input 4 selected as combinational ORed input to CAPIN mux

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Table 3-707. EPWM_CAPINTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0:Trip Input 3 not selected as combinational ORed input 1:Trip Input 3 selected as combinational ORed input to CAPIN mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0:Trip Input 2 not selected as combinational ORed input 1:Trip Input 2 selected as combinational ORed input to CAPIN mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0:Trip Input 1 not selected as combinational ORed input 1:Trip Input 1 selected as combinational ORed input to CAPIN mux

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3.8.2.95 EPWM_CAPTRIPSEL Register

3.8.2.95.1 EPWM_CAPTRIPSEL Register (Offset = 1B2h) [reset = 0h]

Event Capture Signal Select.

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Figure 3-367. EPWM_CAPTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAPGATECOMPSEL				CAPINCOMPSEL			
R/W				R/W			
0h				0h			

Table 3-708. EPWM_CAPTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7:4	CAPGATECOMPSEL	R/W	0h	Digital Compare A Low Input Select Bits 0000 TRIPIN1 0001 TRIPIN2 0010 TRIPIN3 0011 TRIPIN4 ... 1011 TRIPIN12 1100 Reserved 1101 TRIPIN14 1110 TRIPIN15 1111 Trip combination input [all trip inputs selected by CAPGATETRIPSEL register ORed together]
3:0	CAPINCOMPSEL	R/W	0h	Digital Compare A High Input Select Bits 0000 TRIPIN1 0001 TRIPIN2 0010 TRIPIN3 0011 TRIPIN4 ... 1011 TRIPIN12 1100 Reserved 1101 TRIPIN14 1110 TRIPIN15 1111 Trip combination input [all trip inputs selected by CAPINTRIPSEL register ORed together]

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3.8.2.96 EPWM_EPWMLOCK Register

3.8.2.96.1 EPWM_EPWMLOCK Register (Offset = 1F4h) [reset = 0h]

EPWM Lock Register.

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Figure 3-368. EPWM_EPWMLOCK Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			DCLOCK	TZCLRLOCK	TZCFGLOCK	GLLOCK	HRLOCK
R			R/R/WONCE	R/R/WONCE	R/R/WONCE	R/R/WONCE	R/R/WONCE
0h			0h	0h	0h	0h	0h

Table 3-709. EPWM_EPWMLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	KEY	R/W	0h	Write to this register succeeds only if this field is written with a value of 0xa5a5 Note: [1] Due to this KEY, only 32-bit writes will succeed [provided the KEY matches]. 16-bit writes to the upper or lower half of this register will be ignored
15:5	RESERVED_1	R	0h	Reserved
4	DCLOCK	R/R/WONCE	0h	0:Digital Compare registers from 0xC0 to 0xD9 offsets are protected by EALLOW. 1:Digital Compare registers from 0xC0 and 0xD9 offsets are locked and not writable.
3	TZCLRLOCK	R/R/WONCE	0h	0:Digital Compare registers from 0x97 to 0x9B offsets are protected by EALLOW. 1:Digital Compare registers from 0x97 and 0x9B offsets are locked and not writable.
2	TZCFGLOCK	R/R/WONCE	0h	0:TripZone registers from 0x80 to 0x8D and TZTRIPOUTSEL at 0x9D offsets are protected by EALLOW. 1:TripZone registers from 0x80 and 0x8D and TZTRIPOUTSEL at 0x9D offsets are locked and not writable.
1	GLLOCK	R/R/WONCE	0h	0:TripZone registers from 0x34 to 0x35 offsets are protected by EALLOW. 1:TripZone registers from 0x34 to 0x35 offsets are locked and not writable
0	HRLOCK	R/R/WONCE	0h	0: HRPWM registers from 0x20 to 0x2D offsets are protected by EALLOW 1:HRPWM registers from 0x20 and 0x2D offsets are locked and not writable.

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3.8.2.97 EPWM_HWVDELVAL Register

3.8.2.97.1 EPWM_HWVDELVAL Register (Offset = 1FAh) [reset = 0h]

Hardware Valley Mode Delay Register.

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Figure 3-369. EPWM_HWVDELVAL Name Register

15	14	13	12	11	10	9	8
HWVDELVAL							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HWVDELVAL							
R							
0h							

Table 3-710. EPWM_HWVDELVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	HWVDELVAL	R	0h	Hardware Valley Delay Value Register This read only register reflects the hardware delay value calculated by the equations defined in VCAPCTL[VDELAYDIV]. This reflects the latest value from the hardware calculations and can change every time valley capture sequence is triggered and VCAP1 and VCAP2 values are updated.

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3.8.2.98 EPWM_VCNTVAL Register

3.8.2.98.1 EPWM_VCNTVAL Register (Offset = 1FCh) [reset = 0h]

Hardware Valley Counter Register.

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Figure 3-370. EPWM_VCNTVAL Name Register

15	14	13	12	11	10	9	8
VCNTVAL							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VCNTVAL							
R							
0h							

Table 3-711. EPWM_VCNTVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	VCNTVAL	R	0h	Valley Time Base Counter Register This register reflects the captured VCNT value upon occurrence of STOPEDGE selected in VCNTCFG register.

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3.8.2.99 EPWM_XCMPCTL1 Register

3.8.2.99.1 EPWM_XCMPCTL1 Register (Offset = 400h) [reset = 0h]

XCMP Mode Control Register.

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Figure 3-371. EPWM_XCMPCTL1 Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2				XCMPB_ALLOC			
R				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMPA_ALLOC				RESERVED_1		XCMPSPLIT	XCMPEN
R/W				R		R/W	R/W
0h				0h		0h	0h

Table 3-712. EPWM_XCMPCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_2	R	0h	Reserved
11:8	XCMPB_ALLOC	R/W	0h	XCMPn register allocation for CMPB: - 0 --> Reserved - 1 --> Reserved - 2 --> Reserved - 3 --> Reserved - 4 --> Reserved - 5 --> XCMP5 - 6 --> XCMP5, XCMP6 - 7 --> XCMP5, XCMP6, XCMP7 - 8 --> XCMP5, XCMP6, XCMP7, XCMP8 This register settings will take effect only when XCMPEN==1 And XCMPSPLIT ==1
7:4	XCMPA_ALLOC	R/W	0h	XCMPn register allocation for CMPA: - 0 --> No XCMP - 1 --> XCMP1 - 2 --> XCMP1, XCMP2 - 3 --> XCMP1, XCMP2, XCMP3 - 4 --> XCMP1, XCMP2, XCMP3, XCMP4 - 5 --> XCMP1, XCMP2, XCMP3, XCMP4, XCMP5 - 6 --> XCMP1, XCMP2, XCMP3, XCMP4, XCMP5, XCMP6 - 7 --> XCMP1, XCMP2, XCMP3, XCMP4, XCMP5, XCMP6, XCMP7 - 8 --> XCMP1, XCMP2, XCMP3, XCMP4, XCMP5, XCMP6, XCMP7, XCMP8 This register settings will take effect only when XCMPEN==1 If XCMPSPLIT ==1, this field cannot be greater than 4. If XCMPSPLIT ==1 only lower 3 bits are used in this field.
3:2	RESERVED_1	R	0h	Reserved

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Table 3-712. EPWM_XCMPCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	XCMPSPLIT	R/W	0h	XCMP Register Allocation Options: 0 : XCMP1-8 --> CMPA 1 : XCMP1-4 -->CMPA, XCMP5-8 CMPB This register settings will take effect only when XCMPEN==1
0	XCMPEN	R/W	0h	XCMP Compare Register Operation Enable: 0 XCMP register operation Disabled [operation compatible to Type-4] 1 XCMP register operation Enabled [New CMPx registers are effective - section 1.3 details the operation]

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3.8.2.100 EPWM_XLOADCTL Register

3.8.2.100.1 EPWM_XLOADCTL Register (Offset = 410h) [reset = 0h]

XCMP Mode Load Control Register.

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Figure 3-372. EPWM_XLOADCTL Name Register

31	30	29	28	27	26	25	24
RESERVED_8	RPTBUF3CNT			RESERVED_7	RPTBUF3PRD		
R	R			R	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_6	RPTBUF2CNT			RESERVED_5	RPTBUF2PRD		
R	R			R	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_4				SHDWBUFPTR_LOADMULTIPLE		SHDWBUFPTR_LOADONCE	
R				R		R/W	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_3		SHDWLEVEL		RESERVED_2	LOADMODE	RESERVED_1	
R		R/W		R	R/W	R	
0h		0h		0h	0h	0h	

Table 3-713. EPWM_XLOADCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_8	R	0h	Reserved
30:28	RPTBUF3CNT	R	0h	Repeat Count Status Shadow Buffer 3:These bits indicate how many times shadow buffer 3 has been be applied before moving to the next buffer I,e, shadow buffer 1. 3'b000 Shadow buffer reset value with STARTLD and copied to Active register 3'b001 Shadow buffer applied twice on 2 successive load strobes 3'b010 Shadow buffer applied thrice on 3 successive load strobes . . 3'b111 Shadow buffer applied 8 times on 8 successive load strobes These bits reset to zero every time STARTLD is initiated.
27	RESERVED_7	R	0h	Reserved
26:24	RPTBUF3PRD	R/W	0h	Repeat Count Shadow Buffer 3 : These bits indicate how many times shadow buffer 3 will be applied before moving to the next buffer I,e, shadow buffer 1. 3'b000 Apply shadow buffer once and move to the next shadow buffer on the following load pulse 3'b001 Apply shadow buffer twice on 2 successive load strobes and move to the next shadow buffer on the following load pulse 3'b010 Apply shadow buffer thrice on 3 successive load strobes and move to the next shadow buffer on the following load pulse . . 3'b111 Apply shadow buffer 8 times on 8 successive load strobes and move to the next shadow buffer on the following load pulse
23	RESERVED_6	R	0h	Reserved

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Table 3-713. EPWM_XLOADCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22:20	RPTBUF2CNT	R	0h	Repeat Count Status Shadow Buffer 2:These bits indicate how many times shadow buffer 2 has been be applied before moving to the next buffer I,e, shadow buffer 1. 3'b000 Shadow buffer reset value with STARTLD and copied to Active register 3'b001 Shadow buffer applied twice on 2 successive load strobes 3'b010 Shadow buffer applied thrice on 3 successive load strobes . . 3'b111 Shadow buffer applied 8 times on 8 successive load strobes These bits reset to zero every time STARTLD is initiated.
19	RESERVED_5	R	0h	Reserved
18:16	RPTBUF2PRD	R/W	0h	Repeat Count Shadow Buffer 2 : These bits indicate how many times shadow buffer 2 will be applied before moving to the next buffer I,e, shadow buffer 1. 3'b000 Apply shadow buffer once and move to the next shadow buffer on the following load pulse 3'b001 Apply shadow buffer twice on 2 successive load strobes and move to the next shadow buffer on the following load pulse 3'b010 Apply shadow buffer thrice on 3 successive load strobes and move to the next shadow buffer on the following load pulse . . 2'b12'b11 Apply shadow buffer 8 times on 8 successive load strobes and move to the next shadow buffer on the following load pulse
15:12	RESERVED_4	R	0h	Reserved
11:10	SHDWBUFPTR_LOADMULTIPLE	R	0h	Register Load event count: These bits indicate the current shadow buffer in use. 2'b00 Reset value 0,1 1 Shadow buffer 1 in use 2'b10 2 Shadow buffer 2 in use 2'b11 3 Shadow buffer 3 in use
9:8	SHDWBUFPTR_LOADONCE	R/W	0h	Register Load event count: These bits indicate the current shadow buffer in use. 2'b00 Reset value 0,1 1 Shadow buffer 1 in use 2'b10 2 Shadow buffer 2 in use 2'b11 3 Shadow buffer 3 in use
7:6	RESERVED_3	R	0h	Reserved
5:4	SHDWLEVEL	R/W	0h	Shadow Register Level Allocation Options: These bits are effective only when XCMPEN is enabled. 2'b00 : XXXX Shadow level is set at zero. XXXX Active register is available 2'b01 : XXXX Shadow level is set at 1. XXXX_SHDW1 and Active registers are available 2'b10 : XXXX Shadow level is set at 1. XXXX_SHDW1, XXXX_SHDW2 and Active registers are available 2'b11 : XXXX Shadow level is set at 1. XXXX_SHDW1, XXXX_SHDW2, XXXX_SHDW3 and Active registers are available
3	RESERVED_2	R	0h	Reserved
2	LOADMODE	R/W	0h	Load mode selection for Shadow registers: These bits are effective only when XCMPEN is enabled. 0 : [LOADONCE] Load occurs at every load strobe [CNT_Zero or FRCLD] from SHDWn Active registers. And STARTLD is cleared after 1 load strobe. SHDWBUFPTR is not automatically decremented in this case. User would set the SHDWBUFPTR for subsequent loads. 1 : [LOADMULTIPLE] Load occurs at every load strobe [CNT_Zero or FRCLD] from SHDWnActive registers. And STARTLD is cleared after SHDWLEVEL number of load strobes. SHDWBUFPTR decrements by 1 on a load strobe, until the SHDWBUFPTR reaches 1.

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Table 3-713. EPWM_XLOADCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RESERVED_1	R	0h	Reserved

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3.8.2.101 EPWM_XLOAD Register

3.8.2.101.1 EPWM_XLOAD Register (Offset = 418h) [reset = 0h]

XCMP Mode Load Enable Register.

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Figure 3-373. EPWM_XLOAD Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						FRCLD	STARTLD
R						R/W1TS	R/W1TS
0h						0h	0h

Table 3-714. EPWM_XLOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_1	R	0h	Reserved
1	FRCLD	R/W1TS	0h	Force reload event in one shot mode : Writing a 1 to this bit turn force one load event at the input of the event pre-scale counter as shown in the diagram below. This bit is intended to be used for testing and/or software force loading of the events in global load mode. Writing of 0 will be ignored. Always reads back a 0.
0	STARTLD	R/W1TS	0h	Enable reload event : Writing a 1 to this bit turn the one shot latch condition ON. Upon occurrence of a chosen load strobe, one shadow to active reload occurs and the latch will be cleared. Hence Writing "1" to this bit would allow load strobe event to pass through and block further strobe events. Writing of 0 will be ignored. Always reads back a 0.

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3.8.2.102 EPWM_EPWMXLINKXLOAD Register

3.8.2.102.1 EPWM_EPWMXLINKXLOAD Register (Offset = 41Ch) [reset = 0h]

Link register across PWM modules.

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Figure 3-374. EPWM_EPWMXLINKXLOAD Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			XLOADLINK				
R			R/W				
0h			0h				

Table 3-715. EPWM_EPWMXLINKXLOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED_1	R	0h	Reserved
4:0	XLOADLINK	R/W	0h	XLOAD Link Bits: Writes to the XLOAD registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's XLOAD registers 5'b00000: EPWM0 5'b00001: EPWM1 5'b00010: EPWM2 5'b00011: EPWM3 5'b00100: EPWM4 5'b00101: EPWM5 5'b00110: EPWM6 5'b00111: EPWM7 5'b01000: EPWM8 5'b01001: EPWM9 5'b01010: EPWM10 5'b01011: EPWM11 5'b01100: EPWM12 ... 5'b11111: EPWM31

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3.8.2.103 EPWM_XREGSHDW1STS Register

3.8.2.103.1 EPWM_XREGSHDW1STS Register (Offset = 420h) [reset = 0h]

Shadow Buffer 1 Update Status Register.

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Figure 3-375. EPWM_XREGSHDW1STS Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1	XMIN_SHDW1FULL	XMAX_SHDW1FULL	XAQCTLB_SHDW1FULL	XAQCTLA_SHDW1FULL	CMPD_SHDW1FULL	CMPC_SHDW1FULL	XTBPRD_SHDW1FULL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMP8_SHDW1FULL	XCMP7_SHDW1FULL	XCMP6_SHDW1FULL	XCMP5_SHDW1FULL	XCMP4_SHDW1FULL	XCMP3_SHDW1FULL	XCMP2_SHDW1FULL	XCMP1_SHDW1FULL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-716. EPWM_XREGSHDW1STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED_1	R	0h	Reserved
14	XMIN_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
13	XMAX_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
12	XAQCTLB_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
11	XAQCTLA_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
10	CMPD_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
9	CMPC_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
8	XTBPRD_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
7	XCMP8_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value

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Table 3-716. EPWM_XREGSHDW1STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	XCMP7_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
5	XCMP6_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
4	XCMP5_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
3	XCMP4_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
2	XCMP3_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
1	XCMP2_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
0	XCMP1_SHDW1FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value

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3.8.2.104 EPWM_XREGSHDW2STS Register

3.8.2.104.1 EPWM_XREGSHDW2STS Register (Offset = 428h) [reset = 0h]

Shadow Buffer 2 Update Status Register.

Return to Summary Table

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Figure 3-376. EPWM_XREGSHDW2STS Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1	XMIN_SHDW2FULL	XMAX_SHDW2FULL	XAQCTLB_SHDW2FULL	XAQCTLA_SHDW2FULL	CMPD_SHDW2FULL	CMPC_SHDW2FULL	XTBPRD_SHDW2FULL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
XCMP8_SHDW2FULL	XCMP7_SHDW2FULL	XCMP6_SHDW2FULL	XCMP5_SHDW2FULL	XCMP4_SHDW2FULL	XCMP3_SHDW2FULL	XCMP2_SHDW2FULL	XCMP1_SHDW2FULL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-717. EPWM_XREGSHDW2STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED_1	R	0h	Reserved
14	XMIN_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
13	XMAX_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
12	XAQCTLB_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
11	XAQCTLA_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
10	CMPD_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
9	CMPC_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
8	XTBPRD_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
7	XCMP8_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value

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Table 3-717. EPWM_XREGSHDW2STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	XCMP7_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
5	XCMP6_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
4	XCMP5_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
3	XCMP4_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
2	XCMP3_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
1	XCMP2_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
0	XCMP1_SHDW2FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value

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3.8.2.105 EPWM_XREGSHDW3STS Register

3.8.2.105.1 EPWM_XREGSHDW3STS Register (Offset = 430h) [reset = 0h]

Shadow Buffer 3 Update Status Register.

Return to Summary Table

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Figure 3-377. EPWM_XREGSHDW3STS Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1	XMIN_SHDW3FULL	XMAX_SHDW3FULL	XAQCTLB_SHDW3FULL	XAQCTLA_SHDW3FULL	CMPD_SHDW3FULL	CMPC_SHDW3FULL	XTBPRD_SHDW3FULL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
XCMP8_SHDW3FULL	XCMP7_SHDW3FULL	XCMP6_SHDW3FULL	XCMP5_SHDW3FULL	XCMP4_SHDW3FULL	XCMP3_SHDW3FULL	XCMP2_SHDW3FULL	XCMP1_SHDW3FULL
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-718. EPWM_XREGSHDW3STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	RESERVED_1	R	0h	Reserved
14	XMIN_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
13	XMAX_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
12	XAQCTLB_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
11	XAQCTLA_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
10	CMPD_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
9	CMPC_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
8	XTBPRD_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
7	XCMP8_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value

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Table 3-718. EPWM_XREGSHDW3STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	XCMP7_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
5	XCMP6_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
4	XCMP5_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
3	XCMP4_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
2	XCMP3_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
1	XCMP2_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value
0	XCMP1_SHDW3FULL	R	0h	0 Shadow Register is not full yet 1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value

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3.8.2.106 EPWM_XCMP1_ACTIVE Register

3.8.2.106.1 EPWM_XCMP1_ACTIVE Register (Offset = 600h) [reset = 0h]

Additional Compare 1 Active Register.

Return to Summary Table

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Figure 3-378. EPWM_XCMP1_ACTIVE Name Register

31	30	29	28	27	26	25	24
XCMP1_ACTIVE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XCMP1_ACTIVE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XCMP1HR_ACTIVE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMP1HR_ACTIVE							
R/W							
0h							

Table 3-719. EPWM_XCMP1_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP1_ACTIVE	R/W	0h	XCMP1_ACTIVE Register The value in the XCMP1_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.
15:0	XCMP1HR_ACTIVE	R/W	0h	XCMP1HR_ACTIVE Register The value in the XCMP1HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs.

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3.8.2.107 EPWM_XCMP2_ACTIVE Register

3.8.2.107.1 EPWM_XCMP2_ACTIVE Register (Offset = 604h) [reset = 0h]

Additional Compare 2 Active Register.

Return to Summary Table

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Figure 3-379. EPWM_XCMP2_ACTIVE Name Register

31	30	29	28	27	26	25	24
XCMP2_ACTIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP2_ACTIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP2HR_ACTIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP2HR_ACTIVE							
R/W							
0h							

Table 3-720. EPWM_XCMP2_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP2_ACTIVE	R/W	0h	XCMP2_ACTIVE Register The value in the XCMP2_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.
15:0	XCMP2HR_ACTIVE	R/W	0h	XCMP2HR_ACTIVE Register The value in the XCMP2HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs.

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3.8.2.108 EPWM_XCMP3_ACTIVE Register

3.8.2.108.1 EPWM_XCMP3_ACTIVE Register (Offset = 608h) [reset = 0h]

Additional Compare 3 Active Register.

Return to Summary Table

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Figure 3-380. EPWM_XCMP3_ACTIVE Name Register

31	30	29	28	27	26	25	24
XCMP3_ACTIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP3_ACTIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP3HR_ACTIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP3HR_ACTIVE							
R/W							
0h							

Table 3-721. EPWM_XCMP3_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP3_ACTIVE	R/W	0h	XCMP3_ACTIVE Register The value in the XCMP3_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.
15:0	XCMP3HR_ACTIVE	R/W	0h	XCMP3HR_ACTIVE Register The value in the XCMP3HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs.

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3.8.2.109 EPWM_XCMP4_ACTIVE Register

3.8.2.109.1 EPWM_XCMP4_ACTIVE Register (Offset = 60Ch) [reset = 0h]

Additional Compare 4 Active Register.

Return to Summary Table

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Figure 3-381. EPWM_XCMP4_ACTIVE Name Register

31	30	29	28	27	26	25	24
XCMP4_ACTIVE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XCMP4_ACTIVE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XCMP4HR_ACTIVE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMP4HR_ACTIVE							
R/W							
0h							

Table 3-722. EPWM_XCMP4_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP4_ACTIVE	R/W	0h	XCMP4_ACTIVE Register The value in the XCMP4_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.
15:0	XCMP4HR_ACTIVE	R/W	0h	XCMP4HR_ACTIVE Register The value in the XCMP4HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs.

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3.8.2.110 EPWM_XCMP5_ACTIVE Register

3.8.2.110.1 EPWM_XCMP5_ACTIVE Register (Offset = 610h) [reset = 0h]

Additional Compare 5 Active Register.

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Figure 3-382. EPWM_XCMP5_ACTIVE Name Register

31	30	29	28	27	26	25	24
XCMP5_ACTIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP5_ACTIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP5HR_ACTIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP5HR_ACTIVE							
R/W							
0h							

Table 3-723. EPWM_XCMP5_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP5_ACTIVE	R/W	0h	XCMP5_ACTIVE Register The value in the XCMP5_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.
15:0	XCMP5HR_ACTIVE	R/W	0h	XCMP5HR_ACTIVE Register The value in the XCMP5HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs.

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3.8.2.111 EPWM_XCMP6_ACTIVE Register

3.8.2.111.1 EPWM_XCMP6_ACTIVE Register (Offset = 614h) [reset = 0h]

Additional Compare 6 Active Register.

Return to Summary Table

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Figure 3-383. EPWM_XCMP6_ACTIVE Name Register

31	30	29	28	27	26	25	24
XCMP6_ACTIVE							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XCMP6_ACTIVE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XCMP6HR_ACTIVE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMP6HR_ACTIVE							
R/W							
0h							

Table 3-724. EPWM_XCMP6_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP6_ACTIVE	R/W	0h	XCMP6_ACTIVE Register The value in the XCMP6_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.
15:0	XCMP6HR_ACTIVE	R/W	0h	XCMP6HR_ACTIVE Register The value in the XCMP6HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs.

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3.8.2.112 EPWM_XCMP7_ACTIVE Register

3.8.2.112.1 EPWM_XCMP7_ACTIVE Register (Offset = 618h) [reset = 0h]

Additional Compare 7 Active Register.

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Figure 3-384. EPWM_XCMP7_ACTIVE Name Register

31	30	29	28	27	26	25	24
XCMP7_ACTIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP7_ACTIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP7HR_ACTIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP7HR_ACTIVE							
R/W							
0h							

Table 3-725. EPWM_XCMP7_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP7_ACTIVE	R/W	0h	XCMP7_ACTIVE Register The value in the XCMP7_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.
15:0	XCMP7HR_ACTIVE	R/W	0h	XCMP7HR_ACTIVE Register The value in the XCMP7HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs.

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3.8.2.113 EPWM_XCMP8_ACTIVE Register

3.8.2.113.1 EPWM_XCMP8_ACTIVE Register (Offset = 61Ch) [reset = 0h]

Additional Compare 8 Active Register.

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Figure 3-385. EPWM_XCMP8_ACTIVE Name Register

31	30	29	28	27	26	25	24
XCMP8_ACTIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP8_ACTIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP8HR_ACTIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP8HR_ACTIVE							
R/W							
0h							

Table 3-726. EPWM_XCMP8_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP8_ACTIVE	R/W	0h	XCMP8_ACTIVE Register The value in the XCMP8_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.
15:0	XCMP8HR_ACTIVE	R/W	0h	XCMP8HR_ACTIVE Register The value in the XCMP8HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs.

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3.8.2.114 EPWM_XTBPRD_ACTIVE Register

3.8.2.114.1 EPWM_XTBPRD_ACTIVE Register (Offset = 620h) [reset = 0h]

Additional Time Base Period Active Register.

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Figure 3-386. EPWM_XTBPRD_ACTIVE Name Register

31	30	29	28	27	26	25	24
XTBPRD_ACTIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
XTBPRD_ACTIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
XTBPRDHR_ACTIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
XTBPRDHR_ACTIVE							
R/W							
0h							

Table 3-727. EPWM_XTBPRD_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XTBPRD_ACTIVE	R/W	0h	The value in the XTBPRD_ACTIVE register is loaded into TBPRD [shadow/active] registers when shadow to active load occurs.
15:0	XTBPRDHR_ACTIVE	R/W	0h	The value in the XTBPRDHR_ACTIVE register is loaded into TBPRDHR [shadow/active] registers when shadow to active load occurs.

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3.8.2.115 EPWM_XAQCTLA_ACTIVE Register

3.8.2.115.1 EPWM_XAQCTLA_ACTIVE Register (Offset = 630h) [reset = 0h]

AQCTLA Active Register.

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Figure 3-387. EPWM_XAQCTLA_ACTIVE Name Register

15	14	13	12	11	10	9	8
XCMP8		XCMP7		XCMP6		XCMP5	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
XCMP4		XCMP3		XCMP2		XCMP1	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-728. EPWM_XAQCTLA_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	XCMP8	R/W	0h	Action when Counter = CMP8 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
13:12	XCMP7	R/W	0h	Action when Counter = CMP7 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
11:10	XCMP6	R/W	0h	Action when Counter = CMP6 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
9:8	XCMP5	R/W	0h	Action when Counter = CMP5 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
7:6	XCMP4	R/W	0h	Action when Counter = CMP4 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
5:4	XCMP3	R/W	0h	Action when Counter = CMP3 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
3:2	XCMP2	R/W	0h	Action when Counter = CMP2 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]

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Table 3-728. EPWM_XAQCTLA_ACTIVE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	XCMP1	R/W	0h	Action when Counter = CMP1 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]

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3.8.2.116 EPWM_XMINMAX_ACTIVE Register

3.8.2.116.1 EPWM_XMINMAX_ACTIVE Register (Offset = 644h) [reset = 0h]

XMINMAX Active Register.

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Figure 3-388. EPWM_XMINMAX_ACTIVE Name Register

31	30	29	28	27	26	25	24
XMIN_ACTIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
XMIN_ACTIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
XMAX_ACTIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
XMAX_ACTIVE							
R/W							
0h							

Table 3-729. EPWM_XMINMAX_ACTIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XMIN_ACTIVE	R/W	0h	The value in the XMIN_ACTIVE register is used for comparision against the threshold of the capture counter at any given time.
15:0	XMAX_ACTIVE	R/W	0h	The value in the XMAX_ACTIVE register is used for comparision against the threshold of the capture counter at any given time.

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3.8.2.117 EPWM_XCMP1_SHDW1 Register

3.8.2.117.1 EPWM_XCMP1_SHDW1 Register (Offset = 680h) [reset = 0h]

Additional Compare 1 Shadow 1 Register.

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Figure 3-389. EPWM_XCMP1_SHDW1 Name Register

31	30	29	28	27	26	25	24
XCMP1_SHDW1							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP1_SHDW1							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP1HR_SHDW1							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP1HR_SHDW1							
R/W							
0h							

Table 3-730. EPWM_XCMP1_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP1_SHDW1	R/W	0h	XCMP1_SHDW1 Register The value in the XCMP1_SHDW1 register is loaded into XCMP1_ACTIVE register when shadow to active load occurs.
15:0	XCMP1HR_SHDW1	R/W	0h	XCMP1HR_SHDW1 Register The value in the XCMP1HR_SHDW1 register is loaded into XCMP1HR_ACTIVE register when shadow to active load occurs.

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3.8.2.118 EPWM_XCMP2_SHDW1 Register

3.8.2.118.1 EPWM_XCMP2_SHDW1 Register (Offset = 684h) [reset = 0h]

Additional Compare 2 Shadow 1 Register.

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Figure 3-390. EPWM_XCMP2_SHDW1 Name Register

31	30	29	28	27	26	25	24
XCMP2_SHDW1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XCMP2_SHDW1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XCMP2HR_SHDW1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMP2HR_SHDW1							
R/W							
0h							

Table 3-731. EPWM_XCMP2_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP2_SHDW1	R/W	0h	XCMP2_SHDW1 Register The value in the XCMP2_SHDW1 register is loaded into XCMP2_ACTIVE register when shadow to active load occurs.
15:0	XCMP2HR_SHDW1	R/W	0h	XCMP2HR_SHDW1 Register The value in the XCMP2HR_SHDW1 register is loaded into XCMP2HR_ACTIVE register when shadow to active load occurs.

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3.8.2.119 EPWM_XCMP3_SHDW1 Register

3.8.2.119.1 EPWM_XCMP3_SHDW1 Register (Offset = 688h) [reset = 0h]

Additional Compare 3 Shadow 1 Register.

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Figure 3-391. EPWM_XCMP3_SHDW1 Name Register

31	30	29	28	27	26	25	24
XCMP3_SHDW1							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP3_SHDW1							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP3HR_SHDW1							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP3HR_SHDW1							
R/W							
0h							

Table 3-732. EPWM_XCMP3_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP3_SHDW1	R/W	0h	XCMP3_SHDW1 Register The value in the XCMP3_SHDW1 register is loaded into XCMP3_ACTIVE register when shadow to active load occurs.
15:0	XCMP3HR_SHDW1	R/W	0h	XCMP3HR_SHDW1 Register The value in the XCMP3HR_SHDW1 register is loaded into XCMP3HR_ACTIVE register when shadow to active load occurs.

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3.8.2.120 EPWM_XCMP4_SHDW1 Register

3.8.2.120.1 EPWM_XCMP4_SHDW1 Register (Offset = 68Ch) [reset = 0h]

Additional Compare 4 Shadow 1 Register.

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Figure 3-392. EPWM_XCMP4_SHDW1 Name Register

31	30	29	28	27	26	25	24
XCMP4_SHDW1							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP4_SHDW1							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP4HR_SHDW1							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP4HR_SHDW1							
R/W							
0h							

Table 3-733. EPWM_XCMP4_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP4_SHDW1	R/W	0h	XCMP4_SHDW1 Register The value in the XCMP4_SHDW1 register is loaded into XCMP4_ACTIVE register when shadow to active load occurs.
15:0	XCMP4HR_SHDW1	R/W	0h	XCMP4HR_SHDW1 Register The value in the XCMP4HR_SHDW1 register is loaded into XCMP4HR_ACTIVE register when shadow to active load occurs.

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3.8.2.121 EPWM_XCMP5_SHDW1 Register

3.8.2.121.1 EPWM_XCMP5_SHDW1 Register (Offset = 690h) [reset = 0h]

Additional Compare 5 Shadow 1 Register.

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Figure 3-393. EPWM_XCMP5_SHDW1 Name Register

31	30	29	28	27	26	25	24
XCMP5_SHDW1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XCMP5_SHDW1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XCMP5HR_SHDW1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMP5HR_SHDW1							
R/W							
0h							

Table 3-734. EPWM_XCMP5_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP5_SHDW1	R/W	0h	XCMP5_SHDW1 Register The value in the XCMP5_SHDW1 register is loaded into XCMP5_ACTIVE register when shadow to active load occurs.
15:0	XCMP5HR_SHDW1	R/W	0h	XCMP5HR_SHDW1 Register The value in the XCMP5HR_SHDW1 register is loaded into XCMP5HR_ACTIVE register when shadow to active load occurs.

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3.8.2.122 EPWM_XCMP6_SHDW1 Register

3.8.2.122.1 EPWM_XCMP6_SHDW1 Register (Offset = 694h) [reset = 0h]

Additional Compare 6 Shadow 1 Register.

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Figure 3-394. EPWM_XCMP6_SHDW1 Name Register

31	30	29	28	27	26	25	24
XCMP6_SHDW1							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP6_SHDW1							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP6HR_SHDW1							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP6HR_SHDW1							
R/W							
0h							

Table 3-735. EPWM_XCMP6_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP6_SHDW1	R/W	0h	XCMP6_SHDW1 Register The value in the XCMP6_SHDW1 register is loaded into XCMP6_ACTIVE register when shadow to active load occurs.
15:0	XCMP6HR_SHDW1	R/W	0h	XCMP6HR_SHDW1 Register The value in the XCMP6HR_SHDW1 register is loaded into XCMP6HR_ACTIVE register when shadow to active load occurs.

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3.8.2.123 EPWM_XCMP7_SHDW1 Register

3.8.2.123.1 EPWM_XCMP7_SHDW1 Register (Offset = 698h) [reset = 0h]

Additional Compare 7 Shadow 1 Register.

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Figure 3-395. EPWM_XCMP7_SHDW1 Name Register

31	30	29	28	27	26	25	24
XCMP7_SHDW1							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP7_SHDW1							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP7HR_SHDW1							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP7HR_SHDW1							
R/W							
0h							

Table 3-736. EPWM_XCMP7_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP7_SHDW1	R/W	0h	XCMP7_SHDW1 Register The value in the XCMP7_SHDW1 register is loaded into XCMP7_ACTIVE register when shadow to active load occurs.
15:0	XCMP7HR_SHDW1	R/W	0h	XCMP7HR_SHDW1 Register The value in the XCMP7HR_SHDW1 register is loaded into XCMP7HR_ACTIVE register when shadow to active load occurs.

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3.8.2.124 EPWM_XCMP8_SHDW1 Register

3.8.2.124.1 EPWM_XCMP8_SHDW1 Register (Offset = 69Ch) [reset = 0h]

Additional Compare 8 Shadow 1 Register.

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Figure 3-396. EPWM_XCMP8_SHDW1 Name Register

31	30	29	28	27	26	25	24
XCMP8_SHDW1							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP8_SHDW1							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP8HR_SHDW1							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP8HR_SHDW1							
R/W							
0h							

Table 3-737. EPWM_XCMP8_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP8_SHDW1	R/W	0h	XCMP8_SHDW1 Register The value in the XCMP8_SHDW1 register is loaded into XCMP8_ACTIVE register when shadow to active load occurs.
15:0	XCMP8HR_SHDW1	R/W	0h	XCMP8HR_SHDW1 Register The value in the XCMP8HR_SHDW1 register is loaded into XCMP8HR_ACTIVE register when shadow to active load occurs.

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3.8.2.125 EPWM_XTBPRD_SHDW1 Register

3.8.2.125.1 EPWM_XTBPRD_SHDW1 Register (Offset = 6A0h) [reset = 0h]

Additional Time Base Period Shadow 1 Register.

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Figure 3-397. EPWM_XTBPRD_SHDW1 Name Register

31	30	29	28	27	26	25	24
XTBPRD_SHDW1							
R/W							
0h							
23	22	21	20	19	18	17	16
XTBPRD_SHDW1							
R/W							
0h							
15	14	13	12	11	10	9	8
XTBPRDHR_SHDW1							
R/W							
0h							
7	6	5	4	3	2	1	0
XTBPRDHR_SHDW1							
R/W							
0h							

Table 3-738. EPWM_XTBPRD_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XTBPRD_SHDW1	R/W	0h	The value in the XTBPRD_SHDW1 register is loaded into XTBPRD_ACTIVE register when shadow to active load occurs.
15:0	XTBPRDHR_SHDW1	R/W	0h	The value in the XTBPRDHR_SHDW1 register is loaded into XTBPRDHR_ACTIVE register when shadow to active load occurs.

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3.8.2.126 EPWM_XAQCTLA_SHDW1 Register

3.8.2.126.1 EPWM_XAQCTLA_SHDW1 Register (Offset = 6B0h) [reset = 0h]

XAQCTLA Shadow 1 Register.

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Figure 3-398. EPWM_XAQCTLA_SHDW1 Name Register

15	14	13	12	11	10	9	8
XCMP8		XCMP7		XCMP6		XCMP5	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
XCMP4		XCMP3		XCMP2		XCMP1	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-739. EPWM_XAQCTLA_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	XCMP8	R/W	0h	Action when Counter = CMP8 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
13:12	XCMP7	R/W	0h	Action when Counter = CMP7 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
11:10	XCMP6	R/W	0h	Action when Counter = CMP6 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
9:8	XCMP5	R/W	0h	Action when Counter = CMP5 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
7:6	XCMP4	R/W	0h	Action when Counter = CMP4 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
5:4	XCMP3	R/W	0h	Action when Counter = CMP3 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
3:2	XCMP2	R/W	0h	Action when Counter = CMP2 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]

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Table 3-739. EPWM_XAQCTLA_SHDW1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	XCMP1	R/W	0h	Action when Counter = CMP1 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]

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3.8.2.127 EPWM_XAQCTLB_SHDW1 Register

3.8.2.127.1 EPWM_XAQCTLB_SHDW1 Register (Offset = 6B2h) [reset = 0h]

XAQCTLB Shadow 1 Register.

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Figure 3-399. EPWM_XAQCTLB_SHDW1 Name Register

15	14	13	12	11	10	9	8
XCMP8		XCMP7		XCMP6		XCMP5	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							
R							
0h							

Table 3-740. EPWM_XAQCTLB_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	XCMP8	R/W	0h	Action when Counter = CMP8 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
13:12	XCMP7	R/W	0h	Action when Counter = CMP7 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
11:10	XCMP6	R/W	0h	Action when Counter = CMP6 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
9:8	XCMP5	R/W	0h	Action when Counter = CMP5 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
7:0	RESERVED_1	R	0h	Reserved

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3.8.2.128 EPWM_CMPC_SHDW1 Register

3.8.2.128.1 EPWM_CMPC_SHDW1 Register (Offset = 6BAh) [reset = 0h]

CMPC Shadow 1 Register.

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Figure 3-400. EPWM_CMPC_SHDW1 Name Register

15	14	13	12	11	10	9	8
CMPC_SHDW1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPC_SHDW1							
R/W							
0h							

Table 3-741. EPWM_CMPC_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPC_SHDW1	R/W	0h	The value in the CMPC_SHDW1 register is loaded into CMPC_ACTIVE register when shadow to active load occurs.

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3.8.2.129 EPWM_CMPD_SHDW1 Register

3.8.2.129.1 EPWM_CMPD_SHDW1 Register (Offset = 6BEh) [reset = 0h]

CMPD Shadow 1 Register.

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Figure 3-401. EPWM_CMPD_SHDW1 Name Register

15	14	13	12	11	10	9	8
CMPD_SHDW1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMPD_SHDW1							
R/W							
0h							

Table 3-742. EPWM_CMPD_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPD_SHDW1	R/W	0h	The value in the CMPD_SHDW1 register is loaded into CMPD_ACTIVE register when shadow to active load occurs.

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3.8.2.130 EPWM_XMINMAX_SHDW1 Register

3.8.2.130.1 EPWM_XMINMAX_SHDW1 Register (Offset = 6C4h) [reset = 0h]

XMINMAX Shadow 1 Register.

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Figure 3-402. EPWM_XMINMAX_SHDW1 Name Register

31	30	29	28	27	26	25	24
XMIN_SHDW1							
R/W							
0h							
23	22	21	20	19	18	17	16
XMIN_SHDW1							
R/W							
0h							
15	14	13	12	11	10	9	8
XMAX_SHDW1							
R/W							
0h							
7	6	5	4	3	2	1	0
XMAX_SHDW1							
R/W							
0h							

Table 3-743. EPWM_XMINMAX_SHDW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XMIN_SHDW1	R/W	0h	The value in the XMIN_SHDW1 register is loaded into XMIN_ACTIVE register when shadow to active load occurs.
15:0	XMAX_SHDW1	R/W	0h	The value in the XMAX_SHDW1 register is loaded into XMAX_ACTIVE register when shadow to active load occurs.

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3.8.2.131 EPWM_XCMP1_SHDW2 Register

3.8.2.131.1 EPWM_XCMP1_SHDW2 Register (Offset = 700h) [reset = 0h]

Additional Compare 1 Shadow 2 Register.

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Figure 3-403. EPWM_XCMP1_SHDW2 Name Register

31	30	29	28	27	26	25	24
XCMP1_SHDW2							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP1_SHDW2							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP1HR_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP1HR_SHDW2							
R/W							
0h							

Table 3-744. EPWM_XCMP1_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP1_SHDW2	R/W	0h	XCMP1_SHDW2 Register The value in the XCMP1_SHDW2 register is loaded into XCMP1_ACTIVE register when shadow to active load occurs.
15:0	XCMP1HR_SHDW2	R/W	0h	XCMP1HR_SHDW2 Register The value in the XCMP1HR_SHDW2 register is loaded into XCMP1HR_ACTIVE register when shadow to active load occurs.

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3.8.2.132 EPWM_XCMP2_SHDW2 Register

3.8.2.132.1 EPWM_XCMP2_SHDW2 Register (Offset = 704h) [reset = 0h]

Additional Compare 2 Shadow 2 Register.

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Figure 3-404. EPWM_XCMP2_SHDW2 Name Register

31	30	29	28	27	26	25	24
XCMP2_SHDW2							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP2_SHDW2							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP2HR_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP2HR_SHDW2							
R/W							
0h							

Table 3-745. EPWM_XCMP2_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP2_SHDW2	R/W	0h	XCMP2_SHDW2 Register The value in the XCMP2_SHDW2 register is loaded into XCMP2_ACTIVE register when shadow to active load occurs.
15:0	XCMP2HR_SHDW2	R/W	0h	XCMP2HR_SHDW2 Register The value in the XCMP2HR_SHDW2 register is loaded into XCMP2HR_ACTIVE register when shadow to active load occurs.

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3.8.2.133 EPWM_XCMP3_SHDW2 Register

3.8.2.133.1 EPWM_XCMP3_SHDW2 Register (Offset = 708h) [reset = 0h]

Additional Compare 3 Shadow 2 Register.

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Figure 3-405. EPWM_XCMP3_SHDW2 Name Register

31	30	29	28	27	26	25	24
XCMP3_SHDW2							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP3_SHDW2							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP3HR_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP3HR_SHDW2							
R/W							
0h							

Table 3-746. EPWM_XCMP3_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP3_SHDW2	R/W	0h	XCMP3_SHDW2 Register The value in the XCMP3_SHDW2 register is loaded into XCMP3_ACTIVE register when shadow to active load occurs.
15:0	XCMP3HR_SHDW2	R/W	0h	XCMP3HR_SHDW2 Register The value in the XCMP3HR_SHDW2 register is loaded into XCMP3HR_ACTIVE register when shadow to active load occurs.

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3.8.2.134 EPWM_XCMP4_SHDW2 Register

3.8.2.134.1 EPWM_XCMP4_SHDW2 Register (Offset = 70Ch) [reset = 0h]

Additional Compare 4 Shadow 2 Register.

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Figure 3-406. EPWM_XCMP4_SHDW2 Name Register

31	30	29	28	27	26	25	24
XCMP4_SHDW2							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP4_SHDW2							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP4HR_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP4HR_SHDW2							
R/W							
0h							

Table 3-747. EPWM_XCMP4_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP4_SHDW2	R/W	0h	XCMP4_SHDW2 Register The value in the XCMP4_SHDW2 register is loaded into XCMP4_ACTIVE register when shadow to active load occurs.
15:0	XCMP4HR_SHDW2	R/W	0h	XCMP4HR_SHDW2 Register The value in the XCMP4HR_SHDW2 register is loaded into XCMP4HR_ACTIVE register when shadow to active load occurs.

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3.8.2.135 EPWM_XCMP5_SHDW2 Register

3.8.2.135.1 EPWM_XCMP5_SHDW2 Register (Offset = 710h) [reset = 0h]

Additional Compare 5 Shadow 2 Register.

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Figure 3-407. EPWM_XCMP5_SHDW2 Name Register

31	30	29	28	27	26	25	24
XCMP5_SHDW2							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP5_SHDW2							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP5HR_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP5HR_SHDW2							
R/W							
0h							

Table 3-748. EPWM_XCMP5_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP5_SHDW2	R/W	0h	XCMP5_SHDW2 Register The value in the XCMP5_SHDW2 register is loaded into XCMP5_ACTIVE register when shadow to active load occurs.
15:0	XCMP5HR_SHDW2	R/W	0h	XCMP5HR_SHDW2 Register The value in the XCMP5HR_SHDW2 register is loaded into XCMP5HR_ACTIVE register when shadow to active load occurs.

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3.8.2.136 EPWM_XCMP6_SHDW2 Register

3.8.2.136.1 EPWM_XCMP6_SHDW2 Register (Offset = 714h) [reset = 0h]

Additional Compare 6 Shadow 2 Register.

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Figure 3-408. EPWM_XCMP6_SHDW2 Name Register

31	30	29	28	27	26	25	24
XCMP6_SHDW2							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP6_SHDW2							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP6HR_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP6HR_SHDW2							
R/W							
0h							

Table 3-749. EPWM_XCMP6_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP6_SHDW2	R/W	0h	XCMP6_SHDW2 Register The value in the XCMP6_SHDW2 register is loaded into XCMP6_ACTIVE register when shadow to active load occurs.
15:0	XCMP6HR_SHDW2	R/W	0h	XCMP6HR_SHDW2 Register The value in the XCMP6HR_SHDW2 register is loaded into XCMP6HR_ACTIVE register when shadow to active load occurs.

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3.8.2.137 EPWM_XCMP7_SHDW2 Register

3.8.2.137.1 EPWM_XCMP7_SHDW2 Register (Offset = 718h) [reset = 0h]

Additional Compare 7 Shadow 2 Register.

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Figure 3-409. EPWM_XCMP7_SHDW2 Name Register

31	30	29	28	27	26	25	24
XCMP7_SHDW2							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP7_SHDW2							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP7HR_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP7HR_SHDW2							
R/W							
0h							

Table 3-750. EPWM_XCMP7_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP7_SHDW2	R/W	0h	XCMP7_SHDW2 Register The value in the XCMP7_SHDW2 register is loaded into XCMP7_ACTIVE register when shadow to active load occurs.
15:0	XCMP7HR_SHDW2	R/W	0h	XCMP7HR_SHDW2 Register The value in the XCMP7HR_SHDW2 register is loaded into XCMP7HR_ACTIVE register when shadow to active load occurs.

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3.8.2.138 EPWM_XCMP8_SHDW2 Register

3.8.2.138.1 EPWM_XCMP8_SHDW2 Register (Offset = 71Ch) [reset = 0h]

Additional Compare 8 Shadow 2 Register.

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Figure 3-410. EPWM_XCMP8_SHDW2 Name Register

31	30	29	28	27	26	25	24
XCMP8_SHDW2							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP8_SHDW2							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP8HR_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP8HR_SHDW2							
R/W							
0h							

Table 3-751. EPWM_XCMP8_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP8_SHDW2	R/W	0h	XCMP8_SHDW2 Register The value in the XCMP8_SHDW2 register is loaded into XCMP8_ACTIVE register when shadow to active load occurs.
15:0	XCMP8HR_SHDW2	R/W	0h	XCMP8HR_SHDW2 Register The value in the XCMP8HR_SHDW2 register is loaded into XCMP8HR_ACTIVE register when shadow to active load occurs.

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3.8.2.139 EPWM_XTBPRD_SHDW2 Register

3.8.2.139.1 EPWM_XTBPRD_SHDW2 Register (Offset = 720h) [reset = 0h]

Additional Time Base Period Shadow 2 Register.

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Figure 3-411. EPWM_XTBPRD_SHDW2 Name Register

31	30	29	28	27	26	25	24
XTBPRD_SHDW2							
R/W							
0h							
23	22	21	20	19	18	17	16
XTBPRD_SHDW2							
R/W							
0h							
15	14	13	12	11	10	9	8
XTBPRDHR_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
XTBPRDHR_SHDW2							
R/W							
0h							

Table 3-752. EPWM_XTBPRD_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XTBPRD_SHDW2	R/W	0h	The value in the XTBPRD_SHDW2 register is loaded into XTBPRD_ACTIVE register when shadow to active load occurs.
15:0	XTBPRDHR_SHDW2	R/W	0h	The value in the XTBPRDHR_SHDW2 register is loaded into XTBPRDHR_ACTIVE register when shadow to active load occurs.

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3.8.2.140 EPWM_XAQCTLA_SHDW2 Register

3.8.2.140.1 EPWM_XAQCTLA_SHDW2 Register (Offset = 730h) [reset = 0h]

XAQCTLA Shadow 2 Register.

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Figure 3-412. EPWM_XAQCTLA_SHDW2 Name Register

15	14	13	12	11	10	9	8
XCMP8		XCMP7		XCMP6		XCMP5	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMP4		XCMP3		XCMP2		XCMP1	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-753. EPWM_XAQCTLA_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	XCMP8	R/W	0h	Action when Counter = CMP8 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
13:12	XCMP7	R/W	0h	Action when Counter = CMP7 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
11:10	XCMP6	R/W	0h	Action when Counter = CMP6 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
9:8	XCMP5	R/W	0h	Action when Counter = CMP5 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
7:6	XCMP4	R/W	0h	Action when Counter = CMP4 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
5:4	XCMP3	R/W	0h	Action when Counter = CMP3 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
3:2	XCMP2	R/W	0h	Action when Counter = CMP2 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]

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Table 3-753. EPWM_XAQCTLA_SHDW2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	XCMP1	R/W	0h	Action when Counter = CMP1 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]

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3.8.2.141 EPWM_XAQCTLB_SHDW2 Register

3.8.2.141.1 EPWM_XAQCTLB_SHDW2 Register (Offset = 732h) [reset = 0h]

XAQCTLB Shadow 2 Register.

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Figure 3-413. EPWM_XAQCTLB_SHDW2 Name Register

15	14	13	12	11	10	9	8
XCMP8		XCMP7		XCMP6		XCMP5	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							
R							
0h							

Table 3-754. EPWM_XAQCTLB_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	XCMP8	R/W	0h	Action when Counter = CMP8 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
13:12	XCMP7	R/W	0h	Action when Counter = CMP7 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
11:10	XCMP6	R/W	0h	Action when Counter = CMP6 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
9:8	XCMP5	R/W	0h	Action when Counter = CMP5 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
7:0	RESERVED_1	R	0h	Reserved

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3.8.2.142 EPWM_CMPC_SHDW2 Register

3.8.2.142.1 EPWM_CMPC_SHDW2 Register (Offset = 73Ah) [reset = 0h]

CMPC Shadow 2 Register.

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Figure 3-414. EPWM_CMPC_SHDW2 Name Register

15	14	13	12	11	10	9	8
CMPC_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
CMPC_SHDW2							
R/W							
0h							

Table 3-755. EPWM_CMPC_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPC_SHDW2	R/W	0h	The value in the CMPC_SHDW2 register is loaded into CMPC_ACTIVE register when shadow to active load occurs.

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3.8.2.143 EPWM_CMPD_SHDW2 Register

3.8.2.143.1 EPWM_CMPD_SHDW2 Register (Offset = 73Eh) [reset = 0h]

CMPD Shadow 2 Register.

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Figure 3-415. EPWM_CMPD_SHDW2 Name Register

15	14	13	12	11	10	9	8
CMPD_SHDW2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPD_SHDW2							
R/W							
0h							

Table 3-756. EPWM_CMPD_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPD_SHDW2	R/W	0h	The value in the CMPD_SHDW2 register is loaded into CMPD_ACTIVE register when shadow to active load occurs.

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3.8.2.144 EPWM_XMINMAX_SHDW2 Register

3.8.2.144.1 EPWM_XMINMAX_SHDW2 Register (Offset = 744h) [reset = 0h]

XMINMAX Shadow 2 Register.

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Figure 3-416. EPWM_XMINMAX_SHDW2 Name Register

31	30	29	28	27	26	25	24
XMIN_SHDW2							
R/W							
0h							
23	22	21	20	19	18	17	16
XMIN_SHDW2							
R/W							
0h							
15	14	13	12	11	10	9	8
XMAX_SHDW2							
R/W							
0h							
7	6	5	4	3	2	1	0
XMAX_SHDW2							
R/W							
0h							

Table 3-757. EPWM_XMINMAX_SHDW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XMIN_SHDW2	R/W	0h	The value in the XMIN_SHDW2 register is loaded into XMIN_ACTIVE register when shadow to active load occurs.
15:0	XMAX_SHDW2	R/W	0h	The value in the XMAX_SHDW2 register is loaded into XMAX_ACTIVE register when shadow to active load occurs.

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3.8.2.145 EPWM_XCMP1_SHDW3 Register

3.8.2.145.1 EPWM_XCMP1_SHDW3 Register (Offset = 780h) [reset = 0h]

Additional Compare 1 Shadow 3 Register.

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Figure 3-417. EPWM_XCMP1_SHDW3 Name Register

31	30	29	28	27	26	25	24
XCMP1_SHDW3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XCMP1_SHDW3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XCMP1HR_SHDW3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMP1HR_SHDW3							
R/W							
0h							

Table 3-758. EPWM_XCMP1_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP1_SHDW3	R/W	0h	XCMP1_SHDW3 Register The value in the XCMP1_SHDW3 register is loaded into XCMP1_ACTIVE register when shadow to active load occurs.
15:0	XCMP1HR_SHDW3	R/W	0h	XCMP1HR_SHDW3 Register The value in the XCMP1HR_SHDW3 register is loaded into XCMP1HR_ACTIVE register when shadow to active load occurs.

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3.8.2.146 EPWM_XCMP2_SHDW3 Register

3.8.2.146.1 EPWM_XCMP2_SHDW3 Register (Offset = 784h) [reset = 0h]

Additional Compare 2 Shadow 3 Register.

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Figure 3-418. EPWM_XCMP2_SHDW3 Name Register

31	30	29	28	27	26	25	24
XCMP2_SHDW3							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP2_SHDW3							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP2HR_SHDW3							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP2HR_SHDW3							
R/W							
0h							

Table 3-759. EPWM_XCMP2_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP2_SHDW3	R/W	0h	XCMP2_SHDW3 Register The value in the XCMP2_SHDW3 register is loaded into XCMP2_ACTIVE register when shadow to active load occurs.
15:0	XCMP2HR_SHDW3	R/W	0h	XCMP2HR_SHDW3 Register The value in the XCMP2HR_SHDW3 register is loaded into XCMP2HR_ACTIVE register when shadow to active load occurs.

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3.8.2.147 EPWM_XCMP3_SHDW3 Register

3.8.2.147.1 EPWM_XCMP3_SHDW3 Register (Offset = 788h) [reset = 0h]

Additional Compare 3 Shadow 3 Register.

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Figure 3-419. EPWM_XCMP3_SHDW3 Name Register

31	30	29	28	27	26	25	24
XCMP3_SHDW3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XCMP3_SHDW3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XCMP3HR_SHDW3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMP3HR_SHDW3							
R/W							
0h							

Table 3-760. EPWM_XCMP3_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP3_SHDW3	R/W	0h	XCMP3_SHDW3 Register The value in the XCMP3_SHDW3 register is loaded into XCMP3_ACTIVE register when shadow to active load occurs.
15:0	XCMP3HR_SHDW3	R/W	0h	XCMP3HR_SHDW3 Register The value in the XCMP3HR_SHDW3 register is loaded into XCMP3HR_ACTIVE register when shadow to active load occurs.

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3.8.2.148 EPWM_XCMP4_SHDW3 Register

3.8.2.148.1 EPWM_XCMP4_SHDW3 Register (Offset = 78Ch) [reset = 0h]

Additional Compare 4 Shadow 3 Register.

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Figure 3-420. EPWM_XCMP4_SHDW3 Name Register

31	30	29	28	27	26	25	24
XCMP4_SHDW3							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP4_SHDW3							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP4HR_SHDW3							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP4HR_SHDW3							
R/W							
0h							

Table 3-761. EPWM_XCMP4_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP4_SHDW3	R/W	0h	XCMP4_SHDW3 Register The value in the XCMP4_SHDW3 register is loaded into XCMP4_ACTIVE register when shadow to active load occurs.
15:0	XCMP4HR_SHDW3	R/W	0h	XCMP4HR_SHDW3 Register The value in the XCMP4HR_SHDW3 register is loaded into XCMP4HR_ACTIVE register when shadow to active load occurs.

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3.8.2.149 EPWM_XCMP5_SHDW3 Register

3.8.2.149.1 EPWM_XCMP5_SHDW3 Register (Offset = 790h) [reset = 0h]

Additional Compare 5 Shadow 3 Register.

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Figure 3-421. EPWM_XCMP5_SHDW3 Name Register

31	30	29	28	27	26	25	24
XCMP5_SHDW3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XCMP5_SHDW3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
XCMP5HR_SHDW3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
XCMP5HR_SHDW3							
R/W							
0h							

Table 3-762. EPWM_XCMP5_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP5_SHDW3	R/W	0h	XCMP5_SHDW3 Register The value in the XCMP5_SHDW3 register is loaded into XCMP5_ACTIVE register when shadow to active load occurs.
15:0	XCMP5HR_SHDW3	R/W	0h	XCMP5HR_SHDW3 Register The value in the XCMP5HR_SHDW3 register is loaded into XCMP5HR_ACTIVE register when shadow to active load occurs.

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3.8.2.150 EPWM_XCMP6_SHDW3 Register

3.8.2.150.1 EPWM_XCMP6_SHDW3 Register (Offset = 794h) [reset = 0h]

Additional Compare 6 Shadow 3 Register.

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Figure 3-422. EPWM_XCMP6_SHDW3 Name Register

31	30	29	28	27	26	25	24
XCMP6_SHDW3							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP6_SHDW3							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP6HR_SHDW3							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP6HR_SHDW3							
R/W							
0h							

Table 3-763. EPWM_XCMP6_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP6_SHDW3	R/W	0h	XCMP6_SHDW3 Register The value in the XCMP6_SHDW3 register is loaded into XCMP6_ACTIVE register when shadow to active load occurs.
15:0	XCMP6HR_SHDW3	R/W	0h	XCMP6HR_SHDW3 Register The value in the XCMP6HR_SHDW3 register is loaded into XCMP6HR_ACTIVE register when shadow to active load occurs.

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3.8.2.151 EPWM_XCMP7_SHDW3 Register

3.8.2.151.1 EPWM_XCMP7_SHDW3 Register (Offset = 798h) [reset = 0h]

Additional Compare 7 Shadow 3 Register.

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Figure 3-423. EPWM_XCMP7_SHDW3 Name Register

31	30	29	28	27	26	25	24
XCMP7_SHDW3							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP7_SHDW3							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP7HR_SHDW3							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP7HR_SHDW3							
R/W							
0h							

Table 3-764. EPWM_XCMP7_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP7_SHDW3	R/W	0h	XCMP7_SHDW3 Register The value in the XCMP7_SHDW3 register is loaded into XCMP7_ACTIVE register when shadow to active load occurs.
15:0	XCMP7HR_SHDW3	R/W	0h	XCMP7HR_SHDW3 Register The value in the XCMP7HR_SHDW3 register is loaded into XCMP7HR_ACTIVE register when shadow to active load occurs.

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3.8.2.152 EPWM_XCMP8_SHDW3 Register

3.8.2.152.1 EPWM_XCMP8_SHDW3 Register (Offset = 79Ch) [reset = 0h]

Additional Compare 8 Shadow 3 Register.

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Figure 3-424. EPWM_XCMP8_SHDW3 Name Register

31	30	29	28	27	26	25	24
XCMP8_SHDW3							
R/W							
0h							
23	22	21	20	19	18	17	16
XCMP8_SHDW3							
R/W							
0h							
15	14	13	12	11	10	9	8
XCMP8HR_SHDW3							
R/W							
0h							
7	6	5	4	3	2	1	0
XCMP8HR_SHDW3							
R/W							
0h							

Table 3-765. EPWM_XCMP8_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XCMP8_SHDW3	R/W	0h	XCMP8_SHDW3 Register The value in the XCMP8_SHDW3 register is loaded into XCMP8_ACTIVE register when shadow to active load occurs.
15:0	XCMP8HR_SHDW3	R/W	0h	XCMP8HR_SHDW3 Register The value in the XCMP8HR_SHDW3 register is loaded into XCMP8HR_ACTIVE register when shadow to active load occurs.

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3.8.2.153 EPWM_XTBPRD_SHDW3 Register

3.8.2.153.1 EPWM_XTBPRD_SHDW3 Register (Offset = 7A0h) [reset = 0h]

Additional Time Base Period Shadow 3 Register.

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Figure 3-425. EPWM_XTBPRD_SHDW3 Name Register

31	30	29	28	27	26	25	24
XTBPRD_SHDW3							
R/W							
0h							
23	22	21	20	19	18	17	16
XTBPRD_SHDW3							
R/W							
0h							
15	14	13	12	11	10	9	8
XTBPRDHR_SHDW3							
R/W							
0h							
7	6	5	4	3	2	1	0
XTBPRDHR_SHDW3							
R/W							
0h							

Table 3-766. EPWM_XTBPRD_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XTBPRD_SHDW3	R/W	0h	The value in the XTBPRD_SHDW3 register is loaded into XTBPRD_ ACTIVE register when shadow to active load occurs.
15:0	XTBPRDHR_SHDW3	R/W	0h	The value in the XTBPRDHR_SHDW3 register is loaded into XTBPRDHR_ACTIVE register when shadow to active load occurs.

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3.8.2.154 EPWM_XAQCTLA_SHDW3 Register

3.8.2.154.1 EPWM_XAQCTLA_SHDW3 Register (Offset = 7B0h) [reset = 0h]

XAQCTLA Shadow 3 Register.

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Figure 3-426. EPWM_XAQCTLA_SHDW3 Name Register

15	14	13	12	11	10	9	8
XCMP8		XCMP7		XCMP6		XCMP5	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
XCMP4		XCMP3		XCMP2		XCMP1	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-767. EPWM_XAQCTLA_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	XCMP8	R/W	0h	Action when Counter = CMP8 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
13:12	XCMP7	R/W	0h	Action when Counter = CMP7 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
11:10	XCMP6	R/W	0h	Action when Counter = CMP6 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
9:8	XCMP5	R/W	0h	Action when Counter = CMP5 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
7:6	XCMP4	R/W	0h	Action when Counter = CMP4 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
5:4	XCMP3	R/W	0h	Action when Counter = CMP3 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
3:2	XCMP2	R/W	0h	Action when Counter = CMP2 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]

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Table 3-767. EPWM_XAQCTLA_SHDW3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	XCMP1	R/W	0h	Action when Counter = CMP1 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]

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3.8.2.155 EPWM_XAQCTLB_SHDW3 Register

3.8.2.155.1 EPWM_XAQCTLB_SHDW3 Register (Offset = 7B2h) [reset = 0h]

XAQCTLB Shadow 3 Register.

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Figure 3-427. EPWM_XAQCTLB_SHDW3 Name Register

15	14	13	12	11	10	9	8
XCMP8		XCMP7		XCMP6		XCMP5	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							
R							
0h							

Table 3-768. EPWM_XAQCTLB_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	XCMP8	R/W	0h	Action when Counter = CMP8 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
13:12	XCMP7	R/W	0h	Action when Counter = CMP7 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
11:10	XCMP6	R/W	0h	Action when Counter = CMP6 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
9:8	XCMP5	R/W	0h	Action when Counter = CMP5 2'b00 Do nothing [action disabled] 2'b01 Clear [low] 2'b10 Set [high] 2'b11 Toggle [Low -> High, High -> Low]
7:0	RESERVED_1	R	0h	Reserved

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3.8.2.156 EPWM_CMPC_SHDW3 Register

3.8.2.156.1 EPWM_CMPC_SHDW3 Register (Offset = 7BAh) [reset = 0h]

CMPC Shadow 3 Register.

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Figure 3-428. EPWM_CMPC_SHDW3 Name Register

15	14	13	12	11	10	9	8
CMPC_SHDW3							
R/W							
0h							
7	6	5	4	3	2	1	0
CMPC_SHDW3							
R/W							
0h							

Table 3-769. EPWM_CMPC_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPC_SHDW3	R/W	0h	The value in the CMPC_SHDW3 register is loaded into CMPC_ACTIVE register when shadow to active load occurs.

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3.8.2.157 EPWM_CMPD_SHDW3 Register

3.8.2.157.1 EPWM_CMPD_SHDW3 Register (Offset = 7BEh) [reset = 0h]

CMPD Shadow 3 Register.

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Figure 3-429. EPWM_CMPD_SHDW3 Name Register

15	14	13	12	11	10	9	8
CMPD_SHDW3							
R/W							
0h							
7	6	5	4	3	2	1	0
CMPD_SHDW3							
R/W							
0h							

Table 3-770. EPWM_CMPD_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CMPD_SHDW3	R/W	0h	The value in the CMPD_SHDW3 register is loaded into CMPD_ACTIVE register when shadow to active load occurs.

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3.8.2.158 EPWM_XMINMAX_SHDW3 Register

3.8.2.158.1 EPWM_XMINMAX_SHDW3 Register (Offset = 7C4h) [reset = 0h]

XMINMAX Shadow 3 Register.

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Figure 3-430. EPWM_XMINMAX_SHDW3 Name Register

31	30	29	28	27	26	25	24
XMIN_SHDW3							
R/W							
0h							
23	22	21	20	19	18	17	16
XMIN_SHDW3							
R/W							
0h							
15	14	13	12	11	10	9	8
XMAX_SHDW3							
R/W							
0h							
7	6	5	4	3	2	1	0
XMAX_SHDW3							
R/W							
0h							

Table 3-771. EPWM_XMINMAX_SHDW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	XMIN_SHDW3	R/W	0h	The value in the XMIN_SHDW3 register is loaded into XMIN_ACTIVE register when shadow to active load occurs.
15:0	XMAX_SHDW3	R/W	0h	The value in the XMAX_SHDW3 register is loaded into XMAX_ACTIVE register when shadow to active load occurs.

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3.8.2.159 EPWM_DECTL Register

3.8.2.159.1 EPWM_DECTL Register (Offset = 800h) [reset = 0h]

DE control register.

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Figure 3-431. EPWM_DECTL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REENTRYDLY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						MODE	ENABLE
R						R/W	R/W
0h						0h	0h

Table 3-772. EPWM_DECTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:8	REENTRYDLY	R/W	0h	Determines the blocking window after DEACTIVE flag is cleared in which setting of DEACTIVE flag is prevented from being set. 0 : No blocking 1 : Blocked until 1 PWMSYNCOUT event 2 : Blocked until 2 PWMSYNCOUT events . . 255 : Blocked until 127 PWMSYNCOUT events
7:2	RESERVED_1	R	0h	Reserved
1	MODE	R/W	0h	0 : DEACTIVE flag works in cycle by cycle mode. On every PWMSYNCOUT, set condition of DEACTIVE flag is evaluated. If the set condition is not present the flag is cleared. 1 : DEACTIVE flag works in one shot mode [hardware set] and software clear.
0	ENABLE	R/W	0h	DE function enable 0 : Diode Emulation mode functionality is disabled. DEACTIVE flag is not set on a TRIPH_OR_TRIPL event. 1 : Diode Emulation mode functionality is enabled. DEACTIVE flag is set on a TRIPH_OR_TRIPL event. Note: ENABLE bit is cleared on a PWMTRIP event. Software has to re-enable this bit after PWMTRIP condition is serviced.

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3.8.2.160 EPWM_DECOMPSEL Register

3.8.2.160.1 EPWM_DECOMPSEL Register (Offset = 804h) [reset = 0h]

Used to configure the comparator whose trip sources will be used.

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Figure 3-432. EPWM_DECOMPSEL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2		TRIPH					
R		R/W					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1		TRIPL					
R		R/W					
0h		0h					

Table 3-773. EPWM_DECOMPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED_2	R	0h	Reserved
21:16	TRIPH	R/W	0h	000000 : Reserved 000001 : Input-XBAR[0] is the source of TRIPH 000010 : Input-XBAR[1] is the source of TRIPH . . 100000 : Input-XBAR[31] is the source of TRIPH 100001 : CMPSSA0 is the source of TRIPH 100010 : CMPSSA1 is the source of TRIPH . . 101010 : CMPSSA9 is the source of TRIPH 101011 : Reserved . . 110000 : Reserved 110001 : CMPSSB0 is the source of TRIPH 110010 : CMPSSB1 is the source of TRIPH . . 111010 : CMPSSB9 is the source of TRIPH 111011 : Reserved . . 111111 : Reserved Note: All the reserved encodings result in TRIPH being 0.
15:6	RESERVED_1	R	0h	Reserved

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Table 3-773. EPWM_DECOMPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	TRIPL	R/W	0h	000000 : Reserved 000001 : Input-XBAR[0] is the source of TRIPL 000010 : Input-XBAR[1] is the source of TRIPL . . 100000 : Input-XBAR[31] is the source of TRIPL 100001 : CMPSSA0 is the source of TRIPL 100010 : CMPSSA1 is the source of TRIPL . . 101010 : CMPSSA9 is the source of TRIPL 101011 : Reserved . . 110000 : Reserved 110001 : CMPSSB0 is the source of TRIPL 110010 : CMPSSB1 is the source of TRIPL . . 111010 : CMPSSB9 is the source of TRIPL 111011 : Reserved . . 111111 : Reserved Note: All the reserved encodings result in TRIPL being 0.

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3.8.2.161 EPWM_DEACTCTL Register

3.8.2.161.1 EPWM_DEACTCTL Register (Offset = 808h) [reset = 0h]

Used to configure the PWM controls when in DE mode.

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Figure 3-433. EPWM_DEACTCTL Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							

23	22	21	20	19	18	17	16
RESERVED_3							TRIPENABLE
R							R/W
0h							0h

15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_2	TRIPSELB	PWMB		RESERVED_1	TRIPSELA	PWMA	
R	R/W	R/W		R	R/W	R/W	
0h	0h	0h		0h	0h	0h	

Table 3-774. EPWM_DEACTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED_3	R	0h	Reserved
16	TRIPENABLE	R/W	0h	0 : PWMTRIP does not bypass the diode emulation logic. 1 : PWMTRIP bypasses the diode emulation PWM generation logic [not complete bypass of module]
15:7	RESERVED_2	R	0h	Reserved
6	TRIPSELB	R/W	0h	0 : TRIPH 1 : TRIPL
5:4	PWMB	R/W	0h	00 : synchronized version of TRIPH or TRIPL signal as selected by the TRIPSELB 01 : synchronized and inverted version of TRIPH or TRIPL signal as selected by the TRIPSELB 10 : A constant 0 drives PWMB when DEACTIVE flag is set. 11 : A constant 1 drives PWMB when DEACTIVE flag is set.
3	RESERVED_1	R	0h	Reserved
2	TRIPSELA	R/W	0h	0 : TRIPH 1 : TRIPL
1:0	PWMA	R/W	0h	00 : synchronized version of TRIPH or TRIPL signal as selected by the TRIPSELA 01 : synchronized and inverted version of TRIPH or TRIPL signal as selected by the TRIPSELA 10 : A constant 0 drives PWMA when DEACTIVE flag is set. 11 : A constant 1 drives PWMA when DEACTIVE flag is set.

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3.8.2.162 EPWM_DESTS Register

3.8.2.162.1 EPWM_DESTS Register (Offset = 80Ch) [reset = 0h]

DE Status register.

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Figure 3-434. EPWM_DESTS Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							DEACTIVE
R							R
0h							0h

Table 3-775. EPWM_DESTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	DEACTIVE	R	0h	0 : Diode emulation mode is not active 1 : Diode emulation mode is active

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3.8.2.163 EPWM_DEFRC Register

3.8.2.163.1 EPWM_DEFRC Register (Offset = 810h) [reset = 0h]

DE Status force register.

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Figure 3-435. EPWM_DEFRC Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							DEACTIVE
R							R/W1TS
0h							0h

Table 3-776. EPWM_DEFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	DEACTIVE	R/W1TS	0h	0 : No effect. 1 : Forces DEACTIVE flag to 1.

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3.8.2.164 EPWM_DECLR Register

3.8.2.164.1 EPWM_DECLR Register (Offset = 814h) [reset = 0h]

DE Status clear register.

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Figure 3-436. EPWM_DECLR Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							DEACTIVE
R							R/W1TS
0h							0h

Table 3-777. EPWM_DECLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	DEACTIVE	R/W1TS	0h	0 : No effect. 1 : Clears DEACTIVE flag.

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3.8.2.165 EPWM_DEMONCNT Register

3.8.2.165.1 EPWM_DEMONCNT Register (Offset = 820h) [reset = 0h]

DE trip monitor counter.

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Figure 3-437. EPWM_DEMONCNT Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
CNT							
R							
0h							
7	6	5	4	3	2	1	0
CNT							
R							
0h							

Table 3-778. EPWM_DEMONCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_1	R	0h	Reserved
15:0	CNT	R	0h	An 16-bit counter which monitors the frequency of diode mode trip events. When TripHorTripL is active: Increment CNT [increment INCSTEP on every EPWMxSYNC] When TripHorTripL is in-active: Decrement CNT [decrement DECSTEP on every EPWMxSYNC] If[CNT > THRESHOLD] then generate DETRIP and clear the counter. If[[CNT - DECSTEP] < 0] then CNT = 0 If[[CNT + INCSTEP] >= 0xFFFF] then CNT = 0xFFFF Note : CNT is cleared when DECTL.ENABLE is 0 Note: DEMONTHRES == 0x0 should not generate trip as the DEMONTHRES and DEMONCNT registers have reset value of 0x0

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3.8.2.166 EPWM_DEMONCTL Register

3.8.2.166.1 EPWM_DEMONCTL Register (Offset = 824h) [reset = 0h]

DE monitor mode control.

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Figure 3-438. EPWM_DEMONCTL Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							ENABLE
R							R/W
0h							0h

Table 3-779. EPWM_DEMONCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	ENABLE	R/W	0h	Enable bit for DE Mode Monitor counter function. 0:DE Mode Monitor counter function is disabled 1:DE Mode Monitor counter function is enabled

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3.8.2.167 EPWM_DEMONSTEP Register

3.8.2.167.1 EPWM_DEMONSTEP Register (Offset = 828h) [reset = 0h]

DE monitor counter step.

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Figure 3-439. EPWM_DEMONSTEP Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
DECSTEP							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
INCSTEP							
R/W							
0h							

Table 3-780. EPWM_DEMONSTEP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_2	R	0h	Reserved
23:16	DECSTEP	R/W	0h	Defines the decrement step of DEMONCNT.CNT counter.
15:8	RESERVED_1	R	0h	Reserved
7:0	INCSTEP	R/W	0h	Defines the increment step of DEMONCNT.CNT counter.

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3.8.2.168 EPWM_DEMONTHRES Register

3.8.2.168.1 EPWM_DEMONTHRES Register (Offset = 82Ch) [reset = 0h]

DE monitor counter threshold.

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Figure 3-440. EPWM_DEMONTHRES Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
THRESHOLD							
R/W							
0h							

Table 3-781. EPWM_DEMONTHRES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_1	R	0h	Reserved
15:0	THRESHOLD	R/W	0h	Defines the threshold of DE monitor counter.

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3.8.2.169 EPWM_MINDBCFG Register

3.8.2.169.1 EPWM_MINDBCFG Register (Offset = C00h) [reset = 0h]

Minimum dead band configuration register.

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Figure 3-441. EPWM_MINDBCFG Name Register

31	30	29	28	27	26	25	24
RESERVED_4							POLSELB
R							R/W
0h							0h
23	22	21	20	19	18	17	16
SELB				SELBLOCKB	INVERTB	RESERVED_3	ENABLEB
R/W				R/W	R/W	R	R/W
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED_2							POLSELA
R							R/W
0h							0h
7	6	5	4	3	2	1	0
SELA				SELBLOCKA	INVERTA	RESERVED_1	ENABLEA
R/W				R/W	R/W	R	R/W
0h				0h	0h	0h	0h

Table 3-782. EPWM_MINDBCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED_4	R	0h	Reserved
24	POLSELB	R/W	0h	Select signal for the AND OR logic of BLOCKB [output of SELBLOCKB mux] and PWMB signals 0 : Select BLOCKB is inverted and ANDed with PWMB. 1 : Select BLOCKB is Ored with PWMB.
23:20	SELB	R/W	0h	PWMB min dead band reference 0x0 : DEPWMB 0x1 : Output 1 from PWMXBAR 0x2 : Output 2 from PWMXBAR . . 0xf : Output 15 from PWMXBAR
19	SELBLOCKB	R/W	0h	0 : Select BLOCKB as the blocking signal on PWMB. 1 : Select BLOCKA as the blocking signal on PWMB.
18	INVERTB	R/W	0h	0 : No inversion on the selected reference signal which is used in the min deadband logic on PWMB. 1 : Invert the selected reference signal which is used in the min deadband logic on PWMB.
17	RESERVED_3	R	0h	Reserved
16	ENABLEB	R/W	0h	0 : Minimum dead band logic is disabled 1 : Minimum dead band logic is enabled
15:9	RESERVED_2	R	0h	Reserved
8	POLSELA	R/W	0h	Select signal for the AND OR logic of BLOCKA [output of SELBLOCKA mux] and PWMA signals 0 : Select BLOCKA is inverted and ANDed with PWMA. 1 : Select BLOCKA is Ored with PWMA.

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Table 3-782. EPWM_MINDBCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	SELA	R/W	0h	PWMA min dead band reference 0x0 : DEPWMA 0x1 : Output 1 from PWMXBAR 0x2 : Output 2 from PWMXBAR . . 0xf : Output 15 from PWMXBAR
3	SELBLOCKA	R/W	0h	0 : Select BLOCKA as the blocking signal on PWMA. 1 : Select BLOCKB as the blocking signal on PWMB.
2	INVERTA	R/W	0h	0 : No inversion on the selected reference signal which is used in the min deadband logic on PWMA. 1 : Invert the selected reference signal which is used in the min deadband logic on PWMA.
1	RESERVED_1	R	0h	Reserved
0	ENABLEA	R/W	0h	0 : Minimum dead band logic is disabled 1 : Minimum dead band logic is enabled

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3.8.2.170 EPWM_MINDBDLY Register

3.8.2.170.1 EPWM_MINDBDLY Register (Offset = C04h) [reset = 0h]

Minimum dead band delay register.

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Figure 3-442. EPWM_MINDBDLY Name Register

31	30	29	28	27	26	25	24
DELAYB							
R/W							
0h							
23	22	21	20	19	18	17	16
DELAYB							
R/W							
0h							
15	14	13	12	11	10	9	8
DELAYA							
R/W							
0h							
7	6	5	4	3	2	1	0
DELAYA							
R/W							
0h							

Table 3-783. EPWM_MINDBDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DELAYB	R/W	0h	Minimum dead band delay on PWMB in terms of SYSCLK cycles. For delay value of 0, user should configure MINDBCFG[ENABLEA/B] = '0'. If MINDBCFG[ENABLEA/B] = '1' and MINDBDLY[DELAYA/B]='0' then delay is '1' cycle is applied.
15:0	DELAYA	R/W	0h	Minimum dead band delay on PWMA in terms of SYSCLK cycles. For delay value of 0, user should configure MINDBCFG[ENABLEA/B] = '0'. If MINDBCFG[ENABLEA/B] = '1' and MINDBDLY[DELAYA/B]='0' then delay is '1' cycle is applied.

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3.8.2.171 EPWM_LUTCTLA Register

3.8.2.171.1 EPWM_LUTCTLA Register (Offset = C20h) [reset = 1h]

LUT control register on PWMA.

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Figure 3-443. EPWM_LUTCTLA Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LUTDEC7	LUTDEC6	LUTDEC5	LUTDEC4	LUTDEC3	LUTDEC2	LUTDEC1	LUTDEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELXBAR				RESERVED_1			BYPASS
R/W				R			R/W
0h				0h			1h

Table 3-784. EPWM_LUTCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_3	R	0h	Reserved
23	LUTDEC7	R/W	0h	0 : Force 0 1 : Force 1
22	LUTDEC6	R/W	0h	0 : Force 0 1 : Force 1
21	LUTDEC5	R/W	0h	0 : Force 0 1 : Force 1
20	LUTDEC4	R/W	0h	0 : Force 0 1 : Force 1
19	LUTDEC3	R/W	0h	0 : Force 0 1 : Force 1
18	LUTDEC2	R/W	0h	0 : Force 0 1 : Force 1
17	LUTDEC1	R/W	0h	0 : Force 0 1 : Force 1
16	LUTDEC0	R/W	0h	0 : Force 0 1 : Force 1
15:8	RESERVED_2	R	0h	Reserved
7:4	SELXBAR	R/W	0h	Selects one of the 16 outputs of ICSSXBAR to feed into IN3 of LUTA
3:1	RESERVED_1	R	0h	Reserved
0	BYPASS	R/W	1h	1 : Bypass LUT logic on PWMA 0 : PWMA driven by LUTA

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3.8.2.172 EPWM_LUTCTLB Register

3.8.2.172.1 EPWM_LUTCTLB Register (Offset = C24h) [reset = 1h]

LUT control register on PWMB.

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Figure 3-444. EPWM_LUTCTLB Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LUTDEC7	LUTDEC6	LUTDEC5	LUTDEC4	LUTDEC3	LUTDEC2	LUTDEC1	LUTDEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SELXBAR				RESERVED_1			BYPASS
R/W				R			R/W
0h				0h			1h

Table 3-785. EPWM_LUTCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_3	R	0h	Reserved
23	LUTDEC7	R/W	0h	0 : Force 0 1 : Force 1
22	LUTDEC6	R/W	0h	0 : Force 0 1 : Force 1
21	LUTDEC5	R/W	0h	0 : Force 0 1 : Force 1
20	LUTDEC4	R/W	0h	0 : Force 0 1 : Force 1
19	LUTDEC3	R/W	0h	0 : Force 0 1 : Force 1
18	LUTDEC2	R/W	0h	0 : Force 0 1 : Force 1
17	LUTDEC1	R/W	0h	0 : Force 0 1 : Force 1
16	LUTDEC0	R/W	0h	0 : Force 0 1 : Force 1
15:8	RESERVED_2	R	0h	Reserved
7:4	SELXBAR	R/W	0h	Selects one of the 16 outputs of ICSSXBAR to feed into IN3 of LUTB
3:1	RESERVED_1	R	0h	Reserved
0	BYPASS	R/W	1h	1 : Bypass LUT logic on PWMB 0 : PWMB driven by LUTB

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3.9 OTTOCAL

OTTOCAL

3.9.1 OTTOCAL Summaries

OTTOCAL Summaries

Table 3-786. OTTOCAL Registers, Base Address=502E 0000h, Length=4096

Offset	Length	Register Name	OTTOCAL0 Physical Address	OTTOCAL1 Physical Address	OTTOCAL2 Physical Address
42h	16	OTTOCAL_HRPWR	502E 0042h	502E 1042h	502E 2042h
4Ch	16	OTTOCAL_HRMSTEP	502E 004Ch	502E 104Ch	502E 204Ch

Table 3-787. OTTOCAL Registers, Base Address=502E 0000h, Length=4096

Offset	Length	Register Name	OTTOCAL3 Physical Address
42h	16	OTTOCAL_HRPWR	502E 3042h
4Ch	16	OTTOCAL_HRMSTEP	502E 304Ch

3.9.2 OTTOCAL Registers

OTTOCAL Registers

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3.9.2.1 OTTOCAL_HRPWR Register

3.9.2.1.1 OTTOCAL_HRPWR Register (Offset = 42h) [reset = 0h]

HRPWM Power Register
This register is only accessible on EPWM modules with HRPWM capabilities.

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Table 3-788. Instance Table

Instance Name	Physical Address
OTTOCAL0	502E 0042h
OTTOCAL1	502E 1042h
OTTOCAL2	502E 2042h
OTTOCAL3	502E 3042h

Figure 3-445. OTTOCAL_HRPWR Name Register

15	14	13	12	11	10	9	8
CALPWRON	RESERVED_1					CALSEL	
R/W	R					R/W	
0h	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALSEL		TESTSEL	CALSTS	CNTSEL	CALSTART	CALMODE	
R/W		R/W	R	R/W	R/W	R/W	
0h		0h	0h	0h	0h	0h	

Table 3-789. OTTOCAL_HRPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CALPWRON	R/W	0h	MEP Calibration Power Bits [only available on ePWM1] 0:Disables MEP calibration logic in the HRPWM and reduces power consumption. 1:Enables MEP calibration logic
14:10	RESERVED_1	R	0h	Reserved
9:6	CALSEL	R/W	0h	EPWM Delay Line Selection for Calibration:
5	TESTSEL	R/W	0h	Test Mode Select Bit: This bit selects if a dummy delay is added in Oscillator Calibration mode to help reducing frequency when small delays are used:
4	CALSTS	R	0h	Calibration Status Bit: This bit, when set to 1, indicates that calibration is in progress. It is set to 0 when:
3	CNTSEL	R/W	0h	Counter Select Bit: Functionality of this bit has changed. When HRCNT0 or HRCNT1 reaches 0xFFFF, both counters are frozen. This bit will have an effect on when calibration starts:
2	CALSTART	R/W	0h	Calibration Start/Stop Bit:
1:0	CALMODE	R/W	0h	Note: CALMODE bits in HRPWM Module. Not used here.

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3.9.2.2 OTTOCAL_HRMSTEP Register

3.9.2.2.1 OTTOCAL_HRMSTEP Register (Offset = 4Ch) [reset = 0h]

HRPWM MEP Step Register
This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

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Table 3-790. Instance Table

Instance Name	Physical Address
OTTOCAL0	502E 004Ch
OTTOCAL1	502E 104Ch
OTTOCAL2	502E 204Ch
OTTOCAL3	502E 304Ch

Figure 3-446. OTTOCAL_HRMSTEP Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HRMSTEP							
R/W							
0h							

Table 3-791. OTTOCAL_HRMSTEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7:0	HRMSTEP	R/W	0h	High Resolution MEP Step When auto-conversion is enabled [HRCNFG[AUTOCONV] = 1], This 8-bit field contains the MEP_ScaleFactor [number of MEP steps per coarse steps] used by the hardware to automatically convert the value in the CMPAHR, CMPBHR, DBFEDHR, DBREDHR , TBPHSHR, or TBPRDHR register to a scaled micro-edge delay on the high-resolution ePWM output. The value in this register is written by the SFO calibration software at the end of each calibration run.

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3.10 EQEP

EQEP

3.10.1 EQEP Summaries

EQEP Summaries

Table 3-792. EQEP Registers, Base Address=5027 0000h, Length=4096

Offset	Length	Register Name	EQEP0 Physical Address	EQEP1 Physical Address	EQEP2 Physical Address
0h	32	EQEP_QPOSCNT	5027 0000h	5027 1000h	5027 2000h
4h	32	EQEP_QPOSINIT	5027 0004h	5027 1004h	5027 2004h
8h	32	EQEP_QPOSMAX	5027 0008h	5027 1008h	5027 2008h
Ch	32	EQEP_QPOSCMP	5027 000Ch	5027 100Ch	5027 200Ch
10h	32	EQEP_QPOSILAT	5027 0010h	5027 1010h	5027 2010h
14h	32	EQEP_QPOSSLAT	5027 0014h	5027 1014h	5027 2014h
18h	32	EQEP_QPOSLAT	5027 0018h	5027 1018h	5027 2018h
1Ch	32	EQEP_QUTMR	5027 001Ch	5027 101Ch	5027 201Ch
20h	32	EQEP_QUPRD	5027 0020h	5027 1020h	5027 2020h
24h	16	EQEP_QWDTMR	5027 0024h	5027 1024h	5027 2024h
26h	16	EQEP_QWDPRD	5027 0026h	5027 1026h	5027 2026h
28h	16	EQEP_QDECCTL	5027 0028h	5027 1028h	5027 2028h
2Ah	16	EQEP_QEPCTL	5027 002Ah	5027 102Ah	5027 202Ah
2Ch	16	EQEP_QCAPCTL	5027 002Ch	5027 102Ch	5027 202Ch
2Eh	16	EQEP_QPOSCTL	5027 002Eh	5027 102Eh	5027 202Eh
30h	16	EQEP_QEINT	5027 0030h	5027 1030h	5027 2030h
32h	16	EQEP_QFLG	5027 0032h	5027 1032h	5027 2032h
34h	16	EQEP_QCLR	5027 0034h	5027 1034h	5027 2034h
36h	16	EQEP_QFRC	5027 0036h	5027 1036h	5027 2036h
38h	16	EQEP_QEPSTS	5027 0038h	5027 1038h	5027 2038h
3Ah	16	EQEP_QCTMR	5027 003Ah	5027 103Ah	5027 203Ah
3Ch	16	EQEP_QCPRD	5027 003Ch	5027 103Ch	5027 203Ch
3Eh	16	EQEP_QCTMRLAT	5027 003Eh	5027 103Eh	5027 203Eh
40h	16	EQEP_QCPRDLAT	5027 0040h	5027 1040h	5027 2040h
60h	32	EQEP_REV	5027 0060h	5027 1060h	5027 2060h
68h	32	EQEP_QMACTRL	5027 0068h	5027 1068h	5027 2068h
6Ch	32	EQEP_QEPSRCSEL	5027 006Ch	5027 106Ch	5027 206Ch

3.10.2 EQEP Registers

EQEP Registers

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3.10.2.1 EQEP_QPOSCNT Register

3.10.2.1.1 EQEP_QPOSCNT Register (Offset = 0h) [reset = 0h]

Position Counter .

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Table 3-793. Instance Table

Instance Name	Physical Address
EQEP0	5027 0000h
EQEP1	5027 1000h
EQEP2	5027 2000h

Figure 3-447. EQEP_QPOSCNT Name Register

31	30	29	28	27	26	25	24
QPOSCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSCNT							
R/W							
0h							

Table 3-794. EQEP_QPOSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSCNT	R/W	0h	Position Counter This 32-bit position counter register counts up/down on every eQEP pulse based on direction input. This counter acts as a position integrator whose count value is proportional to position from a give reference point. This Register acts as a Read ONLY register while counter is counting up/down. Note: It is recommended to only write to the position counter register [QPOSCNT] during initialization, i.e. when the eQEP position counter is disabled [QPEN bit of QEPCTL is zero]. Once the position counter is enabled [QPEN bit is one], Writing to the eQEP position counter register [QPOSCNT] may cause unexpected results.

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3.10.2.2 EQEP_QPOSINIT Register

3.10.2.2.1 EQEP_QPOSINIT Register (Offset = 4h) [reset = 0h]

Position Counter Init .

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Table 3-795. Instance Table

Instance Name	Physical Address
EQEP0	5027 0004h
EQEP1	5027 1004h
EQEP2	5027 2004h

Figure 3-448. EQEP_QPOSINIT Name Register

31	30	29	28	27	26	25	24
QPOSINIT							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSINIT							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSINIT							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSINIT							
R/W							
0h							

Table 3-796. EQEP_QPOSINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSINIT	R/W	0h	Position Counter Init This register contains the position value that is used to initialize the position counter based on external strobe or index event. The position counter can be initialized through software. Writes to this register should always be full 32-bit writes.

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3.10.2.3 EQEP_QPOSMAX Register

3.10.2.3.1 EQEP_QPOSMAX Register (Offset = 8h) [reset = 0h]

Maximum Position Count .

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Table 3-797. Instance Table

Instance Name	Physical Address
EQEP0	5027 0008h
EQEP1	5027 1008h
EQEP2	5027 2008h

Figure 3-449. EQEP_QPOSMAX Name Register

31	30	29	28	27	26	25	24
QPOSMAX							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSMAX							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSMAX							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSMAX							
R/W							
0h							

Table 3-798. EQEP_QPOSMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSMAX	R/W	0h	Maximum Position Count This register contains the maximum position counter value. Writes to this register should always be full 32-bit writes.

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3.10.2.4 EQEP_QPOSCMP Register

3.10.2.4.1 EQEP_QPOSCMP Register (Offset = Ch) [reset = 0h]

Position Compare .

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Table 3-799. Instance Table

Instance Name	Physical Address
EQEP0	5027 000Ch
EQEP1	5027 100Ch
EQEP2	5027 200Ch

Figure 3-450. EQEP_QPOSCMP Name Register

31	30	29	28	27	26	25	24
QPOSCMP							
R/W							
0h							
23	22	21	20	19	18	17	16
QPOSCMP							
R/W							
0h							
15	14	13	12	11	10	9	8
QPOSCMP							
R/W							
0h							
7	6	5	4	3	2	1	0
QPOSCMP							
R/W							
0h							

Table 3-800. EQEP_QPOSCMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSCMP	R/W	0h	Position Compare The position-compare value in this register is compared with the position counter [QPOSCNT] to generate sync output and/or interrupt on compare match.

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3.10.2.5 EQEP_QPOSILAT Register

3.10.2.5.1 EQEP_QPOSILAT Register (Offset = 10h) [reset = 0h]

Index Position Latch .

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Table 3-801. Instance Table

Instance Name	Physical Address
EQEP0	5027 0010h
EQEP1	5027 1010h
EQEP2	5027 2010h

Figure 3-451. EQEP_QPOSILAT Name Register

31	30	29	28	27	26	25	24
QPOSILAT							
R							
0h							
23	22	21	20	19	18	17	16
QPOSILAT							
R							
0h							
15	14	13	12	11	10	9	8
QPOSILAT							
R							
0h							
7	6	5	4	3	2	1	0
QPOSILAT							
R							
0h							

Table 3-802. EQEP_QPOSILAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSILAT	R	0h	Index Position Latch The position-counter value is latched into this register on an index event as defined by the QEPCTL[IEL] bits.

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3.10.2.6 EQEP_QPOSSLAT Register

3.10.2.6.1 EQEP_QPOSSLAT Register (Offset = 14h) [reset = 0h]

Strobe Position Latch.

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Table 3-803. Instance Table

Instance Name	Physical Address
EQEP0	5027 0014h
EQEP1	5027 1014h
EQEP2	5027 2014h

Figure 3-452. EQEP_QPOSSLAT Name Register

31	30	29	28	27	26	25	24
QPOSSLAT							
R							
0h							
23	22	21	20	19	18	17	16
QPOSSLAT							
R							
0h							
15	14	13	12	11	10	9	8
QPOSSLAT							
R							
0h							
7	6	5	4	3	2	1	0
QPOSSLAT							
R							
0h							

Table 3-804. EQEP_QPOSSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSSLAT	R	0h	Strobe Position Latch The position-counter value is latched into this register on a strobe event as defined by the QEPCTL[SEL] bits.

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3.10.2.7 EQEP_QPOSLAT Register

3.10.2.7.1 EQEP_QPOSLAT Register (Offset = 18h) [reset = 0h]

Position Latch .

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Table 3-805. Instance Table

Instance Name	Physical Address
EQEP0	5027 0018h
EQEP1	5027 1018h
EQEP2	5027 2018h

Figure 3-453. EQEP_QPOSLAT Name Register

31	30	29	28	27	26	25	24
QPOSLAT							
R							
0h							
23	22	21	20	19	18	17	16
QPOSLAT							
R							
0h							
15	14	13	12	11	10	9	8
QPOSLAT							
R							
0h							
7	6	5	4	3	2	1	0
QPOSLAT							
R							
0h							

Table 3-806. EQEP_QPOSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QPOSLAT	R	0h	Position Latch The position-counter value is latched into this register on a unit time out event.

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3.10.2.8 EQEP_QUTMR Register

3.10.2.8.1 EQEP_QUTMR Register (Offset = 1Ch) [reset = 0h]

QEP Unit Timer .

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Table 3-807. Instance Table

Instance Name	Physical Address
EQEP0	5027 001Ch
EQEP1	5027 101Ch
EQEP2	5027 201Ch

Figure 3-454. EQEP_QUTMR Name Register

31	30	29	28	27	26	25	24
QUTMR							
R/W							
0h							
23	22	21	20	19	18	17	16
QUTMR							
R/W							
0h							
15	14	13	12	11	10	9	8
QUTMR							
R/W							
0h							
7	6	5	4	3	2	1	0
QUTMR							
R/W							
0h							

Table 3-808. EQEP_QUTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUTMR	R/W	0h	QEP Unit Timer This register acts as time base for unit time event generation. When this timer value matches the unit time period value a unit time event is generated.

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3.10.2.9 EQEP_QUPRD Register

3.10.2.9.1 EQEP_QUPRD Register (Offset = 20h) [reset = 0h]

QEP Unit Period .

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Table 3-809. Instance Table

Instance Name	Physical Address
EQEP0	5027 0020h
EQEP1	5027 1020h
EQEP2	5027 2020h

Figure 3-455. EQEP_QUPRD Name Register

31	30	29	28	27	26	25	24
QUPRD							
R/W							
0h							
23	22	21	20	19	18	17	16
QUPRD							
R/W							
0h							
15	14	13	12	11	10	9	8
QUPRD							
R/W							
0h							
7	6	5	4	3	2	1	0
QUPRD							
R/W							
0h							

Table 3-810. EQEP_QUPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUPRD	R/W	0h	QEP Unit Period This register contains the period count for the unit timer to generate periodic unit time events. These events latch the eQEP position information at periodic intervals and optionally generate an interrupt. Writes to this register should always be full 32-bit writes.

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3.10.2.10 EQEP_QWDTMR Register

3.10.2.10.1 EQEP_QWDTMR Register (Offset = 24h) [reset = 0h]

QEP Watchdog Timer .

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Table 3-811. Instance Table

Instance Name	Physical Address
EQEP0	5027 0024h
EQEP1	5027 1024h
EQEP2	5027 2024h

Figure 3-456. EQEP_QWDTMR Name Register

15	14	13	12	11	10	9	8
QWDTMR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QWDTMR							
R/W							
0h							

Table 3-812. EQEP_QWDTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QWDTMR	R/W	0h	QEP Watchdog Timer This register acts as time base for the watchdog to detect motor stalls. When this timer value matches with the watchdog's period value a watchdog timeout interrupt is generated. This register is reset upon edge transition in quadrature-clock indicating the motion.

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3.10.2.11 EQEP_QWDPRD Register

3.10.2.11.1 EQEP_QWDPRD Register (Offset = 26h) [reset = 0h]

QEP Watchdog Period .

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Table 3-813. Instance Table

Instance Name	Physical Address
EQEP0	5027 0026h
EQEP1	5027 1026h
EQEP2	5027 2026h

Figure 3-457. EQEP_QWDPRD Name Register

15	14	13	12	11	10	9	8
QWDPRD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QWDPRD							
R/W							
0h							

Table 3-814. EQEP_QWDPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QWDPRD	R/W	0h	QEP Watchdog Period This register contains the time-out count for the eQEP peripheral watch dog timer. When the watchdog timer value matches the watchdog period value, a watchdog timeout interrupt is generated.

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3.10.2.12 EQEP_QDECCTL Register

3.10.2.12.1 EQEP_QDECCTL Register (Offset = 28h) [reset = 0h]

Quadrature Decoder Control .

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Table 3-815. Instance Table

Instance Name	Physical Address
EQEP0	5027 0028h
EQEP1	5027 1028h
EQEP2	5027 2028h

Figure 3-458. EQEP_QDECCTL Name Register

15	14	13	12	11	10	9	8
QSRC		SOEN	SPSEL	XCR	SWAP	IGATE	QAP
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QBP	QIP	QSP	RESERVED_1				QIDIRE
R/W	R/W	R/W	R				R/W
0h	0h	0h	0h				0h

Table 3-816. EQEP_QDECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	QSRC	R/W	0h	Position-counter source selection
13	SOEN	R/W	0h	Sync output-enable 0 Disable position-compare sync output 1 Enable position-compare sync output
12	SPSEL	R/W	0h	Sync output pin selection 0 Index pin is used for sync output 1 Strobe pin is used for sync output
11	XCR	R/W	0h	External Clock Rate 0 2x resolution: Count the rising/falling edge 1 1x resolution: Count the rising edge only
10	SWAP	R/W	0h	CLK/DIR Signal Source for Position Counter 0 Quadrature-clock inputs are not swapped 1 Quadrature-clock inputs are swapped
9	IGATE	R/W	0h	Index pulse gating option 0 Disable gating of Index pulse 1 Gate the index pin with strobe
8	QAP	R/W	0h	QEPA input polarity 0 No effect 1 Negates QEPA input
7	QBP	R/W	0h	QEPB input polarity 0 No effect 1 Negates QEPB input
6	QIP	R/W	0h	QEPI input polarity 0 No effect 1 Negates QEPI input

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Table 3-816. EQEP_QDECCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	QSP	R/W	0h	QEPS input polarity 0 No effect 1 Negates QEPS input
4:1	RESERVED_1	R	0h	Reserved
0	QIDIRE	R/W	0h	0 - Compatible mode, Behavior same as existing devices 1 - Enhancement for Direction change during Index will be enabled

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3.10.2.13 EQEP_QEPCTL Register

3.10.2.13.1 EQEP_QEPCTL Register (Offset = 2Ah) [reset = 0h]

QEP Control .

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Table 3-817. Instance Table

Instance Name	Physical Address
EQEP0	5027 002Ah
EQEP1	5027 102Ah
EQEP2	5027 202Ah

Figure 3-459. EQEP_QEPCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PCRM		SEI		IEI	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
SWI	SEL	IEL		QPEN	QCLM	UTE	WDE
R/W	R/W	R/W		R/W	R/W	R/W	R/W
0h	0h	0h		0h	0h	0h	0h

Table 3-818. EQEP_QEPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	FREE_SOFT	R/W	0h	Emulation mode 0 QPOSCNT behavior Position counter stops immediately on emulation suspend 0h (R/W) = QWDTMR behavior Watchdog counter stops immediately 0h (R/W) = QUTMR behavior Unit timer stops immediately 0h (R/W) = QCTMR behavior Capture Timer stops immediately 1 QPOSCNT behavior Position counter continues to count until the rollover 1h (R/W) = QWDTMR behavior Watchdog counter counts until WD period match roll over 1h (R/W) = QUTMR behavior Unit timer counts until period rollover 1h (R/W) = QCTMR behavior Capture Timer counts until next unit period event 2 QPOSCNT behavior Position counter is unaffected by emulation suspend 2h (R/W) = QWDTMR behavior Watchdog counter is unaffected by emulation suspend 2h (R/W) = QUTMR behavior Unit timer is unaffected by emulation suspend 2h (R/W) = QCTMR behavior Capture Timer is unaffected by emulation suspend 3 Same as FREE_SOFT_2
13:12	PCRM	R/W	0h	Postion counter reset 0 Position counter reset on an index event 1 Position counter reset on the maximum position 2 Position counter reset on the first index event 3 Position counter reset on a unit time event

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Table 3-818. EQEP_QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	SEI	R/W	0h	Strobe event initialization of position counter 0 Does nothing (action disabled) 1 Does nothing (action disabled) 2 Initializes the position counter on rising edge of the QEPS signal 3 Clockwise Direction: Initializes the position counter on the rising edge of QEPS strobe Counter Clockwise Direction: Initializes the position counter on the falling edge of QEPS strobe
9:8	IEI	R/W	0h	Index event init of position count 0 Do nothing (action disabled) 1 Do nothing (action disabled) 2 Initializes the position counter on the rising edge of the QEPI signal (QPOSCNT = QPOSINIT) 3 Initializes the position counter on the falling edge of QEPI signal (QPOSCNT = QPOSINIT)
7	SWI	R/W	0h	Software init position counter 0 Do nothing (action disabled) 1 Initialize position counter (QPOSCNT=QPOSINIT). This bit is not cleared automatically
6	SEL	R/W	0h	Strobe event latch of position counter 0 The position counter is latched on the rising edge of QEPS strobe (QPOSSLAT = POSCCNT). Latching on the falling edge can be done by inverting the strobe input using the QSP bit in the QDECCTL register 1 Clockwise Direction: Position counter is latched on rising edge of QEPS strobe Counter Clockwise Direction: Position counter is latched on falling edge of QEPS strobe
5:4	IEL	R/W	0h	Index event latch of position counter [software index marker] 0 Reserved 1 Latches position counter on rising edge of the index signal 2 Latches position counter on falling edge of the index signal 3 Software index marker. Latches the position counter and quadrature direction flag on index event marker. The position counter is latched to the QPOSILAT register and the direction flag is latched in the QEPSTS[QDLF] bit. This mode is useful for software index marking.
3	QPEN	R/W	0h	Quadrature position counter enable/software reset 0 Reset the eQEP peripheral internal operating flags/read-only registers. Control/configuration registers are not disturbed by a software reset. When QPEN is disabled, some flags in the QFLG register do not get reset or cleared and show the actual state of that flag. 1 eQEP position counter is enabled

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Table 3-818. EQEP_QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	QCLM	R/W	0h	QEP capture latch mode 0 Latch on position counter read by CPU. Capture timer and capture period values are latched into QCTMRLAT and QCPRDLAT registers when CPU reads the QPOSCNT register. 1 Latch on unit time out. Position counter, capture timer and capture period values are latched into QPOSLAT, QCTMRLAT and QCPRDLAT registers on unit time out.
1	UTE	R/W	0h	QEP unit timer enable 0 Disable eQEP unit timer 1 Enable unit timer
0	WDE	R/W	0h	QEP watchdog enable 0 Disable the eQEP watchdog timer 1 Enable the eQEP watchdog timer

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3.10.2.14 EQEP_QCAPCTL Register

3.10.2.14.1 EQEP_QCAPCTL Register (Offset = 2Ch) [reset = 0h]

Qaudrature Capture Control .

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Table 3-819. Instance Table

Instance Name	Physical Address
EQEP0	5027 002Ch
EQEP1	5027 102Ch
EQEP2	5027 202Ch

Figure 3-460. EQEP_QCAPCTL Name Register

15	14	13	12	11	10	9	8
CEN	RESERVED_1						
R/W	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	CCPS			UPPS			
R	R/W			R/W			
0h	0h			0h			

Table 3-820. EQEP_QCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CEN	R/W	0h	Enable eQEP capture 0 eQEP capture unit is disabled 1 eQEP capture unit is enabled
14:7	RESERVED_1	R	0h	Reserved
6:4	CCPS	R/W	0h	EQEP capture timer clock prescaler 0 CAPCLK = SYSCLKOUT/1 1 CAPCLK = SYSCLKOUT/2 2 CAPCLK = SYSCLKOUT/4 3 CAPCLK = SYSCLKOUT/8 4 CAPCLK = SYSCLKOUT/16 5 CAPCLK = SYSCLKOUT/32 6 CAPCLK = SYSCLKOUT/64 7 CAPCLK = SYSCLKOUT/128
3:0	UPPS	R/W	0h	Unit position event prescaler 0 UPEVNT = QCLK/1 1 UPEVNT = QCLK/2 2 UPEVNT = QCLK/4 3 UPEVNT = QCLK/8 4 UPEVNT = QCLK/16 5 UPEVNT = QCLK/32 6 UPEVNT = QCLK/64 7 UPEVNT = QCLK/128 8 UPEVNT = QCLK/256 9 UPEVNT = QCLK/512 10 UPEVNT = QCLK/1024 11 UPEVNT = QCLK/2048 12 Reserved 13 Reserved 14 Reserved 15 Reserved

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3.10.2.15 EQEP_QPOSCTL Register

3.10.2.15.1 EQEP_QPOSCTL Register (Offset = 2Eh) [reset = 0h]

Position Compare Control .

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Table 3-821. Instance Table

Instance Name	Physical Address
EQEP0	5027 002Eh
EQEP1	5027 102Eh
EQEP2	5027 202Eh

Figure 3-461. EQEP_QPOSCTL Name Register

15	14	13	12	11	10	9	8
PCSHDW	PCLOAD	PCPOL	PCE	PCSPW			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCSPW							
R/W							
0h							

Table 3-822. EQEP_QPOSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCSHDW	R/W	0h	Position compare of shadow enable 0 Shadow disabled, load Immediate 1 Shadow enabled
14	PCLOAD	R/W	0h	Position compare of shadow load 0 Load on QPOSCNT = 0 1 Load when QPOSCNT = QPOSCMP
13	PCPOL	R/W	0h	Polarity of sync output 0 Active HIGH pulse output 1 Active LOW pulse output
12	PCE	R/W	0h	Position compare enable/disable 0 Disable position compare unit 1 Enable position compare unit
11:0	PCSPW	R/W	0h	Select-position-compare sync output pulse width 0 1 * 4 * SYSCLKOUT cycles 1 2 * 4 * SYSCLKOUT cycles 4095 4096 * 4 * SYSCLKOUT cycles

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3.10.2.16 EQEP_QEINT Register

3.10.2.16.1 EQEP_QEINT Register (Offset = 30h) [reset = 0h]

QEP Interrupt Control .

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Table 3-823. Instance Table

Instance Name	Physical Address
EQEP0	5027 0030h
EQEP1	5027 1030h
EQEP2	5027 2030h

Figure 3-462. EQEP_QEINT Name Register

15	14	13	12	11	10	9	8
RESERVED_2			QMAE	UTO	IEL	SEL	PCM
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	QPE	PCE	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-824. EQEP_QEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12	QMAE	R/W	0h	QMA Error Interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
11	UTO	R/W	0h	Unit time out interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
10	IEL	R/W	0h	Index event latch interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
9	SEL	R/W	0h	Strobe event latch interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
8	PCM	R/W	0h	Position-compare match interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
7	PCR	R/W	0h	Position-compare ready interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
6	PCO	R/W	0h	Position counter overflow interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
5	PCU	R/W	0h	Position counter underflow interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
4	WTO	R/W	0h	Watchdog time out interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled

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Table 3-824. EQEP_QEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	QDC	R/W	0h	Quadrature direction change interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
2	QPE	R/W	0h	Quadrature phase error interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
1	PCE	R/W	0h	Position counter error interrupt enable 0 Interrupt is disabled 1 Interrupt is enabled
0	RESERVED_1	R	0h	Reserved

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3.10.2.17 EQEP_QFLG Register

3.10.2.17.1 EQEP_QFLG Register (Offset = 32h) [reset = 0h]

QEP Interrupt Flag .

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Table 3-825. Instance Table

Instance Name	Physical Address
EQEP0	5027 0032h
EQEP1	5027 1032h
EQEP2	5027 2032h

Figure 3-463. EQEP_QFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_1			QMAE	UTO	IEL	SEL	PCM
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-826. EQEP_QFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	QMAE	R	0h	QMA Error interrupt flag 0 No interrupt generated 1 Interrupt was generated
11	UTO	R	0h	Unit time out interrupt flag 0 No interrupt generated 1 Set by eQEP unit timer period match
10	IEL	R	0h	Index event latch interrupt flag 0 No interrupt generated 1 This bit is set after latching the QPOSCNT to QPOSILAT
9	SEL	R	0h	Strobe event latch interrupt flag 0 No interrupt generated 1 This bit is set after latching the QPOSCNT to QPOSSLAT
8	PCM	R	0h	EQEP compare match event interrupt flag 0 No interrupt generated 1 This bit is set on position-compare match
7	PCR	R	0h	Position-compare ready interrupt flag 0 No interrupt generated 1 This bit is set after transferring the shadow register value to the active position compare register
6	PCO	R	0h	Position counter overflow interrupt flag 0 No interrupt generated 1 This bit is set on position counter overflow.

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Table 3-826. EQEP_QFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PCU	R	0h	Position counter underflow interrupt flag 0 No interrupt generated 1 This bit is set on position counter underflow.
4	WTO	R	0h	Watchdog timeout interrupt flag 0 No interrupt generated 1 Set by watchdog timeout
3	QDC	R	0h	Quadrature direction change interrupt flag 0 No interrupt generated 1 Interrupt was generated
2	PHE	R	0h	Quadrature phase error interrupt flag 0 No interrupt generated 1 Set on simultaneous transition of QEPA and QEPB
1	PCE	R	0h	Position counter error interrupt flag 0 No interrupt generated 1 Position counter error
0	INT	R	0h	Global interrupt status flag 0 No interrupt generated 1 Interrupt was generated

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3.10.2.18 EQEP_QCLR Register

3.10.2.18.1 EQEP_QCLR Register (Offset = 34h) [reset = 0h]

QEP Interrupt Clear .

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Table 3-827. Instance Table

Instance Name	Physical Address
EQEP0	5027 0034h
EQEP1	5027 1034h
EQEP2	5027 2034h

Figure 3-464. EQEP_QCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1			QMAE	UTO	IEL	SEL	PCM
R			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	PHE	PCE	INT
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-828. EQEP_QCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	QMAE	R/W1TS	0h	Clear QMA Error interrupt flag 0 No effect 1 Clears the interrupt flag
11	UTO	R/W1TS	0h	Clear unit time out interrupt flag 0 No effect 1 Clears the interrupt flag
10	IEL	R/W1TS	0h	Clear index event latch interrupt flag 0 No effect 1 Clears the interrupt flag
9	SEL	R/W1TS	0h	Clear strobe event latch interrupt flag 0 No effect 1 Clears the interrupt flag
8	PCM	R/W1TS	0h	Clear eQEP compare match event interrupt flag 0 No effect 1 Clears the interrupt flag
7	PCR	R/W1TS	0h	Clear position-compare ready interrupt flag 0 No effect 1 Clears the interrupt flag
6	PCO	R/W1TS	0h	Clear position counter overflow interrupt flag 0 No effect 1 Clears the interrupt flag
5	PCU	R/W1TS	0h	Clear position counter underflow interrupt flag 0 No effect 1 Clears the interrupt flag
4	WTO	R/W1TS	0h	Clear watchdog timeout interrupt flag 0 No effect 1 Clears the interrupt flag

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Table 3-828. EQEP_QCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	QDC	R/W1TS	0h	Clear quadrature direction change interrupt flag 0 No effect 1 Clears the interrupt flag
2	PHE	R/W1TS	0h	Clear quadrature phase error interrupt flag 0 No effect 1 Clears the interrupt flag
1	PCE	R/W1TS	0h	Clear position counter error interrupt flag 0 No effect 1 Clears the interrupt flag
0	INT	R/W1TS	0h	Global interrupt clear flag 0 No effect 1 Clears the interrupt flag

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3.10.2.19 EQEP_QFRC Register

3.10.2.19.1 EQEP_QFRC Register (Offset = 36h) [reset = 0h]

QEP Interrupt Force .

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Table 3-829. Instance Table

Instance Name	Physical Address
EQEP0	5027 0036h
EQEP1	5027 1036h
EQEP2	5027 2036h

Figure 3-465. EQEP_QFRC Name Register

15	14	13	12	11	10	9	8
RESERVED_2			QMAE	UTO	IEL	SEL	PCM
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCR	PCO	PCU	WTO	QDC	PHE	PCE	RESERVED_1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-830. EQEP_QFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12	QMAE	R/W	0h	Force QMA error interrupt 0 `No effect` 1 `Force the interrupt`
11	UTO	R/W	0h	Force unit time out interrupt 0 `No effect` 1 `Force the interrupt`
10	IEL	R/W	0h	Force index event latch interrupt 0 `No effect` 1 `Force the interrupt`
9	SEL	R/W	0h	Force strobe event latch interrupt 0 `No effect` 1 `Force the interrupt`
8	PCM	R/W	0h	Force position-compare match interrupt 0 `No effect` 1 `Force the interrupt`
7	PCR	R/W	0h	Force position-compare ready interrupt 0 `No effect` 1 `Force the interrupt`
6	PCO	R/W	0h	Force position counter overflow interrupt 0 `No effect` 1 `Force the interrupt`
5	PCU	R/W	0h	Force position counter underflow interrupt 0 `No effect` 1 `Force the interrupt`
4	WTO	R/W	0h	Force watchdog time out interrupt 0 `No effect` 1 `Force the interrupt`

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Table 3-830. EQEP_QFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	QDC	R/W	0h	Force quadrature direction change interrupt 0 No effect 1 Force the interrupt
2	PHE	R/W	0h	Force quadrature phase error interrupt 0 No effect 1 Force the interrupt
1	PCE	R/W	0h	Force position counter error interrupt 0 No effect 1 Force the interrupt
0	RESERVED_1	R	0h	Reserved

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3.10.2.20 EQEP_QEPSTS Register

3.10.2.20.1 EQEP_QEPSTS Register (Offset = 38h) [reset = 80h]

QEP Status .

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Table 3-831. Instance Table

Instance Name	Physical Address
EQEP0	5027 0038h
EQEP1	5027 1038h
EQEP2	5027 2038h

Figure 3-466. EQEP_QEPSTS Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UPEVNT	FIDF	QDF	QDLF	COEF	CDEF	FIMF	PCEF
R/W1TS	R	R	R	R/W1TS	R/W1TS	R/W1TS	R
1h	0h	0h	0h	0h	0h	0h	0h

Table 3-832. EQEP_QEPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7	UPEVNT	R/W1TS	1h	Unit position event flag 0 No unit position event detected 1 Unit position event detected. Write 1 to clear
6	FIDF	R	0h	Direction on the first index marker Status of the direction is latched on the first index event marker. 0 Counter-clockwise rotation (or reverse movement) on the first index event 1 Clockwise rotation (or forward movement) on the first index event
5	QDF	R	0h	Quadrature direction flag 0 Counter-clockwise rotation (or reverse movement) 1 Clockwise rotation (or forward movement)
4	QDLF	R	0h	EQEP direction latch flag 0 Counter-clockwise rotation (or reverse movement) on index event marker 1 Clockwise rotation (or forward movement) on index event marker
3	COEF	R/W1TS	0h	Capture overflow error flag 0 Overflow has not occurred. 1 Overflow occurred in eQEP Capture timer (QEPCTMR). This bit is cleared by writing a '1'.
2	CDEF	R/W1TS	0h	Capture direction error flag 0 Capture direction error has not occurred. 1 Direction change occurred between the capture position event. This bit is cleared by writing a '1'.

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Table 3-832. EQEP_QEPSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FIMF	R/W1TS	0h	First index marker flag 0 First index pulse has not occurred. 1 Set by first occurrence of index pulse. This bit is cleared by writing a '1'.
0	PCEF	R	0h	Position counter error flag. This bit is not sticky and it is updated for every index event. 0 No error occurred during the last index transition 1 Position counter error

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3.10.2.21 EQEP_QCTMR Register

3.10.2.21.1 EQEP_QCTMR Register (Offset = 3Ah) [reset = 0h]

QEP Capture Timer .

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Table 3-833. Instance Table

Instance Name	Physical Address
EQEP0	5027 003Ah
EQEP1	5027 103Ah
EQEP2	5027 203Ah

Figure 3-467. EQEP_QCTMR Name Register

15	14	13	12	11	10	9	8
QCTMR							
R/W							
0h							
7	6	5	4	3	2	1	0
QCTMR							
R/W							
0h							

Table 3-834. EQEP_QCTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCTMR	R/W	0h	This register provides time base for edge capture unit.

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3.10.2.22 EQEP_QCPRD Register

3.10.2.22.1 EQEP_QCPRD Register (Offset = 3Ch) [reset = 0h]

QEP Capture Period .

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Table 3-835. Instance Table

Instance Name	Physical Address
EQEP0	5027 003Ch
EQEP1	5027 103Ch
EQEP2	5027 203Ch

Figure 3-468. EQEP_QCPRD Name Register

15	14	13	12	11	10	9	8
QCPRD							
R/W							
0h							
7	6	5	4	3	2	1	0
QCPRD							
R/W							
0h							

Table 3-836. EQEP_QCPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCPRD	R/W	0h	This register holds the period count value between the last successive eQEP position events

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3.10.2.23 EQEP_QCTMRLAT Register

3.10.2.23.1 EQEP_QCTMRLAT Register (Offset = 3Eh) [reset = 0h]

QEP Capture Latch .

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Table 3-837. Instance Table

Instance Name	Physical Address
EQEP0	5027 003Eh
EQEP1	5027 103Eh
EQEP2	5027 203Eh

Figure 3-469. EQEP_QCTMRLAT Name Register

15	14	13	12	11	10	9	8
QCTMRLAT							
R							
0h							
7	6	5	4	3	2	1	0
QCTMRLAT							
R							
0h							

Table 3-838. EQEP_QCTMRLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCTMRLAT	R	0h	The eQEP capture timer value can be latched into this register on two events viz., unit timeout event, Reading the eQEP position counter.

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3.10.2.24 EQEP_QCPRDLAT Register

3.10.2.24.1 EQEP_QCPRDLAT Register (Offset = 40h) [reset = 0h]

QEP Capture Period Latch .

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Table 3-839. Instance Table

Instance Name	Physical Address
EQEP0	5027 0040h
EQEP1	5027 1040h
EQEP2	5027 2040h

Figure 3-470. EQEP_QCPRDLAT Name Register

15	14	13	12	11	10	9	8
QCPRDLAT							
R							
0h							
7	6	5	4	3	2	1	0
QCPRDLAT							
R							
0h							

Table 3-840. EQEP_QCPRDLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QCPRDLAT	R	0h	EQEP capture period value can be latched into this register on two events viz., unit timeout event, Reading the eQEP position counter.

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3.10.2.25 EQEP_REV Register

3.10.2.25.1 EQEP_REV Register (Offset = 60h) [reset = 11h]

QEP Revision Number.

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Table 3-841. Instance Table

Instance Name	Physical Address
EQEP0	5027 0060h
EQEP1	5027 1060h
EQEP2	5027 2060h

Figure 3-471. EQEP_REV Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1		MINOR			MAJOR		
R		R			R		
0h		2h			1h		

Table 3-842. EQEP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED_1	R	0h	Reserved
5:3	MINOR	R	2h	This field specifies the Minor Revision number for the eQEP IP.
2:0	MAJOR	R	1h	This field specifies the Major Revision number for the eQEP IP.

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3.10.2.26 EQEP_QMACTRL Register

3.10.2.26.1 EQEP_QMACTRL Register (Offset = 68h) [reset = 0h]

QMA Control register.

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Table 3-843. Instance Table

Instance Name	Physical Address
EQEP0	5027 0068h
EQEP1	5027 1068h
EQEP2	5027 2068h

Figure 3-472. EQEP_QMACTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1					MODE		
R					R/W		
0h					0h		

Table 3-844. EQEP_QMACTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED_1	R	0h	Reserved
2:0	MODE	R/W	0h	Select Mode for QMA mode: 000 : QMA Module is bypassed. 001 : QMA Mode-1 operation selected 010 : QMA Mode-2 operation selected 011 : QMA Module is bypassed [reserved] 1xx : QMA Module is bypassed [reserved]

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3.10.2.27 EQEP_QEPSRCSEL Register

3.10.2.27.1 EQEP_QEPSRCSEL Register (Offset = 6Ch) [reset = 0h]

QEP Source Select Register.

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Table 3-845. Instance Table

Instance Name	Physical Address
EQEP0	5027 006Ch
EQEP1	5027 106Ch
EQEP2	5027 206Ch

Figure 3-473. EQEP_QEPSRCSEL Name Register

31	30	29	28	27	26	25	24
RESERVED_4			QEPSSEL				
R			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED_3			QEPISEL				
R			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED_2			QEPBSEL				
R			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED_1			QEPASEL				
R			R/W				
0h			0h				

Table 3-846. EQEP_QEPSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED_4	R	0h	Reserved
28:24	QEPSSEL	R/W	0h	QEP Strobe source select: 0x0 : Reserved 0x1 : Device Pin 0x2 : PWMXBAR.Out[0] 0x3 : PWMXBAR.Out[1] ... 0x1F : PWMXBAR.Out[29] Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.
23:21	RESERVED_3	R	0h	Reserved
20:16	QEPISEL	R/W	0h	QEP Index source select: 0x0 : Reserved 0x1 : Device Pin 0x2 : PWMXBAR.Out[0] 0x3 : PWMXBAR.Out[1] ... 0x1F : PWMXBAR.Out[29] Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.
15:13	RESERVED_2	R	0h	Reserved

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Table 3-846. EQEP_QEPSRCSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:8	QEPBSEL	R/W	0h	QEPB source select: 0x0 : Reserved 0x1 : Device Pin 0x2 : PWMXBAR.Out[0] 0x3 : PWMXBAR.Out[1] ... 0x1F : PWMXBAR.Out[29] Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.
7:5	RESERVED_1	R	0h	Reserved
4:0	QEPASEL	R/W	0h	QEPA source select: 0x0 : Reserved 0x1 : Device Pin 0x2 : PWMXBAR.Out[0] 0x3 : PWMXBAR.Out[1] ... 0x1F : PWMXBAR.Out[29] Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.

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3.11 FSI_RX

FSI_RX

3.11.1 FSI_RX Summaries

FSI_RX Summaries

Table 3-847. FSI_RX_CFG Registers, Base Address=5029 0000h, Length=4096

Offset	Length	Register Name	FSI_RX0 Physical Address	FSI_RX1 Physical Address	FSI_RX2 Physical Address
0h	16	FSI_RX_CFG_RX_MASTER_CTRL_ALTC	5029 0000h	5029 1000h	502B 0000h
8h	16	FSI_RX_CFG_RX_OPER_CTRL	5029 0008h	5029 1008h	502B 0008h
Ch	16	FSI_RX_CFG_RX_FRAME_INFO	5029 000Ch	5029 100Ch	502B 000Ch
Eh	16	FSI_RX_CFG_RX_FRAME_TAG_UDATA	5029 000Eh	5029 100Eh	502B 000Eh
10h	16	FSI_RX_CFG_RX_DMA_CTRL	5029 0010h	5029 1010h	502B 0010h
14h	16	FSI_RX_CFG_RX_EVT_STS_ALT1	5029 0014h	5029 1014h	502B 0014h
16h	16	FSI_RX_CFG_RX_CRC_INFO	5029 0016h	5029 1016h	502B 0016h
18h	16	FSI_RX_CFG_RX_EVT_CLR_ALT1	5029 0018h	5029 1018h	502B 0018h
1Ah	16	FSI_RX_CFG_RX_EVT_FRC_ALT1	5029 001Ah	5029 101Ah	502B 001Ah
1Ch	16	FSI_RX_CFG_RX_BUF_PTR_LOAD	5029 001Ch	5029 101Ch	502B 001Ch
1Eh	16	FSI_RX_CFG_RX_BUF_PTR_STS	5029 001Eh	5029 101Eh	502B 001Eh
20h	16	FSI_RX_CFG_RX_FRAME_WD_CTRL	5029 0020h	5029 1020h	502B 0020h
24h	32	FSI_RX_CFG_RX_FRAME_WD_REF	5029 0024h	5029 1024h	502B 0024h
28h	32	FSI_RX_CFG_RX_FRAME_WD_CNT	5029 0028h	5029 1028h	502B 0028h
2Ch	16	FSI_RX_CFG_RX_PING_WD_CTRL	5029 002Ch	5029 102Ch	502B 002Ch
2Eh	16	FSI_RX_CFG_RX_PING_TAG	5029 002Eh	5029 102Eh	502B 002Eh
30h	32	FSI_RX_CFG_RX_PING_WD_REF	5029 0030h	5029 1030h	502B 0030h
34h	32	FSI_RX_CFG_RX_PING_WD_CNT	5029 0034h	5029 1034h	502B 0034h
38h	16	FSI_RX_CFG_RX_INT1_CTRL_ALT1	5029 0038h	5029 1038h	502B 0038h
3Ah	16	FSI_RX_CFG_RX_INT2_CTRL_ALT1	5029 003Ah	5029 103Ah	502B 003Ah
3Ch	16	FSI_RX_CFG_RX_LOCK_CTRL	5029 003Ch	5029 103Ch	502B 003Ch
40h	32	FSI_RX_CFG_RX_ECC_DATA	5029 0040h	5029 1040h	502B 0040h
44h	16	FSI_RX_CFG_RX_ECC_VAL	5029 0044h	5029 1044h	502B 0044h
48h	32	FSI_RX_CFG_RX_ECC_SEC_DATA	5029 0048h	5029 1048h	502B 0048h
4Ch	16	FSI_RX_CFG_RX_ECC_LOG	5029 004Ch	5029 104Ch	502B 004Ch
50h	16	FSI_RX_CFG_RX_FRAME_TAG_CMP	5029 0050h	5029 1050h	502B 0050h
52h	16	FSI_RX_CFG_RX_PING_TAG_CMP	5029 0052h	5029 1052h	502B 0052h
58h	32	FSI_RX_CFG_RX_TRIG_CTRL_0	5029 0058h	5029 1058h	502B 0058h

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Table 3-847. FSI_RX_CFG Registers, Base Address=5029 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSI_RX0 Physical Address	FSI_RX1 Physical Address	FSI_RX2 Physical Address
5Ch	32	FSI_RX_CFG_RX_TRIG_WIDTH_0	5029 005Ch	5029 105Ch	502B 005Ch
60h	16	FSI_RX_CFG_RX_DLYLINE_CTRL	5029 0060h	5029 1060h	502B 0060h
64h	32	FSI_RX_CFG_RX_TRIG_CTRL_1	5029 0064h	5029 1064h	502B 0064h
68h	32	FSI_RX_CFG_RX_TRIG_CTRL_2	5029 0068h	5029 1068h	502B 0068h
6Ch	32	FSI_RX_CFG_RX_TRIG_CTRL_3	5029 006Ch	5029 106Ch	502B 006Ch
70h	32	FSI_RX_CFG_RX_VIS_1	5029 0070h	5029 1070h	502B 0070h
74h	16	FSI_RX_CFG_RX_UDATA_FILTER	5029 0074h	5029 1074h	502B 0074h
80h	16	FSI_RX_CFG_RX_BUF_BASE_J	5029 0080h + formula	5029 1080h + formula	502B 0080h + formula

Table 3-848. FSI_RX_CFG Registers, Base Address=5029 0000h, Length=4096

Offset	Length	Register Name	FSI_RX3 Physical Address
0h	16	FSI_RX_CFG_RX_MASTER_CTRL_ALTC	502B 1000h
8h	16	FSI_RX_CFG_RX_OPER_CTRL	502B 1008h
Ch	16	FSI_RX_CFG_RX_FRAME_INFO	502B 100Ch
Eh	16	FSI_RX_CFG_RX_FRAME_TAG_UDATA	502B 100Eh
10h	16	FSI_RX_CFG_RX_DMA_CTRL	502B 1010h
14h	16	FSI_RX_CFG_RX_EVT_STS_ALT1	502B 1014h
16h	16	FSI_RX_CFG_RX_CRC_INFO	502B 1016h
18h	16	FSI_RX_CFG_RX_EVT_CLR_ALT1	502B 1018h
1Ah	16	FSI_RX_CFG_RX_EVT_FRC_ALT1	502B 101Ah
1Ch	16	FSI_RX_CFG_RX_BUF_PTR_LOAD	502B 101Ch
1Eh	16	FSI_RX_CFG_RX_BUF_PTR_STS	502B 101Eh
20h	16	FSI_RX_CFG_RX_FRAME_WD_CTRL	502B 1020h
24h	32	FSI_RX_CFG_RX_FRAME_WD_REF	502B 1024h
28h	32	FSI_RX_CFG_RX_FRAME_WD_CNT	502B 1028h
2Ch	16	FSI_RX_CFG_RX_PING_WD_CTRL	502B 102Ch
2Eh	16	FSI_RX_CFG_RX_PING_TAG	502B 102Eh
30h	32	FSI_RX_CFG_RX_PING_WD_REF	502B 1030h
34h	32	FSI_RX_CFG_RX_PING_WD_CNT	502B 1034h
38h	16	FSI_RX_CFG_RX_INT1_CTRL_ALT1	502B 1038h
3Ah	16	FSI_RX_CFG_RX_INT2_CTRL_ALT1	502B 103Ah
3Ch	16	FSI_RX_CFG_RX_LOCK_CTRL	502B 103Ch
40h	32	FSI_RX_CFG_RX_ECC_DATA	502B 1040h
44h	16	FSI_RX_CFG_RX_ECC_VAL	502B 1044h
48h	32	FSI_RX_CFG_RX_ECC_SEC_DATA	502B 1048h
4Ch	16	FSI_RX_CFG_RX_ECC_LOG	502B 104Ch
50h	16	FSI_RX_CFG_RX_FRAME_TAG_CMP	502B 1050h
52h	16	FSI_RX_CFG_RX_PING_TAG_CMP	502B 1052h
58h	32	FSI_RX_CFG_RX_TRIG_CTRL_0	502B 1058h
5Ch	32	FSI_RX_CFG_RX_TRIG_WIDTH_0	502B 105Ch
60h	16	FSI_RX_CFG_RX_DLYLINE_CTRL	502B 1060h
64h	32	FSI_RX_CFG_RX_TRIG_CTRL_1	502B 1064h
68h	32	FSI_RX_CFG_RX_TRIG_CTRL_2	502B 1068h
6Ch	32	FSI_RX_CFG_RX_TRIG_CTRL_3	502B 106Ch

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Table 3-848. FSI_RX_CFG Registers, Base Address=5029 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSI_RX3 Physical Address
70h	32	FSI_RX_CFG_RX_VIS_1	502B 1070h
74h	16	FSI_RX_CFG_RX_UDATA_FILTER	502B 1074h
80h	16	FSI_RX_CFG_RX_BUF_BASE_J	502B 1080h + formula

3.11.2 FSI_RX Registers

FSI_RX Registers

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3.11.2.1 FSI_RX_CFG_RX_MASTER_CTRL_ALTC Register

3.11.2.1.1 FSI_RX_CFG_RX_MASTER_CTRL_ALTC Register (Offset = 0h) [reset = 0h]

Receive master control register.

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Table 3-849. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0000h
FSI_RX1	5029 1000h
FSI_RX2	502B 0000h
FSI_RX3	502B 1000h

Figure 3-474. FSI_RX_CFG_RX_MASTER_CTRL_ALTC Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							

7	6	5	4	3	2	1	0
RESERVED_1			DATA_FILTER_EN	INPUT_ISOLATE	SPI_PAIRING	INT_LOOPBACK	CORE_RST
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 3-850. FSI_RX_CFG_RX_MASTER_CTRL_ALTC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register.
7:5	RESERVED_1	R	0h	Reserved
4	DATA_FILTER_EN	R/W	0h	Data Filter Enable Bit. 0h[R/W] = Data filtering is disabled. 1h[R/W] = Data filtering is enabled.
3	INPUT_ISOLATE	R/W	0h	When set to 1, the FSI RX inputs [RXCLK, RXD0 and RXD1] will be isolated from what is driven from the device pins and will be held at inactive level of '1'.This isolation facilitates the user to switch the RX inputs to a different set of device pins and hence any potential glitch that could occur during the process of switching will not effect the RX module itself.
2	SPI_PAIRING	R/W	0h	Clock Pairing for SPI-like Behavior Enable bit This bit enables the internal clock pairing with the FSI TX module. This feature internally connects the TXCLK to RXCLK allowing the FSI TX module, acting as a SPI master, to clock data into the receiver and out of the transmitter like a standard SPI module. This configuration is valid when the Module is in SPI mode only [RX_OPER_CTRL.SPI_MODE = 1] 0h[R/W] = SPI clock pairing is not enabled. 1h[R/W] = SPI clock pairing is enabled. The RXCLK will be internally connected to the TXCLK of the corresponding FSI module. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

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Table 3-850. FSI_RX_CFG_RX_MASTER_CTRL_ALTC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT_LOOPBACK	R/W	0h	Internal Loopback Enable bit This bit enables the internal loopback functionality of the FSI receiver. By enabling this bit, a mux will select the signals coming directly from the corresponding FSI transmitter module rather than from the pins. 0h[R/W] = Internal loopback is disabled. The FSI RX module will receive signals coming from the pins. 1h[R/W] = Internal loopback is enabled. The FSI RX module will receive signals from the directly from FSI TX module rather than the pins. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.
0	CORE_RST	R/W	0h	Receiver Controller Core Reset bit This bit controls the receiver master core reset. In order to receive any frame, this bit must be cleared. Note: For reset to take affect, the FSI RX module must be held in reset for at least 4 SYSCLK cycles. 0h[R/W] = Receiver core is not in reset and can receive frames. 1h[R/W] = Receiver core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

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3.11.2.2 FSI_RX_CFG_RX_OPER_CTRL Register

3.11.2.2.1 FSI_RX_CFG_RX_OPER_CTRL Register (Offset = 8h) [reset = 0h]

Receive operation control register.

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Table 3-851. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0008h
FSI_RX1	5029 1008h
FSI_RX2	502B 0008h
FSI_RX3	502B 1008h

Figure 3-475. FSI_RX_CFG_RX_OPER_CTRL Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RESERVED_1</td><td>PING_WD_RST_MODE</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>ECC_SEL</td><td colspan="4">N_WORDS</td><td>SPI_MODE</td><td colspan="2">DATA_WIDTH</td></tr>
<tr><td>R/W</td><td colspan="4">R/W</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td>0h</td><td colspan="4">0h</td><td>0h</td><td colspan="2">0h</td></tr>
</table>

Table 3-852. FSI_RX_CFG_RX_OPER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_1	R	0h	Reserved
8	PING_WD_RST_MODE	R/W	0h	Ping Watchdog Timeout Mode Select bit This bit selects the mode by which the ping watchdog counter is reset. The watchdog counter can be reset and restarted only by ping frames or by any received frame. 0h[R/W] = The ping watchdog counter will reset and restart only by ping frames. 1h[R/W] = The ping watchdog counter will reset and restart by any received frame.
7	ECC_SEL	R/W	0h	ECC Data Width Select bit This bit selects between whether the ECC computation is done on 16-bit or 32-bit words. 0h[R/W] = 32-bit ECC is used. 1h[R/W] = 16-bit ECC is used.
6:3	N_WORDS	R/W	0h	Number of Words to Receive This field defines the number of words which will be received in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the transmitter. Set this bitfield to be one less than the number of words to be received. This value is only applicable when the frame type received is DATA_N_WORD. 0h[R/W] = 1 data word frame [16-bit data]. 1h[R/W] = 2 data word frame [32-bit data]. .. Fh [R/W] = 16 data word frame [256-bit data].
2	SPI_MODE	R/W	0h	SPI Mode Enable bit This bit enables and disables the SPI compatibility mode of the FSI RX. The received data must be formatted as an FSI frame in order for the data to properly be received. SPI compatibility mode will allow FSI RX to receive data that is sent using SPI signal format. Refer to the applicable section in the FSI TRM chapter for more information. 0h[R/W] = FSI is in normal mode of operation. 1h[R/W] = FSI is operating in SPI compatibility mode.

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Table 3-852. FSI_RX_CFG_RX_OPER_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	DATA_WIDTH	R/W	0h	Receive Data Width Select bit These bits decide the number of data lines used for receiving data. 0h[R/W] = Data will be received on one data line, RXD0. 1h[R/W] = Data will be received on two data lines, RXD0 and RXD1. 2h 3h[R/W] = Reserved

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3.11.2.3 FSI_RX_CFG_RX_FRAME_INFO Register

3.11.2.3.1 FSI_RX_CFG_RX_FRAME_INFO Register (Offset = Ch) [reset = 0h]

Receive frame control register.

Return to Summary Table

Table 3-853. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 000Ch
FSI_RX1	5029 100Ch
FSI_RX2	502B 000Ch
FSI_RX3	502B 100Ch

Figure 3-476. FSI_RX_CFG_RX_FRAME_INFO Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				FRAME_TYPE			
R				R			
0h				0h			

Table 3-854. FSI_RX_CFG_RX_FRAME_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3:0	FRAME_TYPE	R	0h	Received Frame Type This field indicates the type of frame that was successfully received last. 0000b[R/W] = A ping frame was received 0100b[R/W] = A DATA_1_WORD frame was received [16-bit data]. 0101b[R/W] = A DATA_2_WORD frame was received [32-bit data]. 0110b[R/W] = A DATA_4_WORD frame was received [64-bit data]. 0111b[R/W] = A DATA_6_WORD frame was received [96-bit data]. 0011b[R/W] = A DATA_N_WORD frame was received. The N_WORD field will determine the number of words [1 to 16] to be sent. The number of words received must equal the value programmed in RX_OPER_CTRL.N_WORDS. 1111b[R/W] = An error frame was received. This frame can be used during error conditions or any condition where the transmitter wants to signal the receiver for attention. However, the user software is at liberty to use this for any purpose. 0001b 0010b and 1000bthrough 1110bare Reserved and should not be used.

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3.11.2.4 FSI_RX_CFG_RX_FRAME_TAG_UDATA Register

3.11.2.4.1 FSI_RX_CFG_RX_FRAME_TAG_UDATA Register (Offset = Eh) [reset = 0h]

Receive frame tag and user data register.

Return to Summary Table

Table 3-855. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 000Eh
FSI_RX1	5029 100Eh
FSI_RX2	502B 000Eh
FSI_RX3	502B 100Eh

Figure 3-477. FSI_RX_CFG_RX_FRAME_TAG_UDATA Name Register

15	14	13	12	11	10	9	8
USER_DATA							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1			FRAME_TAG				ZERO
R			R				R
0h			0h				0h

Table 3-856. FSI_RX_CFG_RX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	USER_DATA	R	0h	Received User Data This field contains the 8-bit user data field of the last successfully received frame.
7:5	RESERVED_1	R	0h	Reserved
4:1	FRAME_TAG	R	0h	Received Frame Tag This field contains the 4-bit frame tag from the last successfully received frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag.
0	ZERO	R	0h	Zero bit This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the FRAME_TAG and ZERO bits of this register [bits 4:0], application software can directly index into an array of 32-bit data.

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3.11.2.5 FSI_RX_CFG_RX_DMA_CTRL Register

3.11.2.5.1 FSI_RX_CFG_RX_DMA_CTRL Register (Offset = 10h) [reset = 0h]

Receive DMA event control register.

Return to Summary Table

Table 3-857. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0010h
FSI_RX1	5029 1010h
FSI_RX2	502B 0010h
FSI_RX3	502B 1010h

Figure 3-478. FSI_RX_CFG_RX_DMA_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							DMA_EVT_EN
R							R/W
0h							0h

Table 3-858. FSI_RX_CFG_RX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	DMA_EVT_EN	R/W	0h	DMA Event Enable bit This bit will enable a DMA Event to be generated upon the completion of a frame reception. 0h[R/W] = A DMA event will not be generated. 1h[R/W] = A DMA event will be generated upon the reception of a frame. Note: The DMA event will only be generated for data frames.

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3.11.2.6 FSI_RX_CFG_RX_EVT_STS_ALT1 Register

3.11.2.6.1 FSI_RX_CFG_RX_EVT_STS_ALT1 Register (Offset = 14h) [reset = 0h]

Receive event and error status flag register.

Return to Summary Table

Table 3-859. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0014h
FSI_RX1	5029 1014h
FSI_RX2	502B 0014h
FSI_RX3	502B 1014h

Figure 3-479. FSI_RX_CFG_RX_EVT_STS_ALT1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-860. FSI_RX_CFG_RX_EVT_STS_ALT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	ERROR_TAG_MATCH	R	0h	Error Tag Match Flag This bit indicates that an error frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = No tag-matched error frame received. 1h[R] = A tag-matched error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
13	DATA_TAG_MATCH	R	0h	Data Tag Match Flag This bit indicates that a dataframe was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = No tag-matched data frame received. 1h[R] = A tag-matched data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
12	PING_TAG_MATCH	R	0h	Ping Tag Match Flag This bit indicates that a ping frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = No tag-matched ping frame received. 1h[R] = A tag-matched ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.

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Table 3-860. FSI_RX_CFG_RX_EVT_STS_ALT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	DATA_FRAME	R	0h	Data Frame Received Flag This bit indicates that an data frame has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = No data frame has been received. 1h[R] = A data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
10	FRAME_OVERRUN	R	0h	Frame Overrun Flag This bit indicates that a frame overrun condition has occured. This bit gets set to 1 when a new DATA/ERROR frame is received and the corresponding DATA_FRAME_RCVD/ERROR_FRAME_RCVD flag is still set to 1. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = Frame overrun has not ocurred. 1h[R] = Frame overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
9	PING_FRAME	R	0h	Ping Frame Received Flag This bit indicates that an ping frame has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = No ping frame has been received. 1h[R] = A ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
8	ERR_FRAME	R	0h	Error Frame Received Flag This bit indicates that an error frame has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = No error frame has been received. 1h[R] = An error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
7	BUF_UNDERRUN	R	0h	Receive Buffer Underrun Flag This bit indicates that a buffer underrun condition has occured in the receive buffer. This will happen when software reads the buffer which is empty and has no valid data. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = Receive Buffer Underrun has not ocurred. 1h[R] = Receive Buffer Underrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
6	FRAME_DONE	R	0h	Frame Done Flag This bit indicates that a frame has been successfully received without error. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = No frame has been successfully received. 1h[R] = A frame has been successfully received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
5	BUF_OVERRUN	R	0h	Receive Buffer Overrun Flag This bit indicates that a buffer overrun condition has occured in the receive buffer. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = Receive buffer overrun has not ocurred. 1h[R] = Receive buffer overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.

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Table 3-860. FSI_RX_CFG_RX_EVT_STS_ALT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	EOF_ERR	R	0h	End-of-Frame Error Flag This bit indicates that an invalid end-of-frame bit pattern has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = Invalid end-of-frame has not been received. 1h[R] = Invalid end-of-frame has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
3	TYPE_ERR	R	0h	Frame Type Error Flag This bit inditcates that an invalid frame type has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = Invalid frame type has not been received. 1h[R] = Invalid frame type has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
2	CRC_ERR	R	0h	CRC Error Flag This bit indicates that a CRC error has occured. A CRC error will be generated on a data frame where the received CRC and the computed CRC do not match. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = CRC error has not occured. 1h[R] = CRC error has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
1	FRAME_WD_TO	R	0h	Frame Watchdog Timeout Flag This bit indicates that the frame watchdog timer has timed out. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = Frame watchdog timeout has not occured. 1h[R] = Frame watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
0	PING_WD_TO	R	0h	Ping Watchdog Timeout Flag This bit indicates that the ping watchdog timer has timed out. Software can also force this bit to get set by Writing to the RX_EVT_FRC register. 0h[R] = Ping watchdog timeout has not occured. 1h[R] = Ping watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.

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3.11.2.7 FSI_RX_CFG_RX_CRC_INFO Register

3.11.2.7.1 FSI_RX_CFG_RX_CRC_INFO Register (Offset = 16h) [reset = 0h]

Receive CRC info of received and computed CRC.

Return to Summary Table

Table 3-861. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0016h
FSI_RX1	5029 1016h
FSI_RX2	502B 0016h
FSI_RX3	502B 1016h

Figure 3-480. FSI_RX_CFG_RX_CRC_INFO Name Register

15	14	13	12	11	10	9	8
CALC_CRC							
R							
0h							
7	6	5	4	3	2	1	0
RX_CRC							
R							
0h							

Table 3-862. FSI_RX_CFG_RX_CRC_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	CALC_CRC	R	0h	Harware Calculated CRC Value This bitfield contains the CRC value that was calculated on the last received data. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames.
7:0	RX_CRC	R	0h	Received CRC Value This bitfield contains the CRC value that was last received a frame. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames.

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3.11.2.8 FSI_RX_CFG_RX_EVT_CLR_ALT1 Register

3.11.2.8.1 FSI_RX_CFG_RX_EVT_CLR_ALT1 Register (Offset = 18h) [reset = 0h]

Receive event and error clear register.

Return to Summary Table

Table 3-863. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0018h
FSI_RX1	5029 1018h
FSI_RX2	502B 0018h
FSI_RX3	502B 1018h

Figure 3-481. FSI_RX_CFG_RX_EVT_CLR_ALT1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-864. FSI_RX_CFG_RX_EVT_CLR_ALT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	ERROR_TAG_MATCH	W	0h	Error Tag Match Glag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
13	DATA_TAG_MATCH	W	0h	Data Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
12	PING_TAG_MATCH	W	0h	Ping Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
11	DATA_FRAME	W	0h	Data Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
10	FRAME_OVERRUN	W	0h	Frame Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
9	PING_FRAME	W	0h	Ping Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.

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Table 3-864. FSI_RX_CFG_RX_EVT_CLR_ALT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ERR_FRAME	W	0h	Error Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
7	BUF_UNDERRUN	W	0h	Receive Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[R/W] = Writing a 0 to this bit will have no effect. 1h[R/W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
6	FRAME_DONE	W	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
5	BUF_OVERRUN	W	0h	Receive Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
4	EOF_ERR	W	0h	End-of-Frame Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
3	TYPE_ERR	W	0h	Frame Type Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
2	CRC_ERR	W	0h	CRC Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
1	FRAME_WD_TO	W	0h	Frame Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
0	PING_WD_TO	W	0h	Ping Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.

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3.11.2.9 FSI_RX_CFG_RX_EVT_FRC_ALT1 Register

3.11.2.9.1 FSI_RX_CFG_RX_EVT_FRC_ALT1 Register (Offset = 1Ah) [reset = 0h]

Receive event and error flag force register.

Return to Summary Table

Table 3-865. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 001Ah
FSI_RX1	5029 101Ah
FSI_RX2	502B 001Ah
FSI_RX3	502B 101Ah

Figure 3-482. FSI_RX_CFG_RX_EVT_FRC_ALT1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	ERROR_TAG_MATCH	DATA_TAG_MATCH	PING_TAG_MATCH	DATA_FRAME	FRAME_OVERRUN	PING_FRAME	ERR_FRAME
R	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BUF_UNDERRUN	FRAME_DONE	BUF_OVERRUN	EOF_ERR	TYPE_ERR	CRC_ERR	FRAME_WD_TO	PING_WD_TO
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-866. FSI_RX_CFG_RX_EVT_FRC_ALT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	ERROR_TAG_MATCH	W	0h	Error Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
13	DATA_TAG_MATCH	W	0h	Data Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
12	PING_TAG_MATCH	W	0h	Ping Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
11	DATA_FRAME	W	0h	Data Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
10	FRAME_OVERRUN	W	0h	Frame Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.

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Table 3-866. FSI_RX_CFG_RX_EVT_FRC_ALT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PING_FRAME	W	0h	Ping Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
8	ERR_FRAME	W	0h	Error Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
7	BUF_UNDERRUN	W	0h	Receive Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
6	FRAME_DONE	W	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
5	BUF_OVERRUN	W	0h	Receive Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
4	EOF_ERR	W	0h	End-of-Frame Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
3	TYPE_ERR	W	0h	Frame Type Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
2	CRC_ERR	W	0h	CRC Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
1	FRAME_WD_TO	W	0h	Frame Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.
0	PING_WD_TO	W	0h	Ping Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding bit in the RX_EVT_STS Register.

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3.11.2.10 FSI_RX_CFG_RX_BUF_PTR_LOAD Register

3.11.2.10.1 FSI_RX_CFG_RX_BUF_PTR_LOAD Register (Offset = 1Ch) [reset = 0h]

Receive buffer pointer load register.

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Table 3-867. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 001Ch
FSI_RX1	5029 101Ch
FSI_RX2	502B 001Ch
FSI_RX3	502B 101Ch

Figure 3-483. FSI_RX_CFG_RX_BUF_PTR_LOAD Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				BUF_PTR_LOAD			
R				R/W			
0h				0h			

Table 3-868. FSI_RX_CFG_RX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3:0	BUF_PTR_LOAD	R/W	0h	Buffer Pointer Load. This is the value to be loaded into the receive word pointer when written. This is to allow software to force the receiver to start storing the received data starting at a specific location in the buffer. NOTE: The value of the CURR_BUF_PTR in the RX_BUF_PTR_STS will not get reflected immediately. This will take effect only when there is a valid receive operation with incoming clocks after [3 RXCLK + 3 SYCLK] cycles.

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3.11.2.11 FSI_RX_CFG_RX_BUF_PTR_STS Register

3.11.2.11.1 FSI_RX_CFG_RX_BUF_PTR_STS Register (Offset = 1Eh) [reset = 0h]

Receive buffer pointer status register.

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Table 3-869. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 001Eh
FSI_RX1	5029 101Eh
FSI_RX2	502B 001Eh
FSI_RX3	502B 101Eh

Figure 3-484. FSI_RX_CFG_RX_BUF_PTR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED_2			CURR_WORD_CNT				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED_1				CURR_BUF_PTR			
R				R			
0h				0h			

Table 3-870. FSI_RX_CFG_RX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12:8	CURR_WORD_CNT	R	0h	Words Available in the Receive Buffer This bitfield indicates the number of valid data words present in the receive buffer that have not been read by the application software. This bitfield is only valid when there is no active transfer. Note: This value will not be valid if there has been a buffer overrun or underrun condition.
7:4	RESERVED_1	R	0h	Reserved
3:0	CURR_BUF_PTR	R	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission.

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3.11.2.12 FSI_RX_CFG_RX_FRAME_WD_CTRL Register

3.11.2.12.1 FSI_RX_CFG_RX_FRAME_WD_CTRL Register (Offset = 20h) [reset = 0h]

Receive frame watchdog control register.

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Table 3-871. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0020h
FSI_RX1	5029 1020h
FSI_RX2	502B 0020h
FSI_RX3	502B 1020h

Figure 3-485. FSI_RX_CFG_RX_FRAME_WD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						FRAME_WD_EN	FRAME_WD_CNT_RST
R						R/W	R/W
0h						0h	0h

Table 3-872. FSI_RX_CFG_RX_FRAME_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED_1	R	0h	Reserved
1	FRAME_WD_EN	R/W	0h	Frame Watchdog Counter Enable bit This bit will enable or disable the frame watchdog counter. The counter [RX_FRAME_WD_CNT] will begin counting from 0 when a valid start-of-frame pattern is received. When the reference value [RX_FRAME_WD_REF] is reached, it will generate a frame watchdog timeout event [RX_EVT_STS.FRAME_WD_TO] and the counter value will reset to 0 and continue counting on the next valid start-of-frame. 0h[R/W] = The frame watchdog counter is disabled and not running. 1h[R/W] = The frame watchdog counter logic is enabled and running.
0	FRAME_WD_CNT_RST	R/W	0h	Frame Watchdog Counter Reset bit This bit will reset the frame watchdog counter to 0. Writing a 1 to this bit will reset the frame watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h[R/W] = Clear the FRAME_WD_CNT_RST. 1h[W] = The frame watchdog counter will be reset to 0.

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3.11.2.13 FSI_RX_CFG_RX_FRAME_WD_REF Register

3.11.2.13.1 FSI_RX_CFG_RX_FRAME_WD_REF Register (Offset = 24h) [reset = 0h]

Receive frame watchdog counter reference.

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Table 3-873. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0024h
FSI_RX1	5029 1024h
FSI_RX2	502B 0024h
FSI_RX3	502B 1024h

Figure 3-486. FSI_RX_CFG_RX_FRAME_WD_REF Name Register

31	30	29	28	27	26	25	24
FRAME_WD_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
FRAME_WD_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
FRAME_WD_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
FRAME_WD_REF							
R/W							
0h							

Table 3-874. FSI_RX_CFG_RX_FRAME_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRAME_WD_REF	R/W	0h	Frame Watchdog Counter Reference Value This is the 32-bit reference value for the frame watchdog timeout counter. The counter will count up starting from 0 at a valid start-of-frame pattern and continue counting until this value is reached.

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3.11.2.14 FSI_RX_CFG_RX_FRAME_WD_CNT Register

3.11.2.14.1 FSI_RX_CFG_RX_FRAME_WD_CNT Register (Offset = 28h) [reset = 0h]

Receive frame watchdog current count.

Return to Summary Table

Table 3-875. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0028h
FSI_RX1	5029 1028h
FSI_RX2	502B 0028h
FSI_RX3	502B 1028h

Figure 3-487. FSI_RX_CFG_RX_FRAME_WD_CNT Name Register

31	30	29	28	27	26	25	24
FRAME_WD_CNT							
R							
0h							
23	22	21	20	19	18	17	16
FRAME_WD_CNT							
R							
0h							
15	14	13	12	11	10	9	8
FRAME_WD_CNT							
R							
0h							
7	6	5	4	3	2	1	0
FRAME_WD_CNT							
R							
0h							

Table 3-876. FSI_RX_CFG_RX_FRAME_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRAME_WD_CNT	R	0h	Frame Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the frame watchdog counter. This counter is reset to 0 in a variety of ways: A write to FRME_WD_CNT_RST, a match with FRAME_WD_REF, or the reception of a successful data frame.

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3.11.2.15 FSI_RX_CFG_RX_PING_WD_CTRL Register

3.11.2.15.1 FSI_RX_CFG_RX_PING_WD_CTRL Register (Offset = 2Ch) [reset = 0h]

Receive ping watchdog control register.

Return to Summary Table

Table 3-877. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 002Ch
FSI_RX1	5029 102Ch
FSI_RX2	502B 002Ch
FSI_RX3	502B 102Ch

Figure 3-488. FSI_RX_CFG_RX_PING_WD_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						PING_WD_EN	PING_WD_RST
R						R/W	R/W
0h						0h	0h

Table 3-878. FSI_RX_CFG_RX_PING_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED_1	R	0h	Reserved
1	PING_WD_EN	R/W	0h	Ping Watchdog Counter Enable bit This bit will enable or disable the ping watchdog counter. The counter [RX_PING_WD_CNT] will begin counting from 0 when it is enabled. When the reference value [RX_PING_WD_REF] is reached, it will generate a ping watchdog timeout event [RX_EVT_STS.PING_WD_TO] and the counter value will reset to 0, and resume counting 0h[R/W] = The ping watchdog counter is disabled and not running. 1h[R/W] = The ping watchdog counter logic is enabled and running.
0	PING_WD_RST	R/W	0h	Ping Watchdog Counter Reset bit This bit will reset the ping watchdog counter to 0. Writing a 1 to this bit will reset the ping watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h[R/W] = Clear the PING_WD_RST. 1h[W] = The ping watchdog counter will be reset to 0.

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3.11.2.16 FSI_RX_CFG_RX_PING_TAG Register

3.11.2.16.1 FSI_RX_CFG_RX_PING_TAG Register (Offset = 2Eh) [reset = 0h]

Receive ping tag register.

Return to Summary Table

Table 3-879. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 002Eh
FSI_RX1	5029 102Eh
FSI_RX2	502B 002Eh
FSI_RX3	502B 102Eh

Figure 3-489. FSI_RX_CFG_RX_PING_TAG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			PING_TAG				ZERO
R			R				R
0h			0h				0h

Table 3-880. FSI_RX_CFG_RX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_1	R	0h	Reserved
4:1	PING_TAG	R	0h	Received Ping Frame Tag This field contains the 4-bit frame tag from the last successfully received ping frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag.
0	ZERO	R	0h	Zero bit This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the PING_TAG and ZERO bits of this register [bits 4:0], application software can directly index into an array of 32-bit data.

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3.11.2.17 FSI_RX_CFG_RX_PING_WD_REF Register

3.11.2.17.1 FSI_RX_CFG_RX_PING_WD_REF Register (Offset = 30h) [reset = 0h]

Receive ping watchdog counter reference.

Return to Summary Table

Table 3-881. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0030h
FSI_RX1	5029 1030h
FSI_RX2	502B 0030h
FSI_RX3	502B 1030h

Figure 3-490. FSI_RX_CFG_RX_PING_WD_REF Name Register

31	30	29	28	27	26	25	24
PING_WD_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
PING_WD_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
PING_WD_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
PING_WD_REF							
R/W							
0h							

Table 3-882. FSI_RX_CFG_RX_PING_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PING_WD_REF	R/W	0h	Ping Watchdog Counter Reference Value This is the 32-bit reference value for the ping watchdog timeout counter. The counter will count up starting from 0 and continue counting until this value is reached.

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3.11.2.18 FSI_RX_CFG_RX_PING_WD_CNT Register

3.11.2.18.1 FSI_RX_CFG_RX_PING_WD_CNT Register (Offset = 34h) [reset = 0h]

Receive pingwatchdog current count.

Return to Summary Table

Table 3-883. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0034h
FSI_RX1	5029 1034h
FSI_RX2	502B 0034h
FSI_RX3	502B 1034h

Figure 3-491. FSI_RX_CFG_RX_PING_WD_CNT Name Register

31	30	29	28	27	26	25	24
PING_WD_CNT							
R							
0h							
23	22	21	20	19	18	17	16
PING_WD_CNT							
R							
0h							
15	14	13	12	11	10	9	8
PING_WD_CNT							
R							
0h							
7	6	5	4	3	2	1	0
PING_WD_CNT							
R							
0h							

Table 3-884. FSI_RX_CFG_RX_PING_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PING_WD_CNT	R	0h	Ping Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the ping watchdog counter. This counter is reset to 0 in a variety of ways: A write to PING_WD_RST, a match with PING_WD_REF, or the reception of a ping frame.

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3.11.2.19 FSI_RX_CFG_RX_INT1_CTRL_ALT1 Register

3.11.2.19.1 FSI_RX_CFG_RX_INT1_CTRL_ALT1 Register (Offset = 38h) [reset = 0h]

Receive interrupt control register for RX_INT1.

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Table 3-885. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0038h
FSI_RX1	5029 1038h
FSI_RX2	502B 0038h
FSI_RX3	502B 1038h

Figure 3-492. FSI_RX_CFG_RX_INT1_CTRL_ALT1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	INT1_EN_ERROR_TAG_MATCH	INT1_EN_DATA_TAG_MATCH	INT1_EN_PING_TAG_MATCH	INT1_EN_DATA_FRAME	INT1_EN_FRAME_OVERRUN	INT1_EN_PING_FRAME	INT1_EN_ERR_FRAME
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INT1_EN_UNDERRUN	INT1_EN_FRAME_DONE	INT1_EN_OVERRUN	INT1_EN_EOF_ERR	INT1_EN_TYPE_ERR	INT1_EN_CRC_ERR	INT1_EN_FRAME_WD_TO	INT1_EN_PING_WD_TO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-886. FSI_RX_CFG_RX_INT1_CTRL_ALT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	INT1_EN_ERROR_TAG_MATCH	R/W	0h	Enable Error Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = An error frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
13	INT1_EN_DATA_TAG_MATCH	R/W	0h	Enable Data Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A data frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
12	INT1_EN_PING_TAG_MATCH	R/W	0h	Enable Ping Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A ping frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
11	INT1_EN_DATA_FRAME	R/W	0h	Enable Data Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A data frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

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Table 3-886. FSI_RX_CFG_RX_INT1_CTRL_ALT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INT1_EN_FRAME_OVERRUN	R/W	0h	Enable Frame Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A frame overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
9	INT1_EN_PING_FRAME	R/W	0h	Enable Ping Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A ping frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
8	INT1_EN_ERR_FRAME	R/W	0h	Enable ERROR Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A error frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
7	INT1_EN_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A buffer underrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
6	INT1_EN_FRAME_DONE	R/W	0h	Enable Frame Done Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A frame done event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
5	INT1_EN_OVERRUN	R/W	0h	Enable Receive Buffer Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A receive buffer overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
4	INT1_EN_EOF_ERR	R/W	0h	Enable End-of-Frame Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = An end-of-frame error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
3	INT1_EN_TYPE_ERR	R/W	0h	Enable Frame Type Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A frame type error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
2	INT1_EN_CRC_ERR	R/W	0h	Enable CRC Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A CRC error will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

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Table 3-886. FSI_RX_CFG_RX_INT1_CTRL_ALT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT1_EN_FRAME_WD_TO	R/W	0h	Enable Frame Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A frame watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
0	INT1_EN_PING_WD_TO	R/W	0h	Enable Ping Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT1. 1h[R/W] = A ping watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

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3.11.2.20 FSI_RX_CFG_RX_INT2_CTRL_ALT1 Register

3.11.2.20.1 FSI_RX_CFG_RX_INT2_CTRL_ALT1 Register (Offset = 3Ah) [reset = 0h]

Receive interrupt control register for RX_INT2.

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Table 3-887. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 003Ah
FSI_RX1	5029 103Ah
FSI_RX2	502B 003Ah
FSI_RX3	502B 103Ah

Figure 3-493. FSI_RX_CFG_RX_INT2_CTRL_ALT1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	INT2_EN_ERROR_TAG_MATCH	INT2_EN_DATA_TAG_MATCH	INT2_EN_PING_TAG_MATCH	INT2_EN_DATA_FRAME	INT2_EN_FRAME_OVERRUN	INT2_EN_PING_FRAME	INT2_EN_ERR_FRAME
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INT2_EN_UNDERRUN	INT2_EN_FRAME_DONE	INT2_EN_OVERRUN	INT2_EN_EOF_ERR	INT2_EN_TYPE_ERR	INT2_EN_CRC_ERR	INT2_EN_FRAME_WD_TO	INT2_EN_PING_WD_TO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-888. FSI_RX_CFG_RX_INT2_CTRL_ALT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14	INT2_EN_ERROR_TAG_MATCH	R/W	0h	Enable Error Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = An error frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
13	INT2_EN_DATA_TAG_MATCH	R/W	0h	Enable Data Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A data frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
12	INT2_EN_PING_TAG_MATCH	R/W	0h	Enable Ping Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A ping frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
11	INT2_EN_DATA_FRAME	R/W	0h	Enable Data Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A data frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

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Table 3-888. FSI_RX_CFG_RX_INT2_CTRL_ALT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	INT2_EN_FRAME_OVERRUN	R/W	0h	Enable Frame Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A frame overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
9	INT2_EN_PING_FRAME	R/W	0h	Enable Ping Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A ping frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
8	INT2_EN_ERR_FRAME	R/W	0h	Enable Error Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A error frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
7	INT2_EN_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A buffer underrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
6	INT2_EN_FRAME_DONE	R/W	0h	Enable Frame Done Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A frame done event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
5	INT2_EN_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A buffer overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
4	INT2_EN_EOF_ERR	R/W	0h	Enable End-of-Frame Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = An end-of-frame error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
3	INT2_EN_TYPE_ERR	R/W	0h	Enable Frame Type Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A frame type error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
2	INT2_EN_CRC_ERR	R/W	0h	Enable CRC Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A CRC error will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

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Table 3-888. FSI_RX_CFG_RX_INT2_CTRL_ALT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT2_EN_FRAME_WD_TO	R/W	0h	Enable Frame Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A frame watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
0	INT2_EN_PING_WD_TO	R/W	0h	Enable Ping Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event. 0h[R/W] = This event will not trigger an interrupt on RX_INT2. 1h[R/W] = A ping watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

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3.11.2.21 FSI_RX_CFG_RX_LOCK_CTRL Register

3.11.2.21.1 FSI_RX_CFG_RX_LOCK_CTRL Register (Offset = 3Ch) [reset = 0h]

Receive lock control register.

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Table 3-889. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 003Ch
FSI_RX1	5029 103Ch
FSI_RX2	502B 003Ch
FSI_RX3	502B 103Ch

Figure 3-494. FSI_RX_CFG_RX_LOCK_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							LOCK
R							R/W
0h							0h

Table 3-890. FSI_RX_CFG_RX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register.
7:1	RESERVED_1	R	0h	Reserved
0	LOCK	R/W	0h	Control Register Lock Enable bit This bit locks the contents of all the receive control registers that support a lock protection. Once locked, further writes will not take effect until SYSRS unlocks the register. Once set, further writes even to this bit will be ignored. 0h[R/W] = Receive control registers can be modified and are not locked. 1h[R/W] = Receive control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

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3.11.2.22 FSI_RX_CFG_RX_ECC_DATA Register

3.11.2.22.1 FSI_RX_CFG_RX_ECC_DATA Register (Offset = 40h) [reset = 0h]

Receive ECC data register.

Return to Summary Table

Table 3-891. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0040h
FSI_RX1	5029 1040h
FSI_RX2	502B 0040h
FSI_RX3	502B 1040h

Figure 3-495. FSI_RX_CFG_RX_ECC_DATA Name Register

31	30	29	28	27	26	25	24
DATA_HIGH							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA_HIGH							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA_LOW							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA_LOW							
R/W							
0h							

Table 3-892. FSI_RX_CFG_RX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA_HIGH	R/W	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register.
15:0	DATA_LOW	R/W	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits.

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3.11.2.23 FSI_RX_CFG_RX_ECC_VAL Register

3.11.2.23.1 FSI_RX_CFG_RX_ECC_VAL Register (Offset = 44h) [reset = 0h]

Receive ECC value register.

Return to Summary Table

Table 3-893. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0044h
FSI_RX1	5029 1044h
FSI_RX2	502B 0044h
FSI_RX3	502B 1044h

Figure 3-496. FSI_RX_CFG_RX_ECC_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	ECC_VAL						
R	R/W						
0h	0h						

Table 3-894. FSI_RX_CFG_RX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6:0	ECC_VAL	R/W	0h	ECC Value for SEC-DED check This field contains the ECC value to be used for SEC-DED either for 16-bit or 32-bit data in the RX_ECC_DATA register.

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3.11.2.24 FSI_RX_CFG_RX_ECC_SEC_DATA Register

3.11.2.24.1 FSI_RX_CFG_RX_ECC_SEC_DATA Register (Offset = 48h) [reset = 0h]

Receive ECC corrected data register.

Return to Summary Table

Table 3-895. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0048h
FSI_RX1	5029 1048h
FSI_RX2	502B 0048h
FSI_RX3	502B 1048h

Figure 3-497. FSI_RX_CFG_RX_ECC_SEC_DATA Name Register

31	30	29	28	27	26	25	24
SEC_DATA							
R							
0h							
23	22	21	20	19	18	17	16
SEC_DATA							
R							
0h							
15	14	13	12	11	10	9	8
SEC_DATA							
R							
0h							
7	6	5	4	3	2	1	0
SEC_DATA							
R							
0h							

Table 3-896. FSI_RX_CFG_RX_ECC_SEC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SEC_DATA	R	0h	ECC Single Error Corrected Data The ECC corrected data will be available in this register. This value is valid only when there are no bit errors, or a single bit error was detected. Otherwise, the contents of this register are invalid and should not be used.

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3.11.2.25 FSI_RX_CFG_RX_ECC_LOG Register

3.11.2.25.1 FSI_RX_CFG_RX_ECC_LOG Register (Offset = 4Ch) [reset = 3h]

Receive ECC log and status register.

Return to Summary Table

Table 3-897. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 004Ch
FSI_RX1	5029 104Ch
FSI_RX2	502B 004Ch
FSI_RX3	502B 104Ch

Figure 3-498. FSI_RX_CFG_RX_ECC_LOG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						MBE	SBE
R						R	R
0h						1h	1h

Table 3-898. FSI_RX_CFG_RX_ECC_LOG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED_1	R	0h	Reserved
1	MBE	R	1h	Multiple Bit Errors Detected This bit indicates the occurrence of multiple bit errors.The data is corrupted and cannot be corrected. If this bit is set, the data present in RX_ECC_SEC_DATA is invalid and should not be used. 0h[R] Multiple Bit Errors were not detected. Check the SBE bit for single bit errors. 1h[R] Multiple Bit Errors were detected. The data is not able to be corrected. The value present in RX_ECC_SEC_DATA is invalid and should not be used.
0	SBE	R	1h	Single Bit Error Detected This bit indicates the occurrence of a single bit error in the data. The data is autocorrected and placed into the RX_ECC_SEC_DATA register. This bit is valid only if MBE is 0. 0h[R] No bit errors were detected. The value in RX_ECC_SEC_DATA is correct. 1h[R] A single bit error was detected and corrected. The corrected data is present in RX_ECC_SEC_DATA.

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3.11.2.26 FSI_RX_CFG_RX_FRAME_TAG_CMP Register

3.11.2.26.1 FSI_RX_CFG_RX_FRAME_TAG_CMP Register (Offset = 50h) [reset = 0h]

Receive frame tag compare register.

Return to Summary Table

Table 3-899. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0050h
FSI_RX1	5029 1050h
FSI_RX2	502B 0050h
FSI_RX3	502B 1050h

Figure 3-499. FSI_RX_CFG_RX_FRAME_TAG_CMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1						BROADCAST_EN	CMP_EN
R						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TAG_MASK				TAG_REF			
R/W				R/W			
0h				0h			

Table 3-900. FSI_RX_CFG_RX_FRAME_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9	BROADCAST_EN	R/W	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the frame tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h[R/W] Broadcast frame match disabled. 1h[R/W] Broadcast frame match enabled.
8	CMP_EN	R/W	0h	Frame Tag Compare Enable bit Set this bit to enable the comparison of an incoming frame tag and the value stored in the frame tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming frame tag will trigger the apprpriate frame tag match event. 0h[R/W] Frame tag comparison is disabled. 1h[R/W] Frame tag comparison is enabled.
7:4	TAG_MASK	R/W	0h	Frame Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for non-ping frames.
3:0	TAG_REF	R/W	0h	Frame Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming frame tag. This reference value is used only for non-ping frames.

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3.11.2.27 FSI_RX_CFG_RX_PING_TAG_CMP Register

3.11.2.27.1 FSI_RX_CFG_RX_PING_TAG_CMP Register (Offset = 52h) [reset = 0h]

Receive ping tag compare register.

Return to Summary Table

Table 3-901. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0052h
FSI_RX1	5029 1052h
FSI_RX2	502B 0052h
FSI_RX3	502B 1052h

Figure 3-500. FSI_RX_CFG_RX_PING_TAG_CMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1						BROADCAST_EN	CMP_EN
R						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TAG_MASK				TAG_REF			
R/W				R/W			
0h				0h			

Table 3-902. FSI_RX_CFG_RX_PING_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9	BROADCAST_EN	R/W	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the ping tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h[R/W] Broadcast frame match disabled. 1h[R/W] Broadcast frame match enabled.
8	CMP_EN	R/W	0h	Ping Tag Compare Enable bit Set this bit to enable the comparison of an incoming ping tag and the value stored in the ping tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming ping tag will trigger a ping frame tag match event. 0h[R/W] Ping tag comparison is disabled. 1h[R/W] Ping tag comparison is enabled.
7:4	TAG_MASK	R/W	0h	Ping Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming ping frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for ping frames.
3:0	TAG_REF	R/W	0h	Ping Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming ping tag. This reference value is used only for ping frames.

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3.11.2.28 FSI_RX_CFG_RX_TRIG_CTRL_0 Register

3.11.2.28.1 FSI_RX_CFG_RX_TRIG_CTRL_0 Register (Offset = 58h) [reset = 0h]

Receive Trigger Control register 0

Return to Summary Table

Table 3-903. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0058h
FSI_RX1	5029 1058h
FSI_RX2	502B 0058h
FSI_RX3	502B 1058h

Figure 3-501. FSI_RX_CFG_RX_TRIG_CTRL_0 Name Register

31	30	29	28	27	26	25	24
RX_TRIG_DLY							
R/W							
0h							
23	22	21	20	19	18	17	16
RX_TRIG_DLY							
R/W							
0h							
15	14	13	12	11	10	9	8
RX_TRIG_DLY							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			TRIG_SEL				TRIG_EN
R			R/W				R/W
0h			0h				0h

Table 3-904. FSI_RX_CFG_RX_TRIG_CTRL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7:5	RESERVED_1	R	0h	Reserved
4:1	TRIG_SEL	R/W	0h	This is the mux Select Value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

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3.11.2.29 FSI_RX_CFG_RX_TRIG_WIDTH_0 Register

3.11.2.29.1 FSI_RX_CFG_RX_TRIG_WIDTH_0 Register (Offset = 5Ch) [reset = 0h]

Receive Trigger Wdith register 0

Return to Summary Table

Table 3-905. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 005Ch
FSI_RX1	5029 105Ch
FSI_RX2	502B 005Ch
FSI_RX3	502B 105Ch

Figure 3-502. FSI_RX_CFG_RX_TRIG_WIDTH_0 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RX_TRIG_WIDTH							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_TRIG_WIDTH							
R/W							
0h							

Table 3-906. FSI_RX_CFG_RX_TRIG_WIDTH_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_1	R	0h	Reserved
15:0	RX_TRIG_WIDTH	R/W	0h	This register decides the width[in SYSCLK cycles] of wide pulse output of the RX trigger module.

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3.11.2.30 FSI_RX_CFG_RX_DLYLINE_CTRL Register

3.11.2.30.1 FSI_RX_CFG_RX_DLYLINE_CTRL Register (Offset = 60h) [reset = 0h]

Receive delay line control register.

Return to Summary Table

Table 3-907. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0060h
FSI_RX1	5029 1060h
FSI_RX2	502B 0060h
FSI_RX3	502B 1060h

Figure 3-503. FSI_RX_CFG_RX_DLYLINE_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	RXD1_DLY					RXD0_DLY	
R	R/W					R/W	
0h	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RXD0_DLY			RXCLK_DLY				
R/W			R/W				
0h			0h				

Table 3-908. FSI_RX_CFG_RX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:10	RXD1_DLY	R/W	0h	Delay Line Tap Select for RXD1 This bitfield selects the number of delay elements inserted into the RXD1 path from the pin boundary to the receiver core. 0h[R/W] Zero delay elements are included in the RXD1 path. RXD1 is taken directly from the pin. 1h[R/W] One delay element is included in the RXD1 path. 2h[R/W] Two delay elements are included in the RXD1 path. ... 1Fh [R/W] 31 delay elements are included in the RXD1 path, the maximum.
9:5	RXD0_DLY	R/W	0h	Delay Line Tap Select for RXD0 This bitfield selects the number of delay elements inserted into the RXD0 path from the pin boundary to the receiver core. 0h[R/W] Zero delay elements are included in the RXD0 path. RXD0 is taken directly from the pin. 1h[R/W] One delay element is included in the RXD0 path. 2h[R/W] Two delay elements are included in the RXD0 path. ... 1Fh [R/W] 31 delay elements are included in the RXD0 path, the maximum.
4:0	RXCLK_DLY	R/W	0h	Delay Line Tap Select for RXCLK This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core. 0h[R/W] Zero delay elements are included in the RXCLK path. RXCLK is taken directly from the pin. 1h[R/W] One delay element is included in the RXCLK path. 2h[R/W] Two delay elements are included in the RXCLK path. ... 1Fh [R/W] 31 delay elements are included in the RXCLK path, the maximum.

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3.11.2.31 FSI_RX_CFG_RX_TRIG_CTRL_1 Register

3.11.2.31.1 FSI_RX_CFG_RX_TRIG_CTRL_1 Register (Offset = 64h) [reset = 0h]

Receive Trigger Control register 1

Return to Summary Table

Table 3-909. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0064h
FSI_RX1	5029 1064h
FSI_RX2	502B 0064h
FSI_RX3	502B 1064h

Figure 3-504. FSI_RX_CFG_RX_TRIG_CTRL_1 Name Register

31	30	29	28	27	26	25	24
RX_TRIG_DLY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_TRIG_DLY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_TRIG_DLY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1			TRIG_SEL				TRIG_EN
R			R/W				R/W
0h			0h				0h

Table 3-910. FSI_RX_CFG_RX_TRIG_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7:5	RESERVED_1	R	0h	Reserved
4:1	TRIG_SEL	R/W	0h	This is the mux Select Value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

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3.11.2.32 FSI_RX_CFG_RX_TRIG_CTRL_2 Register

3.11.2.32.1 FSI_RX_CFG_RX_TRIG_CTRL_2 Register (Offset = 68h) [reset = 0h]

Receive Trigger Control register 2

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Table 3-911. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0068h
FSI_RX1	5029 1068h
FSI_RX2	502B 0068h
FSI_RX3	502B 1068h

Figure 3-505. FSI_RX_CFG_RX_TRIG_CTRL_2 Name Register

31	30	29	28	27	26	25	24
RX_TRIG_DLY							
R/W							
0h							
23	22	21	20	19	18	17	16
RX_TRIG_DLY							
R/W							
0h							
15	14	13	12	11	10	9	8
RX_TRIG_DLY							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			TRIG_SEL				TRIG_EN
R			R/W				R/W
0h			0h				0h

Table 3-912. FSI_RX_CFG_RX_TRIG_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7:5	RESERVED_1	R	0h	Reserved
4:1	TRIG_SEL	R/W	0h	This is the mux Select Value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

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3.11.2.33 FSI_RX_CFG_RX_TRIG_CTRL_3 Register

3.11.2.33.1 FSI_RX_CFG_RX_TRIG_CTRL_3 Register (Offset = 6Ch) [reset = 0h]

Receive Trigger Control register 3

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Table 3-913. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 006Ch
FSI_RX1	5029 106Ch
FSI_RX2	502B 006Ch
FSI_RX3	502B 106Ch

Figure 3-506. FSI_RX_CFG_RX_TRIG_CTRL_3 Name Register

31	30	29	28	27	26	25	24
RX_TRIG_DLY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_TRIG_DLY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_TRIG_DLY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1			TRIG_SEL				TRIG_EN
R			R/W				R/W
0h			0h				0h

Table 3-914. FSI_RX_CFG_RX_TRIG_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RX_TRIG_DLY	R/W	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7:5	RESERVED_1	R	0h	Reserved
4:1	TRIG_SEL	R/W	0h	This is the mux Select Value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	R/W	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

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3.11.2.34 FSI_RX_CFG_RX_VIS_1 Register

3.11.2.34.1 FSI_RX_CFG_RX_VIS_1 Register (Offset = 70h) [reset = 0h]

Receive debug visibility register 1

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Table 3-915. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0070h
FSI_RX1	5029 1070h
FSI_RX2	502B 0070h
FSI_RX3	502B 1070h

Figure 3-507. FSI_RX_CFG_RX_VIS_1 Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2				RX_CORE_STS	RESERVED_1		
R				R	R		
0h				0h	0h		

Table 3-916. FSI_RX_CFG_RX_VIS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED_2	R	0h	Reserved
3	RX_CORE_STS	R	0h	Receiver Core Status bit This bit indicates the status of the receiver core. If this bit is set, the receiver should undergo a reset and subsequent resynchronization with the transmitter. This bit will be always be set when the receiver has detected and end of frame error or a frame type error. This bit can also be set if the receiver becomes corrupted due to noise on the signal lines. If the receiver has experienced a ping watchdog or frame watchdog timeout, this bit should be read to determine if the cause was due to a corrupt transaction, thus putting the receiver core into an unrecoverable state. Only a soft reset will reset the recevier core and thus reset this bit. 0h[R] The receiver core is operating normally. 1h[R] The receiver core has entered into an error state and should be reset.
2:0	RESERVED_1	R	0h	Reserved

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3.11.2.35 FSI_RX_CFG_RX_UDATA_FILTER Register

3.11.2.35.1 FSI_RX_CFG_RX_UDATA_FILTER Register (Offset = 74h) [reset = 0h]

Receive User Data Filter Control register.

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Table 3-917. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0074h
FSI_RX1	5029 1074h
FSI_RX2	502B 0074h
FSI_RX3	502B 1074h

Figure 3-508. FSI_RX_CFG_RX_UDATA_FILTER Name Register

15	14	13	12	11	10	9	8
UDATA_MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
UDATA_REG							
R/W							
0h							

Table 3-918. FSI_RX_CFG_RX_UDATA_FILTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	UDATA_MASK	R/W	0h	Bit Mask to be used for comparing the USERDATA field when filtering is enabled. Every bit that is '1' in this register will be masked for comparison. If a bit position is '1', then it will be considered a successful match for that bit position.
7:0	UDATA_REG	R/W	0h	Reference to be used for comparing the USERDATA field when filtering is enabled.

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3.11.2.36 FSI_RX_CFG_RX_BUF_BASE_J Register

3.11.2.36.1 FSI_RX_CFG_RX_BUF_BASE_J Register (Offset = 80h) [reset = 0h]

Base address for receive data buffer.

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Table 3-919. Instance Table

Instance Name	Physical Address
FSI_RX0	5029 0080h + formula
FSI_RX1	5029 1080h + formula
FSI_RX2	502B 0080h + formula
FSI_RX3	502B 1080h + formula

Figure 3-509. FSI_RX_CFG_RX_BUF_BASE_j Name Register

15	14	13	12	11	10	9	8
BASE_ADDRESS							
R							
0h							
7	6	5	4	3	2	1	0
BASE_ADDRESS							
R							
0h							

Table 3-920. FSI_RX_CFG_RX_BUF_BASE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	BASE_ADDRESS	R	0h	Receive Data Buffer Base Address This is the base address of the 16-word data buffer used by the receiver.

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3.12 FSI_TX

FSI_TX

3.12.1 FSI_TX Summaries

FSI_TX Summaries

Table 3-921. FSI_TX_CFG Registers, Base Address=5028 0000h, Length=4096

Offset	Length	Register Name	FSI_TX0 Physical Address	FSI_TX1 Physical Address	FSI_TX2 Physical Address
0h	16	FSI_TX_CFG_TX_MASTER_CTRL	5028 0000h	5028 1000h	502A 0000h
4h	16	FSI_TX_CFG_TX_CLK_CTRL	5028 0004h	5028 1004h	502A 0004h
8h	16	FSI_TX_CFG_TX_OPER_CTRL_LO_ALT2	5028 0008h	5028 1008h	502A 0008h
Ah	16	FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1	5028 000Ah	5028 100Ah	502A 000Ah
Ch	16	FSI_TX_CFG_TX_FRAME_CTRL	5028 000Ch	5028 100Ch	502A 000Ch
Eh	16	FSI_TX_CFG_TX_FRAME_TAG_UDATA	5028 000Eh	5028 100Eh	502A 000Eh
10h	16	FSI_TX_CFG_TX_BUF_PTR_LOAD	5028 0010h	5028 1010h	502A 0010h
12h	16	FSI_TX_CFG_TX_BUF_PTR_STS	5028 0012h	5028 1012h	502A 0012h
14h	16	FSI_TX_CFG_TX_PING_CTRL_ALT1	5028 0014h	5028 1014h	502A 0014h
16h	16	FSI_TX_CFG_TX_PING_TAG	5028 0016h	5028 1016h	502A 0016h
18h	32	FSI_TX_CFG_TX_PING_TO_REF	5028 0018h	5028 1018h	502A 0018h
1Ch	32	FSI_TX_CFG_TX_PING_TO_CNT	5028 001Ch	5028 101Ch	502A 001Ch
20h	16	FSI_TX_CFG_TX_INT_CTRL	5028 0020h	5028 1020h	502A 0020h
22h	16	FSI_TX_CFG_TX_DMA_CTRL	5028 0022h	5028 1022h	502A 0022h
24h	16	FSI_TX_CFG_TX_LOCK_CTRL	5028 0024h	5028 1024h	502A 0024h
28h	16	FSI_TX_CFG_TX_EVT_STS	5028 0028h	5028 1028h	502A 0028h
2Ch	16	FSI_TX_CFG_TX_EVT_CLR	5028 002Ch	5028 102Ch	502A 002Ch
2Eh	16	FSI_TX_CFG_TX_EVT_FRC	5028 002Eh	5028 102Eh	502A 002Eh
30h	16	FSI_TX_CFG_TX_USER_CRC	5028 0030h	5028 1030h	502A 0030h
40h	32	FSI_TX_CFG_TX_ECC_DATA	5028 0040h	5028 1040h	502A 0040h
44h	16	FSI_TX_CFG_TX_ECC_VAL	5028 0044h	5028 1044h	502A 0044h
48h	16	FSI_TX_CFG_TX_DLYLINE_CTRL	5028 0048h	5028 1048h	502A 0048h
80h	16	FSI_TX_CFG_TX_BUF_BASE_J	5028 0080h + formula	5028 1080h + formula	502A 0080h + formula

Table 3-922. FSI_TX_CFG Registers, Base Address=5028 0000h, Length=4096

Offset	Length	Register Name	FSI_TX3 Physical Address
0h	16	FSI_TX_CFG_TX_MASTER_CTRL	502A 1000h
4h	16	FSI_TX_CFG_TX_CLK_CTRL	502A 1004h
8h	16	FSI_TX_CFG_TX_OPER_CTRL_LO_ALT2	502A 1008h
Ah	16	FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1	502A 100Ah
Ch	16	FSI_TX_CFG_TX_FRAME_CTRL	502A 100Ch
Eh	16	FSI_TX_CFG_TX_FRAME_TAG_UDATA	502A 100Eh
10h	16	FSI_TX_CFG_TX_BUF_PTR_LOAD	502A 1010h
12h	16	FSI_TX_CFG_TX_BUF_PTR_STS	502A 1012h
14h	16	FSI_TX_CFG_TX_PING_CTRL_ALT1	502A 1014h

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Table 3-922. FSI_TX_CFG Registers, Base Address=5028 0000h, Length=4096 (continued)

Offset	Length	Register Name	FSI_TX3 Physical Address
16h	16	FSI_TX_CFG_TX_PING_TAG	502A 1016h
18h	32	FSI_TX_CFG_TX_PING_TO_REF	502A 1018h
1Ch	32	FSI_TX_CFG_TX_PING_TO_CNT	502A 101Ch
20h	16	FSI_TX_CFG_TX_INT_CTRL	502A 1020h
22h	16	FSI_TX_CFG_TX_DMA_CTRL	502A 1022h
24h	16	FSI_TX_CFG_TX_LOCK_CTRL	502A 1024h
28h	16	FSI_TX_CFG_TX_EVT_STS	502A 1028h
2Ch	16	FSI_TX_CFG_TX_EVT_CLR	502A 102Ch
2Eh	16	FSI_TX_CFG_TX_EVT_FRC	502A 102Eh
30h	16	FSI_TX_CFG_TX_USER_CRC	502A 1030h
40h	32	FSI_TX_CFG_TX_ECC_DATA	502A 1040h
44h	16	FSI_TX_CFG_TX_ECC_VAL	502A 1044h
48h	16	FSI_TX_CFG_TX_DLYLINE_CTRL	502A 1048h
80h	16	FSI_TX_CFG_TX_BUF_BASE_J	502A 1080h + formula

3.12.2 FSI_TX Registers

FSI_TX Registers

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3.12.2.1 FSI_TX_CFG_TX_MASTER_CTRL Register

3.12.2.1.1 FSI_TX_CFG_TX_MASTER_CTRL Register (Offset = 0h) [reset = 0h]

Transmit master control register.

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Table 3-923. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0000h
FSI_TX1	5028 1000h
FSI_TX2	502A 0000h
FSI_TX3	502A 1000h

Figure 3-510. FSI_TX_CFG_TX_MASTER_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						FLUSH	CORE_RST
R						R/W	R/W
0h						0h	0h

Table 3-924. FSI_TX_CFG_TX_MASTER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key In order to write to any bit in this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register.
7:2	RESERVED_1	R	0h	Reserved
1	FLUSH	R/W	0h	Flush Operation Start bit This bit will cause the transmitter to initiate a flush pattern of a single toggle on the TXD0 and TXD1 followed by five full cycles of TXCLK. This bit should be written only when the CORE_RST bit is 0 and the clock to the Transmitter core is turned on. 0h[R/W] = Clear this bit. 1h[R/W] = Setting this bit will Initiate flush sequence. To properly execute a flush sequence, Set FLUSH to 1, wait for five TXCLK cycles then clear FLUSH to 0. Note: The KEY field must contain 0xA5 for any write to this bit to take effect. The software must keep this bit set to 1 for at least five TXCLK cycles before setting it back to 0.
0	CORE_RST	R/W	0h	Transmitter Master Core Reset bit This bit controls the transmitter master core reset. In order to send any frame, this bit must be cleared. 0h[R/W] = Transmitter core is not in reset and can transmit frames. 1h[R/W] = Transmitter core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

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3.12.2.2 FSI_TX_CFG_TX_CLK_CTRL Register

3.12.2.2.1 FSI_TX_CFG_TX_CLK_CTRL Register (Offset = 4h) [reset = 0h]

Transmit clock control register.

Return to Summary Table

Table 3-925. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0004h
FSI_TX1	5028 1004h
FSI_TX2	502A 0004h
FSI_TX3	502A 1004h

Figure 3-511. FSI_TX_CFG_TX_CLK_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PRESCALE_VAL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRESCALE_VAL						CLK_EN	CLK_RST
R/W						R/W	R/W
0h						0h	0h

Table 3-926. FSI_TX_CFG_TX_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:2	PRESCALE_VAL	R/W	0h	Clock Divider Prescale Value The input clock is divided by this 8-bit value and fed into the transmitter core. This divided clock is the rate at which TXCLK will operate. 0h[R/W] = Reserved 1h[R/W] = Input clock /1 2h[R/W] = Input clock /2 3h[R/W] = Input clock /3 4h[R/W] = Input clock /4 ... FFh [R/W] = Input clock /255 TXCLKIN = Input clock / PRESCALE_VAL In FSI mode: TXCLK = TXCLKIN / 2 In SPI mode: TXCLK = TXCLKIN
1	CLK_EN	R/W	0h	Clock Divider Enable bit This bit will enable and disable the input clock divider and start the clock to the transmitter core. 0h[R/W] = The input clock divider is not enabled and the clock is not connected to the transmitter core. 1h[R/W] = The input clock to the transmitter core is being divided by the PRESCALE_VAL and enabled.
0	CLK_RST	R/W	0h	Clock Divider Reset bit This bit will reset the clock counter in the clock divider. 0h[R/W] = The clock divider is set based on the value in PRESCALE_VAL. The input clock will be divided by PRESCALE_VAL if CLK_EN is set. 1h[R/W] = The clock divider will be reset to 0 and will stay reset until software writes a 0 to this bit.

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3.12.2.3 FSI_TX_CFG_TX_OPER_CTRL_LO_ALT2 Register

3.12.2.3.1 FSI_TX_CFG_TX_OPER_CTRL_LO_ALT2 Register (Offset = 8h) [reset = 0h]

Transmit operation control register low.

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Table 3-927. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0008h
FSI_TX1	5028 1008h
FSI_TX2	502A 0008h
FSI_TX3	502A 1008h

Figure 3-512. FSI_TX_CFG_TX_OPER_CTRL_LO_ALT2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1					SEL_TDM_IN	TDM_ENABLE	SEL_PLLCLK
R					R/W	R/W	R/W
0h					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PING_TO_MODE	SW_CRC	START_MODE			SPI_MODE	DATA_WIDTH	
R/W	R/W	R/W			R/W	R/W	
0h	0h	0h			0h	0h	

Table 3-928. FSI_TX_CFG_TX_OPER_CTRL_LO_ALT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10	SEL_TDM_IN	R/W	0h	Input TDM port Select bit This bit selects the input port for the transmitter core between the TDM input pins or the RX module. When this bit is '0', the inputs selected for TDM are from the TDM input pins. When this bit is '1', then inputs selected for TDM are from the RX module.
9	TDM_ENABLE	R/W	0h	Transmit TDM Mode Enable bit. This bit enables the TDM Mode for multi-target TDM operation. 0h[R/W] Transmit TDM Mode is not enabled. 1h[R/W] Transmit TDM Mode is enabled.
8	SEL_PLLCLK	R/W	0h	Input Clock Select bit This bit selects the input clock source for the transmitter core. 0h[R/W] = SYSCLK is the source of the transmitter clock into the clock prescaler. 1h[R/W] = PLLRAWCLK is the source of the transmitter core clock into the clock prescaler.
7	PING_TO_MODE	R/W	0h	Ping Counter Reset Mode Select bit This bit selects when the ping counter will reset. 0h[R/W] = The ping counter will reset and restart only on hardware initiated ping frames, when ping counter has timed out. 1h[R/W] = The ping counter will reset and restart on any software initiated frame as well as a ping counter timeout
6	SW_CRC	R/W	0h	CRC Source Select bit This bit selects the source of the CRC value that is transmitted. 0h[R/W] = The transmitted CRC value is computed by hardware. 1h[R/W] = The transmitted CRC value is sourced from the value programmed in the TX_USER_CRC register.

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Table 3-928. FSI_TX_CFG_TX_OPER_CTRL_LO_ALT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:3	START_MODE	R/W	0h	Transmission Start Mode Select bit These bits select the method by which a new frame transmission is started. 0h[R/W] = Only a software write to TX_FRAME_CTRL.START initiate a new transmission. 1h[R/W] = The configured external trigger will initiate a new transmission. 2h[R/W] = Either Writing to TX_FRAME_CTRL.START or the TX_FRAME_TAG_UDATA register will initiate a new transmission. All other combinations of bits are illegal and reserved for future use.
2	SPI_MODE	R/W	0h	SPI Mode Select bit This bit enables and disables SPI compatibility mode. 0h[R/W] = FSI is in normal mode of operation. 1h[R/W] = FSI is operating in SPI compatibility mode.
1:0	DATA_WIDTH	R/W	0h	Transmit Data Width Select bits These bits define the number of data lines used by the transmitter. 0h[R/W] = Data will be transmitted on one data line [TXD0] 1h[R/W] = Data will be transmitted on two data lines [TXD0 and TXD1]. The format of the data is described in the FSI_TX TRM chapter. 2h 3h[R/W] = Reserved

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3.12.2.4 FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1 Register

3.12.2.4.1 FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1 Register (Offset = Ah) [reset = 0h]

Transmit operation control register high.

Return to Summary Table

Table 3-929. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 000Ah
FSI_TX1	5028 100Ah
FSI_TX2	502A 000Ah
FSI_TX3	502A 100Ah

Figure 3-513. FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1 Name Register

15	14	13	12	11	10	9	8
RESERVED_2			EXT_TRIG_SEL				
R			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXT_TRIG_SEL	ECC_SEL	FORCE_ERR	RESERVED_1				
R/W	R/W	R/W	R				
0h	0h	0h	0h				

Table 3-930. FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12:7	EXT_TRIG_SEL	R/W	0h	External Trigger Select bit These bits define which of the 64 external inputs will be used as the source for the external input trigger. 00h[R/W] = Trigger 1 is the source. 01h[R/W] = Trigger 2 is the source. 02h[R/W] = Trigger 3 is the source. ... 3Fh [R/W] = Trigger 64 is the source.
6	ECC_SEL	R/W	0h	ECC Data Width Select bit This bit selects between 16-bit and 32-bit ECC computation. 0h[R/W] = 32-bit ECC is used. 1h[R/W] = 16-bit ECC is used.
5	FORCE_ERR	R/W	0h	Error Frame Force bit This bit will force the the CRC value of the transmitted data frame to 0 whenever there is a buffer overrun or underrun condition. This can be used to force a corrupted CRC as the data is not guaranteed to be reliable. The receiver will treat the data as invalid and can handle this as needed. Note: DO NOT use FORCE_ERR if using the SW CRC mode [FSI Transmit]. 0h[R/W] = The CRC will not be forced to 0. 1h[R/W] = The CRC will be forced to 0 in a buffer overrun or underrun condition.
4:0	RESERVED_1	R	0h	Reserved

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3.12.2.5 FSI_TX_CFG_TX_FRAME_CTRL Register

3.12.2.5.1 FSI_TX_CFG_TX_FRAME_CTRL Register (Offset = Ch) [reset = 0h]

Transmit frame control register.

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Table 3-931. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 000Ch
FSI_TX1	5028 100Ch
FSI_TX2	502A 000Ch
FSI_TX3	502A 100Ch

Figure 3-514. FSI_TX_CFG_TX_FRAME_CTRL Name Register

15	14	13	12	11	10	9	8
START	RESERVED_1						
R/W	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
N_WORDS				FRAME_TYPE			
R/W				R/W			
0h				0h			

Table 3-932. FSI_TX_CFG_TX_FRAME_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	START	R/W	0h	Start Transmission bit This bit will cause the FSI to start transmitting the next frame. 0h[R/W] = Writing a 0 to this bit will have no effect. 1h[R/W] = Start the next transmission. This bit will be cleared by hardware.
14:8	RESERVED_1	R	0h	Reserved
7:4	N_WORDS	R/W	0h	Number of Words to be Transmitted This field defines the number of words which will be transmitted in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the receiver. Set this bitfield to be one less than the number of words to be transmitted. 0h[R/W] = 1 data word frame [16-bit data]. 1h[R/W] = 2 data word frame [32-bit data]. .. Fh [R/W] = 16 data word frame [256-bit data].

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Table 3-932. FSI_TX_CFG_TX_FRAME_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	FRAME_TYPE	R/W	0h	Transmit Frame Type This field determines the type of frame that will be transmitted next. 0000b[R/W] = Ping Frame. This frame can be sent either by software or automatically by hardware. 0100b[R/W] = DATA_1_WORD Frame. One word data frame [16-bit data]. 0101b[R/W] = DATA_2_WORD Frame. Two word data frame [32-bit data]. 0110b[R/W] = DATA_4_WORD Frame. Four word data frame [64-bit data]. 0111b[R/W] = DATA_6_WORD Frame. Six word data frame [96-bit data]. 0011b[R/W] = DATA_N_WORD Frame. The N_WORDS field will determine the number of words [1 to 16] to be sent. Both the transmitter and receiver must have the same value programmed. 1111b[R/W] = Error Frame. This frame can be used during error conditions or any condition where the transmitter wants to notify the receiver of a high priorty status. However, the user software is at liberty to use this for any purpose. 0001b 0010b and 1000bthrough 1110bare Reserved and should not be used.

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3.12.2.6 FSI_TX_CFG_TX_FRAME_TAG_UDATA Register

3.12.2.6.1 FSI_TX_CFG_TX_FRAME_TAG_UDATA Register (Offset = Eh) [reset = 0h]

Transmit frame tag and user data register.

Return to Summary Table

Table 3-933. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 000Eh
FSI_TX1	5028 100Eh
FSI_TX2	502A 000Eh
FSI_TX3	502A 100Eh

Figure 3-515. FSI_TX_CFG_TX_FRAME_TAG_UDATA Name Register

15	14	13	12	11	10	9	8
USER_DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				FRAME_TAG			
R				R/W			
0h				0h			

Table 3-934. FSI_TX_CFG_TX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	USER_DATA	R/W	0h	User Data bits This is a user-defined value that will be loaded into the the user data phase of the frame. This 8-bit value can be used by the receiver for any application need. This value will not impact any hardware behavior.
7:4	RESERVED_1	R	0h	Reserved
3:0	FRAME_TAG	R/W	0h	This will be used only for software initiated transmissions. Frame tag bits This is a user-defined value that will be loaded into the frame tag phase of the next transmission. The receiver may use the frame tag for any application need. This value will not impact any hardware behavior For external triggers do not use this register. Use the TX_PING_TAG register instead.

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3.12.2.7 FSI_TX_CFG_TX_BUF_PTR_LOAD Register

3.12.2.7.1 FSI_TX_CFG_TX_BUF_PTR_LOAD Register (Offset = 10h) [reset = 0h]

Transmit buffer pointer control load register.

Return to Summary Table

Table 3-935. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0010h
FSI_TX1	5028 1010h
FSI_TX2	502A 0010h
FSI_TX3	502A 1010h

Figure 3-516. FSI_TX_CFG_TX_BUF_PTR_LOAD Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				BUF_PTR_LOAD			
R				R/W			
0h				0h			

Table 3-936. FSI_TX_CFG_TX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3:0	BUF_PTR_LOAD	R/W	0h	Buffer Pointer Load bits These bits are used to force the transmit buffer pointer to a desired index within the transmit buffer. The next transmission will begin picking data from this index and increment appropriately. This value will be reflected in TX_BUF_PTR_STS only after a minimum 3 SYSCLK cycles + 3 TXCLK cycles. This value should not be written while there is an active transmission as it may corrupt the ongoing frame or other undefined behavior.

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3.12.2.8 FSI_TX_CFG_TX_BUF_PTR_STS Register

3.12.2.8.1 FSI_TX_CFG_TX_BUF_PTR_STS Register (Offset = 12h) [reset = 0h]

Transmit buffer pointer control status register.

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Table 3-937. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0012h
FSI_TX1	5028 1012h
FSI_TX2	502A 0012h
FSI_TX3	502A 1012h

Figure 3-517. FSI_TX_CFG_TX_BUF_PTR_STS Name Register

15	14	13	12	11	10	9	8
RESERVED_2			CURR_WORD_CNT				
R			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				CURR_BUF_PTR			
R				R			
0h				0h			

Table 3-938. FSI_TX_CFG_TX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_2	R	0h	Reserved
12:8	CURR_WORD_CNT	R	0h	Words Remaining in the transmit buffer This value indicates the number of words present in the data buffer which have not yet been transmitted. This value is only valid when there is no active transmission. Note: This value will not be valid if there is a buffer overrun or underrun condition.
7:4	RESERVED_1	R	0h	Reserved
3:0	CURR_BUF_PTR	R	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission.

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3.12.2.9 FSI_TX_CFG_TX_PING_CTRL_ALT1 Register

3.12.2.9.1 FSI_TX_CFG_TX_PING_CTRL_ALT1 Register (Offset = 14h) [reset = 0h]

Transmit ping control register.

Return to Summary Table

Table 3-939. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0014h
FSI_TX1	5028 1014h
FSI_TX2	502A 0014h
FSI_TX3	502A 1014h

Figure 3-518. FSI_TX_CFG_TX_PING_CTRL_ALT1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1							EXT_TRIG_SEL
R							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXT_TRIG_SEL					EXT_TRIG_EN	TIMER_EN	CNT_RST
R/W					R/W	R/W	R/W
0h					0h	0h	0h

Table 3-940. FSI_TX_CFG_TX_PING_CTRL_ALT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED_1	R	0h	Reserved
8:3	EXT_TRIG_SEL	R/W	0h	External Trigger Select bits This bitfield will select one of the 64 external trigger inputs to as the source to generate a ping frame. A ping frame will only be generated if the EXT_TRIG_EN bit is set. 0h[R/W] = Trigger 1 will be used to generate a ping frame. 1h[R/W] = Trigger 2 will be used to generate a ping frame. .. 3Fh [R/W] = Trigger 64 will be used to generate a ping frame.
2	EXT_TRIG_EN	R/W	0h	External Trigger Enable bit This bit will allow the external trigger logic to generate a ping frame. 0h[R/W] = External triggers will not be used to generate ping frames. 1h[R/W] = The selected external trigger [selected by EXT_TRIG_SEL bits] will be able to generate a ping frame. The ping timer will be ignored if this bit is set.
1	TIMER_EN	R/W	0h	Ping Timer Enable bit This bit will enable the ping timer for generating periodic ping frames. 0h[R/W] = The ping timer is disabled and will not generate ping frames. 1h[R/W] = The ping timer is enabled and can be used to generate ping frames.Once the timer count reaches the value set by the TX_PING_TO_REF register, it will initiate a ping frame transmission. Note: If the ping timer is used, EXT_TRIG_EN should not be set as it will override this function.
0	CNT_RST	R/W	0h	Ping Counter Reset bit Writing a 1 to this bit will reset the ping counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter. 0h[R/W] = Clear the CNT_RST. 1h[R/W] = The ping counter will be reset to 0.

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3.12.2.10 FSI_TX_CFG_TX_PING_TAG Register

3.12.2.10.1 FSI_TX_CFG_TX_PING_TAG Register (Offset = 16h) [reset = 0h]

Transmit ping tag register.

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Table 3-941. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0016h
FSI_TX1	5028 1016h
FSI_TX2	502A 0016h
FSI_TX3	502A 1016h

Figure 3-519. FSI_TX_CFG_TX_PING_TAG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1				TAG			
R				R/W			
0h				0h			

Table 3-942. FSI_TX_CFG_TX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3:0	TAG	R/W	0h	Ping Frame Tag This field contains a 4-bit tag which will be sent in any ping frame that is initiated by an external trigger or the ping timer. This field is user-defined and can be set based on the application requirement. If a ping frame is generated manually, the transmitted tag will be from TX_FRAME_TAG_UDATA.FRAME_TAG, not this value.

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3.12.2.11 FSI_TX_CFG_TX_PING_TO_REF Register

3.12.2.11.1 FSI_TX_CFG_TX_PING_TO_REF Register (Offset = 18h) [reset = 0h]

Transmit ping timeout counter reference.

Return to Summary Table

Table 3-943. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0018h
FSI_TX1	5028 1018h
FSI_TX2	502A 0018h
FSI_TX3	502A 1018h

Figure 3-520. FSI_TX_CFG_TX_PING_TO_REF Name Register

31	30	29	28	27	26	25	24
TO_REF							
R/W							
0h							
23	22	21	20	19	18	17	16
TO_REF							
R/W							
0h							
15	14	13	12	11	10	9	8
TO_REF							
R/W							
0h							
7	6	5	4	3	2	1	0
TO_REF							
R/W							
0h							

Table 3-944. FSI_TX_CFG_TX_PING_TO_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TO_REF	R/W	0h	Ping Timer Reference Value. This is the 32-bit reference value for the ping timer. The timer will increment the counter starting from 0. When the reference value is reached, it will generate a timeout event, triggering a ping frame transmission. The counter will then reset to 0 and continue counting.

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3.12.2.12 FSI_TX_CFG_TX_PING_TO_CNT Register

3.12.2.12.1 FSI_TX_CFG_TX_PING_TO_CNT Register (Offset = 1Ch) [reset = 0h]

Transmit ping timeout current count.

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Table 3-945. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 001Ch
FSI_TX1	5028 101Ch
FSI_TX2	502A 001Ch
FSI_TX3	502A 101Ch

Figure 3-521. FSI_TX_CFG_TX_PING_TO_CNT Name Register

31	30	29	28	27	26	25	24
TO_CNT							
R							
0h							
23	22	21	20	19	18	17	16
TO_CNT							
R							
0h							
15	14	13	12	11	10	9	8
TO_CNT							
R							
0h							
7	6	5	4	3	2	1	0
TO_CNT							
R							
0h							

Table 3-946. FSI_TX_CFG_TX_PING_TO_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TO_CNT	R	0h	Ping Timer Counter Value This register contains the current value of the ping timer counter. After reset, this counter will increment until it reaches the reference value [TX_PING_TO_REF], at which point it generates a ping frame transmission. After this point, the counter will reset to 0 and continue counting. This is a free-running counter

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3.12.2.13 FSI_TX_CFG_TX_INT_CTRL Register

3.12.2.13.1 FSI_TX_CFG_TX_INT_CTRL Register (Offset = 20h) [reset = 0h]

Transmit interrupt event control register.

Return to Summary Table

Table 3-947. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0020h
FSI_TX1	5028 1020h
FSI_TX2	502A 0020h
FSI_TX3	502A 1020h

Figure 3-522. FSI_TX_CFG_TX_INT_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_2				INT2_EN_PING_TO	INT2_EN_BUF_OVERRUN	INT2_EN_BUF_UNDERRUN	INT2_EN_FRAME_DONE
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				INT1_EN_PING_TO	INT1_EN_BUF_OVERRUN	INT1_EN_BUF_UNDERRUN	INT1_EN_FRAME_DONE
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 3-948. FSI_TX_CFG_TX_INT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_2	R	0h	Reserved
11	INT2_EN_PING_TO	R/W	0h	Enable PING Timer Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h[R/W] = This event will not trigger an interrupt on TX_INT2. 1h[R/W] = The ping timer event will trigger an interrupt on TX_INT2.
10	INT2_EN_BUF_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h[R/W] = This event will not trigger an interrupt on TX_INT2. 1h[R/W] = A Buffer Overrun condition will trigger an interrupt on TX_INT2.
9	INT2_EN_BUF_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h[R/W] = This event will not trigger an interrupt on TX_INT2. 1h[R/W] = A Buffer Underrun condition will trigger an interrupt on TX_INT2.
8	INT2_EN_FRAME_DONE	R/W	0h	Enable Frame Done interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h[R/W] = This event will not trigger an interrupt on TX_INT2. 1h[R/W] = A Frame Done event will trigger an interrupt on TX_INT2.
7:4	RESERVED_1	R	0h	Reserved
3	INT1_EN_PING_TO	R/W	0h	Enable Ping Timer Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h[R/W] = This event will not trigger an interrupt on TX_INT1. 1h[R/W] = The ping timer event will trigger an interrupt on TX_INT1.
2	INT1_EN_BUF_OVERRUN	R/W	0h	Enable Buffer Overrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h[R/W] = This event will not trigger an interrupt on TX_INT1. 1h[R/W] = A Buffer Overrun condition will trigger an interrupt on TX_INT1.

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Table 3-948. FSI_TX_CFG_TX_INT_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INT1_EN_BUF_UNDERRUN	R/W	0h	Enable Buffer Underrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h[R/W] = This event will not trigger an interrupt on TX_INT1. 1h[R/W] = A Buffer Underrun condition will trigger an interrupt on TX_INT1.
0	INT1_EN_FRAME_DONE	R/W	0h	Enable Frame Done interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h[R/W] = This event will not trigger an interrupt on TX_INT1. 1h[R/W] = A Frame Done event will trigger an interrupt on TX_INT1.

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3.12.2.14 FSI_TX_CFG_TX_DMA_CTRL Register

3.12.2.14.1 FSI_TX_CFG_TX_DMA_CTRL Register (Offset = 22h) [reset = 0h]

Transmit DMA event control register.

Return to Summary Table

Table 3-949. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0022h
FSI_TX1	5028 1022h
FSI_TX2	502A 0022h
FSI_TX3	502A 1022h

Figure 3-523. FSI_TX_CFG_TX_DMA_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							DMA_EVT_EN
R							R/W
0h							0h

Table 3-950. FSI_TX_CFG_TX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	DMA_EVT_EN	R/W	0h	DMA Event Enable bit This bit will enable the DMA event to be generated upon the completion of a transmit frame. 0h[R/W] = A DMA event will not be generated. 1h[R/W] = A DMA event will be generated upon the completion of a transmitted frame. Note: The DMA event will only be generated for data frames.

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3.12.2.15 FSI_TX_CFG_TX_LOCK_CTRL Register

3.12.2.15.1 FSI_TX_CFG_TX_LOCK_CTRL Register (Offset = 24h) [reset = 0h]

Transmit lock control register.

Return to Summary Table

Table 3-951. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0024h
FSI_TX1	5028 1024h
FSI_TX2	502A 0024h
FSI_TX3	502A 1024h

Figure 3-524. FSI_TX_CFG_TX_LOCK_CTRL Name Register

15	14	13	12	11	10	9	8
KEY							
W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							LOCK
R							R/W
0h							0h

Table 3-952. FSI_TX_CFG_TX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	KEY	W	0h	Write Key In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register.
7:1	RESERVED_1	R	0h	Reserved
0	LOCK	R/W	0h	Control Register Lock Enable bit This bit locks the contents of all the transmit control registers that support a lock protection. Once locked, further writes will not take effect until a SYSRS has reset this register. Once set, further writes to this bit will be ignored. 0h[R/W] = Transmit control registers can be modified and are not locked. 1h[R/W] = Transmit control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

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3.12.2.16 FSI_TX_CFG_TX_EVT_STS Register

3.12.2.16.1 FSI_TX_CFG_TX_EVT_STS Register (Offset = 28h) [reset = 0h]

Transmit event and error status flag register.

Return to Summary Table

Table 3-953. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0028h
FSI_TX1	5028 1028h
FSI_TX2	502A 0028h
FSI_TX3	502A 1028h

Figure 3-525. FSI_TX_CFG_TX_EVT_STS Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R				R	R	R	R
0h				0h	0h	0h	0h

Table 3-954. FSI_TX_CFG_TX_EVT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	PING_TRIGGERED	R	0h	Ping Frame Triggered Flag Bit This bit indicates that a ping frame has been triggered. This bit is set by hardware when either the ping timer or an external trigger event have occured. Software can also force this bit to get set by Writing to the TX_EVT_FRC register. 0h[R] = A ping frame has not been triggered. 1h[R] = A ping frame has been triggered by either the ping timer or external trigger. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.
2	BUF_OVERRUN	R	0h	Buffer Overrun Flag Bit This bit inditcates that buffer overrun has occured.Software can also force this bit to get set by Writing to the TX_EVT_FRC register. 0h[R] = Buffer Overrun has not occured. 1h[R] = Buffer Overrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.
1	BUF_UNDERRUN	R	0h	Buffer Underrun Flag Bit This bit inditcates that buffer underrun has occured.Software can also force this bit to get set by Writing to the TX_EVT_FRC register. 0h[R] = Buffer Underrun has not occured. 1h[R] = Buffer Underrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.

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Table 3-954. FSI_TX_CFG_TX_EVT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FRAME_DONE	R	0h	Frame Done Flag Bit This bit inditcates a Frame Done condition. This bit is set by hardware when a frame transmission has been completed. Software can also force this bit to get set by Writing to the TX_EVT_FRC register. 0h[R] = Frame Done condition has not occured. 1h[R] = Frame Done condition has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.

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3.12.2.17 FSI_TX_CFG_TX_EVT_CLR Register

3.12.2.17.1 FSI_TX_CFG_TX_EVT_CLR Register (Offset = 2Ch) [reset = 0h]

Transmit event and error clear register.

Return to Summary Table

Table 3-955. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 002Ch
FSI_TX1	5028 102Ch
FSI_TX2	502A 002Ch
FSI_TX3	502A 102Ch

Figure 3-526. FSI_TX_CFG_TX_EVT_CLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R				W	W	W	W
0h				0h	0h	0h	0h

Table 3-956. FSI_TX_CFG_TX_EVT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	PING_TRIGGERED	W	0h	Ping Frame Triggered Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Note: This bit may not always be cleared when Writing to the corresponding TX_EVT_CLR bit. If PING_TIMEOUT MODE is configured to be 0, a hardware ping timeout may occur when another frame is actively being transmitted. In this case, if this bit still shows as 1 after the clear bit is written then the ping frame has been triggered but not serviced. This bit does not indicate that the ping frame has been completely sent, only that it has been triggered by the timeout event.
2	BUF_OVERRUN	W	0h	Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.
1	BUF_UNDERRUN	W	0h	Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.
0	FRAME_DONE	W	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.

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3.12.2.18 FSI_TX_CFG_TX_EVT_FRC Register

3.12.2.18.1 FSI_TX_CFG_TX_EVT_FRC Register (Offset = 2Eh) [reset = 0h]

Transmit event and error flag force register.

Return to Summary Table

Table 3-957. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 002Eh
FSI_TX1	5028 102Eh
FSI_TX2	502A 002Eh
FSI_TX3	502A 102Eh

Figure 3-527. FSI_TX_CFG_TX_EVT_FRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1				PING_TRIGGERED	BUF_OVERRUN	BUF_UNDERRUN	FRAME_DONE
R				W	W	W	W
0h				0h	0h	0h	0h

Table 3-958. FSI_TX_CFG_TX_EVT_FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	PING_TRIGGERED	W	0h	Ping Frame Triggered Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding flag bit in the TX_EVT_STS Register.
2	BUF_OVERRUN	W	0h	Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[R/W] = Writing a 0 to this bit will have no effect. 1h[R/W] = Force the corresponding flag bit in the TX_EVT_STS Register.
1	BUF_UNDERRUN	W	0h	Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding flag bit in the TX_EVT_STS Register.
0	FRAME_DONE	W	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h[W] = Writing a 0 to this bit will have no effect. 1h[W] = Force the corresponding flag bit in the TX_EVT_STS Register.

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3.12.2.19 FSI_TX_CFG_TX_USER_CRC Register

3.12.2.19.1 FSI_TX_CFG_TX_USER_CRC Register (Offset = 30h) [reset = 0h]

Transmit user-defined CRC register.

Return to Summary Table

Table 3-959. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0030h
FSI_TX1	5028 1030h
FSI_TX2	502A 0030h
FSI_TX3	502A 1030h

Figure 3-528. FSI_TX_CFG_TX_USER_CRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
USER_CRC							
R/W							
0h							

Table 3-960. FSI_TX_CFG_TX_USER_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7:0	USER_CRC	R/W	0h	User-defined CRC This register contains the 8-bit CRC value to be transmitted in the next frame if the transmission is set for user-defined CRC option [TX_OPER_CTRL_LO.SW_CRC = 1]. This register is ignored if the hardware CRC generation is enabled.

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3.12.2.20 FSI_TX_CFG_TX_ECC_DATA Register

3.12.2.20.1 FSI_TX_CFG_TX_ECC_DATA Register (Offset = 40h) [reset = 0h]

Transmit ECC data register.

Return to Summary Table

Table 3-961. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0040h
FSI_TX1	5028 1040h
FSI_TX2	502A 0040h
FSI_TX3	502A 1040h

Figure 3-529. FSI_TX_CFG_TX_ECC_DATA Name Register

31	30	29	28	27	26	25	24
DATA_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_LOW							
R/W							
0h							

Table 3-962. FSI_TX_CFG_TX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA_HIGH	R/W	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register.
15:0	DATA_LOW	R/W	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits.

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3.12.2.21 FSI_TX_CFG_TX_ECC_VAL Register

3.12.2.21.1 FSI_TX_CFG_TX_ECC_VAL Register (Offset = 44h) [reset = Ch]

Transmit ECC value register.

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Table 3-963. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0044h
FSI_TX1	5028 1044h
FSI_TX2	502A 0044h
FSI_TX3	502A 1044h

Figure 3-530. FSI_TX_CFG_TX_ECC_VAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1	ECC_VAL						
R	R						
0h	Ch						

Table 3-964. FSI_TX_CFG_TX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6:0	ECC_VAL	R	Ch	Computed ECC Value This field contains the ECC value computed using SEC-DED either for 16-bit or 32-bit data in the TX_ECC_DATA register.

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3.12.2.22 FSI_TX_CFG_TX_DLYLINE_CTRL Register

3.12.2.22.1 FSI_TX_CFG_TX_DLYLINE_CTRL Register (Offset = 48h) [reset = 0h]

Transmit delay Line control register.

Return to Summary Table

Table 3-965. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0048h
FSI_TX1	5028 1048h
FSI_TX2	502A 0048h
FSI_TX3	502A 1048h

Figure 3-531. FSI_TX_CFG_TX_DLYLINE_CTRL Name Register

15	14	13	12	11	10	9	8
RESERVED_1	TXD1_DLY					TXD0_DLY	
R	R/W					R/W	
0h	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXD0_DLY			TXCLK_DLY				
R/W			R/W				
0h			0h				

Table 3-966. FSI_TX_CFG_TX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:10	TXD1_DLY	R/W	0h	Delay Line Tap Select for TXD1 This bitfield selects the number of delay elements inserted into the TXD1 path from the pin boundary to the receiver core. 0h[R/W] Zero delay elements are included in the TXD1 path. TXD1 is taken directly from the pin. 1h[R/W] One delay element is included in the TXD1 path. 2h[R/W] Two delay elements are included in the TXD1 path. ... 1Fh [R/W] 31 delay elements are included in the TXD1 path, the maximum.
9:5	TXD0_DLY	R/W	0h	Delay Line Tap Select for TXD0 This bitfield selects the number of delay elements inserted into the TXD0 path from the pin boundary to the receiver core. 0h[R/W] Zero delay elements are included in the TXD0 path. TXD0 is taken directly from the pin. 1h[R/W] One delay element is included in the TXD0 path. 2h[R/W] Two delay elements are included in the TXD0 path. ... 1Fh [R/W] 31 delay elements are included in the TXD0 path, the maximum.
4:0	TXCLK_DLY	R/W	0h	Delay Line Tap Select for TXCLK This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core. 0h[R/W] Zero delay elements are included in the TXCLK path. TXCLK is taken directly from the pin. 1h[R/W] One delay element is included in the TXCLK path. 2h[R/W] Two delay elements are included in the TXCLK path. ... 1Fh [R/W] 31 delay elements are included in the TXCLK path, the maximum.

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3.12.2.23 FSI_TX_CFG_TX_BUF_BASE_J Register

3.12.2.23.1 FSI_TX_CFG_TX_BUF_BASE_J Register (Offset = 80h) [reset = 0h]

Base address for transmit buffer.

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Table 3-967. Instance Table

Instance Name	Physical Address
FSI_TX0	5028 0080h + formula
FSI_TX1	5028 1080h + formula
FSI_TX2	502A 0080h + formula
FSI_TX3	502A 1080h + formula

Figure 3-532. FSI_TX_CFG_TX_BUF_BASE_j Name Register

15	14	13	12	11	10	9	8
BASE_ADDRESS							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BASE_ADDRESS							
R/W							
0h							

Table 3-968. FSI_TX_CFG_TX_BUF_BASE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	BASE_ADDRESS	R/W	0h	Transmit Data Buffer Base Address This is the base address of the 16-word data buffer used by the transmitter.

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3.13 RESOLVER

RESOLVER

3.13.1 RESOLVER Summaries

RESOLVER Summaries

Note

1. Resolver registers with names suffixed with "_0" refers to register space for Resolver to Digital Convertor 0 (RDC0).

   The register space for RDC0 is from 502C B030h to 502C B110h
2. Resolver registers with names suffixed with "_1" refers to register space for Resolver to Digital Convertor 1 (RDC1)

   The register space for RDC1 is from 502C B200h to 502C B2E0h
3. Resolver registers without 0/1 suffix are common registers for both RDC0 and RDC1.

Table 3-969. RESOLVER_REGS Registers, Base Address=502C B000h, Length=1024

Offset	Length	Register Name	RESOLVER Physical Address
0h	32	RESOLVER_REGS_REVID	502C B000h
4h	32	RESOLVER_REGS_GLOBAL_CFG	502C B004h
8h	32	RESOLVER_REGS_EXCIT_SAMPLE_CFG1	502C B008h
Ch	32	RESOLVER_REGS_EXCIT_SAMPLE_CFG2	502C B00Ch
10h	32	RESOLVER_REGS_EXCIT_SAMPLE_CFG3	502C B010h
14h	32	RESOLVER_REGS_IRQSTATUS_RAW_SYS	502C B014h
18h	32	RESOLVER_REGS_IRQSTATUS_SYS	502C B018h
1Ch	32	RESOLVER_REGS_IRQENABLE_SET_SYS	502C B01Ch
20h	32	RESOLVER_REGS_IRQENABLE_CLR_SYS	502C B020h
24h	32	RESOLVER_REGS_CAL_CFG	502C B024h
28h	32	RESOLVER_REGS_CAL_OBS	502C B028h
30h	32	RESOLVER_REGS_IRQSTATUS_RAW_SYS_0	502C B030h
34h	32	RESOLVER_REGS_IRQSTATUS_SYS_0	502C B034h
38h	32	RESOLVER_REGS_IRQENABLE_SET_SYS_0	502C B038h
3Ch	32	RESOLVER_REGS_IRQENABLE_CLR_SYS_0	502C B03Ch
40h	32	RESOLVER_REGS_DC_OFF_CFG1_0	502C B040h
44h	32	RESOLVER_REGS_DC_OFF_CFG2_0	502C B044h
48h	32	RESOLVER_REGS_DC_OFF0	502C B048h
4Ch	32	RESOLVER_REGS_SAMPLE_CFG1_0	502C B04Ch
50h	32	RESOLVER_REGS_SAMPLE_CFG2_0	502C B050h
54h	32	RESOLVER_REGS_DEC_GF_CFG0	502C B054h
58h	32	RESOLVER_REGS_PG_EST_CFG1_0	502C B058h
5Ch	32	RESOLVER_REGS_PG_EST_CFG2_0	502C B05Ch
60h	32	RESOLVER_REGS_PG_EST_CFG3_0	502C B060h
64h	32	RESOLVER_REGS_PG_EST_CFG4_0	502C B064h
68h	32	RESOLVER_REGS_PG_EST_CFG5_0	502C B068h
6Ch	32	RESOLVER_REGS_PG_EST_CFG6_0	502C B06Ch
70h	32	RESOLVER_REGS_TRACK2_CFG1_0	502C B070h
74h	32	RESOLVER_REGS_TRACK2_CFG2_0	502C B074h
78h	32	RESOLVER_REGS_TRACK2_CFG3_0	502C B078h

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Table 3-969. RESOLVER_REGS Registers, Base Address=502C B000h, Length=1024 (continued)

Offset	Length	Register Name	RESOLVER Physical Address
7Ch	32	RESOLVER_REGS_ANGLE_ARCTAN_0	502C B07Ch
80h	32	RESOLVER_REGS_ANGLE_TRACK2_0	502C B080h
84h	32	RESOLVER_REGS_VELOCITY_TRACK2_0	502C B084h
88h	32	RESOLVER_REGS_OFFSET_0	502C B088h
98h	32	RESOLVER_REGS_DIAG1_0	502C B098h
9Ch	32	RESOLVER_REGS_DIAG2_0	502C B09Ch
A0h	32	RESOLVER_REGS_DIAG3_0	502C B0A0h
A4h	32	RESOLVER_REGS_DIAG4_0	502C B0A4h
A8h	32	RESOLVER_REGS_DIAG5_0	502C B0A8h
ACh	32	RESOLVER_REGS_DIAG6_0	502C B0ACh
B0h	32	RESOLVER_REGS_DIAG7_0	502C B0B0h
B4h	32	RESOLVER_REGS_DIAG8_0	502C B0B4h
B8h	32	RESOLVER_REGS_DIAG9_0	502C B0B8h
BCh	32	RESOLVER_REGS_DIAG10_0	502C B0BCh
C0h	32	RESOLVER_REGS_DIAG11_0	502C B0C0h
C4h	32	RESOLVER_REGS_DIAG12_0	502C B0C4h
C8h	32	RESOLVER_REGS_DIAG13_0	502C B0C8h
CCh	32	RESOLVER_REGS_DIAG14_0	502C B0CCh
D0h	32	RESOLVER_REGS_DIAG15_0	502C B0D0h
D4h	32	RESOLVER_REGS_DIAG16_0	502C B0D4h
D8h	32	RESOLVER_REGS_DIAG17_0	502C B0D8h
DCh	32	RESOLVER_REGS_DIAG18_0	502C B0DCh
ECh	32	RESOLVER_REGS_OBS_ADC_0	502C B0ECh
F0h	32	RESOLVER_REGS_OBS_ADC_REC_0	502C B0F0h
F4h	32	RESOLVER_REGS_OBS_ADC_DC_0	502C B0F4h
F8h	32	RESOLVER_REGS_OBS_ADC_PGC_0	502C B0F8h
100h	32	RESOLVER_REGS_OBS_PEAKHISTOGRAM3_0_0	502C B100h
104h	32	RESOLVER_REGS_OBS_PEAKHISTOGRAM7_4_0	502C B104h
108h	32	RESOLVER_REGS_OBS_PEAKHISTOGRAM11_8_0	502C B108h
10Ch	32	RESOLVER_REGS_OBS_PEAKHISTOGRAM15_12_0	502C B10Ch
110h	32	RESOLVER_REGS_OBS_PEAKHISTOGRAM19_16_0	502C B110h
200h	32	RESOLVER_REGS_IRQSTATUS_RAW_SYS_1	502C B200h
204h	32	RESOLVER_REGS_IRQSTATUS_SYS_1	502C B204h
208h	32	RESOLVER_REGS_IRQENABLE_SET_SYS_1	502C B208h
20Ch	32	RESOLVER_REGS_IRQENABLE_CLR_SYS_1	502C B20Ch
210h	32	RESOLVER_REGS_DC_OFF_CFG1_1	502C B210h
214h	32	RESOLVER_REGS_DC_OFF_CFG2_1	502C B214h
218h	32	RESOLVER_REGS_DC_OFF1	502C B218h
21Ch	32	RESOLVER_REGS_SAMPLE_CFG1_1	502C B21Ch
220h	32	RESOLVER_REGS_SAMPLE_CFG2_1	502C B220h
224h	32	RESOLVER_REGS_DEC_GF_CFG1	502C B224h
228h	32	RESOLVER_REGS_PG_EST_CFG1_1	502C B228h
22Ch	32	RESOLVER_REGS_PG_EST_CFG2_1	502C B22Ch
230h	32	RESOLVER_REGS_PG_EST_CFG3_1	502C B230h
234h	32	RESOLVER_REGS_PG_EST_CFG4_1	502C B234h
238h	32	RESOLVER_REGS_PG_EST_CFG5_1	502C B238h
23Ch	32	RESOLVER_REGS_PG_EST_CFG6_1	502C B23Ch

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Table 3-969. RESOLVER_REGS Registers, Base Address=502C B000h, Length=1024 (continued)

Offset	Length	Register Name	RESOLVER Physical Address
240h	32	RESOLVER_REGS_TRACK2_CFG1_1	502C B240h
244h	32	RESOLVER_REGS_TRACK2_CFG2_1	502C B244h
248h	32	RESOLVER_REGS_TRACK2_CFG3_1	502C B248h
24Ch	32	RESOLVER_REGS_ANGLE_ARCTAN_1	502C B24Ch
250h	32	RESOLVER_REGS_ANGLE_TRACK2_1	502C B250h
254h	32	RESOLVER_REGS_VELOCITY_TRACK2_1	502C B254h
258h	32	RESOLVER_REGS_OFFSET_1	502C B258h
268h	32	RESOLVER_REGS_DIAG1_1	502C B268h
26Ch	32	RESOLVER_REGS_DIAG2_1	502C B26Ch
270h	32	RESOLVER_REGS_DIAG3_1	502C B270h
274h	32	RESOLVER_REGS_DIAG4_1	502C B274h
278h	32	RESOLVER_REGS_DIAG5_1	502C B278h
27Ch	32	RESOLVER_REGS_DIAG6_1	502C B27Ch
280h	32	RESOLVER_REGS_DIAG7_1	502C B280h
284h	32	RESOLVER_REGS_DIAG8_1	502C B284h
288h	32	RESOLVER_REGS_DIAG9_1	502C B288h
28Ch	32	RESOLVER_REGS_DIAG10_1	502C B28Ch
290h	32	RESOLVER_REGS_DIAG11_1	502C B290h
294h	32	RESOLVER_REGS_DIAG12_1	502C B294h
298h	32	RESOLVER_REGS_DIAG13_1	502C B298h
29Ch	32	RESOLVER_REGS_DIAG14_1	502C B29Ch
2A0h	32	RESOLVER_REGS_DIAG15_1	502C B2A0h
2A4h	32	RESOLVER_REGS_DIAG16_1	502C B2A4h
2A8h	32	RESOLVER_REGS_DIAG17_1	502C B2A8h
2ACh	32	RESOLVER_REGS_DIAG18_1	502C B2ACh
2BCh	32	RESOLVER_REGS_OBS_ADC_1	502C B2BCh
2C0h	32	RESOLVER_REGS_OBS_ADC_REC_1	502C B2C0h
2C4h	32	RESOLVER_REGS_OBS_ADC_DC_1	502C B2C4h
2C8h	32	RESOLVER_REGS_OBS_ADC_PGC_1	502C B2C8h
2D0h	32	RESOLVER_REGS_OBS_PEAKHISTOGRAM3_0_1	502C B2D0h
2D4h	32	RESOLVER_REGS_OBS_PEAKHISTOGRAM7_4_1	502C B2D4h
2D8h	32	RESOLVER_REGS_OBS_PEAKHISTOGRAM11_8_1	502C B2D8h
2DCh	32	RESOLVER_REGS_OBS_PEAKHISTOGRAM15_12_1	502C B2DCh
2E0h	32	RESOLVER_REGS_OBS_PEAKHISTOGRAM19_16_1	502C B2E0h

3.13.2 RESOLVER Registers

RESOLVER Registers

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3.13.2.1 RESOLVER_REGS_REVID Register

3.13.2.1.1 RESOLVER_REGS_REVID Register (Offset = 0h) [reset = 68CF0100h]

The Module and Version Register identifies the module identifier and revision of the RTL module.

Return to Summary Table

Table 3-970. Instance Table

Instance Name	Physical Address
RESOLVER	502C B000h

Figure 3-533. RESOLVER_REGS_REVID Name Register

31	30	29	28	27	26	25	24
REG_MODULE_ID							
R							
68CFh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REG_MODULE_ID							
R							
68CFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REG_RTL_VERSION					REG_MAJOR_REVISION		
R					R		
0h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REG_CUSTOM_REVISION		REG_MINOR_REVISION					
R		R					
0h		0h					

Table 3-971. RESOLVER_REGS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	REG_MODULE_ID	R	68CFh	Resolver module ID
15:11	REG_RTL_VERSION	R	0h	RTL Version.
10:8	REG_MAJOR_REVISION	R	1h	Major Revision.
7:6	REG_CUSTOM_REVISION	R	0h	Custom Revision.
5:0	REG_MINOR_REVISION	R	0h	Minor Revision.

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3.13.2.2 RESOLVER_REGS_GLOBAL_CFG Register

3.13.2.2.1 RESOLVER_REGS_GLOBAL_CFG Register (Offset = 4h) [reset = 11000h]

Global Configuration.

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Table 3-972. Instance Table

Instance Name	Physical Address
RESOLVER	502C B004h

Figure 3-534. RESOLVER_REGS_GLOBAL_CFG Name Register

31	30	29	28	27	26	25	24
SOC_WIDTH							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BURST_CNT							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			SINGLE_EN	MODE			
NONE			R/W	R/W			
0h			1h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							MASTER_EN
NONE							R/W
0h							0h

Table 3-973. RESOLVER_REGS_GLOBAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SOC_WIDTH	R/W	0h	Extension of Start Of Conversion(SOC) pulse width. Width = 40ns + 20ns*soc_width
23:16	BURST_CNT	R/W	1h	This defines the number of burst per sample, 1 is no burst, 2 is 2 samples which will get avg ect.., only valid values are 1,2,4,8,16, and 32
15:13	RESERVED	NONE	0h	Reserved
12	SINGLE_EN	R/W	1h	1 single adc mode 0 diff adc mode
11:8	MODE	R/W	0h	This defines the mode of the resolver , the user has 6 options to configure
7:1	RESERVED	NONE	0h	Reserved
0	MASTER_EN	R/W	0h	Master Enable must leave disabled when cfg is updated 0:Disabled 1:Enabled When 0 it reset all counters, SM, SEQ, ect..

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3.13.2.3 RESOLVER_REGS_EXCIT_SAMPLE_CFG1 Register

3.13.2.3.1 RESOLVER_REGS_EXCIT_SAMPLE_CFG1 Register (Offset = 8h) [reset = 8C8h]

Excitation and Sample Configuration1.

Return to Summary Table

Table 3-974. Instance Table

Instance Name	Physical Address
RESOLVER	502C B008h

Figure 3-535. RESOLVER_REGS_EXCIT_SAMPLE_CFG1 Name Register

31	30	29	28	27	26	25	24
RESERVED			EXC_FREQ_PHASE_CFG				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EXC_FREQ_PHASE_CFG							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADC_SAMPLE_RATE							
R/W							
8h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXC_FREQ_SEL							
R/W							
C8h							

Table 3-975. RESOLVER_REGS_EXCIT_SAMPLE_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:16	EXC_FREQ_PHASE_CFG	R/W	0h	Defines when to start the 8000counter to the SIN LUT, this is one time per master_en 0 -> 1
15:8	ADC_SAMPLE_RATE	R/W	8h	ADC Over Sample Rate <value> * 2 0 is reserved , 1 = OSR2 .. 16 = OSR32, > 16 is reserved
7:0	EXC_FREQ_SEL	R/W	C8h	Exciter Frequency select <freq *10> * 10, only 200-20k, 100-10k, and 50-5k is valid

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3.13.2.4 RESOLVER_REGS_EXCIT_SAMPLE_CFG2 Register

3.13.2.4.1 RESOLVER_REGS_EXCIT_SAMPLE_CFG2 Register (Offset = Ch) [reset = 1900000h]

Excitation and Sample Configuration2.

Return to Summary Table

Table 3-976. Instance Table

Instance Name	Physical Address
RESOLVER	502C B00Ch

Figure 3-536. RESOLVER_REGS_EXCIT_SAMPLE_CFG2 Name Register

31	30	29	28	27	26	25	24
PWM_SYNC_IN_EVENT	RESERVED	PWM_SYNC_IN_EN	PWM_TO_SOC_DLY_START				
R/W1TC	NONE	R/W	R/W				
0h	0h	0h	190h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWM_TO_SOC_DLY_START							
R/W							
190h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PWM_PHASE_INFO				
NONE			RO				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWM_PHASE_INFO							
RO							
0h							

Table 3-977. RESOLVER_REGS_EXCIT_SAMPLE_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PWM_SYNC_IN_EVENT	R/W1TC	0h	This tells SW we had a pwm_sync_in event after master_en is set, w1tc but new start you must de-assert mater_en to re-arm
30	RESERVED	NONE	0h	Reserved
29	PWM_SYNC_IN_EN	R/W	0h	0 disable 1 enable the pwm_sync_in dep to start soc is
28:16	PWM_TO_SOC_DLY_START	R/W	190h	This delay start of SEQ SOC in steps of 800KHz, this is a one time event per master_en 0 -> 1, first power up needs to be 500uS , so reset state of 400 will hit this
15:13	RESERVED	NONE	0h	Reserved
12:0	PWM_PHASE_INFO	RO	0h	This is the latched value of the last pwm_sync_in risge event

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3.13.2.5 RESOLVER_REGS_EXCIT_SAMPLE_CFG3 Register

3.13.2.5.1 RESOLVER_REGS_EXCIT_SAMPLE_CFG3 Register (Offset = 10h) [reset = EFh]

Excitation and Sample Configuration2.

Return to Summary Table

Table 3-978. Instance Table

Instance Name	Physical Address
RESOLVER	502C B010h

Figure 3-537. RESOLVER_REGS_EXCIT_SAMPLE_CFG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EXC_AMP_CTRL							
R/W							
EFh							

Table 3-979. RESOLVER_REGS_EXCIT_SAMPLE_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EXC_AMP_CTRL	R/W	EFh	Defines the amplitude scale, 249 is 100%, > 250 is res

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3.13.2.6 RESOLVER_REGS_IRQSTATUS_RAW_SYS Register

3.13.2.6.1 RESOLVER_REGS_IRQSTATUS_RAW_SYS Register (Offset = 14h) [reset = 0h]

Interrupt Raw Status Register For Resolver.

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Table 3-980. Instance Table

Instance Name	Physical Address
RESOLVER	502C B014h

Figure 3-538. RESOLVER_REGS_IRQSTATUS_RAW_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SEQ_ERR
NONE							R/W1TS
0h							0h

Table 3-981. RESOLVER_REGS_IRQSTATUS_RAW_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SEQ_ERR	R/W1TS	0h	Raw status of error interrupt for seq_cmp_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.

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3.13.2.7 RESOLVER_REGS_IRQSTATUS_SYS Register

3.13.2.7.1 RESOLVER_REGS_IRQSTATUS_SYS Register (Offset = 18h) [reset = 0h]

Interrupt Status Register For Resolver.

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Table 3-982. Instance Table

Instance Name	Physical Address
RESOLVER	502C B018h

Figure 3-539. RESOLVER_REGS_IRQSTATUS_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SEQ_ERR
NONE							R/W1TC
0h							0h

Table 3-983. RESOLVER_REGS_IRQSTATUS_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SEQ_ERR	R/W1TC	0h	Enabled status of error interrupt for seq_cmp_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.

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3.13.2.8 RESOLVER_REGS_IRQENABLE_SET_SYS Register

3.13.2.8.1 RESOLVER_REGS_IRQENABLE_SET_SYS Register (Offset = 1Ch) [reset = 0h]

Interrupt Enable Set Register For Resolver.

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Table 3-984. Instance Table

Instance Name	Physical Address
RESOLVER	502C B01Ch

Figure 3-540. RESOLVER_REGS_IRQENABLE_SET_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SEQ_ERR
NONE							R/W1TS
0h							0h

Table 3-985. RESOLVER_REGS_IRQENABLE_SET_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SEQ_ERR	R/W1TS	0h	Enable set for seq_cmp_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

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3.13.2.9 RESOLVER_REGS_IRQENABLE_CLR_SYS Register

3.13.2.9.1 RESOLVER_REGS_IRQENABLE_CLR_SYS Register (Offset = 20h) [reset = 0h]

Interrupt Enable Clear Register For Resolver.

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Table 3-986. Instance Table

Instance Name	Physical Address
RESOLVER	502C B020h

Figure 3-541. RESOLVER_REGS_IRQENABLE_CLR_SYS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SEQ_ERR
NONE							R/W1TS
0h							0h

Table 3-987. RESOLVER_REGS_IRQENABLE_CLR_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SEQ_ERR	R/W1TS	0h	Enable clr for seq_cmp_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.

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3.13.2.10 RESOLVER_REGS_CAL_CFG Register

3.13.2.10.1 RESOLVER_REGS_CAL_CFG Register (Offset = 24h) [reset = 0h]

CAL Config.

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Table 3-988. Instance Table

Instance Name	Physical Address
RESOLVER	502C B024h

Figure 3-542. RESOLVER_REGS_CAL_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							CAL_DONE
NONE							R/W1TC
0h							0h
7	6	5	4	3	2	1	0
CAL_CHSEL				RESERVED			CAL_EN
R/W				NONE			R/W
0h				0h			0h

Table 3-989. RESOLVER_REGS_CAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CAL_DONE	R/W1TC	0h	This tells SW CAL data is updated, it will not do a new CAL sample until this is cleared
7:4	CAL_CHSEL	R/W	0h	This defines the ADC channel for ADC0 and ADC1 For 263P bit 4 is reserved To determine correct value per SOC refer to the ADC Spec for that SOC
3:1	RESERVED	NONE	0h	Reserved
0	CAL_EN	R/W	0h	Enable CAL, each wrt of one will start cal, can not start new one until the other is done and done is cleared , to start a new cal just wrt a new one to this mmr

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3.13.2.11 RESOLVER_REGS_CAL_OBS Register

3.13.2.11.1 RESOLVER_REGS_CAL_OBS Register (Offset = 28h) [reset = 0h]

CAL ADC0 and ADC1 Data.

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Table 3-990. Instance Table

Instance Name	Physical Address
RESOLVER	502C B028h

Figure 3-543. RESOLVER_REGS_CAL_OBS Name Register

31	30	29	28	27	26	25	24
CAL_ADC1_DATA							
RO							
0h							
23	22	21	20	19	18	17	16
CAL_ADC1_DATA							
RO							
0h							
15	14	13	12	11	10	9	8
CAL_ADC0_DATA							
RO							
0h							
7	6	5	4	3	2	1	0
CAL_ADC0_DATA							
RO							
0h							

Table 3-991. RESOLVER_REGS_CAL_OBS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CAL_ADC1_DATA	RO	0h	Signed ADC1 Data from CAL channel sample if mode enables ie not mode 1 and mode 2
15:0	CAL_ADC0_DATA	RO	0h	Signed ADC0 Data from CAL channel sample

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3.13.2.12 RESOLVER_REGS_IRQSTATUS_RAW_SYS_0 Register

3.13.2.12.1 RESOLVER_REGS_IRQSTATUS_RAW_SYS_0 Register (Offset = 30h) [reset = 0h]

Interrupt Raw Status Register for Core0.

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Table 3-992. Instance Table

Instance Name	Physical Address
RESOLVER	502C B030h

Figure 3-544. RESOLVER_REGS_IRQSTATUS_RAW_SYS_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRACK_LOCK_ERR0
NONE							R/W1TS
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OFFSETDRIFT_COS_HI_ERR0	OFFSETDRIFT_COS_LO_ERR0	OFFSETDRIFT_SIN_HI_ERR0	OFFSETDRIFT_SIN_LO_ERR0	GAINDRIFT_COS_HI_ERR0	GAINDRIFT_COS_LO_ERR0	GAINDRIFT_SIN_HI_ERR0	GAINDRIFT_SIN_LO_ERR0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASEDRIFT_COS_HI_ERR0	PHASEDRIFT_COS_LO_ERR0	EXCFREQDRIFT_HI_ERR0	EXCFREQDRIFT_COS_LO_ERR0	EXCFREQDRIFT_SIN_LO_ERR0	SIN_POS_ZC_PEAK_MISMATCH_ERR0	SIN_NEG_ZC_PEAK_MISMATCH_ERR0	COS_POS_ZC_PEAK_MISMATCH_ERR0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COS_NEG_ZC_PEAK_MISMATCH_ERR0	SIN_MULTI_ZC_ERROR_ERR0	COS_MULTI_ZC_ERROR_ERR0	SINSQCOSSQ_HI_ERR0	SINSQCOSSQ_LO_ERR0	HIGHAMPLITUDE_SIN_FAULT_ERR0	HIGHAMPLITUDE_COS_FAULT_ERR0	LOWAMPLITUDE_ERR0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-993. RESOLVER_REGS_IRQSTATUS_RAW_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TRACK_LOCK_ERR0	R/W1TS	0h	Raw status of error interrupt for track_lock_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
23	OFFSETDRIFT_COS_HI_ERR0	R/W1TS	0h	Raw status of error interrupt for offsetdrift_cos_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
22	OFFSETDRIFT_COS_LO_ERR0	R/W1TS	0h	Raw status of error interrupt for offsetdrift_cos_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
21	OFFSETDRIFT_SIN_HI_ERR0	R/W1TS	0h	Raw status of error interrupt for offsetdrift_sin_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
20	OFFSETDRIFT_SIN_LO_ERR0	R/W1TS	0h	Raw status of error interrupt for offsetdrift_sin_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
19	GAINDRIFT_COS_HI_ERR0	R/W1TS	0h	Raw status of error interrupt for gaindrift_cos_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
18	GAINDRIFT_COS_LO_ERR0	R/W1TS	0h	Raw status of error interrupt for gaindrift_cos_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
17	GAINDRIFT_SIN_HI_ERR0	R/W1TS	0h	Raw status of error interrupt for gaindrift_sin_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.

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Table 3-993. RESOLVER_REGS_IRQSTATUS_RAW_SYS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	GAINDRIFT_SIN_LO_ERR0	R/W1TS	0h	Raw status of error interrupt for gaindrift_sin_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
15	PHASEDRIFT_COS_HI_ERR0	R/W1TS	0h	Raw status of error interrupt for phasedrift_cos_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
14	PHASEDRIFT_COS_LO_ERR0	R/W1TS	0h	Raw status of error interrupt for phasedrift_cos_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
13	EXCFREQDRIFT_HI_ERR0	R/W1TS	0h	Raw status of error interrupt for excfreqdrift_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
12	EXCFREQDRIFT_COS_LO_ERR0	R/W1TS	0h	Raw status of error interrupt for excfreqdrift_cos_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
11	EXCFREQDRIFT_SIN_LO_ERR0	R/W1TS	0h	Raw status of error interrupt for excfreqdrift_sin_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
10	SIN_POS_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Raw status of error interrupt for sin_pos_zc_peak_mismatch_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
9	SIN_NEG_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Raw status of error interrupt for sin_neg_zc_peak_mismatch_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
8	COS_POS_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Raw status of error interrupt for cos_pos_zc_peak_mismatch_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
7	COS_NEG_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Raw status of error interrupt for cos_neg_zc_peak_mismatch_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
6	SIN_MULTI_ZC_ERROR_ERR0	R/W1TS	0h	Raw status of error interrupt for sin_multi_zc_error_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
5	COS_MULTI_ZC_ERROR_ERR0	R/W1TS	0h	Raw status of error interrupt for cos_multi_zc_error_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
4	SINSQCOSSQ_HI_ERR0	R/W1TS	0h	Raw status of error interrupt for sinsqcossq_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
3	SINSQCOSSQ_LO_ERR0	R/W1TS	0h	Raw status of error interrupt for sinsqcossq_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
2	HIGHAMPLITUDE_SIN_FAULT_ERR0	R/W1TS	0h	Raw status of error interrupt for highamplitude_sin_fault_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
1	HIGHAMPLITUDE_COS_FAULT_ERR0	R/W1TS	0h	Raw status of error interrupt for highamplitude_cos_fault_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
0	LOWAMPLITUDE_ERR0	R/W1TS	0h	Raw status of error interrupt for lowamplitude_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.

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3.13.2.13 RESOLVER_REGS_IRQSTATUS_SYS_0 Register

3.13.2.13.1 RESOLVER_REGS_IRQSTATUS_SYS_0 Register (Offset = 34h) [reset = 0h]

Interrupt Status Register for Core0.

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Table 3-994. Instance Table

Instance Name	Physical Address
RESOLVER	502C B034h

Figure 3-545. RESOLVER_REGS_IRQSTATUS_SYS_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRACK_LOCK_ERR0
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OFFSETDRIFT_COS_HI_ERR0	OFFSETDRIFT_COS_LO_ERR0	OFFSETDRIFT_SIN_HI_ERR0	OFFSETDRIFT_SIN_LO_ERR0	GAINDRIFT_COS_HI_ERR0	GAINDRIFT_COS_LO_ERR0	GAINDRIFT_SIN_HI_ERR0	GAINDRIFT_SIN_LO_ERR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASEDRIFT_COS_HI_ERR0	PHASEDRIFT_COS_LO_ERR0	EXCFREQDRIFT_HI_ERR0	EXCFREQDRIFT_COS_LO_ERR0	EXCFREQDRIFT_SIN_LO_ERR0	SIN_POS_ZC_PEAK_MISMATCH_ERR0	SIN_NEG_ZC_PEAK_MISMATCH_ERR0	COS_POS_ZC_PEAK_MISMATCH_ERR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COS_NEG_ZC_PEAK_MISMATCH_ERR0	SIN_MULTI_ZC_ERROR_ERR0	COS_MULTI_ZC_ERROR_ERR0	SINSQCOSSQ_HI_ERR0	SINSQCOSSQ_LO_ERR0	HIGHAMPLITUDE_SIN_FAULT_ERR0	HIGHAMPLITUDE_COS_FAULT_ERR0	LOWAMPLITUDE_ERR0
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-995. RESOLVER_REGS_IRQSTATUS_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TRACK_LOCK_ERR0	R/W1TC	0h	Enabled status of error interrupt for track_lock_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
23	OFFSETDRIFT_COS_HI_ERR0	R/W1TC	0h	Enabled status of error interrupt for offsetdrift_cos_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
22	OFFSETDRIFT_COS_LO_ERR0	R/W1TC	0h	Enabled status of error interrupt for offsetdrift_cos_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
21	OFFSETDRIFT_SIN_HI_ERR0	R/W1TC	0h	Enabled status of error interrupt for offsetdrift_sin_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
20	OFFSETDRIFT_SIN_LO_ERR0	R/W1TC	0h	Enabled status of error interrupt for offsetdrift_sin_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
19	GAINDRIFT_COS_HI_ERR0	R/W1TC	0h	Enabled status of error interrupt for gaindrift_cos_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.

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Table 3-995. RESOLVER_REGS_IRQSTATUS_SYS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	GAINDRIFT_COS_LO_ERR0	R/W1TC	0h	Enabled status of error interrupt for gaindrift_cos_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
17	GAINDRIFT_SIN_HI_ERR0	R/W1TC	0h	Enabled status of error interrupt for gaindrift_sin_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
16	GAINDRIFT_SIN_LO_ERR0	R/W1TC	0h	Enabled status of error interrupt for gaindrift_sin_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
15	PHASEDRIFT_COS_HI_ERR0	R/W1TC	0h	Enabled status of error interrupt for phasedrift_cos_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
14	PHASEDRIFT_COS_LO_ERR0	R/W1TC	0h	Enabled status of error interrupt for phasedrift_cos_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
13	EXCFREQDRIFT_HI_ERR0	R/W1TC	0h	Enabled status of error interrupt for excfreqdrift_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
12	EXCFREQDRIFT_COS_LO_ERR0	R/W1TC	0h	Enabled status of error interrupt for excfreqdrift_cos_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
11	EXCFREQDRIFT_SIN_LO_ERR0	R/W1TC	0h	Enabled status of error interrupt for excfreqdrift_sin_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
10	SIN_POS_ZC_PEAK_MISMATCH_ERR0	R/W1TC	0h	Enabled status of error interrupt for sin_pos_zc_peak_mismatch_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
9	SIN_NEG_ZC_PEAK_MISMATCH_ERR0	R/W1TC	0h	Enabled status of error interrupt for sin_neg_zc_peak_mismatch_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
8	COS_POS_ZC_PEAK_MISMATCH_ERR0	R/W1TC	0h	Enabled status of error interrupt for cos_pos_zc_peak_mismatch_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
7	COS_NEG_ZC_PEAK_MISMATCH_ERR0	R/W1TC	0h	Enabled status of error interrupt for cos_neg_zc_peak_mismatch_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
6	SIN_MULTI_ZC_ERROR_ERR0	R/W1TC	0h	Enabled status of error interrupt for sin_multi_zc_error_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
5	COS_MULTI_ZC_ERROR_ERR0	R/W1TC	0h	Enabled status of error interrupt for cos_multi_zc_error_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
4	SINSQCOSSQ_HI_ERR0	R/W1TC	0h	Enabled status of error interrupt for sinsqcossq_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
3	SINSQCOSSQ_LO_ERR0	R/W1TC	0h	Enabled status of error interrupt for sinsqcossq_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
2	HIGHAMPLITUDE_SIN_FAULT_ERR0	R/W1TC	0h	Enabled status of error interrupt for highamplitude_sin_fault_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
1	HIGHAMPLITUDE_COS_FAULT_ERR0	R/W1TC	0h	Enabled status of error interrupt for highamplitude_cos_fault_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.

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Table 3-995. RESOLVER_REGS_IRQSTATUS_SYS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOWAMPLITUDE_ERR0	R/W1TC	0h	Enabled status of error interrupt for lowamplitude_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.

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3.13.2.14 RESOLVER_REGS_IRQENABLE_SET_SYS_0 Register

3.13.2.14.1 RESOLVER_REGS_IRQENABLE_SET_SYS_0 Register (Offset = 38h) [reset = 0h]

Interrupt Enable Set Register for Core0.

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Table 3-996. Instance Table

Instance Name	Physical Address
RESOLVER	502C B038h

Figure 3-546. RESOLVER_REGS_IRQENABLE_SET_SYS_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRACK_LOCK_ERR0
NONE							R/W1TS
0h							0h
23	22	21	20	19	18	17	16
OFFSETDRIFT_COS_HI_ERR0	OFFSETDRIFT_COS_LO_ERR0	OFFSETDRIFT_SIN_HI_ERR0	OFFSETDRIFT_SIN_LO_ERR0	GAINDRIFT_COS_HI_ERR0	GAINDRIFT_COS_LO_ERR0	GAINDRIFT_SIN_HI_ERR0	GAINDRIFT_SIN_LO_ERR0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
PHASEDRIFT_COS_HI_ERR0	PHASEDRIFT_COS_LO_ERR0	EXCFREQDRIFT_HI_ERR0	EXCFREQDRIFT_COS_LO_ERR0	EXCFREQDRIFT_SIN_LO_ERR0	SIN_POS_ZC_PEAK_MISMATCH_ERR0	SIN_NEG_ZC_PEAK_MISMATCH_ERR0	COS_POS_ZC_PEAK_MISMATCH_ERR0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
COS_NEG_ZC_PEAK_MISMATCH_ERR0	SIN_MULTI_ZC_ERROR_ERR0	COS_MULTI_ZC_ERROR_ERR0	SINSQCOSSQ_HI_ERR0	SINSQCOSSQ_LO_ERR0	HIGHAMPLITUDE_SIN_FAULT_ERR0	HIGHAMPLITUDE_COS_FAULT_ERR0	LOWAMPLITUDE_ERR0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-997. RESOLVER_REGS_IRQENABLE_SET_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TRACK_LOCK_ERR0	R/W1TS	0h	Enable set for track_lock_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
23	OFFSETDRIFT_COS_HI_ERR0	R/W1TS	0h	Enable set for offsetdrift_cos_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
22	OFFSETDRIFT_COS_LO_ERR0	R/W1TS	0h	Enable set for offsetdrift_cos_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
21	OFFSETDRIFT_SIN_HI_ERR0	R/W1TS	0h	Enable set for offsetdrift_sin_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
20	OFFSETDRIFT_SIN_LO_ERR0	R/W1TS	0h	Enable set for offsetdrift_sin_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
19	GAINDRIFT_COS_HI_ERR0	R/W1TS	0h	Enable set for gaindrift_cos_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

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Table 3-997. RESOLVER_REGS_IRQENABLE_SET_SYS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	GAINDRIFT_COS_LO_ERR0	R/W1TS	0h	Enable set for gaindrift_cos_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
17	GAINDRIFT_SIN_HI_ERR0	R/W1TS	0h	Enable set for gaindrift_sin_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
16	GAINDRIFT_SIN_LO_ERR0	R/W1TS	0h	Enable set for gaindrift_sin_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
15	PHASEDRIFT_COS_HI_ERR0	R/W1TS	0h	Enable set for phasedrift_cos_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
14	PHASEDRIFT_COS_LO_ERR0	R/W1TS	0h	Enable set for phasedrift_cos_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
13	EXCFREQDRIFT_HI_ERR0	R/W1TS	0h	Enable set for excfreqdrift_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
12	EXCFREQDRIFT_COS_LO_ERR0	R/W1TS	0h	Enable set for excfreqdrift_cos_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
11	EXCFREQDRIFT_SIN_LO_ERR0	R/W1TS	0h	Enable set for excfreqdrift_sin_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
10	SIN_POS_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Enable set for sin_pos_zc_peak_mismatch_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
9	SIN_NEG_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Enable set for sin_neg_zc_peak_mismatch_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
8	COS_POS_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Enable set for cos_pos_zc_peak_mismatch_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
7	COS_NEG_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Enable set for cos_neg_zc_peak_mismatch_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
6	SIN_MULTI_ZC_ERROR_ERR0	R/W1TS	0h	Enable set for sin_multi_zc_error_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
5	COS_MULTI_ZC_ERROR_ERR0	R/W1TS	0h	Enable set for cos_multi_zc_error_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
4	SINSQCOSSQ_HI_ERR0	R/W1TS	0h	Enable set for sinsqcossq_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
3	SINSQCOSSQ_LO_ERR0	R/W1TS	0h	Enable set for sinsqcossq_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
2	HIGHAMPLITUDE_SIN_FAULT_ERR0	R/W1TS	0h	Enable set for highamplitude_sin_fault_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
1	HIGHAMPLITUDE_COS_FAULT_ERR0	R/W1TS	0h	Enable set for highamplitude_cos_fault_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
0	LOWAMPLITUDE_ERR0	R/W1TS	0h	Enable set for lowamplitude_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

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3.13.2.15 RESOLVER_REGS_IRQENABLE_CLR_SYS_0 Register

3.13.2.15.1 RESOLVER_REGS_IRQENABLE_CLR_SYS_0 Register (Offset = 3Ch) [reset = 0h]

Interrupt Enable Clear Register for Core0.

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Table 3-998. Instance Table

Instance Name	Physical Address
RESOLVER	502C B03Ch

Figure 3-547. RESOLVER_REGS_IRQENABLE_CLR_SYS_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRACK_LOCK_ERR0
NONE							R/W1TS
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OFFSETDRIFT_COS_HI_ERR0	OFFSETDRIFT_COS_LO_ERR0	OFFSETDRIFT_SIN_HI_ERR0	OFFSETDRIFT_SIN_LO_ERR0	GAINDRIFT_COS_HI_ERR0	GAINDRIFT_COS_LO_ERR0	GAINDRIFT_SIN_HI_ERR0	GAINDRIFT_SIN_LO_ERR0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASEDRIFT_COS_HI_ERR0	PHASEDRIFT_COS_LO_ERR0	EXCFREQDRIFT_HI_ERR0	EXCFREQDRIFT_COS_LO_ERR0	EXCFREQDRIFT_SIN_LO_ERR0	SIN_POS_ZC_PEAK_MISMATCH_ERR0	SIN_NEG_ZC_PEAK_MISMATCH_ERR0	COS_POS_ZC_PEAK_MISMATCH_ERR0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COS_NEG_ZC_PEAK_MISMATCH_ERR0	SIN_MULTI_ZC_ERROR_ERR0	COS_MULTI_ZC_ERROR_ERR0	SINSQCOSSQ_HI_ERR0	SINSQCOSSQ_LO_ERR0	HIGHAMPLITUDE_SIN_FAULT_ERR0	HIGHAMPLITUDE_COS_FAULT_ERR0	LOWAMPLITUDE_ERR0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-999. RESOLVER_REGS_IRQENABLE_CLR_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TRACK_LOCK_ERR0	R/W1TS	0h	Enable clr for track_lock_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
23	OFFSETDRIFT_COS_HI_ERR0	R/W1TS	0h	Enable clr for offsetdrift_cos_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
22	OFFSETDRIFT_COS_LO_ERR0	R/W1TS	0h	Enable clr for offsetdrift_cos_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
21	OFFSETDRIFT_SIN_HI_ERR0	R/W1TS	0h	Enable clr for offsetdrift_sin_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
20	OFFSETDRIFT_SIN_LO_ERR0	R/W1TS	0h	Enable clr for offsetdrift_sin_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
19	GAINDRIFT_COS_HI_ERR0	R/W1TS	0h	Enable clr for gaindrift_cos_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.

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Table 3-999. RESOLVER_REGS_IRQENABLE_CLR_SYS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	GAINDRIFT_COS_LO_ERR0	R/W1TS	0h	Enable clr for gaindrift_cos_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
17	GAINDRIFT_SIN_HI_ERR0	R/W1TS	0h	Enable clr for gaindrift_sin_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
16	GAINDRIFT_SIN_LO_ERR0	R/W1TS	0h	Enable clr for gaindrift_sin_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
15	PHASEDRIFT_COS_HI_ERR0	R/W1TS	0h	Enable clr for phasedrift_cos_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
14	PHASEDRIFT_COS_LO_ERR0	R/W1TS	0h	Enable clr for phasedrift_cos_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
13	EXCFREQDRIFT_HI_ERR0	R/W1TS	0h	Enable clr for excfreqdrift_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
12	EXCFREQDRIFT_COS_LO_ERR0	R/W1TS	0h	Enable clr for excfreqdrift_cos_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
11	EXCFREQDRIFT_SIN_LO_ERR0	R/W1TS	0h	Enable clr for excfreqdrift_sin_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
10	SIN_POS_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Enable clr for sin_pos_zc_peak_mismatch_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
9	SIN_NEG_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Enable clr for sin_neg_zc_peak_mismatch_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
8	COS_POS_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Enable clr for cos_pos_zc_peak_mismatch_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
7	COS_NEG_ZC_PEAK_MISMATCH_ERR0	R/W1TS	0h	Enable clr for cos_neg_zc_peak_mismatch_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
6	SIN_MULTI_ZC_ERROR_ERR0	R/W1TS	0h	Enable clr for sin_multi_zc_error_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
5	COS_MULTI_ZC_ERROR_ERR0	R/W1TS	0h	Enable clr for cos_multi_zc_error_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
4	SINSQCOSSQ_HI_ERR0	R/W1TS	0h	Enable clr for sinsqcossq_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
3	SINSQCOSSQ_LO_ERR0	R/W1TS	0h	Enable clr for sinsqcossq_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
2	HIGHAMPLITUDE_SIN_FAULT_ERR0	R/W1TS	0h	Enable clr for highamplitude_sin_fault_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
1	HIGHAMPLITUDE_COS_FAULT_ERR0	R/W1TS	0h	Enable clr for highamplitude_cos_fault_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
0	LOWAMPLITUDE_ERR0	R/W1TS	0h	Enable clr for lowamplitude_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.

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3.13.2.16 RESOLVER_REGS_DC_OFF_CFG1_0 Register

3.13.2.16.1 RESOLVER_REGS_DC_OFF_CFG1_0 Register (Offset = 40h) [reset = A000h]

DC Offset Config1.

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Table 3-1000. Instance Table

Instance Name	Physical Address
RESOLVER	502C B040h

Figure 3-548. RESOLVER_REGS_DC_OFF_CFG1_0 Name Register

31	30	29	28	27	26	25	24
OFF_CAL_COEF2				OFF_CAL_COEF1			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FILTORDER				RESERVED			BANDPASSFILTER_ON
R/W				NONE			R/W
Ah				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_HYSTERESIS				OFFSET_CORR_ON	RESERVED	COS_AUTO_OFFSET_EN	SIN_AUTO_OFFSET_EN
R/W				R/W	NONE	R/W	R/W
0h				0h	0h	0h	0h

Table 3-1001. RESOLVER_REGS_DC_OFF_CFG1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	OFF_CAL_COEF2	R/W	0h	Offset calibration coefficient2 dc offset
27:24	OFF_CAL_COEF1	R/W	0h	Offset calibration coefficient1 dc offset
23:16	RESERVED	NONE	0h	Reserved
15:12	FILTORDER	R/W	Ah	NOT USED
11:9	RESERVED	NONE	0h	Reserved
8	BANDPASSFILTER_ON	R/W	0h	To enable the bandpass filter before DC offset logix
7:4	OFFSET_HYSTERESIS	R/W	0h	unsigned. Absolute hysteresis limit. 4b(no decimal points) with the 16bLSB, ADC data coming 16bto the resolver
3	OFFSET_CORR_ON	R/W	0h	DC Offset Correction On
2	RESERVED	NONE	0h	Reserved
1	COS_AUTO_OFFSET_EN	R/W	0h	NOT_USED
0	SIN_AUTO_OFFSET_EN	R/W	0h	NOT USED

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3.13.2.17 RESOLVER_REGS_DC_OFF_CFG2_0 Register

3.13.2.17.1 RESOLVER_REGS_DC_OFF_CFG2_0 Register (Offset = 44h) [reset = 0h]

DC Offset Config2.

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Table 3-1002. Instance Table

Instance Name	Physical Address
RESOLVER	502C B044h

Figure 3-549. RESOLVER_REGS_DC_OFF_CFG2_0 Name Register

31	30	29	28	27	26	25	24
COS_MAN_OFF_ADJ							
R/W							
0h							
23	22	21	20	19	18	17	16
COS_MAN_OFF_ADJ							
R/W							
0h							
15	14	13	12	11	10	9	8
SIN_MAN_OFF_ADJ							
R/W							
0h							
7	6	5	4	3	2	1	0
SIN_MAN_OFF_ADJ							
R/W							
0h							

Table 3-1003. RESOLVER_REGS_DC_OFF_CFG2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_MAN_OFF_ADJ	R/W	0h	Signed Cos manual dc offset
15:0	SIN_MAN_OFF_ADJ	R/W	0h	Signed Sin manual dc offset

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3.13.2.18 RESOLVER_REGS_DC_OFF0 Register

3.13.2.18.1 RESOLVER_REGS_DC_OFF0 Register (Offset = 48h) [reset = 0h]

DC Offset.

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Table 3-1004. Instance Table

Instance Name	Physical Address
RESOLVER	502C B048h

Figure 3-550. RESOLVER_REGS_DC_OFF0 Name Register

31	30	29	28	27	26	25	24
COS_OFFSET							
RO							
0h							
23	22	21	20	19	18	17	16
COS_OFFSET							
RO							
0h							
15	14	13	12	11	10	9	8
SIN_OFFSET							
RO							
0h							
7	6	5	4	3	2	1	0
SIN_OFFSET							
RO							
0h							

Table 3-1005. RESOLVER_REGS_DC_OFF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_OFFSET	RO	0h	Signed Cos auto dc offset
15:0	SIN_OFFSET	RO	0h	Signed Sin auto dc offset

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3.13.2.19 RESOLVER_REGS_SAMPLE_CFG1_0 Register

3.13.2.19.1 RESOLVER_REGS_SAMPLE_CFG1_0 Register (Offset = 4Ch) [reset = 0h]

Ideal Sample Config1.

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Table 3-1006. Instance Table

Instance Name	Physical Address
RESOLVER	502C B04Ch

Figure 3-551. RESOLVER_REGS_SAMPLE_CFG1_0 Name Register

31	30	29	28	27	26	25	24
IDEAL_SAMPLE_TIME_OVR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IDEAL_SAMPLE_TIME							
RO							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PEAK_AVG_LIMIT			RESERVED				
R/W			NONE				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 3-1007. RESOLVER_REGS_SAMPLE_CFG1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IDEAL_SAMPLE_TIME_OVR	R/W	0h	Ideal sample count Override
23:16	IDEAL_SAMPLE_TIME	RO	0h	Current Ideal sample count, round down
15:13	PEAK_AVG_LIMIT	R/W	0h	2^n peakaveragelimit is how many times to average the ideal peak point: 0 to 7
12:0	RESERVED	NONE	0h	Reserved

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3.13.2.20 RESOLVER_REGS_SAMPLE_CFG2_0 Register

3.13.2.20.1 RESOLVER_REGS_SAMPLE_CFG2_0 Register (Offset = 50h) [reset = A00h]

Ideal Sample Config2.

Return to Summary Table

Table 3-1008. Instance Table

Instance Name	Physical Address
RESOLVER	502C B050h

Figure 3-552. RESOLVER_REGS_SAMPLE_CFG2_0 Name Register

31	30	29	28	27	26	25	24
SAMPLE_DET_THRESHOLD							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SAMPLE_DET_THRESHOLD							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			BANDPASSFILTERSAMPLEADJUST				
NONE			R/W				
0h			Ah				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PEAK_AVG_LIMIT_DONE
NONE							R/W1TC
0h							0h

Table 3-1009. RESOLVER_REGS_SAMPLE_CFG2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SAMPLE_DET_THRESHOLD	R/W	0h	Abs value, the sig needs to be above to trigger the peak detect
15:13	RESERVED	NONE	0h	Reserved
12:8	BANDPASSFILTERSAMPLEADJUST	R/W	Ah	Offset compensate the ideal phase time selection if bpass filter enabled note when you are in manual mode, this value is not longer added
7:1	RESERVED	NONE	0h	Reserved
0	PEAK_AVG_LIMIT_DONE	R/W1TC	0h	Ideal sample count training completed, Wrt 1 to Clr

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3.13.2.21 RESOLVER_REGS_DEC_GF_CFG0 Register

3.13.2.21.1 RESOLVER_REGS_DEC_GF_CFG0 Register (Offset = 54h) [reset = 0h]

Dec GF Config.

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Table 3-1010. Instance Table

Instance Name	Physical Address
RESOLVER	502C B054h

Figure 3-553. RESOLVER_REGS_DEC_GF_CFG0 Name Register

31	30	29	28	27	26	25	24
RESERVED					IDEAL_SAMPLE_MODE		ENABLE_BOTTOM
NONE					R/W		R/W
0h					0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				NOISE_THRESHOLD			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOISE_THRESHOLD							
R/W							
0h							

Table 3-1011. RESOLVER_REGS_DEC_GF_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:25	IDEAL_SAMPLE_MODE	R/W	0h	Ideal sample time detection: 0 autodetect, 1 detect on sin channel 2 on cos channel 3 manual
24	ENABLE_BOTTOM	R/W	0h	This enables bottom wave to get used in the avg
23:12	RESERVED	NONE	0h	Reserved
11:0	NOISE_THRESHOLD	R/W	0h	Abs value, if above use the current moving avg, drop the new data

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3.13.2.22 RESOLVER_REGS_PG_EST_CFG1_0 Register

3.13.2.22.1 RESOLVER_REGS_PG_EST_CFG1_0 Register (Offset = 58h) [reset = 0h]

Phase and Gain Est for correction block Config1.

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Table 3-1012. Instance Table

Instance Name	Physical Address
RESOLVER	502C B058h

Figure 3-554. RESOLVER_REGS_PG_EST_CFG1_0 Name Register

31	30	29	28	27	26	25	24
AGC_FILTER_COEF2				AGC_FILTER_COEF1			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							AUTOPHASEGAINREADYDONE
NONE							R/W1TC
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASEFILTCOEFF				PG_TRAIN_LIMIT			
R/W				R/W			
0h				0h			

Table 3-1013. RESOLVER_REGS_PG_EST_CFG1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	AGC_FILTER_COEF2	R/W	0h	NOT USED
27:24	AGC_FILTER_COEF1	R/W	0h	NOT USED
23:17	RESERVED	NONE	0h	Reserved
16	AUTOPHASEGAINREADYDONE	R/W1TC	0h	Status of Auto Gain and Phase Est , set when ready for each cycle , wrt 1 to clear, this has no effect to the correction logic
15:8	RESERVED	NONE	0h	Reserved
7:4	PHASEFILTCOEFF	R/W	0h	NOT USED
3:0	PG_TRAIN_LIMIT	R/W	0h	^n pg_train_limit : 0 to 15

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3.13.2.23 RESOLVER_REGS_PG_EST_CFG2_0 Register

3.13.2.23.1 RESOLVER_REGS_PG_EST_CFG2_0 Register (Offset = 5Ch) [reset = 0h]

Phase and Gain Est for correction block Config2.

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Table 3-1014. Instance Table

Instance Name	Physical Address
RESOLVER	502C B05Ch

Figure 3-555. RESOLVER_REGS_PG_EST_CFG2_0 Name Register

31	30	29	28	27	26	25	24
PHASECOSBYP0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHASECOSBYP0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				BYPASSPHASEGAINCORR0	AUTOPHASECONTROL0	AUTOGAINCONTROL0	RESERVED
NONE				R/W	R/W	R/W	NONE
0h				0h	0h	0h	0h

Table 3-1015. RESOLVER_REGS_PG_EST_CFG2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHASECOSBYP0	R/W	0h	Manual Phase Cos correction value
15:4	RESERVED	NONE	0h	Reserved
3	BYPASSPHASEGAINCORR0	R/W	0h	Enables phase and gain est
2	AUTOPHASECONTROL0	R/W	0h	Enable Auto Phase correction
1	AUTOGAINCONTROL0	R/W	0h	Enable Auto Gain correction
0	RESERVED	NONE	0h	Reserved

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3.13.2.24 RESOLVER_REGS_PG_EST_CFG3_0 Register

3.13.2.24.1 RESOLVER_REGS_PG_EST_CFG3_0 Register (Offset = 60h) [reset = 0h]

Phase and Gain Est for correction block Config3.

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Table 3-1016. Instance Table

Instance Name	Physical Address
RESOLVER	502C B060h

Figure 3-556. RESOLVER_REGS_PG_EST_CFG3_0 Name Register

31	30	29	28	27	26	25	24
GAINCOSBYP0							
R/W							
0h							
23	22	21	20	19	18	17	16
GAINCOSBYP0							
R/W							
0h							
15	14	13	12	11	10	9	8
GAINSINBYP0							
R/W							
0h							
7	6	5	4	3	2	1	0
GAINSINBYP0							
R/W							
0h							

Table 3-1017. RESOLVER_REGS_PG_EST_CFG3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	GAINCOSBYP0	R/W	0h	Manual Gain Cos correction value
15:0	GAINSINBYP0	R/W	0h	Manual Gain Sin correction value, always pos

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3.13.2.25 RESOLVER_REGS_PG_EST_CFG4_0 Register

3.13.2.25.1 RESOLVER_REGS_PG_EST_CFG4_0 Register (Offset = 64h) [reset = 4000h]

Phase and Gain Est for correction block Config4.

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Table 3-1018. Instance Table

Instance Name	Physical Address
RESOLVER	502C B064h

Figure 3-557. RESOLVER_REGS_PG_EST_CFG4_0 Name Register

31	30	29	28	27	26	25	24
PHASEESTIMATEFINAL							
RO							
0h							
23	22	21	20	19	18	17	16
PHASEESTIMATEFINAL							
RO							
0h							
15	14	13	12	11	10	9	8
PG_GLITCHTHRESHOLD							
R/W							
4000h							
7	6	5	4	3	2	1	0
PG_GLITCHTHRESHOLD							
R/W							
4000h							

Table 3-1019. RESOLVER_REGS_PG_EST_CFG4_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHASEESTIMATEFINAL	RO	0h	Cos Auto Cal Phase correction value cal by est
15:0	PG_GLITCHTHRESHOLD	R/W	4000h	glitch threshold to estimate new rotation start in degrees

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3.13.2.26 RESOLVER_REGS_PG_EST_CFG5_0 Register

3.13.2.26.1 RESOLVER_REGS_PG_EST_CFG5_0 Register (Offset = 68h) [reset = 0h]

Phase and Gain Est for correction block Config5.

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Table 3-1020. Instance Table

Instance Name	Physical Address
RESOLVER	502C B068h

Figure 3-558. RESOLVER_REGS_PG_EST_CFG5_0 Name Register

31	30	29	28	27	26	25	24
COSSQACCFINAL0							
RO							
0h							
23	22	21	20	19	18	17	16
COSSQACCFINAL0							
RO							
0h							
15	14	13	12	11	10	9	8
COSSQACCFINAL0							
RO							
0h							
7	6	5	4	3	2	1	0
COSSQACCFINAL0							
RO							
0h							

Table 3-1021. RESOLVER_REGS_PG_EST_CFG5_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSSQACCFINAL0	RO	0h	Cos Auto Cal Gain correction value cal by est

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3.13.2.27 RESOLVER_REGS_PG_EST_CFG6_0 Register

3.13.2.27.1 RESOLVER_REGS_PG_EST_CFG6_0 Register (Offset = 6Ch) [reset = 0h]

Phase and Gain Est for correction block Config6.

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Table 3-1022. Instance Table

Instance Name	Physical Address
RESOLVER	502C B06Ch

Figure 3-559. RESOLVER_REGS_PG_EST_CFG6_0 Name Register

31	30	29	28	27	26	25	24
SINSQACCFINAL0							
RO							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SINSQACCFINAL0							
RO							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SINSQACCFINAL0							
RO							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SINSQACCFINAL0							
RO							
0h							

Table 3-1023. RESOLVER_REGS_PG_EST_CFG6_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINSQACCFINAL0	RO	0h	Sin Auto Cal Gain correction value cal by est

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3.13.2.28 RESOLVER_REGS_TRACK2_CFG1_0 Register

3.13.2.28.1 RESOLVER_REGS_TRACK2_CFG1_0 Register (Offset = 70h) [reset = 5003C00h]

Track2 Kp, Ki, Kd, Kvelfilt, Kffw, Boost Cfg1 .

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Table 3-1024. Instance Table

Instance Name	Physical Address
RESOLVER	502C B070h

Figure 3-560. RESOLVER_REGS_TRACK2_CFG1_0 Name Register

31	30	29	28	27	26	25	24
KVELFILT							
R/W							
5h							
23	22	21	20	19	18	17	16
KD							
R/W							
0h							
15	14	13	12	11	10	9	8
KI							
R/W							
3Ch							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 3-1025. RESOLVER_REGS_TRACK2_CFG1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	KVELFILT	R/W	5h	Kvelfilt
23:16	KD	R/W	0h	NOT USED
15:8	KI	R/W	3Ch	Ki
7:0	RESERVED	NONE	0h	Reserved

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3.13.2.29 RESOLVER_REGS_TRACK2_CFG2_0 Register

3.13.2.29.1 RESOLVER_REGS_TRACK2_CFG2_0 Register (Offset = 74h) [reset = 62h]

Track2 Feed Fwd Boost Kffw Cfg2.

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Table 3-1026. Instance Table

Instance Name	Physical Address
RESOLVER	502C B074h

Figure 3-561. RESOLVER_REGS_TRACK2_CFG2_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				KFFW			
NONE				R/W			
0h				6h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KFFW				RESERVED	EARLYESTIMATE	BOOST	FEED_FWD_CORR
R/W				NONE	R/W	R/W	R/W
6h				0h	0h	1h	0h

Table 3-1027. RESOLVER_REGS_TRACK2_CFG2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:4	KFFW	R/W	6h	Kffw
3	RESERVED	NONE	0h	Reserved
2	EARLYESTIMATE	R/W	0h	NOT USED
1	BOOST	R/W	1h	Boost Enable
0	FEED_FWD_CORR	R/W	0h	NOT USED

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3.13.2.30 RESOLVER_REGS_TRACK2_CFG3_0 Register

3.13.2.30.1 RESOLVER_REGS_TRACK2_CFG3_0 Register (Offset = 78h) [reset = 0h]

Track2 Cfg3.

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Table 3-1028. Instance Table

Instance Name	Physical Address
RESOLVER	502C B078h

Figure 3-562. RESOLVER_REGS_TRACK2_CFG3_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							BOOSTVEL
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
KPDIV							
R/W							
0h							
7	6	5	4	3	2	1	0
VBOOSTCOEFF							
R/W							
0h							

Table 3-1029. RESOLVER_REGS_TRACK2_CFG3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	BOOSTVEL	R/W	0h	0 disables and 1 enables accel/decel compensation for velocity calculation. boost also needs to be 1
23:16	RESERVED	NONE	0h	Reserved
15:8	KPDIV	R/W	0h	Kp proportional path gain
7:0	VBOOSTCOEFF	R/W	0h	unsigned velocity accel/decel comp coefficient

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3.13.2.31 RESOLVER_REGS_ANGLE_ARCTAN_0 Register

3.13.2.31.1 RESOLVER_REGS_ANGLE_ARCTAN_0 Register (Offset = 7Ch) [reset = 0h]

Angle and Velocity from acrtan .

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Table 3-1030. Instance Table

Instance Name	Physical Address
RESOLVER	502C B07Ch

Figure 3-563. RESOLVER_REGS_ANGLE_ARCTAN_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ANGLE							
RO							
0h							
7	6	5	4	3	2	1	0
ANGLE							
RO							
0h							

Table 3-1031. RESOLVER_REGS_ANGLE_ARCTAN_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ANGLE	RO	0h	Signed(2s complement) Angle from arctan -180 to 0 to +180 scaled

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3.13.2.32 RESOLVER_REGS_ANGLE_TRACK2_0 Register

3.13.2.32.1 RESOLVER_REGS_ANGLE_TRACK2_0 Register (Offset = 80h) [reset = 0h]

Angle and Velocity from track2.

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Table 3-1032. Instance Table

Instance Name	Physical Address
RESOLVER	502C B080h

Figure 3-564. RESOLVER_REGS_ANGLE_TRACK2_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ANGLE							
RO							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ANGLE							
RO							
0h							

Table 3-1033. RESOLVER_REGS_ANGLE_TRACK2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ANGLE	RO	0h	Signed(2s complement) Angle from track2 -180 to 0 to +180 scaled

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3.13.2.33 RESOLVER_REGS_VELOCITY_TRACK2_0 Register

3.13.2.33.1 RESOLVER_REGS_VELOCITY_TRACK2_0 Register (Offset = 84h) [reset = 0h]

Angle and Velocity from track2.

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Table 3-1034. Instance Table

Instance Name	Physical Address
RESOLVER	502C B084h

Figure 3-565. RESOLVER_REGS_VELOCITY_TRACK2_0 Name Register

31	30	29	28	27	26	25	24
VELOCITY							
RO							
0h							
23	22	21	20	19	18	17	16
VELOCITY							
RO							
0h							
15	14	13	12	11	10	9	8
VELOCITY							
RO							
0h							
7	6	5	4	3	2	1	0
VELOCITY							
RO							
0h							

Table 3-1035. RESOLVER_REGS_VELOCITY_TRACK2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VELOCITY	RO	0h	This register gives rotation frequency as a function of exc freq and double/single sample mode. Formula on matlab comment. (rotation frequency in Hz, signed based on direction) = (velocity) * (1/Ts) * 1/2^32 Note: if its top/bottom sampling, Ts = Texc/2, otherwise Ts=Texc

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3.13.2.34 RESOLVER_REGS_OFFSET_0 Register

3.13.2.34.1 RESOLVER_REGS_OFFSET_0 Register (Offset = 88h) [reset = 0h]

SIN and COS Offset.

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Table 3-1036. Instance Table

Instance Name	Physical Address
RESOLVER	502C B088h

Figure 3-566. RESOLVER_REGS_OFFSET_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 3-1037. RESOLVER_REGS_OFFSET_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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3.13.2.35 RESOLVER_REGS_DIAG1_0 Register

3.13.2.35.1 RESOLVER_REGS_DIAG1_0 Register (Offset = 98h) [reset = 0h]

Diag1 0

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Table 3-1038. Instance Table

Instance Name	Physical Address
RESOLVER	502C B098h

Figure 3-567. RESOLVER_REGS_DIAG1_0 Name Register

31	30	29	28	27	26	25	24
OFFSETDRIFT_THRESHOLD_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
OFFSETDRIFT_THRESHOLD_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
OFFSETDRIFT_THRESHOLD_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
OFFSETDRIFT_THRESHOLD_HI							
R/W							
0h							

Table 3-1039. RESOLVER_REGS_DIAG1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OFFSETDRIFT_THRESHOLD_LO	R/W	0h	Signed Lo threshold to detect offset drift
15:0	OFFSETDRIFT_THRESHOLD_HI	R/W	0h	Signed Hi threshold to detect offsetdrift

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3.13.2.36 RESOLVER_REGS_DIAG2_0 Register

3.13.2.36.1 RESOLVER_REGS_DIAG2_0 Register (Offset = 9Ch) [reset = 0h]

Diag2 0

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Table 3-1040. Instance Table

Instance Name	Physical Address
RESOLVER	502C B09Ch

Figure 3-568. RESOLVER_REGS_DIAG2_0 Name Register

31	30	29	28	27	26	25	24
EXCFREQDETECTED_COS							
RO							
0h							
23	22	21	20	19	18	17	16
EXCFREQDETECTED_COS							
RO							
0h							
15	14	13	12	11	10	9	8
EXCFREQDETECTED_SIN							
RO							
0h							
7	6	5	4	3	2	1	0
EXCFREQDETECTED_SIN							
RO							
0h							

Table 3-1041. RESOLVER_REGS_DIAG2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	EXCFREQDETECTED_COS	RO	0h	SW OBS Counts detected between zcs for cos excitation frequency
15:0	EXCFREQDETECTED_SIN	RO	0h	SW OBS Counts detected between zcs for sin excitation frequency

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3.13.2.37 RESOLVER_REGS_DIAG3_0 Register

3.13.2.37.1 RESOLVER_REGS_DIAG3_0 Register (Offset = A0h) [reset = 0h]

Diag3 0

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Table 3-1042. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0A0h

Figure 3-569. RESOLVER_REGS_DIAG3_0 Name Register

31	30	29	28	27	26	25	24
EXCFREQDRIFT_THRESHOLD_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
EXCFREQDRIFT_THRESHOLD_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
EXCFREQDRIFT_THRESHOLD_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCFREQDRIFT_THRESHOLD_HI							
R/W							
0h							

Table 3-1043. RESOLVER_REGS_DIAG3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	EXCFREQDRIFT_THRESHOLD_LO	R/W	0h	Lo threshold to detect excfreqdrift
15:0	EXCFREQDRIFT_THRESHOLD_HI	R/W	0h	Hi threshold to detect excfreqdrift

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3.13.2.38 RESOLVER_REGS_DIAG4_0 Register

3.13.2.38.1 RESOLVER_REGS_DIAG4_0 Register (Offset = A4h) [reset = 10000h]

Diag4 0

Return to Summary Table

Table 3-1044. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0A4h

Figure 3-570. RESOLVER_REGS_DIAG4_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
EXCFREQDRIFT_GLITCHCOUNT							
R/W							
1h							
15	14	13	12	11	10	9	8
EXCFREQ_LEVEL							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCFREQ_LEVEL							
R/W							
0h							

Table 3-1045. RESOLVER_REGS_DIAG4_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	EXCFREQDRIFT_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error
15:0	EXCFREQ_LEVEL	R/W	0h	Threshold on ADC value to detect sin or cos zero crossings

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3.13.2.39 RESOLVER_REGS_DIAG5_0 Register

3.13.2.39.1 RESOLVER_REGS_DIAG5_0 Register (Offset = A8h) [reset = 10000h]

Diag5 0

Return to Summary Table

Table 3-1046. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0A8h

Figure 3-571. RESOLVER_REGS_DIAG5_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
LOWAMPLITUDE_GLITCHCOUNT							
R/W							
1h							
15	14	13	12	11	10	9	8
LOWAMPLITUDE_THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
LOWAMPLITUDE_THRESHOLD							
R/W							
0h							

Table 3-1047. RESOLVER_REGS_DIAG5_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	LOWAMPLITUDE_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error
15:0	LOWAMPLITUDE_THRESHOLD	R/W	0h	Hi threshold to detect lowamplitude. Both sin and cos need to be lower than this at the same time

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3.13.2.40 RESOLVER_REGS_DIAG6_0 Register

3.13.2.40.1 RESOLVER_REGS_DIAG6_0 Register (Offset = ACh) [reset = 0h]

Diag6 0

Return to Summary Table

Table 3-1048. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0ACh

Figure 3-572. RESOLVER_REGS_DIAG6_0 Name Register

31	30	29	28	27	26	25	24
LOWAMPLITUDE_COS							
RO							
0h							
23	22	21	20	19	18	17	16
LOWAMPLITUDE_COS							
RO							
0h							
15	14	13	12	11	10	9	8
LOWAMPLITUDE_SIN							
RO							
0h							
7	6	5	4	3	2	1	0
LOWAMPLITUDE_SIN							
RO							
0h							

Table 3-1049. RESOLVER_REGS_DIAG6_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	LOWAMPLITUDE_COS	RO	0h	Value of cos channel at the error trigger instant
15:0	LOWAMPLITUDE_SIN	RO	0h	Value of sin channel at the error trigger instant

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3.13.2.41 RESOLVER_REGS_DIAG7_0 Register

3.13.2.41.1 RESOLVER_REGS_DIAG7_0 Register (Offset = B0h) [reset = 10000h]

Diag7 0

Return to Summary Table

Table 3-1050. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0B0h

Figure 3-573. RESOLVER_REGS_DIAG7_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
HIGHAMPLITUDE_GLITCHCOUNT							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HIGHAMPLITUDE_THRESHOLD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HIGHAMPLITUDE_THRESHOLD							
R/W							
0h							

Table 3-1051. RESOLVER_REGS_DIAG7_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	HIGHAMPLITUDE_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error
15:0	HIGHAMPLITUDE_THRESHOLD	R/W	0h	Hi threshold to detect highamplitude. Both sin and cos need to be higher than this at the same time

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3.13.2.42 RESOLVER_REGS_DIAG8_0 Register

3.13.2.42.1 RESOLVER_REGS_DIAG8_0 Register (Offset = B4h) [reset = 0h]

Diag8 0

Return to Summary Table

Table 3-1052. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0B4h

Figure 3-574. RESOLVER_REGS_DIAG8_0 Name Register

31	30	29	28	27	26	25	24
HIGHAMPLITUDE_COS							
RO							
0h							
23	22	21	20	19	18	17	16
HIGHAMPLITUDE_COS							
RO							
0h							
15	14	13	12	11	10	9	8
HIGHAMPLITUDE_SIN							
RO							
0h							
7	6	5	4	3	2	1	0
HIGHAMPLITUDE_SIN							
RO							
0h							

Table 3-1053. RESOLVER_REGS_DIAG8_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HIGHAMPLITUDE_COS	RO	0h	Value of cos channel at the error trigger instant
15:0	HIGHAMPLITUDE_SIN	RO	0h	Value of sin channel at the error trigger instant

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3.13.2.43 RESOLVER_REGS_DIAG9_0 Register

3.13.2.43.1 RESOLVER_REGS_DIAG9_0 Register (Offset = B8h) [reset = 0h]

Diag9 0

Return to Summary Table

Table 3-1054. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0B8h

Figure 3-575. RESOLVER_REGS_DIAG9_0 Name Register

31	30	29	28	27	26	25	24
SINSQCOSSQ_THRESHOLD_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
SINSQCOSSQ_THRESHOLD_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
SINSQCOSSQ_THRESHOLD_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
SINSQCOSSQ_THRESHOLD_LO							
R/W							
0h							

Table 3-1055. RESOLVER_REGS_DIAG9_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SINSQCOSSQ_THRESHOLD_HI	R/W	0h	High threshold to detect sinsqcossq. Sin^2+Cos^2 s needs to be lower than this
15:0	SINSQCOSSQ_THRESHOLD_LO	R/W	0h	Low threshold to detect sinsqcossq. Sin^2+Cos^2 s needs to be lower than this

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3.13.2.44 RESOLVER_REGS_DIAG10_0 Register

3.13.2.44.1 RESOLVER_REGS_DIAG10_0 Register (Offset = BCh) [reset = 0h]

Diag10 0

Return to Summary Table

Table 3-1056. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0BCh

Figure 3-576. RESOLVER_REGS_DIAG10_0 Name Register

31	30	29	28	27	26	25	24
SINSQCOSSQ_COSSQ							
RO							
0h							
23	22	21	20	19	18	17	16
SINSQCOSSQ_COSSQ							
RO							
0h							
15	14	13	12	11	10	9	8
SINSQCOSSQ_SINSQ							
RO							
0h							
7	6	5	4	3	2	1	0
SINSQCOSSQ_SINSQ							
RO							
0h							

Table 3-1057. RESOLVER_REGS_DIAG10_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SINSQCOSSQ_COSSQ	RO	0h	Actual cossq value on error trigger ether lo or hi triggered, first event
15:0	SINSQCOSSQ_SINSQ	RO	0h	Actual sinsq value on error trigger ether lo or hi triggered, first event

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3.13.2.45 RESOLVER_REGS_DIAG11_0 Register

3.13.2.45.1 RESOLVER_REGS_DIAG11_0 Register (Offset = C0h) [reset = 1h]

Diag11 0

Return to Summary Table

Table 3-1058. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0C0h

Figure 3-577. RESOLVER_REGS_DIAG11_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SINSQCOSSQ_GLITCHCOUNT							
R/W							
1h							

Table 3-1059. RESOLVER_REGS_DIAG11_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	SINSQCOSSQ_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error

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3.13.2.46 RESOLVER_REGS_DIAG12_0 Register

3.13.2.46.1 RESOLVER_REGS_DIAG12_0 Register (Offset = C4h) [reset = 0h]

Diag12 0

Return to Summary Table

Table 3-1060. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0C4h

Figure 3-578. RESOLVER_REGS_DIAG12_0 Name Register

31	30	29	28	27	26	25	24
ROTPEAK_LEVEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ROTPEAK_LEVEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ROTFREQ_LEVEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ROTFREQ_LEVEL							
R/W							
0h							

Table 3-1061. RESOLVER_REGS_DIAG12_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ROTPEAK_LEVEL	R/W	0h	Peak level of rotational sin/cos when other signal is zero crossing
15:0	ROTFREQ_LEVEL	R/W	0h	Zero crossing detection level of rotational sin/cos

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3.13.2.47 RESOLVER_REGS_DIAG13_0 Register

3.13.2.47.1 RESOLVER_REGS_DIAG13_0 Register (Offset = C8h) [reset = 0h]

Diag13 0

Return to Summary Table

Table 3-1062. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0C8h

Figure 3-579. RESOLVER_REGS_DIAG13_0 Name Register

31	30	29	28	27	26	25	24
COS_MULTI_ZC_ERROR_COUNT							
RO							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIN_MULTI_ZC_ERROR_COUNT							
RO							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				COS_NEG_ZC_PEAK_MISMATCH_ERR	COS_POS_ZC_PEAK_MISMATCH_ERR	SIN_NEG_ZC_PEAK_MISMATCH_ERR	SIN_POS_ZC_PEAK_MISMATCH_ERR
NONE				RO	RO	RO	RO
0h				0h	0h	0h	0h

Table 3-1063. RESOLVER_REGS_DIAG13_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	COS_MULTI_ZC_ERROR_COUNT	RO	0h	Status of cos Capture number of faulty zcs
23:16	SIN_MULTI_ZC_ERROR_COUNT	RO	0h	Status of sin Capture number of faulty zcs
15:4	RESERVED	NONE	0h	Reserved
3	COS_NEG_ZC_PEAK_MISMATCH_ERR	RO	0h	During negative cos zero-crossing cos is not + or - peak
2	COS_POS_ZC_PEAK_MISMATCH_ERR	RO	0h	During positive cos zero-croscosg cos is not + or - peak
1	SIN_NEG_ZC_PEAK_MISMATCH_ERR	RO	0h	During negative sin zero-crossing cos is not + or - peak
0	SIN_POS_ZC_PEAK_MISMATCH_ERR	RO	0h	During positive sin zero-crossing cos is not + or - peak

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3.13.2.48 RESOLVER_REGS_DIAG14_0 Register

3.13.2.48.1 RESOLVER_REGS_DIAG14_0 Register (Offset = CCh) [reset = 0h]

Diag14 0

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Table 3-1064. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0CCh

Figure 3-580. RESOLVER_REGS_DIAG14_0 Name Register

31	30	29	28	27	26	25	24
GAINDRIFT_THRESHOLD_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
GAINDRIFT_THRESHOLD_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
GAINDRIFT_THRESHOLD_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
GAINDRIFT_THRESHOLD_HI							
R/W							
0h							

Table 3-1065. RESOLVER_REGS_DIAG14_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	GAINDRIFT_THRESHOLD_LO	R/W	0h	Lo threshold to detect cos_gain drift
15:0	GAINDRIFT_THRESHOLD_HI	R/W	0h	Hi threshold to detect cos_gain drift

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3.13.2.49 RESOLVER_REGS_DIAG15_0 Register

3.13.2.49.1 RESOLVER_REGS_DIAG15_0 Register (Offset = D0h) [reset = 1h]

Diag15 0

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Table 3-1066. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0D0h

Figure 3-581. RESOLVER_REGS_DIAG15_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
GAINDRIFT_GLITCHCOUNT							
R/W							
1h							

Table 3-1067. RESOLVER_REGS_DIAG15_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	GAINDRIFT_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error

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3.13.2.50 RESOLVER_REGS_DIAG16_0 Register

3.13.2.50.1 RESOLVER_REGS_DIAG16_0 Register (Offset = D4h) [reset = 0h]

Diag16 0

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Table 3-1068. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0D4h

Figure 3-582. RESOLVER_REGS_DIAG16_0 Name Register

31	30	29	28	27	26	25	24
PHASEDRIFT_THRESHOLD_LO							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHASEDRIFT_THRESHOLD_LO							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASEDRIFT_THRESHOLD_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASEDRIFT_THRESHOLD_HI							
R/W							
0h							

Table 3-1069. RESOLVER_REGS_DIAG16_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHASEDRIFT_THRESHOLD_LO	R/W	0h	Lo threshold to detect cos phase drift
15:0	PHASEDRIFT_THRESHOLD_HI	R/W	0h	Hi threshold to detect cos phase drift

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3.13.2.51 RESOLVER_REGS_DIAG17_0 Register

3.13.2.51.1 RESOLVER_REGS_DIAG17_0 Register (Offset = D8h) [reset = 1h]

Diag17 0

Return to Summary Table

Table 3-1070. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0D8h

Figure 3-583. RESOLVER_REGS_DIAG17_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PHASEDRIFT_GLITCHCOUNT							
R/W							
1h							

Table 3-1071. RESOLVER_REGS_DIAG17_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PHASEDRIFT_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error

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3.13.2.52 RESOLVER_REGS_DIAG18_0 Register

3.13.2.52.1 RESOLVER_REGS_DIAG18_0 Register (Offset = DCh) [reset = 10000h]

Diag18 0

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Table 3-1072. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0DCh

Figure 3-584. RESOLVER_REGS_DIAG18_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRACK_ERR_GLITCH_TIME							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRACK_ERR_THRESHOLD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRACK_ERR_THRESHOLD							
R/W							
0h							

Table 3-1073. RESOLVER_REGS_DIAG18_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TRACK_ERR_GLITCH_TIME	R/W	1h	NOT USED
15:0	TRACK_ERR_THRESHOLD	R/W	0h	Tracking error treshold

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3.13.2.53 RESOLVER_REGS_OBS_ADC_0 Register

3.13.2.53.1 RESOLVER_REGS_OBS_ADC_0 Register (Offset = ECh) [reset = 0h]

Sw Obs adc data post latch and avg if enabled

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Table 3-1074. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0ECh

Figure 3-585. RESOLVER_REGS_OBS_ADC_0 Name Register

31	30	29	28	27	26	25	24
COS_ADC							
RO							
0h							
23	22	21	20	19	18	17	16
COS_ADC							
RO							
0h							
15	14	13	12	11	10	9	8
SIN_ADC							
RO							
0h							
7	6	5	4	3	2	1	0
SIN_ADC							
RO							
0h							

Table 3-1075. RESOLVER_REGS_OBS_ADC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_ADC	RO	0h	Signed SW Obs adc data post latch and avg if enabled
15:0	SIN_ADC	RO	0h	Signed SW Obs adc data post latch and avg if enabled

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3.13.2.54 RESOLVER_REGS_OBS_ADC_REC_0 Register

3.13.2.54.1 RESOLVER_REGS_OBS_ADC_REC_0 Register (Offset = F0h) [reset = 0h]

Sw Obs adc data post recovered data, so post dec

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Table 3-1076. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0F0h

Figure 3-586. RESOLVER_REGS_OBS_ADC_REC_0 Name Register

31	30	29	28	27	26	25	24
COS_REC							
RO							
0h							
23	22	21	20	19	18	17	16
COS_REC							
RO							
0h							
15	14	13	12	11	10	9	8
SIN_REC							
RO							
0h							
7	6	5	4	3	2	1	0
SIN_REC							
RO							
0h							

Table 3-1077. RESOLVER_REGS_OBS_ADC_REC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_REC	RO	0h	Signed SW Ob sadc data post recovered data, so post dec
15:0	SIN_REC	RO	0h	Signed SW Obs adc data post recovered data, so post dec

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3.13.2.55 RESOLVER_REGS_OBS_ADC_DC_0 Register

3.13.2.55.1 RESOLVER_REGS_OBS_ADC_DC_0 Register (Offset = F4h) [reset = 0h]

Sw Obs adc data post dc offset.

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Table 3-1078. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0F4h

Figure 3-587. RESOLVER_REGS_OBS_ADC_DC_0 Name Register

31	30	29	28	27	26	25	24
COS_DC							
RO							
0h							
23	22	21	20	19	18	17	16
COS_DC							
RO							
0h							
15	14	13	12	11	10	9	8
SIN_DC							
RO							
0h							
7	6	5	4	3	2	1	0
SIN_DC							
RO							
0h							

Table 3-1079. RESOLVER_REGS_OBS_ADC_DC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_DC	RO	0h	Signed SW Obs adc data post dc offset
15:0	SIN_DC	RO	0h	Signed SW Obs adc data post dc offset

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3.13.2.56 RESOLVER_REGS_OBS_ADC_PGC_0 Register

3.13.2.56.1 RESOLVER_REGS_OBS_ADC_PGC_0 Register (Offset = F8h) [reset = 0h]

Sw Obs post phase and gain correction .

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Table 3-1080. Instance Table

Instance Name	Physical Address
RESOLVER	502C B0F8h

Figure 3-588. RESOLVER_REGS_OBS_ADC_PGC_0 Name Register

31	30	29	28	27	26	25	24
COS_PGC							
RO							
0h							
23	22	21	20	19	18	17	16
COS_PGC							
RO							
0h							
15	14	13	12	11	10	9	8
SIN_PGC							
RO							
0h							
7	6	5	4	3	2	1	0
SIN_PGC							
RO							
0h							

Table 3-1081. RESOLVER_REGS_OBS_ADC_PGC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_PGC	RO	0h	Signed SW Obs adc data post phase and gain correction
15:0	SIN_PGC	RO	0h	Signed SW Obs adc data post phase and gain correction

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3.13.2.57 RESOLVER_REGS_OBS_PEAKHISTOGRAM3_0_0 Register

3.13.2.57.1 RESOLVER_REGS_OBS_PEAKHISTOGRAM3_0_0 Register (Offset = 100h) [reset = 0h]

SW obs peak histogram buckets.

Return to Summary Table

Table 3-1082. Instance Table

Instance Name	Physical Address
RESOLVER	502C B100h

Figure 3-589. RESOLVER_REGS_OBS_PEAKHISTOGRAM3_0_0 Name Register

31	30	29	28	27	26	25	24
PEAKHISTOGRAM3_0							
RO							
0h							
23	22	21	20	19	18	17	16
PEAKHISTOGRAM2_0							
RO							
0h							
15	14	13	12	11	10	9	8
PEAKHISTOGRAM1_0							
RO							
0h							
7	6	5	4	3	2	1	0
PEAKHISTOGRAM0_0							
RO							
0h							

Table 3-1083. RESOLVER_REGS_OBS_PEAKHISTOGRAM3_0_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PEAKHISTOGRAM3_0	RO	0h	Ideal sample bucket3
23:16	PEAKHISTOGRAM2_0	RO	0h	Ideal sample bucket2
15:8	PEAKHISTOGRAM1_0	RO	0h	Ideal sample bucket1
7:0	PEAKHISTOGRAM0_0	RO	0h	Ideal sample bucket0

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3.13.2.58 RESOLVER_REGS_OBS_PEAKHISTOGRAM7_4_0 Register

3.13.2.58.1 RESOLVER_REGS_OBS_PEAKHISTOGRAM7_4_0 Register (Offset = 104h) [reset = 0h]

SW obs peak histogram buckets .

Return to Summary Table

Table 3-1084. Instance Table

Instance Name	Physical Address
RESOLVER	502C B104h

Figure 3-590. RESOLVER_REGS_OBS_PEAKHISTOGRAM7_4_0 Name Register

31	30	29	28	27	26	25	24
PEAKHISTOGRAM7_0							
RO							
0h							
23	22	21	20	19	18	17	16
PEAKHISTOGRAM6_0							
RO							
0h							
15	14	13	12	11	10	9	8
PEAKHISTOGRAM5_0							
RO							
0h							
7	6	5	4	3	2	1	0
PEAKHISTOGRAM4_0							
RO							
0h							

Table 3-1085. RESOLVER_REGS_OBS_PEAKHISTOGRAM7_4_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PEAKHISTOGRAM7_0	RO	0h	Ideal sample bucket7
23:16	PEAKHISTOGRAM6_0	RO	0h	Ideal sample bucket6
15:8	PEAKHISTOGRAM5_0	RO	0h	Ideal sample bucket5
7:0	PEAKHISTOGRAM4_0	RO	0h	Ideal sample bucket4

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3.13.2.59 RESOLVER_REGS_OBS_PEAKHISTOGRAM11_8_0 Register

3.13.2.59.1 RESOLVER_REGS_OBS_PEAKHISTOGRAM11_8_0 Register (Offset = 108h) [reset = 0h]

SW obs peak histogram buckets .

Return to Summary Table

Table 3-1086. Instance Table

Instance Name	Physical Address
RESOLVER	502C B108h

Figure 3-591. RESOLVER_REGS_OBS_PEAKHISTOGRAM11_8_0 Name Register

31	30	29	28	27	26	25	24
PEAKHISTOGRAM11_0							
RO							
0h							
23	22	21	20	19	18	17	16
PEAKHISTOGRAM10_0							
RO							
0h							
15	14	13	12	11	10	9	8
PEAKHISTOGRAM9_0							
RO							
0h							
7	6	5	4	3	2	1	0
PEAKHISTOGRAM8_0							
RO							
0h							

Table 3-1087. RESOLVER_REGS_OBS_PEAKHISTOGRAM11_8_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PEAKHISTOGRAM11_0	RO	0h	Ideal sample bucket11
23:16	PEAKHISTOGRAM10_0	RO	0h	Ideal sample bucket10
15:8	PEAKHISTOGRAM9_0	RO	0h	Ideal sample bucket9
7:0	PEAKHISTOGRAM8_0	RO	0h	Ideal sample bucket8

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3.13.2.60 RESOLVER_REGS_OBS_PEAKHISTOGRAM15_12_0 Register

3.13.2.60.1 RESOLVER_REGS_OBS_PEAKHISTOGRAM15_12_0 Register (Offset = 10Ch) [reset = 0h]

SW obs peak histogram buckets .

Return to Summary Table

Table 3-1088. Instance Table

Instance Name	Physical Address
RESOLVER	502C B10Ch

Figure 3-592. RESOLVER_REGS_OBS_PEAKHISTOGRAM15_12_0 Name Register

31	30	29	28	27	26	25	24
PEAKHISTOGRAM15_0							
RO							
0h							
23	22	21	20	19	18	17	16
PEAKHISTOGRAM14_0							
RO							
0h							
15	14	13	12	11	10	9	8
PEAKHISTOGRAM13_0							
RO							
0h							
7	6	5	4	3	2	1	0
PEAKHISTOGRAM12_0							
RO							
0h							

Table 3-1089. RESOLVER_REGS_OBS_PEAKHISTOGRAM15_12_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PEAKHISTOGRAM15_0	RO	0h	Ideal sample bucket15
23:16	PEAKHISTOGRAM14_0	RO	0h	Ideal sample bucket14
15:8	PEAKHISTOGRAM13_0	RO	0h	Ideal sample bucket13
7:0	PEAKHISTOGRAM12_0	RO	0h	Ideal sample bucket12

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3.13.2.61 RESOLVER_REGS_OBS_PEAKHISTOGRAM19_16_0 Register

3.13.2.61.1 RESOLVER_REGS_OBS_PEAKHISTOGRAM19_16_0 Register (Offset = 110h) [reset = 0h]

SW obs peak histogram buckets .

Return to Summary Table

Table 3-1090. Instance Table

Instance Name	Physical Address
RESOLVER	502C B110h

Figure 3-593. RESOLVER_REGS_OBS_PEAKHISTOGRAM19_16_0 Name Register

31	30	29	28	27	26	25	24
PEAKHISTOGRAM19_0							
RO							
0h							
23	22	21	20	19	18	17	16
PEAKHISTOGRAM18_0							
RO							
0h							
15	14	13	12	11	10	9	8
PEAKHISTOGRAM17_0							
RO							
0h							
7	6	5	4	3	2	1	0
PEAKHISTOGRAM16_0							
RO							
0h							

Table 3-1091. RESOLVER_REGS_OBS_PEAKHISTOGRAM19_16_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PEAKHISTOGRAM19_0	RO	0h	Ideal sample bucket19
23:16	PEAKHISTOGRAM18_0	RO	0h	Ideal sample bucket18
15:8	PEAKHISTOGRAM17_0	RO	0h	Ideal sample bucket17
7:0	PEAKHISTOGRAM16_0	RO	0h	Ideal sample bucket16

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3.13.2.62 RESOLVER_REGS_IRQSTATUS_RAW_SYS_1 Register

3.13.2.62.1 RESOLVER_REGS_IRQSTATUS_RAW_SYS_1 Register (Offset = 200h) [reset = 0h]

Interrupt Raw Status Register for Core1.

Return to Summary Table

Table 3-1092. Instance Table

Instance Name	Physical Address
RESOLVER	502C B200h

Figure 3-594. RESOLVER_REGS_IRQSTATUS_RAW_SYS_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRACK_LOCK_ERR1
NONE							R/W1TS
0h							0h
23	22	21	20	19	18	17	16
OFFSETDRIFT_COS_HI_ERR1	OFFSETDRIFT_COS_LO_ERR1	OFFSETDRIFT_SIN_HI_ERR1	OFFSETDRIFT_SIN_LO_ERR1	GAINDRIFT_COS_HI_ERR1	GAINDRIFT_COS_LO_ERR1	GAINDRIFT_SIN_HI_ERR1	GAINDRIFT_SIN_LO_ERR1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
PHASEDRIFT_COS_HI_ERR1	PHASEDRIFT_COS_LO_ERR1	EXCFREQDRIFT_HI_ERR1	EXCFREQDRIFT_COS_LO_ERR1	EXCFREQDRIFT_SIN_LO_ERR1	SIN_POS_ZC_PEAK_MISMATCH_ERR1	SIN_NEG_ZC_PEAK_MISMATCH_ERR1	COS_POS_ZC_PEAK_MISMATCH_ERR1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
COS_NEG_ZC_PEAK_MISMATCH_ERR1	SIN_MULTI_ZC_ERROR_ERR1	COS_MULTI_ZC_ERROR_ERR1	SINSQCOSSQ_HI_ERR1	SINSQCOSSQ_LO_ERR1	HIGHAMPLITUDE_SIN_FAULT_ERR1	HIGHAMPLITUDE_COS_FAULT_ERR1	LOWAMPLITUDE_ERR1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1093. RESOLVER_REGS_IRQSTATUS_RAW_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TRACK_LOCK_ERR1	R/W1TS	0h	Raw status of error interrupt for track_lock_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
23	OFFSETDRIFT_COS_HI_ERR1	R/W1TS	0h	Raw status of error interrupt for offsetdrift_cos_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
22	OFFSETDRIFT_COS_LO_ERR1	R/W1TS	0h	Raw status of error interrupt for offsetdrift_cos_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
21	OFFSETDRIFT_SIN_HI_ERR1	R/W1TS	0h	Raw status of error interrupt for offsetdrift_sin_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
20	OFFSETDRIFT_SIN_LO_ERR1	R/W1TS	0h	Raw status of error interrupt for offsetdrift_sin_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
19	GAINDRIFT_COS_HI_ERR1	R/W1TS	0h	Raw status of error interrupt for gaindrift_cos_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
18	GAINDRIFT_COS_LO_ERR1	R/W1TS	0h	Raw status of error interrupt for gaindrift_cos_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
17	GAINDRIFT_SIN_HI_ERR1	R/W1TS	0h	Raw status of error interrupt for gaindrift_sin_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.

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Table 3-1093. RESOLVER_REGS_IRQSTATUS_RAW_SYS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	GAINDRIFT_SIN_LO_ERR1	R/W1TS	0h	Raw status of error interrupt for gaindrift_sin_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
15	PHASEDRIFT_COS_HI_ERR1	R/W1TS	0h	Raw status of error interrupt for phasedrift_cos_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
14	PHASEDRIFT_COS_LO_ERR1	R/W1TS	0h	Raw status of error interrupt for phasedrift_cos_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
13	EXCFREQDRIFT_HI_ERR1	R/W1TS	0h	Raw status of error interrupt for excfreqdrift_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
12	EXCFREQDRIFT_COS_LO_ERR1	R/W1TS	0h	Raw status of error interrupt for excfreqdrift_cos_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
11	EXCFREQDRIFT_SIN_LO_ERR1	R/W1TS	0h	Raw status of error interrupt for excfreqdrift_sin_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
10	SIN_POS_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Raw status of error interrupt for sin_pos_zc_peak_mismatch_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
9	SIN_NEG_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Raw status of error interrupt for sin_neg_zc_peak_mismatch_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
8	COS_POS_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Raw status of error interrupt for cos_pos_zc_peak_mismatch_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
7	COS_NEG_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Raw status of error interrupt for cos_neg_zc_peak_mismatch_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
6	SIN_MULTI_ZC_ERROR_ERR1	R/W1TS	0h	Raw status of error interrupt for sin_multi_zc_error_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
5	COS_MULTI_ZC_ERROR_ERR1	R/W1TS	0h	Raw status of error interrupt for cos_multi_zc_error_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
4	SINSQCOSSQ_HI_ERR1	R/W1TS	0h	Raw status of error interrupt for sinsqcossq_hi_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
3	SINSQCOSSQ_LO_ERR1	R/W1TS	0h	Raw status of error interrupt for sinsqcossq_lo_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
2	HIGHAMPLITUDE_SIN_FAULT_ERR1	R/W1TS	0h	Raw status of error interrupt for highamplitude_sin_fault_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
1	HIGHAMPLITUDE_COS_FAULT_ERR1	R/W1TS	0h	Raw status of error interrupt for highamplitude_cos_fault_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
0	LOWAMPLITUDE_ERR1	R/W1TS	0h	Raw status of error interrupt for lowamplitude_err Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.

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3.13.2.63 RESOLVER_REGS_IRQSTATUS_SYS_1 Register

3.13.2.63.1 RESOLVER_REGS_IRQSTATUS_SYS_1 Register (Offset = 204h) [reset = 0h]

Interrupt Status Register for Core1.

Return to Summary Table

Table 3-1094. Instance Table

Instance Name	Physical Address
RESOLVER	502C B204h

Figure 3-595. RESOLVER_REGS_IRQSTATUS_SYS_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRACK_LOCK_ERR1
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OFFSETDRIFT_COS_HI_ERR1	OFFSETDRIFT_COS_LO_ERR1	OFFSETDRIFT_SIN_HI_ERR1	OFFSETDRIFT_SIN_LO_ERR1	GAINDRIFT_COS_HI_ERR1	GAINDRIFT_COS_LO_ERR1	GAINDRIFT_SIN_HI_ERR1	GAINDRIFT_SIN_LO_ERR1
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASEDRIFT_COS_HI_ERR1	PHASEDRIFT_COS_LO_ERR1	EXCFREQDRIFT_HI_ERR1	EXCFREQDRIFT_COS_LO_ERR1	EXCFREQDRIFT_SIN_LO_ERR1	SIN_POS_ZC_PEAK_MISMATCH_ERR1	SIN_NEG_ZC_PEAK_MISMATCH_ERR1	COS_POS_ZC_PEAK_MISMATCH_ERR1
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COS_NEG_ZC_PEAK_MISMATCH_ERR1	SIN_MULTI_ZC_ERROR_ERR1	COS_MULTI_ZC_ERROR_ERR1	SINSQCOSSQ_HI_ERR1	SINSQCOSSQ_LO_ERR1	HIGHAMPLITUDE_SIN_FAULT_ERR1	HIGHAMPLITUDE_COS_FAULT_ERR1	LOWAMPLITUDE_ERR1
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1095. RESOLVER_REGS_IRQSTATUS_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TRACK_LOCK_ERR1	R/W1TC	0h	Enabled status of error interrupt for track_lock_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
23	OFFSETDRIFT_COS_HI_ERR1	R/W1TC	0h	Enabled status of error interrupt for offsetdrift_cos_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
22	OFFSETDRIFT_COS_LO_ERR1	R/W1TC	0h	Enabled status of error interrupt for offsetdrift_cos_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
21	OFFSETDRIFT_SIN_HI_ERR1	R/W1TC	0h	Enabled status of error interrupt for offsetdrift_sin_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
20	OFFSETDRIFT_SIN_LO_ERR1	R/W1TC	0h	Enabled status of error interrupt for offsetdrift_sin_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
19	GAINDRIFT_COS_HI_ERR1	R/W1TC	0h	Enabled status of error interrupt for gaindrift_cos_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.

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Table 3-1095. RESOLVER_REGS_IRQSTATUS_SYS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	GAINDRIFT_COS_LO_ERR1	R/W1TC	0h	Enabled status of error interrupt for gaindrift_cos_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
17	GAINDRIFT_SIN_HI_ERR1	R/W1TC	0h	Enabled status of error interrupt for gaindrift_sin_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
16	GAINDRIFT_SIN_LO_ERR1	R/W1TC	0h	Enabled status of error interrupt for gaindrift_sin_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
15	PHASEDRIFT_COS_HI_ERR1	R/W1TC	0h	Enabled status of error interrupt for phasedrift_cos_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
14	PHASEDRIFT_COS_LO_ERR1	R/W1TC	0h	Enabled status of error interrupt for phasedrift_cos_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
13	EXCFREQDRIFT_HI_ERR1	R/W1TC	0h	Enabled status of error interrupt for excfreqdrift_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
12	EXCFREQDRIFT_COS_LO_ERR1	R/W1TC	0h	Enabled status of error interrupt for excfreqdrift_cos_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
11	EXCFREQDRIFT_SIN_LO_ERR1	R/W1TC	0h	Enabled status of error interrupt for excfreqdrift_sin_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
10	SIN_POS_ZC_PEAK_MISMATCH_ERR1	R/W1TC	0h	Enabled status of error interrupt for sin_pos_zc_peak_mismatch_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
9	SIN_NEG_ZC_PEAK_MISMATCH_ERR1	R/W1TC	0h	Enabled status of error interrupt for sin_neg_zc_peak_mismatch_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
8	COS_POS_ZC_PEAK_MISMATCH_ERR1	R/W1TC	0h	Enabled status of error interrupt for cos_pos_zc_peak_mismatch_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
7	COS_NEG_ZC_PEAK_MISMATCH_ERR1	R/W1TC	0h	Enabled status of error interrupt for cos_neg_zc_peak_mismatch_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
6	SIN_MULTI_ZC_ERROR_ERR1	R/W1TC	0h	Enabled status of error interrupt for sin_multi_zc_error_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
5	COS_MULTI_ZC_ERROR_ERR1	R/W1TC	0h	Enabled status of error interrupt for cos_multi_zc_error_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
4	SINSQCOSSQ_HI_ERR1	R/W1TC	0h	Enabled status of error interrupt for sinsqcossq_hi_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
3	SINSQCOSSQ_LO_ERR1	R/W1TC	0h	Enabled status of error interrupt for sinsqcossq_lo_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
2	HIGHAMPLITUDE_SIN_FAULT_ERR1	R/W1TC	0h	Enabled status of error interrupt for highamplitude_sin_fault_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
1	HIGHAMPLITUDE_COS_FAULT_ERR1	R/W1TC	0h	Enabled status of error interrupt for highamplitude_cos_fault_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.

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Table 3-1095. RESOLVER_REGS_IRQSTATUS_SYS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOWAMPLITUDE_ERR1	R/W1TC	0h	Enabled status of error interrupt for lowamplitude_err Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.

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3.13.2.64 RESOLVER_REGS_IRQENABLE_SET_SYS_1 Register

3.13.2.64.1 RESOLVER_REGS_IRQENABLE_SET_SYS_1 Register (Offset = 208h) [reset = 0h]

Interrupt Enable Set Register for Core1.

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Table 3-1096. Instance Table

Instance Name	Physical Address
RESOLVER	502C B208h

Figure 3-596. RESOLVER_REGS_IRQENABLE_SET_SYS_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRACK_LOCK_ERR1
NONE							R/W1TS
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OFFSETDRIFT_COS_HI_ERR1	OFFSETDRIFT_COS_LO_ERR1	OFFSETDRIFT_SIN_HI_ERR1	OFFSETDRIFT_SIN_LO_ERR1	GAINDRIFT_COS_HI_ERR1	GAINDRIFT_COS_LO_ERR1	GAINDRIFT_SIN_HI_ERR1	GAINDRIFT_SIN_LO_ERR1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASEDRIFT_COS_HI_ERR1	PHASEDRIFT_COS_LO_ERR1	EXCFREQDRIFT_HI_ERR1	EXCFREQDRIFT_COS_LO_ERR1	EXCFREQDRIFT_SIN_LO_ERR1	SIN_POS_ZC_PEAK_MISMATCH_ERR1	SIN_NEG_ZC_PEAK_MISMATCH_ERR1	COS_POS_ZC_PEAK_MISMATCH_ERR1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COS_NEG_ZC_PEAK_MISMATCH_ERR1	SIN_MULTI_ZC_ERROR_ERR1	COS_MULTI_ZC_ERROR_ERR1	SINSQCOSSQ_HI_ERR1	SINSQCOSSQ_LO_ERR1	HIGHAMPLITUDE_SIN_FAULT_ERR1	HIGHAMPLITUDE_COS_FAULT_ERR1	LOWAMPLITUDE_ERR1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1097. RESOLVER_REGS_IRQENABLE_SET_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TRACK_LOCK_ERR1	R/W1TS	0h	Enable set for track_lock_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
23	OFFSETDRIFT_COS_HI_ERR1	R/W1TS	0h	Enable set for offsetdrift_cos_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
22	OFFSETDRIFT_COS_LO_ERR1	R/W1TS	0h	Enable set for offsetdrift_cos_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
21	OFFSETDRIFT_SIN_HI_ERR1	R/W1TS	0h	Enable set for offsetdrift_sin_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
20	OFFSETDRIFT_SIN_LO_ERR1	R/W1TS	0h	Enable set for offsetdrift_sin_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
19	GAINDRIFT_COS_HI_ERR1	R/W1TS	0h	Enable set for gaindrift_cos_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

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Table 3-1097. RESOLVER_REGS_IRQENABLE_SET_SYS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	GAINDRIFT_COS_LO_ERR1	R/W1TS	0h	Enable set for gaindrift_cos_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
17	GAINDRIFT_SIN_HI_ERR1	R/W1TS	0h	Enable set for gaindrift_sin_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
16	GAINDRIFT_SIN_LO_ERR1	R/W1TS	0h	Enable set for gaindrift_sin_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
15	PHASEDRIFT_COS_HI_ERR1	R/W1TS	0h	Enable set for phasedrift_cos_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
14	PHASEDRIFT_COS_LO_ERR1	R/W1TS	0h	Enable set for phasedrift_cos_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
13	EXCFREQDRIFT_HI_ERR1	R/W1TS	0h	Enable set for excfreqdrift_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
12	EXCFREQDRIFT_COS_LO_ERR1	R/W1TS	0h	Enable set for excfreqdrift_cos_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
11	EXCFREQDRIFT_SIN_LO_ERR1	R/W1TS	0h	Enable set for excfreqdrift_sin_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
10	SIN_POS_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Enable set for sin_pos_zc_peak_mismatch_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
9	SIN_NEG_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Enable set for sin_neg_zc_peak_mismatch_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
8	COS_POS_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Enable set for cos_pos_zc_peak_mismatch_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
7	COS_NEG_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Enable set for cos_neg_zc_peak_mismatch_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
6	SIN_MULTI_ZC_ERROR_ERR1	R/W1TS	0h	Enable set for sin_multi_zc_error_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
5	COS_MULTI_ZC_ERROR_ERR1	R/W1TS	0h	Enable set for cos_multi_zc_error_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
4	SINSQCOSSQ_HI_ERR1	R/W1TS	0h	Enable set for sinsqcossq_hi_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
3	SINSQCOSSQ_LO_ERR1	R/W1TS	0h	Enable set for sinsqcossq_lo_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
2	HIGHAMPLITUDE_SIN_FAULT_ERR1	R/W1TS	0h	Enable set for highamplitude_sin_fault_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
1	HIGHAMPLITUDE_COS_FAULT_ERR1	R/W1TS	0h	Enable set for highamplitude_cos_fault_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
0	LOWAMPLITUDE_ERR1	R/W1TS	0h	Enable set for lowamplitude_err . Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

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3.13.2.65 RESOLVER_REGS_IRQENABLE_CLR_SYS_1 Register

3.13.2.65.1 RESOLVER_REGS_IRQENABLE_CLR_SYS_1 Register (Offset = 20Ch) [reset = 0h]

Interrupt Enable Clear Register for Core1.

Return to Summary Table

Table 3-1098. Instance Table

Instance Name	Physical Address
RESOLVER	502C B20Ch

Figure 3-597. RESOLVER_REGS_IRQENABLE_CLR_SYS_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							TRACK_LOCK_ERR1
NONE							R/W1TS
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OFFSETDRIFT_COS_HI_ERR1	OFFSETDRIFT_COS_LO_ERR1	OFFSETDRIFT_SIN_HI_ERR1	OFFSETDRIFT_SIN_LO_ERR1	GAINDRIFT_COS_HI_ERR1	GAINDRIFT_COS_LO_ERR1	GAINDRIFT_SIN_HI_ERR1	GAINDRIFT_SIN_LO_ERR1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASEDRIFT_COS_HI_ERR1	PHASEDRIFT_COS_LO_ERR1	EXCFREQDRIFT_HI_ERR1	EXCFREQDRIFT_COS_LO_ERR1	EXCFREQDRIFT_SIN_LO_ERR1	SIN_POS_ZC_PEAK_MISMATCH_ERR1	SIN_NEG_ZC_PEAK_MISMATCH_ERR1	COS_POS_ZC_PEAK_MISMATCH_ERR1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COS_NEG_ZC_PEAK_MISMATCH_ERR1	SIN_MULTI_ZC_ERROR_ERR1	COS_MULTI_ZC_ERROR_ERR1	SINSQCOSSQ_HI_ERR1	SINSQCOSSQ_LO_ERR1	HIGHAMPLITUDE_SIN_FAULT_ERR1	HIGHAMPLITUDE_COS_FAULT_ERR1	LOWAMPLITUDE_ERR1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1099. RESOLVER_REGS_IRQENABLE_CLR_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TRACK_LOCK_ERR1	R/W1TS	0h	Enable clr for track_lock_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
23	OFFSETDRIFT_COS_HI_ERR1	R/W1TS	0h	Enable clr for offsetdrift_cos_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
22	OFFSETDRIFT_COS_LO_ERR1	R/W1TS	0h	Enable clr for offsetdrift_cos_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
21	OFFSETDRIFT_SIN_HI_ERR1	R/W1TS	0h	Enable clr for offsetdrift_sin_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
20	OFFSETDRIFT_SIN_LO_ERR1	R/W1TS	0h	Enable clr for offsetdrift_sin_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
19	GAINDRIFT_COS_HI_ERR1	R/W1TS	0h	Enable clr for gaindrift_cos_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.

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Table 3-1099. RESOLVER_REGS_IRQENABLE_CLR_SYS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	GAINDRIFT_COS_LO_ERR1	R/W1TS	0h	Enable clr for gaindrift_cos_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
17	GAINDRIFT_SIN_HI_ERR1	R/W1TS	0h	Enable clr for gaindrift_sin_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
16	GAINDRIFT_SIN_LO_ERR1	R/W1TS	0h	Enable clr for gaindrift_sin_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
15	PHASEDRIFT_COS_HI_ERR1	R/W1TS	0h	Enable clr for phasedrift_cos_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
14	PHASEDRIFT_COS_LO_ERR1	R/W1TS	0h	Enable clr for phasedrift_cos_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
13	EXCFREQDRIFT_HI_ERR1	R/W1TS	0h	Enable clr for excfreqdrift_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
12	EXCFREQDRIFT_COS_LO_ERR1	R/W1TS	0h	Enable clr for excfreqdrift_cos_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
11	EXCFREQDRIFT_SIN_LO_ERR1	R/W1TS	0h	Enable clr for excfreqdrift_sin_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
10	SIN_POS_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Enable clr for sin_pos_zc_peak_mismatch_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
9	SIN_NEG_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Enable clr for sin_neg_zc_peak_mismatch_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
8	COS_POS_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Enable clr for cos_pos_zc_peak_mismatch_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
7	COS_NEG_ZC_PEAK_MISMATCH_ERR1	R/W1TS	0h	Enable clr for cos_neg_zc_peak_mismatch_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
6	SIN_MULTI_ZC_ERROR_ERR1	R/W1TS	0h	Enable clr for sin_multi_zc_error_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
5	COS_MULTI_ZC_ERROR_ERR1	R/W1TS	0h	Enable clr for cos_multi_zc_error_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
4	SINSQCOSSQ_HI_ERR1	R/W1TS	0h	Enable clr for sinsqcossq_hi_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
3	SINSQCOSSQ_LO_ERR1	R/W1TS	0h	Enable clr for sinsqcossq_lo_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
2	HIGHAMPLITUDE_SIN_FAULT_ERR1	R/W1TS	0h	Enable clr for highamplitude_sin_fault_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
1	HIGHAMPLITUDE_COS_FAULT_ERR1	R/W1TS	0h	Enable clr for highamplitude_cos_fault_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.
0	LOWAMPLITUDE_ERR1	R/W1TS	0h	Enable clr for lowamplitude_err. Writing a 1 will disable the interrupt, and set this bit as well as the corresponding Interrupt Enable set Register. Writing a 0 has no effect.

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3.13.2.66 RESOLVER_REGS_DC_OFF_CFG1_1 Register

3.13.2.66.1 RESOLVER_REGS_DC_OFF_CFG1_1 Register (Offset = 210h) [reset = A000h]

DC Offset Config1.

Return to Summary Table

Table 3-1100. Instance Table

Instance Name	Physical Address
RESOLVER	502C B210h

Figure 3-598. RESOLVER_REGS_DC_OFF_CFG1_1 Name Register

31	30	29	28	27	26	25	24
OFF_CAL_COEF2				OFF_CAL_COEF1			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FILTORDER				RESERVED			BANDPASSFILTER_ON
R/W				NONE			R/W
Ah				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSET_HYSTERESIS				OFFSET_CORR_ON	RESERVED	COS_AUTO_OFFSET_EN	SIN_AUTO_OFFSET_EN
R/W				R/W	NONE	R/W	R/W
0h				0h	0h	0h	0h

Table 3-1101. RESOLVER_REGS_DC_OFF_CFG1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	OFF_CAL_COEF2	R/W	0h	Offset calibration coefficient2 dc offset
27:24	OFF_CAL_COEF1	R/W	0h	Offset calibration coefficient1 dc offset
23:16	RESERVED	NONE	0h	Reserved
15:12	FILTORDER	R/W	Ah	NOT USED
11:9	RESERVED	NONE	0h	Reserved
8	BANDPASSFILTER_ON	R/W	0h	To enable the bandpass filter before DC offset logix
7:4	OFFSET_HYSTERESIS	R/W	0h	unsigned. Absolute hysteresis limit. 4b(no decimal points) with the 16bLSB, ADC data coming 16bto the resolver
3	OFFSET_CORR_ON	R/W	0h	DC Offset Correction On
2	RESERVED	NONE	0h	Reserved
1	COS_AUTO_OFFSET_EN	R/W	0h	NOT_USED
0	SIN_AUTO_OFFSET_EN	R/W	0h	NOT USED

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3.13.2.67 RESOLVER_REGS_DC_OFF_CFG2_1 Register

3.13.2.67.1 RESOLVER_REGS_DC_OFF_CFG2_1 Register (Offset = 214h) [reset = 0h]

DC Offset Config2.

Return to Summary Table

Table 3-1102. Instance Table

Instance Name	Physical Address
RESOLVER	502C B214h

Figure 3-599. RESOLVER_REGS_DC_OFF_CFG2_1 Name Register

31	30	29	28	27	26	25	24
COS_MAN_OFF_ADJ							
R/W							
0h							
23	22	21	20	19	18	17	16
COS_MAN_OFF_ADJ							
R/W							
0h							
15	14	13	12	11	10	9	8
SIN_MAN_OFF_ADJ							
R/W							
0h							
7	6	5	4	3	2	1	0
SIN_MAN_OFF_ADJ							
R/W							
0h							

Table 3-1103. RESOLVER_REGS_DC_OFF_CFG2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_MAN_OFF_ADJ	R/W	0h	Signed Cos manual dc offset
15:0	SIN_MAN_OFF_ADJ	R/W	0h	Signed Sin manual dc offset

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3.13.2.68 RESOLVER_REGS_DC_OFF1 Register

3.13.2.68.1 RESOLVER_REGS_DC_OFF1 Register (Offset = 218h) [reset = 0h]

DC Offset.

Return to Summary Table

Table 3-1104. Instance Table

Instance Name	Physical Address
RESOLVER	502C B218h

Figure 3-600. RESOLVER_REGS_DC_OFF1 Name Register

31	30	29	28	27	26	25	24
COS_OFFSET							
RO							
0h							
23	22	21	20	19	18	17	16
COS_OFFSET							
RO							
0h							
15	14	13	12	11	10	9	8
SIN_OFFSET							
RO							
0h							
7	6	5	4	3	2	1	0
SIN_OFFSET							
RO							
0h							

Table 3-1105. RESOLVER_REGS_DC_OFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_OFFSET	RO	0h	Signed Cos auto dc offset
15:0	SIN_OFFSET	RO	0h	Signed Sin auto dc offset

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3.13.2.69 RESOLVER_REGS_SAMPLE_CFG1_1 Register

3.13.2.69.1 RESOLVER_REGS_SAMPLE_CFG1_1 Register (Offset = 21Ch) [reset = 0h]

Ideal Sample Config1.

Return to Summary Table

Table 3-1106. Instance Table

Instance Name	Physical Address
RESOLVER	502C B21Ch

Figure 3-601. RESOLVER_REGS_SAMPLE_CFG1_1 Name Register

31	30	29	28	27	26	25	24
IDEAL_SAMPLE_TIME_OVR							
R/W							
0h							
23	22	21	20	19	18	17	16
IDEAL_SAMPLE_TIME							
RO							
0h							
15	14	13	12	11	10	9	8
PEAK_AVG_LIMIT			RESERVED				
R/W			NONE				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 3-1107. RESOLVER_REGS_SAMPLE_CFG1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IDEAL_SAMPLE_TIME_OVR	R/W	0h	Ideal sample count Overide
23:16	IDEAL_SAMPLE_TIME	RO	0h	Current Ideal sample count, round down
15:13	PEAK_AVG_LIMIT	R/W	0h	2^n peakaveragelimit is how many times to average the ideal peak point: 0 to 7
12:0	RESERVED	NONE	0h	Reserved

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3.13.2.70 RESOLVER_REGS_SAMPLE_CFG2_1 Register

3.13.2.70.1 RESOLVER_REGS_SAMPLE_CFG2_1 Register (Offset = 220h) [reset = A00h]

Ideal Sample Config2.

Return to Summary Table

Table 3-1108. Instance Table

Instance Name	Physical Address
RESOLVER	502C B220h

Figure 3-602. RESOLVER_REGS_SAMPLE_CFG2_1 Name Register

31	30	29	28	27	26	25	24
SAMPLE_DET_THRESHOLD							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SAMPLE_DET_THRESHOLD							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			BANDPASSFILTERSAMPLEADJUST				
NONE			R/W				
0h			Ah				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PEAK_AVG_LIMIT_DONE
NONE							R/W1TC
0h							0h

Table 3-1109. RESOLVER_REGS_SAMPLE_CFG2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SAMPLE_DET_THRESHOLD	R/W	0h	Abs value, the sig needs to be above to trigger the peak detect
15:13	RESERVED	NONE	0h	Reserved
12:8	BANDPASSFILTERSAMPLEADJUST	R/W	Ah	Offset compensate the ideal phase time selection if bpass filter enabled note when you are in manual mode, this value is not longer added
7:1	RESERVED	NONE	0h	Reserved
0	PEAK_AVG_LIMIT_DONE	R/W1TC	0h	Ideal sample count training completed, Wrt 1 to Clr

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3.13.2.71 RESOLVER_REGS_DEC_GF_CFG1 Register

3.13.2.71.1 RESOLVER_REGS_DEC_GF_CFG1 Register (Offset = 224h) [reset = 0h]

Dec GF Config.

Return to Summary Table

Table 3-1110. Instance Table

Instance Name	Physical Address
RESOLVER	502C B224h

Figure 3-603. RESOLVER_REGS_DEC_GF_CFG1 Name Register

31	30	29	28	27	26	25	24
RESERVED					IDEAL_SAMPLE_MODE		ENABLE_BOTTOM
NONE					R/W		R/W
0h					0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				NOISE_THRESHOLD			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NOISE_THRESHOLD							
R/W							
0h							

Table 3-1111. RESOLVER_REGS_DEC_GF_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED	NONE	0h	Reserved
26:25	IDEAL_SAMPLE_MODE	R/W	0h	Ideal sample time detection: 0 autodetect, 1 detect on sin channel 2 on cos channel 3 manual
24	ENABLE_BOTTOM	R/W	0h	This enables bottom wave to get used in the avg
23:12	RESERVED	NONE	0h	Reserved
11:0	NOISE_THRESHOLD	R/W	0h	Abs value, if above use the current moving avg, drop the new data

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3.13.2.72 RESOLVER_REGS_PG_EST_CFG1_1 Register

3.13.2.72.1 RESOLVER_REGS_PG_EST_CFG1_1 Register (Offset = 228h) [reset = 0h]

Phase and Gain Est for correction block Config1.

Return to Summary Table

Table 3-1112. Instance Table

Instance Name	Physical Address
RESOLVER	502C B228h

Figure 3-604. RESOLVER_REGS_PG_EST_CFG1_1 Name Register

31	30	29	28	27	26	25	24
AGC_FILTER_COEF2				AGC_FILTER_COEF1			
R/W				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							AUTOPHASEGAINREADYDONE
NONE							R/W1TC
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASEFILTCOEFF				PG_TRAIN_LIMIT			
R/W				R/W			
0h				0h			

Table 3-1113. RESOLVER_REGS_PG_EST_CFG1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	AGC_FILTER_COEF2	R/W	0h	NOT USED
27:24	AGC_FILTER_COEF1	R/W	0h	NOT USED
23:17	RESERVED	NONE	0h	Reserved
16	AUTOPHASEGAINREADYDONE	R/W1TC	0h	Status of Auto Gain and Phase Est , set when ready for each cycle , wrt 1 to clear, this has no effect to the correction logic
15:8	RESERVED	NONE	0h	Reserved
7:4	PHASEFILTCOEFF	R/W	0h	NOT USED
3:0	PG_TRAIN_LIMIT	R/W	0h	^n pg_train_limit : 0 to 15

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3.13.2.73 RESOLVER_REGS_PG_EST_CFG2_1 Register

3.13.2.73.1 RESOLVER_REGS_PG_EST_CFG2_1 Register (Offset = 22Ch) [reset = 0h]

Phase and Gain Est for correction block Config2.

Return to Summary Table

Table 3-1114. Instance Table

Instance Name	Physical Address
RESOLVER	502C B22Ch

Figure 3-605. RESOLVER_REGS_PG_EST_CFG2_1 Name Register

31	30	29	28	27	26	25	24
PHASECOSBYP1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHASECOSBYP1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				BYPASSPHASEGAINCORR1	AUTOPHASECONTROL1	AUTOGAINCONTROL1	RESERVED
NONE				R/W	R/W	R/W	NONE
0h				0h	0h	0h	0h

Table 3-1115. RESOLVER_REGS_PG_EST_CFG2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHASECOSBYP1	R/W	0h	Manual Phase Cos correction value
15:4	RESERVED	NONE	0h	Reserved
3	BYPASSPHASEGAINCORR1	R/W	0h	Enables phase and gain est
2	AUTOPHASECONTROL1	R/W	0h	Enable Auto Phase correction
1	AUTOGAINCONTROL1	R/W	0h	Enable Auto Gain correction
0	RESERVED	NONE	0h	Reserved

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3.13.2.74 RESOLVER_REGS_PG_EST_CFG3_1 Register

3.13.2.74.1 RESOLVER_REGS_PG_EST_CFG3_1 Register (Offset = 230h) [reset = 0h]

Phase and Gain Est for correction block Config3.

Return to Summary Table

Table 3-1116. Instance Table

Instance Name	Physical Address
RESOLVER	502C B230h

Figure 3-606. RESOLVER_REGS_PG_EST_CFG3_1 Name Register

31	30	29	28	27	26	25	24
GAINCOSBYP1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
GAINCOSBYP1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GAINSINBYP1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GAINSINBYP1							
R/W							
0h							

Table 3-1117. RESOLVER_REGS_PG_EST_CFG3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	GAINCOSBYP1	R/W	0h	Manual Gain Cos correction value
15:0	GAINSINBYP1	R/W	0h	Manual Gain Sin correction value, always pos

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3.13.2.75 RESOLVER_REGS_PG_EST_CFG4_1 Register

3.13.2.75.1 RESOLVER_REGS_PG_EST_CFG4_1 Register (Offset = 234h) [reset = 4000h]

Phase and Gain Est for correction block Config4.

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Table 3-1118. Instance Table

Instance Name	Physical Address
RESOLVER	502C B234h

Figure 3-607. RESOLVER_REGS_PG_EST_CFG4_1 Name Register

31	30	29	28	27	26	25	24
PHASEESTIMATEFINAL							
RO							
0h							
23	22	21	20	19	18	17	16
PHASEESTIMATEFINAL							
RO							
0h							
15	14	13	12	11	10	9	8
PG_GLITCHTHRESHOLD							
R/W							
4000h							
7	6	5	4	3	2	1	0
PG_GLITCHTHRESHOLD							
R/W							
4000h							

Table 3-1119. RESOLVER_REGS_PG_EST_CFG4_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHASEESTIMATEFINAL	RO	0h	Cos Auto Cal Phase correction value cal by est
15:0	PG_GLITCHTHRESHOLD	R/W	4000h	glitch threshold to estimate new rotation start in degrees

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3.13.2.76 RESOLVER_REGS_PG_EST_CFG5_1 Register

3.13.2.76.1 RESOLVER_REGS_PG_EST_CFG5_1 Register (Offset = 238h) [reset = 0h]

Phase and Gain Est for correction block Config5.

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Table 3-1120. Instance Table

Instance Name	Physical Address
RESOLVER	502C B238h

Figure 3-608. RESOLVER_REGS_PG_EST_CFG5_1 Name Register

31	30	29	28	27	26	25	24
COSSQACCFINAL1							
RO							
0h							
23	22	21	20	19	18	17	16
COSSQACCFINAL1							
RO							
0h							
15	14	13	12	11	10	9	8
COSSQACCFINAL1							
RO							
0h							
7	6	5	4	3	2	1	0
COSSQACCFINAL1							
RO							
0h							

Table 3-1121. RESOLVER_REGS_PG_EST_CFG5_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSSQACCFINAL1	RO	0h	Cos Auto Cal Gain correction value cal by est

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3.13.2.77 RESOLVER_REGS_PG_EST_CFG6_1 Register

3.13.2.77.1 RESOLVER_REGS_PG_EST_CFG6_1 Register (Offset = 23Ch) [reset = 0h]

Phase and Gain Est for correction block Config6.

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Table 3-1122. Instance Table

Instance Name	Physical Address
RESOLVER	502C B23Ch

Figure 3-609. RESOLVER_REGS_PG_EST_CFG6_1 Name Register

31	30	29	28	27	26	25	24
SINSQACCFINAL1							
RO							
0h							
23	22	21	20	19	18	17	16
SINSQACCFINAL1							
RO							
0h							
15	14	13	12	11	10	9	8
SINSQACCFINAL1							
RO							
0h							
7	6	5	4	3	2	1	0
SINSQACCFINAL1							
RO							
0h							

Table 3-1123. RESOLVER_REGS_PG_EST_CFG6_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINSQACCFINAL1	RO	0h	Sin Auto Cal Gain correction value cal by est

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3.13.2.78 RESOLVER_REGS_TRACK2_CFG1_1 Register

3.13.2.78.1 RESOLVER_REGS_TRACK2_CFG1_1 Register (Offset = 240h) [reset = 5003C00h]

Track2 Kp, Ki, Kd, Kvelfilt, Kffw, Boost Cfg1 .

Return to Summary Table

Table 3-1124. Instance Table

Instance Name	Physical Address
RESOLVER	502C B240h

Figure 3-610. RESOLVER_REGS_TRACK2_CFG1_1 Name Register

31	30	29	28	27	26	25	24
KVELFILT							
R/W							
5h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KD							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KI							
R/W							
3Ch							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 3-1125. RESOLVER_REGS_TRACK2_CFG1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	KVELFILT	R/W	5h	Kvelfilt
23:16	KD	R/W	0h	NOT USED
15:8	KI	R/W	3Ch	Ki
7:0	RESERVED	NONE	0h	Reserved

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3.13.2.79 RESOLVER_REGS_TRACK2_CFG2_1 Register

3.13.2.79.1 RESOLVER_REGS_TRACK2_CFG2_1 Register (Offset = 244h) [reset = 62h]

Track2 Feed Fwd Boost Kffw Cfg2.

Return to Summary Table

Table 3-1126. Instance Table

Instance Name	Physical Address
RESOLVER	502C B244h

Figure 3-611. RESOLVER_REGS_TRACK2_CFG2_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				KFFW			
NONE				R/W			
0h				6h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KFFW				RESERVED	EARLYESTIMATE	BOOST	FEED_FWD_CORR
R/W				NONE	R/W	R/W	R/W
6h				0h	0h	1h	0h

Table 3-1127. RESOLVER_REGS_TRACK2_CFG2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:4	KFFW	R/W	6h	Kffw
3	RESERVED	NONE	0h	Reserved
2	EARLYESTIMATE	R/W	0h	NOT USED
1	BOOST	R/W	1h	Boost Enable
0	FEED_FWD_CORR	R/W	0h	NOT USED

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3.13.2.80 RESOLVER_REGS_TRACK2_CFG3_1 Register

3.13.2.80.1 RESOLVER_REGS_TRACK2_CFG3_1 Register (Offset = 248h) [reset = 0h]

Track2 Cfg3.

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Table 3-1128. Instance Table

Instance Name	Physical Address
RESOLVER	502C B248h

Figure 3-612. RESOLVER_REGS_TRACK2_CFG3_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							BOOSTVEL
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
KPDIV							
R/W							
0h							
7	6	5	4	3	2	1	0
VBOOSTCOEFF							
R/W							
0h							

Table 3-1129. RESOLVER_REGS_TRACK2_CFG3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	BOOSTVEL	R/W	0h	0 disables and 1 enables accel/decel compensation for velocity calculation. boost also needs to be 1
23:16	RESERVED	NONE	0h	Reserved
15:8	KPDIV	R/W	0h	Kp proportional path gain
7:0	VBOOSTCOEFF	R/W	0h	unsigned velocity accel/decel comp coefficient

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3.13.2.81 RESOLVER_REGS_ANGLE_ARCTAN_1 Register

3.13.2.81.1 RESOLVER_REGS_ANGLE_ARCTAN_1 Register (Offset = 24Ch) [reset = 0h]

Angle and Velocity from acrtan .

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Table 3-1130. Instance Table

Instance Name	Physical Address
RESOLVER	502C B24Ch

Figure 3-613. RESOLVER_REGS_ANGLE_ARCTAN_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ANGLE							
RO							
0h							
7	6	5	4	3	2	1	0
ANGLE							
RO							
0h							

Table 3-1131. RESOLVER_REGS_ANGLE_ARCTAN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ANGLE	RO	0h	Signed(2s complement) Angle from arctan -180 to 0 to +180 scaled

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3.13.2.82 RESOLVER_REGS_ANGLE_TRACK2_1 Register

3.13.2.82.1 RESOLVER_REGS_ANGLE_TRACK2_1 Register (Offset = 250h) [reset = 0h]

Angle and Velocity from track2.

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Table 3-1132. Instance Table

Instance Name	Physical Address
RESOLVER	502C B250h

Figure 3-614. RESOLVER_REGS_ANGLE_TRACK2_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ANGLE							
RO							
0h							
7	6	5	4	3	2	1	0
ANGLE							
RO							
0h							

Table 3-1133. RESOLVER_REGS_ANGLE_TRACK2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ANGLE	RO	0h	Signed(2s complement) Angle from track2 -180 to 0 to +180 scaled

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3.13.2.83 RESOLVER_REGS_VELOCITY_TRACK2_1 Register

3.13.2.83.1 RESOLVER_REGS_VELOCITY_TRACK2_1 Register (Offset = 254h) [reset = 0h]

Angle and Velocity from track2.

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Table 3-1134. Instance Table

Instance Name	Physical Address
RESOLVER	502C B254h

Figure 3-615. RESOLVER_REGS_VELOCITY_TRACK2_1 Name Register

31	30	29	28	27	26	25	24
VELOCITY							
RO							
0h							
23	22	21	20	19	18	17	16
VELOCITY							
RO							
0h							
15	14	13	12	11	10	9	8
VELOCITY							
RO							
0h							
7	6	5	4	3	2	1	0
VELOCITY							
RO							
0h							

Table 3-1135. RESOLVER_REGS_VELOCITY_TRACK2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VELOCITY	RO	0h	This register gives rotation frequency as a function of exc freq and double/single sample mode. Formula on matlab comment. (rotation frequency in Hz, signed based on direction) = (velocity) * (1/Ts) * 1/2^32 Note: if its top/bottom sampling, Ts = Texc/2, otherwise Ts=Texc

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3.13.2.84 RESOLVER_REGS_OFFSET_1 Register

3.13.2.84.1 RESOLVER_REGS_OFFSET_1 Register (Offset = 258h) [reset = 0h]

SIN and COS Offset.

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Table 3-1136. Instance Table

Instance Name	Physical Address
RESOLVER	502C B258h

Figure 3-616. RESOLVER_REGS_OFFSET_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 3-1137. RESOLVER_REGS_OFFSET_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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3.13.2.85 RESOLVER_REGS_DIAG1_1 Register

3.13.2.85.1 RESOLVER_REGS_DIAG1_1 Register (Offset = 268h) [reset = 0h]

Diag1 1

Return to Summary Table

Table 3-1138. Instance Table

Instance Name	Physical Address
RESOLVER	502C B268h

Figure 3-617. RESOLVER_REGS_DIAG1_1 Name Register

31	30	29	28	27	26	25	24
OFFSETDRIFT_THRESHOLD_LO							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OFFSETDRIFT_THRESHOLD_LO							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OFFSETDRIFT_THRESHOLD_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFSETDRIFT_THRESHOLD_HI							
R/W							
0h							

Table 3-1139. RESOLVER_REGS_DIAG1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OFFSETDRIFT_THRESHOLD_LO	R/W	0h	Signed Lo threshold to detect offset drift
15:0	OFFSETDRIFT_THRESHOLD_HI	R/W	0h	Signed Hi threshold to detect offsetdrift

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3.13.2.86 RESOLVER_REGS_DIAG2_1 Register

3.13.2.86.1 RESOLVER_REGS_DIAG2_1 Register (Offset = 26Ch) [reset = 0h]

Diag2 1

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Table 3-1140. Instance Table

Instance Name	Physical Address
RESOLVER	502C B26Ch

Figure 3-618. RESOLVER_REGS_DIAG2_1 Name Register

31	30	29	28	27	26	25	24
EXCFREQDETECTED_COS							
RO							
0h							
23	22	21	20	19	18	17	16
EXCFREQDETECTED_COS							
RO							
0h							
15	14	13	12	11	10	9	8
EXCFREQDETECTED_SIN							
RO							
0h							
7	6	5	4	3	2	1	0
EXCFREQDETECTED_SIN							
RO							
0h							

Table 3-1141. RESOLVER_REGS_DIAG2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	EXCFREQDETECTED_COS	RO	0h	SW OBS Counts detected between zcs for cos excitation frequency
15:0	EXCFREQDETECTED_SIN	RO	0h	SW OBS Counts detected between zcs for sin excitation frequency

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3.13.2.87 RESOLVER_REGS_DIAG3_1 Register

3.13.2.87.1 RESOLVER_REGS_DIAG3_1 Register (Offset = 270h) [reset = 0h]

Diag3 1

Return to Summary Table

Table 3-1142. Instance Table

Instance Name	Physical Address
RESOLVER	502C B270h

Figure 3-619. RESOLVER_REGS_DIAG3_1 Name Register

31	30	29	28	27	26	25	24
EXCFREQDRIFT_THRESHOLD_LO							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EXCFREQDRIFT_THRESHOLD_LO							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EXCFREQDRIFT_THRESHOLD_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EXCFREQDRIFT_THRESHOLD_HI							
R/W							
0h							

Table 3-1143. RESOLVER_REGS_DIAG3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	EXCFREQDRIFT_THRESHOLD_LO	R/W	0h	Lo threshold to detect excfreqdrift
15:0	EXCFREQDRIFT_THRESHOLD_HI	R/W	0h	Hi threshold to detect excfreqdrift

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3.13.2.88 RESOLVER_REGS_DIAG4_1 Register

3.13.2.88.1 RESOLVER_REGS_DIAG4_1 Register (Offset = 274h) [reset = 10000h]

Diag4 1

Return to Summary Table

Table 3-1144. Instance Table

Instance Name	Physical Address
RESOLVER	502C B274h

Figure 3-620. RESOLVER_REGS_DIAG4_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
EXCFREQDRIFT_GLITCHCOUNT							
R/W							
1h							
15	14	13	12	11	10	9	8
EXCFREQ_LEVEL							
R/W							
0h							
7	6	5	4	3	2	1	0
EXCFREQ_LEVEL							
R/W							
0h							

Table 3-1145. RESOLVER_REGS_DIAG4_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	EXCFREQDRIFT_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error
15:0	EXCFREQ_LEVEL	R/W	0h	Threshold on ADC value to detect sin or cos zero crossings

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3.13.2.89 RESOLVER_REGS_DIAG5_1 Register

3.13.2.89.1 RESOLVER_REGS_DIAG5_1 Register (Offset = 278h) [reset = 10000h]

Diag5 1

Return to Summary Table

Table 3-1146. Instance Table

Instance Name	Physical Address
RESOLVER	502C B278h

Figure 3-621. RESOLVER_REGS_DIAG5_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
LOWAMPLITUDE_GLITCHCOUNT							
R/W							
1h							
15	14	13	12	11	10	9	8
LOWAMPLITUDE_THRESHOLD							
R/W							
0h							
7	6	5	4	3	2	1	0
LOWAMPLITUDE_THRESHOLD							
R/W							
0h							

Table 3-1147. RESOLVER_REGS_DIAG5_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	LOWAMPLITUDE_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error
15:0	LOWAMPLITUDE_THRESHOLD	R/W	0h	Hi threshold to detect lowamplitude. Both sin and cos need to be lower than this at the same time

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3.13.2.90 RESOLVER_REGS_DIAG6_1 Register

3.13.2.90.1 RESOLVER_REGS_DIAG6_1 Register (Offset = 27Ch) [reset = 0h]

Diag6 1

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Table 3-1148. Instance Table

Instance Name	Physical Address
RESOLVER	502C B27Ch

Figure 3-622. RESOLVER_REGS_DIAG6_1 Name Register

31	30	29	28	27	26	25	24
LOWAMPLITUDE_COS							
RO							
0h							
23	22	21	20	19	18	17	16
LOWAMPLITUDE_COS							
RO							
0h							
15	14	13	12	11	10	9	8
LOWAMPLITUDE_SIN							
RO							
0h							
7	6	5	4	3	2	1	0
LOWAMPLITUDE_SIN							
RO							
0h							

Table 3-1149. RESOLVER_REGS_DIAG6_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	LOWAMPLITUDE_COS	RO	0h	Value of cos channel at the error trigger instant
15:0	LOWAMPLITUDE_SIN	RO	0h	Value of sin channel at the error trigger instant

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3.13.2.91 RESOLVER_REGS_DIAG7_1 Register

3.13.2.91.1 RESOLVER_REGS_DIAG7_1 Register (Offset = 280h) [reset = 10000h]

Diag7 1

Return to Summary Table

Table 3-1150. Instance Table

Instance Name	Physical Address
RESOLVER	502C B280h

Figure 3-623. RESOLVER_REGS_DIAG7_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
HIGHAMPLITUDE_GLITCHCOUNT							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HIGHAMPLITUDE_THRESHOLD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HIGHAMPLITUDE_THRESHOLD							
R/W							
0h							

Table 3-1151. RESOLVER_REGS_DIAG7_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	HIGHAMPLITUDE_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error
15:0	HIGHAMPLITUDE_THRESHOLD	R/W	0h	Hi threshold to detect highamplitude. Both sin and cos need to be higher than this at the same time

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3.13.2.92 RESOLVER_REGS_DIAG8_1 Register

3.13.2.92.1 RESOLVER_REGS_DIAG8_1 Register (Offset = 284h) [reset = 0h]

Diag8 1

Return to Summary Table

Table 3-1152. Instance Table

Instance Name	Physical Address
RESOLVER	502C B284h

Figure 3-624. RESOLVER_REGS_DIAG8_1 Name Register

31	30	29	28	27	26	25	24
HIGHAMPLITUDE_COS							
RO							
0h							
23	22	21	20	19	18	17	16
HIGHAMPLITUDE_COS							
RO							
0h							
15	14	13	12	11	10	9	8
HIGHAMPLITUDE_SIN							
RO							
0h							
7	6	5	4	3	2	1	0
HIGHAMPLITUDE_SIN							
RO							
0h							

Table 3-1153. RESOLVER_REGS_DIAG8_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	HIGHAMPLITUDE_COS	RO	0h	Value of cos channel at the error trigger instant
15:0	HIGHAMPLITUDE_SIN	RO	0h	Value of sin channel at the error trigger instant

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3.13.2.93 RESOLVER_REGS_DIAG9_1 Register

3.13.2.93.1 RESOLVER_REGS_DIAG9_1 Register (Offset = 288h) [reset = 0h]

Diag9 1

Return to Summary Table

Table 3-1154. Instance Table

Instance Name	Physical Address
RESOLVER	502C B288h

Figure 3-625. RESOLVER_REGS_DIAG9_1 Name Register

31	30	29	28	27	26	25	24
SINSQCOSSQ_THRESHOLD_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
SINSQCOSSQ_THRESHOLD_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
SINSQCOSSQ_THRESHOLD_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
SINSQCOSSQ_THRESHOLD_LO							
R/W							
0h							

Table 3-1155. RESOLVER_REGS_DIAG9_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SINSQCOSSQ_THRESHOLD_HI	R/W	0h	High threshold to detect sinsqcossq. Sin^2+Cos^2 s needs to be lower than this
15:0	SINSQCOSSQ_THRESHOLD_LO	R/W	0h	Low threshold to detect sinsqcossq. Sin^2+Cos^2 s needs to be lower than this

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3.13.2.94 RESOLVER_REGS_DIAG10_1 Register

3.13.2.94.1 RESOLVER_REGS_DIAG10_1 Register (Offset = 28Ch) [reset = 0h]

Diag10 1

Return to Summary Table

Table 3-1156. Instance Table

Instance Name	Physical Address
RESOLVER	502C B28Ch

Figure 3-626. RESOLVER_REGS_DIAG10_1 Name Register

31	30	29	28	27	26	25	24
SINSQCOSSQ_COSSQ							
RO							
0h							
23	22	21	20	19	18	17	16
SINSQCOSSQ_COSSQ							
RO							
0h							
15	14	13	12	11	10	9	8
SINSQCOSSQ_SINSQ							
RO							
0h							
7	6	5	4	3	2	1	0
SINSQCOSSQ_SINSQ							
RO							
0h							

Table 3-1157. RESOLVER_REGS_DIAG10_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SINSQCOSSQ_COSSQ	RO	0h	Actual cossq value on error trigger ether lo or hi triggered, first event
15:0	SINSQCOSSQ_SINSQ	RO	0h	Actual sinsq value on error trigger ether lo or hi triggered, first event

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3.13.2.95 RESOLVER_REGS_DIAG11_1 Register

3.13.2.95.1 RESOLVER_REGS_DIAG11_1 Register (Offset = 290h) [reset = 1h]

Diag11 1

Return to Summary Table

Table 3-1158. Instance Table

Instance Name	Physical Address
RESOLVER	502C B290h

Figure 3-627. RESOLVER_REGS_DIAG11_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
SINSQCOSSQ_GLITCHCOUNT							
R/W							
1h							

Table 3-1159. RESOLVER_REGS_DIAG11_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	SINSQCOSSQ_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error

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3.13.2.96 RESOLVER_REGS_DIAG12_1 Register

3.13.2.96.1 RESOLVER_REGS_DIAG12_1 Register (Offset = 294h) [reset = 0h]

Diag12 1

Return to Summary Table

Table 3-1160. Instance Table

Instance Name	Physical Address
RESOLVER	502C B294h

Figure 3-628. RESOLVER_REGS_DIAG12_1 Name Register

31	30	29	28	27	26	25	24
ROTPEAK_LEVEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ROTPEAK_LEVEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ROTFREQ_LEVEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ROTFREQ_LEVEL							
R/W							
0h							

Table 3-1161. RESOLVER_REGS_DIAG12_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ROTPEAK_LEVEL	R/W	0h	Peak level of rotational sin/cos when other signal is zero crossing
15:0	ROTFREQ_LEVEL	R/W	0h	Zero crossing detection level of rotational sin/cos

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3.13.2.97 RESOLVER_REGS_DIAG13_1 Register

3.13.2.97.1 RESOLVER_REGS_DIAG13_1 Register (Offset = 298h) [reset = 0h]

Diag13 1

Return to Summary Table

Table 3-1162. Instance Table

Instance Name	Physical Address
RESOLVER	502C B298h

Figure 3-629. RESOLVER_REGS_DIAG13_1 Name Register

31	30	29	28	27	26	25	24
COS_MULTI_ZC_ERROR_COUNT							
RO							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIN_MULTI_ZC_ERROR_COUNT							
RO							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				COS_NEG_ZC_PEAK_MISMATCH_ERR	COS_POS_ZC_PEAK_MISMATCH_ERR	SIN_NEG_ZC_PEAK_MISMATCH_ERR	SIN_POS_ZC_PEAK_MISMATCH_ERR
NONE				RO	RO	RO	RO
0h				0h	0h	0h	0h

Table 3-1163. RESOLVER_REGS_DIAG13_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	COS_MULTI_ZC_ERROR_COUNT	RO	0h	Status of cos Capture number of faulty zcs
23:16	SIN_MULTI_ZC_ERROR_COUNT	RO	0h	Status of sin Capture number of faulty zcs
15:4	RESERVED	NONE	0h	Reserved
3	COS_NEG_ZC_PEAK_MISMATCH_ERR	RO	0h	During negative cos zero-crossing cos is not + or - peak
2	COS_POS_ZC_PEAK_MISMATCH_ERR	RO	0h	During positive cos zero-croscosg cos is not + or - peak
1	SIN_NEG_ZC_PEAK_MISMATCH_ERR	RO	0h	During negative sin zero-crossing cos is not + or - peak
0	SIN_POS_ZC_PEAK_MISMATCH_ERR	RO	0h	During positive sin zero-crossing cos is not + or - peak

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3.13.2.98 RESOLVER_REGS_DIAG14_1 Register

3.13.2.98.1 RESOLVER_REGS_DIAG14_1 Register (Offset = 29Ch) [reset = 0h]

Diag14 1

Return to Summary Table

Table 3-1164. Instance Table

Instance Name	Physical Address
RESOLVER	502C B29Ch

Figure 3-630. RESOLVER_REGS_DIAG14_1 Name Register

31	30	29	28	27	26	25	24
GAINDRIFT_THRESHOLD_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
GAINDRIFT_THRESHOLD_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
GAINDRIFT_THRESHOLD_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
GAINDRIFT_THRESHOLD_HI							
R/W							
0h							

Table 3-1165. RESOLVER_REGS_DIAG14_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	GAINDRIFT_THRESHOLD_LO	R/W	0h	Lo threshold to detect cos_gain drift
15:0	GAINDRIFT_THRESHOLD_HI	R/W	0h	Hi threshold to detect cos_gain drift

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3.13.2.99 RESOLVER_REGS_DIAG15_1 Register

3.13.2.99.1 RESOLVER_REGS_DIAG15_1 Register (Offset = 2A0h) [reset = 1h]

Diag15 1

Return to Summary Table

Table 3-1166. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2A0h

Figure 3-631. RESOLVER_REGS_DIAG15_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GAINDRIFT_GLITCHCOUNT							
R/W							
1h							

Table 3-1167. RESOLVER_REGS_DIAG15_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	GAINDRIFT_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error

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3.13.2.100 RESOLVER_REGS_DIAG16_1 Register

3.13.2.100.1 RESOLVER_REGS_DIAG16_1 Register (Offset = 2A4h) [reset = 0h]

Diag16 1

Return to Summary Table

Table 3-1168. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2A4h

Figure 3-632. RESOLVER_REGS_DIAG16_1 Name Register

31	30	29	28	27	26	25	24
PHASEDRIFT_THRESHOLD_LO							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHASEDRIFT_THRESHOLD_LO							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASEDRIFT_THRESHOLD_HI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASEDRIFT_THRESHOLD_HI							
R/W							
0h							

Table 3-1169. RESOLVER_REGS_DIAG16_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHASEDRIFT_THRESHOLD_LO	R/W	0h	Lo threshold to detect cos phase drift
15:0	PHASEDRIFT_THRESHOLD_HI	R/W	0h	Hi threshold to detect cos phase drift

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3.13.2.101 RESOLVER_REGS_DIAG17_1 Register

3.13.2.101.1 RESOLVER_REGS_DIAG17_1 Register (Offset = 2A8h) [reset = 1h]

Diag17 1

Return to Summary Table

Table 3-1170. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2A8h

Figure 3-633. RESOLVER_REGS_DIAG17_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PHASEDRIFT_GLITCHCOUNT							
R/W							
1h							

Table 3-1171. RESOLVER_REGS_DIAG17_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	PHASEDRIFT_GLITCHCOUNT	R/W	1h	Counter limit, how many times before issuing error

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3.13.2.102 RESOLVER_REGS_DIAG18_1 Register

3.13.2.102.1 RESOLVER_REGS_DIAG18_1 Register (Offset = 2ACh) [reset = 10000h]

Diag18 1

Return to Summary Table

Table 3-1172. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2ACh

Figure 3-634. RESOLVER_REGS_DIAG18_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRACK_ERR_GLITCH_TIME							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TRACK_ERR_THRESHOLD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRACK_ERR_THRESHOLD							
R/W							
0h							

Table 3-1173. RESOLVER_REGS_DIAG18_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	TRACK_ERR_GLITCH_TIME	R/W	1h	NOT USED
15:0	TRACK_ERR_THRESHOLD	R/W	0h	Tracking error treshold

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3.13.2.103 RESOLVER_REGS_OBS_ADC_1 Register

3.13.2.103.1 RESOLVER_REGS_OBS_ADC_1 Register (Offset = 2BCh) [reset = 0h]

Sw Obs adc data post latch and avg if enabled

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Table 3-1174. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2BCh

Figure 3-635. RESOLVER_REGS_OBS_ADC_1 Name Register

31	30	29	28	27	26	25	24
COS_ADC							
RO							
0h							
23	22	21	20	19	18	17	16
COS_ADC							
RO							
0h							
15	14	13	12	11	10	9	8
SIN_ADC							
RO							
0h							
7	6	5	4	3	2	1	0
SIN_ADC							
RO							
0h							

Table 3-1175. RESOLVER_REGS_OBS_ADC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_ADC	RO	0h	Signed SW Obs adc data post latch and avg if enabled
15:0	SIN_ADC	RO	0h	Signed SW Obs adc data post latch and avg if enabled

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3.13.2.104 RESOLVER_REGS_OBS_ADC_REC_1 Register

3.13.2.104.1 RESOLVER_REGS_OBS_ADC_REC_1 Register (Offset = 2C0h) [reset = 0h]

Sw Obs adc data post recovered data, so post dec

Return to Summary Table

Table 3-1176. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2C0h

Figure 3-636. RESOLVER_REGS_OBS_ADC_REC_1 Name Register

31	30	29	28	27	26	25	24
COS_REC							
RO							
0h							
23	22	21	20	19	18	17	16
COS_REC							
RO							
0h							
15	14	13	12	11	10	9	8
SIN_REC							
RO							
0h							
7	6	5	4	3	2	1	0
SIN_REC							
RO							
0h							

Table 3-1177. RESOLVER_REGS_OBS_ADC_REC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_REC	RO	0h	Signed SW Ob sadc data post recovered data, so post dec
15:0	SIN_REC	RO	0h	Signed SW Obs adc data post recovered data, so post dec

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3.13.2.105 RESOLVER_REGS_OBS_ADC_DC_1 Register

3.13.2.105.1 RESOLVER_REGS_OBS_ADC_DC_1 Register (Offset = 2C4h) [reset = 0h]

Sw Obs adc data post dc offset.

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Table 3-1178. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2C4h

Figure 3-637. RESOLVER_REGS_OBS_ADC_DC_1 Name Register

31	30	29	28	27	26	25	24
COS_DC							
RO							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COS_DC							
RO							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SIN_DC							
RO							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIN_DC							
RO							
0h							

Table 3-1179. RESOLVER_REGS_OBS_ADC_DC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_DC	RO	0h	Signed SW Obs adc data post dc offset
15:0	SIN_DC	RO	0h	Signed SW Obs adc data post dc offset

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3.13.2.106 RESOLVER_REGS_OBS_ADC_PGC_1 Register

3.13.2.106.1 RESOLVER_REGS_OBS_ADC_PGC_1 Register (Offset = 2C8h) [reset = 0h]

Sw Obs post phase and gain correction .

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Table 3-1180. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2C8h

Figure 3-638. RESOLVER_REGS_OBS_ADC_PGC_1 Name Register

31	30	29	28	27	26	25	24
COS_PGC							
RO							
0h							
23	22	21	20	19	18	17	16
COS_PGC							
RO							
0h							
15	14	13	12	11	10	9	8
SIN_PGC							
RO							
0h							
7	6	5	4	3	2	1	0
SIN_PGC							
RO							
0h							

Table 3-1181. RESOLVER_REGS_OBS_ADC_PGC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	COS_PGC	RO	0h	Signed SW Obs adc data post phase and gain correction
15:0	SIN_PGC	RO	0h	Signed SW Obs adc data post phase and gain correction

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3.13.2.107 RESOLVER_REGS_OBS_PEAKHISTOGRAM3_0_1 Register

3.13.2.107.1 RESOLVER_REGS_OBS_PEAKHISTOGRAM3_0_1 Register (Offset = 2D0h) [reset = 0h]

SW obs peak histogram buckets.

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Table 3-1182. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2D0h

Figure 3-639. RESOLVER_REGS_OBS_PEAKHISTOGRAM3_0_1 Name Register

31	30	29	28	27	26	25	24
PEAKHISTOGRAM3_1							
RO							
0h							
23	22	21	20	19	18	17	16
PEAKHISTOGRAM2_1							
RO							
0h							
15	14	13	12	11	10	9	8
PEAKHISTOGRAM1_1							
RO							
0h							
7	6	5	4	3	2	1	0
PEAKHISTOGRAM0_1							
RO							
0h							

Table 3-1183. RESOLVER_REGS_OBS_PEAKHISTOGRAM3_0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PEAKHISTOGRAM3_1	RO	0h	Ideal sample bucket3
23:16	PEAKHISTOGRAM2_1	RO	0h	Ideal sample bucket2
15:8	PEAKHISTOGRAM1_1	RO	0h	Ideal sample bucket1
7:0	PEAKHISTOGRAM0_1	RO	0h	Ideal sample bucket0

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3.13.2.108 RESOLVER_REGS_OBS_PEAKHISTOGRAM7_4_1 Register

3.13.2.108.1 RESOLVER_REGS_OBS_PEAKHISTOGRAM7_4_1 Register (Offset = 2D4h) [reset = 0h]

SW obs peak histogram buckets .

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Table 3-1184. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2D4h

Figure 3-640. RESOLVER_REGS_OBS_PEAKHISTOGRAM7_4_1 Name Register

31	30	29	28	27	26	25	24
PEAKHISTOGRAM7_1							
RO							
0h							
23	22	21	20	19	18	17	16
PEAKHISTOGRAM6_1							
RO							
0h							
15	14	13	12	11	10	9	8
PEAKHISTOGRAM5_1							
RO							
0h							
7	6	5	4	3	2	1	0
PEAKHISTOGRAM4_1							
RO							
0h							

Table 3-1185. RESOLVER_REGS_OBS_PEAKHISTOGRAM7_4_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PEAKHISTOGRAM7_1	RO	0h	Ideal sample bucket7
23:16	PEAKHISTOGRAM6_1	RO	0h	Ideal sample bucket6
15:8	PEAKHISTOGRAM5_1	RO	0h	Ideal sample bucket5
7:0	PEAKHISTOGRAM4_1	RO	0h	Ideal sample bucket4

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3.13.2.109 RESOLVER_REGS_OBS_PEAKHISTOGRAM11_8_1 Register

3.13.2.109.1 RESOLVER_REGS_OBS_PEAKHISTOGRAM11_8_1 Register (Offset = 2D8h) [reset = 0h]

SW obs peak histogram buckets .

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Table 3-1186. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2D8h

Figure 3-641. RESOLVER_REGS_OBS_PEAKHISTOGRAM11_8_1 Name Register

31	30	29	28	27	26	25	24
PEAKHISTOGRAM11_1							
RO							
0h							
23	22	21	20	19	18	17	16
PEAKHISTOGRAM10_1							
RO							
0h							
15	14	13	12	11	10	9	8
PEAKHISTOGRAM9_1							
RO							
0h							
7	6	5	4	3	2	1	0
PEAKHISTOGRAM8_1							
RO							
0h							

Table 3-1187. RESOLVER_REGS_OBS_PEAKHISTOGRAM11_8_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PEAKHISTOGRAM11_1	RO	0h	Ideal sample bucket11
23:16	PEAKHISTOGRAM10_1	RO	0h	Ideal sample bucket10
15:8	PEAKHISTOGRAM9_1	RO	0h	Ideal sample bucket9
7:0	PEAKHISTOGRAM8_1	RO	0h	Ideal sample bucket8

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3.13.2.110 RESOLVER_REGS_OBS_PEAKHISTOGRAM15_12_1 Register

3.13.2.110.1 RESOLVER_REGS_OBS_PEAKHISTOGRAM15_12_1 Register (Offset = 2DCh) [reset = 0h]

SW obs peak histogram buckets .

Return to Summary Table

Table 3-1188. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2DCh

Figure 3-642. RESOLVER_REGS_OBS_PEAKHISTOGRAM15_12_1 Name Register

31	30	29	28	27	26	25	24
PEAKHISTOGRAM15_1							
RO							
0h							
23	22	21	20	19	18	17	16
PEAKHISTOGRAM14_1							
RO							
0h							
15	14	13	12	11	10	9	8
PEAKHISTOGRAM13_1							
RO							
0h							
7	6	5	4	3	2	1	0
PEAKHISTOGRAM12_1							
RO							
0h							

Table 3-1189. RESOLVER_REGS_OBS_PEAKHISTOGRAM15_12_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PEAKHISTOGRAM15_1	RO	0h	Ideal sample bucket15
23:16	PEAKHISTOGRAM14_1	RO	0h	Ideal sample bucket14
15:8	PEAKHISTOGRAM13_1	RO	0h	Ideal sample bucket13
7:0	PEAKHISTOGRAM12_1	RO	0h	Ideal sample bucket12

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3.13.2.111 RESOLVER_REGS_OBS_PEAKHISTOGRAM19_16_1 Register

3.13.2.111.1 RESOLVER_REGS_OBS_PEAKHISTOGRAM19_16_1 Register (Offset = 2E0h) [reset = 0h]

SW obs peak histogram buckets .

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Table 3-1190. Instance Table

Instance Name	Physical Address
RESOLVER	502C B2E0h

Figure 3-643. RESOLVER_REGS_OBS_PEAKHISTOGRAM19_16_1 Name Register

31	30	29	28	27	26	25	24
PEAKHISTOGRAM19_1							
RO							
0h							
23	22	21	20	19	18	17	16
PEAKHISTOGRAM18_1							
RO							
0h							
15	14	13	12	11	10	9	8
PEAKHISTOGRAM17_1							
RO							
0h							
7	6	5	4	3	2	1	0
PEAKHISTOGRAM16_1							
RO							
0h							

Table 3-1191. RESOLVER_REGS_OBS_PEAKHISTOGRAM19_16_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PEAKHISTOGRAM19_1	RO	0h	Ideal sample bucket19
23:16	PEAKHISTOGRAM18_1	RO	0h	Ideal sample bucket18
15:8	PEAKHISTOGRAM17_1	RO	0h	Ideal sample bucket17
7:0	PEAKHISTOGRAM16_1	RO	0h	Ideal sample bucket16

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3.14 ADC_R

ADC_R

3.14.1 ADC_R Summaries

ADC_R Summaries

Table 3-1192. ADC_R_CFG Registers, Base Address=502C 5000h, Length=512

Offset	Length	Register Name	ADC_R0 Physical Address	ADC_R1 Physical Address
0h	16	ADC_R_CFG_ADCCTL1	502C 5000h	502C 7000h
2h	16	ADC_R_CFG_ADCCTL2	502C 5002h	502C 7002h
4h	16	ADC_R_CFG_ADCBURSTCTL	502C 5004h	502C 7004h
6h	16	ADC_R_CFG_ADCINTFLG	502C 5006h	502C 7006h
8h	16	ADC_R_CFG_ADCINTFLGCLR	502C 5008h	502C 7008h
Ah	16	ADC_R_CFG_ADCINTOVF	502C 500Ah	502C 700Ah
Ch	16	ADC_R_CFG_ADCINTOVFCLR	502C 500Ch	502C 700Ch
Eh	16	ADC_R_CFG_ADCINTSEL1N2	502C 500Eh	502C 700Eh
10h	16	ADC_R_CFG_ADCINTSEL3N4	502C 5010h	502C 7010h
12h	16	ADC_R_CFG_ADCSOCPRICTL	502C 5012h	502C 7012h
14h	16	ADC_R_CFG_ADCINTSOCSEL1	502C 5014h	502C 7014h
16h	16	ADC_R_CFG_ADCINTSOCSEL2	502C 5016h	502C 7016h
18h	16	ADC_R_CFG_ADCSOCFLG1	502C 5018h	502C 7018h
1Ah	16	ADC_R_CFG_ADCSOCFRC1	502C 501Ah	502C 701Ah
1Ch	16	ADC_R_CFG_ADCSOCOVF1	502C 501Ch	502C 701Ch
1Eh	16	ADC_R_CFG_ADCSOCOVFCLR1	502C 501Eh	502C 701Eh
20h	32	ADC_R_CFG_ADCSOC0CTL	502C 5020h	502C 7020h
24h	32	ADC_R_CFG_ADCSOC1CTL	502C 5024h	502C 7024h
28h	32	ADC_R_CFG_ADCSOC2CTL	502C 5028h	502C 7028h
2Ch	32	ADC_R_CFG_ADCSOC3CTL	502C 502Ch	502C 702Ch
30h	32	ADC_R_CFG_ADCSOC4CTL	502C 5030h	502C 7030h
34h	32	ADC_R_CFG_ADCSOC5CTL	502C 5034h	502C 7034h
38h	32	ADC_R_CFG_ADCSOC6CTL	502C 5038h	502C 7038h
3Ch	32	ADC_R_CFG_ADCSOC7CTL	502C 503Ch	502C 703Ch
40h	32	ADC_R_CFG_ADCSOC8CTL	502C 5040h	502C 7040h
44h	32	ADC_R_CFG_ADCSOC9CTL	502C 5044h	502C 7044h
48h	32	ADC_R_CFG_ADCSOC10CTL	502C 5048h	502C 7048h
4Ch	32	ADC_R_CFG_ADCSOC11CTL	502C 504Ch	502C 704Ch
50h	32	ADC_R_CFG_ADCSOC12CTL	502C 5050h	502C 7050h
54h	32	ADC_R_CFG_ADCSOC13CTL	502C 5054h	502C 7054h
58h	32	ADC_R_CFG_ADCSOC14CTL	502C 5058h	502C 7058h
5Ch	32	ADC_R_CFG_ADCSOC15CTL	502C 505Ch	502C 705Ch
60h	16	ADC_R_CFG_ADCEVTSTAT	502C 5060h	502C 7060h
64h	16	ADC_R_CFG_ADCEVTCLR	502C 5064h	502C 7064h
68h	16	ADC_R_CFG_ADCEVTSEL	502C 5068h	502C 7068h
6Ch	16	ADC_R_CFG_ADCEVTINTSEL	502C 506Ch	502C 706Ch
72h	16	ADC_R_CFG_ADCCOUNTER	502C 5072h	502C 7072h
74h	16	ADC_R_CFG_ADCREV	502C 5074h	502C 7074h
80h	16	ADC_R_CFG_ADCPPB1CONFIG	502C 5080h	502C 7080h
82h	16	ADC_R_CFG_ADCPPB1STAMP	502C 5082h	502C 7082h

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Table 3-1192. ADC_R_CFG Registers, Base Address=502C 5000h, Length=512 (continued)

Offset	Length	Register Name	ADC_R0 Physical Address	ADC_R1 Physical Address
84h	16	ADC_R_CFG_ADCPPB1OFFCAL	502C 5084h	502C 7084h
86h	16	ADC_R_CFG_ADCPPB1OFFREF	502C 5086h	502C 7086h
88h	32	ADC_R_CFG_ADCPPB1TRIPHI	502C 5088h	502C 7088h
8Ch	32	ADC_R_CFG_ADCPPB1TRIPLO	502C 508Ch	502C 708Ch
90h	16	ADC_R_CFG_ADCPPB2CONFIG	502C 5090h	502C 7090h
92h	16	ADC_R_CFG_ADCPPB2STAMP	502C 5092h	502C 7092h
94h	16	ADC_R_CFG_ADCPPB2OFFCAL	502C 5094h	502C 7094h
96h	16	ADC_R_CFG_ADCPPB2OFFREF	502C 5096h	502C 7096h
98h	32	ADC_R_CFG_ADCPPB2TRIPHI	502C 5098h	502C 7098h
9Ch	32	ADC_R_CFG_ADCPPB2TRIPLO	502C 509Ch	502C 709Ch
A0h	16	ADC_R_CFG_ADCPPB3CONFIG	502C 50A0h	502C 70A0h
A2h	16	ADC_R_CFG_ADCPPB3STAMP	502C 50A2h	502C 70A2h
A4h	16	ADC_R_CFG_ADCPPB3OFFCAL	502C 50A4h	502C 70A4h
A6h	16	ADC_R_CFG_ADCPPB3OFFREF	502C 50A6h	502C 70A6h
A8h	32	ADC_R_CFG_ADCPPB3TRIPHI	502C 50A8h	502C 70A8h
ACh	32	ADC_R_CFG_ADCPPB3TRIPLO	502C 50ACh	502C 70ACh
B0h	16	ADC_R_CFG_ADCPPB4CONFIG	502C 50B0h	502C 70B0h
B2h	16	ADC_R_CFG_ADCPPB4STAMP	502C 50B2h	502C 70B2h
B4h	16	ADC_R_CFG_ADCPPB4OFFCAL	502C 50B4h	502C 70B4h
B6h	16	ADC_R_CFG_ADCPPB4OFFREF	502C 50B6h	502C 70B6h
B8h	32	ADC_R_CFG_ADCPPB4TRIPHI	502C 50B8h	502C 70B8h
BCh	32	ADC_R_CFG_ADCPPB4TRIPLO	502C 50BCh	502C 70BCh
C0h	32	ADC_R_CFG_ADCSAFECHECKRESEN	502C 50C0h	502C 70C0h
DEh	16	ADC_R_CFG_ADCINTCYCLE	502C 50DEh	502C 70DEh
FAh	16	ADC_R_CFG_ADCREV2	502C 50FAh	502C 70FAh
FCh	32	ADC_R_CFG_ADCINLTRIMCTL	502C 50FCh	502C 70FCh
100h	32	ADC_R_CFG_REP1CTL	502C 5100h	502C 7100h
104h	32	ADC_R_CFG_REP1N	502C 5104h	502C 7104h
108h	32	ADC_R_CFG_REP1PHASE	502C 5108h	502C 7108h
10Ch	32	ADC_R_CFG_REP1SPREAD	502C 510Ch	502C 710Ch
110h	16	ADC_R_CFG_REP1FRC	502C 5110h	502C 7110h
120h	32	ADC_R_CFG_REP2CTL	502C 5120h	502C 7120h
124h	32	ADC_R_CFG_REP2N	502C 5124h	502C 7124h
128h	32	ADC_R_CFG_REP2PHASE	502C 5128h	502C 7128h
12Ch	32	ADC_R_CFG_REP2SPREAD	502C 512Ch	502C 712Ch
130h	16	ADC_R_CFG_REP2FRC	502C 5130h	502C 7130h
140h	16	ADC_R_CFG_ADCPPB1LIMIT	502C 5140h	502C 7140h
144h	16	ADC_R_CFG_ADCPPBP1PCOUNT	502C 5144h	502C 7144h
148h	16	ADC_R_CFG_ADCPPB1CONFIG2	502C 5148h	502C 7148h
14Ch	32	ADC_R_CFG_ADCPPB1PSUM	502C 514Ch	502C 714Ch
150h	32	ADC_R_CFG_ADCPPB1PMAX	502C 5150h	502C 7150h
154h	16	ADC_R_CFG_ADCPPB1PMAXI	502C 5154h	502C 7154h
158h	32	ADC_R_CFG_ADCPPB1PMIN	502C 5158h	502C 7158h
15Ch	16	ADC_R_CFG_ADCPPB1PMINI	502C 515Ch	502C 715Ch
160h	32	ADC_R_CFG_ADCPPB1TRIPLO2	502C 5160h	502C 7160h
174h	16	ADC_R_CFG_ADCPPB2LIMIT	502C 5174h	502C 7174h
178h	16	ADC_R_CFG_ADCPPBP2PCOUNT	502C 5178h	502C 7178h

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Table 3-1192. ADC_R_CFG Registers, Base Address=502C 5000h, Length=512 (continued)

Offset	Length	Register Name	ADC_R0 Physical Address	ADC_R1 Physical Address
17Ch	16	ADC_R_CFG_ADCPPB2CONFIG2	502C 517Ch	502C 717Ch
180h	32	ADC_R_CFG_ADCPPB2PSUM	502C 5180h	502C 7180h
184h	32	ADC_R_CFG_ADCPPB2PMAX	502C 5184h	502C 7184h
188h	16	ADC_R_CFG_ADCPPB2PMAXI	502C 5188h	502C 7188h
18Ch	32	ADC_R_CFG_ADCPPB2PMIN	502C 518Ch	502C 718Ch
190h	16	ADC_R_CFG_ADCPPB2PMINI	502C 5190h	502C 7190h
194h	32	ADC_R_CFG_ADCPPB2TRIPLO2	502C 5194h	502C 7194h
1A8h	16	ADC_R_CFG_ADCPPB3LIMIT	502C 51A8h	502C 71A8h
1ACh	16	ADC_R_CFG_ADCPPBP3PCOUNT	502C 51ACh	502C 71ACh
1B0h	16	ADC_R_CFG_ADCPPB3CONFIG2	502C 51B0h	502C 71B0h
1B4h	32	ADC_R_CFG_ADCPPB3PSUM	502C 51B4h	502C 71B4h
1B8h	32	ADC_R_CFG_ADCPPB3PMAX	502C 51B8h	502C 71B8h
1BCh	16	ADC_R_CFG_ADCPPB3PMAXI	502C 51BCh	502C 71BCh
1C0h	32	ADC_R_CFG_ADCPPB3PMIN	502C 51C0h	502C 71C0h
1C4h	16	ADC_R_CFG_ADCPPB3PMINI	502C 51C4h	502C 71C4h
1C8h	32	ADC_R_CFG_ADCPPB3TRIPLO2	502C 51C8h	502C 71C8h
1DCh	16	ADC_R_CFG_ADCPPB4LIMIT	502C 51DCh	502C 71DCh
1E0h	16	ADC_R_CFG_ADCPPBP4PCOUNT	502C 51E0h	502C 71E0h
1E4h	16	ADC_R_CFG_ADCPPB4CONFIG2	502C 51E4h	502C 71E4h
1E8h	32	ADC_R_CFG_ADCPPB4PSUM	502C 51E8h	502C 71E8h
1ECh	32	ADC_R_CFG_ADCPPB4PMAX	502C 51ECh	502C 71ECh
1F0h	16	ADC_R_CFG_ADCPPB4PMAXI	502C 51F0h	502C 71F0h
1F4h	32	ADC_R_CFG_ADCPPB4PMIN	502C 51F4h	502C 71F4h
1F8h	16	ADC_R_CFG_ADCPPB4PMINI	502C 51F8h	502C 71F8h
1FCh	32	ADC_R_CFG_ADCPPB4TRIPLO2	502C 51FCh	502C 71FCh

Table 3-1193. ADC_R_RESULTS Registers, Base Address=502C 6000h, Length=256

Offset	Length	Register Name	ADC_R0 Physical Address	ADC_R1 Physical Address
0h	16	ADC_R_RESULTS_ADCRESULT0	502C 6000h	502C 8000h
2h	16	ADC_R_RESULTS_ADCRESULT1	502C 6002h	502C 8002h
4h	16	ADC_R_RESULTS_ADCRESULT2	502C 6004h	502C 8004h
6h	16	ADC_R_RESULTS_ADCRESULT3	502C 6006h	502C 8006h
8h	16	ADC_R_RESULTS_ADCRESULT4	502C 6008h	502C 8008h
Ah	16	ADC_R_RESULTS_ADCRESULT5	502C 600Ah	502C 800Ah
Ch	16	ADC_R_RESULTS_ADCRESULT6	502C 600Ch	502C 800Ch
Eh	16	ADC_R_RESULTS_ADCRESULT7	502C 600Eh	502C 800Eh
10h	16	ADC_R_RESULTS_ADCRESULT8	502C 6010h	502C 8010h
12h	16	ADC_R_RESULTS_ADCRESULT9	502C 6012h	502C 8012h
14h	16	ADC_R_RESULTS_ADCRESULT10	502C 6014h	502C 8014h
16h	16	ADC_R_RESULTS_ADCRESULT11	502C 6016h	502C 8016h
18h	16	ADC_R_RESULTS_ADCRESULT12	502C 6018h	502C 8018h
1Ah	16	ADC_R_RESULTS_ADCRESULT13	502C 601Ah	502C 801Ah
1Ch	16	ADC_R_RESULTS_ADCRESULT14	502C 601Ch	502C 801Ch
1Eh	16	ADC_R_RESULTS_ADCRESULT15	502C 601Eh	502C 801Eh
20h	32	ADC_R_RESULTS_ADCPPB1RESULT	502C 6020h	502C 8020h
24h	32	ADC_R_RESULTS_ADCPPB2RESULT	502C 6024h	502C 8024h

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Table 3-1193. ADC_R_RESULTS Registers, Base Address=502C 6000h, Length=256 (continued)

Offset	Length	Register Name	ADC_R0 Physical Address	ADC_R1 Physical Address
28h	32	ADC_R_RESULTS_ADCPPB3RESULT	502C 6028h	502C 8028h
2Ch	32	ADC_R_RESULTS_ADCPPB4RESULT	502C 602Ch	502C 802Ch
30h	32	ADC_R_RESULTS_ADCPPB1SUM	502C 6030h	502C 8030h
34h	16	ADC_R_RESULTS_ADCPPB1COUNT	502C 6034h	502C 8034h
38h	32	ADC_R_RESULTS_ADCPPB2SUM	502C 6038h	502C 8038h
3Ch	16	ADC_R_RESULTS_ADCPPB2COUNT	502C 603Ch	502C 803Ch
40h	32	ADC_R_RESULTS_ADCPPB3SUM	502C 6040h	502C 8040h
44h	16	ADC_R_RESULTS_ADCPPB3COUNT	502C 6044h	502C 8044h
48h	32	ADC_R_RESULTS_ADCPPB4SUM	502C 6048h	502C 8048h
4Ch	16	ADC_R_RESULTS_ADCPPB4COUNT	502C 604Ch	502C 804Ch
50h	32	ADC_R_RESULTS_ADCPPB1MAX	502C 6050h	502C 8050h
54h	16	ADC_R_RESULTS_ADCPPB1MAXI	502C 6054h	502C 8054h
58h	32	ADC_R_RESULTS_ADCPPB1MIN	502C 6058h	502C 8058h
5Ch	16	ADC_R_RESULTS_ADCPPB1MINI	502C 605Ch	502C 805Ch
60h	32	ADC_R_RESULTS_ADCPPB2MAX	502C 6060h	502C 8060h
64h	16	ADC_R_RESULTS_ADCPPB2MAXI	502C 6064h	502C 8064h
68h	32	ADC_R_RESULTS_ADCPPB2MIN	502C 6068h	502C 8068h
6Ch	16	ADC_R_RESULTS_ADCPPB2MINI	502C 606Ch	502C 806Ch
70h	32	ADC_R_RESULTS_ADCPPB3MAX	502C 6070h	502C 8070h
74h	16	ADC_R_RESULTS_ADCPPB3MAXI	502C 6074h	502C 8074h
78h	32	ADC_R_RESULTS_ADCPPB3MIN	502C 6078h	502C 8078h
7Ch	16	ADC_R_RESULTS_ADCPPB3MINI	502C 607Ch	502C 807Ch
80h	32	ADC_R_RESULTS_ADCPPB4MAX	502C 6080h	502C 8080h
84h	16	ADC_R_RESULTS_ADCPPB4MAXI	502C 6084h	502C 8084h
88h	32	ADC_R_RESULTS_ADCPPB4MIN	502C 6088h	502C 8088h
8Ch	16	ADC_R_RESULTS_ADCPPB4MINI	502C 608Ch	502C 808Ch

3.14.2 ADC_R Registers

ADC_R Registers

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3.14.2.1 ADC_R_CFG_ADCCTL1 Register

3.14.2.1.1 ADC_R_CFG_ADCCTL1 Register (Offset = 0h) [reset = 0h]

ADC Control 1 Register.

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Table 3-1194. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5000h
ADC_R1	502C 7000h

Figure 3-644. ADC_R_CFG_ADCCTL1 Name Register

15	14	13	12	11	10	9	8
TDMAEN	EXTMUXPRESELECTEN	ADCBSY	RESERVED_3	ADCBSYCHN			
R/W	R/W	R	R	R			
0h	0h	0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADCPWDNZ	RESERVED_2				INTPULSEPOS	RESERVED_1	
R/W	R				R/W	R	
0h	0h				0h	0h	

Table 3-1195. ADC_R_CFG_ADCCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TDMAEN	R/W	0h	Enable Alternate DMA Timings. This bit controls when the DMA is triggered. 0 DMA is triggered at the same time as the CPU interrupt 1 DMA is always triggered at tDMA regardless or whether the ADC is in early interrupt mode or late interrupt mode
14	EXTMUXPRESELECTEN	R/W	0h	If th the ADC SOC sequence is deterministic, the ADCEXTMUX pins can be set earlier: at the end of the S+H window of the previous conversion instead of the beginning of the S+H window of the current conversion. This allows some of the external mux settling time to be pipelined with the previous conversion's conversion time. However, this will not work in the case where high-priority SOCs can arrive asynchronously. 0 ADCEXTMUX pins only change at beginning of S+H window 1 ADCEXTMUX pins are set after the end of S+H window based on pending SOCs
13	ADCBSY	R	0h	ADC Busy. Set when ADC SOC is generated, cleared by hardware four ADC clocks after negative edge of S/H pulse. Used by the ADC state machine to determine if ADC is available to sample. 0 ADC is available to sample next channel 1 ADC is busy and cannot sample another channel
12	RESERVED_3	R	0h	Reserved

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Table 3-1195. ADC_R_CFG_ADCCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	ADCBSYCHN	R	0h	ADC Busy Channel. Set when an ADC Start of Conversion [SOC] is generated. When ADCBSY 0:holds the value of the last converted SOC When ADCBSY 1:reflects the SOC currently being processed 0h SOC0 is currently processing or was last SOC converted 1h SOC1 is currently processing or was last SOC converted 2h SOC2 is currently processing or was last SOC converted 3h SOC3 is currently processing or was last SOC converted 4h SOC4 is currently processing or was last SOC converted 5h SOC5 is currently processing or was last SOC converted 6h SOC6 is currently processing or was last SOC converted 7h SOC7 is currently processing or was last SOC converted 8h SOC8 is currently processing or was last SOC converted 9h SOC9 is currently processing or was last SOC converted Ah SOC10 is currently processing or was last SOC converted Bh SOC11 is currently processing or was last SOC converted Ch SOC12 is currently processing or was last SOC converted Dh SOC13 is currently processing or was last SOC converted Eh SOC14 is currently processing or was last SOC converted Fh SOC15 is currently processing or was last SOC converted
7	ADCPWDNZ	R/W	0h	ADC Power Down [active low]. This bit controls the power up and power down of all the analog circuitry inside the analog core. 0 All analog circuitry inside the core is powered down 1 All analog circuitry inside the core is powered up
6:3	RESERVED_2	R	0h	Reserved
2	INTPULSEPOS	R/W	0h	ADC Interrupt Pulse Position. 0 Interrupt pulse generation occurs when ADC begins conversion [at the end of the acquisition window] plus a number of SYSCLK cycles as specified in the ADCINTCYCLE.OFFSET register. 1 Interrupt pulse generation occurs at the end of the conversion, 1 cycle prior to the ADC result latching into its result register
1:0	RESERVED_1	R	0h	Reserved

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3.14.2.2 ADC_R_CFG_ADCCTL2 Register

3.14.2.2.1 ADC_R_CFG_ADCCTL2 Register (Offset = 2h) [reset = 0h]

ADC Control 2 Register.

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Table 3-1196. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5002h
ADC_R1	502C 7002h

Figure 3-645. ADC_R_CFG_ADCCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_3			RESERVED_2				
R			R				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SIGNALMODE	RESOLUTION	RESERVED_1		PRESCALE			
R/W	R/W	R		R/W			
0h	0h	0h		0h			

Table 3-1197. ADC_R_CFG_ADCCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_3	R	0h	Reserved
12:8	RESERVED_2	R	0h	Reserved
7	SIGNALMODE	R/W	0h	SOC Signaling Mode. Selects the input mode of the converter. Use the AdcSetMode function to change the signal mode. 0 Single-ended 1 Differential
6	RESOLUTION	R/W	0h	SOC Conversion Resolution. Selects the resolution of the converter. Use the AdcSetMode function to change the resolution. 0 12-bit resolution
5:4	RESERVED_1	R	0h	Reserved
3:0	PRESCALE	R/W	0h	ADC Clock Prescaler. 0000 ADCCLK = Input Clock / 1.0 0001 Invalid 0010 ADCCLK = Input Clock / 2.0 0011 ADCCLK = Input Clock / 2.5 0100 ADCCLK = Input Clock / 3.0 0101 ADCCLK = Input Clock / 3.5 0110 ADCCLK = Input Clock / 4.0 0111 ADCCLK = Input Clock / 4.5 1000 ADCCLK = Input Clock / 5.0 1001 ADCCLK = Input Clock / 5.5 1010 ADCCLK = Input Clock / 6.0 1011 ADCCLK = Input Clock / 6.5 1100 ADCCLK = Input Clock / 7.0 1101 ADCCLK = Input Clock / 7.5 1110 ADCCLK = Input Clock / 8.0 1111 ADCCLK = Input Clock / 8.5

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3.14.2.3 ADC_R_CFG_ADCBURSTCTL Register

3.14.2.3.1 ADC_R_CFG_ADCBURSTCTL Register (Offset = 4h) [reset = 0h]

ADC Burst Control Register.

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Table 3-1198. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5004h
ADC_R1	502C 7004h

Figure 3-646. ADC_R_CFG_ADCBURSTCTL Name Register

15	14	13	12	11	10	9	8
BURSTEN	RESERVED_2			BURSTSIZE			
R/W	R			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	BURSTTRIGSEL						
R	R/W						
0h	0h						

Table 3-1199. ADC_R_CFG_ADCBURSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BURSTEN	R/W	0h	SOC Burst Mode Enable. This bit enables the SOC Burst Mode of operation. 0 Burst mode is disabled. 1 Burst mode is enabled.
14:12	RESERVED_2	R	0h	Reserved
11:8	BURSTSIZE	R/W	0h	SOC Burst Size Select. This bit field determines how many SOCs are converted when a burst conversion sequence is started. The first SOC converted is defined by the round robin pointer, which is advanced as each SOC is converted. 0h 1 SOC converted 1h 2 SOCs converted 2h 3 SOCs converted 3h 4 SOCs converted 4h 5 SOCs converted 5h 6 SOCs converted 6h 7 SOCs converted 7h 8 SOCs converted 8h 9 SOCs converted 9h 10 SOCs converted Ah 11 SOCs converted Bh 12 SOCs converted Ch 13 SOCs converted Dh 14 SOCs converted Eh 15 SOCs converted Fh 16 SOCs converted Note: If the burst causes SOCs to be set for conversion that were already pending, the corresponding bits in the ADCSOCOVF register will be set.
7	RESERVED_1	R	0h	Reserved

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Table 3-1199. ADC_R_CFG_ADCBURSTCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	BURSTTRIGSEL	R/W	0h	SOC Burst Trigger Source Select. Configures which trigger will start a burst conversion sequence. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h BURSTTRIG0 - Software only 01h BURSTTRIG1 - RTI0 Timer 02h BURSTTRIG2 - RTI1 Timer 03h BURSTTRIG3 - RTI2 Timer 04h BURSTTRIG4 - RTI3 Timer 05h BURSTTRIG5 - InputXBAR.Out[5] 06h BURSTTRIG6 - spare 07h BURSTTRIG7 - spare 08h BURSTTRIG8 - EPWM0, ADCSOCA 09h BURSTTRIG9 - EPWM0, ADCSOCB 0Ah BURSTTRIG10 - EPWM1, ADCSOCA 0Bh BURSTTRIG11 - EPWM1, ADCSOCB 0Ch BURSTTRIG12 - EPWM2, ADCSOCA 0Dh BURSTTRIG13 - EPWM2, ADCSOCB 0Eh BURSTTRIG14 - EPWM3, ADCSOCA 0Fh BURSTTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h BURSTTRIG64 - EPWM28, ADCSOCA 41h BURSTTRIG65 - EPWM28, ADCSOCB 42h BURSTTRIG66 - EPWM29, ADCSOCA 43h BURSTTRIG67 - EPWM29, ADCSOCB 44h BURSTTRIG68 - EPWM30, ADCSOCA 45h BURSTTRIG69 - EPWM30, ADCSOCB 46h BURSTTRIG70 - EPWM31, ADCSOCA 47h BURSTTRIG71 - EPWM31, ADCSOCB 48h BURSTTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h BURSTTRIG81 - ECAP9, TRIGOUT 52h BURSTTRIG82 - ECAP10, TRIGOUT .... 57h BURSTTRIG73 - ECAP15, TRIGOUT 58h BURSTTRIG1 - RTI4 Timer 59h BURSTTRIG1 - RTI5 Timer 5Ah BURSTTRIG1 - RTI6 Timer 5Bh BURSTTRIG1 - RTI7 Timer

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3.14.2.4 ADC_R_CFG_ADCINTFLG Register

3.14.2.4.1 ADC_R_CFG_ADCINTFLG Register (Offset = 6h) [reset = 0h]

ADC Interrupt Flag Register.

Return to Summary Table

Table 3-1200. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5006h
ADC_R1	502C 7006h

Figure 3-647. ADC_R_CFG_ADCINTFLG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADCINT4RESULT	ADCINT3RESULT	ADCINT2RESULT	ADCINT1RESULT	ADCINT4	ADCINT3	ADCINT2	ADCINT1
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1201. ADC_R_CFG_ADCINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_1	R	0h	Reserved
7	ADCINT4RESULT	R	0h	ADC Interrupt 4 Results Ready Flag. This flag is set when the conversions results associated with ADCINT4 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT4 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.
6	ADCINT3RESULT	R	0h	ADC Interrupt 3 Results Ready Flag. This flag is set when the conversions results associated with ADCINT3 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT3 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.

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Table 3-1201. ADC_R_CFG_ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ADCINT2RESULT	R	0h	ADC Interrupt 2 Results Ready Flag. This flag is set when the conversions results associated with ADCINT2 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT2 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.
4	ADCINT1RESULT	R	0h	ADC Interrupt 1 Results Ready Flag. This flag is set when the conversions results associated with ADCINT1 latch into the corresponding results register. 0 Conversion results have not latched 1 Conversion results have latched This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register. This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT1 flag. In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE. In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.
3	ADCINT4	R	0h	ADC Interrupt 4 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
2	ADCINT3	R	0h	ADC Interrupt 3 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
1	ADCINT2	R	0h	ADC Interrupt 2 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

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Table 3-1201. ADC_R_CFG_ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADCINT1	R	0h	ADC Interrupt 1 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

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3.14.2.5 ADC_R_CFG_ADCINTFLGCLR Register

3.14.2.5.1 ADC_R_CFG_ADCINTFLGCLR Register (Offset = 8h) [reset = 0h]

ADC Interrupt Flag Clear Register.

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Table 3-1202. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5008h
ADC_R1	502C 7008h

Figure 3-648. ADC_R_CFG_ADCINTFLGCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 3-1203. ADC_R_CFG_ADCINTFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	ADCINT4	R/W1TS	0h	ADC Interrupt 4 Flag Clear. Reads return 0. 0 No action 1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
2	ADCINT3	R/W1TS	0h	ADC Interrupt 3 Flag Clear. Reads return 0. 0 No action 1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
1	ADCINT2	R/W1TS	0h	ADC Interrupt 2 Flag Clear. Reads return 0. 0 No action 1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
0	ADCINT1	R/W1TS	0h	ADC Interrupt 1 Flag Clear. Reads return 0. 0 No action 1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set

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3.14.2.6 ADC_R_CFG_ADCINTOVF Register

3.14.2.6.1 ADC_R_CFG_ADCINTOVF Register (Offset = Ah) [reset = 0h]

ADC Interrupt Overflow Register.

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Table 3-1204. Instance Table

Instance Name	Physical Address
ADC_R0	502C 500Ah
ADC_R1	502C 700Ah

Figure 3-649. ADC_R_CFG_ADCINTOVF Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R	R	R	R
0h				0h	0h	0h	0h

Table 3-1205. ADC_R_CFG_ADCINTOVF Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	ADCINT4	R	0h	ADC Interrupt 4 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
2	ADCINT3	R	0h	ADC Interrupt 3 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
1	ADCINT2	R	0h	ADC Interrupt 2 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.

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Table 3-1205. ADC_R_CFG_ADCINTOVF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADCINT1	R	0h	ADC Interrupt 1 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.

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3.14.2.7 ADC_R_CFG_ADCINTOVFCLR Register

3.14.2.7.1 ADC_R_CFG_ADCINTOVFCLR Register (Offset = Ch) [reset = 0h]

ADC Interrupt Overflow Clear Register.

Return to Summary Table

Table 3-1206. Instance Table

Instance Name	Physical Address
ADC_R0	502C 500Ch
ADC_R1	502C 700Ch

Figure 3-650. ADC_R_CFG_ADCINTOVFCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 3-1207. ADC_R_CFG_ADCINTOVFCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED_1	R	0h	Reserved
3	ADCINT4	R/W1TS	0h	ADC Interrupt 4 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
2	ADCINT3	R/W1TS	0h	ADC Interrupt 3 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
1	ADCINT2	R/W1TS	0h	ADC Interrupt 2 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
0	ADCINT1	R/W1TS	0h	ADC Interrupt 1 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.

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3.14.2.8 ADC_R_CFG_ADCINTSEL1N2 Register

3.14.2.8.1 ADC_R_CFG_ADCINTSEL1N2 Register (Offset = Eh) [reset = 0h]

ADC Interrupt 1 and 2 Selection Register.

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Table 3-1208. Instance Table

Instance Name	Physical Address
ADC_R0	502C 500Eh
ADC_R1	502C 700Eh

Figure 3-651. ADC_R_CFG_ADCINTSEL1N2 Name Register

15	14	13	12	11	10	9	8
RESERVED_2	INT2CONT	INT2E	INT2SEL				
R	R/W	R/W	R/W				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	INT1CONT	INT1E	INT1SEL				
R	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 3-1209. ADC_R_CFG_ADCINTSEL1N2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_2	R	0h	Reserved
14	INT2CONT	R/W	0h	ADCINT2 Continue to Interrupt Mode 0 No further ADCINT2 pulses are generated until ADCINT2 flag [in ADCINTFLG register] is cleared by user. 1 ADCINT2 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT2E	R/W	0h	ADCINT2 Interrupt Enable 0 ADCINT2 is disabled 1 ADCINT2 is enabled
12:8	INT2SEL	R/W	0h	ADCINT2 EOC Source Select 00h EOC0 is trigger for ADCINT2 01h EOC1 is trigger for ADCINT2 02h EOC2 is trigger for ADCINT2 03h EOC3 is trigger for ADCINT2 04h EOC4 is trigger for ADCINT2 05h EOC5 is trigger for ADCINT2 06h EOC6 is trigger for ADCINT2 07h EOC7 is trigger for ADCINT2 08h EOC8 is trigger for ADCINT2 09h EOC9 is trigger for ADCINT2 0Ah EOC10 is trigger for ADCINT2 0Bh EOC11 is trigger for ADCINT2 0Ch EOC12 is trigger for ADCINT2 0Dh EOC13 is trigger for ADCINT2 0Eh EOC14 is trigger for ADCINT2 0Fh EOC15 is trigger for ADCINT2 10h OSINT1 is trigger for ADCINT2 11h OSINT2 is trigger for ADCINT2 12h OSINT3 is trigger for ADCINT2 13h OSINT4 is trigger for ADCINT2
7	RESERVED_1	R	0h	Reserved
6	INT1CONT	R/W	0h	ADCINT1 Continue to Interrupt Mode 0 No further ADCINT1 pulses are generated until ADCINT1 flag [in ADCINTFLG register] is cleared by user. 1 ADCINT1 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.

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Table 3-1209. ADC_R_CFG_ADCINTSEL1N2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT1E	R/W	0h	ADCINT1 Interrupt Enable 0 ADCINT1 is disabled 1 ADCINT1 is enabled
4:0	INT1SEL	R/W	0h	ADCINT1 EOC Source Select 00h EOC0 is trigger for ADCINT1 01h EOC1 is trigger for ADCINT1 02h EOC2 is trigger for ADCINT1 03h EOC3 is trigger for ADCINT1 04h EOC4 is trigger for ADCINT1 05h EOC5 is trigger for ADCINT1 06h EOC6 is trigger for ADCINT1 07h EOC7 is trigger for ADCINT1 08h EOC8 is trigger for ADCINT1 09h EOC9 is trigger for ADCINT1 0Ah EOC10 is trigger for ADCINT1 0Bh EOC11 is trigger for ADCINT1 0Ch EOC12 is trigger for ADCINT1 0Dh EOC13 is trigger for ADCINT1 0Eh EOC14 is trigger for ADCINT1 0Fh EOC15 is trigger for ADCINT1 10h OSINT1 is trigger for ADCINT1 11h OSINT2 is trigger for ADCINT1 12h OSINT3 is trigger for ADCINT1 13h OSINT4 is trigger for ADCINT1

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3.14.2.9 ADC_R_CFG_ADCINTSEL3N4 Register

3.14.2.9.1 ADC_R_CFG_ADCINTSEL3N4 Register (Offset = 10h) [reset = 0h]

ADC Interrupt 3 and 4 Selection Register.

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Table 3-1210. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5010h
ADC_R1	502C 7010h

Figure 3-652. ADC_R_CFG_ADCINTSEL3N4 Name Register

15	14	13	12	11	10	9	8
RESERVED_2	INT4CONT	INT4E	INT4SEL				
R	R/W	R/W	R/W				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	INT3CONT	INT3E	INT3SEL				
R	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 3-1211. ADC_R_CFG_ADCINTSEL3N4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_2	R	0h	Reserved
14	INT4CONT	R/W	0h	ADCINT4 Continue to Interrupt Mode 0 No further ADCINT4 pulses are generated until ADCINT4 flag [in ADCINTFLG register] is cleared by user. 1 ADCINT4 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT4E	R/W	0h	ADCINT4 Interrupt Enable 0 ADCINT4 is disabled 1 ADCINT4 is enabled
12:8	INT4SEL	R/W	0h	ADCINT4 EOC Source Select 00h EOC0 is trigger for ADCINT4 01h EOC1 is trigger for ADCINT4 02h EOC2 is trigger for ADCINT4 03h EOC3 is trigger for ADCINT4 04h EOC4 is trigger for ADCINT4 05h EOC5 is trigger for ADCINT4 06h EOC6 is trigger for ADCINT4 07h EOC7 is trigger for ADCINT4 08h EOC8 is trigger for ADCINT4 09h EOC9 is trigger for ADCINT4 0Ah EOC10 is trigger for ADCINT4 0Bh EOC11 is trigger for ADCINT4 0Ch EOC12 is trigger for ADCINT4 0Dh EOC13 is trigger for ADCINT4 0Eh EOC14 is trigger for ADCINT4 0Fh EOC15 is trigger for ADCINT4 10hOSINT1 is trigger for ADCINT4 11hOSINT2 is trigger for ADCINT4 12hOSINT3 is trigger for ADCINT4 13hOSINT4 is trigger for ADCINT4
7	RESERVED_1	R	0h	Reserved
6	INT3CONT	R/W	0h	ADCINT3 Continue to Interrupt Mode 0 No further ADCINT3 pulses are generated until ADCINT3 flag [in ADCINTFLG register] is cleared by user. 1 ADCINT3 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.

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Table 3-1211. ADC_R_CFG_ADCINTSEL3N4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	INT3E	R/W	0h	ADCINT3 Interrupt Enable 0 ADCINT3 is disabled 1 ADCINT3 is enabled
4:0	INT3SEL	R/W	0h	ADCINT3 EOC Source Select 00h EOC0 is trigger for ADCINT3 01h EOC1 is trigger for ADCINT3 02h EOC2 is trigger for ADCINT3 03h EOC3 is trigger for ADCINT3 04h EOC4 is trigger for ADCINT3 05h EOC5 is trigger for ADCINT3 06h EOC6 is trigger for ADCINT3 07h EOC7 is trigger for ADCINT3 08h EOC8 is trigger for ADCINT3 09h EOC9 is trigger for ADCINT3 0Ah EOC10 is trigger for ADCINT3 0Bh EOC11 is trigger for ADCINT3 0Ch EOC12 is trigger for ADCINT3 0Dh EOC13 is trigger for ADCINT3 0Eh EOC14 is trigger for ADCINT3 0Fh EOC15 is trigger for ADCINT3 10h OSINT1 is trigger for ADCINT3 11h OSINT2 is trigger for ADCINT3 12h OSINT3 is trigger for ADCINT3 13h OSINT4 is trigger for ADCINT3

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3.14.2.10 ADC_R_CFG_ADCSOCPRICTL Register

3.14.2.10.1 ADC_R_CFG_ADCSOCPRICTL Register (Offset = 12h) [reset = 200h]

ADC SOC Priority Control Register.

Return to Summary Table

Table 3-1212. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5012h
ADC_R1	502C 7012h

Figure 3-653. ADC_R_CFG_ADCSOCPRICTL Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED_1</td><td colspan="2">RRPOINTER</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">10h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RRPOINTER</td><td colspan="5">SOCPRIORITY</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">10h</td><td colspan="5">0h</td></tr>
</table>

Table 3-1213. ADC_R_CFG_ADCSOCPRICTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved

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Table 3-1213. ADC_R_CFG_ADCSOCPRICTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:5	RRPOINTER	R	10h	Round Robin Pointer. Holds the value of the last converted round robin SOCx to be used by the round robin scheme to determine order of conversions. 00h SOC0 was last round robin SOC to convert, SOC1 is highest round robin priority. 01h SOC1 was last round robin SOC to convert, SOC2 is highest round robin priority. 02h SOC2 was last round robin SOC to convert, SOC3 is highest round robin priority. 03h SOC3 was last round robin SOC to convert, SOC4 is highest round robin priority. 04h SOC4 was last round robin SOC to convert, SOC5 is highest round robin priority. 05h SOC5 was last round robin SOC to convert, SOC6 is highest round robin priority. 06h SOC6 was last round robin SOC to convert, SOC7 is highest round robin priority. 07h SOC7 was last round robin SOC to convert, SOC8 is highest round robin priority. 08h SOC8 was last round robin SOC to convert, SOC9 is highest round robin priority. 09h SOC9 was last round robin SOC to convert, SOC10 is highest round robin priority. 0Ah SOC10 was last round robin SOC to convert, SOC11 is highest round robin priority. 0Bh SOC11 was last round robin SOC to convert, SOC12 is highest round robin priority. 0Ch SOC12 was last round robin SOC to convert, SOC13 is highest round robin priority. 0Dh SOC13 was last round robin SOC to convert, SOC14 is highest round robin priority. 0Eh SOC14 was last round robin SOC to convert, SOC15 is highest round robin priority. 0Fh SOC15 was last round robin SOC to convert, SOC0 is highest round robin priority. 10h Reset value to indicate no SOC has been converted. SOC0 is highest round robin priority. Set to this value when the ADC module is reset by SOFTPRES or when the ADCSOCPRICTL register is written. In the latter case, if a conversion is currently in progress, it will complete and then the new priority will take effect. Others Invalid value.

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Table 3-1213. ADC_R_CFG_ADCSOCPRICTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	SOCPRIORITY	R/W	0h	SOC Priority Determines the cutoff point for priority mode and round robin arbitration for SOCx 00h SOC priority is handled in round robin mode for all channels. 01h SOC0 is high priority, rest of channels are in round robin mode. 02h SOC0-SOC1 are high priority, SOC2-SOC15 are in round robin mode. 03h SOC0-SOC2 are high priority, SOC3-SOC15 are in round robin mode. 04h SOC0-SOC3 are high priority, SOC4-SOC15 are in round robin mode. 05h SOC0-SOC4 are high priority, SOC5-SOC15 are in round robin mode. 06h SOC0-SOC5 are high priority, SOC6-SOC15 are in round robin mode. 07h SOC0-SOC6 are high priority, SOC7-SOC15 are in round robin mode. 08h SOC0-SOC7 are high priority, SOC8-SOC15 are in round robin mode. 09h SOC0-SOC8 are high priority, SOC9-SOC15 are in round robin mode. 0Ah SOC0-SOC9 are high priority, SOC10-SOC15 are in round robin mode. 0Bh SOC0-SOC10 are high priority, SOC11-SOC15 are in round robin mode. 0Ch SOC0-SOC11 are high priority, SOC12-SOC15 are in round robin mode. 0Dh SOC0-SOC12 are high priority, SOC13-SOC15 are in round robin mode. 0Eh SOC0-SOC13 are high priority, SOC14-SOC15 are in round robin mode. 0Fh SOC0-SOC14 are high priority, SOC15 is in round robin mode. 10h All SOCs are in high priority mode, arbitrated by SOC number. Others Invalid selection.

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3.14.2.11 ADC_R_CFG_ADCINTSOCSEL1 Register

3.14.2.11.1 ADC_R_CFG_ADCINTSOCSEL1 Register (Offset = 14h) [reset = 0h]

ADC Interrupt SOC Selection 1 Register.

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Table 3-1214. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5014h
ADC_R1	502C 7014h

Figure 3-654. ADC_R_CFG_ADCINTSOCSEL1 Name Register

15	14	13	12	11	10	9	8
SOC7		SOC6		SOC5		SOC4	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SOC3		SOC2		SOC1		SOC0	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-1215. ADC_R_CFG_ADCINTSOCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SOC7	R/W	0h	SOC7 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC7. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC7. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC7. 10 ADCINT2 will trigger SOC7. 11 Invalid selection.
13:12	SOC6	R/W	0h	SOC6 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC6. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC6. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC6. 10 ADCINT2 will trigger SOC6. 11 Invalid selection.
11:10	SOC5	R/W	0h	SOC5 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC5. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC5. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC5. 10 ADCINT2 will trigger SOC5. 11 Invalid selection.
9:8	SOC4	R/W	0h	SOC4 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC4. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC4. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC4. 10 ADCINT2 will trigger SOC4. 11 Invalid selection.

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Table 3-1215. ADC_R_CFG_ADCINTSOCSEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	SOC3	R/W	0h	SOC3 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC3. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC3. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC3. 10 ADCINT2 will trigger SOC3. 11 Invalid selection.
5:4	SOC2	R/W	0h	SOC2 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC2. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC2. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC2. 10 ADCINT2 will trigger SOC2. 11 Invalid selection.
3:2	SOC1	R/W	0h	SOC1 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC1. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC1. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC1. 10 ADCINT2 will trigger SOC1. 11 Invalid selection.
1:0	SOC0	R/W	0h	SOC0 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC0. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC0. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC0. 10 ADCINT2 will trigger SOC0. 11 Invalid selection.

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3.14.2.12 ADC_R_CFG_ADCINTSOCSEL2 Register

3.14.2.12.1 ADC_R_CFG_ADCINTSOCSEL2 Register (Offset = 16h) [reset = 0h]

ADC Interrupt SOC Selection 2 Register.

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Table 3-1216. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5016h
ADC_R1	502C 7016h

Figure 3-655. ADC_R_CFG_ADCINTSOCSEL2 Name Register

15	14	13	12	11	10	9	8
SOC15		SOC14		SOC13		SOC12	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
SOC11		SOC10		SOC9		SOC8	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-1217. ADC_R_CFG_ADCINTSOCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SOC15	R/W	0h	SOC15 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC15. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC15. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC15. 10 ADCINT2 will trigger SOC15. 11 Invalid selection.
13:12	SOC14	R/W	0h	SOC14 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC14. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC14. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC14. 10 ADCINT2 will trigger SOC14. 11 Invalid selection.
11:10	SOC13	R/W	0h	SOC13 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC13. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC13. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC13. 10 ADCINT2 will trigger SOC13. 11 Invalid selection.
9:8	SOC12	R/W	0h	SOC12 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC12. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC12. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC12. 10 ADCINT2 will trigger SOC12. 11 Invalid selection.

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Table 3-1217. ADC_R_CFG_ADCINTSOCSEL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	SOC11	R/W	0h	SOC11 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC11. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC11. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC11. 10 ADCINT2 will trigger SOC11. 11 Invalid selection.
5:4	SOC10	R/W	0h	SOC10 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC10. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC10. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC10. 10 ADCINT2 will trigger SOC10. 11 Invalid selection.
3:2	SOC9	R/W	0h	SOC9 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC9. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC9. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC9. 10 ADCINT2 will trigger SOC9. 11 Invalid selection.
1:0	SOC8	R/W	0h	SOC8 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC8. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC8. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC8. 10 ADCINT2 will trigger SOC8. 11 Invalid selection.

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3.14.2.13 ADC_R_CFG_ADCSOCFLG1 Register

3.14.2.13.1 ADC_R_CFG_ADCSOCFLG1 Register (Offset = 18h) [reset = 0h]

ADC SOC Flag 1 Register.

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Table 3-1218. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5018h
ADC_R1	502C 7018h

Figure 3-656. ADC_R_CFG_ADCSOCFLG1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1219. ADC_R_CFG_ADCSOCFLG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R	0h	SOC15 Start of Conversion Flag. Indicates the state of SOC15 conversions. 0 No sample pending for SOC15. 1 Trigger has been received and sample is pending for SOC15. This bit will be automatically cleared when the SOC15 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
14	SOC14	R	0h	SOC14 Start of Conversion Flag. Indicates the state of SOC14 conversions. 0 No sample pending for SOC14. 1 Trigger has been received and sample is pending for SOC14. This bit will be automatically cleared when the SOC14 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
13	SOC13	R	0h	SOC13 Start of Conversion Flag. Indicates the state of SOC13 conversions. 0 No sample pending for SOC13. 1 Trigger has been received and sample is pending for SOC13. This bit will be automatically cleared when the SOC13 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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Table 3-1219. ADC_R_CFG_ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	SOC12	R	0h	SOC12 Start of Conversion Flag. Indicates the state of SOC12 conversions. 0 No sample pending for SOC12. 1 Trigger has been received and sample is pending for SOC12. This bit will be automatically cleared when the SOC12 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
11	SOC11	R	0h	SOC11 Start of Conversion Flag. Indicates the state of SOC11 conversions. 0 No sample pending for SOC11. 1 Trigger has been received and sample is pending for SOC11. This bit will be automatically cleared when the SOC11 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
10	SOC10	R	0h	SOC10 Start of Conversion Flag. Indicates the state of SOC10 conversions. 0 No sample pending for SOC10. 1 Trigger has been received and sample is pending for SOC10. This bit will be automatically cleared when the SOC10 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
9	SOC9	R	0h	SOC9 Start of Conversion Flag. Indicates the state of SOC9 conversions. 0 No sample pending for SOC9. 1 Trigger has been received and sample is pending for SOC9. This bit will be automatically cleared when the SOC9 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
8	SOC8	R	0h	SOC8 Start of Conversion Flag. Indicates the state of SOC8 conversions. 0 No sample pending for SOC8. 1 Trigger has been received and sample is pending for SOC8. This bit will be automatically cleared when the SOC8 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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Table 3-1219. ADC_R_CFG_ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SOC7	R	0h	SOC7 Start of Conversion Flag. Indicates the state of SOC7 conversions. 0 No sample pending for SOC7. 1 Trigger has been received and sample is pending for SOC7. This bit will be automatically cleared when the SOC7 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
6	SOC6	R	0h	SOC6 Start of Conversion Flag. Indicates the state of SOC6 conversions. 0 No sample pending for SOC6. 1 Trigger has been received and sample is pending for SOC6. This bit will be automatically cleared when the SOC6 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
5	SOC5	R	0h	SOC5 Start of Conversion Flag. Indicates the state of SOC5 conversions. 0 No sample pending for SOC5. 1 Trigger has been received and sample is pending for SOC5. This bit will be automatically cleared when the SOC5 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
4	SOC4	R	0h	SOC4 Start of Conversion Flag. Indicates the state of SOC4 conversions. 0 No sample pending for SOC4. 1 Trigger has been received and sample is pending for SOC4. This bit will be automatically cleared when the SOC4 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
3	SOC3	R	0h	SOC3 Start of Conversion Flag. Indicates the state of SOC3 conversions. 0 No sample pending for SOC3. 1 Trigger has been received and sample is pending for SOC3. This bit will be automatically cleared when the SOC3 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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Table 3-1219. ADC_R_CFG_ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SOC2	R	0h	SOC2 Start of Conversion Flag. Indicates the state of SOC2 conversions. 0 No sample pending for SOC2. 1 Trigger has been received and sample is pending for SOC2. This bit will be automatically cleared when the SOC2 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
1	SOC1	R	0h	SOC1 Start of Conversion Flag. Indicates the state of SOC1 conversions. 0 No sample pending for SOC1. 1 Trigger has been received and sample is pending for SOC1. This bit will be automatically cleared when the SOC1 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
0	SOC0	R	0h	SOC0 Start of Conversion Flag. Indicates the state of SOC0 conversions. 0 No sample pending for SOC0. 1 Trigger has been received and sample is pending for SOC0. This bit will be automatically cleared when the SOC0 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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3.14.2.14 ADC_R_CFG_ADCSOCFRC1 Register

3.14.2.14.1 ADC_R_CFG_ADCSOCFRC1 Register (Offset = 1Ah) [reset = 0h]

ADC SOC Force 1 Register.

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Table 3-1220. Instance Table

Instance Name	Physical Address
ADC_R0	502C 501Ah
ADC_R1	502C 701Ah

Figure 3-657. ADC_R_CFG_ADCSOCFRC1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1221. ADC_R_CFG_ADCSOCFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R/W1TS	0h	SOC15 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC15 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC15 flag bit to 1. This will cause a conversion to start once priority is given to SOC15. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC15 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
14	SOC14	R/W1TS	0h	SOC14 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC14 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC14 flag bit to 1. This will cause a conversion to start once priority is given to SOC14. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC14 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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Table 3-1221. ADC_R_CFG_ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SOC13	R/W1TS	0h	SOC13 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC13 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC13 flag bit to 1. This will cause a conversion to start once priority is given to SOC13. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC13 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
12	SOC12	R/W1TS	0h	SOC12 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC12 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC12 flag bit to 1. This will cause a conversion to start once priority is given to SOC12. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC12 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
11	SOC11	R/W1TS	0h	SOC11 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC11 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC11 flag bit to 1. This will cause a conversion to start once priority is given to SOC11. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC11 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
10	SOC10	R/W1TS	0h	SOC10 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC10 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC10 flag bit to 1. This will cause a conversion to start once priority is given to SOC10. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC10 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
9	SOC9	R/W1TS	0h	SOC9 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC9 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC9 flag bit to 1. This will cause a conversion to start once priority is given to SOC9. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC9 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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Table 3-1221. ADC_R_CFG_ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SOC8	R/W1TS	0h	SOC8 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC8 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC8 flag bit to 1. This will cause a conversion to start once priority is given to SOC8. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC8 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
7	SOC7	R/W1TS	0h	SOC7 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC7 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC7 flag bit to 1. This will cause a conversion to start once priority is given to SOC7. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC7 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
6	SOC6	R/W1TS	0h	SOC6 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC6 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC6 flag bit to 1. This will cause a conversion to start once priority is given to SOC6. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC6 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
5	SOC5	R/W1TS	0h	SOC5 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC5 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC5 flag bit to 1. This will cause a conversion to start once priority is given to SOC5. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC5 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
4	SOC4	R/W1TS	0h	SOC4 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC4 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC4 flag bit to 1. This will cause a conversion to start once priority is given to SOC4. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC4 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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Table 3-1221. ADC_R_CFG_ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SOC3	R/W1TS	0h	SOC3 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC3 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC3 flag bit to 1. This will cause a conversion to start once priority is given to SOC3. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC3 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
2	SOC2	R/W1TS	0h	SOC2 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC2 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC2 flag bit to 1. This will cause a conversion to start once priority is given to SOC2. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC2 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
1	SOC1	R/W1TS	0h	SOC1 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC1 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC1 flag bit to 1. This will cause a conversion to start once priority is given to SOC1. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC1 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
0	SOC0	R/W1TS	0h	SOC0 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC0 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC0 flag bit to 1. This will cause a conversion to start once priority is given to SOC0. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC0 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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3.14.2.15 ADC_R_CFG_ADCSOCOVF1 Register

3.14.2.15.1 ADC_R_CFG_ADCSOCOVF1 Register (Offset = 1Ch) [reset = 0h]

ADC SOC Overflow 1 Register.

Return to Summary Table

Table 3-1222. Instance Table

Instance Name	Physical Address
ADC_R0	502C 501Ch
ADC_R1	502C 701Ch

Figure 3-658. ADC_R_CFG_ADCSOCOVF1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1223. ADC_R_CFG_ADCSOCOVF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R	0h	SOC15 Start of Conversion Overflow Flag. Indicates an SOC15 event was generated in hardware while an existing SOC15 event was already pending. 0 No SOC15 event overflow. 1 SOC15 event overflow. An overflow condition does not stop SOC15 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
14	SOC14	R	0h	SOC14 Start of Conversion Overflow Flag. Indicates an SOC14 event was generated in hardware while an existing SOC14 event was already pending. 0 No SOC14 event overflow. 1 SOC14 event overflow. An overflow condition does not stop SOC14 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
13	SOC13	R	0h	SOC13 Start of Conversion Overflow Flag. Indicates an SOC13 event was generated in hardware while an existing SOC13 event was already pending. 0 No SOC13 event overflow. 1 SOC13 event overflow. An overflow condition does not stop SOC13 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
12	SOC12	R	0h	SOC12 Start of Conversion Overflow Flag. Indicates an SOC12 event was generated in hardware while an existing SOC12 event was already pending. 0 No SOC12 event overflow. 1 SOC12 event overflow. An overflow condition does not stop SOC12 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.

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Table 3-1223. ADC_R_CFG_ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	R	0h	SOC11 Start of Conversion Overflow Flag. Indicates an SOC11 event was generated in hardware while an existing SOC11 event was already pending. 0 No SOC11 event overflow. 1 SOC11 event overflow. An overflow condition does not stop SOC11 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
10	SOC10	R	0h	SOC10 Start of Conversion Overflow Flag. Indicates an SOC10 event was generated in hardware while an existing SOC10 event was already pending. 0 No SOC10 event overflow. 1 SOC10 event overflow. An overflow condition does not stop SOC10 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
9	SOC9	R	0h	SOC9 Start of Conversion Overflow Flag. Indicates an SOC9 event was generated in hardware while an existing SOC9 event was already pending. 0 No SOC9 event overflow. 1 SOC9 event overflow. An overflow condition does not stop SOC9 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
8	SOC8	R	0h	SOC8 Start of Conversion Overflow Flag. Indicates an SOC8 event was generated in hardware while an existing SOC8 event was already pending. 0 No SOC8 event overflow. 1 SOC8 event overflow. An overflow condition does not stop SOC8 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
7	SOC7	R	0h	SOC7 Start of Conversion Overflow Flag. Indicates an SOC7 event was generated in hardware while an existing SOC7 event was already pending. 0 No SOC7 event overflow. 1 SOC7 event overflow. An overflow condition does not stop SOC7 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
6	SOC6	R	0h	SOC6 Start of Conversion Overflow Flag. Indicates an SOC6 event was generated in hardware while an existing SOC6 event was already pending. 0 No SOC6 event overflow. 1 SOC6 event overflow. An overflow condition does not stop SOC6 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
5	SOC5	R	0h	SOC5 Start of Conversion Overflow Flag. Indicates an SOC5 event was generated in hardware while an existing SOC5 event was already pending. 0 No SOC5 event overflow. 1 SOC5 event overflow. An overflow condition does not stop SOC5 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
4	SOC4	R	0h	SOC4 Start of Conversion Overflow Flag. Indicates an SOC4 event was generated in hardware while an existing SOC4 event was already pending. 0 No SOC4 event overflow. 1 SOC4 event overflow. An overflow condition does not stop SOC4 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.

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Table 3-1223. ADC_R_CFG_ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SOC3	R	0h	SOC3 Start of Conversion Overflow Flag. Indicates an SOC3 event was generated in hardware while an existing SOC3 event was already pending. 0 No SOC3 event overflow. 1 SOC3 event overflow. An overflow condition does not stop SOC3 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
2	SOC2	R	0h	SOC2 Start of Conversion Overflow Flag. Indicates an SOC2 event was generated in hardware while an existing SOC2 event was already pending. 0 No SOC2 event overflow. 1 SOC2 event overflow. An overflow condition does not stop SOC2 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
1	SOC1	R	0h	SOC1 Start of Conversion Overflow Flag. Indicates an SOC1 event was generated in hardware while an existing SOC1 event was already pending. 0 No SOC1 event overflow. 1 SOC1 event overflow. An overflow condition does not stop SOC1 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.
0	SOC0	R	0h	SOC0 Start of Conversion Overflow Flag. Indicates an SOC0 event was generated in hardware while an existing SOC0 event was already pending. 0 No SOC0 event overflow. 1 SOC0 event overflow. An overflow condition does not stop SOC0 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.

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3.14.2.16 ADC_R_CFG_ADCSOCOVFCLR1 Register

3.14.2.16.1 ADC_R_CFG_ADCSOCOVFCLR1 Register (Offset = 1Eh) [reset = 0h]

ADC SOC Overflow Clear 1 Register.

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Table 3-1224. Instance Table

Instance Name	Physical Address
ADC_R0	502C 501Eh
ADC_R1	502C 701Eh

Figure 3-659. ADC_R_CFG_ADCSOCOVFCLR1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1225. ADC_R_CFG_ADCSOCOVFCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R/W1TS	0h	SOC15 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC15 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC15 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
14	SOC14	R/W1TS	0h	SOC14 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC14 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC14 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
13	SOC13	R/W1TS	0h	SOC13 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC13 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC13 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
12	SOC12	R/W1TS	0h	SOC12 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC12 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC12 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

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Table 3-1225. ADC_R_CFG_ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	R/W1TS	0h	SOC11 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC11 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC11 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
10	SOC10	R/W1TS	0h	SOC10 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC10 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC10 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
9	SOC9	R/W1TS	0h	SOC9 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC9 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC9 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
8	SOC8	R/W1TS	0h	SOC8 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC8 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC8 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
7	SOC7	R/W1TS	0h	SOC7 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC7 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC7 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
6	SOC6	R/W1TS	0h	SOC6 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC6 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC6 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
5	SOC5	R/W1TS	0h	SOC5 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC5 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC5 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
4	SOC4	R/W1TS	0h	SOC4 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC4 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC4 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

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Table 3-1225. ADC_R_CFG_ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SOC3	R/W1TS	0h	SOC3 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC3 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC3 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
2	SOC2	R/W1TS	0h	SOC2 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC2 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC2 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
1	SOC1	R/W1TS	0h	SOC1 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC1 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC1 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
0	SOC0	R/W1TS	0h	SOC0 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC0 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC0 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

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3.14.2.17 ADC_R_CFG_ADCSOC0CTL Register

3.14.2.17.1 ADC_R_CFG_ADCSOC0CTL Register (Offset = 20h) [reset = 0h]

ADC SOC0 Control Register.

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Table 3-1226. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5020h
ADC_R1	502C 7020h

Figure 3-660. ADC_R_CFG_ADCSOC0CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-1227. ADC_R_CFG_ADCSOC0CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC0 External Channel Mux Select. Selects the external mux combination to output when SOC0 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1227. ADC_R_CFG_ADCSOC0CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC0 Trigger Source Select. Along with the SOC0 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC0 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1227. ADC_R_CFG_ADCSOC0CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC0 Channel Select. Selects the channel to be converted when SOC0 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC0 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.18 ADC_R_CFG_ADCSOC1CTL Register

3.14.2.18.1 ADC_R_CFG_ADCSOC1CTL Register (Offset = 24h) [reset = 0h]

ADC SOC1 Control Register.

Return to Summary Table

Table 3-1228. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5024h
ADC_R1	502C 7024h

Figure 3-661. ADC_R_CFG_ADCSOC1CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	22	21	20	19	18	17	16
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	6	5	4	3	2	1	0
ACQPS							
R/W							
0h							

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Table 3-1229. ADC_R_CFG_ADCSOC1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC1 External Channel Mux Select. Selects the external mux combination to output when SOC1 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1229. ADC_R_CFG_ADCSOC1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC1 Trigger Source Select. Along with the SOC1 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC1 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1229. ADC_R_CFG_ADCSOC1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC1 Channel Select. Selects the channel to be converted when SOC1 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC1 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.19 ADC_R_CFG_ADCSOC2CTL Register

3.14.2.19.1 ADC_R_CFG_ADCSOC2CTL Register (Offset = 28h) [reset = 0h]

ADC SOC2 Control Register.

Return to Summary Table

Table 3-1230. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5028h
ADC_R1	502C 7028h

Figure 3-662. ADC_R_CFG_ADCSOC2CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-1231. ADC_R_CFG_ADCSOC2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC2 External Channel Mux Select. Selects the external mux combination to output when SOC2 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1231. ADC_R_CFG_ADCSOC2CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC2 Trigger Source Select. Along with the SOC2 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC2 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1231. ADC_R_CFG_ADCSOC2CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC2 Channel Select. Selects the channel to be converted when SOC2 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC2 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.20 ADC_R_CFG_ADCSOC3CTL Register

3.14.2.20.1 ADC_R_CFG_ADCSOC3CTL Register (Offset = 2Ch) [reset = 0h]

ADC SOC3 Control Register.

Return to Summary Table

Table 3-1232. Instance Table

Instance Name	Physical Address
ADC_R0	502C 502Ch
ADC_R1	502C 702Ch

Figure 3-663. ADC_R_CFG_ADCSOC3CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-1233. ADC_R_CFG_ADCSOC3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC3 External Channel Mux Select. Selects the external mux combination to output when SOC3 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1233. ADC_R_CFG_ADCSOC3CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC3 Trigger Source Select. Along with the SOC3 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC3 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1233. ADC_R_CFG_ADCSOC3CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC3 Channel Select. Selects the channel to be converted when SOC3 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC3 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.21 ADC_R_CFG_ADCSOC4CTL Register

3.14.2.21.1 ADC_R_CFG_ADCSOC4CTL Register (Offset = 30h) [reset = 0h]

ADC SOC4 Control Register.

Return to Summary Table

Table 3-1234. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5030h
ADC_R1	502C 7030h

Figure 3-664. ADC_R_CFG_ADCSOC4CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-1235. ADC_R_CFG_ADCSOC4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC4 External Channel Mux Select. Selects the external mux combination to output when SOC4 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1235. ADC_R_CFG_ADCSOC4CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC4 Trigger Source Select. Along with the SOC4 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC4 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1235. ADC_R_CFG_ADCSOC4CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC4 Channel Select. Selects the channel to be converted when SOC4 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC4 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.22 ADC_R_CFG_ADCSOC5CTL Register

3.14.2.22.1 ADC_R_CFG_ADCSOC5CTL Register (Offset = 34h) [reset = 0h]

ADC SOC5 Control Register.

Return to Summary Table

Table 3-1236. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5034h
ADC_R1	502C 7034h

Figure 3-665. ADC_R_CFG_ADCSOC5CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-1237. ADC_R_CFG_ADCSOC5CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC5 External Channel Mux Select. Selects the external mux combination to output when SOC5 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1237. ADC_R_CFG_ADCSOC5CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC5 Trigger Source Select. Along with the SOC5 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC5 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1237. ADC_R_CFG_ADCSOC5CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC5 Channel Select. Selects the channel to be converted when SOC5 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC5 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.23 ADC_R_CFG_ADCSOC6CTL Register

3.14.2.23.1 ADC_R_CFG_ADCSOC6CTL Register (Offset = 38h) [reset = 0h]

ADC SOC6 Control Register.

Return to Summary Table

Table 3-1238. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5038h
ADC_R1	502C 7038h

Figure 3-666. ADC_R_CFG_ADCSOC6CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-1239. ADC_R_CFG_ADCSOC6CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC6 External Channel Mux Select. Selects the external mux combination to output when SOC6 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1239. ADC_R_CFG_ADCSOC6CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC6 Trigger Source Select. Along with the SOC6 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC6 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1239. ADC_R_CFG_ADCSOC6CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC6 Channel Select. Selects the channel to be converted when SOC6 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC6 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.24 ADC_R_CFG_ADCSOC7CTL Register

3.14.2.24.1 ADC_R_CFG_ADCSOC7CTL Register (Offset = 3Ch) [reset = 0h]

ADC SOC7 Control Register.

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Table 3-1240. Instance Table

Instance Name	Physical Address
ADC_R0	502C 503Ch
ADC_R1	502C 703Ch

Figure 3-667. ADC_R_CFG_ADCSOC7CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-1241. ADC_R_CFG_ADCSOC7CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC7 External Channel Mux Select. Selects the external mux combination to output when SOC7 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1241. ADC_R_CFG_ADCSOC7CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC7 Trigger Source Select. Along with the SOC7 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC7 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1241. ADC_R_CFG_ADCSOC7CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC7 Channel Select. Selects the channel to be converted when SOC7 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC7 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.25 ADC_R_CFG_ADCSOC8CTL Register

3.14.2.25.1 ADC_R_CFG_ADCSOC8CTL Register (Offset = 40h) [reset = 0h]

ADC SOC8 Control Register.

Return to Summary Table

Table 3-1242. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5040h
ADC_R1	502C 7040h

Figure 3-668. ADC_R_CFG_ADCSOC8CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-1243. ADC_R_CFG_ADCSOC8CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC8 External Channel Mux Select. Selects the external mux combination to output when SOC8 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1243. ADC_R_CFG_ADCSOC8CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC8 Trigger Source Select. Along with the SOC8 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC8 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1243. ADC_R_CFG_ADCSOC8CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC8 Channel Select. Selects the channel to be converted when SOC8 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC8 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.26 ADC_R_CFG_ADCSOC9CTL Register

3.14.2.26.1 ADC_R_CFG_ADCSOC9CTL Register (Offset = 44h) [reset = 0h]

ADC SOC9 Control Register.

Return to Summary Table

Table 3-1244. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5044h
ADC_R1	502C 7044h

Figure 3-669. ADC_R_CFG_ADCSOC9CTL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">EXTCHSEL</td><td>RESERVED_2</td><td colspan="3">TRIGSEL</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">TRIGSEL</td><td colspan="4">CHSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>CHSEL</td><td colspan="3">RESOLUTION</td><td colspan="2">SIGNALMODE</td><td>RESERVED_1</td><td>ACQPS</td></tr>
<tr><td>R/W</td><td colspan="3">R</td><td colspan="2">R</td><td>R</td><td>R/W</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ACQPS</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

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Table 3-1245. ADC_R_CFG_ADCSOC9CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC9 External Channel Mux Select. Selects the external mux combination to output when SOC9 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1245. ADC_R_CFG_ADCSOC9CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC9 Trigger Source Select. Along with the SOC9 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC9 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1245. ADC_R_CFG_ADCSOC9CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC9 Channel Select. Selects the channel to be converted when SOC9 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC9 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.27 ADC_R_CFG_ADCSOC10CTL Register

3.14.2.27.1 ADC_R_CFG_ADCSOC10CTL Register (Offset = 48h) [reset = 0h]

ADC SOC10 Control Register.

Return to Summary Table

Table 3-1246. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5048h
ADC_R1	502C 7048h

Figure 3-670. ADC_R_CFG_ADCSOC10CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		

23	22	21	20	19	18	17	16
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			

15	14	13	12	11	10	9	8
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h

7	6	5	4	3	2	1	0
ACQPS							
R/W							
0h							

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Table 3-1247. ADC_R_CFG_ADCSOC10CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC10 External Channel Mux Select. Selects the external mux combination to output when SOC10 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1247. ADC_R_CFG_ADCSOC10CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC10 Trigger Source Select. Along with the SOC10 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC10 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1247. ADC_R_CFG_ADCSOC10CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC10 Channel Select. Selects the channel to be converted when SOC10 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC10 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.28 ADC_R_CFG_ADCSOC11CTL Register

3.14.2.28.1 ADC_R_CFG_ADCSOC11CTL Register (Offset = 4Ch) [reset = 0h]

ADC SOC11 Control Register.

Return to Summary Table

Table 3-1248. Instance Table

Instance Name	Physical Address
ADC_R0	502C 504Ch
ADC_R1	502C 704Ch

Figure 3-671. ADC_R_CFG_ADCSOC11CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-1249. ADC_R_CFG_ADCSOC11CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC11 External Channel Mux Select. Selects the external mux combination to output when SOC11 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1249. ADC_R_CFG_ADCSOC11CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC11 Trigger Source Select. Along with the SOC11 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC11 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1249. ADC_R_CFG_ADCSOC11CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC11 Channel Select. Selects the channel to be converted when SOC11 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC11 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.29 ADC_R_CFG_ADCSOC12CTL Register

3.14.2.29.1 ADC_R_CFG_ADCSOC12CTL Register (Offset = 50h) [reset = 0h]

ADC SOC12 Control Register.

Return to Summary Table

Table 3-1250. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5050h
ADC_R1	502C 7050h

Figure 3-672. ADC_R_CFG_ADCSOC12CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-1251. ADC_R_CFG_ADCSOC12CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC12 External Channel Mux Select. Selects the external mux combination to output when SOC12 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1251. ADC_R_CFG_ADCSOC12CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC12 Trigger Source Select. Along with the SOC12 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC12 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1251. ADC_R_CFG_ADCSOC12CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC12 Channel Select. Selects the channel to be converted when SOC12 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC12 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.30 ADC_R_CFG_ADCSOC13CTL Register

3.14.2.30.1 ADC_R_CFG_ADCSOC13CTL Register (Offset = 54h) [reset = 0h]

ADC SOC13 Control Register.

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Table 3-1252. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5054h
ADC_R1	502C 7054h

Figure 3-673. ADC_R_CFG_ADCSOC13CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-1253. ADC_R_CFG_ADCSOC13CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC13 External Channel Mux Select. Selects the external mux combination to output when SOC13 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1253. ADC_R_CFG_ADCSOC13CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC13 Trigger Source Select. Along with the SOC13 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC13 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1253. ADC_R_CFG_ADCSOC13CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC13 Channel Select. Selects the channel to be converted when SOC13 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC13 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.31 ADC_R_CFG_ADCSOC14CTL Register

3.14.2.31.1 ADC_R_CFG_ADCSOC14CTL Register (Offset = 58h) [reset = 0h]

ADC SOC14 Control Register.

Return to Summary Table

Table 3-1254. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5058h
ADC_R1	502C 7058h

Figure 3-674. ADC_R_CFG_ADCSOC14CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	22	21	20	19	18	17	16
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	6	5	4	3	2	1	0
ACQPS							
R/W							
0h							

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Table 3-1255. ADC_R_CFG_ADCSOC14CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC14 External Channel Mux Select. Selects the external mux combination to output when SOC14 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1255. ADC_R_CFG_ADCSOC14CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC14 Trigger Source Select. Along with the SOC14 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC14 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1255. ADC_R_CFG_ADCSOC14CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC14 Channel Select. Selects the channel to be converted when SOC14 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC14 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.32 ADC_R_CFG_ADCSOC15CTL Register

3.14.2.32.1 ADC_R_CFG_ADCSOC15CTL Register (Offset = 5Ch) [reset = 0h]

ADC SOC15 Control Register.

Return to Summary Table

Table 3-1256. Instance Table

Instance Name	Physical Address
ADC_R0	502C 505Ch
ADC_R1	502C 705Ch

Figure 3-675. ADC_R_CFG_ADCSOC15CTL Name Register

31	30	29	28	27	26	25	24
EXTCHSEL				RESERVED_2	TRIGSEL		
R/W				R	R/W		
0h				0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TRIGSEL				CHSEL			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CHSEL	RESOLUTION			SIGNALMODE		RESERVED_1	ACQPS
R/W	R			R		R	R/W
0h	0h			0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACQPS							
R/W							
0h							

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Table 3-1257. ADC_R_CFG_ADCSOC15CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	EXTCHSEL	R/W	0h	SOC15 External Channel Mux Select. Selects the external mux combination to output when SOC15 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. 0h ADCEXTMUX[3:0] = 0000 1h ADCEXTMUX[3:0] = 0001 2h ADCEXTMUX[3:0] = 0010 3h ADCEXTMUX[3:0] = 0011 4h ADCEXTMUX[3:0] = 0100 5h ADCEXTMUX[3:0] = 0101 6h ADCEXTMUX[3:0] = 0110 7h ADCEXTMUX[3:0] = 0111 8h ADCEXTMUX[3:0] = 1000 9h ADCEXTMUX[3:0] = 1001 Ah ADCEXTMUX[3:0] = 1010 Bh ADCEXTMUX[3:0] = 1011 Ch ADCEXTMUX[3:0] = 1100 Dh ADCEXTMUX[3:0] = 1101 Eh ADCEXTMUX[3:0] = 1110 Fh ADCEXTMUX[3:0] = 1111
27	RESERVED_2	R	0h	Reserved

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Table 3-1257. ADC_R_CFG_ADCSOC15CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26:20	TRIGSEL	R/W	0h	SOC15 Trigger Source Select. Along with the SOC15 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC15 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. Note: SOCFRC1 register can always be used to software trigger SOCs in addition to any hardware trigger configuration. 00h ADCTRIG0 - Software only 01h ADCTRIG1 - RTI0 Timer 02h ADCTRIG2 - RTI1 Timer 03h ADCTRIG3 - RTI2 Timer 04h ADCTRIG4 - RTI3 Timer 05h ADCTRIG5 - InputXBAR.Out[5] 06h ADCTRIG6 - spare 07h ADCTRIG7 - spare 08h ADCTRIG8 - EPWM0, ADCSOCA 09h ADCTRIG9 - EPWM0, ADCSOCB 0Ah ADCTRIG10 - EPWM1, ADCSOCA 0Bh ADCTRIG11 - EPWM1, ADCSOCB 0Ch ADCTRIG12 - EPWM2, ADCSOCA 0Dh ADCTRIG13 - EPWM2, ADCSOCB 0Eh ADCTRIG14 - EPWM3, ADCSOCA 0Fh ADCTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h ADCTRIG64 - EPWM28, ADCSOCA 41h ADCTRIG65 - EPWM28, ADCSOCB 42h ADCTRIG66 - EPWM29, ADCSOCA 43h ADCTRIG67 - EPWM29, ADCSOCB 44h ADCTRIG68 - EPWM30, ADCSOCA 45h ADCTRIG69 - EPWM30, ADCSOCB 46h ADCTRIG70 - EPWM31, ADCSOCA 47h ADCTRIG71 - EPWM31, ADCSOCB 48h ADCTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h ADCTRIG81 - ECAP9, TRIGOUT 52h ADCTRIG82 - ECAP10, TRIGOUT .... 57h ADCTRIG87 - ECAP15, TRIGOUT 58h ADCTRIG88 - RTI4 Timer 59h ADCTRIG89 - RTI5 Timer 5Ah ADCTRIG90 - RTI6 Timer 5Bh ADCTRIG91 - RTI7 Timer .... 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.

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Table 3-1257. ADC_R_CFG_ADCSOC15CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:15	CHSEL	R/W	0h	SOC15 Channel Select. Selects the channel to be converted when SOC15 is received by the ADC. Single-ended Signaling Mode [SIGNALMODE = 0]: 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31 Differential Signaling Mode [SIGNALMODE = 1]: 00h ADCIN0 [non-inverting] and ADCIN1 [inverting] 01h ADCIN0 [non-inverting] and ADCIN1 [inverting] 02h ADCIN2 [non-inverting] and ADCIN3 [inverting] 03h ADCIN2 [non-inverting] and ADCIN3 [inverting] 04h ADCIN4 [non-inverting] and ADCIN5 [inverting] 05h ADCIN4 [non-inverting] and ADCIN5 [inverting] ... 0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting] 0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting] 10h ADCIN28 [non-inverting] and ADCIN29 [inverting] 11h ADCIN28 [non-inverting] and ADCIN29 [inverting] 1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting] 1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]
14:12	RESOLUTION	R	0h	Placeholder for per-SOC resolution
11:10	SIGNALMODE	R	0h	Placeholder for per-SOC signal mode
9	RESERVED_1	R	0h	Reserved
8:0	ACQPS	R/W	0h	SOC15 Acquisition Prescale. Controls the sample and hold window for this SOC. 000h Reserved 001h Reserved 002h Sample window is 3 system clock cycles wide 003h Sample window is 4 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.

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3.14.2.33 ADC_R_CFG_ADCEVTSTAT Register

3.14.2.33.1 ADC_R_CFG_ADCEVTSTAT Register (Offset = 60h) [reset = 0h]

ADC Event Status Register.

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Table 3-1258. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5060h
ADC_R1	502C 7060h

Figure 3-676. ADC_R_CFG_ADCEVTSTAT Name Register

15	14	13	12	11	10	9	8
RESERVED_4	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED_3	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_2	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED_1	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1259. ADC_R_CFG_ADCEVTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_4	R	0h	Reserved
14	PPB4ZERO	R	0h	Post Processing Block 4 Zero Crossing Flag. When set indicates the ADCPPB4RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
13	PPB4TRIPLO	R	0h	Post Processing Block 4 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
12	PPB4TRIPHI	R	0h	Post Processing Block 4 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
11	RESERVED_3	R	0h	Reserved
10	PPB3ZERO	R	0h	Post Processing Block 3 Zero Crossing Flag. When set indicates the ADCPPB3RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority

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Table 3-1259. ADC_R_CFG_ADCEVTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	PPB3TRIPLO	R	0h	Post Processing Block 3 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
8	PPB3TRIPHI	R	0h	Post Processing Block 3 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
7	RESERVED_2	R	0h	Reserved
6	PPB2ZERO	R	0h	Post Processing Block 2 Zero Crossing Flag. When set indicates the ADCPPB2RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
5	PPB2TRIPLO	R	0h	Post Processing Block 2 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
4	PPB2TRIPHI	R	0h	Post Processing Block 2 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
3	RESERVED_1	R	0h	Reserved
2	PPB1ZERO	R	0h	Post Processing Block 1 Zero Crossing Flag. When set indicates the ADCPPB1RESULT register has changed sign. This bit is gated by EOC signal. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
1	PPB1TRIPLO	R	0h	Post Processing Block 1 Trip Low Flag. When set indicates a digital compare trip low event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority

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Table 3-1259. ADC_R_CFG_ADCEVTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PPB1TRIPHI	R	0h	Post Processing Block 1 Trip High Flag. When set indicates a digital compare trip high event has occurred. Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority

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3.14.2.34 ADC_R_CFG_ADCEVTCLR Register

3.14.2.34.1 ADC_R_CFG_ADCEVTCLR Register (Offset = 64h) [reset = 0h]

ADC Event Clear Register.

Return to Summary Table

Table 3-1260. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5064h
ADC_R1	502C 7064h

Figure 3-677. ADC_R_CFG_ADCEVTCLR Name Register

15	14	13	12	11	10	9	8
RESERVED_4	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED_3	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R	R/W1TS	R/W1TS	R/W1TS	R	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED_1	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R	R/W1TS	R/W1TS	R/W1TS	R	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1261. ADC_R_CFG_ADCEVTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_4	R	0h	Reserved
14	PPB4ZERO	R/W1TS	0h	Post Processing Block 4 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
13	PPB4TRIPLO	R/W1TS	0h	Post Processing Block 4 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
12	PPB4TRIPHI	R/W1TS	0h	Post Processing Block 4 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
11	RESERVED_3	R	0h	Reserved
10	PPB3ZERO	R/W1TS	0h	Post Processing Block 3 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
9	PPB3TRIPLO	R/W1TS	0h	Post Processing Block 3 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
8	PPB3TRIPHI	R/W1TS	0h	Post Processing Block 3 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
7	RESERVED_2	R	0h	Reserved
6	PPB2ZERO	R/W1TS	0h	Post Processing Block 2 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority

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Table 3-1261. ADC_R_CFG_ADCEVTCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PPB2TRIPLO	R/W1TS	0h	Post Processing Block 2 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
4	PPB2TRIPHI	R/W1TS	0h	Post Processing Block 2 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
3	RESERVED_1	R	0h	Reserved
2	PPB1ZERO	R/W1TS	0h	Post Processing Block 1 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
1	PPB1TRIPLO	R/W1TS	0h	Post Processing Block 1 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority
0	PPB1TRIPHI	R/W1TS	0h	Post Processing Block 1 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority

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3.14.2.35 ADC_R_CFG_ADCEVTSEL Register

3.14.2.35.1 ADC_R_CFG_ADCEVTSEL Register (Offset = 68h) [reset = 0h]

ADC Event Selection Register.

Return to Summary Table

Table 3-1262. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5068h
ADC_R1	502C 7068h

Figure 3-678. ADC_R_CFG_ADCEVTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_4	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED_3	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED_1	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1263. ADC_R_CFG_ADCEVTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_4	R	0h	Reserved
14	PPB4ZERO	R/W	0h	Post Processing Block 4 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
11	RESERVED_3	R	0h	Reserved
10	PPB3ZERO	R/W	0h	Post Processing Block 3 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
7	RESERVED_2	R	0h	Reserved
6	PPB2ZERO	R/W	0h	Post Processing Block 2 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.

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Table 3-1263. ADC_R_CFG_ADCEVTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
3	RESERVED_1	R	0h	Reserved
2	PPB1ZERO	R/W	0h	Post Processing Block 1 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.

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3.14.2.36 ADC_R_CFG_ADCEVTINTSEL Register

3.14.2.36.1 ADC_R_CFG_ADCEVTINTSEL Register (Offset = 6Ch) [reset = 0h]

ADC Event Interrupt Selection Register.

Return to Summary Table

Table 3-1264. Instance Table

Instance Name	Physical Address
ADC_R0	502C 506Ch
ADC_R1	502C 706Ch

Figure 3-679. ADC_R_CFG_ADCEVTINTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED_4	PPB4ZERO	PPB4TRIPLO	PPB4TRIPHI	RESERVED_3	PPB3ZERO	PPB3TRIPLO	PPB3TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_2	PPB2ZERO	PPB2TRIPLO	PPB2TRIPHI	RESERVED_1	PPB1ZERO	PPB1TRIPLO	PPB1TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1265. ADC_R_CFG_ADCEVTINTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_4	R	0h	Reserved
14	PPB4ZERO	R/W	0h	Post Processing Block 4 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
11	RESERVED_3	R	0h	Reserved
10	PPB3ZERO	R/W	0h	Post Processing Block 3 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
7	RESERVED_2	R	0h	Reserved
6	PPB2ZERO	R/W	0h	Post Processing Block 2 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.

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Table 3-1265. ADC_R_CFG_ADCEVTINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
3	RESERVED_1	R	0h	Reserved
2	PPB1ZERO	R/W	0h	Post Processing Block 1 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.

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3.14.2.37 ADC_R_CFG_ADCCOUNTER Register

3.14.2.37.1 ADC_R_CFG_ADCCOUNTER Register (Offset = 72h) [reset = 0h]

ADC Counter Register.

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Table 3-1266. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5072h
ADC_R1	502C 7072h

Figure 3-680. ADC_R_CFG_ADCCOUNTER Name Register

15	14	13	12	11	10	9	8
RESERVED_1				FREECOUNT			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FREECOUNT							
R							
0h							

Table 3-1267. ADC_R_CFG_ADCCOUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	FREECOUNT	R	0h	ADC Free Running Counter Value. This bit field reflects the status of the free running ADC counter.

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3.14.2.38 ADC_R_CFG_ADCREV Register

3.14.2.38.1 ADC_R_CFG_ADCREV Register (Offset = 74h) [reset = 105h]

ADC Revision Register.

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Table 3-1268. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5074h
ADC_R1	502C 7074h

Figure 3-681. ADC_R_CFG_ADCREV Name Register

15	14	13	12	11	10	9	8
REV							
R							
1h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TYPE							
R							
5h							

Table 3-1269. ADC_R_CFG_ADCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	REV	R	1h	ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h
7:0	TYPE	R	5h	ADC Type. Always set to 5 for this ADC.

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3.14.2.39 ADC_R_CFG_ADCPPB1CONFIG Register

3.14.2.39.1 ADC_R_CFG_ADCPPB1CONFIG Register (Offset = 80h) [reset = 0h]

ADC PPB1 Config Register.

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Table 3-1270. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5080h
ADC_R1	502C 7080h

Figure 3-682. ADC_R_CFG_ADCPPB1CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1	ABSEN	CBCEN	TWOSCOMPEN	CONFIG			
R	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			

Table 3-1271. ADC_R_CFG_ADCPPB1CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6	ABSEN	R/W	0h	ADC Post Processing Block 1 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULx associated with ADCPPB1. This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT] 0 ADCPPB1RESULT = ADCRESULTx - ADCPPB1OFFREF 1 ADCPPB1RESULT = abs[ADCRESULTx - ADCPPB1OFFREF]
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 1 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB1RESULT register. 0 ADCPPB1RESULT = ADCRESULTx - ADCPPB1OFFREF 1 ADCPPB1RESULT = ADCPPB1OFFREF - ADCRESULTx

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Table 3-1271. ADC_R_CFG_ADCPPB1CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CONFIG	R/W	0h	ADC Post Processing Block 1 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 1 0001 SOC1/EOC1/RESULT1 is associated with post processing block 1 0010 SOC2/EOC2/RESULT2 is associated with post processing block 1 0011 SOC3/EOC3/RESULT3 is associated with post processing block 1 0100 SOC4/EOC4/RESULT4 is associated with post processing block 1 0101 SOC5/EOC5/RESULT5 is associated with post processing block 1 0110 SOC6/EOC6/RESULT6 is associated with post processing block 1 0111 SOC7/EOC7/RESULT7 is associated with post processing block 1 1000 SOC8/EOC8/RESULT8 is associated with post processing block 1 1001 SOC9/EOC9/RESULT9 is associated with post processing block 1 1010 SOC10/EOC10/RESULT10 is associated with post processing block 1 1011 SOC11/EOC11/RESULT11 is associated with post processing block 1 1100 SOC12/EOC12/RESULT12 is associated with post processing block 1 1101 SOC13/EOC13/RESULT13 is associated with post processing block 1 1110 SOC14/EOC14/RESULT14 is associated with post processing block 1 1111 SOC15/EOC15/RESULT15 is associated with post processing block 1

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3.14.2.40 ADC_R_CFG_ADCPPB1STAMP Register

3.14.2.40.1 ADC_R_CFG_ADCPPB1STAMP Register (Offset = 82h) [reset = 0h]

ADC PPB1 Sample Delay Time Stamp Register.

Return to Summary Table

Table 3-1272. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5082h
ADC_R1	502C 7082h

Figure 3-683. ADC_R_CFG_ADCPPB1STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DLYSTAMP			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLYSTAMP							
R							
0h							

Table 3-1273. ADC_R_CFG_ADCPPB1STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DLYSTAMP	R	0h	ADC Post Processing Block 1 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.14.2.41 ADC_R_CFG_ADCPPB1OFFCAL Register

3.14.2.41.1 ADC_R_CFG_ADCPPB1OFFCAL Register (Offset = 84h) [reset = 0h]

ADC PPB1 Offset Calibration Register.

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Table 3-1274. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5084h
ADC_R1	502C 7084h

Figure 3-684. ADC_R_CFG_ADCPPB1OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						OFFCAL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFCAL							
R/W							
0h							

Table 3-1275. ADC_R_CFG_ADCPPB1OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	OFFCAL	R/W	0h	ADC Post Processing Block 1 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000hand FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000hand 0FFFh before being stored into the ADCRESULT register. Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.

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3.14.2.42 ADC_R_CFG_ADCPPB1OFFREF Register

3.14.2.42.1 ADC_R_CFG_ADCPPB1OFFREF Register (Offset = 86h) [reset = 0h]

ADC PPB1 Offset Reference Register.

Return to Summary Table

Table 3-1276. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5086h
ADC_R1	502C 7086h

Figure 3-685. ADC_R_CFG_ADCPPB1OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFREF							
R/W							
0h							

Table 3-1277. ADC_R_CFG_ADCPPB1OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFREF	R/W	0h	ADC Post Processing Block 1 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB1RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.14.2.43 ADC_R_CFG_ADCPPB1TRIPHI Register

3.14.2.43.1 ADC_R_CFG_ADCPPB1TRIPHI Register (Offset = 88h) [reset = 0h]

ADC PPB1 Trip High Register.

Return to Summary Table

Table 3-1278. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5088h
ADC_R1	502C 7088h

Figure 3-686. ADC_R_CFG_ADCPPB1TRIPHI Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITHI							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITHI							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITHI							
R/W							
0h							

Table 3-1279. ADC_R_CFG_ADCPPB1TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITHI	R/W	0h	ADC Post Processing Block 1 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPHI[23:17] will be ignored in 16 bit mode - TRIPHI[23:13] will be ignored in 12 bit mode

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3.14.2.44 ADC_R_CFG_ADCPPB1TRIPLO Register

3.14.2.44.1 ADC_R_CFG_ADCPPB1TRIPLO Register (Offset = 8Ch) [reset = 0h]

ADC PPB1 Trip Low/Trigger Time Stamp Register.

Return to Summary Table

Table 3-1280. Instance Table

Instance Name	Physical Address
ADC_R0	502C 508Ch
ADC_R1	502C 708Ch

Figure 3-687. ADC_R_CFG_ADCPPB1TRIPLO Name Register

31	30	29	28	27	26	25	24
REQSTAMP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REQSTAMP				LIMITLO2EN	RESERVED_1		LSIGN
R				R/W	R		R/W
0h				0h	0h		0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LIMITLO							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMITLO							
R/W							
0h							

Table 3-1281. ADC_R_CFG_ADCPPB1TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	REQSTAMP	R	0h	ADC Post Processing Block 1 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19	LIMITLO2EN	R/W	0h	Extended Low Limit 2 Enable. 0 = Low limit set by ADCPPB1TRIPLO register. Not compatible with comparison with ADCPPB1PSUM or ADCPPB1SUM 1 = Low limit set by ADCPPB1TRIPLO2 register
18:17	RESERVED_1	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.
15:0	LIMITLO	R/W	0h	ADC Post Processing Block 1 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB1RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB1RESULT register.

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3.14.2.45 ADC_R_CFG_ADCPPB2CONFIG Register

3.14.2.45.1 ADC_R_CFG_ADCPPB2CONFIG Register (Offset = 90h) [reset = 1h]

ADC PPB2 Config Register.

Return to Summary Table

Table 3-1282. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5090h
ADC_R1	502C 7090h

Figure 3-688. ADC_R_CFG_ADCPPB2CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1	ABSEN	CBCEN	TWOSCOMPEN	CONFIG			
R	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	1h			

Table 3-1283. ADC_R_CFG_ADCPPB2CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6	ABSEN	R/W	0h	ADC Post Processing Block 2 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULx associated with ADCPPB2. This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT] 0 ADCPPB2RESULT = ADCRESULTx - ADCPPB2OFFREF 1 ADCPPB2RESULT = abs[ADCRESULTx - ADCPPB2OFFREF]
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 2 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB2RESULT register. 0 ADCPPB2RESULT = ADCRESULTx - ADCPPB2OFFREF 1 ADCPPB2RESULT = ADCPPB2OFFREF - ADCRESULTx

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Table 3-1283. ADC_R_CFG_ADCPPB2CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CONFIG	R/W	1h	ADC Post Processing Block 2 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 2 0001 SOC1/EOC1/RESULT1 is associated with post processing block 2 0010 SOC2/EOC2/RESULT2 is associated with post processing block 2 0011 SOC3/EOC3/RESULT3 is associated with post processing block 2 0100 SOC4/EOC4/RESULT4 is associated with post processing block 2 0101 SOC5/EOC5/RESULT5 is associated with post processing block 2 0110 SOC6/EOC6/RESULT6 is associated with post processing block 2 0111 SOC7/EOC7/RESULT7 is associated with post processing block 2 1000 SOC8/EOC8/RESULT8 is associated with post processing block 2 1001 SOC9/EOC9/RESULT9 is associated with post processing block 2 1010 SOC10/EOC10/RESULT10 is associated with post processing block 2 1011 SOC11/EOC11/RESULT11 is associated with post processing block 2 1100 SOC12/EOC12/RESULT12 is associated with post processing block 2 1101 SOC13/EOC13/RESULT13 is associated with post processing block 2 1110 SOC14/EOC14/RESULT14 is associated with post processing block 2 1111 SOC15/EOC15/RESULT15 is associated with post processing block 2

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3.14.2.46 ADC_R_CFG_ADCPPB2STAMP Register

3.14.2.46.1 ADC_R_CFG_ADCPPB2STAMP Register (Offset = 92h) [reset = 0h]

ADC PPB2 Sample Delay Time Stamp Register.

Return to Summary Table

Table 3-1284. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5092h
ADC_R1	502C 7092h

Figure 3-689. ADC_R_CFG_ADCPPB2STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DLYSTAMP			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLYSTAMP							
R							
0h							

Table 3-1285. ADC_R_CFG_ADCPPB2STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DLYSTAMP	R	0h	ADC Post Processing Block 2 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.14.2.47 ADC_R_CFG_ADCPPB2OFFCAL Register

3.14.2.47.1 ADC_R_CFG_ADCPPB2OFFCAL Register (Offset = 94h) [reset = 0h]

ADC PPB2 Offset Calibration Register.

Return to Summary Table

Table 3-1286. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5094h
ADC_R1	502C 7094h

Figure 3-690. ADC_R_CFG_ADCPPB2OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						OFFCAL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFCAL							
R/W							
0h							

Table 3-1287. ADC_R_CFG_ADCPPB2OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	OFFCAL	R/W	0h	ADC Post Processing Block 2 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000hand FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000hand 0FFFh before being stored into the ADCRESULT register. Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.

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3.14.2.48 ADC_R_CFG_ADCPPB2OFFREF Register

3.14.2.48.1 ADC_R_CFG_ADCPPB2OFFREF Register (Offset = 96h) [reset = 0h]

ADC PPB2 Offset Reference Register.

Return to Summary Table

Table 3-1288. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5096h
ADC_R1	502C 7096h

Figure 3-691. ADC_R_CFG_ADCPPB2OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0h							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0h							

Table 3-1289. ADC_R_CFG_ADCPPB2OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFREF	R/W	0h	ADC Post Processing Block 2 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB2RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.14.2.49 ADC_R_CFG_ADCPPB2TRIPHI Register

3.14.2.49.1 ADC_R_CFG_ADCPPB2TRIPHI Register (Offset = 98h) [reset = 0h]

ADC PPB2 Trip High Register.

Return to Summary Table

Table 3-1290. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5098h
ADC_R1	502C 7098h

Figure 3-692. ADC_R_CFG_ADCPPB2TRIPHI Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LIMITHI							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LIMITHI							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMITHI							
R/W							
0h							

Table 3-1291. ADC_R_CFG_ADCPPB2TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITHI	R/W	0h	ADC Post Processing Block 2 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPHI[23:17] will be ignored in 16 bit mode - TRIPHI[23:13] will be ignored in 12 bit mode

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3.14.2.50 ADC_R_CFG_ADCPPB2TRIPLO Register

3.14.2.50.1 ADC_R_CFG_ADCPPB2TRIPLO Register (Offset = 9Ch) [reset = 0h]

ADC PPB2 Trip Low/Trigger Time Stamp Register.

Return to Summary Table

Table 3-1292. Instance Table

Instance Name	Physical Address
ADC_R0	502C 509Ch
ADC_R1	502C 709Ch

Figure 3-693. ADC_R_CFG_ADCPPB2TRIPLO Name Register

31	30	29	28	27	26	25	24
REQSTAMP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REQSTAMP				LIMITLO2EN	RESERVED_1		LSIGN
R				R/W	R		R/W
0h				0h	0h		0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LIMITLO							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMITLO							
R/W							
0h							

Table 3-1293. ADC_R_CFG_ADCPPB2TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	REQSTAMP	R	0h	ADC Post Processing Block 2 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19	LIMITLO2EN	R/W	0h	Extended Low Limit 2 Enable. 0 = Low limit set by ADCPPB2TRIPLO register. Not compatible with comparison with ADCPPB2PSUM or ADCPPB2SUM 1 = Low limit set by ADCPPB2TRIPLO2 register
18:17	RESERVED_1	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.
15:0	LIMITLO	R/W	0h	ADC Post Processing Block 2 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB2RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB2RESULT register.

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3.14.2.51 ADC_R_CFG_ADCPPB3CONFIG Register

3.14.2.51.1 ADC_R_CFG_ADCPPB3CONFIG Register (Offset = A0h) [reset = 2h]

ADC PPB3 Config Register.

Return to Summary Table

Table 3-1294. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50A0h
ADC_R1	502C 70A0h

Figure 3-694. ADC_R_CFG_ADCPPB3CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1	ABSEN	CBCEN	TWOSCOMPEN	CONFIG			
R	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	2h			

Table 3-1295. ADC_R_CFG_ADCPPB3CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6	ABSEN	R/W	0h	ADC Post Processing Block 3 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULx associated with ADCPPB3. This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT] 0 ADCPPB3RESULT = ADCRESULTx - ADCPPB3OFFREF 1 ADCPPB3RESULT = abs[ADCRESULTx - ADCPPB3OFFREF]
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 3 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB3RESULT register. 0 ADCPPB3RESULT = ADCRESULTx - ADCPPB3OFFREF 1 ADCPPB3RESULT = ADCPPB3OFFREF - ADCRESULTx

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Table 3-1295. ADC_R_CFG_ADCPPB3CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CONFIG	R/W	2h	ADC Post Processing Block 3 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 3 0001 SOC1/EOC1/RESULT1 is associated with post processing block 3 0010 SOC2/EOC2/RESULT2 is associated with post processing block 3 0011 SOC3/EOC3/RESULT3 is associated with post processing block 3 0100 SOC4/EOC4/RESULT4 is associated with post processing block 3 0101 SOC5/EOC5/RESULT5 is associated with post processing block 3 0110 SOC6/EOC6/RESULT6 is associated with post processing block 3 0111 SOC7/EOC7/RESULT7 is associated with post processing block 3 1000 SOC8/EOC8/RESULT8 is associated with post processing block 3 1001 SOC9/EOC9/RESULT9 is associated with post processing block 3 1010 SOC10/EOC10/RESULT10 is associated with post processing block 3 1011 SOC11/EOC11/RESULT11 is associated with post processing block 3 1100 SOC12/EOC12/RESULT12 is associated with post processing block 3 1101 SOC13/EOC13/RESULT13 is associated with post processing block 3 1110 SOC14/EOC14/RESULT14 is associated with post processing block 3 1111 SOC15/EOC15/RESULT15 is associated with post processing block 3

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3.14.2.52 ADC_R_CFG_ADCPPB3STAMP Register

3.14.2.52.1 ADC_R_CFG_ADCPPB3STAMP Register (Offset = A2h) [reset = 0h]

ADC PPB3 Sample Delay Time Stamp Register.

Return to Summary Table

Table 3-1296. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50A2h
ADC_R1	502C 70A2h

Figure 3-695. ADC_R_CFG_ADCPPB3STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DLYSTAMP			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLYSTAMP							
R							
0h							

Table 3-1297. ADC_R_CFG_ADCPPB3STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DLYSTAMP	R	0h	ADC Post Processing Block 3 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.14.2.53 ADC_R_CFG_ADCPPB3OFFCAL Register

3.14.2.53.1 ADC_R_CFG_ADCPPB3OFFCAL Register (Offset = A4h) [reset = 0h]

ADC PPB3 Offset Calibration Register.

Return to Summary Table

Table 3-1298. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50A4h
ADC_R1	502C 70A4h

Figure 3-696. ADC_R_CFG_ADCPPB3OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						OFFCAL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFCAL							
R/W							
0h							

Table 3-1299. ADC_R_CFG_ADCPPB3OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	OFFCAL	R/W	0h	ADC Post Processing Block 3 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000hand FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000hand 0FFFh before being stored into the ADCRESULT register. Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.

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3.14.2.54 ADC_R_CFG_ADCPPB3OFFREF Register

3.14.2.54.1 ADC_R_CFG_ADCPPB3OFFREF Register (Offset = A6h) [reset = 0h]

ADC PPB3 Offset Reference Register.

Return to Summary Table

Table 3-1300. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50A6h
ADC_R1	502C 70A6h

Figure 3-697. ADC_R_CFG_ADCPPB3OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0h							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0h							

Table 3-1301. ADC_R_CFG_ADCPPB3OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFREF	R/W	0h	ADC Post Processing Block 3 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB3RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.14.2.55 ADC_R_CFG_ADCPPB3TRIPHI Register

3.14.2.55.1 ADC_R_CFG_ADCPPB3TRIPHI Register (Offset = A8h) [reset = 0h]

ADC PPB3 Trip High Register.

Return to Summary Table

Table 3-1302. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50A8h
ADC_R1	502C 70A8h

Figure 3-698. ADC_R_CFG_ADCPPB3TRIPHI Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITHI							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITHI							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITHI							
R/W							
0h							

Table 3-1303. ADC_R_CFG_ADCPPB3TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITHI	R/W	0h	ADC Post Processing Block 3 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPHI[23:17] will be ignored in 16 bit mode - TRIPHI[23:13] will be ignored in 12 bit mode

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3.14.2.56 ADC_R_CFG_ADCPPB3TRIPLO Register

3.14.2.56.1 ADC_R_CFG_ADCPPB3TRIPLO Register (Offset = ACh) [reset = 0h]

ADC PPB3 Trip Low/Trigger Time Stamp Register.

Return to Summary Table

Table 3-1304. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50ACh
ADC_R1	502C 70ACh

Figure 3-699. ADC_R_CFG_ADCPPB3TRIPLO Name Register

31	30	29	28	27	26	25	24
REQSTAMP							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REQSTAMP				LIMITLO2EN	RESERVED_1		LSIGN
R				R/W	R		R/W
0h				0h	0h		0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LIMITLO							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMITLO							
R/W							
0h							

Table 3-1305. ADC_R_CFG_ADCPPB3TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	REQSTAMP	R	0h	ADC Post Processing Block 3 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19	LIMITLO2EN	R/W	0h	Extended Low Limit 2 Enable. 0 = Low limit set by ADCPPB3TRIPLO register. Not compatible with comparison with ADCPPB3PSUM or ADCPPB3SUM 1 = Low limit set by ADCPPB3TRIPLO2 register
18:17	RESERVED_1	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.
15:0	LIMITLO	R/W	0h	ADC Post Processing Block 3 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB3RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB3RESULT register.

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3.14.2.57 ADC_R_CFG_ADCPPB4CONFIG Register

3.14.2.57.1 ADC_R_CFG_ADCPPB4CONFIG Register (Offset = B0h) [reset = 3h]

ADC PPB4 Config Register.

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Table 3-1306. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50B0h
ADC_R1	502C 70B0h

Figure 3-700. ADC_R_CFG_ADCPPB4CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_1	ABSEN	CBCEN	TWOSCOMPEN	CONFIG			
R	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	3h			

Table 3-1307. ADC_R_CFG_ADCPPB4CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED_1	R	0h	Reserved
6	ABSEN	R/W	0h	ADC Post Processing Block 4 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULx associated with ADCPPB4. This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT] 0 ADCPPB4RESULT = ADCRESULTx - ADCPPB4OFFREF 1 ADCPPB4RESULT = abs[ADCRESULTx - ADCPPB4OFFREF]
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 4 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB4RESULT register. 0 ADCPPB4RESULT = ADCRESULTx - ADCPPB4OFFREF 1 ADCPPB4RESULT = ADCPPB4OFFREF - ADCRESULTx

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Table 3-1307. ADC_R_CFG_ADCPPB4CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	CONFIG	R/W	3h	ADC Post Processing Block 4 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 4 0001 SOC1/EOC1/RESULT1 is associated with post processing block 4 0010 SOC2/EOC2/RESULT2 is associated with post processing block 4 0011 SOC3/EOC3/RESULT3 is associated with post processing block 4 0100 SOC4/EOC4/RESULT4 is associated with post processing block 4 0101 SOC5/EOC5/RESULT5 is associated with post processing block 4 0110 SOC6/EOC6/RESULT6 is associated with post processing block 4 0111 SOC7/EOC7/RESULT7 is associated with post processing block 4 1000 SOC8/EOC8/RESULT8 is associated with post processing block 4 1001 SOC9/EOC9/RESULT9 is associated with post processing block 4 1010 SOC10/EOC10/RESULT10 is associated with post processing block 4 1011 SOC11/EOC11/RESULT11 is associated with post processing block 4 1100 SOC12/EOC12/RESULT12 is associated with post processing block 4 1101 SOC13/EOC13/RESULT13 is associated with post processing block 4 1110 SOC14/EOC14/RESULT14 is associated with post processing block 4 1111 SOC15/EOC15/RESULT15 is associated with post processing block 4

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3.14.2.58 ADC_R_CFG_ADCPPB4STAMP Register

3.14.2.58.1 ADC_R_CFG_ADCPPB4STAMP Register (Offset = B2h) [reset = 0h]

ADC PPB4 Sample Delay Time Stamp Register.

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Table 3-1308. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50B2h
ADC_R1	502C 70B2h

Figure 3-701. ADC_R_CFG_ADCPPB4STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED_1				DLYSTAMP			
R				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLYSTAMP							
R							
0h							

Table 3-1309. ADC_R_CFG_ADCPPB4STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED_1	R	0h	Reserved
11:0	DLYSTAMP	R	0h	ADC Post Processing Block 4 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.14.2.59 ADC_R_CFG_ADCPPB4OFFCAL Register

3.14.2.59.1 ADC_R_CFG_ADCPPB4OFFCAL Register (Offset = B4h) [reset = 0h]

ADC PPB4 Offset Calibration Register.

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Table 3-1310. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50B4h
ADC_R1	502C 70B4h

Figure 3-702. ADC_R_CFG_ADCPPB4OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						OFFCAL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFCAL							
R/W							
0h							

Table 3-1311. ADC_R_CFG_ADCPPB4OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	OFFCAL	R/W	0h	ADC Post Processing Block 4 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000hand FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000hand 0FFFh before being stored into the ADCRESULT register. Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.

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3.14.2.60 ADC_R_CFG_ADCPPB4OFFREF Register

3.14.2.60.1 ADC_R_CFG_ADCPPB4OFFREF Register (Offset = B6h) [reset = 0h]

ADC PPB4 Offset Reference Register.

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Table 3-1312. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50B6h
ADC_R1	502C 70B6h

Figure 3-703. ADC_R_CFG_ADCPPB4OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OFFREF							
R/W							
0h							

Table 3-1313. ADC_R_CFG_ADCPPB4OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFFREF	R/W	0h	ADC Post Processing Block 4 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB4RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.14.2.61 ADC_R_CFG_ADCPPB4TRIPHI Register

3.14.2.61.1 ADC_R_CFG_ADCPPB4TRIPHI Register (Offset = B8h) [reset = 0h]

ADC PPB4 Trip High Register.

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Table 3-1314. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50B8h
ADC_R1	502C 70B8h

Figure 3-704. ADC_R_CFG_ADCPPB4TRIPHI Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITHI							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITHI							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITHI							
R/W							
0h							

Table 3-1315. ADC_R_CFG_ADCPPB4TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITHI	R/W	0h	ADC Post Processing Block 4 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPHI[23:17] will be ignored in 16 bit mode - TRIPHI[23:13] will be ignored in 12 bit mode

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3.14.2.62 ADC_R_CFG_ADCPPB4TRIPLO Register

3.14.2.62.1 ADC_R_CFG_ADCPPB4TRIPLO Register (Offset = BCh) [reset = 0h]

ADC PPB4 Trip Low/Trigger Time Stamp Register.

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Table 3-1316. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50BCh
ADC_R1	502C 70BCh

Figure 3-705. ADC_R_CFG_ADCPPB4TRIPLO Name Register

31	30	29	28	27	26	25	24
REQSTAMP							
R							
0h							
23	22	21	20	19	18	17	16
REQSTAMP				LIMITLO2EN	RESERVED_1		LSIGN
R				R/W	R		R/W
0h				0h	0h		0h
15	14	13	12	11	10	9	8
LIMITLO							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITLO							
R/W							
0h							

Table 3-1317. ADC_R_CFG_ADCPPB4TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	REQSTAMP	R	0h	ADC Post Processing Block 4 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19	LIMITLO2EN	R/W	0h	Extended Low Limit 2 Enable. 0 = Low limit set by ADCPPB4TRIPLO register. Not compatible with comparison with ADCPPB4PSUM or ADCPPB4SUM 1 = Low limit set by ADCPPB4TRIPLO2 register
18:17	RESERVED_1	R	0h	Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.
15:0	LIMITLO	R/W	0h	ADC Post Processing Block 4 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB4RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB4RESULT register.

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3.14.2.63 ADC_R_CFG_ADCSAFECHECKRESEN Register

3.14.2.63.1 ADC_R_CFG_ADCSAFECHECKRESEN Register (Offset = C0h) [reset = 0h]

ADC Safe Check Result Enable Register.

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Table 3-1318. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50C0h
ADC_R1	502C 70C0h

Figure 3-706. ADC_R_CFG_ADCSAFECHECKRESEN Name Register

31	30	29	28	27	26	25	24
SOC15CHKEN		SOC14CHKEN		SOC13CHKEN		SOC12CHKEN	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
23	22	21	20	19	18	17	16
SOC11CHKEN		SOC10CHKEN		SOC9CHKEN		SOC8CHKEN	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
15	14	13	12	11	10	9	8
SOC7CHKEN		SOC6CHKEN		SOC5CHKEN		SOC4CHKEN	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	
7	6	5	4	3	2	1	0
SOC3CHKEN		SOC2CHKEN		SOC1CHKEN		SOC0CHKEN	
R/W		R/W		R/W		R/W	
0h		0h		0h		0h	

Table 3-1319. ADC_R_CFG_ADCSAFECHECKRESEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SOC15CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT15 passed to safety checker 10 PPB Result associated with SOC15 passed to safety checker 11 PPB Sum associated with SOC15 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
29:28	SOC14CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT14 passed to safety checker 10 PPB Result associated with SOC14 passed to safety checker 11 PPB Sum associated with SOC14 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker

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Table 3-1319. ADC_R_CFG_ADCSAFECHECKRESEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:26	SOC13CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT13 passed to safety checker 10 PPB Result associated with SOC13 passed to safety checker 11 PPB Sum associated with SOC13 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
25:24	SOC12CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT12 passed to safety checker 10 PPB Result associated with SOC12 passed to safety checker 11 PPB Sum associated with SOC12 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
23:22	SOC11CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT11 passed to safety checker 10 PPB Result associated with SOC11 passed to safety checker 11 PPB Sum associated with SOC11 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
21:20	SOC10CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT10 passed to safety checker 10 PPB Result associated with SOC10 passed to safety checker 11 PPB Sum associated with SOC10 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
19:18	SOC9CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT9 passed to safety checker 10 PPB Result associated with SOC9 passed to safety checker 11 PPB Sum associated with SOC9 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
17:16	SOC8CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT8 passed to safety checker 10 PPB Result associated with SOC8 passed to safety checker 11 PPB Sum associated with SOC8 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker

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Table 3-1319. ADC_R_CFG_ADCSAFECHECKRESEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SOC7CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT7 passed to safety checker 10 PPB Result associated with SOC7 passed to safety checker 11 PPB Sum associated with SOC7 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
13:12	SOC6CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT6 passed to safety checker 10 PPB Result associated with SOC6 passed to safety checker 11 PPB Sum associated with SOC6 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
11:10	SOC5CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT5 passed to safety checker 10 PPB Result associated with SOC5 passed to safety checker 11 PPB Sum associated with SOC5 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
9:8	SOC4CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT4 passed to safety checker 10 PPB Result associated with SOC4 passed to safety checker 11 PPB Sum associated with SOC4 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
7:6	SOC3CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT3 passed to safety checker 10 PPB Result associated with SOC3 passed to safety checker 11 PPB Sum associated with SOC3 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
5:4	SOC2CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT2 passed to safety checker 10 PPB Result associated with SOC2 passed to safety checker 11 PPB Sum associated with SOC2 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker

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Table 3-1319. ADC_R_CFG_ADCSAFECHECKRESEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	SOC1CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT1 passed to safety checker 10 PPB Result associated with SOC1 passed to safety checker 11 PPB Sum associated with SOC1 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker
1:0	SOC0CHKEN	R/W	0h	Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion. 00 No result passed to safety checker 01 ADCRESULT0 passed to safety checker 10 PPB Result associated with SOC0 passed to safety checker 11 PPB Sum associated with SOC0 passed to safety chekcer Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker

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3.14.2.64 ADC_R_CFG_ADCINTCYCLE Register

3.14.2.64.1 ADC_R_CFG_ADCINTCYCLE Register (Offset = DEh) [reset = 0h]

ADC Early Interrupt Generation Cycle.

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Table 3-1320. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50DEh
ADC_R1	502C 70DEh

Figure 3-707. ADC_R_CFG_ADCINTCYCLE Name Register

15	14	13	12	11	10	9	8
DELAY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DELAY							
R/W							
0h							

Table 3-1321. ADC_R_CFG_ADCINTCYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DELAY	R/W	0h	ADC Early Interrupt Generation Cycle Delay: Defines the delay from the fall edge of ADCSOC in terms of system clock cycles, for the interrupt to be generated.

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3.14.2.65 ADC_R_CFG_ADCREV2 Register

3.14.2.65.1 ADC_R_CFG_ADCREV2 Register (Offset = FAh) [reset = 4h]

ADC Wrapper Revision Register.

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Table 3-1322. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50FAh
ADC_R1	502C 70FAh

Figure 3-708. ADC_R_CFG_ADCREV2 Name Register

15	14	13	12	11	10	9	8
WRAPPERREV							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WRAPPERTYPE							
R							
4h							

Table 3-1323. ADC_R_CFG_ADCREV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	WRAPPERREV	R	0h	ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h
7:0	WRAPPERTYPE	R	4h	ADC Wrapper Type. Always set to 4 for this ADC.

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3.14.2.66 ADC_R_CFG_ADCINLTRIMCTL Register

3.14.2.66.1 ADC_R_CFG_ADCINLTRIMCTL Register (Offset = FCh) [reset = 0h]

ADC Linearity Trim Control Register.

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Table 3-1324. Instance Table

Instance Name	Physical Address
ADC_R0	502C 50FCh
ADC_R1	502C 70FCh

Figure 3-709. ADC_R_CFG_ADCINLTRIMCTL Name Register

31	30	29	28	27	26	25	24
KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1		CALIBSTEP					CALIBMODE
R		R/W					R/W
0h		0h					0h

Table 3-1325. ADC_R_CFG_ADCINLTRIMCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	KEY	R/W	0h	ADC Linearity Trim Control Write Key. Any write to this register must contain the value 0xA5A5 in these bit locations. If a write request attempts to load any other value into these bits, the write for the entire register is ignored. These bits always read back a zero.
15:6	RESERVED_1	R	0h	Reserved
5:1	CALIBSTEP	R/W	0h	ADC Linearity Calibration Step. Defines which of the 24 steps of calibration is to be executed. Never set this bit field while the ADC SELFTRIM is in progress. The R-M-W operation could unintentionally set the CALIBMODE bit again.
0	CALIBMODE	R/W	0h	ADC Linearity Calibration Mode.

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3.14.2.67 ADC_R_CFG_REP1CTL Register

3.14.2.67.1 ADC_R_CFG_REP1CTL Register (Offset = 100h) [reset = 0h]

ADC Trigger Repeater 1 Control Register.

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Table 3-1326. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5100h
ADC_R1	502C 7100h

Figure 3-710. ADC_R_CFG_REP1CTL Name Register

31	30	29	28	27	26	25	24
RESERVED_5							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SWSYNC	RESERVED_4	SYNCINSEL					
R/W1TS	R	R/W					
0h	0h	0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_3	TRIGGER						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIGGEROVF	PHASEOVF	RESERVED_2	SOCBUSY	MODULEBUSY	RESERVED_1	ACTIVEMODE	MODE
R/W1TC	R/W1TC	R	R	R	R	R	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1327. ADC_R_CFG_REP1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_5	R	0h	Reserved
23	SWSYNC	R/W1TS	0h	Trigger repeater 1 software force sync. On a sync. event, all registers in repeater 1 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved. Note: SOCs associated with repeater 1 are not cleared.
22	RESERVED_4	R	0h	Reserved
21:16	SYNCINSEL	R/W	0h	Trigger repeater 1 sync. input select. On a sync. event, all registers in repeater 1 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved. Note: SOCs associated with repeater 1 are not cleared.
15	RESERVED_3	R	0h	Reserved

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Table 3-1327. ADC_R_CFG_REP1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:8	TRIGGER	R/W	0h	ADC Trigger Repeater 1 Trigger Select. Selects the trigger to modify via oversampling or undersampling. 00h REPTRIG0 - Software only 01h REPTRIG1 - RTI0 Timer 02h REPTRIG2 - RTI1 Timer 03h REPTRIG3 - RTI2 Timer 04h REPTRIG4 - RTI3 Timer 05h REPTRIG5 - InputXBAR.Out[5] 06h REPTRIG6 - spare 07h REPTRIG7 - spare 08h REPTRIG8 - EPWM0, ADCSOCA 09h REPTRIG9 - EPWM0, ADCSOCB 0Ah REPTRIG10 - EPWM1, ADCSOCA 0Bh REPTRIG11 - EPWM1, ADCSOCB 0Ch REPTRIG12 - EPWM2, ADCSOCA 0Dh REPTRIG13 - EPWM2, ADCSOCB 0Eh REPTRIG14 - EPWM3, ADCSOCA 0Fh REPTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h REPTRIG64 - EPWM28, ADCSOCA 41h REPTRIG65 - EPWM28, ADCSOCB 42h REPTRIG66 - EPWM29, ADCSOCA 43h REPTRIG67 - EPWM29, ADCSOCB 44h REPTRIG68 - EPWM30, ADCSOCA 45h REPTRIG69 - EPWM30, ADCSOCB 46h REPTRIG70 - EPWM31, ADCSOCA 47h REPTRIG71 - EPWM31, ADCSOCB 48h REPTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h REPTRIG81 - ECAP9, TRIGOUT 52h REPTRIG82 - ECAP10, TRIGOUT .... 57h REPTRIG73 - ECAP15, TRIGOUT 58h REPTRIG1 - RTI4 Timer 59h REPTRIG1 - RTI5 Timer 5Ah REPTRIG1 - RTI6 Timer 5Bh REPTRIG1 - RTI7 Timer .... 7Fh - Reserved
7	TRIGGEROVF	R/W1TC	0h	ADC Trigger Repeater 1 Oversampled Trigger Overflow. Indicates that a trigger was dropped because a trigger arrived while the repeater was still generating repeated oversampled triggers [NCOUNT was not 0 or SOCs associated with Repeater 1 were still pending]. Writing a 1 will clear this flag. Note: This flag won't be set in undersampling mode or when NSEL = 0; if a trigger arrives before the previous SOCs have completed, the trigger will be passed and the overflow flags of the SOCs that were still pending will be set. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
6	PHASEOVF	R/W1TC	0h	ADC Trigger Repeater 1 Phase Delay Overflow. Indicates that a trigger was dropped because a trigger arrived when the phase delay logic was still waiting to send the delayed trigger [PHASECOUNT was not 0]. Writing a 1 will clear this flag. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
5	RESERVED_2	R	0h	Reserved

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Table 3-1327. ADC_R_CFG_REP1CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SOCBUSY	R	0h	ADC Trigger Repeater 1 Associated SOCs Busy indicator. In oversampling mode: 0 = no SOCs associated with this repeater are pending 1 = SOCs associated with this repeater are still pending The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP1CTL.BUSY = 0 [SOCs associated with trigger repeater 1 are no longer pending]. Note: If the ADC is in burstmode and the BURSTTRIG is Repeater 1, then all round-robin SOCs are considered associated with this repeater and the repeater will not re-trigger until there are no pending round-robin SOCs [in addition to any associated pending high-priority SOCs].
3	MODULEBUSY	R	0h	ADC Trigger Repeater 1 Module Busy indicator. In oversampling mode: 0 = Repeater 1 is idle and can accept a new repeated trigger in oversampling mode 1 = Repeater 1 still has repeated triggers remaining [NCOUNT ' 0] or associated SOCs are still pending [SOCBUSY is 1] If a new oversampled trigger is received while the module is still busy, the TRIGGEROVF bit will be set and the trigger will be ignored.
2	RESERVED_1	R	0h	Reserved
1	ACTIVEMODE	R	0h	When a trigger is recived in oversampling or undersampling mode the value of MODE is copied to ACTIVEMODE. ACTIVEMODE determines if the repeater will repeat of filter triggers. Changes to MODE while the repeater is working therefore won't cause any changes in functionality until the module becomes idle and then a new trigger is received. 0 = module is oversampling 1 = module is undersampling
0	MODE	R/W	0h	ADC trigger repeater 1 mode selection. Select either oversampling or undersampling mode. In oversampling mode, when the trigger selected by REP1CTL.TRIGSEL is received, the repeater will repeat the trigger REP1N.NSEL + 1 times. In undersampling mode, when the trigger selected by REP1CTL.TRIGSEL is received the first time, the repeater will pass the trigger through. The next REP1N.NSEL triggers will be ignored. 0 = oversampling 1 = undersampling

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3.14.2.68 ADC_R_CFG_REP1N Register

3.14.2.68.1 ADC_R_CFG_REP1N Register (Offset = 104h) [reset = 0h]

ADC Trigger Repeater 1 N Select Register.

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Table 3-1328. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5104h
ADC_R1	502C 7104h

Figure 3-711. ADC_R_CFG_REP1N Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2	NCOUNT						
R	R						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1	NSEL						
R	R/W						
0h	0h						

Table 3-1329. ADC_R_CFG_REP1N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED_2	R	0h	Reserved
22:16	NCOUNT	R	0h	ADC trigger repeater 1 trigger count. In oversampling mode, indicates the number of triggers remaining to be generated. If a trigger is received corresponding to REP1CTL.TRIGSEL while NCOUNT is not 0 [the repeater is still busy generating the repeated triggers] then the trigger will be ignored and REP1CTL.TRIGOVF will be set to 1. In undersampling mode, indicates the number of triggers remaining to be supressed.
15:7	RESERVED_1	R	0h	Reserved

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Table 3-1329. ADC_R_CFG_REP1N Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	NSEL	R/W	0h	ADC Trigger Repeater 1 selection of number of triggers. In oversampling mode, selects the number of repeated triggers. For each trigger received corresponding to REP1CTL.TRIGSEL, NSEL + 1 triggers will be generated. 0 = 1 trigger is generated [pass-through] 1 = 2 triggers are generated 2 = 3 triggers are generated ... 127 = 128 triggers are generated In undersampling mode, selects the number triggers to be supressed. 1 out NSEL + 1 triggers received corresponding to REP1CTL.TRIGSEL will be passed through [the first trigger will be passed through and the subsequent NSEL triggers will be supressed]. 0 = all triggers are passed 1 = 1 out of 2 triggers are passed 2 = 1 out of 3 triggers are passed ... 127 = 1 out of 128 triggers are passed

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3.14.2.69 ADC_R_CFG_REP1PHASE Register

3.14.2.69.1 ADC_R_CFG_REP1PHASE Register (Offset = 108h) [reset = 0h]

ADC Trigger Repeater 1 Phase Select Register.

Return to Summary Table

Table 3-1330. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5108h
ADC_R1	502C 7108h

Figure 3-712. ADC_R_CFG_REP1PHASE Name Register

31	30	29	28	27	26	25	24
PHASECOUNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHASECOUNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASE							
R/W							
0h							

Table 3-1331. ADC_R_CFG_REP1PHASE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHASECOUNT	R	0h	ADC trigger repeater 1 phase delay status. When the trigger selected by REP1CTL.TRIGSEL is received, this register will start counting down from PHASECOUNT until the counter reaches 0, at which point the trigger will be passed on to the repeater re-trigger logic. If the trigger selected by REP1CTL.TRIGSEL is recieved when PHASECOUNT is not 0 [the phase delay logic is busy from the previous trigger] then the new trigger will be ignored and REP1CTL.PHASEOVF will be set to 1.
15:0	PHASE	R/W	0h	ADC trigger repeater 1 phase delay configuration. Defines the number of SYSCLKs to delay the selected trigger before passing it on to the re-triggering logic. 0 = trigger is passed through without delay 1 = trigger is delayed by 1 SYSCLK 2 = trigger is delayed by 2 SYSCLKs ... 65535 = trigger is delayed by 65535 SYSCLKs

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3.14.2.70 ADC_R_CFG_REP1SPREAD Register

3.14.2.70.1 ADC_R_CFG_REP1SPREAD Register (Offset = 10Ch) [reset = 0h]

ADC Trigger Repeater 1 Spread Select Register.

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Table 3-1332. Instance Table

Instance Name	Physical Address
ADC_R0	502C 510Ch
ADC_R1	502C 710Ch

Figure 3-713. ADC_R_CFG_REP1SPREAD Name Register

31	30	29	28	27	26	25	24
SPREADCOUNT							
R							
0h							
23	22	21	20	19	18	17	16
SPREADCOUNT							
R							
0h							
15	14	13	12	11	10	9	8
SPREAD							
R/W							
0h							
7	6	5	4	3	2	1	0
SPREAD							
R/W							
0h							

Table 3-1333. ADC_R_CFG_REP1SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SPREADCOUNT	R	0h	ADC trigger repeater 1 spread status. When a trigger is sent to the ADC in oversampling mode, this register will start counting down from SPREAD until SPREADCOUNT equals 0. The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP1CTL.BUSY = 0 [SOCs associated with trigger repeater 1 are no longer pending].
15:0	SPREAD	R/W	0h	ADC trigger repeater 1 spread delay configuration. In oversampling mode, defines the minimum number of SYSCLKs to wait before creating the next repeated trigger to the ADC. If SPREAD is less than the time needed for all SOCs associated with repeater 1 to sample and convert, then the repeater will generate triggers as fast as the ADC can convert the associated conversions. If SPREAD is greater than the time needed for all SOCs associated with repeater 1 to sample and convert, then repeated triggers to the ADC will be SPREAD SYSCLK cycles apart. 0 = oversampled repeated triggers occur as fast as the ADC can sample and convert associated SOCs 1 = time between repeated triggers is at least 1 SYSCLKs 2 = time between repeated triggers is at least 2 SYSCLKs ... 65535 = time between repeated triggers is at least 65535 SYSCLKs

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3.14.2.71 ADC_R_CFG_REP1FRC Register

3.14.2.71.1 ADC_R_CFG_REP1FRC Register (Offset = 110h) [reset = 0h]

ADC Trigger Repeater 1 Software Force Register.

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Table 3-1334. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5110h
ADC_R1	502C 7110h

Figure 3-714. ADC_R_CFG_REP1FRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							SWFRC
R							R/W1TS
0h							0h

Table 3-1335. ADC_R_CFG_REP1FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	SWFRC	R/W1TS	0h	Write 1 to force a trigger to repeat block 1 input regardless of the value of TRIGGER. Always reads 0.

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3.14.2.72 ADC_R_CFG_REP2CTL Register

3.14.2.72.1 ADC_R_CFG_REP2CTL Register (Offset = 120h) [reset = 0h]

ADC Trigger Repeater 2 Control Register.

Return to Summary Table

Table 3-1336. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5120h
ADC_R1	502C 7120h

Figure 3-715. ADC_R_CFG_REP2CTL Name Register

31	30	29	28	27	26	25	24
RESERVED_5							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SWSYNC	RESERVED_4	SYNCINSEL					
R/W1TS	R	R/W					
0h	0h	0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_3	TRIGGER						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TRIGGEROVF	PHASEOVF	RESERVED_2	SOCBUSY	MODULEBUSY	RESERVED_1	ACTIVEMODE	MODE
R/W1TC	R/W1TC	R	R	R	R	R	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1337. ADC_R_CFG_REP2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_5	R	0h	Reserved
23	SWSYNC	R/W1TS	0h	Trigger repeater 2 software force sync. On a sync. event, all registers in repeater 2 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved. Note: SOCs associated with repeater 2 are not cleared.
22	RESERVED_4	R	0h	Reserved
21:16	SYNCINSEL	R/W	0h	Trigger repeater 2 sync. input select. On a sync. event, all registers in repeater 2 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved. Note: SOCs associated with repeater 2 are not cleared.
15	RESERVED_3	R	0h	Reserved

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Table 3-1337. ADC_R_CFG_REP2CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:8	TRIGGER	R/W	0h	ADC Trigger Repeater 2 Trigger Select. Selects the trigger to modify via oversampling or undersampling. 00h REPTRIG0 - Software only 01h REPTRIG1 - RTI0 Timer 02h REPTRIG2 - RTI1 Timer 03h REPTRIG3 - RTI2 Timer 04h REPTRIG4 - RTI3 Timer 05h REPTRIG5 - InputXBAR.Out[5] 06h REPTRIG6 - spare 07h REPTRIG7 - spare 08h REPTRIG8 - EPWM0, ADCSOCA 09h REPTRIG9 - EPWM0, ADCSOCB 0Ah REPTRIG10 - EPWM1, ADCSOCA 0Bh REPTRIG11 - EPWM1, ADCSOCB 0Ch REPTRIG12 - EPWM2, ADCSOCA 0Dh REPTRIG13 - EPWM2, ADCSOCB 0Eh REPTRIG14 - EPWM3, ADCSOCA 0Fh REPTRIG15 - EPWM3, ADCSOCB .... EPWM4 to EPWM27 40h REPTRIG64 - EPWM28, ADCSOCA 41h REPTRIG65 - EPWM28, ADCSOCB 42h REPTRIG66 - EPWM29, ADCSOCA 43h REPTRIG67 - EPWM29, ADCSOCB 44h REPTRIG68 - EPWM30, ADCSOCA 45h REPTRIG69 - EPWM30, ADCSOCB 46h REPTRIG70 - EPWM31, ADCSOCA 47h REPTRIG71 - EPWM31, ADCSOCB 48h REPTRIG72 - ECAP0, TRIGOUT .... ECAP1 to ECAP8 51h REPTRIG81 - ECAP9, TRIGOUT 52h REPTRIG82 - ECAP10, TRIGOUT .... 57h REPTRIG73 - ECAP15, TRIGOUT 58h REPTRIG1 - RTI4 Timer 59h REPTRIG1 - RTI5 Timer 5Ah REPTRIG1 - RTI6 Timer 5Bh REPTRIG1 - RTI7 Timer .... 64h- 7Fh - Reserved
7	TRIGGEROVF	R/W1TC	0h	ADC Trigger Repeater 2 Oversampled Trigger Overflow. Indicates that a trigger was dropped because a trigger arrived while the repeater was still generating repeated oversampled triggers [NCOUNT was not 0 or SOCs associated with Repeater 2 were still pending]. Writing a 1 will clear this flag. Note: This flag won't be set in undersampling mode or when NSEL = 0; if a trigger arrives before the previous SOCs have completed, the trigger will be passed and the overflow flags of the SOCs that were still pending will be set. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
6	PHASEOVF	R/W1TC	0h	ADC Trigger Repeater 2 Phase Delay Overflow. Indicates that a trigger was dropped because a trigger arrived when the phase delay logic was still waiting to send the delayed trigger [PHASECOUNT was not 0]. Writing a 1 will clear this flag. Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
5	RESERVED_2	R	0h	Reserved

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Table 3-1337. ADC_R_CFG_REP2CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SOCBUSY	R	0h	ADC Trigger Repeater 2 Associated SOCs Busy indicator. In oversampling mode: 0 = no SOCs associated with this repeater are pending 1 = SOCs associated with this repeater are still pending The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP2CTL.BUSY = 0 [SOCs associated with trigger repeater 2 are no longer pending]. Note: If the ADC is in burstmode and the BURSTTRIG is Repeater 2, then all round-robin SOCs are considered associated with this repeater and the repeater will not re-trigger until there are no pending round-robin SOCs [in addition to any associated pending high-priority SOCs].
3	MODULEBUSY	R	0h	ADC Trigger Repeater 2 Module Busy indicator. In oversampling mode: 0 = Repeater 2 is idle and can accept a new repeated trigger in oversampling mode 1 = Repeater 2 still has repeated triggers remaining [NCOUNT ' 0] or associated SOCs are still pending [SOCBUSY is 1] If a new oversampled trigger is received while the module is still busy, the TRIGGEROVF bit will be set and the trigger will be ignored.
2	RESERVED_1	R	0h	Reserved
1	ACTIVEMODE	R	0h	When a trigger is recived in oversampling or undersampling mode the value of MODE is copied to ACTIVEMODE. ACTIVEMODE determines if the repeater will repeat of filter triggers. Changes to MODE while the repeater is working therefore won't cause any changes in functionality until the module becomes idle and then a new trigger is received. 0 = module is oversampling 1 = module is undersampling
0	MODE	R/W	0h	ADC trigger repeater 2 mode selection. Select either oversampling or undersampling mode. In oversampling mode, when the trigger selected by REP2CTL.TRIGSEL is received, the repeater will repeat the trigger REP2N.NSEL + 1 times. In undersampling mode, when the trigger selected by REP2CTL.TRIGSEL is received the first time, the repeater will pass the trigger through. The next REP2N.NSEL triggers will be ignored. 0 = oversampling 1 = undersampling

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3.14.2.73 ADC_R_CFG_REP2N Register

3.14.2.73.1 ADC_R_CFG_REP2N Register (Offset = 124h) [reset = 0h]

ADC Trigger Repeater 2 N Select Register.

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Table 3-1338. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5124h
ADC_R1	502C 7124h

Figure 3-716. ADC_R_CFG_REP2N Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2	NCOUNT						
R	R						
0h	0h						
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1	NSEL						
R	R/W						
0h	0h						

Table 3-1339. ADC_R_CFG_REP2N Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED_2	R	0h	Reserved
22:16	NCOUNT	R	0h	ADC trigger repeater 2 trigger count. In oversampling mode, indicates the number of triggers remaining to be generated. If a trigger is received corresponding to REP2CTL.TRIGSEL while NCOUNT is not 0 [the repeater is still busy generating the repeated triggers] then the trigger will be ignored and REP2CTL.TRIGOVF will be set to 1. In undersampling mode, indicates the number of triggers remaining to be supressed.
15:7	RESERVED_1	R	0h	Reserved

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Table 3-1339. ADC_R_CFG_REP2N Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	NSEL	R/W	0h	ADC Trigger Repeater 2 selection of number of triggers. In oversampling mode, selects the number of repeated triggers. For each trigger received corresponding to REP2CTL.TRIGSEL, NSEL + 1 triggers will be generated. 0 = 1 trigger is generated [pass-through] 1 = 2 triggers are generated 2 = 3 triggers are generated ... 127 = 128 triggers are generated In undersampling mode, selects the number triggers to be supressed. 1 out NSEL + 1 triggers received corresponding to REP2CTL.TRIGSEL will be passed through [the first trigger will be passed through and the subsequent NSEL triggers will be supressed]. 0 = all triggers are passed 1 = 1 out of 2 triggers are passed 2 = 1 out of 3 triggers are passed ... 127 = 1 out of 128 triggers are passed

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3.14.2.74 ADC_R_CFG_REP2PHASE Register

3.14.2.74.1 ADC_R_CFG_REP2PHASE Register (Offset = 128h) [reset = 0h]

ADC Trigger Repeater 2 Phase Select Register.

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Table 3-1340. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5128h
ADC_R1	502C 7128h

Figure 3-717. ADC_R_CFG_REP2PHASE Name Register

31	30	29	28	27	26	25	24
PHASECOUNT							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHASECOUNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHASE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASE							
R/W							
0h							

Table 3-1341. ADC_R_CFG_REP2PHASE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PHASECOUNT	R	0h	ADC trigger repeater 2 phase delay status. When the trigger selected by REP2CTL.TRIGSEL is received, this register will start counting down from PHASECOUNT until the counter reaches 0, at which point the trigger will be passed on to the repeater re-trigger logic. If the trigger selected by REP2CTL.TRIGSEL is recieved when PHASECOUNT is not 0 [the phase delay logic is busy from the previous trigger] then the new trigger will be ignored and REP2CTL.PHASEOVF will be set to 1.
15:0	PHASE	R/W	0h	ADC trigger repeater 2 phase delay configuration. Defines the number of SYSCLKs to delay the selected trigger before passing it on to the re-triggering logic. 0 = trigger is passed through without delay 1 = trigger is delayed by 1 SYSCLK 2 = trigger is delayed by 2 SYSCLKs ... 65535 = trigger is delayed by 65535 SYSCLKs

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3.14.2.75 ADC_R_CFG_REP2SPREAD Register

3.14.2.75.1 ADC_R_CFG_REP2SPREAD Register (Offset = 12Ch) [reset = 0h]

ADC Trigger Repeater 2 Spread Select Register.

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Table 3-1342. Instance Table

Instance Name	Physical Address
ADC_R0	502C 512Ch
ADC_R1	502C 712Ch

Figure 3-718. ADC_R_CFG_REP2SPREAD Name Register

31	30	29	28	27	26	25	24
SPREADCOUNT							
R							
0h							
23	22	21	20	19	18	17	16
SPREADCOUNT							
R							
0h							
15	14	13	12	11	10	9	8
SPREAD							
R/W							
0h							
7	6	5	4	3	2	1	0
SPREAD							
R/W							
0h							

Table 3-1343. ADC_R_CFG_REP2SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SPREADCOUNT	R	0h	ADC trigger repeater 2 spread status. When a trigger is sent to the ADC in oversampling mode, this register will start counting down from SPREAD until SPREADCOUNT equals 0. The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP2CTL.BUSY = 0 [SOCs associated with trigger repeater 2 are no longer pending].
15:0	SPREAD	R/W	0h	ADC trigger repeater 2 spread delay configuration. In oversampling mode, defines the minimum number of SYSCLKs to wait before creating the next repeated trigger to the ADC. If SPREAD is less than the time needed for all SOCs associated with repeater 2 to sample and convert, then the repeater will generate triggers as fast as the ADC can convert the associated conversions. If SPREAD is greater than the time needed for all SOCs associated with repeater 2 to sample and convert, then repeated triggers to the ADC will be SPREAD SYSCLK cycles apart. 0 = oversampled repeated triggers occur as fast as the ADC can sample and convert associated SOCs 1 = time between repeated triggers is at least 1 SYSCLKs 2 = time between repeated triggers is at least 2 SYSCLKs ... 65535 = time between repeated triggers is at least 65535 SYSCLKs

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3.14.2.76 ADC_R_CFG_REP2FRC Register

3.14.2.76.1 ADC_R_CFG_REP2FRC Register (Offset = 130h) [reset = 0h]

ADC Trigger Repeater 2 Software Force Register.

Return to Summary Table

Table 3-1344. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5130h
ADC_R1	502C 7130h

Figure 3-719. ADC_R_CFG_REP2FRC Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							SWFRC
R							R/W1TS
0h							0h

Table 3-1345. ADC_R_CFG_REP2FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	SWFRC	R/W1TS	0h	Write 1 to force a trigger to repeat block 2 input regardless of the value of TRIGGER. Always reads 0.

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3.14.2.77 ADC_R_CFG_ADCPPB1LIMIT Register

3.14.2.77.1 ADC_R_CFG_ADCPPB1LIMIT Register (Offset = 140h) [reset = 0h]

ADC PPB1Conversion Count Limit Register.

Return to Summary Table

Table 3-1346. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5140h
ADC_R1	502C 7140h

Figure 3-720. ADC_R_CFG_ADCPPB1LIMIT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						LIMIT	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMIT							
R/W							
0h							

Table 3-1347. ADC_R_CFG_ADCPPB1LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	LIMIT	R/W	0h	Post Processing Block 1 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. To prevent PSUM from overflowing, do not write a value larger than 128 when the ADC is operating in 16-bit mode.

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3.14.2.78 ADC_R_CFG_ADCPPBP1PCOUNT Register

3.14.2.78.1 ADC_R_CFG_ADCPPBP1PCOUNT Register (Offset = 144h) [reset = 0h]

ADC PPB1 Partial Conversion Count Register.

Return to Summary Table

Table 3-1348. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5144h
ADC_R1	502C 7144h

Figure 3-721. ADC_R_CFG_ADCPPBP1PCOUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PCOUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCOUNT							
R							
0h							

Table 3-1349. ADC_R_CFG_ADCPPBP1PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PCOUNT	R	0h	Post Processing Block 1 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB1PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.79 ADC_R_CFG_ADCPPB1CONFIG2 Register

3.14.2.79.1 ADC_R_CFG_ADCPPB1CONFIG2 Register (Offset = 148h) [reset = 0h]

ADC PPB1 Sum Shift Register.

Return to Summary Table

Table 3-1350. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5148h
ADC_R1	502C 7148h

Figure 3-722. ADC_R_CFG_ADCPPB1CONFIG2 Name Register

15	14	13	12	11	10	9	8
COMPSEL		RESERVED_2	OSINTSEL	SWSYNC	RESERVED_1	SYNCINSEL	
R/W		R	R/W	R/W1TS	R	R/W	
0h		0h	0h	0h	0h	0h	

7	6	5	4	3	2	1	0
SYNCINSEL				SHIFT			
R/W				R/W			
0h				0h			

Table 3-1351. ADC_R_CFG_ADCPPB1CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	COMPSEL	R/W	0h	Post Processing Block 1 Compare Source Select. This field determines whether ADCPPB1RESULT, ADCPPB1PSUM, or ADCPPB1SUM is used for the zero-crossing detect logic and threshold compare. 00 = ADCPPB1RESULT is used for compare logic 01 = ADCPPB1PSUM is used for compare logic 10 = ADCPPB1SUM is used for compare logic 11 = Reserved Note: when ADCPPB1PSUM is selected as the compare source and when a LIMIT match occurs [ADCPPB1LIMIT equals ADCPPB1COUNT] the ADCPPB1PSUM register will be cleared and the final sum will be loaded into ADCPPB1SUM. For this sample, the final sum, ADCPPB1SUM will be used for the compariosn instead of ADCPPB1PSUM.
13	RESERVED_2	R	0h	Reserved
12	OSINTSEL	R/W	0h	Post Processing Block 1 Interrupt Source Select. OSINT1 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT1 in addition to a PCOUNT = LIMIT event. 0 = OSINT1 will be generated from PCOUNT = LIMIT only 1 = OSTIN1 will be generated form PCOUNT = LIMIT or a sync. event. Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.
11	SWSYNC	R/W1TS	0h	PPB 1 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur.
10	RESERVED_1	R	0h	Reserved
9:4	SYNCINSEL	R/W	0h	PPB 1 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details

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Table 3-1351. ADC_R_CFG_ADCPPB1CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SHIFT	R/W	0h	Post Processing Block 1 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM " 1 2 : SUM = PSUM " 2 ... 10 : SUM = PSUM " 10 11 - 15 : Reserved

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3.14.2.80 ADC_R_CFG_ADCPPB1PSUM Register

3.14.2.80.1 ADC_R_CFG_ADCPPB1PSUM Register (Offset = 14Ch) [reset = 0h]

ADC PPB1 Partial Sum Register.

Return to Summary Table

Table 3-1352. Instance Table

Instance Name	Physical Address
ADC_R0	502C 514Ch
ADC_R1	502C 714Ch

Figure 3-723. ADC_R_CFG_ADCPPB1PSUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
PSUM							
R							
0h							
15	14	13	12	11	10	9	8
PSUM							
R							
0h							
7	6	5	4	3	2	1	0
PSUM							
R							
0h							

Table 3-1353. ADC_R_CFG_ADCPPB1PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	PSUM	R	0h	Post Processing Block 1 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information].

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3.14.2.81 ADC_R_CFG_ADCPPB1PMAX Register

3.14.2.81.1 ADC_R_CFG_ADCPPB1PMAX Register (Offset = 150h) [reset = 0h]

ADC PPB1 Partial Max Register.

Return to Summary Table

Table 3-1354. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5150h
ADC_R1	502C 7150h

Figure 3-724. ADC_R_CFG_ADCPPB1PMAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							PMAX
R							R
0h							0h
15	14	13	12	11	10	9	8
PMAX							
R							
0h							
7	6	5	4	3	2	1	0
PMAX							
R							
0h							

Table 3-1355. ADC_R_CFG_ADCPPB1PMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMAX	R	0h	Post Processing Block 1 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.82 ADC_R_CFG_ADCPPB1PMAXI Register

3.14.2.82.1 ADC_R_CFG_ADCPPB1PMAXI Register (Offset = 154h) [reset = 0h]

ADC PPB1 Partial Max Index Register.

Return to Summary Table

Table 3-1356. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5154h
ADC_R1	502C 7154h

Figure 3-725. ADC_R_CFG_ADCPPB1PMAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMAXI							
R							
0h							

Table 3-1357. ADC_R_CFG_ADCPPB1PMAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMAXI	R	0h	Post Processing Block 1 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.83 ADC_R_CFG_ADCPPB1PMIN Register

3.14.2.83.1 ADC_R_CFG_ADCPPB1PMIN Register (Offset = 158h) [reset = 0h]

ADC PPB1 Partial MIN Register.

Return to Summary Table

Table 3-1358. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5158h
ADC_R1	502C 7158h

Figure 3-726. ADC_R_CFG_ADCPPB1PMIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							PMIN
R							R
0h							0h
15	14	13	12	11	10	9	8
PMIN							
R							
0h							
7	6	5	4	3	2	1	0
PMIN							
R							
0h							

Table 3-1359. ADC_R_CFG_ADCPPB1PMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMIN	R	0h	Post Processing Block 1 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.84 ADC_R_CFG_ADCPPB1PMINI Register

3.14.2.84.1 ADC_R_CFG_ADCPPB1PMINI Register (Offset = 15Ch) [reset = 0h]

ADC PPB1 Partial Min Index Register.

Return to Summary Table

Table 3-1360. Instance Table

Instance Name	Physical Address
ADC_R0	502C 515Ch
ADC_R1	502C 715Ch

Figure 3-727. ADC_R_CFG_ADCPPB1PMINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMINI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMINI							
R							
0h							

Table 3-1361. ADC_R_CFG_ADCPPB1PMINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMINI	R	0h	Post Processing Block 1 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.85 ADC_R_CFG_ADCPPB1TRIPLO2 Register

3.14.2.85.1 ADC_R_CFG_ADCPPB1TRIPLO2 Register (Offset = 160h) [reset = 0h]

ADC PPB1 Extended Trip Low Register.

Return to Summary Table

Table 3-1362. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5160h
ADC_R1	502C 7160h

Figure 3-728. ADC_R_CFG_ADCPPB1TRIPLO2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITLO							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITLO							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITLO							
R/W							
0h							

Table 3-1363. ADC_R_CFG_ADCPPB1TRIPLO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITLO	R/W	0h	ADC Post Processing Block 1 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB1TRIPLO.LIMITLO2EN = 1. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPLO2[23:17] will be ignored in 16 bit mode - TRIPLO2[23:13] will be ignored in 12 bit mode

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3.14.2.86 ADC_R_CFG_ADCPPB2LIMIT Register

3.14.2.86.1 ADC_R_CFG_ADCPPB2LIMIT Register (Offset = 174h) [reset = 0h]

ADC PPB2Conversion Count Limit Register.

Return to Summary Table

Table 3-1364. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5174h
ADC_R1	502C 7174h

Figure 3-729. ADC_R_CFG_ADCPPB2LIMIT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						LIMIT	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMIT							
R/W							
0h							

Table 3-1365. ADC_R_CFG_ADCPPB2LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	LIMIT	R/W	0h	Post Processing Block 2 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. To prevent PSUM from overflowing, do not write a value larger than 128 when the ADC is operating in 16-bit mode.

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3.14.2.87 ADC_R_CFG_ADCPPBP2PCOUNT Register

3.14.2.87.1 ADC_R_CFG_ADCPPBP2PCOUNT Register (Offset = 178h) [reset = 0h]

ADC PPB2 Partial Conversion Count Register.

Return to Summary Table

Table 3-1366. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5178h
ADC_R1	502C 7178h

Figure 3-730. ADC_R_CFG_ADCPPBP2PCOUNT Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED_1</td><td colspan="2">PCOUNT</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PCOUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 3-1367. ADC_R_CFG_ADCPPBP2PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PCOUNT	R	0h	Post Processing Block 2 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB2PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.88 ADC_R_CFG_ADCPPB2CONFIG2 Register

3.14.2.88.1 ADC_R_CFG_ADCPPB2CONFIG2 Register (Offset = 17Ch) [reset = 0h]

ADC PPB2 Sum Shift Register.

Return to Summary Table

Table 3-1368. Instance Table

Instance Name	Physical Address
ADC_R0	502C 517Ch
ADC_R1	502C 717Ch

Figure 3-731. ADC_R_CFG_ADCPPB2CONFIG2 Name Register

15	14	13	12	11	10	9	8
COMPSEL		RESERVED_2	OSINTSEL	SWSYNC	RESERVED_1	SYNCINSEL	
R/W		R	R/W	R/W1TS	R	R/W	
0h		0h	0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYNCINSEL				SHIFT			
R/W				R/W			
0h				0h			

Table 3-1369. ADC_R_CFG_ADCPPB2CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	COMPSEL	R/W	0h	Post Processing Block 2 Compare Source Select. This field determines whether ADCPPB2RESULT, ADCPPB2PSUM, or ADCPPB2SUM is used for the zero-crossing detect logic and threshold compare. 00 = ADCPPB2RESULT is used for compare logic 01 = ADCPPB2PSUM is used for compare logic 10 = ADCPPB2SUM is used for compare logic 11 = Reserved Note: when ADCPPB2PSUM is selected as the compare source and when a LIMIT match occurs [ADCPPB2LIMIT equals ADCPPB2COUNT] the ADCPPB2PSUM register will be cleared and the final sum will be loaded into ADCPPB2SUM. For this sample, the final sum, ADCPPB2SUM will be used for the compariosn instead of ADCPPB2PSUM.
13	RESERVED_2	R	0h	Reserved
12	OSINTSEL	R/W	0h	Post Processing Block 2 Interrupt Source Select. OSINT2 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT2 in addition to a PCOUNT = LIMIT event. 0 = OSINT2 will be generated from PCOUNT = LIMIT only 1 = OSTIN2 will be generated form PCOUNT = LIMIT or a sync. event. Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.
11	SWSYNC	R/W1TS	0h	PPB 2 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur.
10	RESERVED_1	R	0h	Reserved
9:4	SYNCINSEL	R/W	0h	PPB 2 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details

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Table 3-1369. ADC_R_CFG_ADCPPB2CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SHIFT	R/W	0h	Post Processing Block 2 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM " 1 2 : SUM = PSUM " 2 ... 10 : SUM = PSUM " 10 11 - 15 : Reserved

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3.14.2.89 ADC_R_CFG_ADCPPB2PSUM Register

3.14.2.89.1 ADC_R_CFG_ADCPPB2PSUM Register (Offset = 180h) [reset = 0h]

ADC PPB2 Partial Sum Register.

Return to Summary Table

Table 3-1370. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5180h
ADC_R1	502C 7180h

Figure 3-732. ADC_R_CFG_ADCPPB2PSUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
PSUM							
R							
0h							
15	14	13	12	11	10	9	8
PSUM							
R							
0h							
7	6	5	4	3	2	1	0
PSUM							
R							
0h							

Table 3-1371. ADC_R_CFG_ADCPPB2PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	PSUM	R	0h	Post Processing Block 2 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information].

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3.14.2.90 ADC_R_CFG_ADCPPB2PMAX Register

3.14.2.90.1 ADC_R_CFG_ADCPPB2PMAX Register (Offset = 184h) [reset = 0h]

ADC PPB2 Partial Max Register.

Return to Summary Table

Table 3-1372. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5184h
ADC_R1	502C 7184h

Figure 3-733. ADC_R_CFG_ADCPPB2PMAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							PMAX
R							R
0h							0h
15	14	13	12	11	10	9	8
PMAX							
R							
0h							
7	6	5	4	3	2	1	0
PMAX							
R							
0h							

Table 3-1373. ADC_R_CFG_ADCPPB2PMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMAX	R	0h	Post Processing Block 2 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.91 ADC_R_CFG_ADCPPB2PMAXI Register

3.14.2.91.1 ADC_R_CFG_ADCPPB2PMAXI Register (Offset = 188h) [reset = 0h]

ADC PPB2 Partial Max Index Register.

Return to Summary Table

Table 3-1374. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5188h
ADC_R1	502C 7188h

Figure 3-734. ADC_R_CFG_ADCPPB2PMAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMAXI							
R							
0h							

Table 3-1375. ADC_R_CFG_ADCPPB2PMAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMAXI	R	0h	Post Processing Block 2 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.92 ADC_R_CFG_ADCPPB2PMIN Register

3.14.2.92.1 ADC_R_CFG_ADCPPB2PMIN Register (Offset = 18Ch) [reset = 0h]

ADC PPB2 Partial MIN Register.

Return to Summary Table

Table 3-1376. Instance Table

Instance Name	Physical Address
ADC_R0	502C 518Ch
ADC_R1	502C 718Ch

Figure 3-735. ADC_R_CFG_ADCPPB2PMIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							PMIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMIN							
R							
0h							

Table 3-1377. ADC_R_CFG_ADCPPB2PMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMIN	R	0h	Post Processing Block 2 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.93 ADC_R_CFG_ADCPPB2PMINI Register

3.14.2.93.1 ADC_R_CFG_ADCPPB2PMINI Register (Offset = 190h) [reset = 0h]

ADC PPB2 Partial Min Index Register.

Return to Summary Table

Table 3-1378. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5190h
ADC_R1	502C 7190h

Figure 3-736. ADC_R_CFG_ADCPPB2PMINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMINI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
PMINI							
R							
0h							

Table 3-1379. ADC_R_CFG_ADCPPB2PMINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMINI	R	0h	Post Processing Block 2 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.94 ADC_R_CFG_ADCPPB2TRIPLO2 Register

3.14.2.94.1 ADC_R_CFG_ADCPPB2TRIPLO2 Register (Offset = 194h) [reset = 0h]

ADC PPB2 Extended Trip Low Register.

Return to Summary Table

Table 3-1380. Instance Table

Instance Name	Physical Address
ADC_R0	502C 5194h
ADC_R1	502C 7194h

Figure 3-737. ADC_R_CFG_ADCPPB2TRIPLO2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
LIMITLO							
R/W							
0h							
15	14	13	12	11	10	9	8
LIMITLO							
R/W							
0h							
7	6	5	4	3	2	1	0
LIMITLO							
R/W							
0h							

Table 3-1381. ADC_R_CFG_ADCPPB2TRIPLO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITLO	R/W	0h	ADC Post Processing Block 2 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB2TRIPLO.LIMITLO2EN = 1. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPLO2[23:17] will be ignored in 16 bit mode - TRIPLO2[23:13] will be ignored in 12 bit mode

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3.14.2.95 ADC_R_CFG_ADCPPB3LIMIT Register

3.14.2.95.1 ADC_R_CFG_ADCPPB3LIMIT Register (Offset = 1A8h) [reset = 0h]

ADC PPB3Conversion Count Limit Register.

Return to Summary Table

Table 3-1382. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51A8h
ADC_R1	502C 71A8h

Figure 3-738. ADC_R_CFG_ADCPPB3LIMIT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						LIMIT	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMIT							
R/W							
0h							

Table 3-1383. ADC_R_CFG_ADCPPB3LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	LIMIT	R/W	0h	Post Processing Block 3 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. To prevent PSUM from overflowing, do not write a value larger than 128 when the ADC is operating in 16-bit mode.

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3.14.2.96 ADC_R_CFG_ADCPPBP3PCOUNT Register

3.14.2.96.1 ADC_R_CFG_ADCPPBP3PCOUNT Register (Offset = 1ACh) [reset = 0h]

ADC PPB3 Partial Conversion Count Register.

Return to Summary Table

Table 3-1384. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51ACh
ADC_R1	502C 71ACh

Figure 3-739. ADC_R_CFG_ADCPPBP3PCOUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PCOUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCOUNT							
R							
0h							

Table 3-1385. ADC_R_CFG_ADCPPBP3PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PCOUNT	R	0h	Post Processing Block 3 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB3PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.97 ADC_R_CFG_ADCPPB3CONFIG2 Register

3.14.2.97.1 ADC_R_CFG_ADCPPB3CONFIG2 Register (Offset = 1B0h) [reset = 0h]

ADC PPB3 Sum Shift Register.

Return to Summary Table

Table 3-1386. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51B0h
ADC_R1	502C 71B0h

Figure 3-740. ADC_R_CFG_ADCPPB3CONFIG2 Name Register

15	14	13	12	11	10	9	8
COMPSEL		RESERVED_2	OSINTSEL	SWSYNC	RESERVED_1	SYNCINSEL	
R/W		R	R/W	R/W1TS	R	R/W	
0h		0h	0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYNCINSEL				SHIFT			
R/W				R/W			
0h				0h			

Table 3-1387. ADC_R_CFG_ADCPPB3CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	COMPSEL	R/W	0h	Post Processing Block 3 Compare Source Select. This field determines whether ADCPPB3RESULT, ADCPPB3PSUM, or ADCPPB3SUM is used for the zero-crossing detect logic and threshold compare. 00 = ADCPPB3RESULT is used for compare logic 01 = ADCPPB3PSUM is used for compare logic 10 = ADCPPB3SUM is used for compare logic 11 = Reserved Note: when ADCPPB3PSUM is selected as the compare source and when a LIMIT match occurs [ADCPPB3LIMIT equals ADCPPB3COUNT] the ADCPPB3PSUM register will be cleared and the final sum will be loaded into ADCPPB3SUM. For this sample, the final sum, ADCPPB3SUM will be used for the compariosn instead of ADCPPB3PSUM.
13	RESERVED_2	R	0h	Reserved
12	OSINTSEL	R/W	0h	Post Processing Block 3 Interrupt Source Select. OSINT3 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT3 in addition to a PCOUNT = LIMIT event. 0 = OSINT3 will be generated from PCOUNT = LIMIT only 1 = OSTIN3 will be generated form PCOUNT = LIMIT or a sync. event. Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.
11	SWSYNC	R/W1TS	0h	PPB 3 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur.
10	RESERVED_1	R	0h	Reserved
9:4	SYNCINSEL	R/W	0h	PPB 3 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details

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Table 3-1387. ADC_R_CFG_ADCPPB3CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SHIFT	R/W	0h	Post Processing Block 3 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM " 1 2 : SUM = PSUM " 2 ... 10 : SUM = PSUM " 10 11 - 15 : Reserved

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3.14.2.98 ADC_R_CFG_ADCPPB3PSUM Register

3.14.2.98.1 ADC_R_CFG_ADCPPB3PSUM Register (Offset = 1B4h) [reset = 0h]

ADC PPB3 Partial Sum Register.

Return to Summary Table

Table 3-1388. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51B4h
ADC_R1	502C 71B4h

Figure 3-741. ADC_R_CFG_ADCPPB3PSUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
PSUM							
R							
0h							
15	14	13	12	11	10	9	8
PSUM							
R							
0h							
7	6	5	4	3	2	1	0
PSUM							
R							
0h							

Table 3-1389. ADC_R_CFG_ADCPPB3PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	PSUM	R	0h	Post Processing Block 3 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information].

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3.14.2.99 ADC_R_CFG_ADCPPB3PMAX Register

3.14.2.99.1 ADC_R_CFG_ADCPPB3PMAX Register (Offset = 1B8h) [reset = 0h]

ADC PPB3 Partial Max Register.

Return to Summary Table

Table 3-1390. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51B8h
ADC_R1	502C 71B8h

Figure 3-742. ADC_R_CFG_ADCPPB3PMAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							PMAX
R							R
0h							0h
15	14	13	12	11	10	9	8
PMAX							
R							
0h							
7	6	5	4	3	2	1	0
PMAX							
R							
0h							

Table 3-1391. ADC_R_CFG_ADCPPB3PMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMAX	R	0h	Post Processing Block 3 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.100 ADC_R_CFG_ADCPPB3PMAXI Register

3.14.2.100.1 ADC_R_CFG_ADCPPB3PMAXI Register (Offset = 1BCh) [reset = 0h]

ADC PPB3 Partial Max Index Register.

Return to Summary Table

Table 3-1392. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51BCh
ADC_R1	502C 71BCh

Figure 3-743. ADC_R_CFG_ADCPPB3PMAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMAXI							
R							
0h							

Table 3-1393. ADC_R_CFG_ADCPPB3PMAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMAXI	R	0h	Post Processing Block 3 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.101 ADC_R_CFG_ADCPPB3PMIN Register

3.14.2.101.1 ADC_R_CFG_ADCPPB3PMIN Register (Offset = 1C0h) [reset = 0h]

ADC PPB3 Partial MIN Register.

Return to Summary Table

Table 3-1394. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51C0h
ADC_R1	502C 71C0h

Figure 3-744. ADC_R_CFG_ADCPPB3PMIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							PMIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMIN							
R							
0h							

Table 3-1395. ADC_R_CFG_ADCPPB3PMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMIN	R	0h	Post Processing Block 3 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.102 ADC_R_CFG_ADCPPB3PMINI Register

3.14.2.102.1 ADC_R_CFG_ADCPPB3PMINI Register (Offset = 1C4h) [reset = 0h]

ADC PPB3 Partial Min Index Register.

Return to Summary Table

Table 3-1396. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51C4h
ADC_R1	502C 71C4h

Figure 3-745. ADC_R_CFG_ADCPPB3PMINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMINI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMINI							
R							
0h							

Table 3-1397. ADC_R_CFG_ADCPPB3PMINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMINI	R	0h	Post Processing Block 3 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.103 ADC_R_CFG_ADCPPB3TRIPLO2 Register

3.14.2.103.1 ADC_R_CFG_ADCPPB3TRIPLO2 Register (Offset = 1C8h) [reset = 0h]

ADC PPB3 Extended Trip Low Register.

Return to Summary Table

Table 3-1398. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51C8h
ADC_R1	502C 71C8h

Figure 3-746. ADC_R_CFG_ADCPPB3TRIPLO2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LIMITLO							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LIMITLO							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMITLO							
R/W							
0h							

Table 3-1399. ADC_R_CFG_ADCPPB3TRIPLO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITLO	R/W	0h	ADC Post Processing Block 3 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB3TRIPLO.LIMITLO2EN = 1. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPLO2[23:17] will be ignored in 16 bit mode - TRIPLO2[23:13] will be ignored in 12 bit mode

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3.14.2.104 ADC_R_CFG_ADCPPB4LIMIT Register

3.14.2.104.1 ADC_R_CFG_ADCPPB4LIMIT Register (Offset = 1DCh) [reset = 0h]

ADC PPB4Conversion Count Limit Register.

Return to Summary Table

Table 3-1400. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51DCh
ADC_R1	502C 71DCh

Figure 3-747. ADC_R_CFG_ADCPPB4LIMIT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						LIMIT	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMIT							
R/W							
0h							

Table 3-1401. ADC_R_CFG_ADCPPB4LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	LIMIT	R/W	0h	Post Processing Block 4 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. To prevent PSUM from overflowing, do not write a value larger than 128 when the ADC is operating in 16-bit mode.

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3.14.2.105 ADC_R_CFG_ADCPPBP4PCOUNT Register

3.14.2.105.1 ADC_R_CFG_ADCPPBP4PCOUNT Register (Offset = 1E0h) [reset = 0h]

ADC PPB4 Partial Conversion Count Register.

Return to Summary Table

Table 3-1402. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51E0h
ADC_R1	502C 71E0h

Figure 3-748. ADC_R_CFG_ADCPPBP4PCOUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PCOUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCOUNT							
R							
0h							

Table 3-1403. ADC_R_CFG_ADCPPBP4PCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PCOUNT	R	0h	Post Processing Block 4 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB4PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.14.2.106 ADC_R_CFG_ADCPPB4CONFIG2 Register

3.14.2.106.1 ADC_R_CFG_ADCPPB4CONFIG2 Register (Offset = 1E4h) [reset = 0h]

ADC PPB4 Sum Shift Register.

Return to Summary Table

Table 3-1404. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51E4h
ADC_R1	502C 71E4h

Figure 3-749. ADC_R_CFG_ADCPPB4CONFIG2 Name Register

15	14	13	12	11	10	9	8
COMPSEL		RESERVED_2	OSINTSEL	SWSYNC	RESERVED_1	SYNCINSEL	
R/W		R	R/W	R/W1TS	R	R/W	
0h		0h	0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYNCINSEL				SHIFT			
R/W				R/W			
0h				0h			

Table 3-1405. ADC_R_CFG_ADCPPB4CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	COMPSEL	R/W	0h	Post Processing Block 4 Compare Source Select. This field determines whether ADCPPB4RESULT, ADCPPB4PSUM, or ADCPPB4SUM is used for the zero-crossing detect logic and threshold compare. 00 = ADCPPB4RESULT is used for compare logic 01 = ADCPPB4PSUM is used for compare logic 10 = ADCPPB4SUM is used for compare logic 11 = Reserved Note: when ADCPPB4PSUM is selected as the compare source and when a LIMIT match occurs [ADCPPB4LIMIT equals ADCPPB4COUNT] the ADCPPB4PSUM register will be cleared and the final sum will be loaded into ADCPPB4SUM. For this sample, the final sum, ADCPPB4SUM will be used for the compariosn instead of ADCPPB4PSUM.
13	RESERVED_2	R	0h	Reserved
12	OSINTSEL	R/W	0h	Post Processing Block 4 Interrupt Source Select. OSINT4 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT4 in addition to a PCOUNT = LIMIT event. 0 = OSINT4 will be generated from PCOUNT = LIMIT only 1 = OSTIN4 will be generated form PCOUNT = LIMIT or a sync. event. Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.
11	SWSYNC	R/W1TS	0h	PPB 4 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset. Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur.
10	RESERVED_1	R	0h	Reserved
9:4	SYNCINSEL	R/W	0h	PPB 4 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset. Refer to SOC spec for details

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Table 3-1405. ADC_R_CFG_ADCPPB4CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SHIFT	R/W	0h	Post Processing Block 4 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM. 0 : no right shift 1 : SUM = PSUM " 1 2 : SUM = PSUM " 2 ... 10 : SUM = PSUM " 10 11 - 15 : Reserved

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3.14.2.107 ADC_R_CFG_ADCPPB4PSUM Register

3.14.2.107.1 ADC_R_CFG_ADCPPB4PSUM Register (Offset = 1E8h) [reset = 0h]

ADC PPB4 Partial Sum Register.

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Table 3-1406. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51E8h
ADC_R1	502C 71E8h

Figure 3-750. ADC_R_CFG_ADCPPB4PSUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PSUM							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PSUM							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PSUM							
R							
0h							

Table 3-1407. ADC_R_CFG_ADCPPB4PSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	PSUM	R	0h	Post Processing Block 4 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT the result is subsequently accumulated into this register. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information].

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3.14.2.108 ADC_R_CFG_ADCPPB4PMAX Register

3.14.2.108.1 ADC_R_CFG_ADCPPB4PMAX Register (Offset = 1ECh) [reset = 0h]

ADC PPB4 Partial Max Register.

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Table 3-1408. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51ECh
ADC_R1	502C 71ECh

Figure 3-751. ADC_R_CFG_ADCPPB4PMAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							PMAX
R							R
0h							0h
15	14	13	12	11	10	9	8
PMAX							
R							
0h							
7	6	5	4	3	2	1	0
PMAX							
R							
0h							

Table 3-1409. ADC_R_CFG_ADCPPB4PMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMAX	R	0h	Post Processing Block 4 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.14.2.109 ADC_R_CFG_ADCPPB4PMAXI Register

3.14.2.109.1 ADC_R_CFG_ADCPPB4PMAXI Register (Offset = 1F0h) [reset = 0h]

ADC PPB4 Partial Max Index Register.

Return to Summary Table

Table 3-1410. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51F0h
ADC_R1	502C 71F0h

Figure 3-752. ADC_R_CFG_ADCPPB4PMAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMAXI							
R							
0h							

Table 3-1411. ADC_R_CFG_ADCPPB4PMAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMAXI	R	0h	Post Processing Block 4 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.14.2.110 ADC_R_CFG_ADCPPB4PMIN Register

3.14.2.110.1 ADC_R_CFG_ADCPPB4PMIN Register (Offset = 1F4h) [reset = 0h]

ADC PPB4 Partial MIN Register.

Return to Summary Table

Table 3-1412. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51F4h
ADC_R1	502C 71F4h

Figure 3-753. ADC_R_CFG_ADCPPB4PMIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							PMIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PMIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMIN							
R							
0h							

Table 3-1413. ADC_R_CFG_ADCPPB4PMIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	PMIN	R	0h	Post Processing Block 4 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.14.2.111 ADC_R_CFG_ADCPPB4PMINI Register

3.14.2.111.1 ADC_R_CFG_ADCPPB4PMINI Register (Offset = 1F8h) [reset = 0h]

ADC PPB4 Partial Min Index Register.

Return to Summary Table

Table 3-1414. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51F8h
ADC_R1	502C 71F8h

Figure 3-754. ADC_R_CFG_ADCPPB4PMINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						PMINI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PMINI							
R							
0h							

Table 3-1415. ADC_R_CFG_ADCPPB4PMINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	PMINI	R	0h	Post Processing Block 4 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.14.2.112 ADC_R_CFG_ADCPPB4TRIPLO2 Register

3.14.2.112.1 ADC_R_CFG_ADCPPB4TRIPLO2 Register (Offset = 1FCh) [reset = 0h]

ADC PPB4 Extended Trip Low Register.

Return to Summary Table

Table 3-1416. Instance Table

Instance Name	Physical Address
ADC_R0	502C 51FCh
ADC_R1	502C 71FCh

Figure 3-755. ADC_R_CFG_ADCPPB4TRIPLO2 Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LIMITLO							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LIMITLO							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LIMITLO							
R/W							
0h							

Table 3-1417. ADC_R_CFG_ADCPPB4TRIPLO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:0	LIMITLO	R/W	0h	ADC Post Processing Block 4 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB4TRIPLO.LIMITLO2EN = 1. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored: - TRIPLO2[23:17] will be ignored in 16 bit mode - TRIPLO2[23:13] will be ignored in 12 bit mode

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3.14.2.113 ADC_R_RESULTS_ADCRESULT0 Register

3.14.2.113.1 ADC_R_RESULTS_ADCRESULT0 Register (Offset = 0h) [reset = 0h]

ADC Result 0 Register.

Return to Summary Table

Table 3-1418. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6000h
ADC_R1	502C 8000h

Figure 3-756. ADC_R_RESULTS_ADCRESULT0 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1419. ADC_R_RESULTS_ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 0 16-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field.

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3.14.2.114 ADC_R_RESULTS_ADCRESULT1 Register

3.14.2.114.1 ADC_R_RESULTS_ADCRESULT1 Register (Offset = 2h) [reset = 0h]

ADC Result 1 Register.

Return to Summary Table

Table 3-1420. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6002h
ADC_R1	502C 8002h

Figure 3-757. ADC_R_RESULTS_ADCRESULT1 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1421. ADC_R_RESULTS_ADCRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 1 16-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field.

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3.14.2.115 ADC_R_RESULTS_ADCRESULT2 Register

3.14.2.115.1 ADC_R_RESULTS_ADCRESULT2 Register (Offset = 4h) [reset = 0h]

ADC Result 2 Register.

Return to Summary Table

Table 3-1422. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6004h
ADC_R1	502C 8004h

Figure 3-758. ADC_R_RESULTS_ADCRESULT2 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1423. ADC_R_RESULTS_ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 2 16-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field.

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3.14.2.116 ADC_R_RESULTS_ADCRESULT3 Register

3.14.2.116.1 ADC_R_RESULTS_ADCRESULT3 Register (Offset = 6h) [reset = 0h]

ADC Result 3 Register.

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Table 3-1424. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6006h
ADC_R1	502C 8006h

Figure 3-759. ADC_R_RESULTS_ADCRESULT3 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1425. ADC_R_RESULTS_ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 3 16-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field.

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3.14.2.117 ADC_R_RESULTS_ADCRESULT4 Register

3.14.2.117.1 ADC_R_RESULTS_ADCRESULT4 Register (Offset = 8h) [reset = 0h]

ADC Result 4 Register.

Return to Summary Table

Table 3-1426. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6008h
ADC_R1	502C 8008h

Figure 3-760. ADC_R_RESULTS_ADCRESULT4 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1427. ADC_R_RESULTS_ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 4 16-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field.

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3.14.2.118 ADC_R_RESULTS_ADCRESULT5 Register

3.14.2.118.1 ADC_R_RESULTS_ADCRESULT5 Register (Offset = Ah) [reset = 0h]

ADC Result 5 Register.

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Table 3-1428. Instance Table

Instance Name	Physical Address
ADC_R0	502C 600Ah
ADC_R1	502C 800Ah

Figure 3-761. ADC_R_RESULTS_ADCRESULT5 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1429. ADC_R_RESULTS_ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 5 16-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field.

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3.14.2.119 ADC_R_RESULTS_ADCRESULT6 Register

3.14.2.119.1 ADC_R_RESULTS_ADCRESULT6 Register (Offset = Ch) [reset = 0h]

ADC Result 6 Register.

Return to Summary Table

Table 3-1430. Instance Table

Instance Name	Physical Address
ADC_R0	502C 600Ch
ADC_R1	502C 800Ch

Figure 3-762. ADC_R_RESULTS_ADCRESULT6 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-1431. ADC_R_RESULTS_ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 6 16-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field.

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3.14.2.120 ADC_R_RESULTS_ADCRESULT7 Register

3.14.2.120.1 ADC_R_RESULTS_ADCRESULT7 Register (Offset = Eh) [reset = 0h]

ADC Result 7 Register.

Return to Summary Table

Table 3-1432. Instance Table

Instance Name	Physical Address
ADC_R0	502C 600Eh
ADC_R1	502C 800Eh

Figure 3-763. ADC_R_RESULTS_ADCRESULT7 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1433. ADC_R_RESULTS_ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 7 16-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field.

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3.14.2.121 ADC_R_RESULTS_ADCRESULT8 Register

3.14.2.121.1 ADC_R_RESULTS_ADCRESULT8 Register (Offset = 10h) [reset = 0h]

ADC Result 8 Register.

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Table 3-1434. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6010h
ADC_R1	502C 8010h

Figure 3-764. ADC_R_RESULTS_ADCRESULT8 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-1435. ADC_R_RESULTS_ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 8 16-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field.

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3.14.2.122 ADC_R_RESULTS_ADCRESULT9 Register

3.14.2.122.1 ADC_R_RESULTS_ADCRESULT9 Register (Offset = 12h) [reset = 0h]

ADC Result 9 Register.

Return to Summary Table

Table 3-1436. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6012h
ADC_R1	502C 8012h

Figure 3-765. ADC_R_RESULTS_ADCRESULT9 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1437. ADC_R_RESULTS_ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 9 16-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field.

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3.14.2.123 ADC_R_RESULTS_ADCRESULT10 Register

3.14.2.123.1 ADC_R_RESULTS_ADCRESULT10 Register (Offset = 14h) [reset = 0h]

ADC Result 10 Register.

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Table 3-1438. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6014h
ADC_R1	502C 8014h

Figure 3-766. ADC_R_RESULTS_ADCRESULT10 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1439. ADC_R_RESULTS_ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 10 16-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field.

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3.14.2.124 ADC_R_RESULTS_ADCRESULT11 Register

3.14.2.124.1 ADC_R_RESULTS_ADCRESULT11 Register (Offset = 16h) [reset = 0h]

ADC Result 11 Register.

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Table 3-1440. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6016h
ADC_R1	502C 8016h

Figure 3-767. ADC_R_RESULTS_ADCRESULT11 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1441. ADC_R_RESULTS_ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 11 16-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field.

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3.14.2.125 ADC_R_RESULTS_ADCRESULT12 Register

3.14.2.125.1 ADC_R_RESULTS_ADCRESULT12 Register (Offset = 18h) [reset = 0h]

ADC Result 12 Register.

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Table 3-1442. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6018h
ADC_R1	502C 8018h

Figure 3-768. ADC_R_RESULTS_ADCRESULT12 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1443. ADC_R_RESULTS_ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 12 16-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field.

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3.14.2.126 ADC_R_RESULTS_ADCRESULT13 Register

3.14.2.126.1 ADC_R_RESULTS_ADCRESULT13 Register (Offset = 1Ah) [reset = 0h]

ADC Result 13 Register.

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Table 3-1444. Instance Table

Instance Name	Physical Address
ADC_R0	502C 601Ah
ADC_R1	502C 801Ah

Figure 3-769. ADC_R_RESULTS_ADCRESULT13 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-1445. ADC_R_RESULTS_ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 13 16-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field.

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3.14.2.127 ADC_R_RESULTS_ADCRESULT14 Register

3.14.2.127.1 ADC_R_RESULTS_ADCRESULT14 Register (Offset = 1Ch) [reset = 0h]

ADC Result 14 Register.

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Table 3-1446. Instance Table

Instance Name	Physical Address
ADC_R0	502C 601Ch
ADC_R1	502C 801Ch

Figure 3-770. ADC_R_RESULTS_ADCRESULT14 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	6	5	4	3	2	1	0
RESULT							
R							
0h							

Table 3-1447. ADC_R_RESULTS_ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 14 16-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field.

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3.14.2.128 ADC_R_RESULTS_ADCRESULT15 Register

3.14.2.128.1 ADC_R_RESULTS_ADCRESULT15 Register (Offset = 1Eh) [reset = 0h]

ADC Result 15 Register.

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Table 3-1448. Instance Table

Instance Name	Physical Address
ADC_R0	502C 601Eh
ADC_R1	502C 801Eh

Figure 3-771. ADC_R_RESULTS_ADCRESULT15 Name Register

15	14	13	12	11	10	9	8
RESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESULT							
R							
0h							

Table 3-1449. ADC_R_RESULTS_ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESULT	R	0h	ADC Result 15 16-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field.

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3.14.2.129 ADC_R_RESULTS_ADCPPB1RESULT Register

3.14.2.129.1 ADC_R_RESULTS_ADCPPB1RESULT Register (Offset = 20h) [reset = 0h]

ADC Post Processing Block 1 Result Register.

Return to Summary Table

Table 3-1450. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6020h
ADC_R1	502C 8020h

Figure 3-772. ADC_R_RESULTS_ADCPPB1RESULT Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							
R							
0h							
15	14	13	12	11	10	9	8
PPBRESULT							
R							
0h							
7	6	5	4	3	2	1	0
PPBRESULT							
R							
0h							

Table 3-1451. ADC_R_RESULTS_ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15:0	PPBRESULT	R	0h	ADC Post Processing Block Result 1 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information]. If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.14.2.130 ADC_R_RESULTS_ADCPPB2RESULT Register

3.14.2.130.1 ADC_R_RESULTS_ADCPPB2RESULT Register (Offset = 24h) [reset = 0h]

ADC Post Processing Block 2 Result Register.

Return to Summary Table

Table 3-1452. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6024h
ADC_R1	502C 8024h

Figure 3-773. ADC_R_RESULTS_ADCPPB2RESULT Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							
R							
0h							
15	14	13	12	11	10	9	8
PPBRESULT							
R							
0h							
7	6	5	4	3	2	1	0
PPBRESULT							
R							
0h							

Table 3-1453. ADC_R_RESULTS_ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15:0	PPBRESULT	R	0h	ADC Post Processing Block Result 2 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information]. If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.14.2.131 ADC_R_RESULTS_ADCPPB3RESULT Register

3.14.2.131.1 ADC_R_RESULTS_ADCPPB3RESULT Register (Offset = 28h) [reset = 0h]

ADC Post Processing Block 3 Result Register.

Return to Summary Table

Table 3-1454. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6028h
ADC_R1	502C 8028h

Figure 3-774. ADC_R_RESULTS_ADCPPB3RESULT Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							
R							
0h							
15	14	13	12	11	10	9	8
PPBRESULT							
R							
0h							
7	6	5	4	3	2	1	0
PPBRESULT							
R							
0h							

Table 3-1455. ADC_R_RESULTS_ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15:0	PPBRESULT	R	0h	ADC Post Processing Block Result 3 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information]. If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.14.2.132 ADC_R_RESULTS_ADCPPB4RESULT Register

3.14.2.132.1 ADC_R_RESULTS_ADCPPB4RESULT Register (Offset = 2Ch) [reset = 0h]

ADC Post Processing Block 4 Result Register.

Return to Summary Table

Table 3-1456. Instance Table

Instance Name	Physical Address
ADC_R0	502C 602Ch
ADC_R1	502C 802Ch

Figure 3-775. ADC_R_RESULTS_ADCPPB4RESULT Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PPBRESULT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PPBRESULT							
R							
0h							

Table 3-1457. ADC_R_RESULTS_ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15:0	PPBRESULT	R	0h	ADC Post Processing Block Result 4 The result of the offset/reference subtraction post conversion processing is stored in this register. This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be availble 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information]. If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register. NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.14.2.133 ADC_R_RESULTS_ADCPPB1SUM Register

3.14.2.133.1 ADC_R_RESULTS_ADCPPB1SUM Register (Offset = 30h) [reset = 0h]

ADC PPB 1 Final Sum Result Register.

Return to Summary Table

Table 3-1458. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6030h
ADC_R1	502C 8030h

Figure 3-776. ADC_R_RESULTS_ADCPPB1SUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SUM							
R							
0h							
15	14	13	12	11	10	9	8
SUM							
R							
0h							
7	6	5	4	3	2	1	0
SUM							
R							
0h							

Table 3-1459. ADC_R_RESULTS_ADCPPB1SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	SUM	R	0h	Post Processing Block 1 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.134 ADC_R_RESULTS_ADCPPB1COUNT Register

3.14.2.134.1 ADC_R_RESULTS_ADCPPB1COUNT Register (Offset = 34h) [reset = 0h]

ADC PPB1 Final Conversion Count Register.

Return to Summary Table

Table 3-1460. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6034h
ADC_R1	502C 8034h

Figure 3-777. ADC_R_RESULTS_ADCPPB1COUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						COUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 3-1461. ADC_R_RESULTS_ADCPPB1COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	COUNT	R	0h	Post Processing Block 1 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.135 ADC_R_RESULTS_ADCPPB2SUM Register

3.14.2.135.1 ADC_R_RESULTS_ADCPPB2SUM Register (Offset = 38h) [reset = 0h]

ADC PPB 2 Final Sum Result Register.

Return to Summary Table

Table 3-1462. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6038h
ADC_R1	502C 8038h

Figure 3-778. ADC_R_RESULTS_ADCPPB2SUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SUM							
R							
0h							
15	14	13	12	11	10	9	8
SUM							
R							
0h							
7	6	5	4	3	2	1	0
SUM							
R							
0h							

Table 3-1463. ADC_R_RESULTS_ADCPPB2SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	SUM	R	0h	Post Processing Block 2 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.136 ADC_R_RESULTS_ADCPPB2COUNT Register

3.14.2.136.1 ADC_R_RESULTS_ADCPPB2COUNT Register (Offset = 3Ch) [reset = 0h]

ADC PPB2 Final Conversion Count Register.

Return to Summary Table

Table 3-1464. Instance Table

Instance Name	Physical Address
ADC_R0	502C 603Ch
ADC_R1	502C 803Ch

Figure 3-779. ADC_R_RESULTS_ADCPPB2COUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						COUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 3-1465. ADC_R_RESULTS_ADCPPB2COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	COUNT	R	0h	Post Processing Block 2 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.137 ADC_R_RESULTS_ADCPPB3SUM Register

3.14.2.137.1 ADC_R_RESULTS_ADCPPB3SUM Register (Offset = 40h) [reset = 0h]

ADC PPB 3 Final Sum Result Register.

Return to Summary Table

Table 3-1466. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6040h
ADC_R1	502C 8040h

Figure 3-780. ADC_R_RESULTS_ADCPPB3SUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SUM							
R							
0h							
15	14	13	12	11	10	9	8
SUM							
R							
0h							
7	6	5	4	3	2	1	0
SUM							
R							
0h							

Table 3-1467. ADC_R_RESULTS_ADCPPB3SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	SUM	R	0h	Post Processing Block 3 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.138 ADC_R_RESULTS_ADCPPB3COUNT Register

3.14.2.138.1 ADC_R_RESULTS_ADCPPB3COUNT Register (Offset = 44h) [reset = 0h]

ADC PPB3 Final Conversion Count Register.

Return to Summary Table

Table 3-1468. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6044h
ADC_R1	502C 8044h

Figure 3-781. ADC_R_RESULTS_ADCPPB3COUNT Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED_1</td><td colspan="2">COUNT</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">COUNT</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 3-1469. ADC_R_RESULTS_ADCPPB3COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	COUNT	R	0h	Post Processing Block 3 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.139 ADC_R_RESULTS_ADCPPB4SUM Register

3.14.2.139.1 ADC_R_RESULTS_ADCPPB4SUM Register (Offset = 48h) [reset = 0h]

ADC PPB 4 Final Sum Result Register.

Return to Summary Table

Table 3-1470. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6048h
ADC_R1	502C 8048h

Figure 3-782. ADC_R_RESULTS_ADCPPB4SUM Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SUM							
R							
0h							
15	14	13	12	11	10	9	8
SUM							
R							
0h							
7	6	5	4	3	2	1	0
SUM							
R							
0h							

Table 3-1471. ADC_R_RESULTS_ADCPPB4SUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 23.
23:0	SUM	R	0h	Post Processing Block 4 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion. The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.14.2.140 ADC_R_RESULTS_ADCPPB4COUNT Register

3.14.2.140.1 ADC_R_RESULTS_ADCPPB4COUNT Register (Offset = 4Ch) [reset = 0h]

ADC PPB4 Final Conversion Count Register.

Return to Summary Table

Table 3-1472. Instance Table

Instance Name	Physical Address
ADC_R0	502C 604Ch
ADC_R1	502C 804Ch

Figure 3-783. ADC_R_RESULTS_ADCPPB4COUNT Name Register

15	14	13	12	11	10	9	8
RESERVED_1						COUNT	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R							
0h							

Table 3-1473. ADC_R_RESULTS_ADCPPB4COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	COUNT	R	0h	Post Processing Block 4 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.14.2.141 ADC_R_RESULTS_ADCPPB1MAX Register

3.14.2.141.1 ADC_R_RESULTS_ADCPPB1MAX Register (Offset = 50h) [reset = 0h]

ADC PPB 1 Final Max Result Register.

Return to Summary Table

Table 3-1474. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6050h
ADC_R1	502C 8050h

Figure 3-784. ADC_R_RESULTS_ADCPPB1MAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MAX
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAX							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX							
R							
0h							

Table 3-1475. ADC_R_RESULTS_ADCPPB1MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MAX	R	0h	Post Processing Block 1 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.142 ADC_R_RESULTS_ADCPPB1MAXI Register

3.14.2.142.1 ADC_R_RESULTS_ADCPPB1MAXI Register (Offset = 54h) [reset = 0h]

ADC PPB 1 Final Max Index Result Register.

Return to Summary Table

Table 3-1476. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6054h
ADC_R1	502C 8054h

Figure 3-785. ADC_R_RESULTS_ADCPPB1MAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAXI							
R							
0h							

Table 3-1477. ADC_R_RESULTS_ADCPPB1MAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MAXI	R	0h	Post Processing Block 1 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMAXI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.143 ADC_R_RESULTS_ADCPPB1MIN Register

3.14.2.143.1 ADC_R_RESULTS_ADCPPB1MIN Register (Offset = 58h) [reset = 0h]

ADC PPB 1 Final Min Result Register.

Return to Summary Table

Table 3-1478. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6058h
ADC_R1	502C 8058h

Figure 3-786. ADC_R_RESULTS_ADCPPB1MIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MIN							
R							
0h							

Table 3-1479. ADC_R_RESULTS_ADCPPB1MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MIN	R	0h	Post Processing Block 1 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.144 ADC_R_RESULTS_ADCPPB1MINI Register

3.14.2.144.1 ADC_R_RESULTS_ADCPPB1MINI Register (Offset = 5Ch) [reset = 0h]

ADC PPB 1 Final Min Index Result Register.

Return to Summary Table

Table 3-1480. Instance Table

Instance Name	Physical Address
ADC_R0	502C 605Ch
ADC_R1	502C 805Ch

Figure 3-787. ADC_R_RESULTS_ADCPPB1MINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MINI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MINI							
R							
0h							

Table 3-1481. ADC_R_RESULTS_ADCPPB1MINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MINI	R	0h	Post Processing Block 1 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information].

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3.14.2.145 ADC_R_RESULTS_ADCPPB2MAX Register

3.14.2.145.1 ADC_R_RESULTS_ADCPPB2MAX Register (Offset = 60h) [reset = 0h]

ADC PPB 2 Final Max Result Register.

Return to Summary Table

Table 3-1482. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6060h
ADC_R1	502C 8060h

Figure 3-788. ADC_R_RESULTS_ADCPPB2MAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							MAX
R							R
0h							0h
15	14	13	12	11	10	9	8
MAX							
R							
0h							
7	6	5	4	3	2	1	0
MAX							
R							
0h							

Table 3-1483. ADC_R_RESULTS_ADCPPB2MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MAX	R	0h	Post Processing Block 2 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.146 ADC_R_RESULTS_ADCPPB2MAXI Register

3.14.2.146.1 ADC_R_RESULTS_ADCPPB2MAXI Register (Offset = 64h) [reset = 0h]

ADC PPB 2 Final Max Index Result Register.

Return to Summary Table

Table 3-1484. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6064h
ADC_R1	502C 8064h

Figure 3-789. ADC_R_RESULTS_ADCPPB2MAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MAXI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
MAXI							
R							
0h							

Table 3-1485. ADC_R_RESULTS_ADCPPB2MAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MAXI	R	0h	Post Processing Block 2 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMAXI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.147 ADC_R_RESULTS_ADCPPB2MIN Register

3.14.2.147.1 ADC_R_RESULTS_ADCPPB2MIN Register (Offset = 68h) [reset = 0h]

ADC PPB 2 Final Min Result Register.

Return to Summary Table

Table 3-1486. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6068h
ADC_R1	502C 8068h

Figure 3-790. ADC_R_RESULTS_ADCPPB2MIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MIN							
R							
0h							

Table 3-1487. ADC_R_RESULTS_ADCPPB2MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MIN	R	0h	Post Processing Block 2 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.148 ADC_R_RESULTS_ADCPPB2MINI Register

3.14.2.148.1 ADC_R_RESULTS_ADCPPB2MINI Register (Offset = 6Ch) [reset = 0h]

ADC PPB 2 Final Min Index Result Register.

Return to Summary Table

Table 3-1488. Instance Table

Instance Name	Physical Address
ADC_R0	502C 606Ch
ADC_R1	502C 806Ch

Figure 3-791. ADC_R_RESULTS_ADCPPB2MINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MINI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MINI							
R							
0h							

Table 3-1489. ADC_R_RESULTS_ADCPPB2MINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MINI	R	0h	Post Processing Block 2 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information].

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3.14.2.149 ADC_R_RESULTS_ADCPPB3MAX Register

3.14.2.149.1 ADC_R_RESULTS_ADCPPB3MAX Register (Offset = 70h) [reset = 0h]

ADC PPB 3 Final Max Result Register.

Return to Summary Table

Table 3-1490. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6070h
ADC_R1	502C 8070h

Figure 3-792. ADC_R_RESULTS_ADCPPB3MAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MAX
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAX							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX							
R							
0h							

Table 3-1491. ADC_R_RESULTS_ADCPPB3MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MAX	R	0h	Post Processing Block 3 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.150 ADC_R_RESULTS_ADCPPB3MAXI Register

3.14.2.150.1 ADC_R_RESULTS_ADCPPB3MAXI Register (Offset = 74h) [reset = 0h]

ADC PPB 3 Final Max Index Result Register.

Return to Summary Table

Table 3-1492. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6074h
ADC_R1	502C 8074h

Figure 3-793. ADC_R_RESULTS_ADCPPB3MAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAXI							
R							
0h							

Table 3-1493. ADC_R_RESULTS_ADCPPB3MAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MAXI	R	0h	Post Processing Block 3 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMAXI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.151 ADC_R_RESULTS_ADCPPB3MIN Register

3.14.2.151.1 ADC_R_RESULTS_ADCPPB3MIN Register (Offset = 78h) [reset = 0h]

ADC PPB 3 Final Min Result Register.

Return to Summary Table

Table 3-1494. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6078h
ADC_R1	502C 8078h

Figure 3-794. ADC_R_RESULTS_ADCPPB3MIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MIN
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MIN							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MIN							
R							
0h							

Table 3-1495. ADC_R_RESULTS_ADCPPB3MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MIN	R	0h	Post Processing Block 3 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.152 ADC_R_RESULTS_ADCPPB3MINI Register

3.14.2.152.1 ADC_R_RESULTS_ADCPPB3MINI Register (Offset = 7Ch) [reset = 0h]

ADC PPB 3 Final Min Index Result Register.

Return to Summary Table

Table 3-1496. Instance Table

Instance Name	Physical Address
ADC_R0	502C 607Ch
ADC_R1	502C 807Ch

Figure 3-795. ADC_R_RESULTS_ADCPPB3MINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MINI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
MINI							
R							
0h							

Table 3-1497. ADC_R_RESULTS_ADCPPB3MINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MINI	R	0h	Post Processing Block 3 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].

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3.14.2.153 ADC_R_RESULTS_ADCPPB4MAX Register

3.14.2.153.1 ADC_R_RESULTS_ADCPPB4MAX Register (Offset = 80h) [reset = 0h]

ADC PPB 4 Final Max Result Register.

Return to Summary Table

Table 3-1498. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6080h
ADC_R1	502C 8080h

Figure 3-796. ADC_R_RESULTS_ADCPPB4MAX Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SIGN							MAX
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAX							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAX							
R							
0h							

Table 3-1499. ADC_R_RESULTS_ADCPPB4MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MAX	R	0h	Post Processing Block 4 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.14.2.154 ADC_R_RESULTS_ADCPPB4MAXI Register

3.14.2.154.1 ADC_R_RESULTS_ADCPPB4MAXI Register (Offset = 84h) [reset = 0h]

ADC PPB 4 Final Max Index Result Register.

Return to Summary Table

Table 3-1500. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6084h
ADC_R1	502C 8084h

Figure 3-797. ADC_R_RESULTS_ADCPPB4MAXI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MAXI	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MAXI							
R							
0h							

Table 3-1501. ADC_R_RESULTS_ADCPPB4MAXI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MAXI	R	0h	Post Processing Block 4 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMAXI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.14.2.155 ADC_R_RESULTS_ADCPPB4MIN Register

3.14.2.155.1 ADC_R_RESULTS_ADCPPB4MIN Register (Offset = 88h) [reset = 0h]

ADC PPB 4 Final Min Result Register.

Return to Summary Table

Table 3-1502. Instance Table

Instance Name	Physical Address
ADC_R0	502C 6088h
ADC_R1	502C 8088h

Figure 3-798. ADC_R_RESULTS_ADCPPB4MIN Name Register

31	30	29	28	27	26	25	24
SIGN							
R							
0h							
23	22	21	20	19	18	17	16
SIGN							MIN
R							R
0h							0h
15	14	13	12	11	10	9	8
MIN							
R							
0h							
7	6	5	4	3	2	1	0
MIN							
R							
0h							

Table 3-1503. ADC_R_RESULTS_ADCPPB4MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16.
16:0	MIN	R	0h	Post Processing Block 4 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.14.2.156 ADC_R_RESULTS_ADCPPB4MINI Register

3.14.2.156.1 ADC_R_RESULTS_ADCPPB4MINI Register (Offset = 8Ch) [reset = 0h]

ADC PPB 4 Final Min Index Result Register.

Return to Summary Table

Table 3-1504. Instance Table

Instance Name	Physical Address
ADC_R0	502C 608Ch
ADC_R1	502C 808Ch

Figure 3-799. ADC_R_RESULTS_ADCPPB4MINI Name Register

15	14	13	12	11	10	9	8
RESERVED_1						MINI	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
MINI							
R							
0h							

Table 3-1505. ADC_R_RESULTS_ADCPPB4MINI Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	MINI	R	0h	Post Processing Block 4 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information].

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3.15 CONTROLSS_PWMXBAR

CONTROLSS_PWMXBAR

3.15.1 CONTROLSS_PWMXBAR Summaries

CONTROLSS_PWMXBAR Summaries

Table 3-1506. CONTROLSS Registers, Base Address=502D 1000h, Length=4096

Offset	Length	Register Name	CONTROLSS_PWMXBAR Physical Address
10h	32	CONTROLSS_PWMXBAR_STATUS	502D 1010h
14h	32	CONTROLSS_PWMXBAR_FLAGINVERT	502D 1014h
18h	32	CONTROLSS_PWMXBAR_FLAG	502D 1018h
1Ch	32	CONTROLSS_PWMXBAR_FLAG_CLR	502D 101Ch
100h	32	CONTROLSS_PWMXBAR0_G0	502D 1100h
104h	32	CONTROLSS_PWMXBAR0_G1	502D 1104h
108h	32	CONTROLSS_PWMXBAR0_G2	502D 1108h
10Ch	32	CONTROLSS_PWMXBAR0_G3	502D 110Ch
110h	32	CONTROLSS_PWMXBAR0_G4	502D 1110h
114h	32	CONTROLSS_PWMXBAR0_G5	502D 1114h
118h	32	CONTROLSS_PWMXBAR0_G6	502D 1118h
11Ch	32	CONTROLSS_PWMXBAR0_G7	502D 111Ch
120h	32	CONTROLSS_PWMXBAR0_G8	502D 1120h
124h	32	CONTROLSS_PWMXBAR0_G9	502D 1124h
140h	32	CONTROLSS_PWMXBAR1_G0	502D 1140h
144h	32	CONTROLSS_PWMXBAR1_G1	502D 1144h
148h	32	CONTROLSS_PWMXBAR1_G2	502D 1148h
14Ch	32	CONTROLSS_PWMXBAR1_G3	502D 114Ch
150h	32	CONTROLSS_PWMXBAR1_G4	502D 1150h
154h	32	CONTROLSS_PWMXBAR1_G5	502D 1154h
158h	32	CONTROLSS_PWMXBAR1_G6	502D 1158h
15Ch	32	CONTROLSS_PWMXBAR1_G7	502D 115Ch
160h	32	CONTROLSS_PWMXBAR1_G8	502D 1160h
164h	32	CONTROLSS_PWMXBAR1_G9	502D 1164h
180h	32	CONTROLSS_PWMXBAR2_G0	502D 1180h
184h	32	CONTROLSS_PWMXBAR2_G1	502D 1184h
188h	32	CONTROLSS_PWMXBAR2_G2	502D 1188h
18Ch	32	CONTROLSS_PWMXBAR2_G3	502D 118Ch
190h	32	CONTROLSS_PWMXBAR2_G4	502D 1190h
194h	32	CONTROLSS_PWMXBAR2_G5	502D 1194h
198h	32	CONTROLSS_PWMXBAR2_G6	502D 1198h
19Ch	32	CONTROLSS_PWMXBAR2_G7	502D 119Ch
1A0h	32	CONTROLSS_PWMXBAR2_G8	502D 11A0h
1A4h	32	CONTROLSS_PWMXBAR2_G9	502D 11A4h
1C0h	32	CONTROLSS_PWMXBAR3_G0	502D 11C0h
1C4h	32	CONTROLSS_PWMXBAR3_G1	502D 11C4h
1C8h	32	CONTROLSS_PWMXBAR3_G2	502D 11C8h
1CCh	32	CONTROLSS_PWMXBAR3_G3	502D 11CCh
1D0h	32	CONTROLSS_PWMXBAR3_G4	502D 11D0h

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Table 3-1506. CONTROLSS Registers, Base Address=502D 1000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_PWMXBAR Physical Address
1D4h	32	CONTROLSS_PWMXBAR3_G5	502D 11D4h
1D8h	32	CONTROLSS_PWMXBAR3_G6	502D 11D8h
1DCh	32	CONTROLSS_PWMXBAR3_G7	502D 11DCh
1E0h	32	CONTROLSS_PWMXBAR3_G8	502D 11E0h
1E4h	32	CONTROLSS_PWMXBAR3_G9	502D 11E4h
200h	32	CONTROLSS_PWMXBAR4_G0	502D 1200h
204h	32	CONTROLSS_PWMXBAR4_G1	502D 1204h
208h	32	CONTROLSS_PWMXBAR4_G2	502D 1208h
20Ch	32	CONTROLSS_PWMXBAR4_G3	502D 120Ch
210h	32	CONTROLSS_PWMXBAR4_G4	502D 1210h
214h	32	CONTROLSS_PWMXBAR4_G5	502D 1214h
218h	32	CONTROLSS_PWMXBAR4_G6	502D 1218h
21Ch	32	CONTROLSS_PWMXBAR4_G7	502D 121Ch
220h	32	CONTROLSS_PWMXBAR4_G8	502D 1220h
224h	32	CONTROLSS_PWMXBAR4_G9	502D 1224h
240h	32	CONTROLSS_PWMXBAR5_G0	502D 1240h
244h	32	CONTROLSS_PWMXBAR5_G1	502D 1244h
248h	32	CONTROLSS_PWMXBAR5_G2	502D 1248h
24Ch	32	CONTROLSS_PWMXBAR5_G3	502D 124Ch
250h	32	CONTROLSS_PWMXBAR5_G4	502D 1250h
254h	32	CONTROLSS_PWMXBAR5_G5	502D 1254h
258h	32	CONTROLSS_PWMXBAR5_G6	502D 1258h
25Ch	32	CONTROLSS_PWMXBAR5_G7	502D 125Ch
260h	32	CONTROLSS_PWMXBAR5_G8	502D 1260h
264h	32	CONTROLSS_PWMXBAR5_G9	502D 1264h
280h	32	CONTROLSS_PWMXBAR6_G0	502D 1280h
284h	32	CONTROLSS_PWMXBAR6_G1	502D 1284h
288h	32	CONTROLSS_PWMXBAR6_G2	502D 1288h
28Ch	32	CONTROLSS_PWMXBAR6_G3	502D 128Ch
290h	32	CONTROLSS_PWMXBAR6_G4	502D 1290h
294h	32	CONTROLSS_PWMXBAR6_G5	502D 1294h
298h	32	CONTROLSS_PWMXBAR6_G6	502D 1298h
29Ch	32	CONTROLSS_PWMXBAR6_G7	502D 129Ch
2A0h	32	CONTROLSS_PWMXBAR6_G8	502D 12A0h
2A4h	32	CONTROLSS_PWMXBAR6_G9	502D 12A4h
2C0h	32	CONTROLSS_PWMXBAR7_G0	502D 12C0h
2C4h	32	CONTROLSS_PWMXBAR7_G1	502D 12C4h
2C8h	32	CONTROLSS_PWMXBAR7_G2	502D 12C8h
2CCh	32	CONTROLSS_PWMXBAR7_G3	502D 12CCh
2D0h	32	CONTROLSS_PWMXBAR7_G4	502D 12D0h
2D4h	32	CONTROLSS_PWMXBAR7_G5	502D 12D4h
2D8h	32	CONTROLSS_PWMXBAR7_G6	502D 12D8h
2DCh	32	CONTROLSS_PWMXBAR7_G7	502D 12DCh
2E0h	32	CONTROLSS_PWMXBAR7_G8	502D 12E0h
2E4h	32	CONTROLSS_PWMXBAR7_G9	502D 12E4h
300h	32	CONTROLSS_PWMXBAR8_G0	502D 1300h

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Table 3-1506. CONTROLSS Registers, Base Address=502D 1000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_PWMXBAR Physical Address
304h	32	CONTROLSS_PWMXBAR8_G1	502D 1304h
308h	32	CONTROLSS_PWMXBAR8_G2	502D 1308h
30Ch	32	CONTROLSS_PWMXBAR8_G3	502D 130Ch
310h	32	CONTROLSS_PWMXBAR8_G4	502D 1310h
314h	32	CONTROLSS_PWMXBAR8_G5	502D 1314h
318h	32	CONTROLSS_PWMXBAR8_G6	502D 1318h
31Ch	32	CONTROLSS_PWMXBAR8_G7	502D 131Ch
320h	32	CONTROLSS_PWMXBAR8_G8	502D 1320h
324h	32	CONTROLSS_PWMXBAR8_G9	502D 1324h
340h	32	CONTROLSS_PWMXBAR9_G0	502D 1340h
344h	32	CONTROLSS_PWMXBAR9_G1	502D 1344h
348h	32	CONTROLSS_PWMXBAR9_G2	502D 1348h
34Ch	32	CONTROLSS_PWMXBAR9_G3	502D 134Ch
350h	32	CONTROLSS_PWMXBAR9_G4	502D 1350h
354h	32	CONTROLSS_PWMXBAR9_G5	502D 1354h
358h	32	CONTROLSS_PWMXBAR9_G6	502D 1358h
35Ch	32	CONTROLSS_PWMXBAR9_G7	502D 135Ch
360h	32	CONTROLSS_PWMXBAR9_G8	502D 1360h
364h	32	CONTROLSS_PWMXBAR9_G9	502D 1364h
380h	32	CONTROLSS_PWMXBAR10_G0	502D 1380h
384h	32	CONTROLSS_PWMXBAR10_G1	502D 1384h
388h	32	CONTROLSS_PWMXBAR10_G2	502D 1388h
38Ch	32	CONTROLSS_PWMXBAR10_G3	502D 138Ch
390h	32	CONTROLSS_PWMXBAR10_G4	502D 1390h
394h	32	CONTROLSS_PWMXBAR10_G5	502D 1394h
398h	32	CONTROLSS_PWMXBAR10_G6	502D 1398h
39Ch	32	CONTROLSS_PWMXBAR10_G7	502D 139Ch
3A0h	32	CONTROLSS_PWMXBAR10_G8	502D 13A0h
3A4h	32	CONTROLSS_PWMXBAR10_G9	502D 13A4h
3C0h	32	CONTROLSS_PWMXBAR11_G0	502D 13C0h
3C4h	32	CONTROLSS_PWMXBAR11_G1	502D 13C4h
3C8h	32	CONTROLSS_PWMXBAR11_G2	502D 13C8h
3CCh	32	CONTROLSS_PWMXBAR11_G3	502D 13CCh
3D0h	32	CONTROLSS_PWMXBAR11_G4	502D 13D0h
3D4h	32	CONTROLSS_PWMXBAR11_G5	502D 13D4h
3D8h	32	CONTROLSS_PWMXBAR11_G6	502D 13D8h
3DCh	32	CONTROLSS_PWMXBAR11_G7	502D 13DCh
3E0h	32	CONTROLSS_PWMXBAR11_G8	502D 13E0h
3E4h	32	CONTROLSS_PWMXBAR11_G9	502D 13E4h
400h	32	CONTROLSS_PWMXBAR12_G0	502D 1400h
404h	32	CONTROLSS_PWMXBAR12_G1	502D 1404h
408h	32	CONTROLSS_PWMXBAR12_G2	502D 1408h
40Ch	32	CONTROLSS_PWMXBAR12_G3	502D 140Ch
410h	32	CONTROLSS_PWMXBAR12_G4	502D 1410h
414h	32	CONTROLSS_PWMXBAR12_G5	502D 1414h
418h	32	CONTROLSS_PWMXBAR12_G6	502D 1418h

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Table 3-1506. CONTROLSS Registers, Base Address=502D 1000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_PWMXBAR Physical Address
41Ch	32	CONTROLSS_PWMXBAR12_G7	502D 141Ch
420h	32	CONTROLSS_PWMXBAR12_G8	502D 1420h
424h	32	CONTROLSS_PWMXBAR12_G9	502D 1424h
440h	32	CONTROLSS_PWMXBAR13_G0	502D 1440h
444h	32	CONTROLSS_PWMXBAR13_G1	502D 1444h
448h	32	CONTROLSS_PWMXBAR13_G2	502D 1448h
44Ch	32	CONTROLSS_PWMXBAR13_G3	502D 144Ch
450h	32	CONTROLSS_PWMXBAR13_G4	502D 1450h
454h	32	CONTROLSS_PWMXBAR13_G5	502D 1454h
458h	32	CONTROLSS_PWMXBAR13_G6	502D 1458h
45Ch	32	CONTROLSS_PWMXBAR13_G7	502D 145Ch
460h	32	CONTROLSS_PWMXBAR13_G8	502D 1460h
464h	32	CONTROLSS_PWMXBAR13_G9	502D 1464h
480h	32	CONTROLSS_PWMXBAR14_G0	502D 1480h
484h	32	CONTROLSS_PWMXBAR14_G1	502D 1484h
488h	32	CONTROLSS_PWMXBAR14_G2	502D 1488h
48Ch	32	CONTROLSS_PWMXBAR14_G3	502D 148Ch
490h	32	CONTROLSS_PWMXBAR14_G4	502D 1490h
494h	32	CONTROLSS_PWMXBAR14_G5	502D 1494h
498h	32	CONTROLSS_PWMXBAR14_G6	502D 1498h
49Ch	32	CONTROLSS_PWMXBAR14_G7	502D 149Ch
4A0h	32	CONTROLSS_PWMXBAR14_G8	502D 14A0h
4A4h	32	CONTROLSS_PWMXBAR14_G9	502D 14A4h
4C0h	32	CONTROLSS_PWMXBAR15_G0	502D 14C0h
4C4h	32	CONTROLSS_PWMXBAR15_G1	502D 14C4h
4C8h	32	CONTROLSS_PWMXBAR15_G2	502D 14C8h
4CCh	32	CONTROLSS_PWMXBAR15_G3	502D 14CCh
4D0h	32	CONTROLSS_PWMXBAR15_G4	502D 14D0h
4D4h	32	CONTROLSS_PWMXBAR15_G5	502D 14D4h
4D8h	32	CONTROLSS_PWMXBAR15_G6	502D 14D8h
4DCh	32	CONTROLSS_PWMXBAR15_G7	502D 14DCh
4E0h	32	CONTROLSS_PWMXBAR15_G8	502D 14E0h
4E4h	32	CONTROLSS_PWMXBAR15_G9	502D 14E4h
500h	32	CONTROLSS_PWMXBAR16_G0	502D 1500h
504h	32	CONTROLSS_PWMXBAR16_G1	502D 1504h
508h	32	CONTROLSS_PWMXBAR16_G2	502D 1508h
50Ch	32	CONTROLSS_PWMXBAR16_G3	502D 150Ch
510h	32	CONTROLSS_PWMXBAR16_G4	502D 1510h
514h	32	CONTROLSS_PWMXBAR16_G5	502D 1514h
518h	32	CONTROLSS_PWMXBAR16_G6	502D 1518h
51Ch	32	CONTROLSS_PWMXBAR16_G7	502D 151Ch
520h	32	CONTROLSS_PWMXBAR16_G8	502D 1520h
524h	32	CONTROLSS_PWMXBAR16_G9	502D 1524h
540h	32	CONTROLSS_PWMXBAR17_G0	502D 1540h
544h	32	CONTROLSS_PWMXBAR17_G1	502D 1544h
548h	32	CONTROLSS_PWMXBAR17_G2	502D 1548h

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Table 3-1506. CONTROLSS Registers, Base Address=502D 1000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_PWMXBAR Physical Address
54Ch	32	CONTROLSS_PWMXBAR17_G3	502D 154Ch
550h	32	CONTROLSS_PWMXBAR17_G4	502D 1550h
554h	32	CONTROLSS_PWMXBAR17_G5	502D 1554h
558h	32	CONTROLSS_PWMXBAR17_G6	502D 1558h
55Ch	32	CONTROLSS_PWMXBAR17_G7	502D 155Ch
560h	32	CONTROLSS_PWMXBAR17_G8	502D 1560h
564h	32	CONTROLSS_PWMXBAR17_G9	502D 1564h
580h	32	CONTROLSS_PWMXBAR18_G0	502D 1580h
584h	32	CONTROLSS_PWMXBAR18_G1	502D 1584h
588h	32	CONTROLSS_PWMXBAR18_G2	502D 1588h
58Ch	32	CONTROLSS_PWMXBAR18_G3	502D 158Ch
590h	32	CONTROLSS_PWMXBAR18_G4	502D 1590h
594h	32	CONTROLSS_PWMXBAR18_G5	502D 1594h
598h	32	CONTROLSS_PWMXBAR18_G6	502D 1598h
59Ch	32	CONTROLSS_PWMXBAR18_G7	502D 159Ch
5A0h	32	CONTROLSS_PWMXBAR18_G8	502D 15A0h
5A4h	32	CONTROLSS_PWMXBAR18_G9	502D 15A4h
5C0h	32	CONTROLSS_PWMXBAR19_G0	502D 15C0h
5C4h	32	CONTROLSS_PWMXBAR19_G1	502D 15C4h
5C8h	32	CONTROLSS_PWMXBAR19_G2	502D 15C8h
5CCh	32	CONTROLSS_PWMXBAR19_G3	502D 15CCh
5D0h	32	CONTROLSS_PWMXBAR19_G4	502D 15D0h
5D4h	32	CONTROLSS_PWMXBAR19_G5	502D 15D4h
5D8h	32	CONTROLSS_PWMXBAR19_G6	502D 15D8h
5DCh	32	CONTROLSS_PWMXBAR19_G7	502D 15DCh
5E0h	32	CONTROLSS_PWMXBAR19_G8	502D 15E0h
5E4h	32	CONTROLSS_PWMXBAR19_G9	502D 15E4h
600h	32	CONTROLSS_PWMXBAR20_G0	502D 1600h
604h	32	CONTROLSS_PWMXBAR20_G1	502D 1604h
608h	32	CONTROLSS_PWMXBAR20_G2	502D 1608h
60Ch	32	CONTROLSS_PWMXBAR20_G3	502D 160Ch
610h	32	CONTROLSS_PWMXBAR20_G4	502D 1610h
614h	32	CONTROLSS_PWMXBAR20_G5	502D 1614h
618h	32	CONTROLSS_PWMXBAR20_G6	502D 1618h
61Ch	32	CONTROLSS_PWMXBAR20_G7	502D 161Ch
620h	32	CONTROLSS_PWMXBAR20_G8	502D 1620h
624h	32	CONTROLSS_PWMXBAR20_G9	502D 1624h
640h	32	CONTROLSS_PWMXBAR21_G0	502D 1640h
644h	32	CONTROLSS_PWMXBAR21_G1	502D 1644h
648h	32	CONTROLSS_PWMXBAR21_G2	502D 1648h
64Ch	32	CONTROLSS_PWMXBAR21_G3	502D 164Ch
650h	32	CONTROLSS_PWMXBAR21_G4	502D 1650h
654h	32	CONTROLSS_PWMXBAR21_G5	502D 1654h
658h	32	CONTROLSS_PWMXBAR21_G6	502D 1658h
65Ch	32	CONTROLSS_PWMXBAR21_G7	502D 165Ch
660h	32	CONTROLSS_PWMXBAR21_G8	502D 1660h

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Table 3-1506. CONTROLSS Registers, Base Address=502D 1000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_PWMXBAR Physical Address
664h	32	CONTROLSS_PWMXBAR21_G9	502D 1664h
680h	32	CONTROLSS_PWMXBAR22_G0	502D 1680h
684h	32	CONTROLSS_PWMXBAR22_G1	502D 1684h
688h	32	CONTROLSS_PWMXBAR22_G2	502D 1688h
68Ch	32	CONTROLSS_PWMXBAR22_G3	502D 168Ch
690h	32	CONTROLSS_PWMXBAR22_G4	502D 1690h
694h	32	CONTROLSS_PWMXBAR22_G5	502D 1694h
698h	32	CONTROLSS_PWMXBAR22_G6	502D 1698h
69Ch	32	CONTROLSS_PWMXBAR22_G7	502D 169Ch
6A0h	32	CONTROLSS_PWMXBAR22_G8	502D 16A0h
6A4h	32	CONTROLSS_PWMXBAR22_G9	502D 16A4h
6C0h	32	CONTROLSS_PWMXBAR23_G0	502D 16C0h
6C4h	32	CONTROLSS_PWMXBAR23_G1	502D 16C4h
6C8h	32	CONTROLSS_PWMXBAR23_G2	502D 16C8h
6CCh	32	CONTROLSS_PWMXBAR23_G3	502D 16CCh
6D0h	32	CONTROLSS_PWMXBAR23_G4	502D 16D0h
6D4h	32	CONTROLSS_PWMXBAR23_G5	502D 16D4h
6D8h	32	CONTROLSS_PWMXBAR23_G6	502D 16D8h
6DCh	32	CONTROLSS_PWMXBAR23_G7	502D 16DCh
6E0h	32	CONTROLSS_PWMXBAR23_G8	502D 16E0h
6E4h	32	CONTROLSS_PWMXBAR23_G9	502D 16E4h
700h	32	CONTROLSS_PWMXBAR24_G0	502D 1700h
704h	32	CONTROLSS_PWMXBAR24_G1	502D 1704h
708h	32	CONTROLSS_PWMXBAR24_G2	502D 1708h
70Ch	32	CONTROLSS_PWMXBAR24_G3	502D 170Ch
710h	32	CONTROLSS_PWMXBAR24_G4	502D 1710h
714h	32	CONTROLSS_PWMXBAR24_G5	502D 1714h
718h	32	CONTROLSS_PWMXBAR24_G6	502D 1718h
71Ch	32	CONTROLSS_PWMXBAR24_G7	502D 171Ch
720h	32	CONTROLSS_PWMXBAR24_G8	502D 1720h
724h	32	CONTROLSS_PWMXBAR24_G9	502D 1724h
740h	32	CONTROLSS_PWMXBAR25_G0	502D 1740h
744h	32	CONTROLSS_PWMXBAR25_G1	502D 1744h
748h	32	CONTROLSS_PWMXBAR25_G2	502D 1748h
74Ch	32	CONTROLSS_PWMXBAR25_G3	502D 174Ch
750h	32	CONTROLSS_PWMXBAR25_G4	502D 1750h
754h	32	CONTROLSS_PWMXBAR25_G5	502D 1754h
758h	32	CONTROLSS_PWMXBAR25_G6	502D 1758h
75Ch	32	CONTROLSS_PWMXBAR25_G7	502D 175Ch
760h	32	CONTROLSS_PWMXBAR25_G8	502D 1760h
764h	32	CONTROLSS_PWMXBAR25_G9	502D 1764h
780h	32	CONTROLSS_PWMXBAR26_G0	502D 1780h
784h	32	CONTROLSS_PWMXBAR26_G1	502D 1784h
788h	32	CONTROLSS_PWMXBAR26_G2	502D 1788h
78Ch	32	CONTROLSS_PWMXBAR26_G3	502D 178Ch
790h	32	CONTROLSS_PWMXBAR26_G4	502D 1790h

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Table 3-1506. CONTROLSS Registers, Base Address=502D 1000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_PWMXBAR Physical Address
794h	32	CONTROLSS_PWMXBAR26_G5	502D 1794h
798h	32	CONTROLSS_PWMXBAR26_G6	502D 1798h
79Ch	32	CONTROLSS_PWMXBAR26_G7	502D 179Ch
7A0h	32	CONTROLSS_PWMXBAR26_G8	502D 17A0h
7A4h	32	CONTROLSS_PWMXBAR26_G9	502D 17A4h
7C0h	32	CONTROLSS_PWMXBAR27_G0	502D 17C0h
7C4h	32	CONTROLSS_PWMXBAR27_G1	502D 17C4h
7C8h	32	CONTROLSS_PWMXBAR27_G2	502D 17C8h
7CCh	32	CONTROLSS_PWMXBAR27_G3	502D 17CCh
7D0h	32	CONTROLSS_PWMXBAR27_G4	502D 17D0h
7D4h	32	CONTROLSS_PWMXBAR27_G5	502D 17D4h
7D8h	32	CONTROLSS_PWMXBAR27_G6	502D 17D8h
7DCh	32	CONTROLSS_PWMXBAR27_G7	502D 17DCh
7E0h	32	CONTROLSS_PWMXBAR27_G8	502D 17E0h
7E4h	32	CONTROLSS_PWMXBAR27_G9	502D 17E4h
800h	32	CONTROLSS_PWMXBAR28_G0	502D 1800h
804h	32	CONTROLSS_PWMXBAR28_G1	502D 1804h
808h	32	CONTROLSS_PWMXBAR28_G2	502D 1808h
80Ch	32	CONTROLSS_PWMXBAR28_G3	502D 180Ch
810h	32	CONTROLSS_PWMXBAR28_G4	502D 1810h
814h	32	CONTROLSS_PWMXBAR28_G5	502D 1814h
818h	32	CONTROLSS_PWMXBAR28_G6	502D 1818h
81Ch	32	CONTROLSS_PWMXBAR28_G7	502D 181Ch
820h	32	CONTROLSS_PWMXBAR28_G8	502D 1820h
824h	32	CONTROLSS_PWMXBAR28_G9	502D 1824h
840h	32	CONTROLSS_PWMXBAR29_G0	502D 1840h
844h	32	CONTROLSS_PWMXBAR29_G1	502D 1844h
848h	32	CONTROLSS_PWMXBAR29_G2	502D 1848h
84Ch	32	CONTROLSS_PWMXBAR29_G3	502D 184Ch
850h	32	CONTROLSS_PWMXBAR29_G4	502D 1850h
854h	32	CONTROLSS_PWMXBAR29_G5	502D 1854h
858h	32	CONTROLSS_PWMXBAR29_G6	502D 1858h
85Ch	32	CONTROLSS_PWMXBAR29_G7	502D 185Ch
860h	32	CONTROLSS_PWMXBAR29_G8	502D 1860h
864h	32	CONTROLSS_PWMXBAR29_G9	502D 1864h

3.15.2 CONTROLSS_PWMXBAR Registers

CONTROLSS_PWMXBAR Registers

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3.15.2.1 CONTROLSS_PWMXBAR_STATUS Register

3.15.2.1.1 CONTROLSS_PWMXBAR_STATUS Register (Offset = 10h) [reset = 0h]

Output Signal Status.

Return to Summary Table

Table 3-1507. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1010h

Figure 3-800. CONTROLSS_PWMXBAR_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED		PWMXBAR_STATUS_STS					
NONE		R					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR_STATUS_STS							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR_STATUS_STS							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR_STATUS_STS							
R							
0h							

Table 3-1508. CONTROLSS_PWMXBAR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PWMXBAR_STATUS_STS	R	0h	Output Signal Status

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3.15.2.2 CONTROLSS_PWMXBAR_FLAGINVERT Register

3.15.2.2.1 CONTROLSS_PWMXBAR_FLAGINVERT Register (Offset = 14h) [reset = 0h]

Output Signal Invert Before Latch.

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Table 3-1509. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1014h

Figure 3-801. CONTROLSS_PWMXBAR_FLAGINVERT Name Register

31	30	29	28	27	26	25	24
RESERVED		PWMXBAR_FLAGINVERT_INVERT					
NONE		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR_FLAGINVERT_INVERT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR_FLAGINVERT_INVERT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR_FLAGINVERT_INVERT							
R/W							
0h							

Table 3-1510. CONTROLSS_PWMXBAR_FLAGINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	PWMXBAR_FLAGINVERT_INVERT	R/W	0h	Output Signal Invert Before Latch

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3.15.2.3 CONTROLSS_PWMXBAR_FLAG Register

3.15.2.3.1 CONTROLSS_PWMXBAR_FLAG Register (Offset = 18h) [reset = 0h]

Output Signal Latched Flag.

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Table 3-1511. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1018h

Figure 3-802. CONTROLSS_PWMXBAR_FLAG Name Register

31	30	29	28	27	26	25	24
RESERVED		PWMXBAR_FLAG_BIT29	PWMXBAR_FLAG_BIT28	PWMXBAR_FLAG_BIT27	PWMXBAR_FLAG_BIT26	PWMXBAR_FLAG_BIT25	PWMXBAR_FLAG_BIT24
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
PWMXBAR_FLAG_BIT23	PWMXBAR_FLAG_BIT22	PWMXBAR_FLAG_BIT21	PWMXBAR_FLAG_BIT20	PWMXBAR_FLAG_BIT19	PWMXBAR_FLAG_BIT18	PWMXBAR_FLAG_BIT17	PWMXBAR_FLAG_BIT16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
PWMXBAR_FLAG_BIT15	PWMXBAR_FLAG_BIT14	PWMXBAR_FLAG_BIT13	PWMXBAR_FLAG_BIT12	PWMXBAR_FLAG_BIT11	PWMXBAR_FLAG_BIT10	PWMXBAR_FLAG_BIT9	PWMXBAR_FLAG_BIT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PWMXBAR_FLAG_BIT7	PWMXBAR_FLAG_BIT6	PWMXBAR_FLAG_BIT5	PWMXBAR_FLAG_BIT4	PWMXBAR_FLAG_BIT3	PWMXBAR_FLAG_BIT2	PWMXBAR_FLAG_BIT1	PWMXBAR_FLAG_BIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1512. CONTROLSS_PWMXBAR_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	PWMXBAR_FLAG_BIT29	R/W	0h	Output Signal Latched Flag
28	PWMXBAR_FLAG_BIT28	R/W	0h	Output Signal Latched Flag
27	PWMXBAR_FLAG_BIT27	R/W	0h	Output Signal Latched Flag
26	PWMXBAR_FLAG_BIT26	R/W	0h	Output Signal Latched Flag
25	PWMXBAR_FLAG_BIT25	R/W	0h	Output Signal Latched Flag
24	PWMXBAR_FLAG_BIT24	R/W	0h	Output Signal Latched Flag
23	PWMXBAR_FLAG_BIT23	R/W	0h	Output Signal Latched Flag
22	PWMXBAR_FLAG_BIT22	R/W	0h	Output Signal Latched Flag
21	PWMXBAR_FLAG_BIT21	R/W	0h	Output Signal Latched Flag
20	PWMXBAR_FLAG_BIT20	R/W	0h	Output Signal Latched Flag
19	PWMXBAR_FLAG_BIT19	R/W	0h	Output Signal Latched Flag
18	PWMXBAR_FLAG_BIT18	R/W	0h	Output Signal Latched Flag
17	PWMXBAR_FLAG_BIT17	R/W	0h	Output Signal Latched Flag
16	PWMXBAR_FLAG_BIT16	R/W	0h	Output Signal Latched Flag
15	PWMXBAR_FLAG_BIT15	R/W	0h	Output Signal Latched Flag
14	PWMXBAR_FLAG_BIT14	R/W	0h	Output Signal Latched Flag

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Table 3-1512. CONTROLSS_PWMXBAR_FLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	PWMXBAR_FLAG_BIT13	R/W	0h	Output Signal Latched Flag
12	PWMXBAR_FLAG_BIT12	R/W	0h	Output Signal Latched Flag
11	PWMXBAR_FLAG_BIT11	R/W	0h	Output Signal Latched Flag
10	PWMXBAR_FLAG_BIT10	R/W	0h	Output Signal Latched Flag
9	PWMXBAR_FLAG_BIT9	R/W	0h	Output Signal Latched Flag
8	PWMXBAR_FLAG_BIT8	R/W	0h	Output Signal Latched Flag
7	PWMXBAR_FLAG_BIT7	R/W	0h	Output Signal Latched Flag
6	PWMXBAR_FLAG_BIT6	R/W	0h	Output Signal Latched Flag
5	PWMXBAR_FLAG_BIT5	R/W	0h	Output Signal Latched Flag
4	PWMXBAR_FLAG_BIT4	R/W	0h	Output Signal Latched Flag
3	PWMXBAR_FLAG_BIT3	R/W	0h	Output Signal Latched Flag
2	PWMXBAR_FLAG_BIT2	R/W	0h	Output Signal Latched Flag
1	PWMXBAR_FLAG_BIT1	R/W	0h	Output Signal Latched Flag
0	PWMXBAR_FLAG_BIT0	R/W	0h	Output Signal Latched Flag

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3.15.2.4 CONTROLSS_PWMXBAR_FLAG_CLR Register

3.15.2.4.1 CONTROLSS_PWMXBAR_FLAG_CLR Register (Offset = 1Ch) [reset = 0h]

Output Signal Latched Flag Clear.

Return to Summary Table

Table 3-1513. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 101Ch

Figure 3-803. CONTROLSS_PWMXBAR_FLAG_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED		PWMXBAR_FLAG_CLR_BIT29	PWMXBAR_FLAG_CLR_BIT28	PWMXBAR_FLAG_CLR_BIT27	PWMXBAR_FLAG_CLR_BIT26	PWMXBAR_FLAG_CLR_BIT25	PWMXBAR_FLAG_CLR_BIT24
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR_FLAG_CLR_BIT23	PWMXBAR_FLAG_CLR_BIT22	PWMXBAR_FLAG_CLR_BIT21	PWMXBAR_FLAG_CLR_BIT20	PWMXBAR_FLAG_CLR_BIT19	PWMXBAR_FLAG_CLR_BIT18	PWMXBAR_FLAG_CLR_BIT17	PWMXBAR_FLAG_CLR_BIT16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR_FLAG_CLR_BIT15	PWMXBAR_FLAG_CLR_BIT14	PWMXBAR_FLAG_CLR_BIT13	PWMXBAR_FLAG_CLR_BIT12	PWMXBAR_FLAG_CLR_BIT11	PWMXBAR_FLAG_CLR_BIT10	PWMXBAR_FLAG_CLR_BIT9	PWMXBAR_FLAG_CLR_BIT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR_FLAG_CLR_BIT7	PWMXBAR_FLAG_CLR_BIT6	PWMXBAR_FLAG_CLR_BIT5	PWMXBAR_FLAG_CLR_BIT4	PWMXBAR_FLAG_CLR_BIT3	PWMXBAR_FLAG_CLR_BIT2	PWMXBAR_FLAG_CLR_BIT1	PWMXBAR_FLAG_CLR_BIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-1514. CONTROLSS_PWMXBAR_FLAG_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	PWMXBAR_FLAG_CLR_BIT29	R/W	0h	Output Signal Latched Flag Clear
28	PWMXBAR_FLAG_CLR_BIT28	R/W	0h	Output Signal Latched Flag Clear
27	PWMXBAR_FLAG_CLR_BIT27	R/W	0h	Output Signal Latched Flag Clear
26	PWMXBAR_FLAG_CLR_BIT26	R/W	0h	Output Signal Latched Flag Clear
25	PWMXBAR_FLAG_CLR_BIT25	R/W	0h	Output Signal Latched Flag Clear
24	PWMXBAR_FLAG_CLR_BIT24	R/W	0h	Output Signal Latched Flag Clear
23	PWMXBAR_FLAG_CLR_BIT23	R/W	0h	Output Signal Latched Flag Clear
22	PWMXBAR_FLAG_CLR_BIT22	R/W	0h	Output Signal Latched Flag Clear
21	PWMXBAR_FLAG_CLR_BIT21	R/W	0h	Output Signal Latched Flag Clear

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Table 3-1514. CONTROLSS_PWMXBAR_FLAG_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	PWMXBAR_FLAG_CLR_BIT20	R/W	0h	Output Signal Latched Flag Clear
19	PWMXBAR_FLAG_CLR_BIT19	R/W	0h	Output Signal Latched Flag Clear
18	PWMXBAR_FLAG_CLR_BIT18	R/W	0h	Output Signal Latched Flag Clear
17	PWMXBAR_FLAG_CLR_BIT17	R/W	0h	Output Signal Latched Flag Clear
16	PWMXBAR_FLAG_CLR_BIT16	R/W	0h	Output Signal Latched Flag Clear
15	PWMXBAR_FLAG_CLR_BIT15	R/W	0h	Output Signal Latched Flag Clear
14	PWMXBAR_FLAG_CLR_BIT14	R/W	0h	Output Signal Latched Flag Clear
13	PWMXBAR_FLAG_CLR_BIT13	R/W	0h	Output Signal Latched Flag Clear
12	PWMXBAR_FLAG_CLR_BIT12	R/W	0h	Output Signal Latched Flag Clear
11	PWMXBAR_FLAG_CLR_BIT11	R/W	0h	Output Signal Latched Flag Clear
10	PWMXBAR_FLAG_CLR_BIT10	R/W	0h	Output Signal Latched Flag Clear
9	PWMXBAR_FLAG_CLR_BIT9	R/W	0h	Output Signal Latched Flag Clear
8	PWMXBAR_FLAG_CLR_BIT8	R/W	0h	Output Signal Latched Flag Clear
7	PWMXBAR_FLAG_CLR_BIT7	R/W	0h	Output Signal Latched Flag Clear
6	PWMXBAR_FLAG_CLR_BIT6	R/W	0h	Output Signal Latched Flag Clear
5	PWMXBAR_FLAG_CLR_BIT5	R/W	0h	Output Signal Latched Flag Clear
4	PWMXBAR_FLAG_CLR_BIT4	R/W	0h	Output Signal Latched Flag Clear
3	PWMXBAR_FLAG_CLR_BIT3	R/W	0h	Output Signal Latched Flag Clear
2	PWMXBAR_FLAG_CLR_BIT2	R/W	0h	Output Signal Latched Flag Clear
1	PWMXBAR_FLAG_CLR_BIT1	R/W	0h	Output Signal Latched Flag Clear
0	PWMXBAR_FLAG_CLR_BIT0	R/W	0h	Output Signal Latched Flag Clear

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3.15.2.5 CONTROLSS_PWMXBAR0_G0 Register

3.15.2.5.1 CONTROLSS_PWMXBAR0_G0 Register (Offset = 100h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to Summary Table

Table 3-1515. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1100h

Figure 3-804. CONTROLSS_PWMXBAR0_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR0_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR0_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR0_G0_SEL							
R/W							
0h							

Table 3-1516. CONTROLSS_PWMXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1516. CONTROLSS_PWMXBAR0_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR0_G0_SEL	R/W	0h	PWM XBAR0 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.6 CONTROLSS_PWMXBAR0_G1 Register

3.15.2.6.1 CONTROLSS_PWMXBAR0_G1 Register (Offset = 104h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to Summary Table

Table 3-1517. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1104h

Figure 3-805. CONTROLSS_PWMXBAR0_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR0_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR0_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR0_G1_SEL							
R/W							
0h							

Table 3-1518. CONTROLSS_PWMXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1518. CONTROLSS_PWMXBAR0_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR0_G1_SEL	R/W	0h	PWM XBAR0 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.7 CONTROLSS_PWMXBAR0_G2 Register

3.15.2.7.1 CONTROLSS_PWMXBAR0_G2 Register (Offset = 108h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to Summary Table

Table 3-1519. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1108h

Figure 3-806. CONTROLSS_PWMXBAR0_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR0_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR0_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR0_G2_SEL							
R/W							
0h							

Table 3-1520. CONTROLSS_PWMXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1520. CONTROLSS_PWMXBAR0_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR0_G2_SEL	R/W	0h	PWM XBAR0 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.8 CONTROLSS_PWMXBAR0_G3 Register

3.15.2.8.1 CONTROLSS_PWMXBAR0_G3 Register (Offset = 10Ch) [reset = 0h]

PWM XBAR 0 Input Select.

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Table 3-1521. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 110Ch

Figure 3-807. CONTROLSS_PWMXBAR0_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR0_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR0_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR0_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR0_G3_SEL							
R/W							
0h							

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Table 3-1522. CONTROLSS_PWMXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR0_G3_SEL	R/W	0h	PWM XBAR0 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.9 CONTROLSS_PWMXBAR0_G4 Register

3.15.2.9.1 CONTROLSS_PWMXBAR0_G4 Register (Offset = 110h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to Summary Table

Table 3-1523. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1110h

Figure 3-808. CONTROLSS_PWMXBAR0_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR0_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR0_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR0_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR0_G4_SEL							
R/W							
0h							

Table 3-1524. CONTROLSS_PWMXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR0_G4_SEL	R/W	0h	PWM XBAR0 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.10 CONTROLSS_PWMXBAR0_G5 Register

3.15.2.10.1 CONTROLSS_PWMXBAR0_G5 Register (Offset = 114h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to Summary Table

Table 3-1525. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1114h

Figure 3-809. CONTROLSS_PWMXBAR0_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR0_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR0_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR0_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR0_G5_SEL							
R/W							
0h							

Table 3-1526. CONTROLSS_PWMXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR0_G5_SEL	R/W	0h	PWM XBAR0 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.11 CONTROLSS_PWMXBAR0_G6 Register

3.15.2.11.1 CONTROLSS_PWMXBAR0_G6 Register (Offset = 118h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to Summary Table

Table 3-1527. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1118h

Figure 3-810. CONTROLSS_PWMXBAR0_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR0_G6_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR0_G6_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR0_G6_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR0_G6_SEL							
R/W							
0h							

Table 3-1528. CONTROLSS_PWMXBAR0_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR0_G6_SEL	R/W	0h	PWM XBAR0 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.12 CONTROLSS_PWMXBAR0_G7 Register

3.15.2.12.1 CONTROLSS_PWMXBAR0_G7 Register (Offset = 11Ch) [reset = 0h]

PWM XBAR 0 Input Select.

Return to Summary Table

Table 3-1529. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 111Ch

Figure 3-811. CONTROLSS_PWMXBAR0_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR0_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR0_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR0_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR0_G7_SEL							
R/W							
0h							

Table 3-1530. CONTROLSS_PWMXBAR0_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR0_G7_SEL	R/W	0h	PWM XBAR0 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.13 CONTROLSS_PWMXBAR0_G8 Register

3.15.2.13.1 CONTROLSS_PWMXBAR0_G8 Register (Offset = 120h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to Summary Table

Table 3-1531. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1120h

Figure 3-812. CONTROLSS_PWMXBAR0_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR0_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR0_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR0_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR0_G8_SEL							
R/W							
0h							

Table 3-1532. CONTROLSS_PWMXBAR0_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR0_G8_SEL	R/W	0h	PWM XBAR0 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.14 CONTROLSS_PWMXBAR0_G9 Register

3.15.2.14.1 CONTROLSS_PWMXBAR0_G9 Register (Offset = 124h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to Summary Table

Table 3-1533. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1124h

Figure 3-813. CONTROLSS_PWMXBAR0_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR0_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1534. CONTROLSS_PWMXBAR0_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR0_G9_SEL	R/W	0h	PWM XBAR0 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.15 CONTROLSS_PWMXBAR1_G0 Register

3.15.2.15.1 CONTROLSS_PWMXBAR1_G0 Register (Offset = 140h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to Summary Table

Table 3-1535. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1140h

Figure 3-814. CONTROLSS_PWMXBAR1_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR1_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR1_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR1_G0_SEL							
R/W							
0h							

Table 3-1536. CONTROLSS_PWMXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1536. CONTROLSS_PWMXBAR1_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR1_G0_SEL	R/W	0h	PWM XBAR1 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.16 CONTROLSS_PWMXBAR1_G1 Register

3.15.2.16.1 CONTROLSS_PWMXBAR1_G1 Register (Offset = 144h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to Summary Table

Table 3-1537. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1144h

Figure 3-815. CONTROLSS_PWMXBAR1_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR1_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR1_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR1_G1_SEL							
R/W							
0h							

Table 3-1538. CONTROLSS_PWMXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1538. CONTROLSS_PWMXBAR1_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR1_G1_SEL	R/W	0h	PWM XBAR1 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.17 CONTROLSS_PWMXBAR1_G2 Register

3.15.2.17.1 CONTROLSS_PWMXBAR1_G2 Register (Offset = 148h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to Summary Table

Table 3-1539. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1148h

Figure 3-816. CONTROLSS_PWMXBAR1_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR1_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR1_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR1_G2_SEL							
R/W							
0h							

Table 3-1540. CONTROLSS_PWMXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1540. CONTROLSS_PWMXBAR1_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR1_G2_SEL	R/W	0h	PWM XBAR1 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.18 CONTROLSS_PWMXBAR1_G3 Register

3.15.2.18.1 CONTROLSS_PWMXBAR1_G3 Register (Offset = 14Ch) [reset = 0h]

PWM XBAR 1 Input Select.

Return to Summary Table

Table 3-1541. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 114Ch

Figure 3-817. CONTROLSS_PWMXBAR1_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR1_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR1_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR1_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR1_G3_SEL							
R/W							
0h							

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Table 3-1542. CONTROLSS_PWMXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR1_G3_SEL	R/W	0h	PWM XBAR1 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.19 CONTROLSS_PWMXBAR1_G4 Register

3.15.2.19.1 CONTROLSS_PWMXBAR1_G4 Register (Offset = 150h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to Summary Table

Table 3-1543. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1150h

Figure 3-818. CONTROLSS_PWMXBAR1_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR1_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR1_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR1_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR1_G4_SEL							
R/W							
0h							

Table 3-1544. CONTROLSS_PWMXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR1_G4_SEL	R/W	0h	PWM XBAR1 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.20 CONTROLSS_PWMXBAR1_G5 Register

3.15.2.20.1 CONTROLSS_PWMXBAR1_G5 Register (Offset = 154h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to Summary Table

Table 3-1545. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1154h

Figure 3-819. CONTROLSS_PWMXBAR1_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR1_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR1_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR1_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR1_G5_SEL							
R/W							
0h							

Table 3-1546. CONTROLSS_PWMXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR1_G5_SEL	R/W	0h	PWM XBAR1 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.21 CONTROLSS_PWMXBAR1_G6 Register

3.15.2.21.1 CONTROLSS_PWMXBAR1_G6 Register (Offset = 158h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to Summary Table

Table 3-1547. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1158h

Figure 3-820. CONTROLSS_PWMXBAR1_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR1_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR1_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR1_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR1_G6_SEL							
R/W							
0h							

Table 3-1548. CONTROLSS_PWMXBAR1_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR1_G6_SEL	R/W	0h	PWM XBAR1 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.22 CONTROLSS_PWMXBAR1_G7 Register

3.15.2.22.1 CONTROLSS_PWMXBAR1_G7 Register (Offset = 15Ch) [reset = 0h]

PWM XBAR 1 Input Select.

Return to Summary Table

Table 3-1549. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 115Ch

Figure 3-821. CONTROLSS_PWMXBAR1_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR1_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR1_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR1_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR1_G7_SEL							
R/W							
0h							

Table 3-1550. CONTROLSS_PWMXBAR1_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR1_G7_SEL	R/W	0h	PWM XBAR1 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.23 CONTROLSS_PWMXBAR1_G8 Register

3.15.2.23.1 CONTROLSS_PWMXBAR1_G8 Register (Offset = 160h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to Summary Table

Table 3-1551. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1160h

Figure 3-822. CONTROLSS_PWMXBAR1_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR1_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR1_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR1_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR1_G8_SEL							
R/W							
0h							

Table 3-1552. CONTROLSS_PWMXBAR1_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR1_G8_SEL	R/W	0h	PWM XBAR1 G8 Input Select 0:EQEP0.ERR 1:EQEP1.ERR 2:EQEP2.ERR 6 3:FSIRX0.RX_TRIG4 10 7:FSIRX1.RX_TRIG4 14 11:FSIRX2.RX_TRIG4 18 15:FSIRX3.RX_TRIG4 31 19:ECAP[12:0].TRIPOUT

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3.15.2.24 CONTROLSS_PWMXBAR1_G9 Register

3.15.2.24.1 CONTROLSS_PWMXBAR1_G9 Register (Offset = 164h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to Summary Table

Table 3-1553. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1164h

Figure 3-823. CONTROLSS_PWMXBAR1_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PWMXBAR1_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1554. CONTROLSS_PWMXBAR1_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR1_G9_SEL	R/W	0h	PWM XBAR1 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.25 CONTROLSS_PWMXBAR2_G0 Register

3.15.2.25.1 CONTROLSS_PWMXBAR2_G0 Register (Offset = 180h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to Summary Table

Table 3-1555. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1180h

Figure 3-824. CONTROLSS_PWMXBAR2_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR2_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR2_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR2_G0_SEL							
R/W							
0h							

Table 3-1556. CONTROLSS_PWMXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1556. CONTROLSS_PWMXBAR2_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR2_G0_SEL	R/W	0h	PWM XBAR2 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.26 CONTROLSS_PWMXBAR2_G1 Register

3.15.2.26.1 CONTROLSS_PWMXBAR2_G1 Register (Offset = 184h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to Summary Table

Table 3-1557. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1184h

Figure 3-825. CONTROLSS_PWMXBAR2_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR2_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR2_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR2_G1_SEL							
R/W							
0h							

Table 3-1558. CONTROLSS_PWMXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1558. CONTROLSS_PWMXBAR2_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR2_G1_SEL	R/W	0h	PWM XBAR2 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.27 CONTROLSS_PWMXBAR2_G2 Register

3.15.2.27.1 CONTROLSS_PWMXBAR2_G2 Register (Offset = 188h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to Summary Table

Table 3-1559. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1188h

Figure 3-826. CONTROLSS_PWMXBAR2_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR2_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR2_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR2_G2_SEL							
R/W							
0h							

Table 3-1560. CONTROLSS_PWMXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1560. CONTROLSS_PWMXBAR2_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR2_G2_SEL	R/W	0h	PWM XBAR2 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.28 CONTROLSS_PWMXBAR2_G3 Register

3.15.2.28.1 CONTROLSS_PWMXBAR2_G3 Register (Offset = 18Ch) [reset = 0h]

PWM XBAR 2 Input Select.

Return to Summary Table

Table 3-1561. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 118Ch

Figure 3-827. CONTROLSS_PWMXBAR2_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR2_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR2_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR2_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR2_G3_SEL							
R/W							
0h							

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Table 3-1562. CONTROLSS_PWMXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR2_G3_SEL	R/W	0h	PWM XBAR2 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.29 CONTROLSS_PWMXBAR2_G4 Register

3.15.2.29.1 CONTROLSS_PWMXBAR2_G4 Register (Offset = 190h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to Summary Table

Table 3-1563. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1190h

Figure 3-828. CONTROLSS_PWMXBAR2_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR2_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR2_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR2_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR2_G4_SEL							
R/W							
0h							

Table 3-1564. CONTROLSS_PWMXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR2_G4_SEL	R/W	0h	PWM XBAR2 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.30 CONTROLSS_PWMXBAR2_G5 Register

3.15.2.30.1 CONTROLSS_PWMXBAR2_G5 Register (Offset = 194h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to Summary Table

Table 3-1565. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1194h

Figure 3-829. CONTROLSS_PWMXBAR2_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR2_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR2_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR2_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR2_G5_SEL							
R/W							
0h							

Table 3-1566. CONTROLSS_PWMXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR2_G5_SEL	R/W	0h	PWM XBAR2 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.31 CONTROLSS_PWMXBAR2_G6 Register

3.15.2.31.1 CONTROLSS_PWMXBAR2_G6 Register (Offset = 198h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to Summary Table

Table 3-1567. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1198h

Figure 3-830. CONTROLSS_PWMXBAR2_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR2_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR2_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR2_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR2_G6_SEL							
R/W							
0h							

Table 3-1568. CONTROLSS_PWMXBAR2_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR2_G6_SEL	R/W	0h	PWM XBAR2 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.32 CONTROLSS_PWMXBAR2_G7 Register

3.15.2.32.1 CONTROLSS_PWMXBAR2_G7 Register (Offset = 19Ch) [reset = 0h]

PWM XBAR 2 Input Select.

Return to Summary Table

Table 3-1569. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 119Ch

Figure 3-831. CONTROLSS_PWMXBAR2_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR2_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR2_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR2_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR2_G7_SEL							
R/W							
0h							

Table 3-1570. CONTROLSS_PWMXBAR2_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR2_G7_SEL	R/W	0h	PWM XBAR2 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.33 CONTROLSS_PWMXBAR2_G8 Register

3.15.2.33.1 CONTROLSS_PWMXBAR2_G8 Register (Offset = 1A0h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to Summary Table

Table 3-1571. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11A0h

Figure 3-832. CONTROLSS_PWMXBAR2_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR2_G8_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR2_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR2_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR2_G8_SEL							
R/W							
0h							

Table 3-1572. CONTROLSS_PWMXBAR2_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR2_G8_SEL	R/W	0h	PWM XBAR2 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.34 CONTROLSS_PWMXBAR2_G9 Register

3.15.2.34.1 CONTROLSS_PWMXBAR2_G9 Register (Offset = 1A4h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to Summary Table

Table 3-1573. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11A4h

Figure 3-833. CONTROLSS_PWMXBAR2_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR2_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1574. CONTROLSS_PWMXBAR2_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR2_G9_SEL	R/W	0h	PWM XBAR2 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.35 CONTROLSS_PWMXBAR3_G0 Register

3.15.2.35.1 CONTROLSS_PWMXBAR3_G0 Register (Offset = 1C0h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to Summary Table

Table 3-1575. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11C0h

Figure 3-834. CONTROLSS_PWMXBAR3_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR3_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR3_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR3_G0_SEL							
R/W							
0h							

Table 3-1576. CONTROLSS_PWMXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1576. CONTROLSS_PWMXBAR3_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR3_G0_SEL	R/W	0h	PWM XBAR3 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.36 CONTROLSS_PWMXBAR3_G1 Register

3.15.2.36.1 CONTROLSS_PWMXBAR3_G1 Register (Offset = 1C4h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to Summary Table

Table 3-1577. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11C4h

Figure 3-835. CONTROLSS_PWMXBAR3_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR3_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR3_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR3_G1_SEL							
R/W							
0h							

Table 3-1578. CONTROLSS_PWMXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1578. CONTROLSS_PWMXBAR3_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR3_G1_SEL	R/W	0h	PWM XBAR3 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.37 CONTROLSS_PWMXBAR3_G2 Register

3.15.2.37.1 CONTROLSS_PWMXBAR3_G2 Register (Offset = 1C8h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to Summary Table

Table 3-1579. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11C8h

Figure 3-836. CONTROLSS_PWMXBAR3_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR3_G2_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR3_G2_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR3_G2_SEL							
R/W							
0h							

Table 3-1580. CONTROLSS_PWMXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1580. CONTROLSS_PWMXBAR3_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR3_G2_SEL	R/W	0h	PWM XBAR3 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.38 CONTROLSS_PWMXBAR3_G3 Register

3.15.2.38.1 CONTROLSS_PWMXBAR3_G3 Register (Offset = 1CCh) [reset = 0h]

PWM XBAR 3 Input Select.

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Table 3-1581. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11CCh

Figure 3-837. CONTROLSS_PWMXBAR3_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR3_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR3_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR3_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR3_G3_SEL							
R/W							
0h							

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Table 3-1582. CONTROLSS_PWMXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR3_G3_SEL	R/W	0h	PWM XBAR3 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.39 CONTROLSS_PWMXBAR3_G4 Register

3.15.2.39.1 CONTROLSS_PWMXBAR3_G4 Register (Offset = 1D0h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to Summary Table

Table 3-1583. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11D0h

Figure 3-838. CONTROLSS_PWMXBAR3_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR3_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR3_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR3_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR3_G4_SEL							
R/W							
0h							

Table 3-1584. CONTROLSS_PWMXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR3_G4_SEL	R/W	0h	PWM XBAR3 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.40 CONTROLSS_PWMXBAR3_G5 Register

3.15.2.40.1 CONTROLSS_PWMXBAR3_G5 Register (Offset = 1D4h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to Summary Table

Table 3-1585. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11D4h

Figure 3-839. CONTROLSS_PWMXBAR3_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR3_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR3_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR3_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR3_G5_SEL							
R/W							
0h							

Table 3-1586. CONTROLSS_PWMXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR3_G5_SEL	R/W	0h	PWM XBAR3 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.41 CONTROLSS_PWMXBAR3_G6 Register

3.15.2.41.1 CONTROLSS_PWMXBAR3_G6 Register (Offset = 1D8h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to Summary Table

Table 3-1587. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11D8h

Figure 3-840. CONTROLSS_PWMXBAR3_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR3_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR3_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR3_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR3_G6_SEL							
R/W							
0h							

Table 3-1588. CONTROLSS_PWMXBAR3_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR3_G6_SEL	R/W	0h	PWM XBAR3 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.42 CONTROLSS_PWMXBAR3_G7 Register

3.15.2.42.1 CONTROLSS_PWMXBAR3_G7 Register (Offset = 1DCh) [reset = 0h]

PWM XBAR 3 Input Select.

Return to Summary Table

Table 3-1589. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11DCh

Figure 3-841. CONTROLSS_PWMXBAR3_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR3_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR3_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR3_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR3_G7_SEL							
R/W							
0h							

Table 3-1590. CONTROLSS_PWMXBAR3_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR3_G7_SEL	R/W	0h	PWM XBAR3 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.43 CONTROLSS_PWMXBAR3_G8 Register

3.15.2.43.1 CONTROLSS_PWMXBAR3_G8 Register (Offset = 1E0h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to Summary Table

Table 3-1591. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11E0h

Figure 3-842. CONTROLSS_PWMXBAR3_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR3_G8_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR3_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR3_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR3_G8_SEL							
R/W							
0h							

Table 3-1592. CONTROLSS_PWMXBAR3_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR3_G8_SEL	R/W	0h	PWM XBAR3 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.44 CONTROLSS_PWMXBAR3_G9 Register

3.15.2.44.1 CONTROLSS_PWMXBAR3_G9 Register (Offset = 1E4h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to Summary Table

Table 3-1593. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 11E4h

Figure 3-843. CONTROLSS_PWMXBAR3_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR3_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1594. CONTROLSS_PWMXBAR3_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR3_G9_SEL	R/W	0h	PWM XBAR3 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.45 CONTROLSS_PWMXBAR4_G0 Register

3.15.2.45.1 CONTROLSS_PWMXBAR4_G0 Register (Offset = 200h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to Summary Table

Table 3-1595. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1200h

Figure 3-844. CONTROLSS_PWMXBAR4_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR4_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR4_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR4_G0_SEL							
R/W							
0h							

Table 3-1596. CONTROLSS_PWMXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1596. CONTROLSS_PWMXBAR4_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR4_G0_SEL	R/W	0h	PWM XBAR4 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.46 CONTROLSS_PWMXBAR4_G1 Register

3.15.2.46.1 CONTROLSS_PWMXBAR4_G1 Register (Offset = 204h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to Summary Table

Table 3-1597. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1204h

Figure 3-845. CONTROLSS_PWMXBAR4_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR4_G1_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR4_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR4_G1_SEL							
R/W							
0h							

Table 3-1598. CONTROLSS_PWMXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1598. CONTROLSS_PWMXBAR4_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR4_G1_SEL	R/W	0h	PWM XBAR4 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.47 CONTROLSS_PWMXBAR4_G2 Register

3.15.2.47.1 CONTROLSS_PWMXBAR4_G2 Register (Offset = 208h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to Summary Table

Table 3-1599. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1208h

Figure 3-846. CONTROLSS_PWMXBAR4_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR4_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR4_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR4_G2_SEL							
R/W							
0h							

Table 3-1600. CONTROLSS_PWMXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1600. CONTROLSS_PWMXBAR4_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR4_G2_SEL	R/W	0h	PWM XBAR4 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.48 CONTROLSS_PWMXBAR4_G3 Register

3.15.2.48.1 CONTROLSS_PWMXBAR4_G3 Register (Offset = 20Ch) [reset = 0h]

PWM XBAR 4 Input Select.

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Table 3-1601. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 120Ch

Figure 3-847. CONTROLSS_PWMXBAR4_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR4_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR4_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR4_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR4_G3_SEL							
R/W							
0h							

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Table 3-1602. CONTROLSS_PWMXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR4_G3_SEL	R/W	0h	PWM XBAR4 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.49 CONTROLSS_PWMXBAR4_G4 Register

3.15.2.49.1 CONTROLSS_PWMXBAR4_G4 Register (Offset = 210h) [reset = 0h]

PWM XBAR 4 Input Select.

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Table 3-1603. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1210h

Figure 3-848. CONTROLSS_PWMXBAR4_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR4_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR4_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR4_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR4_G4_SEL							
R/W							
0h							

Table 3-1604. CONTROLSS_PWMXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR4_G4_SEL	R/W	0h	PWM XBAR4 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.50 CONTROLSS_PWMXBAR4_G5 Register

3.15.2.50.1 CONTROLSS_PWMXBAR4_G5 Register (Offset = 214h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to Summary Table

Table 3-1605. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1214h

Figure 3-849. CONTROLSS_PWMXBAR4_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR4_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR4_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR4_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR4_G5_SEL							
R/W							
0h							

Table 3-1606. CONTROLSS_PWMXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR4_G5_SEL	R/W	0h	PWM XBAR4 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.51 CONTROLSS_PWMXBAR4_G6 Register

3.15.2.51.1 CONTROLSS_PWMXBAR4_G6 Register (Offset = 218h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to Summary Table

Table 3-1607. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1218h

Figure 3-850. CONTROLSS_PWMXBAR4_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR4_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR4_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR4_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR4_G6_SEL							
R/W							
0h							

Table 3-1608. CONTROLSS_PWMXBAR4_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR4_G6_SEL	R/W	0h	PWM XBAR4 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.52 CONTROLSS_PWMXBAR4_G7 Register

3.15.2.52.1 CONTROLSS_PWMXBAR4_G7 Register (Offset = 21Ch) [reset = 0h]

PWM XBAR 4 Input Select.

Return to Summary Table

Table 3-1609. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 121Ch

Figure 3-851. CONTROLSS_PWMXBAR4_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR4_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR4_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR4_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR4_G7_SEL							
R/W							
0h							

Table 3-1610. CONTROLSS_PWMXBAR4_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR4_G7_SEL	R/W	0h	PWM XBAR4 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.53 CONTROLSS_PWMXBAR4_G8 Register

3.15.2.53.1 CONTROLSS_PWMXBAR4_G8 Register (Offset = 220h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to Summary Table

Table 3-1611. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1220h

Figure 3-852. CONTROLSS_PWMXBAR4_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR4_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR4_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR4_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR4_G8_SEL							
R/W							
0h							

Table 3-1612. CONTROLSS_PWMXBAR4_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR4_G8_SEL	R/W	0h	PWM XBAR4 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.54 CONTROLSS_PWMXBAR4_G9 Register

3.15.2.54.1 CONTROLSS_PWMXBAR4_G9 Register (Offset = 224h) [reset = 0h]

PWM XBAR 4 Input Select.

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Table 3-1613. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1224h

Figure 3-853. CONTROLSS_PWMXBAR4_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR4_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1614. CONTROLSS_PWMXBAR4_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR4_G9_SEL	R/W	0h	PWM XBAR4 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.55 CONTROLSS_PWMXBAR5_G0 Register

3.15.2.55.1 CONTROLSS_PWMXBAR5_G0 Register (Offset = 240h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to Summary Table

Table 3-1615. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1240h

Figure 3-854. CONTROLSS_PWMXBAR5_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR5_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR5_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR5_G0_SEL							
R/W							
0h							

Table 3-1616. CONTROLSS_PWMXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1616. CONTROLSS_PWMXBAR5_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR5_G0_SEL	R/W	0h	PWM XBAR5 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.56 CONTROLSS_PWMXBAR5_G1 Register

3.15.2.56.1 CONTROLSS_PWMXBAR5_G1 Register (Offset = 244h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to Summary Table

Table 3-1617. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1244h

Figure 3-855. CONTROLSS_PWMXBAR5_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR5_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR5_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR5_G1_SEL							
R/W							
0h							

Table 3-1618. CONTROLSS_PWMXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1618. CONTROLSS_PWMXBAR5_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR5_G1_SEL	R/W	0h	PWM XBAR5 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.57 CONTROLSS_PWMXBAR5_G2 Register

3.15.2.57.1 CONTROLSS_PWMXBAR5_G2 Register (Offset = 248h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to Summary Table

Table 3-1619. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1248h

Figure 3-856. CONTROLSS_PWMXBAR5_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR5_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR5_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR5_G2_SEL							
R/W							
0h							

Table 3-1620. CONTROLSS_PWMXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1620. CONTROLSS_PWMXBAR5_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR5_G2_SEL	R/W	0h	PWM XBAR5 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.58 CONTROLSS_PWMXBAR5_G3 Register

3.15.2.58.1 CONTROLSS_PWMXBAR5_G3 Register (Offset = 24Ch) [reset = 0h]

PWM XBAR 5 Input Select.

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Table 3-1621. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 124Ch

Figure 3-857. CONTROLSS_PWMXBAR5_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR5_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR5_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR5_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR5_G3_SEL							
R/W							
0h							

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Table 3-1622. CONTROLSS_PWMXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR5_G3_SEL	R/W	0h	PWM XBAR5 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.59 CONTROLSS_PWMXBAR5_G4 Register

3.15.2.59.1 CONTROLSS_PWMXBAR5_G4 Register (Offset = 250h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to Summary Table

Table 3-1623. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1250h

Figure 3-858. CONTROLSS_PWMXBAR5_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR5_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR5_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR5_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR5_G4_SEL							
R/W							
0h							

Table 3-1624. CONTROLSS_PWMXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR5_G4_SEL	R/W	0h	PWM XBAR5 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.60 CONTROLSS_PWMXBAR5_G5 Register

3.15.2.60.1 CONTROLSS_PWMXBAR5_G5 Register (Offset = 254h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to Summary Table

Table 3-1625. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1254h

Figure 3-859. CONTROLSS_PWMXBAR5_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR5_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR5_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR5_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR5_G5_SEL							
R/W							
0h							

Table 3-1626. CONTROLSS_PWMXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR5_G5_SEL	R/W	0h	PWM XBAR5 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.61 CONTROLSS_PWMXBAR5_G6 Register

3.15.2.61.1 CONTROLSS_PWMXBAR5_G6 Register (Offset = 258h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to Summary Table

Table 3-1627. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1258h

Figure 3-860. CONTROLSS_PWMXBAR5_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR5_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR5_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR5_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR5_G6_SEL							
R/W							
0h							

Table 3-1628. CONTROLSS_PWMXBAR5_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR5_G6_SEL	R/W	0h	PWM XBAR5 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.62 CONTROLSS_PWMXBAR5_G7 Register

3.15.2.62.1 CONTROLSS_PWMXBAR5_G7 Register (Offset = 25Ch) [reset = 0h]

PWM XBAR 5 Input Select.

Return to Summary Table

Table 3-1629. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 125Ch

Figure 3-861. CONTROLSS_PWMXBAR5_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR5_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR5_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR5_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR5_G7_SEL							
R/W							
0h							

Table 3-1630. CONTROLSS_PWMXBAR5_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR5_G7_SEL	R/W	0h	PWM XBAR5 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.63 CONTROLSS_PWMXBAR5_G8 Register

3.15.2.63.1 CONTROLSS_PWMXBAR5_G8 Register (Offset = 260h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to Summary Table

Table 3-1631. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1260h

Figure 3-862. CONTROLSS_PWMXBAR5_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR5_G8_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR5_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR5_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR5_G8_SEL							
R/W							
0h							

Table 3-1632. CONTROLSS_PWMXBAR5_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR5_G8_SEL	R/W	0h	PWM XBAR5 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.64 CONTROLSS_PWMXBAR5_G9 Register

3.15.2.64.1 CONTROLSS_PWMXBAR5_G9 Register (Offset = 264h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to Summary Table

Table 3-1633. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1264h

Figure 3-863. CONTROLSS_PWMXBAR5_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR5_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1634. CONTROLSS_PWMXBAR5_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR5_G9_SEL	R/W	0h	PWM XBAR5 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.65 CONTROLSS_PWMXBAR6_G0 Register

3.15.2.65.1 CONTROLSS_PWMXBAR6_G0 Register (Offset = 280h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to Summary Table

Table 3-1635. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1280h

Figure 3-864. CONTROLSS_PWMXBAR6_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR6_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR6_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR6_G0_SEL							
R/W							
0h							

Table 3-1636. CONTROLSS_PWMXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1636. CONTROLSS_PWMXBAR6_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR6_G0_SEL	R/W	0h	PWM XBAR6 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.66 CONTROLSS_PWMXBAR6_G1 Register

3.15.2.66.1 CONTROLSS_PWMXBAR6_G1 Register (Offset = 284h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to Summary Table

Table 3-1637. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1284h

Figure 3-865. CONTROLSS_PWMXBAR6_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR6_G1_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR6_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR6_G1_SEL							
R/W							
0h							

Table 3-1638. CONTROLSS_PWMXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1638. CONTROLSS_PWMXBAR6_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR6_G1_SEL	R/W	0h	PWM XBAR6 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.67 CONTROLSS_PWMXBAR6_G2 Register

3.15.2.67.1 CONTROLSS_PWMXBAR6_G2 Register (Offset = 288h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to Summary Table

Table 3-1639. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1288h

Figure 3-866. CONTROLSS_PWMXBAR6_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR6_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR6_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR6_G2_SEL							
R/W							
0h							

Table 3-1640. CONTROLSS_PWMXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1640. CONTROLSS_PWMXBAR6_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR6_G2_SEL	R/W	0h	PWM XBAR6 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.68 CONTROLSS_PWMXBAR6_G3 Register

3.15.2.68.1 CONTROLSS_PWMXBAR6_G3 Register (Offset = 28Ch) [reset = 0h]

PWM XBAR 6 Input Select.

Return to Summary Table

Table 3-1641. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 128Ch

Figure 3-867. CONTROLSS_PWMXBAR6_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR6_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR6_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR6_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR6_G3_SEL							
R/W							
0h							

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Table 3-1642. CONTROLSS_PWMXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR6_G3_SEL	R/W	0h	PWM XBAR6 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.69 CONTROLSS_PWMXBAR6_G4 Register

3.15.2.69.1 CONTROLSS_PWMXBAR6_G4 Register (Offset = 290h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to Summary Table

Table 3-1643. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1290h

Figure 3-868. CONTROLSS_PWMXBAR6_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR6_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR6_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR6_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR6_G4_SEL							
R/W							
0h							

Table 3-1644. CONTROLSS_PWMXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR6_G4_SEL	R/W	0h	PWM XBAR6 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.70 CONTROLSS_PWMXBAR6_G5 Register

3.15.2.70.1 CONTROLSS_PWMXBAR6_G5 Register (Offset = 294h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to Summary Table

Table 3-1645. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1294h

Figure 3-869. CONTROLSS_PWMXBAR6_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR6_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR6_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR6_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR6_G5_SEL							
R/W							
0h							

Table 3-1646. CONTROLSS_PWMXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR6_G5_SEL	R/W	0h	PWM XBAR6 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.71 CONTROLSS_PWMXBAR6_G6 Register

3.15.2.71.1 CONTROLSS_PWMXBAR6_G6 Register (Offset = 298h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to Summary Table

Table 3-1647. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1298h

Figure 3-870. CONTROLSS_PWMXBAR6_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR6_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR6_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR6_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR6_G6_SEL							
R/W							
0h							

Table 3-1648. CONTROLSS_PWMXBAR6_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR6_G6_SEL	R/W	0h	PWM XBAR6 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.72 CONTROLSS_PWMXBAR6_G7 Register

3.15.2.72.1 CONTROLSS_PWMXBAR6_G7 Register (Offset = 29Ch) [reset = 0h]

PWM XBAR 6 Input Select.

Return to Summary Table

Table 3-1649. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 129Ch

Figure 3-871. CONTROLSS_PWMXBAR6_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR6_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR6_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR6_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR6_G7_SEL							
R/W							
0h							

Table 3-1650. CONTROLSS_PWMXBAR6_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR6_G7_SEL	R/W	0h	PWM XBAR6 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.73 CONTROLSS_PWMXBAR6_G8 Register

3.15.2.73.1 CONTROLSS_PWMXBAR6_G8 Register (Offset = 2A0h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to Summary Table

Table 3-1651. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12A0h

Figure 3-872. CONTROLSS_PWMXBAR6_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR6_G8_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR6_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR6_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR6_G8_SEL							
R/W							
0h							

Table 3-1652. CONTROLSS_PWMXBAR6_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR6_G8_SEL	R/W	0h	PWM XBAR6 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.74 CONTROLSS_PWMXBAR6_G9 Register

3.15.2.74.1 CONTROLSS_PWMXBAR6_G9 Register (Offset = 2A4h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to Summary Table

Table 3-1653. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12A4h

Figure 3-873. CONTROLSS_PWMXBAR6_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR6_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1654. CONTROLSS_PWMXBAR6_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR6_G9_SEL	R/W	0h	PWM XBAR6 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.75 CONTROLSS_PWMXBAR7_G0 Register

3.15.2.75.1 CONTROLSS_PWMXBAR7_G0 Register (Offset = 2C0h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to Summary Table

Table 3-1655. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12C0h

Figure 3-874. CONTROLSS_PWMXBAR7_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR7_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR7_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR7_G0_SEL							
R/W							
0h							

Table 3-1656. CONTROLSS_PWMXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1656. CONTROLSS_PWMXBAR7_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR7_G0_SEL	R/W	0h	PWM XBAR7 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.76 CONTROLSS_PWMXBAR7_G1 Register

3.15.2.76.1 CONTROLSS_PWMXBAR7_G1 Register (Offset = 2C4h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to Summary Table

Table 3-1657. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12C4h

Figure 3-875. CONTROLSS_PWMXBAR7_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR7_G1_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR7_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR7_G1_SEL							
R/W							
0h							

Table 3-1658. CONTROLSS_PWMXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1658. CONTROLSS_PWMXBAR7_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR7_G1_SEL	R/W	0h	PWM XBAR7 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.77 CONTROLSS_PWMXBAR7_G2 Register

3.15.2.77.1 CONTROLSS_PWMXBAR7_G2 Register (Offset = 2C8h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to Summary Table

Table 3-1659. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12C8h

Figure 3-876. CONTROLSS_PWMXBAR7_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR7_G2_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR7_G2_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR7_G2_SEL							
R/W							
0h							

Table 3-1660. CONTROLSS_PWMXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1660. CONTROLSS_PWMXBAR7_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR7_G2_SEL	R/W	0h	PWM XBAR7 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.78 CONTROLSS_PWMXBAR7_G3 Register

3.15.2.78.1 CONTROLSS_PWMXBAR7_G3 Register (Offset = 2CCh) [reset = 0h]

PWM XBAR 7 Input Select.

Return to Summary Table

Table 3-1661. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12CCh

Figure 3-877. CONTROLSS_PWMXBAR7_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR7_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR7_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR7_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR7_G3_SEL							
R/W							
0h							

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Table 3-1662. CONTROLSS_PWMXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR7_G3_SEL	R/W	0h	PWM XBAR7 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.79 CONTROLSS_PWMXBAR7_G4 Register

3.15.2.79.1 CONTROLSS_PWMXBAR7_G4 Register (Offset = 2D0h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to Summary Table

Table 3-1663. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12D0h

Figure 3-878. CONTROLSS_PWMXBAR7_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR7_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR7_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR7_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR7_G4_SEL							
R/W							
0h							

Table 3-1664. CONTROLSS_PWMXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR7_G4_SEL	R/W	0h	PWM XBAR7 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.80 CONTROLSS_PWMXBAR7_G5 Register

3.15.2.80.1 CONTROLSS_PWMXBAR7_G5 Register (Offset = 2D4h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to Summary Table

Table 3-1665. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12D4h

Figure 3-879. CONTROLSS_PWMXBAR7_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR7_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR7_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR7_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR7_G5_SEL							
R/W							
0h							

Table 3-1666. CONTROLSS_PWMXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR7_G5_SEL	R/W	0h	PWM XBAR7 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.81 CONTROLSS_PWMXBAR7_G6 Register

3.15.2.81.1 CONTROLSS_PWMXBAR7_G6 Register (Offset = 2D8h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to Summary Table

Table 3-1667. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12D8h

Figure 3-880. CONTROLSS_PWMXBAR7_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR7_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR7_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR7_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR7_G6_SEL							
R/W							
0h							

Table 3-1668. CONTROLSS_PWMXBAR7_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR7_G6_SEL	R/W	0h	PWM XBAR7 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.82 CONTROLSS_PWMXBAR7_G7 Register

3.15.2.82.1 CONTROLSS_PWMXBAR7_G7 Register (Offset = 2DCh) [reset = 0h]

PWM XBAR 7 Input Select.

Return to Summary Table

Table 3-1669. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12DCh

Figure 3-881. CONTROLSS_PWMXBAR7_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR7_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR7_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR7_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR7_G7_SEL							
R/W							
0h							

Table 3-1670. CONTROLSS_PWMXBAR7_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR7_G7_SEL	R/W	0h	PWM XBAR7 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.83 CONTROLSS_PWMXBAR7_G8 Register

3.15.2.83.1 CONTROLSS_PWMXBAR7_G8 Register (Offset = 2E0h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to Summary Table

Table 3-1671. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12E0h

Figure 3-882. CONTROLSS_PWMXBAR7_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR7_G8_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR7_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR7_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR7_G8_SEL							
R/W							
0h							

Table 3-1672. CONTROLSS_PWMXBAR7_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR7_G8_SEL	R/W	0h	PWM XBAR7 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.84 CONTROLSS_PWMXBAR7_G9 Register

3.15.2.84.1 CONTROLSS_PWMXBAR7_G9 Register (Offset = 2E4h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to Summary Table

Table 3-1673. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 12E4h

Figure 3-883. CONTROLSS_PWMXBAR7_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR7_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1674. CONTROLSS_PWMXBAR7_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR7_G9_SEL	R/W	0h	PWM XBAR7 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.85 CONTROLSS_PWMXBAR8_G0 Register

3.15.2.85.1 CONTROLSS_PWMXBAR8_G0 Register (Offset = 300h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to Summary Table

Table 3-1675. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1300h

Figure 3-884. CONTROLSS_PWMXBAR8_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR8_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR8_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR8_G0_SEL							
R/W							
0h							

Table 3-1676. CONTROLSS_PWMXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1676. CONTROLSS_PWMXBAR8_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR8_G0_SEL	R/W	0h	PWM XBAR8 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.86 CONTROLSS_PWMXBAR8_G1 Register

3.15.2.86.1 CONTROLSS_PWMXBAR8_G1 Register (Offset = 304h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to Summary Table

Table 3-1677. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1304h

Figure 3-885. CONTROLSS_PWMXBAR8_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR8_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR8_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR8_G1_SEL							
R/W							
0h							

Table 3-1678. CONTROLSS_PWMXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1678. CONTROLSS_PWMXBAR8_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR8_G1_SEL	R/W	0h	PWM XBAR8 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.87 CONTROLSS_PWMXBAR8_G2 Register

3.15.2.87.1 CONTROLSS_PWMXBAR8_G2 Register (Offset = 308h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to Summary Table

Table 3-1679. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1308h

Figure 3-886. CONTROLSS_PWMXBAR8_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR8_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR8_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR8_G2_SEL							
R/W							
0h							

Table 3-1680. CONTROLSS_PWMXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1680. CONTROLSS_PWMXBAR8_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR8_G2_SEL	R/W	0h	PWM XBAR8 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.88 CONTROLSS_PWMXBAR8_G3 Register

3.15.2.88.1 CONTROLSS_PWMXBAR8_G3 Register (Offset = 30Ch) [reset = 0h]

PWM XBAR 8 Input Select.

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Table 3-1681. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 130Ch

Figure 3-887. CONTROLSS_PWMXBAR8_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR8_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR8_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR8_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR8_G3_SEL							
R/W							
0h							

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Table 3-1682. CONTROLSS_PWMXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR8_G3_SEL	R/W	0h	PWM XBAR8 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.89 CONTROLSS_PWMXBAR8_G4 Register

3.15.2.89.1 CONTROLSS_PWMXBAR8_G4 Register (Offset = 310h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to Summary Table

Table 3-1683. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1310h

Figure 3-888. CONTROLSS_PWMXBAR8_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR8_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR8_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR8_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR8_G4_SEL							
R/W							
0h							

Table 3-1684. CONTROLSS_PWMXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR8_G4_SEL	R/W	0h	PWM XBAR8 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.90 CONTROLSS_PWMXBAR8_G5 Register

3.15.2.90.1 CONTROLSS_PWMXBAR8_G5 Register (Offset = 314h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to Summary Table

Table 3-1685. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1314h

Figure 3-889. CONTROLSS_PWMXBAR8_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR8_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR8_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR8_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR8_G5_SEL							
R/W							
0h							

Table 3-1686. CONTROLSS_PWMXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR8_G5_SEL	R/W	0h	PWM XBAR8 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.91 CONTROLSS_PWMXBAR8_G6 Register

3.15.2.91.1 CONTROLSS_PWMXBAR8_G6 Register (Offset = 318h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to Summary Table

Table 3-1687. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1318h

Figure 3-890. CONTROLSS_PWMXBAR8_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR8_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR8_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR8_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR8_G6_SEL							
R/W							
0h							

Table 3-1688. CONTROLSS_PWMXBAR8_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR8_G6_SEL	R/W	0h	PWM XBAR8 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.92 CONTROLSS_PWMXBAR8_G7 Register

3.15.2.92.1 CONTROLSS_PWMXBAR8_G7 Register (Offset = 31Ch) [reset = 0h]

PWM XBAR 8 Input Select.

Return to Summary Table

Table 3-1689. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 131Ch

Figure 3-891. CONTROLSS_PWMXBAR8_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR8_G7_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR8_G7_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR8_G7_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR8_G7_SEL							
R/W							
0h							

Table 3-1690. CONTROLSS_PWMXBAR8_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR8_G7_SEL	R/W	0h	PWM XBAR8 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.93 CONTROLSS_PWMXBAR8_G8 Register

3.15.2.93.1 CONTROLSS_PWMXBAR8_G8 Register (Offset = 320h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to Summary Table

Table 3-1691. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1320h

Figure 3-892. CONTROLSS_PWMXBAR8_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR8_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR8_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR8_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR8_G8_SEL							
R/W							
0h							

Table 3-1692. CONTROLSS_PWMXBAR8_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR8_G8_SEL	R/W	0h	PWM XBAR8 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.94 CONTROLSS_PWMXBAR8_G9 Register

3.15.2.94.1 CONTROLSS_PWMXBAR8_G9 Register (Offset = 324h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to Summary Table

Table 3-1693. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1324h

Figure 3-893. CONTROLSS_PWMXBAR8_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR8_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1694. CONTROLSS_PWMXBAR8_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR8_G9_SEL	R/W	0h	PWM XBAR8 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.95 CONTROLSS_PWMXBAR9_G0 Register

3.15.2.95.1 CONTROLSS_PWMXBAR9_G0 Register (Offset = 340h) [reset = 0h]

PWM XBAR 9 Input Select.

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Table 3-1695. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1340h

Figure 3-894. CONTROLSS_PWMXBAR9_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR9_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR9_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR9_G0_SEL							
R/W							
0h							

Table 3-1696. CONTROLSS_PWMXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1696. CONTROLSS_PWMXBAR9_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR9_G0_SEL	R/W	0h	PWM XBAR9 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.96 CONTROLSS_PWMXBAR9_G1 Register

3.15.2.96.1 CONTROLSS_PWMXBAR9_G1 Register (Offset = 344h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to Summary Table

Table 3-1697. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1344h

Figure 3-895. CONTROLSS_PWMXBAR9_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR9_G1_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR9_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR9_G1_SEL							
R/W							
0h							

Table 3-1698. CONTROLSS_PWMXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1698. CONTROLSS_PWMXBAR9_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR9_G1_SEL	R/W	0h	PWM XBAR9 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.97 CONTROLSS_PWMXBAR9_G2 Register

3.15.2.97.1 CONTROLSS_PWMXBAR9_G2 Register (Offset = 348h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to Summary Table

Table 3-1699. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1348h

Figure 3-896. CONTROLSS_PWMXBAR9_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR9_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR9_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR9_G2_SEL							
R/W							
0h							

Table 3-1700. CONTROLSS_PWMXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1700. CONTROLSS_PWMXBAR9_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR9_G2_SEL	R/W	0h	PWM XBAR9 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.98 CONTROLSS_PWMXBAR9_G3 Register

3.15.2.98.1 CONTROLSS_PWMXBAR9_G3 Register (Offset = 34Ch) [reset = 0h]

PWM XBAR 9 Input Select.

Return to Summary Table

Table 3-1701. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 134Ch

Figure 3-897. CONTROLSS_PWMXBAR9_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR9_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR9_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR9_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR9_G3_SEL							
R/W							
0h							

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Table 3-1702. CONTROLSS_PWMXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR9_G3_SEL	R/W	0h	PWM XBAR9 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.99 CONTROLSS_PWMXBAR9_G4 Register

3.15.2.99.1 CONTROLSS_PWMXBAR9_G4 Register (Offset = 350h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to Summary Table

Table 3-1703. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1350h

Figure 3-898. CONTROLSS_PWMXBAR9_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR9_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR9_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR9_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR9_G4_SEL							
R/W							
0h							

Table 3-1704. CONTROLSS_PWMXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR9_G4_SEL	R/W	0h	PWM XBAR9 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.100 CONTROLSS_PWMXBAR9_G5 Register

3.15.2.100.1 CONTROLSS_PWMXBAR9_G5 Register (Offset = 354h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to Summary Table

Table 3-1705. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1354h

Figure 3-899. CONTROLSS_PWMXBAR9_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR9_G5_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR9_G5_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR9_G5_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR9_G5_SEL							
R/W							
0h							

Table 3-1706. CONTROLSS_PWMXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR9_G5_SEL	R/W	0h	PWM XBAR9 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.101 CONTROLSS_PWMXBAR9_G6 Register

3.15.2.101.1 CONTROLSS_PWMXBAR9_G6 Register (Offset = 358h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to Summary Table

Table 3-1707. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1358h

Figure 3-900. CONTROLSS_PWMXBAR9_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR9_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR9_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR9_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR9_G6_SEL							
R/W							
0h							

Table 3-1708. CONTROLSS_PWMXBAR9_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR9_G6_SEL	R/W	0h	PWM XBAR9 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.102 CONTROLSS_PWMXBAR9_G7 Register

3.15.2.102.1 CONTROLSS_PWMXBAR9_G7 Register (Offset = 35Ch) [reset = 0h]

PWM XBAR 9 Input Select.

Return to Summary Table

Table 3-1709. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 135Ch

Figure 3-901. CONTROLSS_PWMXBAR9_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR9_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR9_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR9_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR9_G7_SEL							
R/W							
0h							

Table 3-1710. CONTROLSS_PWMXBAR9_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR9_G7_SEL	R/W	0h	PWM XBAR9 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.103 CONTROLSS_PWMXBAR9_G8 Register

3.15.2.103.1 CONTROLSS_PWMXBAR9_G8 Register (Offset = 360h) [reset = 0h]

PWM XBAR 9 Input Select.

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Table 3-1711. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1360h

Figure 3-902. CONTROLSS_PWMXBAR9_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR9_G8_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR9_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR9_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR9_G8_SEL							
R/W							
0h							

Table 3-1712. CONTROLSS_PWMXBAR9_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR9_G8_SEL	R/W	0h	PWM XBAR9 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.104 CONTROLSS_PWMXBAR9_G9 Register

3.15.2.104.1 CONTROLSS_PWMXBAR9_G9 Register (Offset = 364h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to Summary Table

Table 3-1713. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1364h

Figure 3-903. CONTROLSS_PWMXBAR9_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR9_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1714. CONTROLSS_PWMXBAR9_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR9_G9_SEL	R/W	0h	PWM XBAR9 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.105 CONTROLSS_PWMXBAR10_G0 Register

3.15.2.105.1 CONTROLSS_PWMXBAR10_G0 Register (Offset = 380h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to Summary Table

Table 3-1715. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1380h

Figure 3-904. CONTROLSS_PWMXBAR10_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR10_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR10_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR10_G0_SEL							
R/W							
0h							

Table 3-1716. CONTROLSS_PWMXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1716. CONTROLSS_PWMXBAR10_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR10_G0_SEL	R/W	0h	PWM XBAR10 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.106 CONTROLSS_PWMXBAR10_G1 Register

3.15.2.106.1 CONTROLSS_PWMXBAR10_G1 Register (Offset = 384h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to Summary Table

Table 3-1717. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1384h

Figure 3-905. CONTROLSS_PWMXBAR10_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR10_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR10_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR10_G1_SEL							
R/W							
0h							

Table 3-1718. CONTROLSS_PWMXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1718. CONTROLSS_PWMXBAR10_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR10_G1_SEL	R/W	0h	PWM XBAR10 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.107 CONTROLSS_PWMXBAR10_G2 Register

3.15.2.107.1 CONTROLSS_PWMXBAR10_G2 Register (Offset = 388h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to Summary Table

Table 3-1719. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1388h

Figure 3-906. CONTROLSS_PWMXBAR10_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR10_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR10_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR10_G2_SEL							
R/W							
0h							

Table 3-1720. CONTROLSS_PWMXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1720. CONTROLSS_PWMXBAR10_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR10_G2_SEL	R/W	0h	PWM XBAR10 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.108 CONTROLSS_PWMXBAR10_G3 Register

3.15.2.108.1 CONTROLSS_PWMXBAR10_G3 Register (Offset = 38Ch) [reset = 0h]

PWM XBAR 10 Input Select.

Return to Summary Table

Table 3-1721. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 138Ch

Figure 3-907. CONTROLSS_PWMXBAR10_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR10_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR10_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR10_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR10_G3_SEL							
R/W							
0h							

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Table 3-1722. CONTROLSS_PWMXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR10_G3_SEL	R/W	0h	PWM XBAR10 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.109 CONTROLSS_PWMXBAR10_G4 Register

3.15.2.109.1 CONTROLSS_PWMXBAR10_G4 Register (Offset = 390h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to Summary Table

Table 3-1723. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1390h

Figure 3-908. CONTROLSS_PWMXBAR10_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR10_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR10_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR10_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR10_G4_SEL							
R/W							
0h							

Table 3-1724. CONTROLSS_PWMXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR10_G4_SEL	R/W	0h	PWM XBAR10 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.110 CONTROLSS_PWMXBAR10_G5 Register

3.15.2.110.1 CONTROLSS_PWMXBAR10_G5 Register (Offset = 394h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to Summary Table

Table 3-1725. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1394h

Figure 3-909. CONTROLSS_PWMXBAR10_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR10_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR10_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR10_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR10_G5_SEL							
R/W							
0h							

Table 3-1726. CONTROLSS_PWMXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR10_G5_SEL	R/W	0h	PWM XBAR10 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.111 CONTROLSS_PWMXBAR10_G6 Register

3.15.2.111.1 CONTROLSS_PWMXBAR10_G6 Register (Offset = 398h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to Summary Table

Table 3-1727. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1398h

Figure 3-910. CONTROLSS_PWMXBAR10_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR10_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR10_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR10_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR10_G6_SEL							
R/W							
0h							

Table 3-1728. CONTROLSS_PWMXBAR10_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR10_G6_SEL	R/W	0h	PWM XBAR10 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.112 CONTROLSS_PWMXBAR10_G7 Register

3.15.2.112.1 CONTROLSS_PWMXBAR10_G7 Register (Offset = 39Ch) [reset = 0h]

PWM XBAR 10 Input Select.

Return to Summary Table

Table 3-1729. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 139Ch

Figure 3-911. CONTROLSS_PWMXBAR10_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR10_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR10_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR10_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR10_G7_SEL							
R/W							
0h							

Table 3-1730. CONTROLSS_PWMXBAR10_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR10_G7_SEL	R/W	0h	PWM XBAR10 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.113 CONTROLSS_PWMXBAR10_G8 Register

3.15.2.113.1 CONTROLSS_PWMXBAR10_G8 Register (Offset = 3A0h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to Summary Table

Table 3-1731. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13A0h

Figure 3-912. CONTROLSS_PWMXBAR10_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR10_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR10_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR10_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR10_G8_SEL							
R/W							
0h							

Table 3-1732. CONTROLSS_PWMXBAR10_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR10_G8_SEL	R/W	0h	PWM XBAR10 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.114 CONTROLSS_PWMXBAR10_G9 Register

3.15.2.114.1 CONTROLSS_PWMXBAR10_G9 Register (Offset = 3A4h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to Summary Table

Table 3-1733. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13A4h

Figure 3-913. CONTROLSS_PWMXBAR10_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PWMXBAR10_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1734. CONTROLSS_PWMXBAR10_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR10_G9_SEL	R/W	0h	PWM XBAR10 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.115 CONTROLSS_PWMXBAR11_G0 Register

3.15.2.115.1 CONTROLSS_PWMXBAR11_G0 Register (Offset = 3C0h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to Summary Table

Table 3-1735. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13C0h

Figure 3-914. CONTROLSS_PWMXBAR11_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR11_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR11_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR11_G0_SEL							
R/W							
0h							

Table 3-1736. CONTROLSS_PWMXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1736. CONTROLSS_PWMXBAR11_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR11_G0_SEL	R/W	0h	PWM XBAR11 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.116 CONTROLSS_PWMXBAR11_G1 Register

3.15.2.116.1 CONTROLSS_PWMXBAR11_G1 Register (Offset = 3C4h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to Summary Table

Table 3-1737. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13C4h

Figure 3-915. CONTROLSS_PWMXBAR11_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR11_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR11_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR11_G1_SEL							
R/W							
0h							

Table 3-1738. CONTROLSS_PWMXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1738. CONTROLSS_PWMXBAR11_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR11_G1_SEL	R/W	0h	PWM XBAR11 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.117 CONTROLSS_PWMXBAR11_G2 Register

3.15.2.117.1 CONTROLSS_PWMXBAR11_G2 Register (Offset = 3C8h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to Summary Table

Table 3-1739. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13C8h

Figure 3-916. CONTROLSS_PWMXBAR11_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR11_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR11_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR11_G2_SEL							
R/W							
0h							

Table 3-1740. CONTROLSS_PWMXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1740. CONTROLSS_PWMXBAR11_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR11_G2_SEL	R/W	0h	PWM XBAR11 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.118 CONTROLSS_PWMXBAR11_G3 Register

3.15.2.118.1 CONTROLSS_PWMXBAR11_G3 Register (Offset = 3CCh) [reset = 0h]

PWM XBAR 11 Input Select.

Return to Summary Table

Table 3-1741. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13CCh

Figure 3-917. CONTROLSS_PWMXBAR11_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR11_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR11_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR11_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR11_G3_SEL							
R/W							
0h							

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Table 3-1742. CONTROLSS_PWMXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR11_G3_SEL	R/W	0h	PWM XBAR11 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.119 CONTROLSS_PWMXBAR11_G4 Register

3.15.2.119.1 CONTROLSS_PWMXBAR11_G4 Register (Offset = 3D0h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to Summary Table

Table 3-1743. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13D0h

Figure 3-918. CONTROLSS_PWMXBAR11_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR11_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR11_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR11_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR11_G4_SEL							
R/W							
0h							

Table 3-1744. CONTROLSS_PWMXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR11_G4_SEL	R/W	0h	PWM XBAR11 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.120 CONTROLSS_PWMXBAR11_G5 Register

3.15.2.120.1 CONTROLSS_PWMXBAR11_G5 Register (Offset = 3D4h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to Summary Table

Table 3-1745. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13D4h

Figure 3-919. CONTROLSS_PWMXBAR11_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR11_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR11_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR11_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR11_G5_SEL							
R/W							
0h							

Table 3-1746. CONTROLSS_PWMXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR11_G5_SEL	R/W	0h	PWM XBAR11 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.121 CONTROLSS_PWMXBAR11_G6 Register

3.15.2.121.1 CONTROLSS_PWMXBAR11_G6 Register (Offset = 3D8h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to Summary Table

Table 3-1747. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13D8h

Figure 3-920. CONTROLSS_PWMXBAR11_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR11_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR11_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR11_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR11_G6_SEL							
R/W							
0h							

Table 3-1748. CONTROLSS_PWMXBAR11_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR11_G6_SEL	R/W	0h	PWM XBAR11 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.122 CONTROLSS_PWMXBAR11_G7 Register

3.15.2.122.1 CONTROLSS_PWMXBAR11_G7 Register (Offset = 3DCh) [reset = 0h]

PWM XBAR 11 Input Select.

Return to Summary Table

Table 3-1749. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13DCh

Figure 3-921. CONTROLSS_PWMXBAR11_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR11_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR11_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR11_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR11_G7_SEL							
R/W							
0h							

Table 3-1750. CONTROLSS_PWMXBAR11_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR11_G7_SEL	R/W	0h	PWM XBAR11 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.123 CONTROLSS_PWMXBAR11_G8 Register

3.15.2.123.1 CONTROLSS_PWMXBAR11_G8 Register (Offset = 3E0h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to Summary Table

Table 3-1751. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13E0h

Figure 3-922. CONTROLSS_PWMXBAR11_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR11_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR11_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR11_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR11_G8_SEL							
R/W							
0h							

Table 3-1752. CONTROLSS_PWMXBAR11_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR11_G8_SEL	R/W	0h	PWM XBAR11 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.124 CONTROLSS_PWMXBAR11_G9 Register

3.15.2.124.1 CONTROLSS_PWMXBAR11_G9 Register (Offset = 3E4h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to Summary Table

Table 3-1753. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 13E4h

Figure 3-923. CONTROLSS_PWMXBAR11_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR11_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1754. CONTROLSS_PWMXBAR11_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR11_G9_SEL	R/W	0h	PWM XBAR11 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.125 CONTROLSS_PWMXBAR12_G0 Register

3.15.2.125.1 CONTROLSS_PWMXBAR12_G0 Register (Offset = 400h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to Summary Table

Table 3-1755. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1400h

Figure 3-924. CONTROLSS_PWMXBAR12_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR12_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR12_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR12_G0_SEL							
R/W							
0h							

Table 3-1756. CONTROLSS_PWMXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1756. CONTROLSS_PWMXBAR12_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR12_G0_SEL	R/W	0h	PWM XBAR12 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.126 CONTROLSS_PWMXBAR12_G1 Register

3.15.2.126.1 CONTROLSS_PWMXBAR12_G1 Register (Offset = 404h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to Summary Table

Table 3-1757. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1404h

Figure 3-925. CONTROLSS_PWMXBAR12_G1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PWMXBAR12_G1_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PWMXBAR12_G1_SEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PWMXBAR12_G1_SEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 3-1758. CONTROLSS_PWMXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1758. CONTROLSS_PWMXBAR12_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR12_G1_SEL	R/W	0h	PWM XBAR12 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.127 CONTROLSS_PWMXBAR12_G2 Register

3.15.2.127.1 CONTROLSS_PWMXBAR12_G2 Register (Offset = 408h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to Summary Table

Table 3-1759. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1408h

Figure 3-926. CONTROLSS_PWMXBAR12_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR12_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR12_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR12_G2_SEL							
R/W							
0h							

Table 3-1760. CONTROLSS_PWMXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1760. CONTROLSS_PWMXBAR12_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR12_G2_SEL	R/W	0h	PWM XBAR12 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.128 CONTROLSS_PWMXBAR12_G3 Register

3.15.2.128.1 CONTROLSS_PWMXBAR12_G3 Register (Offset = 40Ch) [reset = 0h]

PWM XBAR 12 Input Select.

Return to Summary Table

Table 3-1761. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 140Ch

Figure 3-927. CONTROLSS_PWMXBAR12_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR12_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR12_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR12_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR12_G3_SEL							
R/W							
0h							

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Table 3-1762. CONTROLSS_PWMXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR12_G3_SEL	R/W	0h	PWM XBAR12 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.129 CONTROLSS_PWMXBAR12_G4 Register

3.15.2.129.1 CONTROLSS_PWMXBAR12_G4 Register (Offset = 410h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to Summary Table

Table 3-1763. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1410h

Figure 3-928. CONTROLSS_PWMXBAR12_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR12_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR12_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR12_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR12_G4_SEL							
R/W							
0h							

Table 3-1764. CONTROLSS_PWMXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR12_G4_SEL	R/W	0h	PWM XBAR12 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.130 CONTROLSS_PWMXBAR12_G5 Register

3.15.2.130.1 CONTROLSS_PWMXBAR12_G5 Register (Offset = 414h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to Summary Table

Table 3-1765. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1414h

Figure 3-929. CONTROLSS_PWMXBAR12_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR12_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR12_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR12_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR12_G5_SEL							
R/W							
0h							

Table 3-1766. CONTROLSS_PWMXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR12_G5_SEL	R/W	0h	PWM XBAR12 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.131 CONTROLSS_PWMXBAR12_G6 Register

3.15.2.131.1 CONTROLSS_PWMXBAR12_G6 Register (Offset = 418h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to Summary Table

Table 3-1767. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1418h

Figure 3-930. CONTROLSS_PWMXBAR12_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR12_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR12_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR12_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR12_G6_SEL							
R/W							
0h							

Table 3-1768. CONTROLSS_PWMXBAR12_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR12_G6_SEL	R/W	0h	PWM XBAR12 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.132 CONTROLSS_PWMXBAR12_G7 Register

3.15.2.132.1 CONTROLSS_PWMXBAR12_G7 Register (Offset = 41Ch) [reset = 0h]

PWM XBAR 12 Input Select.

Return to Summary Table

Table 3-1769. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 141Ch

Figure 3-931. CONTROLSS_PWMXBAR12_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR12_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR12_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR12_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR12_G7_SEL							
R/W							
0h							

Table 3-1770. CONTROLSS_PWMXBAR12_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR12_G7_SEL	R/W	0h	PWM XBAR12 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.133 CONTROLSS_PWMXBAR12_G8 Register

3.15.2.133.1 CONTROLSS_PWMXBAR12_G8 Register (Offset = 420h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to Summary Table

Table 3-1771. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1420h

Figure 3-932. CONTROLSS_PWMXBAR12_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR12_G8_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR12_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR12_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR12_G8_SEL							
R/W							
0h							

Table 3-1772. CONTROLSS_PWMXBAR12_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR12_G8_SEL	R/W	0h	PWM XBAR12 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.134 CONTROLSS_PWMXBAR12_G9 Register

3.15.2.134.1 CONTROLSS_PWMXBAR12_G9 Register (Offset = 424h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to Summary Table

Table 3-1773. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1424h

Figure 3-933. CONTROLSS_PWMXBAR12_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR12_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1774. CONTROLSS_PWMXBAR12_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR12_G9_SEL	R/W	0h	PWM XBAR12 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.135 CONTROLSS_PWMXBAR13_G0 Register

3.15.2.135.1 CONTROLSS_PWMXBAR13_G0 Register (Offset = 440h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to Summary Table

Table 3-1775. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1440h

Figure 3-934. CONTROLSS_PWMXBAR13_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR13_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR13_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR13_G0_SEL							
R/W							
0h							

Table 3-1776. CONTROLSS_PWMXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1776. CONTROLSS_PWMXBAR13_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR13_G0_SEL	R/W	0h	PWM XBAR13 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.136 CONTROLSS_PWMXBAR13_G1 Register

3.15.2.136.1 CONTROLSS_PWMXBAR13_G1 Register (Offset = 444h) [reset = 0h]

PWM XBAR 13 Input Select.

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Table 3-1777. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1444h

Figure 3-935. CONTROLSS_PWMXBAR13_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR13_G1_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR13_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR13_G1_SEL							
R/W							
0h							

Table 3-1778. CONTROLSS_PWMXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1778. CONTROLSS_PWMXBAR13_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR13_G1_SEL	R/W	0h	PWM XBAR13 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.137 CONTROLSS_PWMXBAR13_G2 Register

3.15.2.137.1 CONTROLSS_PWMXBAR13_G2 Register (Offset = 448h) [reset = 0h]

PWM XBAR 13 Input Select.

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Table 3-1779. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1448h

Figure 3-936. CONTROLSS_PWMXBAR13_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR13_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR13_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR13_G2_SEL							
R/W							
0h							

Table 3-1780. CONTROLSS_PWMXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1780. CONTROLSS_PWMXBAR13_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR13_G2_SEL	R/W	0h	PWM XBAR13 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.138 CONTROLSS_PWMXBAR13_G3 Register

3.15.2.138.1 CONTROLSS_PWMXBAR13_G3 Register (Offset = 44Ch) [reset = 0h]

PWM XBAR 13 Input Select.

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Table 3-1781. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 144Ch

Figure 3-937. CONTROLSS_PWMXBAR13_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR13_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR13_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR13_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR13_G3_SEL							
R/W							
0h							

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Table 3-1782. CONTROLSS_PWMXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR13_G3_SEL	R/W	0h	PWM XBAR13 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.139 CONTROLSS_PWMXBAR13_G4 Register

3.15.2.139.1 CONTROLSS_PWMXBAR13_G4 Register (Offset = 450h) [reset = 0h]

PWM XBAR 13 Input Select.

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Table 3-1783. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1450h

Figure 3-938. CONTROLSS_PWMXBAR13_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR13_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR13_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR13_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR13_G4_SEL							
R/W							
0h							

Table 3-1784. CONTROLSS_PWMXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR13_G4_SEL	R/W	0h	PWM XBAR13 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.140 CONTROLSS_PWMXBAR13_G5 Register

3.15.2.140.1 CONTROLSS_PWMXBAR13_G5 Register (Offset = 454h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to Summary Table

Table 3-1785. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1454h

Figure 3-939. CONTROLSS_PWMXBAR13_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR13_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR13_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR13_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR13_G5_SEL							
R/W							
0h							

Table 3-1786. CONTROLSS_PWMXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR13_G5_SEL	R/W	0h	PWM XBAR13 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.141 CONTROLSS_PWMXBAR13_G6 Register

3.15.2.141.1 CONTROLSS_PWMXBAR13_G6 Register (Offset = 458h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to Summary Table

Table 3-1787. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1458h

Figure 3-940. CONTROLSS_PWMXBAR13_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR13_G6_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR13_G6_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR13_G6_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR13_G6_SEL							
R/W							
0h							

Table 3-1788. CONTROLSS_PWMXBAR13_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR13_G6_SEL	R/W	0h	PWM XBAR13 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.142 CONTROLSS_PWMXBAR13_G7 Register

3.15.2.142.1 CONTROLSS_PWMXBAR13_G7 Register (Offset = 45Ch) [reset = 0h]

PWM XBAR 13 Input Select.

Return to Summary Table

Table 3-1789. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 145Ch

Figure 3-941. CONTROLSS_PWMXBAR13_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR13_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR13_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR13_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR13_G7_SEL							
R/W							
0h							

Table 3-1790. CONTROLSS_PWMXBAR13_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR13_G7_SEL	R/W	0h	PWM XBAR13 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.143 CONTROLSS_PWMXBAR13_G8 Register

3.15.2.143.1 CONTROLSS_PWMXBAR13_G8 Register (Offset = 460h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to Summary Table

Table 3-1791. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1460h

Figure 3-942. CONTROLSS_PWMXBAR13_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR13_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR13_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR13_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR13_G8_SEL							
R/W							
0h							

Table 3-1792. CONTROLSS_PWMXBAR13_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR13_G8_SEL	R/W	0h	PWM XBAR13 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.144 CONTROLSS_PWMXBAR13_G9 Register

3.15.2.144.1 CONTROLSS_PWMXBAR13_G9 Register (Offset = 464h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to Summary Table

Table 3-1793. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1464h

Figure 3-943. CONTROLSS_PWMXBAR13_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR13_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1794. CONTROLSS_PWMXBAR13_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR13_G9_SEL	R/W	0h	PWM XBAR13 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.145 CONTROLSS_PWMXBAR14_G0 Register

3.15.2.145.1 CONTROLSS_PWMXBAR14_G0 Register (Offset = 480h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to Summary Table

Table 3-1795. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1480h

Figure 3-944. CONTROLSS_PWMXBAR14_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR14_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR14_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR14_G0_SEL							
R/W							
0h							

Table 3-1796. CONTROLSS_PWMXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1796. CONTROLSS_PWMXBAR14_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR14_G0_SEL	R/W	0h	PWM XBAR14 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.146 CONTROLSS_PWMXBAR14_G1 Register

3.15.2.146.1 CONTROLSS_PWMXBAR14_G1 Register (Offset = 484h) [reset = 0h]

PWM XBAR 14 Input Select.

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Table 3-1797. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1484h

Figure 3-945. CONTROLSS_PWMXBAR14_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR14_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR14_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR14_G1_SEL							
R/W							
0h							

Table 3-1798. CONTROLSS_PWMXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1798. CONTROLSS_PWMXBAR14_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR14_G1_SEL	R/W	0h	PWM XBAR14 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.147 CONTROLSS_PWMXBAR14_G2 Register

3.15.2.147.1 CONTROLSS_PWMXBAR14_G2 Register (Offset = 488h) [reset = 0h]

PWM XBAR 14 Input Select.

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Table 3-1799. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1488h

Figure 3-946. CONTROLSS_PWMXBAR14_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR14_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR14_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR14_G2_SEL							
R/W							
0h							

Table 3-1800. CONTROLSS_PWMXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1800. CONTROLSS_PWMXBAR14_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR14_G2_SEL	R/W	0h	PWM XBAR14 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.148 CONTROLSS_PWMXBAR14_G3 Register

3.15.2.148.1 CONTROLSS_PWMXBAR14_G3 Register (Offset = 48Ch) [reset = 0h]

PWM XBAR 14 Input Select.

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Table 3-1801. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 148Ch

Figure 3-947. CONTROLSS_PWMXBAR14_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR14_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR14_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR14_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR14_G3_SEL							
R/W							
0h							

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Table 3-1802. CONTROLSS_PWMXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR14_G3_SEL	R/W	0h	PWM XBAR14 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.149 CONTROLSS_PWMXBAR14_G4 Register

3.15.2.149.1 CONTROLSS_PWMXBAR14_G4 Register (Offset = 490h) [reset = 0h]

PWM XBAR 14 Input Select.

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Table 3-1803. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1490h

Figure 3-948. CONTROLSS_PWMXBAR14_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR14_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR14_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR14_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR14_G4_SEL							
R/W							
0h							

Table 3-1804. CONTROLSS_PWMXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR14_G4_SEL	R/W	0h	PWM XBAR14 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.150 CONTROLSS_PWMXBAR14_G5 Register

3.15.2.150.1 CONTROLSS_PWMXBAR14_G5 Register (Offset = 494h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to Summary Table

Table 3-1805. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1494h

Figure 3-949. CONTROLSS_PWMXBAR14_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR14_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR14_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR14_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR14_G5_SEL							
R/W							
0h							

Table 3-1806. CONTROLSS_PWMXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR14_G5_SEL	R/W	0h	PWM XBAR14 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.151 CONTROLSS_PWMXBAR14_G6 Register

3.15.2.151.1 CONTROLSS_PWMXBAR14_G6 Register (Offset = 498h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to Summary Table

Table 3-1807. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1498h

Figure 3-950. CONTROLSS_PWMXBAR14_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR14_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR14_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR14_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR14_G6_SEL							
R/W							
0h							

Table 3-1808. CONTROLSS_PWMXBAR14_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR14_G6_SEL	R/W	0h	PWM XBAR14 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.152 CONTROLSS_PWMXBAR14_G7 Register

3.15.2.152.1 CONTROLSS_PWMXBAR14_G7 Register (Offset = 49Ch) [reset = 0h]

PWM XBAR 14 Input Select.

Return to Summary Table

Table 3-1809. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 149Ch

Figure 3-951. CONTROLSS_PWMXBAR14_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR14_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR14_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR14_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR14_G7_SEL							
R/W							
0h							

Table 3-1810. CONTROLSS_PWMXBAR14_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR14_G7_SEL	R/W	0h	PWM XBAR14 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.153 CONTROLSS_PWMXBAR14_G8 Register

3.15.2.153.1 CONTROLSS_PWMXBAR14_G8 Register (Offset = 4A0h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to Summary Table

Table 3-1811. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14A0h

Figure 3-952. CONTROLSS_PWMXBAR14_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR14_G8_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR14_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR14_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR14_G8_SEL							
R/W							
0h							

Table 3-1812. CONTROLSS_PWMXBAR14_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR14_G8_SEL	R/W	0h	PWM XBAR14 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.154 CONTROLSS_PWMXBAR14_G9 Register

3.15.2.154.1 CONTROLSS_PWMXBAR14_G9 Register (Offset = 4A4h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to Summary Table

Table 3-1813. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14A4h

Figure 3-953. CONTROLSS_PWMXBAR14_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR14_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1814. CONTROLSS_PWMXBAR14_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR14_G9_SEL	R/W	0h	PWM XBAR14 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.155 CONTROLSS_PWMXBAR15_G0 Register

3.15.2.155.1 CONTROLSS_PWMXBAR15_G0 Register (Offset = 4C0h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to Summary Table

Table 3-1815. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14C0h

Figure 3-954. CONTROLSS_PWMXBAR15_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR15_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR15_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR15_G0_SEL							
R/W							
0h							

Table 3-1816. CONTROLSS_PWMXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1816. CONTROLSS_PWMXBAR15_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR15_G0_SEL	R/W	0h	PWM XBAR15 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.156 CONTROLSS_PWMXBAR15_G1 Register

3.15.2.156.1 CONTROLSS_PWMXBAR15_G1 Register (Offset = 4C4h) [reset = 0h]

PWM XBAR 15 Input Select.

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Table 3-1817. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14C4h

Figure 3-955. CONTROLSS_PWMXBAR15_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR15_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR15_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR15_G1_SEL							
R/W							
0h							

Table 3-1818. CONTROLSS_PWMXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1818. CONTROLSS_PWMXBAR15_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR15_G1_SEL	R/W	0h	PWM XBAR15 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.157 CONTROLSS_PWMXBAR15_G2 Register

3.15.2.157.1 CONTROLSS_PWMXBAR15_G2 Register (Offset = 4C8h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to Summary Table

Table 3-1819. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14C8h

Figure 3-956. CONTROLSS_PWMXBAR15_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR15_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR15_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR15_G2_SEL							
R/W							
0h							

Table 3-1820. CONTROLSS_PWMXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1820. CONTROLSS_PWMXBAR15_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR15_G2_SEL	R/W	0h	PWM XBAR15 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.158 CONTROLSS_PWMXBAR15_G3 Register

3.15.2.158.1 CONTROLSS_PWMXBAR15_G3 Register (Offset = 4CCh) [reset = 0h]

PWM XBAR 15 Input Select.

Return to Summary Table

Table 3-1821. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14CCh

Figure 3-957. CONTROLSS_PWMXBAR15_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR15_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR15_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR15_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR15_G3_SEL							
R/W							
0h							

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Table 3-1822. CONTROLSS_PWMXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR15_G3_SEL	R/W	0h	PWM XBAR15 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.159 CONTROLSS_PWMXBAR15_G4 Register

3.15.2.159.1 CONTROLSS_PWMXBAR15_G4 Register (Offset = 4D0h) [reset = 0h]

PWM XBAR 15 Input Select.

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Table 3-1823. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14D0h

Figure 3-958. CONTROLSS_PWMXBAR15_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR15_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR15_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR15_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR15_G4_SEL							
R/W							
0h							

Table 3-1824. CONTROLSS_PWMXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR15_G4_SEL	R/W	0h	PWM XBAR15 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.160 CONTROLSS_PWMXBAR15_G5 Register

3.15.2.160.1 CONTROLSS_PWMXBAR15_G5 Register (Offset = 4D4h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to Summary Table

Table 3-1825. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14D4h

Figure 3-959. CONTROLSS_PWMXBAR15_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR15_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR15_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR15_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR15_G5_SEL							
R/W							
0h							

Table 3-1826. CONTROLSS_PWMXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR15_G5_SEL	R/W	0h	PWM XBAR15 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.161 CONTROLSS_PWMXBAR15_G6 Register

3.15.2.161.1 CONTROLSS_PWMXBAR15_G6 Register (Offset = 4D8h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to Summary Table

Table 3-1827. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14D8h

Figure 3-960. CONTROLSS_PWMXBAR15_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR15_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR15_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR15_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR15_G6_SEL							
R/W							
0h							

Table 3-1828. CONTROLSS_PWMXBAR15_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR15_G6_SEL	R/W	0h	PWM XBAR15 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.162 CONTROLSS_PWMXBAR15_G7 Register

3.15.2.162.1 CONTROLSS_PWMXBAR15_G7 Register (Offset = 4DCh) [reset = 0h]

PWM XBAR 15 Input Select.

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Table 3-1829. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14DCh

Figure 3-961. CONTROLSS_PWMXBAR15_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR15_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR15_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR15_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR15_G7_SEL							
R/W							
0h							

Table 3-1830. CONTROLSS_PWMXBAR15_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR15_G7_SEL	R/W	0h	PWM XBAR15 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.163 CONTROLSS_PWMXBAR15_G8 Register

3.15.2.163.1 CONTROLSS_PWMXBAR15_G8 Register (Offset = 4E0h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to Summary Table

Table 3-1831. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14E0h

Figure 3-962. CONTROLSS_PWMXBAR15_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR15_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR15_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR15_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR15_G8_SEL							
R/W							
0h							

Table 3-1832. CONTROLSS_PWMXBAR15_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR15_G8_SEL	R/W	0h	PWM XBAR15 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.164 CONTROLSS_PWMXBAR15_G9 Register

3.15.2.164.1 CONTROLSS_PWMXBAR15_G9 Register (Offset = 4E4h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to Summary Table

Table 3-1833. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 14E4h

Figure 3-963. CONTROLSS_PWMXBAR15_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR15_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1834. CONTROLSS_PWMXBAR15_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR15_G9_SEL	R/W	0h	PWM XBAR15 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.165 CONTROLSS_PWMXBAR16_G0 Register

3.15.2.165.1 CONTROLSS_PWMXBAR16_G0 Register (Offset = 500h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to Summary Table

Table 3-1835. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1500h

Figure 3-964. CONTROLSS_PWMXBAR16_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR16_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR16_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR16_G0_SEL							
R/W							
0h							

Table 3-1836. CONTROLSS_PWMXBAR16_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1836. CONTROLSS_PWMXBAR16_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR16_G0_SEL	R/W	0h	PWM XBAR16 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.166 CONTROLSS_PWMXBAR16_G1 Register

3.15.2.166.1 CONTROLSS_PWMXBAR16_G1 Register (Offset = 504h) [reset = 0h]

PWM XBAR 16 Input Select.

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Table 3-1837. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1504h

Figure 3-965. CONTROLSS_PWMXBAR16_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR16_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR16_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR16_G1_SEL							
R/W							
0h							

Table 3-1838. CONTROLSS_PWMXBAR16_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1838. CONTROLSS_PWMXBAR16_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR16_G1_SEL	R/W	0h	PWM XBAR16 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.167 CONTROLSS_PWMXBAR16_G2 Register

3.15.2.167.1 CONTROLSS_PWMXBAR16_G2 Register (Offset = 508h) [reset = 0h]

PWM XBAR 16 Input Select.

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Table 3-1839. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1508h

Figure 3-966. CONTROLSS_PWMXBAR16_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR16_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR16_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR16_G2_SEL							
R/W							
0h							

Table 3-1840. CONTROLSS_PWMXBAR16_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1840. CONTROLSS_PWMXBAR16_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR16_G2_SEL	R/W	0h	PWM XBAR16 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.168 CONTROLSS_PWMXBAR16_G3 Register

3.15.2.168.1 CONTROLSS_PWMXBAR16_G3 Register (Offset = 50Ch) [reset = 0h]

PWM XBAR 16 Input Select.

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Table 3-1841. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 150Ch

Figure 3-967. CONTROLSS_PWMXBAR16_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR16_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR16_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR16_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR16_G3_SEL							
R/W							
0h							

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Table 3-1842. CONTROLSS_PWMXBAR16_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR16_G3_SEL	R/W	0h	PWM XBAR16 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.169 CONTROLSS_PWMXBAR16_G4 Register

3.15.2.169.1 CONTROLSS_PWMXBAR16_G4 Register (Offset = 510h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to Summary Table

Table 3-1843. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1510h

Figure 3-968. CONTROLSS_PWMXBAR16_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR16_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR16_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR16_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR16_G4_SEL							
R/W							
0h							

Table 3-1844. CONTROLSS_PWMXBAR16_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR16_G4_SEL	R/W	0h	PWM XBAR16 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.170 CONTROLSS_PWMXBAR16_G5 Register

3.15.2.170.1 CONTROLSS_PWMXBAR16_G5 Register (Offset = 514h) [reset = 0h]

PWM XBAR 16 Input Select.

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Table 3-1845. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1514h

Figure 3-969. CONTROLSS_PWMXBAR16_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR16_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR16_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR16_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR16_G5_SEL							
R/W							
0h							

Table 3-1846. CONTROLSS_PWMXBAR16_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR16_G5_SEL	R/W	0h	PWM XBAR16 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.171 CONTROLSS_PWMXBAR16_G6 Register

3.15.2.171.1 CONTROLSS_PWMXBAR16_G6 Register (Offset = 518h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to Summary Table

Table 3-1847. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1518h

Figure 3-970. CONTROLSS_PWMXBAR16_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR16_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR16_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR16_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR16_G6_SEL							
R/W							
0h							

Table 3-1848. CONTROLSS_PWMXBAR16_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR16_G6_SEL	R/W	0h	PWM XBAR16 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.172 CONTROLSS_PWMXBAR16_G7 Register

3.15.2.172.1 CONTROLSS_PWMXBAR16_G7 Register (Offset = 51Ch) [reset = 0h]

PWM XBAR 16 Input Select.

Return to Summary Table

Table 3-1849. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 151Ch

Figure 3-971. CONTROLSS_PWMXBAR16_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR16_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR16_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR16_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR16_G7_SEL							
R/W							
0h							

Table 3-1850. CONTROLSS_PWMXBAR16_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR16_G7_SEL	R/W	0h	PWM XBAR16 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.173 CONTROLSS_PWMXBAR16_G8 Register

3.15.2.173.1 CONTROLSS_PWMXBAR16_G8 Register (Offset = 520h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to Summary Table

Table 3-1851. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1520h

Figure 3-972. CONTROLSS_PWMXBAR16_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR16_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR16_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR16_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR16_G8_SEL							
R/W							
0h							

Table 3-1852. CONTROLSS_PWMXBAR16_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR16_G8_SEL	R/W	0h	PWM XBAR16 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.174 CONTROLSS_PWMXBAR16_G9 Register

3.15.2.174.1 CONTROLSS_PWMXBAR16_G9 Register (Offset = 524h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to Summary Table

Table 3-1853. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1524h

Figure 3-973. CONTROLSS_PWMXBAR16_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR16_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1854. CONTROLSS_PWMXBAR16_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR16_G9_SEL	R/W	0h	PWM XBAR16 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.175 CONTROLSS_PWMXBAR17_G0 Register

3.15.2.175.1 CONTROLSS_PWMXBAR17_G0 Register (Offset = 540h) [reset = 0h]

PWM XBAR 17 Input Select.

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Table 3-1855. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1540h

Figure 3-974. CONTROLSS_PWMXBAR17_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR17_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR17_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR17_G0_SEL							
R/W							
0h							

Table 3-1856. CONTROLSS_PWMXBAR17_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1856. CONTROLSS_PWMXBAR17_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR17_G0_SEL	R/W	0h	PWM XBAR17 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.176 CONTROLSS_PWMXBAR17_G1 Register

3.15.2.176.1 CONTROLSS_PWMXBAR17_G1 Register (Offset = 544h) [reset = 0h]

PWM XBAR 17 Input Select.

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Table 3-1857. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1544h

Figure 3-975. CONTROLSS_PWMXBAR17_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR17_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR17_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR17_G1_SEL							
R/W							
0h							

Table 3-1858. CONTROLSS_PWMXBAR17_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1858. CONTROLSS_PWMXBAR17_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR17_G1_SEL	R/W	0h	PWM XBAR17 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.177 CONTROLSS_PWMXBAR17_G2 Register

3.15.2.177.1 CONTROLSS_PWMXBAR17_G2 Register (Offset = 548h) [reset = 0h]

PWM XBAR 17 Input Select.

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Table 3-1859. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1548h

Figure 3-976. CONTROLSS_PWMXBAR17_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR17_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR17_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR17_G2_SEL							
R/W							
0h							

Table 3-1860. CONTROLSS_PWMXBAR17_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1860. CONTROLSS_PWMXBAR17_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR17_G2_SEL	R/W	0h	PWM XBAR17 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.178 CONTROLSS_PWMXBAR17_G3 Register

3.15.2.178.1 CONTROLSS_PWMXBAR17_G3 Register (Offset = 54Ch) [reset = 0h]

PWM XBAR 17 Input Select.

Return to Summary Table

Table 3-1861. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 154Ch

Figure 3-977. CONTROLSS_PWMXBAR17_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR17_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR17_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR17_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR17_G3_SEL							
R/W							
0h							

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Table 3-1862. CONTROLSS_PWMXBAR17_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR17_G3_SEL	R/W	0h	PWM XBAR17 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.179 CONTROLSS_PWMXBAR17_G4 Register

3.15.2.179.1 CONTROLSS_PWMXBAR17_G4 Register (Offset = 550h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to Summary Table

Table 3-1863. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1550h

Figure 3-978. CONTROLSS_PWMXBAR17_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR17_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR17_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR17_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR17_G4_SEL							
R/W							
0h							

Table 3-1864. CONTROLSS_PWMXBAR17_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR17_G4_SEL	R/W	0h	PWM XBAR17 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.180 CONTROLSS_PWMXBAR17_G5 Register

3.15.2.180.1 CONTROLSS_PWMXBAR17_G5 Register (Offset = 554h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to Summary Table

Table 3-1865. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1554h

Figure 3-979. CONTROLSS_PWMXBAR17_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR17_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR17_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR17_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR17_G5_SEL							
R/W							
0h							

Table 3-1866. CONTROLSS_PWMXBAR17_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR17_G5_SEL	R/W	0h	PWM XBAR17 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.181 CONTROLSS_PWMXBAR17_G6 Register

3.15.2.181.1 CONTROLSS_PWMXBAR17_G6 Register (Offset = 558h) [reset = 0h]

PWM XBAR 17 Input Select.

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Table 3-1867. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1558h

Figure 3-980. CONTROLSS_PWMXBAR17_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR17_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR17_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR17_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR17_G6_SEL							
R/W							
0h							

Table 3-1868. CONTROLSS_PWMXBAR17_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR17_G6_SEL	R/W	0h	PWM XBAR17 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.182 CONTROLSS_PWMXBAR17_G7 Register

3.15.2.182.1 CONTROLSS_PWMXBAR17_G7 Register (Offset = 55Ch) [reset = 0h]

PWM XBAR 17 Input Select.

Return to Summary Table

Table 3-1869. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 155Ch

Figure 3-981. CONTROLSS_PWMXBAR17_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR17_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR17_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR17_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR17_G7_SEL							
R/W							
0h							

Table 3-1870. CONTROLSS_PWMXBAR17_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR17_G7_SEL	R/W	0h	PWM XBAR17 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.183 CONTROLSS_PWMXBAR17_G8 Register

3.15.2.183.1 CONTROLSS_PWMXBAR17_G8 Register (Offset = 560h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to Summary Table

Table 3-1871. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1560h

Figure 3-982. CONTROLSS_PWMXBAR17_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR17_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR17_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR17_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR17_G8_SEL							
R/W							
0h							

Table 3-1872. CONTROLSS_PWMXBAR17_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR17_G8_SEL	R/W	0h	PWM XBAR17 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.184 CONTROLSS_PWMXBAR17_G9 Register

3.15.2.184.1 CONTROLSS_PWMXBAR17_G9 Register (Offset = 564h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to Summary Table

Table 3-1873. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1564h

Figure 3-983. CONTROLSS_PWMXBAR17_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR17_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1874. CONTROLSS_PWMXBAR17_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR17_G9_SEL	R/W	0h	PWM XBAR17 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.185 CONTROLSS_PWMXBAR18_G0 Register

3.15.2.185.1 CONTROLSS_PWMXBAR18_G0 Register (Offset = 580h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to Summary Table

Table 3-1875. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1580h

Figure 3-984. CONTROLSS_PWMXBAR18_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR18_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR18_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR18_G0_SEL							
R/W							
0h							

Table 3-1876. CONTROLSS_PWMXBAR18_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1876. CONTROLSS_PWMXBAR18_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR18_G0_SEL	R/W	0h	PWM XBAR18 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.186 CONTROLSS_PWMXBAR18_G1 Register

3.15.2.186.1 CONTROLSS_PWMXBAR18_G1 Register (Offset = 584h) [reset = 0h]

PWM XBAR 18 Input Select.

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Table 3-1877. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1584h

Figure 3-985. CONTROLSS_PWMXBAR18_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR18_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR18_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR18_G1_SEL							
R/W							
0h							

Table 3-1878. CONTROLSS_PWMXBAR18_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1878. CONTROLSS_PWMXBAR18_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR18_G1_SEL	R/W	0h	PWM XBAR18 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.187 CONTROLSS_PWMXBAR18_G2 Register

3.15.2.187.1 CONTROLSS_PWMXBAR18_G2 Register (Offset = 588h) [reset = 0h]

PWM XBAR 18 Input Select.

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Table 3-1879. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1588h

Figure 3-986. CONTROLSS_PWMXBAR18_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR18_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR18_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR18_G2_SEL							
R/W							
0h							

Table 3-1880. CONTROLSS_PWMXBAR18_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1880. CONTROLSS_PWMXBAR18_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR18_G2_SEL	R/W	0h	PWM XBAR18 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.188 CONTROLSS_PWMXBAR18_G3 Register

3.15.2.188.1 CONTROLSS_PWMXBAR18_G3 Register (Offset = 58Ch) [reset = 0h]

PWM XBAR 18 Input Select.

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Table 3-1881. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 158Ch

Figure 3-987. CONTROLSS_PWMXBAR18_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR18_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR18_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR18_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR18_G3_SEL							
R/W							
0h							

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Table 3-1882. CONTROLSS_PWMXBAR18_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR18_G3_SEL	R/W	0h	PWM XBAR18 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.189 CONTROLSS_PWMXBAR18_G4 Register

3.15.2.189.1 CONTROLSS_PWMXBAR18_G4 Register (Offset = 590h) [reset = 0h]

PWM XBAR 18 Input Select.

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Table 3-1883. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1590h

Figure 3-988. CONTROLSS_PWMXBAR18_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR18_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR18_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR18_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR18_G4_SEL							
R/W							
0h							

Table 3-1884. CONTROLSS_PWMXBAR18_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR18_G4_SEL	R/W	0h	PWM XBAR18 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.190 CONTROLSS_PWMXBAR18_G5 Register

3.15.2.190.1 CONTROLSS_PWMXBAR18_G5 Register (Offset = 594h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to Summary Table

Table 3-1885. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1594h

Figure 3-989. CONTROLSS_PWMXBAR18_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR18_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR18_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR18_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR18_G5_SEL							
R/W							
0h							

Table 3-1886. CONTROLSS_PWMXBAR18_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR18_G5_SEL	R/W	0h	PWM XBAR18 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.191 CONTROLSS_PWMXBAR18_G6 Register

3.15.2.191.1 CONTROLSS_PWMXBAR18_G6 Register (Offset = 598h) [reset = 0h]

PWM XBAR 18 Input Select.

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Table 3-1887. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1598h

Figure 3-990. CONTROLSS_PWMXBAR18_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR18_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR18_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR18_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR18_G6_SEL							
R/W							
0h							

Table 3-1888. CONTROLSS_PWMXBAR18_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR18_G6_SEL	R/W	0h	PWM XBAR18 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.192 CONTROLSS_PWMXBAR18_G7 Register

3.15.2.192.1 CONTROLSS_PWMXBAR18_G7 Register (Offset = 59Ch) [reset = 0h]

PWM XBAR 18 Input Select.

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Table 3-1889. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 159Ch

Figure 3-991. CONTROLSS_PWMXBAR18_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR18_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR18_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR18_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR18_G7_SEL							
R/W							
0h							

Table 3-1890. CONTROLSS_PWMXBAR18_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR18_G7_SEL	R/W	0h	PWM XBAR18 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.193 CONTROLSS_PWMXBAR18_G8 Register

3.15.2.193.1 CONTROLSS_PWMXBAR18_G8 Register (Offset = 5A0h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to Summary Table

Table 3-1891. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15A0h

Figure 3-992. CONTROLSS_PWMXBAR18_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR18_G8_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR18_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR18_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR18_G8_SEL							
R/W							
0h							

Table 3-1892. CONTROLSS_PWMXBAR18_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR18_G8_SEL	R/W	0h	PWM XBAR18 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.194 CONTROLSS_PWMXBAR18_G9 Register

3.15.2.194.1 CONTROLSS_PWMXBAR18_G9 Register (Offset = 5A4h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to Summary Table

Table 3-1893. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15A4h

Figure 3-993. CONTROLSS_PWMXBAR18_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR18_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1894. CONTROLSS_PWMXBAR18_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR18_G9_SEL	R/W	0h	PWM XBAR18 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.195 CONTROLSS_PWMXBAR19_G0 Register

3.15.2.195.1 CONTROLSS_PWMXBAR19_G0 Register (Offset = 5C0h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to Summary Table

Table 3-1895. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15C0h

Figure 3-994. CONTROLSS_PWMXBAR19_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR19_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR19_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR19_G0_SEL							
R/W							
0h							

Table 3-1896. CONTROLSS_PWMXBAR19_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1896. CONTROLSS_PWMXBAR19_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR19_G0_SEL	R/W	0h	PWM XBAR19 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.196 CONTROLSS_PWMXBAR19_G1 Register

3.15.2.196.1 CONTROLSS_PWMXBAR19_G1 Register (Offset = 5C4h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to Summary Table

Table 3-1897. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15C4h

Figure 3-995. CONTROLSS_PWMXBAR19_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR19_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR19_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR19_G1_SEL							
R/W							
0h							

Table 3-1898. CONTROLSS_PWMXBAR19_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1898. CONTROLSS_PWMXBAR19_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR19_G1_SEL	R/W	0h	PWM XBAR19 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.197 CONTROLSS_PWMXBAR19_G2 Register

3.15.2.197.1 CONTROLSS_PWMXBAR19_G2 Register (Offset = 5C8h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to Summary Table

Table 3-1899. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15C8h

Figure 3-996. CONTROLSS_PWMXBAR19_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR19_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR19_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR19_G2_SEL							
R/W							
0h							

Table 3-1900. CONTROLSS_PWMXBAR19_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1900. CONTROLSS_PWMXBAR19_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR19_G2_SEL	R/W	0h	PWM XBAR19 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.198 CONTROLSS_PWMXBAR19_G3 Register

3.15.2.198.1 CONTROLSS_PWMXBAR19_G3 Register (Offset = 5CCh) [reset = 0h]

PWM XBAR 19 Input Select.

Return to Summary Table

Table 3-1901. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15CCh

Figure 3-997. CONTROLSS_PWMXBAR19_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR19_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR19_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR19_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR19_G3_SEL							
R/W							
0h							

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Table 3-1902. CONTROLSS_PWMXBAR19_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR19_G3_SEL	R/W	0h	PWM XBAR19 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.199 CONTROLSS_PWMXBAR19_G4 Register

3.15.2.199.1 CONTROLSS_PWMXBAR19_G4 Register (Offset = 5D0h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to Summary Table

Table 3-1903. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15D0h

Figure 3-998. CONTROLSS_PWMXBAR19_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR19_G4_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR19_G4_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR19_G4_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR19_G4_SEL							
R/W							
0h							

Table 3-1904. CONTROLSS_PWMXBAR19_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR19_G4_SEL	R/W	0h	PWM XBAR19 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.200 CONTROLSS_PWMXBAR19_G5 Register

3.15.2.200.1 CONTROLSS_PWMXBAR19_G5 Register (Offset = 5D4h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to Summary Table

Table 3-1905. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15D4h

Figure 3-999. CONTROLSS_PWMXBAR19_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR19_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR19_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR19_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR19_G5_SEL							
R/W							
0h							

Table 3-1906. CONTROLSS_PWMXBAR19_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR19_G5_SEL	R/W	0h	PWM XBAR19 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.201 CONTROLSS_PWMXBAR19_G6 Register

3.15.2.201.1 CONTROLSS_PWMXBAR19_G6 Register (Offset = 5D8h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to Summary Table

Table 3-1907. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15D8h

Figure 3-1000. CONTROLSS_PWMXBAR19_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR19_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR19_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR19_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR19_G6_SEL							
R/W							
0h							

Table 3-1908. CONTROLSS_PWMXBAR19_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR19_G6_SEL	R/W	0h	PWM XBAR19 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.202 CONTROLSS_PWMXBAR19_G7 Register

3.15.2.202.1 CONTROLSS_PWMXBAR19_G7 Register (Offset = 5DCh) [reset = 0h]

PWM XBAR 19 Input Select.

Return to Summary Table

Table 3-1909. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15DCh

Figure 3-1001. CONTROLSS_PWMXBAR19_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR19_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR19_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR19_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR19_G7_SEL							
R/W							
0h							

Table 3-1910. CONTROLSS_PWMXBAR19_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR19_G7_SEL	R/W	0h	PWM XBAR19 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.203 CONTROLSS_PWMXBAR19_G8 Register

3.15.2.203.1 CONTROLSS_PWMXBAR19_G8 Register (Offset = 5E0h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to Summary Table

Table 3-1911. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15E0h

Figure 3-1002. CONTROLSS_PWMXBAR19_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR19_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR19_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR19_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR19_G8_SEL							
R/W							
0h							

Table 3-1912. CONTROLSS_PWMXBAR19_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR19_G8_SEL	R/W	0h	PWM XBAR19 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.204 CONTROLSS_PWMXBAR19_G9 Register

3.15.2.204.1 CONTROLSS_PWMXBAR19_G9 Register (Offset = 5E4h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to Summary Table

Table 3-1913. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 15E4h

Figure 3-1003. CONTROLSS_PWMXBAR19_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR19_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1914. CONTROLSS_PWMXBAR19_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR19_G9_SEL	R/W	0h	PWM XBAR19 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.205 CONTROLSS_PWMXBAR20_G0 Register

3.15.2.205.1 CONTROLSS_PWMXBAR20_G0 Register (Offset = 600h) [reset = 0h]

PWM XBAR 20 Input Select.

Return to Summary Table

Table 3-1915. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1600h

Figure 3-1004. CONTROLSS_PWMXBAR20_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR20_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR20_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR20_G0_SEL							
R/W							
0h							

Table 3-1916. CONTROLSS_PWMXBAR20_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1916. CONTROLSS_PWMXBAR20_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR20_G0_SEL	R/W	0h	PWM XBAR20 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.206 CONTROLSS_PWMXBAR20_G1 Register

3.15.2.206.1 CONTROLSS_PWMXBAR20_G1 Register (Offset = 604h) [reset = 0h]

PWM XBAR 20 Input Select.

Return to Summary Table

Table 3-1917. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1604h

Figure 3-1005. CONTROLSS_PWMXBAR20_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR20_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR20_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR20_G1_SEL							
R/W							
0h							

Table 3-1918. CONTROLSS_PWMXBAR20_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1918. CONTROLSS_PWMXBAR20_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR20_G1_SEL	R/W	0h	PWM XBAR20 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.207 CONTROLSS_PWMXBAR20_G2 Register

3.15.2.207.1 CONTROLSS_PWMXBAR20_G2 Register (Offset = 608h) [reset = 0h]

PWM XBAR 20 Input Select.

Return to Summary Table

Table 3-1919. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1608h

Figure 3-1006. CONTROLSS_PWMXBAR20_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR20_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR20_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR20_G2_SEL							
R/W							
0h							

Table 3-1920. CONTROLSS_PWMXBAR20_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1920. CONTROLSS_PWMXBAR20_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR20_G2_SEL	R/W	0h	PWM XBAR20 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.208 CONTROLSS_PWMXBAR20_G3 Register

3.15.2.208.1 CONTROLSS_PWMXBAR20_G3 Register (Offset = 60Ch) [reset = 0h]

PWM XBAR 20 Input Select.

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Table 3-1921. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 160Ch

Figure 3-1007. CONTROLSS_PWMXBAR20_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR20_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR20_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR20_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR20_G3_SEL							
R/W							
0h							

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Table 3-1922. CONTROLSS_PWMXBAR20_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR20_G3_SEL	R/W	0h	PWM XBAR20 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.209 CONTROLSS_PWMXBAR20_G4 Register

3.15.2.209.1 CONTROLSS_PWMXBAR20_G4 Register (Offset = 610h) [reset = 0h]

PWM XBAR 20 Input Select.

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Table 3-1923. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1610h

Figure 3-1008. CONTROLSS_PWMXBAR20_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR20_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR20_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR20_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR20_G4_SEL							
R/W							
0h							

Table 3-1924. CONTROLSS_PWMXBAR20_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR20_G4_SEL	R/W	0h	PWM XBAR20 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.210 CONTROLSS_PWMXBAR20_G5 Register

3.15.2.210.1 CONTROLSS_PWMXBAR20_G5 Register (Offset = 614h) [reset = 0h]

PWM XBAR 20 Input Select.

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Table 3-1925. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1614h

Figure 3-1009. CONTROLSS_PWMXBAR20_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR20_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR20_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR20_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR20_G5_SEL							
R/W							
0h							

Table 3-1926. CONTROLSS_PWMXBAR20_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR20_G5_SEL	R/W	0h	PWM XBAR20 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.211 CONTROLSS_PWMXBAR20_G6 Register

3.15.2.211.1 CONTROLSS_PWMXBAR20_G6 Register (Offset = 618h) [reset = 0h]

PWM XBAR 20 Input Select.

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Table 3-1927. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1618h

Figure 3-1010. CONTROLSS_PWMXBAR20_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR20_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR20_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR20_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR20_G6_SEL							
R/W							
0h							

Table 3-1928. CONTROLSS_PWMXBAR20_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR20_G6_SEL	R/W	0h	PWM XBAR20 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.212 CONTROLSS_PWMXBAR20_G7 Register

3.15.2.212.1 CONTROLSS_PWMXBAR20_G7 Register (Offset = 61Ch) [reset = 0h]

PWM XBAR 20 Input Select.

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Table 3-1929. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 161Ch

Figure 3-1011. CONTROLSS_PWMXBAR20_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR20_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR20_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR20_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR20_G7_SEL							
R/W							
0h							

Table 3-1930. CONTROLSS_PWMXBAR20_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR20_G7_SEL	R/W	0h	PWM XBAR20 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.213 CONTROLSS_PWMXBAR20_G8 Register

3.15.2.213.1 CONTROLSS_PWMXBAR20_G8 Register (Offset = 620h) [reset = 0h]

PWM XBAR 20 Input Select.

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Table 3-1931. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1620h

Figure 3-1012. CONTROLSS_PWMXBAR20_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR20_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR20_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR20_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR20_G8_SEL							
R/W							
0h							

Table 3-1932. CONTROLSS_PWMXBAR20_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR20_G8_SEL	R/W	0h	PWM XBAR20 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.214 CONTROLSS_PWMXBAR20_G9 Register

3.15.2.214.1 CONTROLSS_PWMXBAR20_G9 Register (Offset = 624h) [reset = 0h]

PWM XBAR 20 Input Select.

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Table 3-1933. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1624h

Figure 3-1013. CONTROLSS_PWMXBAR20_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR20_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1934. CONTROLSS_PWMXBAR20_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR20_G9_SEL	R/W	0h	PWM XBAR20 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.215 CONTROLSS_PWMXBAR21_G0 Register

3.15.2.215.1 CONTROLSS_PWMXBAR21_G0 Register (Offset = 640h) [reset = 0h]

PWM XBAR 21 Input Select.

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Table 3-1935. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1640h

Figure 3-1014. CONTROLSS_PWMXBAR21_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR21_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR21_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR21_G0_SEL							
R/W							
0h							

Table 3-1936. CONTROLSS_PWMXBAR21_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1936. CONTROLSS_PWMXBAR21_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR21_G0_SEL	R/W	0h	PWM XBAR21 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.216 CONTROLSS_PWMXBAR21_G1 Register

3.15.2.216.1 CONTROLSS_PWMXBAR21_G1 Register (Offset = 644h) [reset = 0h]

PWM XBAR 21 Input Select.

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Table 3-1937. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1644h

Figure 3-1015. CONTROLSS_PWMXBAR21_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR21_G1_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR21_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR21_G1_SEL							
R/W							
0h							

Table 3-1938. CONTROLSS_PWMXBAR21_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1938. CONTROLSS_PWMXBAR21_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR21_G1_SEL	R/W	0h	PWM XBAR21 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.217 CONTROLSS_PWMXBAR21_G2 Register

3.15.2.217.1 CONTROLSS_PWMXBAR21_G2 Register (Offset = 648h) [reset = 0h]

PWM XBAR 21 Input Select.

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Table 3-1939. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1648h

Figure 3-1016. CONTROLSS_PWMXBAR21_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR21_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR21_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR21_G2_SEL							
R/W							
0h							

Table 3-1940. CONTROLSS_PWMXBAR21_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1940. CONTROLSS_PWMXBAR21_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR21_G2_SEL	R/W	0h	PWM XBAR21 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.218 CONTROLSS_PWMXBAR21_G3 Register

3.15.2.218.1 CONTROLSS_PWMXBAR21_G3 Register (Offset = 64Ch) [reset = 0h]

PWM XBAR 21 Input Select.

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Table 3-1941. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 164Ch

Figure 3-1017. CONTROLSS_PWMXBAR21_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR21_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR21_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR21_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR21_G3_SEL							
R/W							
0h							

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Table 3-1942. CONTROLSS_PWMXBAR21_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR21_G3_SEL	R/W	0h	PWM XBAR21 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.219 CONTROLSS_PWMXBAR21_G4 Register

3.15.2.219.1 CONTROLSS_PWMXBAR21_G4 Register (Offset = 650h) [reset = 0h]

PWM XBAR 21 Input Select.

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Table 3-1943. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1650h

Figure 3-1018. CONTROLSS_PWMXBAR21_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR21_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR21_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR21_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR21_G4_SEL							
R/W							
0h							

Table 3-1944. CONTROLSS_PWMXBAR21_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR21_G4_SEL	R/W	0h	PWM XBAR21 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.220 CONTROLSS_PWMXBAR21_G5 Register

3.15.2.220.1 CONTROLSS_PWMXBAR21_G5 Register (Offset = 654h) [reset = 0h]

PWM XBAR 21 Input Select.

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Table 3-1945. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1654h

Figure 3-1019. CONTROLSS_PWMXBAR21_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR21_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR21_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR21_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR21_G5_SEL							
R/W							
0h							

Table 3-1946. CONTROLSS_PWMXBAR21_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR21_G5_SEL	R/W	0h	PWM XBAR21 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.221 CONTROLSS_PWMXBAR21_G6 Register

3.15.2.221.1 CONTROLSS_PWMXBAR21_G6 Register (Offset = 658h) [reset = 0h]

PWM XBAR 21 Input Select.

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Table 3-1947. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1658h

Figure 3-1020. CONTROLSS_PWMXBAR21_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR21_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR21_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR21_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR21_G6_SEL							
R/W							
0h							

Table 3-1948. CONTROLSS_PWMXBAR21_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR21_G6_SEL	R/W	0h	PWM XBAR21 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.222 CONTROLSS_PWMXBAR21_G7 Register

3.15.2.222.1 CONTROLSS_PWMXBAR21_G7 Register (Offset = 65Ch) [reset = 0h]

PWM XBAR 21 Input Select.

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Table 3-1949. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 165Ch

Figure 3-1021. CONTROLSS_PWMXBAR21_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR21_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR21_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR21_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR21_G7_SEL							
R/W							
0h							

Table 3-1950. CONTROLSS_PWMXBAR21_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR21_G7_SEL	R/W	0h	PWM XBAR21 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.223 CONTROLSS_PWMXBAR21_G8 Register

3.15.2.223.1 CONTROLSS_PWMXBAR21_G8 Register (Offset = 660h) [reset = 0h]

PWM XBAR 21 Input Select.

Return to Summary Table

Table 3-1951. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1660h

Figure 3-1022. CONTROLSS_PWMXBAR21_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR21_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR21_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR21_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR21_G8_SEL							
R/W							
0h							

Table 3-1952. CONTROLSS_PWMXBAR21_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR21_G8_SEL	R/W	0h	PWM XBAR21 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.224 CONTROLSS_PWMXBAR21_G9 Register

3.15.2.224.1 CONTROLSS_PWMXBAR21_G9 Register (Offset = 664h) [reset = 0h]

PWM XBAR 21 Input Select.

Return to Summary Table

Table 3-1953. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1664h

Figure 3-1023. CONTROLSS_PWMXBAR21_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR21_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1954. CONTROLSS_PWMXBAR21_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR21_G9_SEL	R/W	0h	PWM XBAR21 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.225 CONTROLSS_PWMXBAR22_G0 Register

3.15.2.225.1 CONTROLSS_PWMXBAR22_G0 Register (Offset = 680h) [reset = 0h]

PWM XBAR 22 Input Select.

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Table 3-1955. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1680h

Figure 3-1024. CONTROLSS_PWMXBAR22_G0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PWMXBAR22_G0_SEL</td></tr>
<tr><td colspan="4">NONE</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PWMXBAR22_G0_SEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PWMXBAR22_G0_SEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 3-1956. CONTROLSS_PWMXBAR22_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1956. CONTROLSS_PWMXBAR22_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR22_G0_SEL	R/W	0h	PWM XBAR22 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.226 CONTROLSS_PWMXBAR22_G1 Register

3.15.2.226.1 CONTROLSS_PWMXBAR22_G1 Register (Offset = 684h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to Summary Table

Table 3-1957. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1684h

Figure 3-1025. CONTROLSS_PWMXBAR22_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR22_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR22_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR22_G1_SEL							
R/W							
0h							

Table 3-1958. CONTROLSS_PWMXBAR22_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1958. CONTROLSS_PWMXBAR22_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR22_G1_SEL	R/W	0h	PWM XBAR22 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.227 CONTROLSS_PWMXBAR22_G2 Register

3.15.2.227.1 CONTROLSS_PWMXBAR22_G2 Register (Offset = 688h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to Summary Table

Table 3-1959. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1688h

Figure 3-1026. CONTROLSS_PWMXBAR22_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR22_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR22_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR22_G2_SEL							
R/W							
0h							

Table 3-1960. CONTROLSS_PWMXBAR22_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1960. CONTROLSS_PWMXBAR22_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR22_G2_SEL	R/W	0h	PWM XBAR22 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.228 CONTROLSS_PWMXBAR22_G3 Register

3.15.2.228.1 CONTROLSS_PWMXBAR22_G3 Register (Offset = 68Ch) [reset = 0h]

PWM XBAR 22 Input Select.

Return to Summary Table

Table 3-1961. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 168Ch

Figure 3-1027. CONTROLSS_PWMXBAR22_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR22_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR22_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR22_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR22_G3_SEL							
R/W							
0h							

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Table 3-1962. CONTROLSS_PWMXBAR22_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR22_G3_SEL	R/W	0h	PWM XBAR22 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.229 CONTROLSS_PWMXBAR22_G4 Register

3.15.2.229.1 CONTROLSS_PWMXBAR22_G4 Register (Offset = 690h) [reset = 0h]

PWM XBAR 22 Input Select.

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Table 3-1963. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1690h

Figure 3-1028. CONTROLSS_PWMXBAR22_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR22_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR22_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR22_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR22_G4_SEL							
R/W							
0h							

Table 3-1964. CONTROLSS_PWMXBAR22_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR22_G4_SEL	R/W	0h	PWM XBAR22 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.230 CONTROLSS_PWMXBAR22_G5 Register

3.15.2.230.1 CONTROLSS_PWMXBAR22_G5 Register (Offset = 694h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to Summary Table

Table 3-1965. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1694h

Figure 3-1029. CONTROLSS_PWMXBAR22_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR22_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR22_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR22_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR22_G5_SEL							
R/W							
0h							

Table 3-1966. CONTROLSS_PWMXBAR22_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR22_G5_SEL	R/W	0h	PWM XBAR22 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.231 CONTROLSS_PWMXBAR22_G6 Register

3.15.2.231.1 CONTROLSS_PWMXBAR22_G6 Register (Offset = 698h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to Summary Table

Table 3-1967. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1698h

Figure 3-1030. CONTROLSS_PWMXBAR22_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR22_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR22_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR22_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR22_G6_SEL							
R/W							
0h							

Table 3-1968. CONTROLSS_PWMXBAR22_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR22_G6_SEL	R/W	0h	PWM XBAR22 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.232 CONTROLSS_PWMXBAR22_G7 Register

3.15.2.232.1 CONTROLSS_PWMXBAR22_G7 Register (Offset = 69Ch) [reset = 0h]

PWM XBAR 22 Input Select.

Return to Summary Table

Table 3-1969. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 169Ch

Figure 3-1031. CONTROLSS_PWMXBAR22_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR22_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR22_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR22_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR22_G7_SEL							
R/W							
0h							

Table 3-1970. CONTROLSS_PWMXBAR22_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR22_G7_SEL	R/W	0h	PWM XBAR22 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.233 CONTROLSS_PWMXBAR22_G8 Register

3.15.2.233.1 CONTROLSS_PWMXBAR22_G8 Register (Offset = 6A0h) [reset = 0h]

PWM XBAR 22 Input Select.

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Table 3-1971. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16A0h

Figure 3-1032. CONTROLSS_PWMXBAR22_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR22_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR22_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR22_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR22_G8_SEL							
R/W							
0h							

Table 3-1972. CONTROLSS_PWMXBAR22_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR22_G8_SEL	R/W	0h	PWM XBAR22 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.234 CONTROLSS_PWMXBAR22_G9 Register

3.15.2.234.1 CONTROLSS_PWMXBAR22_G9 Register (Offset = 6A4h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to Summary Table

Table 3-1973. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16A4h

Figure 3-1033. CONTROLSS_PWMXBAR22_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PWMXBAR22_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1974. CONTROLSS_PWMXBAR22_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR22_G9_SEL	R/W	0h	PWM XBAR22 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.235 CONTROLSS_PWMXBAR23_G0 Register

3.15.2.235.1 CONTROLSS_PWMXBAR23_G0 Register (Offset = 6C0h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to Summary Table

Table 3-1975. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16C0h

Figure 3-1034. CONTROLSS_PWMXBAR23_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR23_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR23_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR23_G0_SEL							
R/W							
0h							

Table 3-1976. CONTROLSS_PWMXBAR23_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1976. CONTROLSS_PWMXBAR23_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR23_G0_SEL	R/W	0h	PWM XBAR23 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.236 CONTROLSS_PWMXBAR23_G1 Register

3.15.2.236.1 CONTROLSS_PWMXBAR23_G1 Register (Offset = 6C4h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to Summary Table

Table 3-1977. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16C4h

Figure 3-1035. CONTROLSS_PWMXBAR23_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR23_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR23_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR23_G1_SEL							
R/W							
0h							

Table 3-1978. CONTROLSS_PWMXBAR23_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1978. CONTROLSS_PWMXBAR23_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR23_G1_SEL	R/W	0h	PWM XBAR23 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.237 CONTROLSS_PWMXBAR23_G2 Register

3.15.2.237.1 CONTROLSS_PWMXBAR23_G2 Register (Offset = 6C8h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to Summary Table

Table 3-1979. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16C8h

Figure 3-1036. CONTROLSS_PWMXBAR23_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR23_G2_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR23_G2_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR23_G2_SEL							
R/W							
0h							

Table 3-1980. CONTROLSS_PWMXBAR23_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-1980. CONTROLSS_PWMXBAR23_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR23_G2_SEL	R/W	0h	PWM XBAR23 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.238 CONTROLSS_PWMXBAR23_G3 Register

3.15.2.238.1 CONTROLSS_PWMXBAR23_G3 Register (Offset = 6CCh) [reset = 0h]

PWM XBAR 23 Input Select.

Return to Summary Table

Table 3-1981. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16CCh

Figure 3-1037. CONTROLSS_PWMXBAR23_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR23_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR23_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR23_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR23_G3_SEL							
R/W							
0h							

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Table 3-1982. CONTROLSS_PWMXBAR23_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR23_G3_SEL	R/W	0h	PWM XBAR23 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.239 CONTROLSS_PWMXBAR23_G4 Register

3.15.2.239.1 CONTROLSS_PWMXBAR23_G4 Register (Offset = 6D0h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to Summary Table

Table 3-1983. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16D0h

Figure 3-1038. CONTROLSS_PWMXBAR23_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR23_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR23_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR23_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR23_G4_SEL							
R/W							
0h							

Table 3-1984. CONTROLSS_PWMXBAR23_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR23_G4_SEL	R/W	0h	PWM XBAR23 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.240 CONTROLSS_PWMXBAR23_G5 Register

3.15.2.240.1 CONTROLSS_PWMXBAR23_G5 Register (Offset = 6D4h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to Summary Table

Table 3-1985. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16D4h

Figure 3-1039. CONTROLSS_PWMXBAR23_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR23_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR23_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR23_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR23_G5_SEL							
R/W							
0h							

Table 3-1986. CONTROLSS_PWMXBAR23_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR23_G5_SEL	R/W	0h	PWM XBAR23 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.241 CONTROLSS_PWMXBAR23_G6 Register

3.15.2.241.1 CONTROLSS_PWMXBAR23_G6 Register (Offset = 6D8h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to Summary Table

Table 3-1987. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16D8h

Figure 3-1040. CONTROLSS_PWMXBAR23_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR23_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR23_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR23_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR23_G6_SEL							
R/W							
0h							

Table 3-1988. CONTROLSS_PWMXBAR23_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR23_G6_SEL	R/W	0h	PWM XBAR23 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.242 CONTROLSS_PWMXBAR23_G7 Register

3.15.2.242.1 CONTROLSS_PWMXBAR23_G7 Register (Offset = 6DCh) [reset = 0h]

PWM XBAR 23 Input Select.

Return to Summary Table

Table 3-1989. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16DCh

Figure 3-1041. CONTROLSS_PWMXBAR23_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR23_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR23_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR23_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR23_G7_SEL							
R/W							
0h							

Table 3-1990. CONTROLSS_PWMXBAR23_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR23_G7_SEL	R/W	0h	PWM XBAR23 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.243 CONTROLSS_PWMXBAR23_G8 Register

3.15.2.243.1 CONTROLSS_PWMXBAR23_G8 Register (Offset = 6E0h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to Summary Table

Table 3-1991. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16E0h

Figure 3-1042. CONTROLSS_PWMXBAR23_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR23_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR23_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR23_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR23_G8_SEL							
R/W							
0h							

Table 3-1992. CONTROLSS_PWMXBAR23_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR23_G8_SEL	R/W	0h	PWM XBAR23 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.244 CONTROLSS_PWMXBAR23_G9 Register

3.15.2.244.1 CONTROLSS_PWMXBAR23_G9 Register (Offset = 6E4h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to Summary Table

Table 3-1993. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 16E4h

Figure 3-1043. CONTROLSS_PWMXBAR23_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR23_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-1994. CONTROLSS_PWMXBAR23_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR23_G9_SEL	R/W	0h	PWM XBAR23 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.245 CONTROLSS_PWMXBAR24_G0 Register

3.15.2.245.1 CONTROLSS_PWMXBAR24_G0 Register (Offset = 700h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to Summary Table

Table 3-1995. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1700h

Figure 3-1044. CONTROLSS_PWMXBAR24_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR24_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR24_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR24_G0_SEL							
R/W							
0h							

Table 3-1996. CONTROLSS_PWMXBAR24_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1996. CONTROLSS_PWMXBAR24_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR24_G0_SEL	R/W	0h	PWM XBAR24 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.246 CONTROLSS_PWMXBAR24_G1 Register

3.15.2.246.1 CONTROLSS_PWMXBAR24_G1 Register (Offset = 704h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to Summary Table

Table 3-1997. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1704h

Figure 3-1045. CONTROLSS_PWMXBAR24_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR24_G1_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR24_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR24_G1_SEL							
R/W							
0h							

Table 3-1998. CONTROLSS_PWMXBAR24_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-1998. CONTROLSS_PWMXBAR24_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR24_G1_SEL	R/W	0h	PWM XBAR24 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.247 CONTROLSS_PWMXBAR24_G2 Register

3.15.2.247.1 CONTROLSS_PWMXBAR24_G2 Register (Offset = 708h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to Summary Table

Table 3-1999. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1708h

Figure 3-1046. CONTROLSS_PWMXBAR24_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR24_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR24_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR24_G2_SEL							
R/W							
0h							

Table 3-2000. CONTROLSS_PWMXBAR24_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-2000. CONTROLSS_PWMXBAR24_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR24_G2_SEL	R/W	0h	PWM XBAR24 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.248 CONTROLSS_PWMXBAR24_G3 Register

3.15.2.248.1 CONTROLSS_PWMXBAR24_G3 Register (Offset = 70Ch) [reset = 0h]

PWM XBAR 24 Input Select.

Return to Summary Table

Table 3-2001. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 170Ch

Figure 3-1047. CONTROLSS_PWMXBAR24_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR24_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR24_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR24_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR24_G3_SEL							
R/W							
0h							

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Table 3-2002. CONTROLSS_PWMXBAR24_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR24_G3_SEL	R/W	0h	PWM XBAR24 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.249 CONTROLSS_PWMXBAR24_G4 Register

3.15.2.249.1 CONTROLSS_PWMXBAR24_G4 Register (Offset = 710h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to Summary Table

Table 3-2003. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1710h

Figure 3-1048. CONTROLSS_PWMXBAR24_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR24_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR24_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR24_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR24_G4_SEL							
R/W							
0h							

Table 3-2004. CONTROLSS_PWMXBAR24_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR24_G4_SEL	R/W	0h	PWM XBAR24 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.250 CONTROLSS_PWMXBAR24_G5 Register

3.15.2.250.1 CONTROLSS_PWMXBAR24_G5 Register (Offset = 714h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to Summary Table

Table 3-2005. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1714h

Figure 3-1049. CONTROLSS_PWMXBAR24_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR24_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR24_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR24_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR24_G5_SEL							
R/W							
0h							

Table 3-2006. CONTROLSS_PWMXBAR24_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR24_G5_SEL	R/W	0h	PWM XBAR24 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.251 CONTROLSS_PWMXBAR24_G6 Register

3.15.2.251.1 CONTROLSS_PWMXBAR24_G6 Register (Offset = 718h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to Summary Table

Table 3-2007. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1718h

Figure 3-1050. CONTROLSS_PWMXBAR24_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR24_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR24_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR24_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR24_G6_SEL							
R/W							
0h							

Table 3-2008. CONTROLSS_PWMXBAR24_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR24_G6_SEL	R/W	0h	PWM XBAR24 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.252 CONTROLSS_PWMXBAR24_G7 Register

3.15.2.252.1 CONTROLSS_PWMXBAR24_G7 Register (Offset = 71Ch) [reset = 0h]

PWM XBAR 24 Input Select.

Return to Summary Table

Table 3-2009. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 171Ch

Figure 3-1051. CONTROLSS_PWMXBAR24_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR24_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR24_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR24_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR24_G7_SEL							
R/W							
0h							

Table 3-2010. CONTROLSS_PWMXBAR24_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR24_G7_SEL	R/W	0h	PWM XBAR24 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.253 CONTROLSS_PWMXBAR24_G8 Register

3.15.2.253.1 CONTROLSS_PWMXBAR24_G8 Register (Offset = 720h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to Summary Table

Table 3-2011. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1720h

Figure 3-1052. CONTROLSS_PWMXBAR24_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR24_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR24_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR24_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR24_G8_SEL							
R/W							
0h							

Table 3-2012. CONTROLSS_PWMXBAR24_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR24_G8_SEL	R/W	0h	PWM XBAR24 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.254 CONTROLSS_PWMXBAR24_G9 Register

3.15.2.254.1 CONTROLSS_PWMXBAR24_G9 Register (Offset = 724h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to Summary Table

Table 3-2013. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1724h

Figure 3-1053. CONTROLSS_PWMXBAR24_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR24_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-2014. CONTROLSS_PWMXBAR24_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR24_G9_SEL	R/W	0h	PWM XBAR24 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.255 CONTROLSS_PWMXBAR25_G0 Register

3.15.2.255.1 CONTROLSS_PWMXBAR25_G0 Register (Offset = 740h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to Summary Table

Table 3-2015. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1740h

Figure 3-1054. CONTROLSS_PWMXBAR25_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR25_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR25_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR25_G0_SEL							
R/W							
0h							

Table 3-2016. CONTROLSS_PWMXBAR25_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-2016. CONTROLSS_PWMXBAR25_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR25_G0_SEL	R/W	0h	PWM XBAR25 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.256 CONTROLSS_PWMXBAR25_G1 Register

3.15.2.256.1 CONTROLSS_PWMXBAR25_G1 Register (Offset = 744h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to Summary Table

Table 3-2017. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1744h

Figure 3-1055. CONTROLSS_PWMXBAR25_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR25_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR25_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR25_G1_SEL							
R/W							
0h							

Table 3-2018. CONTROLSS_PWMXBAR25_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-2018. CONTROLSS_PWMXBAR25_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR25_G1_SEL	R/W	0h	PWM XBAR25 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.257 CONTROLSS_PWMXBAR25_G2 Register

3.15.2.257.1 CONTROLSS_PWMXBAR25_G2 Register (Offset = 748h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to Summary Table

Table 3-2019. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1748h

Figure 3-1056. CONTROLSS_PWMXBAR25_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR25_G2_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR25_G2_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR25_G2_SEL							
R/W							
0h							

Table 3-2020. CONTROLSS_PWMXBAR25_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-2020. CONTROLSS_PWMXBAR25_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR25_G2_SEL	R/W	0h	PWM XBAR25 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.258 CONTROLSS_PWMXBAR25_G3 Register

3.15.2.258.1 CONTROLSS_PWMXBAR25_G3 Register (Offset = 74Ch) [reset = 0h]

PWM XBAR 25 Input Select.

Return to Summary Table

Table 3-2021. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 174Ch

Figure 3-1057. CONTROLSS_PWMXBAR25_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR25_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR25_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR25_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR25_G3_SEL							
R/W							
0h							

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Table 3-2022. CONTROLSS_PWMXBAR25_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR25_G3_SEL	R/W	0h	PWM XBAR25 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.259 CONTROLSS_PWMXBAR25_G4 Register

3.15.2.259.1 CONTROLSS_PWMXBAR25_G4 Register (Offset = 750h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to Summary Table

Table 3-2023. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1750h

Figure 3-1058. CONTROLSS_PWMXBAR25_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR25_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR25_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR25_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR25_G4_SEL							
R/W							
0h							

Table 3-2024. CONTROLSS_PWMXBAR25_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR25_G4_SEL	R/W	0h	PWM XBAR25 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.260 CONTROLSS_PWMXBAR25_G5 Register

3.15.2.260.1 CONTROLSS_PWMXBAR25_G5 Register (Offset = 754h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to Summary Table

Table 3-2025. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1754h

Figure 3-1059. CONTROLSS_PWMXBAR25_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR25_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR25_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR25_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR25_G5_SEL							
R/W							
0h							

Table 3-2026. CONTROLSS_PWMXBAR25_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR25_G5_SEL	R/W	0h	PWM XBAR25 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.261 CONTROLSS_PWMXBAR25_G6 Register

3.15.2.261.1 CONTROLSS_PWMXBAR25_G6 Register (Offset = 758h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to Summary Table

Table 3-2027. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1758h

Figure 3-1060. CONTROLSS_PWMXBAR25_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR25_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR25_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR25_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR25_G6_SEL							
R/W							
0h							

Table 3-2028. CONTROLSS_PWMXBAR25_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR25_G6_SEL	R/W	0h	PWM XBAR25 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.262 CONTROLSS_PWMXBAR25_G7 Register

3.15.2.262.1 CONTROLSS_PWMXBAR25_G7 Register (Offset = 75Ch) [reset = 0h]

PWM XBAR 25 Input Select.

Return to Summary Table

Table 3-2029. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 175Ch

Figure 3-1061. CONTROLSS_PWMXBAR25_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR25_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR25_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR25_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR25_G7_SEL							
R/W							
0h							

Table 3-2030. CONTROLSS_PWMXBAR25_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR25_G7_SEL	R/W	0h	PWM XBAR25 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.263 CONTROLSS_PWMXBAR25_G8 Register

3.15.2.263.1 CONTROLSS_PWMXBAR25_G8 Register (Offset = 760h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to Summary Table

Table 3-2031. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1760h

Figure 3-1062. CONTROLSS_PWMXBAR25_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR25_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR25_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR25_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR25_G8_SEL							
R/W							
0h							

Table 3-2032. CONTROLSS_PWMXBAR25_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR25_G8_SEL	R/W	0h	PWM XBAR25 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.264 CONTROLSS_PWMXBAR25_G9 Register

3.15.2.264.1 CONTROLSS_PWMXBAR25_G9 Register (Offset = 764h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to Summary Table

Table 3-2033. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1764h

Figure 3-1063. CONTROLSS_PWMXBAR25_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR25_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-2034. CONTROLSS_PWMXBAR25_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR25_G9_SEL	R/W	0h	PWM XBAR25 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.265 CONTROLSS_PWMXBAR26_G0 Register

3.15.2.265.1 CONTROLSS_PWMXBAR26_G0 Register (Offset = 780h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to Summary Table

Table 3-2035. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1780h

Figure 3-1064. CONTROLSS_PWMXBAR26_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR26_G0_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR26_G0_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR26_G0_SEL							
R/W							
0h							

Table 3-2036. CONTROLSS_PWMXBAR26_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-2036. CONTROLSS_PWMXBAR26_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR26_G0_SEL	R/W	0h	PWM XBAR26 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.266 CONTROLSS_PWMXBAR26_G1 Register

3.15.2.266.1 CONTROLSS_PWMXBAR26_G1 Register (Offset = 784h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to Summary Table

Table 3-2037. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1784h

Figure 3-1065. CONTROLSS_PWMXBAR26_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR26_G1_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR26_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR26_G1_SEL							
R/W							
0h							

Table 3-2038. CONTROLSS_PWMXBAR26_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-2038. CONTROLSS_PWMXBAR26_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR26_G1_SEL	R/W	0h	PWM XBAR26 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.267 CONTROLSS_PWMXBAR26_G2 Register

3.15.2.267.1 CONTROLSS_PWMXBAR26_G2 Register (Offset = 788h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to Summary Table

Table 3-2039. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1788h

Figure 3-1066. CONTROLSS_PWMXBAR26_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR26_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR26_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR26_G2_SEL							
R/W							
0h							

Table 3-2040. CONTROLSS_PWMXBAR26_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-2040. CONTROLSS_PWMXBAR26_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR26_G2_SEL	R/W	0h	PWM XBAR26 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.268 CONTROLSS_PWMXBAR26_G3 Register

3.15.2.268.1 CONTROLSS_PWMXBAR26_G3 Register (Offset = 78Ch) [reset = 0h]

PWM XBAR 26 Input Select.

Return to Summary Table

Table 3-2041. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 178Ch

Figure 3-1067. CONTROLSS_PWMXBAR26_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR26_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR26_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR26_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR26_G3_SEL							
R/W							
0h							

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Table 3-2042. CONTROLSS_PWMXBAR26_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR26_G3_SEL	R/W	0h	PWM XBAR26 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.269 CONTROLSS_PWMXBAR26_G4 Register

3.15.2.269.1 CONTROLSS_PWMXBAR26_G4 Register (Offset = 790h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to Summary Table

Table 3-2043. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1790h

Figure 3-1068. CONTROLSS_PWMXBAR26_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR26_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR26_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR26_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR26_G4_SEL							
R/W							
0h							

Table 3-2044. CONTROLSS_PWMXBAR26_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR26_G4_SEL	R/W	0h	PWM XBAR26 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.270 CONTROLSS_PWMXBAR26_G5 Register

3.15.2.270.1 CONTROLSS_PWMXBAR26_G5 Register (Offset = 794h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to Summary Table

Table 3-2045. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1794h

Figure 3-1069. CONTROLSS_PWMXBAR26_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR26_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR26_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR26_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR26_G5_SEL							
R/W							
0h							

Table 3-2046. CONTROLSS_PWMXBAR26_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR26_G5_SEL	R/W	0h	PWM XBAR26 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.271 CONTROLSS_PWMXBAR26_G6 Register

3.15.2.271.1 CONTROLSS_PWMXBAR26_G6 Register (Offset = 798h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to Summary Table

Table 3-2047. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1798h

Figure 3-1070. CONTROLSS_PWMXBAR26_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR26_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR26_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR26_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR26_G6_SEL							
R/W							
0h							

Table 3-2048. CONTROLSS_PWMXBAR26_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR26_G6_SEL	R/W	0h	PWM XBAR26 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.272 CONTROLSS_PWMXBAR26_G7 Register

3.15.2.272.1 CONTROLSS_PWMXBAR26_G7 Register (Offset = 79Ch) [reset = 0h]

PWM XBAR 26 Input Select.

Return to Summary Table

Table 3-2049. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 179Ch

Figure 3-1071. CONTROLSS_PWMXBAR26_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR26_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR26_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR26_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR26_G7_SEL							
R/W							
0h							

Table 3-2050. CONTROLSS_PWMXBAR26_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR26_G7_SEL	R/W	0h	PWM XBAR26 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.273 CONTROLSS_PWMXBAR26_G8 Register

3.15.2.273.1 CONTROLSS_PWMXBAR26_G8 Register (Offset = 7A0h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to Summary Table

Table 3-2051. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17A0h

Figure 3-1072. CONTROLSS_PWMXBAR26_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR26_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR26_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR26_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR26_G8_SEL							
R/W							
0h							

Table 3-2052. CONTROLSS_PWMXBAR26_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR26_G8_SEL	R/W	0h	PWM XBAR26 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.274 CONTROLSS_PWMXBAR26_G9 Register

3.15.2.274.1 CONTROLSS_PWMXBAR26_G9 Register (Offset = 7A4h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to Summary Table

Table 3-2053. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17A4h

Figure 3-1073. CONTROLSS_PWMXBAR26_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR26_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-2054. CONTROLSS_PWMXBAR26_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR26_G9_SEL	R/W	0h	PWM XBAR26 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.275 CONTROLSS_PWMXBAR27_G0 Register

3.15.2.275.1 CONTROLSS_PWMXBAR27_G0 Register (Offset = 7C0h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to Summary Table

Table 3-2055. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17C0h

Figure 3-1074. CONTROLSS_PWMXBAR27_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR27_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR27_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR27_G0_SEL							
R/W							
0h							

Table 3-2056. CONTROLSS_PWMXBAR27_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-2056. CONTROLSS_PWMXBAR27_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR27_G0_SEL	R/W	0h	PWM XBAR27 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.276 CONTROLSS_PWMXBAR27_G1 Register

3.15.2.276.1 CONTROLSS_PWMXBAR27_G1 Register (Offset = 7C4h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to Summary Table

Table 3-2057. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17C4h

Figure 3-1075. CONTROLSS_PWMXBAR27_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR27_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR27_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR27_G1_SEL							
R/W							
0h							

Table 3-2058. CONTROLSS_PWMXBAR27_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-2058. CONTROLSS_PWMXBAR27_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR27_G1_SEL	R/W	0h	PWM XBAR27 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.277 CONTROLSS_PWMXBAR27_G2 Register

3.15.2.277.1 CONTROLSS_PWMXBAR27_G2 Register (Offset = 7C8h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to Summary Table

Table 3-2059. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17C8h

Figure 3-1076. CONTROLSS_PWMXBAR27_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR27_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR27_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR27_G2_SEL							
R/W							
0h							

Table 3-2060. CONTROLSS_PWMXBAR27_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-2060. CONTROLSS_PWMXBAR27_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR27_G2_SEL	R/W	0h	PWM XBAR27 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.278 CONTROLSS_PWMXBAR27_G3 Register

3.15.2.278.1 CONTROLSS_PWMXBAR27_G3 Register (Offset = 7CCh) [reset = 0h]

PWM XBAR 27 Input Select.

Return to Summary Table

Table 3-2061. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17CCh

Figure 3-1077. CONTROLSS_PWMXBAR27_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR27_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR27_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR27_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR27_G3_SEL							
R/W							
0h							

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Table 3-2062. CONTROLSS_PWMXBAR27_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR27_G3_SEL	R/W	0h	PWM XBAR27 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.279 CONTROLSS_PWMXBAR27_G4 Register

3.15.2.279.1 CONTROLSS_PWMXBAR27_G4 Register (Offset = 7D0h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to Summary Table

Table 3-2063. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17D0h

Figure 3-1078. CONTROLSS_PWMXBAR27_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR27_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR27_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR27_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR27_G4_SEL							
R/W							
0h							

Table 3-2064. CONTROLSS_PWMXBAR27_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR27_G4_SEL	R/W	0h	PWM XBAR27 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.280 CONTROLSS_PWMXBAR27_G5 Register

3.15.2.280.1 CONTROLSS_PWMXBAR27_G5 Register (Offset = 7D4h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to Summary Table

Table 3-2065. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17D4h

Figure 3-1079. CONTROLSS_PWMXBAR27_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR27_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR27_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR27_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR27_G5_SEL							
R/W							
0h							

Table 3-2066. CONTROLSS_PWMXBAR27_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR27_G5_SEL	R/W	0h	PWM XBAR27 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.281 CONTROLSS_PWMXBAR27_G6 Register

3.15.2.281.1 CONTROLSS_PWMXBAR27_G6 Register (Offset = 7D8h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to Summary Table

Table 3-2067. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17D8h

Figure 3-1080. CONTROLSS_PWMXBAR27_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR27_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR27_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR27_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR27_G6_SEL							
R/W							
0h							

Table 3-2068. CONTROLSS_PWMXBAR27_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR27_G6_SEL	R/W	0h	PWM XBAR27 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.282 CONTROLSS_PWMXBAR27_G7 Register

3.15.2.282.1 CONTROLSS_PWMXBAR27_G7 Register (Offset = 7DCh) [reset = 0h]

PWM XBAR 27 Input Select.

Return to Summary Table

Table 3-2069. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17DCh

Figure 3-1081. CONTROLSS_PWMXBAR27_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR27_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR27_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR27_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR27_G7_SEL							
R/W							
0h							

Table 3-2070. CONTROLSS_PWMXBAR27_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR27_G7_SEL	R/W	0h	PWM XBAR27 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.283 CONTROLSS_PWMXBAR27_G8 Register

3.15.2.283.1 CONTROLSS_PWMXBAR27_G8 Register (Offset = 7E0h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to Summary Table

Table 3-2071. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17E0h

Figure 3-1082. CONTROLSS_PWMXBAR27_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR27_G8_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR27_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR27_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR27_G8_SEL							
R/W							
0h							

Table 3-2072. CONTROLSS_PWMXBAR27_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR27_G8_SEL	R/W	0h	PWM XBAR27 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.284 CONTROLSS_PWMXBAR27_G9 Register

3.15.2.284.1 CONTROLSS_PWMXBAR27_G9 Register (Offset = 7E4h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to Summary Table

Table 3-2073. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 17E4h

Figure 3-1083. CONTROLSS_PWMXBAR27_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR27_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-2074. CONTROLSS_PWMXBAR27_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR27_G9_SEL	R/W	0h	PWM XBAR27 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.285 CONTROLSS_PWMXBAR28_G0 Register

3.15.2.285.1 CONTROLSS_PWMXBAR28_G0 Register (Offset = 800h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to Summary Table

Table 3-2075. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1800h

Figure 3-1084. CONTROLSS_PWMXBAR28_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR28_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR28_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR28_G0_SEL							
R/W							
0h							

Table 3-2076. CONTROLSS_PWMXBAR28_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-2076. CONTROLSS_PWMXBAR28_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR28_G0_SEL	R/W	0h	PWM XBAR28 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.286 CONTROLSS_PWMXBAR28_G1 Register

3.15.2.286.1 CONTROLSS_PWMXBAR28_G1 Register (Offset = 804h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to Summary Table

Table 3-2077. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1804h

Figure 3-1085. CONTROLSS_PWMXBAR28_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR28_G1_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR28_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR28_G1_SEL							
R/W							
0h							

Table 3-2078. CONTROLSS_PWMXBAR28_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-2078. CONTROLSS_PWMXBAR28_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR28_G1_SEL	R/W	0h	PWM XBAR28 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.287 CONTROLSS_PWMXBAR28_G2 Register

3.15.2.287.1 CONTROLSS_PWMXBAR28_G2 Register (Offset = 808h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to Summary Table

Table 3-2079. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1808h

Figure 3-1086. CONTROLSS_PWMXBAR28_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PWMXBAR28_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR28_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR28_G2_SEL							
R/W							
0h							

Table 3-2080. CONTROLSS_PWMXBAR28_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-2080. CONTROLSS_PWMXBAR28_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR28_G2_SEL	R/W	0h	PWM XBAR28 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.288 CONTROLSS_PWMXBAR28_G3 Register

3.15.2.288.1 CONTROLSS_PWMXBAR28_G3 Register (Offset = 80Ch) [reset = 0h]

PWM XBAR 28 Input Select.

Return to Summary Table

Table 3-2081. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 180Ch

Figure 3-1087. CONTROLSS_PWMXBAR28_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR28_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR28_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR28_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR28_G3_SEL							
R/W							
0h							

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Table 3-2082. CONTROLSS_PWMXBAR28_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR28_G3_SEL	R/W	0h	PWM XBAR28 G3 Input Select Bit 1:ADC0.EVT2 Bit 2:ADC0.EVT3 Bit 3:ADC0.EVT4 Bit 4:ADC1.EVT1 Bit 5:ADC1.EVT2 Bit 6:ADC1.EVT3 Bit 7:ADC1.EVT4 Bit 8:ADC2.EVT1 Bit 9:ADC2.EVT2 Bit 10:ADC2.EVT3 Bit 11:ADC2.EVT4 Bit 12:ADC3.EVT1 Bit 13:ADC3.EVT2 Bit 14:ADC3.EVT3 Bit 15:ADC3.EVT4 Bit 16:ADC4.EVT1 Bit 17:ADC4.EVT2 Bit 18:ADC4.EVT3 Bit 19:ADC4.EVT4 Bit 20:ADCR0.EVT1 Bit 21:ADCR0.EVT2 Bit 22:ADCR0.EVT3 Bit 23:ADCR0.EVT4 Bit 24:ADCR1.EVT1 Bit 25:ADCR1.EVT2 Bit 26:ADCR1.EVT3 Bit 27:ADCR1.EVT4 Bit [31:28]: ADC_ASC_CHECKEVENT[3:0]

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3.15.2.289 CONTROLSS_PWMXBAR28_G4 Register

3.15.2.289.1 CONTROLSS_PWMXBAR28_G4 Register (Offset = 810h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to Summary Table

Table 3-2083. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1810h

Figure 3-1088. CONTROLSS_PWMXBAR28_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR28_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR28_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR28_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR28_G4_SEL							
R/W							
0h							

Table 3-2084. CONTROLSS_PWMXBAR28_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR28_G4_SEL	R/W	0h	PWM XBAR28 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.290 CONTROLSS_PWMXBAR28_G5 Register

3.15.2.290.1 CONTROLSS_PWMXBAR28_G5 Register (Offset = 814h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to Summary Table

Table 3-2085. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1814h

Figure 3-1089. CONTROLSS_PWMXBAR28_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR28_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR28_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR28_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR28_G5_SEL							
R/W							
0h							

Table 3-2086. CONTROLSS_PWMXBAR28_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR28_G5_SEL	R/W	0h	PWM XBAR28 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.291 CONTROLSS_PWMXBAR28_G6 Register

3.15.2.291.1 CONTROLSS_PWMXBAR28_G6 Register (Offset = 818h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to Summary Table

Table 3-2087. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1818h

Figure 3-1090. CONTROLSS_PWMXBAR28_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR28_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR28_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR28_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR28_G6_SEL							
R/W							
0h							

Table 3-2088. CONTROLSS_PWMXBAR28_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR28_G6_SEL	R/W	0h	PWM XBAR28 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.292 CONTROLSS_PWMXBAR28_G7 Register

3.15.2.292.1 CONTROLSS_PWMXBAR28_G7 Register (Offset = 81Ch) [reset = 0h]

PWM XBAR 28 Input Select.

Return to Summary Table

Table 3-2089. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 181Ch

Figure 3-1091. CONTROLSS_PWMXBAR28_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR28_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR28_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR28_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR28_G7_SEL							
R/W							
0h							

Table 3-2090. CONTROLSS_PWMXBAR28_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR28_G7_SEL	R/W	0h	PWM XBAR28 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.293 CONTROLSS_PWMXBAR28_G8 Register

3.15.2.293.1 CONTROLSS_PWMXBAR28_G8 Register (Offset = 820h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to Summary Table

Table 3-2091. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1820h

Figure 3-1092. CONTROLSS_PWMXBAR28_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR28_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR28_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR28_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR28_G8_SEL							
R/W							
0h							

Table 3-2092. CONTROLSS_PWMXBAR28_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR28_G8_SEL	R/W	0h	PWM XBAR28 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.294 CONTROLSS_PWMXBAR28_G9 Register

3.15.2.294.1 CONTROLSS_PWMXBAR28_G9 Register (Offset = 824h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to Summary Table

Table 3-2093. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1824h

Figure 3-1093. CONTROLSS_PWMXBAR28_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR28_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-2094. CONTROLSS_PWMXBAR28_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR28_G9_SEL	R/W	0h	PWM XBAR28 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.15.2.295 CONTROLSS_PWMXBAR29_G0 Register

3.15.2.295.1 CONTROLSS_PWMXBAR29_G0 Register (Offset = 840h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to Summary Table

Table 3-2095. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1840h

Figure 3-1094. CONTROLSS_PWMXBAR29_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				PWMXBAR29_G0_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PWMXBAR29_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR29_G0_SEL							
R/W							
0h							

Table 3-2096. CONTROLSS_PWMXBAR29_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-2096. CONTROLSS_PWMXBAR29_G0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR29_G0_SEL	R/W	0h	PWM XBAR29 G0 Input Select Bit 0:CMP12SS0.CTRIPL Bit 1:CMP12SS0.CTRIPH Bit 2:CMP12SS1.CTRIPL Bit 3:CMP12SS1.CTRIPH Bit 4:CMP12SS2.CTRIPL Bit 5:CMP12SS2.CTRIPH Bit 6:CMP12SS3.CTRIPL Bit 7:CMP12SS3.CTRIPH Bit 8:CMP12SS4.CTRIPL Bit 9:CMP12SS4.CTRIPH Bit 10:CMP12SS5.CTRIPL Bit 11:CMP12SS5.CTRIPH Bit 12:CMP12SS6.CTRIPL Bit 13:CMP12SS6.CTRIPH Bit 14:CMP12SS7.CTRIPL Bit 15:CMP12SS7.CTRIPH Bit 16:CMP12SS8.CTRIPL Bit 17:CMP12SS8.CTRIPH Bit 18:CMP12SS9.CTRIPL Bit 19:CMP12SS9.CTRIPH

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3.15.2.296 CONTROLSS_PWMXBAR29_G1 Register

3.15.2.296.1 CONTROLSS_PWMXBAR29_G1 Register (Offset = 844h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to Summary Table

Table 3-2097. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1844h

Figure 3-1095. CONTROLSS_PWMXBAR29_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PWMXBAR29_G1_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR29_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR29_G1_SEL							
R/W							
0h							

Table 3-2098. CONTROLSS_PWMXBAR29_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved

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Table 3-2098. CONTROLSS_PWMXBAR29_G1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:0	PWMXBAR29_G1_SEL	R/W	0h	PWM XBAR29 G1 Input Select Bit 0:CMP8SS0.CTRIPL Bit 1:CMP8SS0.CTRIPH Bit 2:CMP8SS1.CTRIPL Bit 3:CMP8SS1.CTRIPH Bit 4:CMP8SS2.CTRIPL Bit 5:CMP8SS2.CTRIPH Bit 6:CMP8SS3.CTRIPL Bit 7:CMP8SS3.CTRIPH Bit 8:CMP8SS4.CTRIPL Bit 9:CMP8SS4.CTRIPH Bit 10:CMP8SS5.CTRIPL Bit 11:CMP8SS5.CTRIPH Bit 12:CMP8SS6.CTRIPL Bit 13:CMP8SS6.CTRIPH Bit 14:CMP8SS7.CTRIPL Bit 15:CMP8SS7.CTRIPH Bit 16:CMP8SS8.CTRIPL Bit 17:CMP8SS8.CTRIPH Bit 18:CMP8SS9.CTRIPL Bit 19:CMP8SS9.CTRIPH

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3.15.2.297 CONTROLSS_PWMXBAR29_G2 Register

3.15.2.297.1 CONTROLSS_PWMXBAR29_G2 Register (Offset = 848h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to Summary Table

Table 3-2099. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1848h

Figure 3-1096. CONTROLSS_PWMXBAR29_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PWMXBAR29_G2_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PWMXBAR29_G2_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PWMXBAR29_G2_SEL							
R/W							
0h							

Table 3-2100. CONTROLSS_PWMXBAR29_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved

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Table 3-2100. CONTROLSS_PWMXBAR29_G2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:0	PWMXBAR29_G2_SEL	R/W	0h	PWM XBAR29 G2 Input Select Bit 0:SDFM0.FILT1CEVT1 Bit 1:SDFM0.FILT1CEVT2 Bit 2:SDFM0.FILT1COMPHZ Bit 3:SDFM0.FILT2CEVT1 Bit 4:SDFM0.FILT2CEVT2 Bit 5:SDFM0.FILT2COMPHZ Bit 6:SDFM0.FILT3CEVT1 Bit 7:SDFM0.FILT3CEVT2 Bit 8:SDFM0.FILT3COMPHZ Bit 9:SDFM0.FILT4CEVT1 Bit 10:SDFM0.FILT4CEVT2 Bit 11:SDFM0.FILT4COMPHZ Bit 12:SDFM1.FILT1CEVT1 Bit 13:SDFM1.FILT1CEVT2 Bit 14:SDFM1.FILT1COMPHZ Bit 15:SDFM1.FILT2CEVT1 Bit 16:SDFM1.FILT2CEVT2 Bit 17:SDFM1.FILT2COMPHZ Bit 18:SDFM1.FILT3CEVT1 Bit 19:SDFM1.FILT3CEVT2 Bit 20:SDFM1.FILT3COMPHZ Bit 21:SDFM1.FILT4CEVT1 Bit 22:SDFM1.FILT4CEVT2 Bit 23:SDFM1.FILT4COMPHZ

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3.15.2.298 CONTROLSS_PWMXBAR29_G3 Register

3.15.2.298.1 CONTROLSS_PWMXBAR29_G3 Register (Offset = 84Ch) [reset = 0h]

PWM XBAR 29 Input Select.

Return to Summary Table

Table 3-2101. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 184Ch

Figure 3-1097. CONTROLSS_PWMXBAR29_G3 Name Register

31	30	29	28	27	26	25	24
PWMXBAR29_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR29_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR29_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR29_G3_SEL							
R/W							
0h							

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Table 3-2102. CONTROLSS_PWMXBAR29_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR29_G3_SEL	R/W	0h	PWM XBAR29 G3 Input Select 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1.EVT4 8:ADC2.EVT1 9:ADC2.EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4 28 31:ADC_ASC_CHECKEVENT[3:0]

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3.15.2.299 CONTROLSS_PWMXBAR29_G4 Register

3.15.2.299.1 CONTROLSS_PWMXBAR29_G4 Register (Offset = 850h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to Summary Table

Table 3-2103. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1850h

Figure 3-1098. CONTROLSS_PWMXBAR29_G4 Name Register

31	30	29	28	27	26	25	24
PWMXBAR29_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR29_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR29_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR29_G4_SEL							
R/W							
0h							

Table 3-2104. CONTROLSS_PWMXBAR29_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR29_G4_SEL	R/W	0h	PWM XBAR29 G4 input bit select. Input source is INPUT XBAR. 1:INPUT XBAR output bit[x] selected 0:INPUT XBAR output bit[x] is de-selected

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3.15.2.300 CONTROLSS_PWMXBAR29_G5 Register

3.15.2.300.1 CONTROLSS_PWMXBAR29_G5 Register (Offset = 854h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to Summary Table

Table 3-2105. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1854h

Figure 3-1099. CONTROLSS_PWMXBAR29_G5 Name Register

31	30	29	28	27	26	25	24
PWMXBAR29_G5_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR29_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR29_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR29_G5_SEL							
R/W							
0h							

Table 3-2106. CONTROLSS_PWMXBAR29_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR29_G5_SEL	R/W	0h	PWM XBAR29 G5 input bit select. Input source is PWM TRIPOUT. 1:PWM TRIPOUT bit[x] selected 0:PWM TRIPOUT bit[x] is de-selected

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3.15.2.301 CONTROLSS_PWMXBAR29_G6 Register

3.15.2.301.1 CONTROLSS_PWMXBAR29_G6 Register (Offset = 858h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to Summary Table

Table 3-2107. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1858h

Figure 3-1100. CONTROLSS_PWMXBAR29_G6 Name Register

31	30	29	28	27	26	25	24
PWMXBAR29_G6_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR29_G6_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR29_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR29_G6_SEL							
R/W							
0h							

Table 3-2108. CONTROLSS_PWMXBAR29_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR29_G6_SEL	R/W	0h	PWM XBAR29 G6 input bit select. Input source is PWM DEL TRIP 1:PWM DEL TRIP bit[x] selected 0:PWM DEL TRIP bit[x] is de-selected

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3.15.2.302 CONTROLSS_PWMXBAR29_G7 Register

3.15.2.302.1 CONTROLSS_PWMXBAR29_G7 Register (Offset = 85Ch) [reset = 0h]

PWM XBAR 29 Input Select.

Return to Summary Table

Table 3-2109. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 185Ch

Figure 3-1101. CONTROLSS_PWMXBAR29_G7 Name Register

31	30	29	28	27	26	25	24
PWMXBAR29_G7_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR29_G7_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR29_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR29_G7_SEL							
R/W							
0h							

Table 3-2110. CONTROLSS_PWMXBAR29_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR29_G7_SEL	R/W	0h	PWM XBAR29 G7 input bit select. Input source is PWM DEL ACTIVE 1:PWM DEL ACTIVE bit[x] selected 0:PWM DEL ACTIVE bit[x] is de-selected

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3.15.2.303 CONTROLSS_PWMXBAR29_G8 Register

3.15.2.303.1 CONTROLSS_PWMXBAR29_G8 Register (Offset = 860h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to Summary Table

Table 3-2111. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1860h

Figure 3-1102. CONTROLSS_PWMXBAR29_G8 Name Register

31	30	29	28	27	26	25	24
PWMXBAR29_G8_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMXBAR29_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMXBAR29_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMXBAR29_G8_SEL							
R/W							
0h							

Table 3-2112. CONTROLSS_PWMXBAR29_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMXBAR29_G8_SEL	R/W	0h	PWM XBAR29 G8 Input Select Bit 0:EQEP0.ERR Bit 1:EQEP1.ERR Bit 2:EQEP2.ERR Bit [6:3]: FSIRX0.RX_TRIG4 Bit [10:7]: FSIRX1.RX_TRIG4 Bit [14:11]: FSIRX2.RX_TRIG4 Bit [18:15]: FSIRX3.RX_TRIG4 Bit [31:19]: ECAP[12:0].TRIPOUT

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3.15.2.304 CONTROLSS_PWMXBAR29_G9 Register

3.15.2.304.1 CONTROLSS_PWMXBAR29_G9 Register (Offset = 864h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to Summary Table

Table 3-2113. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1864h

Figure 3-1103. CONTROLSS_PWMXBAR29_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PWMXBAR29_G9_SEL						
NONE	R/W						
0h	0h						

Table 3-2114. CONTROLSS_PWMXBAR29_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	PWMXBAR29_G9_SEL	R/W	0h	PWM XBAR29 G9 Input Select 2 0:ECAP[15:13].TRIPOUT 3:SYNCOUTXBAR0 4:SYNCOUTXBAR1 5:SOC_A_SEL 6:SOC_B_SEL

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3.16 CONTROLSS_PWMSYNCOUTXBAR

CONTROLSS_PWMSYNCOUTXBAR

3.16.1 CONTROLSS_PWMSYNCOUTXBAR Summaries

CONTROLSS_PWMSYNCOUTXBAR Summaries

Table 3-2115. CONTROLSS Registers, Base Address=502D 2000h, Length=2048

Offset	Length	Register Name	CONTROLSS_PWMSYNCOUTXBAR Physical Address
100h	32	CONTROLSS_PWMSYNCOUTXBAR0_G0	502D 2100h
140h	32	CONTROLSS_PWMSYNCOUTXBAR1_G0	502D 2140h
180h	32	CONTROLSS_PWMSYNCOUTXBAR2_G0	502D 2180h
1C0h	32	CONTROLSS_PWMSYNCOUTXBAR3_G0	502D 21C0h
200h	32	CONTROLSS_PWMSYNCOUTXBAR0_G1	502D 2200h
240h	32	CONTROLSS_PWMSYNCOUTXBAR1_G1	502D 2240h
280h	32	CONTROLSS_PWMSYNCOUTXBAR2_G1	502D 2280h
2C0h	32	CONTROLSS_PWMSYNCOUTXBAR3_G1	502D 22C0h

3.16.2 CONTROLSS_PWMSYNCOUTXBAR Registers

CONTROLSS_PWMSYNCOUTXBAR Registers

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3.16.2.1 CONTROLSS_PWMSYNCOUTXBAR0_G0 Register

3.16.2.1.1 CONTROLSS_PWMSYNCOUTXBAR0_G0 Register (Offset = 100h) [reset = 0h]

EPWM pwmsyncout XBAR0 select.

Return to Summary Table

Table 3-2116. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTX BAR	502D 2100h

Figure 3-1104. CONTROLSS_PWMSYNCOUTXBAR0_G0 Name Register

31	30	29	28	27	26	25	24
PWMSYNCOUTXBAR0_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMSYNCOUTXBAR0_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMSYNCOUTXBAR0_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR0_G0_SEL							
R/W							
0h							

Table 3-2117. CONTROLSS_PWMSYNCOUTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMSYNCOUTXBAR0_G0_SEL	R/W	0h	EPWM pwmsyncout XBAR0 select 1:PWM[x] SYNCOUT selected 0:PWM[x] SYNCOUT is de-selected

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3.16.2.2 CONTROLSS_PWMSYNCOUTXBAR1_G0 Register

3.16.2.2.1 CONTROLSS_PWMSYNCOUTXBAR1_G0 Register (Offset = 140h) [reset = 0h]

EPWM pwmsyncout XBAR1 select.

Return to Summary Table

Table 3-2118. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2140h

Figure 3-1105. CONTROLSS_PWMSYNCOUTXBAR1_G0 Name Register

31	30	29	28	27	26	25	24
PWMSYNCOUTXBAR1_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMSYNCOUTXBAR1_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMSYNCOUTXBAR1_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR1_G0_SEL							
R/W							
0h							

Table 3-2119. CONTROLSS_PWMSYNCOUTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMSYNCOUTXBAR1_G0_SEL	R/W	0h	EPWM pwmsyncout XBAR1 select 1:PWM[x] SYNCOUT selected 0:PWM[x] SYNCOUT is de-selected

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3.16.2.3 CONTROLSS_PWMSYNCOUTXBAR2_G0 Register

3.16.2.3.1 CONTROLSS_PWMSYNCOUTXBAR2_G0 Register (Offset = 180h) [reset = 0h]

EPWM pwmsyncout XBAR2 select.

Return to Summary Table

Table 3-2120. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2180h

Figure 3-1106. CONTROLSS_PWMSYNCOUTXBAR2_G0 Name Register

31	30	29	28	27	26	25	24
PWMSYNCOUTXBAR2_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMSYNCOUTXBAR2_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMSYNCOUTXBAR2_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR2_G0_SEL							
R/W							
0h							

Table 3-2121. CONTROLSS_PWMSYNCOUTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMSYNCOUTXBAR2_G0_SEL	R/W	0h	EPWM pwmsyncout XBAR2 select 1:PWM[x] SYNCOUT selected 0:PWM[x] SYNCOUT is de-selected

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3.16.2.4 CONTROLSS_PWMSYNCOUTXBAR3_G0 Register

3.16.2.4.1 CONTROLSS_PWMSYNCOUTXBAR3_G0 Register (Offset = 1C0h) [reset = 0h]

EPWM pwmsyncout XBAR2 select.

Return to Summary Table

Table 3-2122. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 21C0h

Figure 3-1107. CONTROLSS_PWMSYNCOUTXBAR3_G0 Name Register

31	30	29	28	27	26	25	24
PWMSYNCOUTXBAR3_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
PWMSYNCOUTXBAR3_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
PWMSYNCOUTXBAR3_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR3_G0_SEL							
R/W							
0h							

Table 3-2123. CONTROLSS_PWMSYNCOUTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PWMSYNCOUTXBAR3_G0_SEL	R/W	0h	EPWM pwmsyncout XBAR3 select 1:PWM[x] SYNCOUT selected 0:PWM[x] SYNCOUT is de-selected

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3.16.2.5 CONTROLSS_PWMSYNCOUTXBAR0_G1 Register

3.16.2.5.1 CONTROLSS_PWMSYNCOUTXBAR0_G1 Register (Offset = 200h) [reset = 0h]

EPWM pwmsyncout XBAR3 select.

Return to Summary Table

Table 3-2124. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2200h

Figure 3-1108. CONTROLSS_PWMSYNCOUTXBAR0_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PWMSYNCOUTXBAR0_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR0_G1_SEL							
R/W							
0h							

Table 3-2125. CONTROLSS_PWMSYNCOUTXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PWMSYNCOUTXBAR0_G1_SEL	R/W	0h	EPWM pwmsyncout XBAR0 select 1:ECAP[x] SYNCOUT selected 0:ECAP[x] SYNCOUT is de-selected

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3.16.2.6 CONTROLSS_PWMSYNCOUTXBAR1_G1 Register

3.16.2.6.1 CONTROLSS_PWMSYNCOUTXBAR1_G1 Register (Offset = 240h) [reset = 0h]

EPWM pwmsyncout XBAR3 select.

Return to Summary Table

Table 3-2126. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2240h

Figure 3-1109. CONTROLSS_PWMSYNCOUTXBAR1_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PWMSYNCOUTXBAR1_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR1_G1_SEL							
R/W							
0h							

Table 3-2127. CONTROLSS_PWMSYNCOUTXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PWMSYNCOUTXBAR1_G1_SEL	R/W	0h	EPWM pwmsyncout XBAR1 select 1:ECAP[x] SYNCOUT selected 0:ECAP[x] SYNCOUT is de-selected

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3.16.2.7 CONTROLSS_PWMSYNCOUTXBAR2_G1 Register

3.16.2.7.1 CONTROLSS_PWMSYNCOUTXBAR2_G1 Register (Offset = 280h) [reset = 0h]

EPWM pwmsyncout XBAR0 select.

Return to Summary Table

Table 3-2128. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2280h

Figure 3-1110. CONTROLSS_PWMSYNCOUTXBAR2_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PWMSYNCOUTXBAR2_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR2_G1_SEL							
R/W							
0h							

Table 3-2129. CONTROLSS_PWMSYNCOUTXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PWMSYNCOUTXBAR2_G1_SEL	R/W	0h	EPWM pwmsyncout XBAR2 select 1:ECAP[x] SYNCOUT selected 0:ECAP[x] SYNCOUT is de-selected

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3.16.2.8 CONTROLSS_PWMSYNCOUTXBAR3_G1 Register

3.16.2.8.1 CONTROLSS_PWMSYNCOUTXBAR3_G1 Register (Offset = 2C0h) [reset = 0h]

EPWM pwmsyncout XBAR1 select.

Return to Summary Table

Table 3-2130. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 22C0h

Figure 3-1111. CONTROLSS_PWMSYNCOUTXBAR3_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PWMSYNCOUTXBAR3_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
PWMSYNCOUTXBAR3_G1_SEL							
R/W							
0h							

Table 3-2131. CONTROLSS_PWMSYNCOUTXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PWMSYNCOUTXBAR3_G1_SEL	R/W	0h	EPWM pwmsyncout XBAR3 select 1:ECAP[x] SYNCOUT selected 0:ECAP[x] SYNCOUT is de-selected

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3.17 CONTROLSS_OUTPUTXBAR

CONTROLSS_OUTPUTXBAR

3.17.1 CONTROLSS_OUTPUTXBAR Summaries

CONTROLSS_OUTPUTXBAR Summaries

Table 3-2132. CONTROLSS Registers, Base Address=502D 8000h, Length=4096

Offset	Length	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
10h	32	CONTROLSS_OUTPUTXBAR_STATUS	502D 8010h
14h	32	CONTROLSS_OUTPUTXBAR_FLAGINVERT	502D 8014h
18h	32	CONTROLSS_OUTPUTXBAR_FLAG	502D 8018h
1Ch	32	CONTROLSS_OUTPUTXBAR_FLAG_CLR	502D 801Ch
20h	32	CONTROLSS_OUTPUTXBAR_FLAGFORCE	502D 8020h
24h	32	CONTROLSS_OUTPUTXBAR_OUTLATCH	502D 8024h
28h	32	CONTROLSS_OUTPUTXBAR_OUTSTRETCH	502D 8028h
2Ch	32	CONTROLSS_OUTPUTXBAR_OUTLENGTH	502D 802Ch
30h	32	CONTROLSS_OUTPUTXBAR_OUTINVERT	502D 8030h
100h	32	CONTROLSS_OUTPUTXBAR0_G0	502D 8100h
104h	32	CONTROLSS_OUTPUTXBAR0_G1	502D 8104h
108h	32	CONTROLSS_OUTPUTXBAR0_G2	502D 8108h
10Ch	32	CONTROLSS_OUTPUTXBAR0_G3	502D 810Ch
110h	32	CONTROLSS_OUTPUTXBAR0_G4	502D 8110h
114h	32	CONTROLSS_OUTPUTXBAR0_G5	502D 8114h
118h	32	CONTROLSS_OUTPUTXBAR0_G6	502D 8118h
11Ch	32	CONTROLSS_OUTPUTXBAR0_G7	502D 811Ch
120h	32	CONTROLSS_OUTPUTXBAR0_G8	502D 8120h
124h	32	CONTROLSS_OUTPUTXBAR0_G9	502D 8124h
128h	32	CONTROLSS_OUTPUTXBAR0_G10	502D 8128h
140h	32	CONTROLSS_OUTPUTXBAR1_G0	502D 8140h
144h	32	CONTROLSS_OUTPUTXBAR1_G1	502D 8144h
148h	32	CONTROLSS_OUTPUTXBAR1_G2	502D 8148h
14Ch	32	CONTROLSS_OUTPUTXBAR1_G3	502D 814Ch
150h	32	CONTROLSS_OUTPUTXBAR1_G4	502D 8150h
154h	32	CONTROLSS_OUTPUTXBAR1_G5	502D 8154h
158h	32	CONTROLSS_OUTPUTXBAR1_G6	502D 8158h
15Ch	32	CONTROLSS_OUTPUTXBAR1_G7	502D 815Ch
160h	32	CONTROLSS_OUTPUTXBAR1_G8	502D 8160h
164h	32	CONTROLSS_OUTPUTXBAR1_G9	502D 8164h
168h	32	CONTROLSS_OUTPUTXBAR1_G10	502D 8168h
180h	32	CONTROLSS_OUTPUTXBAR2_G0	502D 8180h
184h	32	CONTROLSS_OUTPUTXBAR2_G1	502D 8184h
188h	32	CONTROLSS_OUTPUTXBAR2_G2	502D 8188h
18Ch	32	CONTROLSS_OUTPUTXBAR2_G3	502D 818Ch
190h	32	CONTROLSS_OUTPUTXBAR2_G4	502D 8190h
194h	32	CONTROLSS_OUTPUTXBAR2_G5	502D 8194h
198h	32	CONTROLSS_OUTPUTXBAR2_G6	502D 8198h
19Ch	32	CONTROLSS_OUTPUTXBAR2_G7	502D 819Ch

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Table 3-2132. CONTROLSS Registers, Base Address=502D 8000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
1A0h	32	CONTROLSS_OUTPUTXBAR2_G8	502D 81A0h
1A4h	32	CONTROLSS_OUTPUTXBAR2_G9	502D 81A4h
1A8h	32	CONTROLSS_OUTPUTXBAR2_G10	502D 81A8h
1C0h	32	CONTROLSS_OUTPUTXBAR3_G0	502D 81C0h
1C4h	32	CONTROLSS_OUTPUTXBAR3_G1	502D 81C4h
1C8h	32	CONTROLSS_OUTPUTXBAR3_G2	502D 81C8h
1CCh	32	CONTROLSS_OUTPUTXBAR3_G3	502D 81CCh
1D0h	32	CONTROLSS_OUTPUTXBAR3_G4	502D 81D0h
1D4h	32	CONTROLSS_OUTPUTXBAR3_G5	502D 81D4h
1D8h	32	CONTROLSS_OUTPUTXBAR3_G6	502D 81D8h
1DCh	32	CONTROLSS_OUTPUTXBAR3_G7	502D 81DCh
1E0h	32	CONTROLSS_OUTPUTXBAR3_G8	502D 81E0h
1E4h	32	CONTROLSS_OUTPUTXBAR3_G9	502D 81E4h
1E8h	32	CONTROLSS_OUTPUTXBAR3_G10	502D 81E8h
200h	32	CONTROLSS_OUTPUTXBAR4_G0	502D 8200h
204h	32	CONTROLSS_OUTPUTXBAR4_G1	502D 8204h
208h	32	CONTROLSS_OUTPUTXBAR4_G2	502D 8208h
20Ch	32	CONTROLSS_OUTPUTXBAR4_G3	502D 820Ch
210h	32	CONTROLSS_OUTPUTXBAR4_G4	502D 8210h
214h	32	CONTROLSS_OUTPUTXBAR4_G5	502D 8214h
218h	32	CONTROLSS_OUTPUTXBAR4_G6	502D 8218h
21Ch	32	CONTROLSS_OUTPUTXBAR4_G7	502D 821Ch
220h	32	CONTROLSS_OUTPUTXBAR4_G8	502D 8220h
224h	32	CONTROLSS_OUTPUTXBAR4_G9	502D 8224h
228h	32	CONTROLSS_OUTPUTXBAR4_G10	502D 8228h
240h	32	CONTROLSS_OUTPUTXBAR5_G0	502D 8240h
244h	32	CONTROLSS_OUTPUTXBAR5_G1	502D 8244h
248h	32	CONTROLSS_OUTPUTXBAR5_G2	502D 8248h
24Ch	32	CONTROLSS_OUTPUTXBAR5_G3	502D 824Ch
250h	32	CONTROLSS_OUTPUTXBAR5_G4	502D 8250h
254h	32	CONTROLSS_OUTPUTXBAR5_G5	502D 8254h
258h	32	CONTROLSS_OUTPUTXBAR5_G6	502D 8258h
25Ch	32	CONTROLSS_OUTPUTXBAR5_G7	502D 825Ch
260h	32	CONTROLSS_OUTPUTXBAR5_G8	502D 8260h
264h	32	CONTROLSS_OUTPUTXBAR5_G9	502D 8264h
268h	32	CONTROLSS_OUTPUTXBAR5_G10	502D 8268h
280h	32	CONTROLSS_OUTPUTXBAR6_G0	502D 8280h
284h	32	CONTROLSS_OUTPUTXBAR6_G1	502D 8284h
288h	32	CONTROLSS_OUTPUTXBAR6_G2	502D 8288h
28Ch	32	CONTROLSS_OUTPUTXBAR6_G3	502D 828Ch
290h	32	CONTROLSS_OUTPUTXBAR6_G4	502D 8290h
294h	32	CONTROLSS_OUTPUTXBAR6_G5	502D 8294h
298h	32	CONTROLSS_OUTPUTXBAR6_G6	502D 8298h
29Ch	32	CONTROLSS_OUTPUTXBAR6_G7	502D 829Ch
2A0h	32	CONTROLSS_OUTPUTXBAR6_G8	502D 82A0h
2A4h	32	CONTROLSS_OUTPUTXBAR6_G9	502D 82A4h

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Table 3-2132. CONTROLSS Registers, Base Address=502D 8000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
2A8h	32	CONTROLSS_OUTPUTXBAR6_G10	502D 82A8h
2C0h	32	CONTROLSS_OUTPUTXBAR7_G0	502D 82C0h
2C4h	32	CONTROLSS_OUTPUTXBAR7_G1	502D 82C4h
2C8h	32	CONTROLSS_OUTPUTXBAR7_G2	502D 82C8h
2CCh	32	CONTROLSS_OUTPUTXBAR7_G3	502D 82CCh
2D0h	32	CONTROLSS_OUTPUTXBAR7_G4	502D 82D0h
2D4h	32	CONTROLSS_OUTPUTXBAR7_G5	502D 82D4h
2D8h	32	CONTROLSS_OUTPUTXBAR7_G6	502D 82D8h
2DCh	32	CONTROLSS_OUTPUTXBAR7_G7	502D 82DCh
2E0h	32	CONTROLSS_OUTPUTXBAR7_G8	502D 82E0h
2E4h	32	CONTROLSS_OUTPUTXBAR7_G9	502D 82E4h
2E8h	32	CONTROLSS_OUTPUTXBAR7_G10	502D 82E8h
300h	32	CONTROLSS_OUTPUTXBAR8_G0	502D 8300h
304h	32	CONTROLSS_OUTPUTXBAR8_G1	502D 8304h
308h	32	CONTROLSS_OUTPUTXBAR8_G2	502D 8308h
30Ch	32	CONTROLSS_OUTPUTXBAR8_G3	502D 830Ch
310h	32	CONTROLSS_OUTPUTXBAR8_G4	502D 8310h
314h	32	CONTROLSS_OUTPUTXBAR8_G5	502D 8314h
318h	32	CONTROLSS_OUTPUTXBAR8_G6	502D 8318h
31Ch	32	CONTROLSS_OUTPUTXBAR8_G7	502D 831Ch
320h	32	CONTROLSS_OUTPUTXBAR8_G8	502D 8320h
324h	32	CONTROLSS_OUTPUTXBAR8_G9	502D 8324h
328h	32	CONTROLSS_OUTPUTXBAR8_G10	502D 8328h
340h	32	CONTROLSS_OUTPUTXBAR9_G0	502D 8340h
344h	32	CONTROLSS_OUTPUTXBAR9_G1	502D 8344h
348h	32	CONTROLSS_OUTPUTXBAR9_G2	502D 8348h
34Ch	32	CONTROLSS_OUTPUTXBAR9_G3	502D 834Ch
350h	32	CONTROLSS_OUTPUTXBAR9_G4	502D 8350h
354h	32	CONTROLSS_OUTPUTXBAR9_G5	502D 8354h
358h	32	CONTROLSS_OUTPUTXBAR9_G6	502D 8358h
35Ch	32	CONTROLSS_OUTPUTXBAR9_G7	502D 835Ch
360h	32	CONTROLSS_OUTPUTXBAR9_G8	502D 8360h
364h	32	CONTROLSS_OUTPUTXBAR9_G9	502D 8364h
368h	32	CONTROLSS_OUTPUTXBAR9_G10	502D 8368h
380h	32	CONTROLSS_OUTPUTXBAR10_G0	502D 8380h
384h	32	CONTROLSS_OUTPUTXBAR10_G1	502D 8384h
388h	32	CONTROLSS_OUTPUTXBAR10_G2	502D 8388h
38Ch	32	CONTROLSS_OUTPUTXBAR10_G3	502D 838Ch
390h	32	CONTROLSS_OUTPUTXBAR10_G4	502D 8390h
394h	32	CONTROLSS_OUTPUTXBAR10_G5	502D 8394h
398h	32	CONTROLSS_OUTPUTXBAR10_G6	502D 8398h
39Ch	32	CONTROLSS_OUTPUTXBAR10_G7	502D 839Ch
3A0h	32	CONTROLSS_OUTPUTXBAR10_G8	502D 83A0h
3A4h	32	CONTROLSS_OUTPUTXBAR10_G9	502D 83A4h
3A8h	32	CONTROLSS_OUTPUTXBAR10_G10	502D 83A8h
3C0h	32	CONTROLSS_OUTPUTXBAR11_G0	502D 83C0h

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Table 3-2132. CONTROLSS Registers, Base Address=502D 8000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
3C4h	32	CONTROLSS_OUTPUTXBAR11_G1	502D 83C4h
3C8h	32	CONTROLSS_OUTPUTXBAR11_G2	502D 83C8h
3CCh	32	CONTROLSS_OUTPUTXBAR11_G3	502D 83CCh
3D0h	32	CONTROLSS_OUTPUTXBAR11_G4	502D 83D0h
3D4h	32	CONTROLSS_OUTPUTXBAR11_G5	502D 83D4h
3D8h	32	CONTROLSS_OUTPUTXBAR11_G6	502D 83D8h
3DCh	32	CONTROLSS_OUTPUTXBAR11_G7	502D 83DCh
3E0h	32	CONTROLSS_OUTPUTXBAR11_G8	502D 83E0h
3E4h	32	CONTROLSS_OUTPUTXBAR11_G9	502D 83E4h
3E8h	32	CONTROLSS_OUTPUTXBAR11_G10	502D 83E8h
400h	32	CONTROLSS_OUTPUTXBAR12_G0	502D 8400h
404h	32	CONTROLSS_OUTPUTXBAR12_G1	502D 8404h
408h	32	CONTROLSS_OUTPUTXBAR12_G2	502D 8408h
40Ch	32	CONTROLSS_OUTPUTXBAR12_G3	502D 840Ch
410h	32	CONTROLSS_OUTPUTXBAR12_G4	502D 8410h
414h	32	CONTROLSS_OUTPUTXBAR12_G5	502D 8414h
418h	32	CONTROLSS_OUTPUTXBAR12_G6	502D 8418h
41Ch	32	CONTROLSS_OUTPUTXBAR12_G7	502D 841Ch
420h	32	CONTROLSS_OUTPUTXBAR12_G8	502D 8420h
424h	32	CONTROLSS_OUTPUTXBAR12_G9	502D 8424h
428h	32	CONTROLSS_OUTPUTXBAR12_G10	502D 8428h
440h	32	CONTROLSS_OUTPUTXBAR13_G0	502D 8440h
444h	32	CONTROLSS_OUTPUTXBAR13_G1	502D 8444h
448h	32	CONTROLSS_OUTPUTXBAR13_G2	502D 8448h
44Ch	32	CONTROLSS_OUTPUTXBAR13_G3	502D 844Ch
450h	32	CONTROLSS_OUTPUTXBAR13_G4	502D 8450h
454h	32	CONTROLSS_OUTPUTXBAR13_G5	502D 8454h
458h	32	CONTROLSS_OUTPUTXBAR13_G6	502D 8458h
45Ch	32	CONTROLSS_OUTPUTXBAR13_G7	502D 845Ch
460h	32	CONTROLSS_OUTPUTXBAR13_G8	502D 8460h
464h	32	CONTROLSS_OUTPUTXBAR13_G9	502D 8464h
468h	32	CONTROLSS_OUTPUTXBAR13_G10	502D 8468h
480h	32	CONTROLSS_OUTPUTXBAR14_G0	502D 8480h
484h	32	CONTROLSS_OUTPUTXBAR14_G1	502D 8484h
488h	32	CONTROLSS_OUTPUTXBAR14_G2	502D 8488h
48Ch	32	CONTROLSS_OUTPUTXBAR14_G3	502D 848Ch
490h	32	CONTROLSS_OUTPUTXBAR14_G4	502D 8490h
494h	32	CONTROLSS_OUTPUTXBAR14_G5	502D 8494h
498h	32	CONTROLSS_OUTPUTXBAR14_G6	502D 8498h
49Ch	32	CONTROLSS_OUTPUTXBAR14_G7	502D 849Ch
4A0h	32	CONTROLSS_OUTPUTXBAR14_G8	502D 84A0h
4A4h	32	CONTROLSS_OUTPUTXBAR14_G9	502D 84A4h
4A8h	32	CONTROLSS_OUTPUTXBAR14_G10	502D 84A8h
4C0h	32	CONTROLSS_OUTPUTXBAR15_G0	502D 84C0h
4C4h	32	CONTROLSS_OUTPUTXBAR15_G1	502D 84C4h
4C8h	32	CONTROLSS_OUTPUTXBAR15_G2	502D 84C8h

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Table 3-2132. CONTROLSS Registers, Base Address=502D 8000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_OUTPUTXBAR Physical Address
4CCh	32	CONTROLSS_OUTPUTXBAR15_G3	502D 84CCh
4D0h	32	CONTROLSS_OUTPUTXBAR15_G4	502D 84D0h
4D4h	32	CONTROLSS_OUTPUTXBAR15_G5	502D 84D4h
4D8h	32	CONTROLSS_OUTPUTXBAR15_G6	502D 84D8h
4DCh	32	CONTROLSS_OUTPUTXBAR15_G7	502D 84DCh
4E0h	32	CONTROLSS_OUTPUTXBAR15_G8	502D 84E0h
4E4h	32	CONTROLSS_OUTPUTXBAR15_G9	502D 84E4h
4E8h	32	CONTROLSS_OUTPUTXBAR15_G10	502D 84E8h

3.17.2 CONTROLSS_OUTPUTXBAR Registers

CONTROLSS_OUTPUTXBAR Registers

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3.17.2.1 CONTROLSS_OUTPUTXBAR_STATUS Register

3.17.2.1.1 CONTROLSS_OUTPUTXBAR_STATUS Register (Offset = 10h) [reset = 0h]

Output Signal Status.

Return to Summary Table

Table 3-2133. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8010h

Figure 3-1112. CONTROLSS_OUTPUTXBAR_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR_STATUS_STS							
R							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR_STATUS_STS							
R							
0h							

Table 3-2134. CONTROLSS_OUTPUTXBAR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OUTPUTXBAR_STATUS_STS	R	0h	Status

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3.17.2.2 CONTROLSS_OUTPUTXBAR_FLAGINVERT Register

3.17.2.2.1 CONTROLSS_OUTPUTXBAR_FLAGINVERT Register (Offset = 14h) [reset = 0h]

Output Signal Invert Before Latch.

Return to Summary Table

Table 3-2135. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8014h

Figure 3-1113. CONTROLSS_OUTPUTXBAR_FLAGINVERT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR_FLAGINVERT_INVERT							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR_FLAGINVERT_INVERT							
R/W							
0h							

Table 3-2136. CONTROLSS_OUTPUTXBAR_FLAGINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OUTPUTXBAR_FLAGINVERT_INVERT	R/W	0h	FlagInvert

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3.17.2.3 CONTROLSS_OUTPUTXBAR_FLAG Register

3.17.2.3.1 CONTROLSS_OUTPUTXBAR_FLAG Register (Offset = 18h) [reset = 0h]

Output Signal Latched Flag.

Return to Summary Table

Table 3-2137. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8018h

Figure 3-1114. CONTROLSS_OUTPUTXBAR_FLAG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR_FLAG_BIT15	OUTPUTXBAR_FLAG_BIT14	OUTPUTXBAR_FLAG_BIT13	OUTPUTXBAR_FLAG_BIT12	OUTPUTXBAR_FLAG_BIT11	OUTPUTXBAR_FLAG_BIT10	OUTPUTXBAR_FLAG_BIT9	OUTPUTXBAR_FLAG_BIT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR_FLAG_BIT7	OUTPUTXBAR_FLAG_BIT6	OUTPUTXBAR_FLAG_BIT5	OUTPUTXBAR_FLAG_BIT4	OUTPUTXBAR_FLAG_BIT3	OUTPUTXBAR_FLAG_BIT2	OUTPUTXBAR_FLAG_BIT1	OUTPUTXBAR_FLAG_BIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-2138. CONTROLSS_OUTPUTXBAR_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	OUTPUTXBAR_FLAG_BIT15	R/W	0h	Output XBAR flag
14	OUTPUTXBAR_FLAG_BIT14	R/W	0h	Output XBAR flag
13	OUTPUTXBAR_FLAG_BIT13	R/W	0h	Output XBAR flag
12	OUTPUTXBAR_FLAG_BIT12	R/W	0h	Output XBAR flag
11	OUTPUTXBAR_FLAG_BIT11	R/W	0h	Output XBAR flag
10	OUTPUTXBAR_FLAG_BIT10	R/W	0h	Output XBAR flag
9	OUTPUTXBAR_FLAG_BIT9	R/W	0h	Output XBAR flag
8	OUTPUTXBAR_FLAG_BIT8	R/W	0h	Output XBAR flag
7	OUTPUTXBAR_FLAG_BIT7	R/W	0h	Output XBAR flag
6	OUTPUTXBAR_FLAG_BIT6	R/W	0h	Output XBAR flag

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Table 3-2138. CONTROLSS_OUTPUTXBAR_FLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	OUTPUTXBAR_FLAG_BIT5	R/W	0h	Output XBAR flag
4	OUTPUTXBAR_FLAG_BIT4	R/W	0h	Output XBAR flag
3	OUTPUTXBAR_FLAG_BIT3	R/W	0h	Output XBAR flag
2	OUTPUTXBAR_FLAG_BIT2	R/W	0h	Output XBAR flag
1	OUTPUTXBAR_FLAG_BIT1	R/W	0h	Output XBAR flag
0	OUTPUTXBAR_FLAG_BIT0	R/W	0h	Output XBAR flag

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3.17.2.4 CONTROLSS_OUTPUTXBAR_FLAG_CLR Register

3.17.2.4.1 CONTROLSS_OUTPUTXBAR_FLAG_CLR Register (Offset = 1Ch) [reset = 0h]

Output Signal Latched Flag Clear.

Return to Summary Table

Table 3-2139. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 801Ch

Figure 3-1115. CONTROLSS_OUTPUTXBAR_FLAG_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR_FLAG_CLR_BIT15	OUTPUTXBAR_FLAG_CLR_BIT14	OUTPUTXBAR_FLAG_CLR_BIT13	OUTPUTXBAR_FLAG_CLR_BIT12	OUTPUTXBAR_FLAG_CLR_BIT11	OUTPUTXBAR_FLAG_CLR_BIT10	OUTPUTXBAR_FLAG_CLR_BIT9	OUTPUTXBAR_FLAG_CLR_BIT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
OUTPUTXBAR_FLAG_CLR_BIT7	OUTPUTXBAR_FLAG_CLR_BIT6	OUTPUTXBAR_FLAG_CLR_BIT5	OUTPUTXBAR_FLAG_CLR_BIT4	OUTPUTXBAR_FLAG_CLR_BIT3	OUTPUTXBAR_FLAG_CLR_BIT2	OUTPUTXBAR_FLAG_CLR_BIT1	OUTPUTXBAR_FLAG_CLR_BIT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-2140. CONTROLSS_OUTPUTXBAR_FLAG_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	OUTPUTXBAR_FLAG_CLR_BIT15	R/W	0h	Output XBAR flag clear
14	OUTPUTXBAR_FLAG_CLR_BIT14	R/W	0h	Output XBAR flag clear
13	OUTPUTXBAR_FLAG_CLR_BIT13	R/W	0h	Output XBAR flag clear
12	OUTPUTXBAR_FLAG_CLR_BIT12	R/W	0h	Output XBAR flag clear
11	OUTPUTXBAR_FLAG_CLR_BIT11	R/W	0h	Output XBAR flag clear
10	OUTPUTXBAR_FLAG_CLR_BIT10	R/W	0h	Output XBAR flag clear
9	OUTPUTXBAR_FLAG_CLR_BIT9	R/W	0h	Output XBAR flag clear
8	OUTPUTXBAR_FLAG_CLR_BIT8	R/W	0h	Output XBAR flag clear
7	OUTPUTXBAR_FLAG_CLR_BIT7	R/W	0h	Output XBAR flag clear

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Table 3-2140. CONTROLSS_OUTPUTXBAR_FLAG_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUTPUTXBAR_FLAG_CLR_BIT6	R/W	0h	Output XBAR flag clear
5	OUTPUTXBAR_FLAG_CLR_BIT5	R/W	0h	Output XBAR flag clear
4	OUTPUTXBAR_FLAG_CLR_BIT4	R/W	0h	Output XBAR flag clear
3	OUTPUTXBAR_FLAG_CLR_BIT3	R/W	0h	Output XBAR flag clear
2	OUTPUTXBAR_FLAG_CLR_BIT2	R/W	0h	Output XBAR flag clear
1	OUTPUTXBAR_FLAG_CLR_BIT1	R/W	0h	Output XBAR flag clear
0	OUTPUTXBAR_FLAG_CLR_BIT0	R/W	0h	Output XBAR flag clear

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3.17.2.5 CONTROLSS_OUTPUTXBAR_FLAGFORCE Register

3.17.2.5.1 CONTROLSS_OUTPUTXBAR_FLAGFORCE Register (Offset = 20h) [reset = 0h]

Output Signal Latched Flag Force.

Return to Summary Table

Table 3-2141. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8020h

Figure 3-1116. CONTROLSS_OUTPUTXBAR_FLAGFORCE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR_FLAGFORCE_FRC							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR_FLAGFORCE_FRC							
R/W							
0h							

Table 3-2142. CONTROLSS_OUTPUTXBAR_FLAGFORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OUTPUTXBAR_FLAGFORCE_FRC	R/W	0h	FlagForce

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3.17.2.6 CONTROLSS_OUTPUTXBAR_OUTLATCH Register

3.17.2.6.1 CONTROLSS_OUTPUTXBAR_OUTLATCH Register (Offset = 24h) [reset = 0h]

Output Signal Select Latch.

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Table 3-2143. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8024h

Figure 3-1117. CONTROLSS_OUTPUTXBAR_OUTLATCH Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR_OUTLATCH_LATCHSEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR_OUTLATCH_LATCHSEL							
R/W							
0h							

Table 3-2144. CONTROLSS_OUTPUTXBAR_OUTLATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OUTPUTXBAR_OUTLATCH_LATCHSEL	R/W	0h	OutLatch

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3.17.2.7 CONTROLSS_OUTPUTXBAR_OUTSTRETCH Register

3.17.2.7.1 CONTROLSS_OUTPUTXBAR_OUTSTRETCH Register (Offset = 28h) [reset = 0h]

Output Signal Stretched Pulse Version Select.

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Table 3-2145. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8028h

Figure 3-1118. CONTROLSS_OUTPUTXBAR_OUTSTRETCH Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR_OUTSTRETCH_STRETCHSEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR_OUTSTRETCH_STRETCHSEL							
R/W							
0h							

Table 3-2146. CONTROLSS_OUTPUTXBAR_OUTSTRETCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OUTPUTXBAR_OUTSTRETCH_STRETCHSEL	R/W	0h	OutStretch

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3.17.2.8 CONTROLSS_OUTPUTXBAR_OUTLENGTH Register

3.17.2.8.1 CONTROLSS_OUTPUTXBAR_OUTLENGTH Register (Offset = 2Ch) [reset = 0h]

Output Signal Stretched Pulse Length Select.

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Table 3-2147. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 802Ch

Figure 3-1119. CONTROLSS_OUTPUTXBAR_OUTLENGTH Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR_OUTLENGTH_LENGTHSEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR_OUTLENGTH_LENGTHSEL							
R/W							
0h							

Table 3-2148. CONTROLSS_OUTPUTXBAR_OUTLENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OUTPUTXBAR_OUTLENGTH_LENGTHSEL	R/W	0h	OutLength

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3.17.2.9 CONTROLSS_OUTPUTXBAR_OUTINVERT Register

3.17.2.9.1 CONTROLSS_OUTPUTXBAR_OUTINVERT Register (Offset = 30h) [reset = 0h]

Output Signal Invert Select.

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Table 3-2149. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8030h

Figure 3-1120. CONTROLSS_OUTPUTXBAR_OUTINVERT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR_OUTINVERT_OUTINVERT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR_OUTINVERT_OUTINVERT							
R/W							
0h							

Table 3-2150. CONTROLSS_OUTPUTXBAR_OUTINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	OUTPUTXBAR_OUTINVERT_OUTINVERT	R/W	0h	OutInvert

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3.17.2.10 CONTROLSS_OUTPUTXBAR0_G0 Register

3.17.2.10.1 CONTROLSS_OUTPUTXBAR0_G0 Register (Offset = 100h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2151. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8100h

Figure 3-1121. CONTROLSS_OUTPUTXBAR0_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR0_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR0_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR0_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR0_G0_SEL							
R/W							
0h							

Table 3-2152. CONTROLSS_OUTPUTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR0_G0_SEL	R/W	0h	G0: PWM XBAR0 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.11 CONTROLSS_OUTPUTXBAR0_G1 Register

3.17.2.11.1 CONTROLSS_OUTPUTXBAR0_G1 Register (Offset = 104h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2153. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8104h

Figure 3-1122. CONTROLSS_OUTPUTXBAR0_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR0_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR0_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR0_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR0_G1_SEL							
R/W							
0h							

Table 3-2154. CONTROLSS_OUTPUTXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR0_G1_SEL	R/W	0h	G1: OUTPUT XBAR0 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.12 CONTROLSS_OUTPUTXBAR0_G2 Register

3.17.2.12.1 CONTROLSS_OUTPUTXBAR0_G2 Register (Offset = 108h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2155. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8108h

Figure 3-1123. CONTROLSS_OUTPUTXBAR0_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR0_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR0_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR0_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR0_G2_SEL							
R/W							
0h							

Table 3-2156. CONTROLSS_OUTPUTXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR0_G2_SEL	R/W	0h	G2: OUTPUT XBAR0 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.13 CONTROLSS_OUTPUTXBAR0_G3 Register

3.17.2.13.1 CONTROLSS_OUTPUTXBAR0_G3 Register (Offset = 10Ch) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2157. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 810Ch

Figure 3-1124. CONTROLSS_OUTPUTXBAR0_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR0_G3_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR0_G3_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR0_G3_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR0_G3_SEL							
R/W							
0h							

Table 3-2158. CONTROLSS_OUTPUTXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR0_G3_SEL	R/W	0h	G3: OUTPUT XBAR0 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.14 CONTROLSS_OUTPUTXBAR0_G4 Register

3.17.2.14.1 CONTROLSS_OUTPUTXBAR0_G4 Register (Offset = 110h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2159. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8110h

Figure 3-1125. CONTROLSS_OUTPUTXBAR0_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR0_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR0_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR0_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR0_G4_SEL							
R/W							
0h							

Table 3-2160. CONTROLSS_OUTPUTXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR0_G4_SEL	R/W	0h	G4: OUTPUT XBAR0 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.15 CONTROLSS_OUTPUTXBAR0_G5 Register

3.17.2.15.1 CONTROLSS_OUTPUTXBAR0_G5 Register (Offset = 114h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2161. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8114h

Figure 3-1126. CONTROLSS_OUTPUTXBAR0_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR0_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR0_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR0_G5_SEL							
R/W							
0h							

Table 3-2162. CONTROLSS_OUTPUTXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR0_G5_SEL	R/W	0h	G5: OUTPUT XBAR0 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.16 CONTROLSS_OUTPUTXBAR0_G6 Register

3.17.2.16.1 CONTROLSS_OUTPUTXBAR0_G6 Register (Offset = 118h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2163. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8118h

Figure 3-1127. CONTROLSS_OUTPUTXBAR0_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OUTPUTXBAR0_G6_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR0_G6_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR0_G6_SEL							
R/W							
0h							

Table 3-2164. CONTROLSS_OUTPUTXBAR0_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR0_G6_SEL	R/W	0h	G6: OUTPUT XBAR0 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.17 CONTROLSS_OUTPUTXBAR0_G7 Register

3.17.2.17.1 CONTROLSS_OUTPUTXBAR0_G7 Register (Offset = 11Ch) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2165. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 811Ch

Figure 3-1128. CONTROLSS_OUTPUTXBAR0_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR0_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR0_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR0_G7_SEL							
R/W							
0h							

Table 3-2166. CONTROLSS_OUTPUTXBAR0_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR0_G7_SEL	R/W	0h	G7: OUTPUT XBAR0 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.18 CONTROLSS_OUTPUTXBAR0_G8 Register

3.17.2.18.1 CONTROLSS_OUTPUTXBAR0_G8 Register (Offset = 120h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2167. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8120h

Figure 3-1129. CONTROLSS_OUTPUTXBAR0_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR0_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR0_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR0_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR0_G8_SEL							
R/W							
0h							

Table 3-2168. CONTROLSS_OUTPUTXBAR0_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2168. CONTROLSS_OUTPUTXBAR0_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR0_G8_SEL	R/W	0h	G8: OUTPUT XBAR0 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.19 CONTROLSS_OUTPUTXBAR0_G9 Register

3.17.2.19.1 CONTROLSS_OUTPUTXBAR0_G9 Register (Offset = 124h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2169. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8124h

Figure 3-1130. CONTROLSS_OUTPUTXBAR0_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR0_G9_SEL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
OUTPUTXBAR0_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR0_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR0_G9_SEL							
R/W							
0h							

Table 3-2170. CONTROLSS_OUTPUTXBAR0_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2170. CONTROLSS_OUTPUTXBAR0_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR0_G9_SEL	R/W	0h	G9: OUTPUT XBAR0 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.20 CONTROLSS_OUTPUTXBAR0_G10 Register

3.17.2.20.1 CONTROLSS_OUTPUTXBAR0_G10 Register (Offset = 128h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

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Table 3-2171. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8128h

Figure 3-1131. CONTROLSS_OUTPUTXBAR0_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		OUTPUTXBAR0_G10_SEL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
OUTPUTXBAR0_G10_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR0_G10_SEL							
R/W							
0h							

Table 3-2172. CONTROLSS_OUTPUTXBAR0_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR0_G10_SEL	R/W	0h	G10: OUTPUT XBAR0 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.21 CONTROLSS_OUTPUTXBAR1_G0 Register

3.17.2.21.1 CONTROLSS_OUTPUTXBAR1_G0 Register (Offset = 140h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

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Table 3-2173. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8140h

Figure 3-1132. CONTROLSS_OUTPUTXBAR1_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR1_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR1_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR1_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR1_G0_SEL							
R/W							
0h							

Table 3-2174. CONTROLSS_OUTPUTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR1_G0_SEL	R/W	0h	G0: PWM XBAR1 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.22 CONTROLSS_OUTPUTXBAR1_G1 Register

3.17.2.22.1 CONTROLSS_OUTPUTXBAR1_G1 Register (Offset = 144h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to Summary Table

Table 3-2175. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8144h

Figure 3-1133. CONTROLSS_OUTPUTXBAR1_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR1_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR1_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR1_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR1_G1_SEL							
R/W							
0h							

Table 3-2176. CONTROLSS_OUTPUTXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR1_G1_SEL	R/W	0h	G1: OUTPUT XBAR1 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.23 CONTROLSS_OUTPUTXBAR1_G2 Register

3.17.2.23.1 CONTROLSS_OUTPUTXBAR1_G2 Register (Offset = 148h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to Summary Table

Table 3-2177. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8148h

Figure 3-1134. CONTROLSS_OUTPUTXBAR1_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR1_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR1_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR1_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR1_G2_SEL							
R/W							
0h							

Table 3-2178. CONTROLSS_OUTPUTXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR1_G2_SEL	R/W	0h	G2: OUTPUT XBAR1 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.24 CONTROLSS_OUTPUTXBAR1_G3 Register

3.17.2.24.1 CONTROLSS_OUTPUTXBAR1_G3 Register (Offset = 14Ch) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to Summary Table

Table 3-2179. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 814Ch

Figure 3-1135. CONTROLSS_OUTPUTXBAR1_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR1_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR1_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR1_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR1_G3_SEL							
R/W							
0h							

Table 3-2180. CONTROLSS_OUTPUTXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR1_G3_SEL	R/W	0h	G3: OUTPUT XBAR1 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.25 CONTROLSS_OUTPUTXBAR1_G4 Register

3.17.2.25.1 CONTROLSS_OUTPUTXBAR1_G4 Register (Offset = 150h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to Summary Table

Table 3-2181. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8150h

Figure 3-1136. CONTROLSS_OUTPUTXBAR1_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR1_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR1_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR1_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR1_G4_SEL							
R/W							
0h							

Table 3-2182. CONTROLSS_OUTPUTXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR1_G4_SEL	R/W	0h	G4: OUTPUT XBAR1 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.26 CONTROLSS_OUTPUTXBAR1_G5 Register

3.17.2.26.1 CONTROLSS_OUTPUTXBAR1_G5 Register (Offset = 154h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

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Table 3-2183. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8154h

Figure 3-1137. CONTROLSS_OUTPUTXBAR1_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR1_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR1_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR1_G5_SEL							
R/W							
0h							

Table 3-2184. CONTROLSS_OUTPUTXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR1_G5_SEL	R/W	0h	G5: OUTPUT XBAR1 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.27 CONTROLSS_OUTPUTXBAR1_G6 Register

3.17.2.27.1 CONTROLSS_OUTPUTXBAR1_G6 Register (Offset = 158h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

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Table 3-2185. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8158h

Figure 3-1138. CONTROLSS_OUTPUTXBAR1_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR1_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR1_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR1_G6_SEL							
R/W							
0h							

Table 3-2186. CONTROLSS_OUTPUTXBAR1_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR1_G6_SEL	R/W	0h	G6: OUTPUT XBAR1 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.28 CONTROLSS_OUTPUTXBAR1_G7 Register

3.17.2.28.1 CONTROLSS_OUTPUTXBAR1_G7 Register (Offset = 15Ch) [reset = 0h]

OUTPUT XBAR 1 Input Select.

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Table 3-2187. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 815Ch

Figure 3-1139. CONTROLSS_OUTPUTXBAR1_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR1_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR1_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR1_G7_SEL							
R/W							
0h							

Table 3-2188. CONTROLSS_OUTPUTXBAR1_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR1_G7_SEL	R/W	0h	G7: OUTPUT XBAR1 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.29 CONTROLSS_OUTPUTXBAR1_G8 Register

3.17.2.29.1 CONTROLSS_OUTPUTXBAR1_G8 Register (Offset = 160h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to Summary Table

Table 3-2189. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8160h

Figure 3-1140. CONTROLSS_OUTPUTXBAR1_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR1_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR1_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR1_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR1_G8_SEL							
R/W							
0h							

Table 3-2190. CONTROLSS_OUTPUTXBAR1_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2190. CONTROLSS_OUTPUTXBAR1_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR1_G8_SEL	R/W	0h	G8: OUTPUT XBAR1 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.30 CONTROLSS_OUTPUTXBAR1_G9 Register

3.17.2.30.1 CONTROLSS_OUTPUTXBAR1_G9 Register (Offset = 164h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

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Table 3-2191. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8164h

Figure 3-1141. CONTROLSS_OUTPUTXBAR1_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR1_G9_SEL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
OUTPUTXBAR1_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR1_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR1_G9_SEL							
R/W							
0h							

Table 3-2192. CONTROLSS_OUTPUTXBAR1_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2192. CONTROLSS_OUTPUTXBAR1_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR1_G9_SEL	R/W	0h	G9: OUTPUT XBAR1 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.31 CONTROLSS_OUTPUTXBAR1_G10 Register

3.17.2.31.1 CONTROLSS_OUTPUTXBAR1_G10 Register (Offset = 168h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to Summary Table

Table 3-2193. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8168h

Figure 3-1142. CONTROLSS_OUTPUTXBAR1_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		OUTPUTXBAR1_G10_SEL					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR1_G10_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR1_G10_SEL							
R/W							
0h							

Table 3-2194. CONTROLSS_OUTPUTXBAR1_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR1_G10_SEL	R/W	0h	G10: OUTPUT XBAR1 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.32 CONTROLSS_OUTPUTXBAR2_G0 Register

3.17.2.32.1 CONTROLSS_OUTPUTXBAR2_G0 Register (Offset = 180h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

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Table 3-2195. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8180h

Figure 3-1143. CONTROLSS_OUTPUTXBAR2_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR2_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR2_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR2_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR2_G0_SEL							
R/W							
0h							

Table 3-2196. CONTROLSS_OUTPUTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR2_G0_SEL	R/W	0h	G0: PWM XBAR2 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.33 CONTROLSS_OUTPUTXBAR2_G1 Register

3.17.2.33.1 CONTROLSS_OUTPUTXBAR2_G1 Register (Offset = 184h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to Summary Table

Table 3-2197. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8184h

Figure 3-1144. CONTROLSS_OUTPUTXBAR2_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR2_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR2_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR2_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR2_G1_SEL							
R/W							
0h							

Table 3-2198. CONTROLSS_OUTPUTXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR2_G1_SEL	R/W	0h	G1: OUTPUT XBAR2 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.34 CONTROLSS_OUTPUTXBAR2_G2 Register

3.17.2.34.1 CONTROLSS_OUTPUTXBAR2_G2 Register (Offset = 188h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to Summary Table

Table 3-2199. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8188h

Figure 3-1145. CONTROLSS_OUTPUTXBAR2_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR2_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR2_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR2_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR2_G2_SEL							
R/W							
0h							

Table 3-2200. CONTROLSS_OUTPUTXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR2_G2_SEL	R/W	0h	G2: OUTPUT XBAR2 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.35 CONTROLSS_OUTPUTXBAR2_G3 Register

3.17.2.35.1 CONTROLSS_OUTPUTXBAR2_G3 Register (Offset = 18Ch) [reset = 0h]

OUTPUT XBAR 2 Input Select.

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Table 3-2201. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 818Ch

Figure 3-1146. CONTROLSS_OUTPUTXBAR2_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR2_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR2_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR2_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR2_G3_SEL							
R/W							
0h							

Table 3-2202. CONTROLSS_OUTPUTXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR2_G3_SEL	R/W	0h	G3: OUTPUT XBAR2 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.36 CONTROLSS_OUTPUTXBAR2_G4 Register

3.17.2.36.1 CONTROLSS_OUTPUTXBAR2_G4 Register (Offset = 190h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

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Table 3-2203. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8190h

Figure 3-1147. CONTROLSS_OUTPUTXBAR2_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR2_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR2_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR2_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR2_G4_SEL							
R/W							
0h							

Table 3-2204. CONTROLSS_OUTPUTXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR2_G4_SEL	R/W	0h	G4: OUTPUT XBAR2 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.37 CONTROLSS_OUTPUTXBAR2_G5 Register

3.17.2.37.1 CONTROLSS_OUTPUTXBAR2_G5 Register (Offset = 194h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

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Table 3-2205. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8194h

Figure 3-1148. CONTROLSS_OUTPUTXBAR2_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR2_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR2_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR2_G5_SEL							
R/W							
0h							

Table 3-2206. CONTROLSS_OUTPUTXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR2_G5_SEL	R/W	0h	G5: OUTPUT XBAR2 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.38 CONTROLSS_OUTPUTXBAR2_G6 Register

3.17.2.38.1 CONTROLSS_OUTPUTXBAR2_G6 Register (Offset = 198h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to Summary Table

Table 3-2207. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8198h

Figure 3-1149. CONTROLSS_OUTPUTXBAR2_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OUTPUTXBAR2_G6_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR2_G6_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR2_G6_SEL							
R/W							
0h							

Table 3-2208. CONTROLSS_OUTPUTXBAR2_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR2_G6_SEL	R/W	0h	G6: OUTPUT XBAR2 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.39 CONTROLSS_OUTPUTXBAR2_G7 Register

3.17.2.39.1 CONTROLSS_OUTPUTXBAR2_G7 Register (Offset = 19Ch) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to Summary Table

Table 3-2209. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 819Ch

Figure 3-1150. CONTROLSS_OUTPUTXBAR2_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OUTPUTXBAR2_G7_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR2_G7_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR2_G7_SEL							
R/W							
0h							

Table 3-2210. CONTROLSS_OUTPUTXBAR2_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR2_G7_SEL	R/W	0h	G7: OUTPUT XBAR2 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.40 CONTROLSS_OUTPUTXBAR2_G8 Register

3.17.2.40.1 CONTROLSS_OUTPUTXBAR2_G8 Register (Offset = 1A0h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

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Table 3-2211. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81A0h

Figure 3-1151. CONTROLSS_OUTPUTXBAR2_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR2_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR2_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR2_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR2_G8_SEL							
R/W							
0h							

Table 3-2212. CONTROLSS_OUTPUTXBAR2_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2212. CONTROLSS_OUTPUTXBAR2_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR2_G8_SEL	R/W	0h	G8: OUTPUT XBAR2 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.41 CONTROLSS_OUTPUTXBAR2_G9 Register

3.17.2.41.1 CONTROLSS_OUTPUTXBAR2_G9 Register (Offset = 1A4h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to Summary Table

Table 3-2213. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81A4h

Figure 3-1152. CONTROLSS_OUTPUTXBAR2_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR2_G9_SEL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
OUTPUTXBAR2_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR2_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR2_G9_SEL							
R/W							
0h							

Table 3-2214. CONTROLSS_OUTPUTXBAR2_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2214. CONTROLSS_OUTPUTXBAR2_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR2_G9_SEL	R/W	0h	G9: OUTPUT XBAR2 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.42 CONTROLSS_OUTPUTXBAR2_G10 Register

3.17.2.42.1 CONTROLSS_OUTPUTXBAR2_G10 Register (Offset = 1A8h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

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Table 3-2215. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81A8h

Figure 3-1153. CONTROLSS_OUTPUTXBAR2_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		OUTPUTXBAR2_G10_SEL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
OUTPUTXBAR2_G10_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR2_G10_SEL							
R/W							
0h							

Table 3-2216. CONTROLSS_OUTPUTXBAR2_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR2_G10_SEL	R/W	0h	G10: OUTPUT XBAR2 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.43 CONTROLSS_OUTPUTXBAR3_G0 Register

3.17.2.43.1 CONTROLSS_OUTPUTXBAR3_G0 Register (Offset = 1C0h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to Summary Table

Table 3-2217. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81C0h

Figure 3-1154. CONTROLSS_OUTPUTXBAR3_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR3_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR3_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR3_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR3_G0_SEL							
R/W							
0h							

Table 3-2218. CONTROLSS_OUTPUTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR3_G0_SEL	R/W	0h	G0: PWM XBAR3 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.44 CONTROLSS_OUTPUTXBAR3_G1 Register

3.17.2.44.1 CONTROLSS_OUTPUTXBAR3_G1 Register (Offset = 1C4h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to Summary Table

Table 3-2219. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81C4h

Figure 3-1155. CONTROLSS_OUTPUTXBAR3_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR3_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR3_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR3_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR3_G1_SEL							
R/W							
0h							

Table 3-2220. CONTROLSS_OUTPUTXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR3_G1_SEL	R/W	0h	G1: OUTPUT XBAR3 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.45 CONTROLSS_OUTPUTXBAR3_G2 Register

3.17.2.45.1 CONTROLSS_OUTPUTXBAR3_G2 Register (Offset = 1C8h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to Summary Table

Table 3-2221. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81C8h

Figure 3-1156. CONTROLSS_OUTPUTXBAR3_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR3_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR3_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR3_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR3_G2_SEL							
R/W							
0h							

Table 3-2222. CONTROLSS_OUTPUTXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR3_G2_SEL	R/W	0h	G2: OUTPUT XBAR3 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.46 CONTROLSS_OUTPUTXBAR3_G3 Register

3.17.2.46.1 CONTROLSS_OUTPUTXBAR3_G3 Register (Offset = 1CCh) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to Summary Table

Table 3-2223. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81CCh

Figure 3-1157. CONTROLSS_OUTPUTXBAR3_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR3_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR3_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR3_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR3_G3_SEL							
R/W							
0h							

Table 3-2224. CONTROLSS_OUTPUTXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR3_G3_SEL	R/W	0h	G3: OUTPUT XBAR3 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.47 CONTROLSS_OUTPUTXBAR3_G4 Register

3.17.2.47.1 CONTROLSS_OUTPUTXBAR3_G4 Register (Offset = 1D0h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to Summary Table

Table 3-2225. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81D0h

Figure 3-1158. CONTROLSS_OUTPUTXBAR3_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR3_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR3_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR3_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR3_G4_SEL							
R/W							
0h							

Table 3-2226. CONTROLSS_OUTPUTXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR3_G4_SEL	R/W	0h	G4: OUTPUT XBAR3 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.48 CONTROLSS_OUTPUTXBAR3_G5 Register

3.17.2.48.1 CONTROLSS_OUTPUTXBAR3_G5 Register (Offset = 1D4h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to Summary Table

Table 3-2227. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81D4h

Figure 3-1159. CONTROLSS_OUTPUTXBAR3_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR3_G5_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR3_G5_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR3_G5_SEL							
R/W							
0h							

Table 3-2228. CONTROLSS_OUTPUTXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR3_G5_SEL	R/W	0h	G5: OUTPUT XBAR3 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.49 CONTROLSS_OUTPUTXBAR3_G6 Register

3.17.2.49.1 CONTROLSS_OUTPUTXBAR3_G6 Register (Offset = 1D8h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to Summary Table

Table 3-2229. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81D8h

Figure 3-1160. CONTROLSS_OUTPUTXBAR3_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR3_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR3_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR3_G6_SEL							
R/W							
0h							

Table 3-2230. CONTROLSS_OUTPUTXBAR3_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR3_G6_SEL	R/W	0h	G6: OUTPUT XBAR3 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.50 CONTROLSS_OUTPUTXBAR3_G7 Register

3.17.2.50.1 CONTROLSS_OUTPUTXBAR3_G7 Register (Offset = 1DCh) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to Summary Table

Table 3-2231. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81DCh

Figure 3-1161. CONTROLSS_OUTPUTXBAR3_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR3_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR3_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR3_G7_SEL							
R/W							
0h							

Table 3-2232. CONTROLSS_OUTPUTXBAR3_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR3_G7_SEL	R/W	0h	G7: OUTPUT XBAR3 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.51 CONTROLSS_OUTPUTXBAR3_G8 Register

3.17.2.51.1 CONTROLSS_OUTPUTXBAR3_G8 Register (Offset = 1E0h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to Summary Table

Table 3-2233. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81E0h

Figure 3-1162. CONTROLSS_OUTPUTXBAR3_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR3_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR3_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR3_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR3_G8_SEL							
R/W							
0h							

Table 3-2234. CONTROLSS_OUTPUTXBAR3_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2234. CONTROLSS_OUTPUTXBAR3_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR3_G8_SEL	R/W	0h	G8: OUTPUT XBAR3 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.52 CONTROLSS_OUTPUTXBAR3_G9 Register

3.17.2.52.1 CONTROLSS_OUTPUTXBAR3_G9 Register (Offset = 1E4h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to Summary Table

Table 3-2235. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81E4h

Figure 3-1163. CONTROLSS_OUTPUTXBAR3_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR3_G9_SEL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
OUTPUTXBAR3_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR3_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR3_G9_SEL							
R/W							
0h							

Table 3-2236. CONTROLSS_OUTPUTXBAR3_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2236. CONTROLSS_OUTPUTXBAR3_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR3_G9_SEL	R/W	0h	G9: OUTPUT XBAR3 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.53 CONTROLSS_OUTPUTXBAR3_G10 Register

3.17.2.53.1 CONTROLSS_OUTPUTXBAR3_G10 Register (Offset = 1E8h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

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Table 3-2237. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 81E8h

Figure 3-1164. CONTROLSS_OUTPUTXBAR3_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		OUTPUTXBAR3_G10_SEL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
OUTPUTXBAR3_G10_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR3_G10_SEL							
R/W							
0h							

Table 3-2238. CONTROLSS_OUTPUTXBAR3_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR3_G10_SEL	R/W	0h	G10: OUTPUT XBAR3 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.54 CONTROLSS_OUTPUTXBAR4_G0 Register

3.17.2.54.1 CONTROLSS_OUTPUTXBAR4_G0 Register (Offset = 200h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

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Table 3-2239. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8200h

Figure 3-1165. CONTROLSS_OUTPUTXBAR4_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR4_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR4_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G0_SEL							
R/W							
0h							

Table 3-2240. CONTROLSS_OUTPUTXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR4_G0_SEL	R/W	0h	G0: PWM XBAR4 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.55 CONTROLSS_OUTPUTXBAR4_G1 Register

3.17.2.55.1 CONTROLSS_OUTPUTXBAR4_G1 Register (Offset = 204h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to Summary Table

Table 3-2241. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8204h

Figure 3-1166. CONTROLSS_OUTPUTXBAR4_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR4_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR4_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G1_SEL							
R/W							
0h							

Table 3-2242. CONTROLSS_OUTPUTXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR4_G1_SEL	R/W	0h	G1: OUTPUT XBAR4 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.56 CONTROLSS_OUTPUTXBAR4_G2 Register

3.17.2.56.1 CONTROLSS_OUTPUTXBAR4_G2 Register (Offset = 208h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

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Table 3-2243. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8208h

Figure 3-1167. CONTROLSS_OUTPUTXBAR4_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR4_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR4_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G2_SEL							
R/W							
0h							

Table 3-2244. CONTROLSS_OUTPUTXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR4_G2_SEL	R/W	0h	G2: OUTPUT XBAR4 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.57 CONTROLSS_OUTPUTXBAR4_G3 Register

3.17.2.57.1 CONTROLSS_OUTPUTXBAR4_G3 Register (Offset = 20Ch) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to Summary Table

Table 3-2245. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 820Ch

Figure 3-1168. CONTROLSS_OUTPUTXBAR4_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR4_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR4_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G3_SEL							
R/W							
0h							

Table 3-2246. CONTROLSS_OUTPUTXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR4_G3_SEL	R/W	0h	G3: OUTPUT XBAR4 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.58 CONTROLSS_OUTPUTXBAR4_G4 Register

3.17.2.58.1 CONTROLSS_OUTPUTXBAR4_G4 Register (Offset = 210h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to Summary Table

Table 3-2247. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8210h

Figure 3-1169. CONTROLSS_OUTPUTXBAR4_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR4_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR4_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G4_SEL							
R/W							
0h							

Table 3-2248. CONTROLSS_OUTPUTXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR4_G4_SEL	R/W	0h	G4: OUTPUT XBAR4 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.59 CONTROLSS_OUTPUTXBAR4_G5 Register

3.17.2.59.1 CONTROLSS_OUTPUTXBAR4_G5 Register (Offset = 214h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to Summary Table

Table 3-2249. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8214h

Figure 3-1170. CONTROLSS_OUTPUTXBAR4_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR4_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G5_SEL							
R/W							
0h							

Table 3-2250. CONTROLSS_OUTPUTXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR4_G5_SEL	R/W	0h	G5: OUTPUT XBAR4 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.60 CONTROLSS_OUTPUTXBAR4_G6 Register

3.17.2.60.1 CONTROLSS_OUTPUTXBAR4_G6 Register (Offset = 218h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to Summary Table

Table 3-2251. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8218h

Figure 3-1171. CONTROLSS_OUTPUTXBAR4_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR4_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G6_SEL							
R/W							
0h							

Table 3-2252. CONTROLSS_OUTPUTXBAR4_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR4_G6_SEL	R/W	0h	G6: OUTPUT XBAR4 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.61 CONTROLSS_OUTPUTXBAR4_G7 Register

3.17.2.61.1 CONTROLSS_OUTPUTXBAR4_G7 Register (Offset = 21Ch) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to Summary Table

Table 3-2253. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 821Ch

Figure 3-1172. CONTROLSS_OUTPUTXBAR4_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR4_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G7_SEL							
R/W							
0h							

Table 3-2254. CONTROLSS_OUTPUTXBAR4_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR4_G7_SEL	R/W	0h	G7: OUTPUT XBAR4 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.62 CONTROLSS_OUTPUTXBAR4_G8 Register

3.17.2.62.1 CONTROLSS_OUTPUTXBAR4_G8 Register (Offset = 220h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to Summary Table

Table 3-2255. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8220h

Figure 3-1173. CONTROLSS_OUTPUTXBAR4_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR4_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR4_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G8_SEL							
R/W							
0h							

Table 3-2256. CONTROLSS_OUTPUTXBAR4_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2256. CONTROLSS_OUTPUTXBAR4_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR4_G8_SEL	R/W	0h	G8: OUTPUT XBAR4 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.63 CONTROLSS_OUTPUTXBAR4_G9 Register

3.17.2.63.1 CONTROLSS_OUTPUTXBAR4_G9 Register (Offset = 224h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

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Table 3-2257. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8224h

Figure 3-1174. CONTROLSS_OUTPUTXBAR4_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR4_G9_SEL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
OUTPUTXBAR4_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G9_SEL							
R/W							
0h							

Table 3-2258. CONTROLSS_OUTPUTXBAR4_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2258. CONTROLSS_OUTPUTXBAR4_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR4_G9_SEL	R/W	0h	G9: OUTPUT XBAR4 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.64 CONTROLSS_OUTPUTXBAR4_G10 Register

3.17.2.64.1 CONTROLSS_OUTPUTXBAR4_G10 Register (Offset = 228h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to Summary Table

Table 3-2259. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8228h

Figure 3-1175. CONTROLSS_OUTPUTXBAR4_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		OUTPUTXBAR4_G10_SEL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
OUTPUTXBAR4_G10_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR4_G10_SEL							
R/W							
0h							

Table 3-2260. CONTROLSS_OUTPUTXBAR4_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR4_G10_SEL	R/W	0h	G10: OUTPUT XBAR4 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.65 CONTROLSS_OUTPUTXBAR5_G0 Register

3.17.2.65.1 CONTROLSS_OUTPUTXBAR5_G0 Register (Offset = 240h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

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Table 3-2261. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8240h

Figure 3-1176. CONTROLSS_OUTPUTXBAR5_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR5_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR5_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR5_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR5_G0_SEL							
R/W							
0h							

Table 3-2262. CONTROLSS_OUTPUTXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR5_G0_SEL	R/W	0h	G0: PWM XBAR5 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.66 CONTROLSS_OUTPUTXBAR5_G1 Register

3.17.2.66.1 CONTROLSS_OUTPUTXBAR5_G1 Register (Offset = 244h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

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Table 3-2263. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8244h

Figure 3-1177. CONTROLSS_OUTPUTXBAR5_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR5_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR5_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR5_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR5_G1_SEL							
R/W							
0h							

Table 3-2264. CONTROLSS_OUTPUTXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR5_G1_SEL	R/W	0h	G1: OUTPUT XBAR5 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.67 CONTROLSS_OUTPUTXBAR5_G2 Register

3.17.2.67.1 CONTROLSS_OUTPUTXBAR5_G2 Register (Offset = 248h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to Summary Table

Table 3-2265. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8248h

Figure 3-1178. CONTROLSS_OUTPUTXBAR5_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR5_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR5_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR5_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR5_G2_SEL							
R/W							
0h							

Table 3-2266. CONTROLSS_OUTPUTXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR5_G2_SEL	R/W	0h	G2: OUTPUT XBAR5 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.68 CONTROLSS_OUTPUTXBAR5_G3 Register

3.17.2.68.1 CONTROLSS_OUTPUTXBAR5_G3 Register (Offset = 24Ch) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to Summary Table

Table 3-2267. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 824Ch

Figure 3-1179. CONTROLSS_OUTPUTXBAR5_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR5_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR5_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR5_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR5_G3_SEL							
R/W							
0h							

Table 3-2268. CONTROLSS_OUTPUTXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR5_G3_SEL	R/W	0h	G3: OUTPUT XBAR5 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.69 CONTROLSS_OUTPUTXBAR5_G4 Register

3.17.2.69.1 CONTROLSS_OUTPUTXBAR5_G4 Register (Offset = 250h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to Summary Table

Table 3-2269. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8250h

Figure 3-1180. CONTROLSS_OUTPUTXBAR5_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR5_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR5_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR5_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR5_G4_SEL							
R/W							
0h							

Table 3-2270. CONTROLSS_OUTPUTXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR5_G4_SEL	R/W	0h	G4: OUTPUT XBAR5 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.70 CONTROLSS_OUTPUTXBAR5_G5 Register

3.17.2.70.1 CONTROLSS_OUTPUTXBAR5_G5 Register (Offset = 254h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to Summary Table

Table 3-2271. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8254h

Figure 3-1181. CONTROLSS_OUTPUTXBAR5_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR5_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR5_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR5_G5_SEL							
R/W							
0h							

Table 3-2272. CONTROLSS_OUTPUTXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR5_G5_SEL	R/W	0h	G5: OUTPUT XBAR5 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.71 CONTROLSS_OUTPUTXBAR5_G6 Register

3.17.2.71.1 CONTROLSS_OUTPUTXBAR5_G6 Register (Offset = 258h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to Summary Table

Table 3-2273. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8258h

Figure 3-1182. CONTROLSS_OUTPUTXBAR5_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR5_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR5_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR5_G6_SEL							
R/W							
0h							

Table 3-2274. CONTROLSS_OUTPUTXBAR5_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR5_G6_SEL	R/W	0h	G6: OUTPUT XBAR5 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.72 CONTROLSS_OUTPUTXBAR5_G7 Register

3.17.2.72.1 CONTROLSS_OUTPUTXBAR5_G7 Register (Offset = 25Ch) [reset = 0h]

OUTPUT XBAR 5 Input Select.

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Table 3-2275. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 825Ch

Figure 3-1183. CONTROLSS_OUTPUTXBAR5_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR5_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR5_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR5_G7_SEL							
R/W							
0h							

Table 3-2276. CONTROLSS_OUTPUTXBAR5_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR5_G7_SEL	R/W	0h	G7: OUTPUT XBAR5 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.73 CONTROLSS_OUTPUTXBAR5_G8 Register

3.17.2.73.1 CONTROLSS_OUTPUTXBAR5_G8 Register (Offset = 260h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to Summary Table

Table 3-2277. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8260h

Figure 3-1184. CONTROLSS_OUTPUTXBAR5_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR5_G8_SEL			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR5_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR5_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR5_G8_SEL							
R/W							
0h							

Table 3-2278. CONTROLSS_OUTPUTXBAR5_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2278. CONTROLSS_OUTPUTXBAR5_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR5_G8_SEL	R/W	0h	G8: OUTPUT XBAR5 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.74 CONTROLSS_OUTPUTXBAR5_G9 Register

3.17.2.74.1 CONTROLSS_OUTPUTXBAR5_G9 Register (Offset = 264h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

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Table 3-2279. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8264h

Figure 3-1185. CONTROLSS_OUTPUTXBAR5_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR5_G9_SEL	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR5_G9_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR5_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR5_G9_SEL							
R/W							
0h							

Table 3-2280. CONTROLSS_OUTPUTXBAR5_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2280. CONTROLSS_OUTPUTXBAR5_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR5_G9_SEL	R/W	0h	G9: OUTPUT XBAR5 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.75 CONTROLSS_OUTPUTXBAR5_G10 Register

3.17.2.75.1 CONTROLSS_OUTPUTXBAR5_G10 Register (Offset = 268h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to Summary Table

Table 3-2281. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8268h

Figure 3-1186. CONTROLSS_OUTPUTXBAR5_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		OUTPUTXBAR5_G10_SEL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
OUTPUTXBAR5_G10_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR5_G10_SEL							
R/W							
0h							

Table 3-2282. CONTROLSS_OUTPUTXBAR5_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR5_G10_SEL	R/W	0h	G10: OUTPUT XBAR5 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.76 CONTROLSS_OUTPUTXBAR6_G0 Register

3.17.2.76.1 CONTROLSS_OUTPUTXBAR6_G0 Register (Offset = 280h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to Summary Table

Table 3-2283. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8280h

Figure 3-1187. CONTROLSS_OUTPUTXBAR6_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR6_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR6_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR6_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR6_G0_SEL							
R/W							
0h							

Table 3-2284. CONTROLSS_OUTPUTXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR6_G0_SEL	R/W	0h	G0: PWM XBAR6 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.77 CONTROLSS_OUTPUTXBAR6_G1 Register

3.17.2.77.1 CONTROLSS_OUTPUTXBAR6_G1 Register (Offset = 284h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to Summary Table

Table 3-2285. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8284h

Figure 3-1188. CONTROLSS_OUTPUTXBAR6_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR6_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR6_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR6_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR6_G1_SEL							
R/W							
0h							

Table 3-2286. CONTROLSS_OUTPUTXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR6_G1_SEL	R/W	0h	G1: OUTPUT XBAR6 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.78 CONTROLSS_OUTPUTXBAR6_G2 Register

3.17.2.78.1 CONTROLSS_OUTPUTXBAR6_G2 Register (Offset = 288h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to Summary Table

Table 3-2287. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8288h

Figure 3-1189. CONTROLSS_OUTPUTXBAR6_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR6_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR6_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR6_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR6_G2_SEL							
R/W							
0h							

Table 3-2288. CONTROLSS_OUTPUTXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR6_G2_SEL	R/W	0h	G2: OUTPUT XBAR6 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.79 CONTROLSS_OUTPUTXBAR6_G3 Register

3.17.2.79.1 CONTROLSS_OUTPUTXBAR6_G3 Register (Offset = 28Ch) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to Summary Table

Table 3-2289. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 828Ch

Figure 3-1190. CONTROLSS_OUTPUTXBAR6_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR6_G3_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR6_G3_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR6_G3_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR6_G3_SEL							
R/W							
0h							

Table 3-2290. CONTROLSS_OUTPUTXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR6_G3_SEL	R/W	0h	G3: OUTPUT XBAR6 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.80 CONTROLSS_OUTPUTXBAR6_G4 Register

3.17.2.80.1 CONTROLSS_OUTPUTXBAR6_G4 Register (Offset = 290h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to Summary Table

Table 3-2291. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8290h

Figure 3-1191. CONTROLSS_OUTPUTXBAR6_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR6_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR6_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR6_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR6_G4_SEL							
R/W							
0h							

Table 3-2292. CONTROLSS_OUTPUTXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR6_G4_SEL	R/W	0h	G4: OUTPUT XBAR6 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.81 CONTROLSS_OUTPUTXBAR6_G5 Register

3.17.2.81.1 CONTROLSS_OUTPUTXBAR6_G5 Register (Offset = 294h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

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Table 3-2293. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8294h

Figure 3-1192. CONTROLSS_OUTPUTXBAR6_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR6_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR6_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR6_G5_SEL							
R/W							
0h							

Table 3-2294. CONTROLSS_OUTPUTXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR6_G5_SEL	R/W	0h	G5: OUTPUT XBAR6 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.82 CONTROLSS_OUTPUTXBAR6_G6 Register

3.17.2.82.1 CONTROLSS_OUTPUTXBAR6_G6 Register (Offset = 298h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to Summary Table

Table 3-2295. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8298h

Figure 3-1193. CONTROLSS_OUTPUTXBAR6_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR6_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR6_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR6_G6_SEL							
R/W							
0h							

Table 3-2296. CONTROLSS_OUTPUTXBAR6_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR6_G6_SEL	R/W	0h	G6: OUTPUT XBAR6 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.83 CONTROLSS_OUTPUTXBAR6_G7 Register

3.17.2.83.1 CONTROLSS_OUTPUTXBAR6_G7 Register (Offset = 29Ch) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to Summary Table

Table 3-2297. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 829Ch

Figure 3-1194. CONTROLSS_OUTPUTXBAR6_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OUTPUTXBAR6_G7_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR6_G7_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR6_G7_SEL							
R/W							
0h							

Table 3-2298. CONTROLSS_OUTPUTXBAR6_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR6_G7_SEL	R/W	0h	G7: OUTPUT XBAR6 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.84 CONTROLSS_OUTPUTXBAR6_G8 Register

3.17.2.84.1 CONTROLSS_OUTPUTXBAR6_G8 Register (Offset = 2A0h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

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Table 3-2299. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82A0h

Figure 3-1195. CONTROLSS_OUTPUTXBAR6_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR6_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR6_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR6_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR6_G8_SEL							
R/W							
0h							

Table 3-2300. CONTROLSS_OUTPUTXBAR6_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2300. CONTROLSS_OUTPUTXBAR6_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR6_G8_SEL	R/W	0h	G8: OUTPUT XBAR6 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.85 CONTROLSS_OUTPUTXBAR6_G9 Register

3.17.2.85.1 CONTROLSS_OUTPUTXBAR6_G9 Register (Offset = 2A4h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to Summary Table

Table 3-2301. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82A4h

Figure 3-1196. CONTROLSS_OUTPUTXBAR6_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR6_G9_SEL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
OUTPUTXBAR6_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR6_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR6_G9_SEL							
R/W							
0h							

Table 3-2302. CONTROLSS_OUTPUTXBAR6_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2302. CONTROLSS_OUTPUTXBAR6_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR6_G9_SEL	R/W	0h	G9: OUTPUT XBAR6 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.86 CONTROLSS_OUTPUTXBAR6_G10 Register

3.17.2.86.1 CONTROLSS_OUTPUTXBAR6_G10 Register (Offset = 2A8h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to Summary Table

Table 3-2303. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82A8h

Figure 3-1197. CONTROLSS_OUTPUTXBAR6_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		OUTPUTXBAR6_G10_SEL					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR6_G10_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR6_G10_SEL							
R/W							
0h							

Table 3-2304. CONTROLSS_OUTPUTXBAR6_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR6_G10_SEL	R/W	0h	G10: OUTPUT XBAR6 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.87 CONTROLSS_OUTPUTXBAR7_G0 Register

3.17.2.87.1 CONTROLSS_OUTPUTXBAR7_G0 Register (Offset = 2C0h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2305. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82C0h

Figure 3-1198. CONTROLSS_OUTPUTXBAR7_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR7_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR7_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR7_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR7_G0_SEL							
R/W							
0h							

Table 3-2306. CONTROLSS_OUTPUTXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR7_G0_SEL	R/W	0h	G0: PWM XBAR7 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.88 CONTROLSS_OUTPUTXBAR7_G1 Register

3.17.2.88.1 CONTROLSS_OUTPUTXBAR7_G1 Register (Offset = 2C4h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2307. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82C4h

Figure 3-1199. CONTROLSS_OUTPUTXBAR7_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR7_G1_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR7_G1_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR7_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR7_G1_SEL							
R/W							
0h							

Table 3-2308. CONTROLSS_OUTPUTXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR7_G1_SEL	R/W	0h	G1: OUTPUT XBAR7 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.89 CONTROLSS_OUTPUTXBAR7_G2 Register

3.17.2.89.1 CONTROLSS_OUTPUTXBAR7_G2 Register (Offset = 2C8h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2309. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82C8h

Figure 3-1200. CONTROLSS_OUTPUTXBAR7_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR7_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR7_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR7_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR7_G2_SEL							
R/W							
0h							

Table 3-2310. CONTROLSS_OUTPUTXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR7_G2_SEL	R/W	0h	G2: OUTPUT XBAR7 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.90 CONTROLSS_OUTPUTXBAR7_G3 Register

3.17.2.90.1 CONTROLSS_OUTPUTXBAR7_G3 Register (Offset = 2CCh) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2311. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82CCh

Figure 3-1201. CONTROLSS_OUTPUTXBAR7_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR7_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR7_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR7_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR7_G3_SEL							
R/W							
0h							

Table 3-2312. CONTROLSS_OUTPUTXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR7_G3_SEL	R/W	0h	G3: OUTPUT XBAR7 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.91 CONTROLSS_OUTPUTXBAR7_G4 Register

3.17.2.91.1 CONTROLSS_OUTPUTXBAR7_G4 Register (Offset = 2D0h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2313. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82D0h

Figure 3-1202. CONTROLSS_OUTPUTXBAR7_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR7_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR7_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR7_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR7_G4_SEL							
R/W							
0h							

Table 3-2314. CONTROLSS_OUTPUTXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR7_G4_SEL	R/W	0h	G4: OUTPUT XBAR7 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.92 CONTROLSS_OUTPUTXBAR7_G5 Register

3.17.2.92.1 CONTROLSS_OUTPUTXBAR7_G5 Register (Offset = 2D4h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2315. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82D4h

Figure 3-1203. CONTROLSS_OUTPUTXBAR7_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR7_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR7_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR7_G5_SEL							
R/W							
0h							

Table 3-2316. CONTROLSS_OUTPUTXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR7_G5_SEL	R/W	0h	G5: OUTPUT XBAR7 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.93 CONTROLSS_OUTPUTXBAR7_G6 Register

3.17.2.93.1 CONTROLSS_OUTPUTXBAR7_G6 Register (Offset = 2D8h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2317. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82D8h

Figure 3-1204. CONTROLSS_OUTPUTXBAR7_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR7_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR7_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR7_G6_SEL							
R/W							
0h							

Table 3-2318. CONTROLSS_OUTPUTXBAR7_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR7_G6_SEL	R/W	0h	G6: OUTPUT XBAR7 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.94 CONTROLSS_OUTPUTXBAR7_G7 Register

3.17.2.94.1 CONTROLSS_OUTPUTXBAR7_G7 Register (Offset = 2DCh) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2319. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82DCh

Figure 3-1205. CONTROLSS_OUTPUTXBAR7_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OUTPUTXBAR7_G7_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR7_G7_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR7_G7_SEL							
R/W							
0h							

Table 3-2320. CONTROLSS_OUTPUTXBAR7_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR7_G7_SEL	R/W	0h	G7: OUTPUT XBAR7 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.95 CONTROLSS_OUTPUTXBAR7_G8 Register

3.17.2.95.1 CONTROLSS_OUTPUTXBAR7_G8 Register (Offset = 2E0h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2321. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82E0h

Figure 3-1206. CONTROLSS_OUTPUTXBAR7_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR7_G8_SEL			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR7_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR7_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR7_G8_SEL							
R/W							
0h							

Table 3-2322. CONTROLSS_OUTPUTXBAR7_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2322. CONTROLSS_OUTPUTXBAR7_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR7_G8_SEL	R/W	0h	G8: OUTPUT XBAR7 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.96 CONTROLSS_OUTPUTXBAR7_G9 Register

3.17.2.96.1 CONTROLSS_OUTPUTXBAR7_G9 Register (Offset = 2E4h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2323. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82E4h

Figure 3-1207. CONTROLSS_OUTPUTXBAR7_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR7_G9_SEL	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR7_G9_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR7_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR7_G9_SEL							
R/W							
0h							

Table 3-2324. CONTROLSS_OUTPUTXBAR7_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2324. CONTROLSS_OUTPUTXBAR7_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR7_G9_SEL	R/W	0h	G9: OUTPUT XBAR7 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.97 CONTROLSS_OUTPUTXBAR7_G10 Register

3.17.2.97.1 CONTROLSS_OUTPUTXBAR7_G10 Register (Offset = 2E8h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to Summary Table

Table 3-2325. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 82E8h

Figure 3-1208. CONTROLSS_OUTPUTXBAR7_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		OUTPUTXBAR7_G10_SEL					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR7_G10_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR7_G10_SEL							
R/W							
0h							

Table 3-2326. CONTROLSS_OUTPUTXBAR7_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR7_G10_SEL	R/W	0h	G10: OUTPUT XBAR7 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.98 CONTROLSS_OUTPUTXBAR8_G0 Register

3.17.2.98.1 CONTROLSS_OUTPUTXBAR8_G0 Register (Offset = 300h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to Summary Table

Table 3-2327. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8300h

Figure 3-1209. CONTROLSS_OUTPUTXBAR8_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR8_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR8_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR8_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR8_G0_SEL							
R/W							
0h							

Table 3-2328. CONTROLSS_OUTPUTXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR8_G0_SEL	R/W	0h	G0: PWM XBAR8 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.99 CONTROLSS_OUTPUTXBAR8_G1 Register

3.17.2.99.1 CONTROLSS_OUTPUTXBAR8_G1 Register (Offset = 304h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to Summary Table

Table 3-2329. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8304h

Figure 3-1210. CONTROLSS_OUTPUTXBAR8_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR8_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR8_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR8_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR8_G1_SEL							
R/W							
0h							

Table 3-2330. CONTROLSS_OUTPUTXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR8_G1_SEL	R/W	0h	G1: OUTPUT XBAR8 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.100 CONTROLSS_OUTPUTXBAR8_G2 Register

3.17.2.100.1 CONTROLSS_OUTPUTXBAR8_G2 Register (Offset = 308h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to Summary Table

Table 3-2331. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8308h

Figure 3-1211. CONTROLSS_OUTPUTXBAR8_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR8_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR8_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR8_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR8_G2_SEL							
R/W							
0h							

Table 3-2332. CONTROLSS_OUTPUTXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR8_G2_SEL	R/W	0h	G2: OUTPUT XBAR8 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.101 CONTROLSS_OUTPUTXBAR8_G3 Register

3.17.2.101.1 CONTROLSS_OUTPUTXBAR8_G3 Register (Offset = 30Ch) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to Summary Table

Table 3-2333. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 830Ch

Figure 3-1212. CONTROLSS_OUTPUTXBAR8_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR8_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR8_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR8_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR8_G3_SEL							
R/W							
0h							

Table 3-2334. CONTROLSS_OUTPUTXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR8_G3_SEL	R/W	0h	G3: OUTPUT XBAR8 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.102 CONTROLSS_OUTPUTXBAR8_G4 Register

3.17.2.102.1 CONTROLSS_OUTPUTXBAR8_G4 Register (Offset = 310h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to Summary Table

Table 3-2335. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8310h

Figure 3-1213. CONTROLSS_OUTPUTXBAR8_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR8_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR8_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR8_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR8_G4_SEL							
R/W							
0h							

Table 3-2336. CONTROLSS_OUTPUTXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR8_G4_SEL	R/W	0h	G4: OUTPUT XBAR8 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.103 CONTROLSS_OUTPUTXBAR8_G5 Register

3.17.2.103.1 CONTROLSS_OUTPUTXBAR8_G5 Register (Offset = 314h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to Summary Table

Table 3-2337. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8314h

Figure 3-1214. CONTROLSS_OUTPUTXBAR8_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR8_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR8_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR8_G5_SEL							
R/W							
0h							

Table 3-2338. CONTROLSS_OUTPUTXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR8_G5_SEL	R/W	0h	G5: OUTPUT XBAR8 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.104 CONTROLSS_OUTPUTXBAR8_G6 Register

3.17.2.104.1 CONTROLSS_OUTPUTXBAR8_G6 Register (Offset = 318h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to Summary Table

Table 3-2339. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8318h

Figure 3-1215. CONTROLSS_OUTPUTXBAR8_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR8_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR8_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR8_G6_SEL							
R/W							
0h							

Table 3-2340. CONTROLSS_OUTPUTXBAR8_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR8_G6_SEL	R/W	0h	G6: OUTPUT XBAR8 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.105 CONTROLSS_OUTPUTXBAR8_G7 Register

3.17.2.105.1 CONTROLSS_OUTPUTXBAR8_G7 Register (Offset = 31Ch) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to Summary Table

Table 3-2341. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 831Ch

Figure 3-1216. CONTROLSS_OUTPUTXBAR8_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR8_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR8_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR8_G7_SEL							
R/W							
0h							

Table 3-2342. CONTROLSS_OUTPUTXBAR8_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR8_G7_SEL	R/W	0h	G7: OUTPUT XBAR8 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.106 CONTROLSS_OUTPUTXBAR8_G8 Register

3.17.2.106.1 CONTROLSS_OUTPUTXBAR8_G8 Register (Offset = 320h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to Summary Table

Table 3-2343. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8320h

Figure 3-1217. CONTROLSS_OUTPUTXBAR8_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR8_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR8_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR8_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR8_G8_SEL							
R/W							
0h							

Table 3-2344. CONTROLSS_OUTPUTXBAR8_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2344. CONTROLSS_OUTPUTXBAR8_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR8_G8_SEL	R/W	0h	G8: OUTPUT XBAR8 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.107 CONTROLSS_OUTPUTXBAR8_G9 Register

3.17.2.107.1 CONTROLSS_OUTPUTXBAR8_G9 Register (Offset = 324h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to Summary Table

Table 3-2345. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8324h

Figure 3-1218. CONTROLSS_OUTPUTXBAR8_G9 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">OUTPUTXBAR8_G9_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">OUTPUTXBAR8_G9_SEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">OUTPUTXBAR8_G9_SEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUTPUTXBAR8_G9_SEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 3-2346. CONTROLSS_OUTPUTXBAR8_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2346. CONTROLSS_OUTPUTXBAR8_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR8_G9_SEL	R/W	0h	G9: OUTPUT XBAR8 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.108 CONTROLSS_OUTPUTXBAR8_G10 Register

3.17.2.108.1 CONTROLSS_OUTPUTXBAR8_G10 Register (Offset = 328h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

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Table 3-2347. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8328h

Figure 3-1219. CONTROLSS_OUTPUTXBAR8_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		OUTPUTXBAR8_G10_SEL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
OUTPUTXBAR8_G10_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR8_G10_SEL							
R/W							
0h							

Table 3-2348. CONTROLSS_OUTPUTXBAR8_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR8_G10_SEL	R/W	0h	G10: OUTPUT XBAR8 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.109 CONTROLSS_OUTPUTXBAR9_G0 Register

3.17.2.109.1 CONTROLSS_OUTPUTXBAR9_G0 Register (Offset = 340h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to Summary Table

Table 3-2349. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8340h

Figure 3-1220. CONTROLSS_OUTPUTXBAR9_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR9_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR9_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR9_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR9_G0_SEL							
R/W							
0h							

Table 3-2350. CONTROLSS_OUTPUTXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR9_G0_SEL	R/W	0h	G0: PWM XBAR9 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.110 CONTROLSS_OUTPUTXBAR9_G1 Register

3.17.2.110.1 CONTROLSS_OUTPUTXBAR9_G1 Register (Offset = 344h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to Summary Table

Table 3-2351. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8344h

Figure 3-1221. CONTROLSS_OUTPUTXBAR9_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR9_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR9_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR9_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR9_G1_SEL							
R/W							
0h							

Table 3-2352. CONTROLSS_OUTPUTXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR9_G1_SEL	R/W	0h	G1: OUTPUT XBAR9 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.111 CONTROLSS_OUTPUTXBAR9_G2 Register

3.17.2.111.1 CONTROLSS_OUTPUTXBAR9_G2 Register (Offset = 348h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to Summary Table

Table 3-2353. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8348h

Figure 3-1222. CONTROLSS_OUTPUTXBAR9_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR9_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR9_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR9_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR9_G2_SEL							
R/W							
0h							

Table 3-2354. CONTROLSS_OUTPUTXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR9_G2_SEL	R/W	0h	G2: OUTPUT XBAR9 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.112 CONTROLSS_OUTPUTXBAR9_G3 Register

3.17.2.112.1 CONTROLSS_OUTPUTXBAR9_G3 Register (Offset = 34Ch) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to Summary Table

Table 3-2355. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 834Ch

Figure 3-1223. CONTROLSS_OUTPUTXBAR9_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR9_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR9_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR9_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR9_G3_SEL							
R/W							
0h							

Table 3-2356. CONTROLSS_OUTPUTXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR9_G3_SEL	R/W	0h	G3: OUTPUT XBAR9 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.113 CONTROLSS_OUTPUTXBAR9_G4 Register

3.17.2.113.1 CONTROLSS_OUTPUTXBAR9_G4 Register (Offset = 350h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to Summary Table

Table 3-2357. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8350h

Figure 3-1224. CONTROLSS_OUTPUTXBAR9_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR9_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR9_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR9_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR9_G4_SEL							
R/W							
0h							

Table 3-2358. CONTROLSS_OUTPUTXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR9_G4_SEL	R/W	0h	G4: OUTPUT XBAR9 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.114 CONTROLSS_OUTPUTXBAR9_G5 Register

3.17.2.114.1 CONTROLSS_OUTPUTXBAR9_G5 Register (Offset = 354h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to Summary Table

Table 3-2359. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8354h

Figure 3-1225. CONTROLSS_OUTPUTXBAR9_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR9_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR9_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR9_G5_SEL							
R/W							
0h							

Table 3-2360. CONTROLSS_OUTPUTXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR9_G5_SEL	R/W	0h	G5: OUTPUT XBAR9 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.115 CONTROLSS_OUTPUTXBAR9_G6 Register

3.17.2.115.1 CONTROLSS_OUTPUTXBAR9_G6 Register (Offset = 358h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

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Table 3-2361. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8358h

Figure 3-1226. CONTROLSS_OUTPUTXBAR9_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OUTPUTXBAR9_G6_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR9_G6_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR9_G6_SEL							
R/W							
0h							

Table 3-2362. CONTROLSS_OUTPUTXBAR9_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR9_G6_SEL	R/W	0h	G6: OUTPUT XBAR9 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.116 CONTROLSS_OUTPUTXBAR9_G7 Register

3.17.2.116.1 CONTROLSS_OUTPUTXBAR9_G7 Register (Offset = 35Ch) [reset = 0h]

OUTPUT XBAR 9 Input Select.

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Table 3-2363. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 835Ch

Figure 3-1227. CONTROLSS_OUTPUTXBAR9_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR9_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR9_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR9_G7_SEL							
R/W							
0h							

Table 3-2364. CONTROLSS_OUTPUTXBAR9_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR9_G7_SEL	R/W	0h	G7: OUTPUT XBAR9 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.117 CONTROLSS_OUTPUTXBAR9_G8 Register

3.17.2.117.1 CONTROLSS_OUTPUTXBAR9_G8 Register (Offset = 360h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

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Table 3-2365. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8360h

Figure 3-1228. CONTROLSS_OUTPUTXBAR9_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR9_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR9_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR9_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR9_G8_SEL							
R/W							
0h							

Table 3-2366. CONTROLSS_OUTPUTXBAR9_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2366. CONTROLSS_OUTPUTXBAR9_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR9_G8_SEL	R/W	0h	G8: OUTPUT XBAR9 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.118 CONTROLSS_OUTPUTXBAR9_G9 Register

3.17.2.118.1 CONTROLSS_OUTPUTXBAR9_G9 Register (Offset = 364h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

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Table 3-2367. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8364h

Figure 3-1229. CONTROLSS_OUTPUTXBAR9_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR9_G9_SEL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
OUTPUTXBAR9_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR9_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR9_G9_SEL							
R/W							
0h							

Table 3-2368. CONTROLSS_OUTPUTXBAR9_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2368. CONTROLSS_OUTPUTXBAR9_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR9_G9_SEL	R/W	0h	G9: OUTPUT XBAR9 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.119 CONTROLSS_OUTPUTXBAR9_G10 Register

3.17.2.119.1 CONTROLSS_OUTPUTXBAR9_G10 Register (Offset = 368h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

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Table 3-2369. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8368h

Figure 3-1230. CONTROLSS_OUTPUTXBAR9_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		OUTPUTXBAR9_G10_SEL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
OUTPUTXBAR9_G10_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR9_G10_SEL							
R/W							
0h							

Table 3-2370. CONTROLSS_OUTPUTXBAR9_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR9_G10_SEL	R/W	0h	G10: OUTPUT XBAR9 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.120 CONTROLSS_OUTPUTXBAR10_G0 Register

3.17.2.120.1 CONTROLSS_OUTPUTXBAR10_G0 Register (Offset = 380h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

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Table 3-2371. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8380h

Figure 3-1231. CONTROLSS_OUTPUTXBAR10_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR10_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR10_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G0_SEL							
R/W							
0h							

Table 3-2372. CONTROLSS_OUTPUTXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR10_G0_SEL	R/W	0h	G0: PWM XBAR10 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.121 CONTROLSS_OUTPUTXBAR10_G1 Register

3.17.2.121.1 CONTROLSS_OUTPUTXBAR10_G1 Register (Offset = 384h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to Summary Table

Table 3-2373. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8384h

Figure 3-1232. CONTROLSS_OUTPUTXBAR10_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR10_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR10_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G1_SEL							
R/W							
0h							

Table 3-2374. CONTROLSS_OUTPUTXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR10_G1_SEL	R/W	0h	G1: OUTPUT XBAR10 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.122 CONTROLSS_OUTPUTXBAR10_G2 Register

3.17.2.122.1 CONTROLSS_OUTPUTXBAR10_G2 Register (Offset = 388h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

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Table 3-2375. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8388h

Figure 3-1233. CONTROLSS_OUTPUTXBAR10_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR10_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR10_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G2_SEL							
R/W							
0h							

Table 3-2376. CONTROLSS_OUTPUTXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR10_G2_SEL	R/W	0h	G2: OUTPUT XBAR10 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.123 CONTROLSS_OUTPUTXBAR10_G3 Register

3.17.2.123.1 CONTROLSS_OUTPUTXBAR10_G3 Register (Offset = 38Ch) [reset = 0h]

OUTPUT XBAR 10 Input Select.

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Table 3-2377. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 838Ch

Figure 3-1234. CONTROLSS_OUTPUTXBAR10_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR10_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR10_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G3_SEL							
R/W							
0h							

Table 3-2378. CONTROLSS_OUTPUTXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR10_G3_SEL	R/W	0h	G3: OUTPUT XBAR10 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.124 CONTROLSS_OUTPUTXBAR10_G4 Register

3.17.2.124.1 CONTROLSS_OUTPUTXBAR10_G4 Register (Offset = 390h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

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Table 3-2379. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8390h

Figure 3-1235. CONTROLSS_OUTPUTXBAR10_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR10_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR10_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G4_SEL							
R/W							
0h							

Table 3-2380. CONTROLSS_OUTPUTXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR10_G4_SEL	R/W	0h	G4: OUTPUT XBAR10 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.125 CONTROLSS_OUTPUTXBAR10_G5 Register

3.17.2.125.1 CONTROLSS_OUTPUTXBAR10_G5 Register (Offset = 394h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

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Table 3-2381. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8394h

Figure 3-1236. CONTROLSS_OUTPUTXBAR10_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR10_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G5_SEL							
R/W							
0h							

Table 3-2382. CONTROLSS_OUTPUTXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR10_G5_SEL	R/W	0h	G5: OUTPUT XBAR10 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.126 CONTROLSS_OUTPUTXBAR10_G6 Register

3.17.2.126.1 CONTROLSS_OUTPUTXBAR10_G6 Register (Offset = 398h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to Summary Table

Table 3-2383. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8398h

Figure 3-1237. CONTROLSS_OUTPUTXBAR10_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR10_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G6_SEL							
R/W							
0h							

Table 3-2384. CONTROLSS_OUTPUTXBAR10_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR10_G6_SEL	R/W	0h	G6: OUTPUT XBAR10 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.127 CONTROLSS_OUTPUTXBAR10_G7 Register

3.17.2.127.1 CONTROLSS_OUTPUTXBAR10_G7 Register (Offset = 39Ch) [reset = 0h]

OUTPUT XBAR 10 Input Select.

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Table 3-2385. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 839Ch

Figure 3-1238. CONTROLSS_OUTPUTXBAR10_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR10_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G7_SEL							
R/W							
0h							

Table 3-2386. CONTROLSS_OUTPUTXBAR10_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR10_G7_SEL	R/W	0h	G7: OUTPUT XBAR10 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.128 CONTROLSS_OUTPUTXBAR10_G8 Register

3.17.2.128.1 CONTROLSS_OUTPUTXBAR10_G8 Register (Offset = 3A0h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

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Table 3-2387. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83A0h

Figure 3-1239. CONTROLSS_OUTPUTXBAR10_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR10_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR10_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G8_SEL							
R/W							
0h							

Table 3-2388. CONTROLSS_OUTPUTXBAR10_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2388. CONTROLSS_OUTPUTXBAR10_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR10_G8_SEL	R/W	0h	G8: OUTPUT XBAR10 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.129 CONTROLSS_OUTPUTXBAR10_G9 Register

3.17.2.129.1 CONTROLSS_OUTPUTXBAR10_G9 Register (Offset = 3A4h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

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Table 3-2389. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83A4h

Figure 3-1240. CONTROLSS_OUTPUTXBAR10_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR10_G9_SEL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
OUTPUTXBAR10_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G9_SEL							
R/W							
0h							

Table 3-2390. CONTROLSS_OUTPUTXBAR10_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2390. CONTROLSS_OUTPUTXBAR10_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR10_G9_SEL	R/W	0h	G9: OUTPUT XBAR10 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.130 CONTROLSS_OUTPUTXBAR10_G10 Register

3.17.2.130.1 CONTROLSS_OUTPUTXBAR10_G10 Register (Offset = 3A8h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

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Table 3-2391. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83A8h

Figure 3-1241. CONTROLSS_OUTPUTXBAR10_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		OUTPUTXBAR10_G10_SEL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
OUTPUTXBAR10_G10_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR10_G10_SEL							
R/W							
0h							

Table 3-2392. CONTROLSS_OUTPUTXBAR10_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR10_G10_SEL	R/W	0h	G10: OUTPUT XBAR10 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.131 CONTROLSS_OUTPUTXBAR11_G0 Register

3.17.2.131.1 CONTROLSS_OUTPUTXBAR11_G0 Register (Offset = 3C0h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

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Table 3-2393. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83C0h

Figure 3-1242. CONTROLSS_OUTPUTXBAR11_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR11_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR11_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR11_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR11_G0_SEL							
R/W							
0h							

Table 3-2394. CONTROLSS_OUTPUTXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR11_G0_SEL	R/W	0h	G0: PWM XBAR11 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.132 CONTROLSS_OUTPUTXBAR11_G1 Register

3.17.2.132.1 CONTROLSS_OUTPUTXBAR11_G1 Register (Offset = 3C4h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

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Table 3-2395. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83C4h

Figure 3-1243. CONTROLSS_OUTPUTXBAR11_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR11_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR11_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR11_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR11_G1_SEL							
R/W							
0h							

Table 3-2396. CONTROLSS_OUTPUTXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR11_G1_SEL	R/W	0h	G1: OUTPUT XBAR11 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.133 CONTROLSS_OUTPUTXBAR11_G2 Register

3.17.2.133.1 CONTROLSS_OUTPUTXBAR11_G2 Register (Offset = 3C8h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

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Table 3-2397. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83C8h

Figure 3-1244. CONTROLSS_OUTPUTXBAR11_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR11_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR11_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR11_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR11_G2_SEL							
R/W							
0h							

Table 3-2398. CONTROLSS_OUTPUTXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR11_G2_SEL	R/W	0h	G2: OUTPUT XBAR11 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.134 CONTROLSS_OUTPUTXBAR11_G3 Register

3.17.2.134.1 CONTROLSS_OUTPUTXBAR11_G3 Register (Offset = 3CCh) [reset = 0h]

OUTPUT XBAR 11 Input Select.

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Table 3-2399. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83CCh

Figure 3-1245. CONTROLSS_OUTPUTXBAR11_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR11_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR11_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR11_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR11_G3_SEL							
R/W							
0h							

Table 3-2400. CONTROLSS_OUTPUTXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR11_G3_SEL	R/W	0h	G3: OUTPUT XBAR11 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.135 CONTROLSS_OUTPUTXBAR11_G4 Register

3.17.2.135.1 CONTROLSS_OUTPUTXBAR11_G4 Register (Offset = 3D0h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to Summary Table

Table 3-2401. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83D0h

Figure 3-1246. CONTROLSS_OUTPUTXBAR11_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR11_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR11_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR11_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR11_G4_SEL							
R/W							
0h							

Table 3-2402. CONTROLSS_OUTPUTXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR11_G4_SEL	R/W	0h	G4: OUTPUT XBAR11 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.136 CONTROLSS_OUTPUTXBAR11_G5 Register

3.17.2.136.1 CONTROLSS_OUTPUTXBAR11_G5 Register (Offset = 3D4h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to Summary Table

Table 3-2403. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83D4h

Figure 3-1247. CONTROLSS_OUTPUTXBAR11_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR11_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR11_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR11_G5_SEL							
R/W							
0h							

Table 3-2404. CONTROLSS_OUTPUTXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR11_G5_SEL	R/W	0h	G5: OUTPUT XBAR11 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.137 CONTROLSS_OUTPUTXBAR11_G6 Register

3.17.2.137.1 CONTROLSS_OUTPUTXBAR11_G6 Register (Offset = 3D8h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to Summary Table

Table 3-2405. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83D8h

Figure 3-1248. CONTROLSS_OUTPUTXBAR11_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR11_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR11_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR11_G6_SEL							
R/W							
0h							

Table 3-2406. CONTROLSS_OUTPUTXBAR11_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR11_G6_SEL	R/W	0h	G6: OUTPUT XBAR11 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.138 CONTROLSS_OUTPUTXBAR11_G7 Register

3.17.2.138.1 CONTROLSS_OUTPUTXBAR11_G7 Register (Offset = 3DCh) [reset = 0h]

OUTPUT XBAR 11 Input Select.

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Table 3-2407. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83DCh

Figure 3-1249. CONTROLSS_OUTPUTXBAR11_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR11_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR11_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR11_G7_SEL							
R/W							
0h							

Table 3-2408. CONTROLSS_OUTPUTXBAR11_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR11_G7_SEL	R/W	0h	G7: OUTPUT XBAR11 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.139 CONTROLSS_OUTPUTXBAR11_G8 Register

3.17.2.139.1 CONTROLSS_OUTPUTXBAR11_G8 Register (Offset = 3E0h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

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Table 3-2409. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83E0h

Figure 3-1250. CONTROLSS_OUTPUTXBAR11_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR11_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR11_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR11_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR11_G8_SEL							
R/W							
0h							

Table 3-2410. CONTROLSS_OUTPUTXBAR11_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2410. CONTROLSS_OUTPUTXBAR11_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR11_G8_SEL	R/W	0h	G8: OUTPUT XBAR11 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.140 CONTROLSS_OUTPUTXBAR11_G9 Register

3.17.2.140.1 CONTROLSS_OUTPUTXBAR11_G9 Register (Offset = 3E4h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

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Table 3-2411. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83E4h

Figure 3-1251. CONTROLSS_OUTPUTXBAR11_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR11_G9_SEL	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR11_G9_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR11_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR11_G9_SEL							
R/W							
0h							

Table 3-2412. CONTROLSS_OUTPUTXBAR11_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2412. CONTROLSS_OUTPUTXBAR11_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR11_G9_SEL	R/W	0h	G9: OUTPUT XBAR11 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.141 CONTROLSS_OUTPUTXBAR11_G10 Register

3.17.2.141.1 CONTROLSS_OUTPUTXBAR11_G10 Register (Offset = 3E8h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to Summary Table

Table 3-2413. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 83E8h

Figure 3-1252. CONTROLSS_OUTPUTXBAR11_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		OUTPUTXBAR11_G10_SEL					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR11_G10_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR11_G10_SEL							
R/W							
0h							

Table 3-2414. CONTROLSS_OUTPUTXBAR11_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR11_G10_SEL	R/W	0h	G10: OUTPUT XBAR11 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.142 CONTROLSS_OUTPUTXBAR12_G0 Register

3.17.2.142.1 CONTROLSS_OUTPUTXBAR12_G0 Register (Offset = 400h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2415. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8400h

Figure 3-1253. CONTROLSS_OUTPUTXBAR12_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR12_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR12_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR12_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR12_G0_SEL							
R/W							
0h							

Table 3-2416. CONTROLSS_OUTPUTXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR12_G0_SEL	R/W	0h	G0: PWM XBAR12 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.143 CONTROLSS_OUTPUTXBAR12_G1 Register

3.17.2.143.1 CONTROLSS_OUTPUTXBAR12_G1 Register (Offset = 404h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2417. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8404h

Figure 3-1254. CONTROLSS_OUTPUTXBAR12_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR12_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR12_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR12_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR12_G1_SEL							
R/W							
0h							

Table 3-2418. CONTROLSS_OUTPUTXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR12_G1_SEL	R/W	0h	G1: OUTPUT XBAR12 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.144 CONTROLSS_OUTPUTXBAR12_G2 Register

3.17.2.144.1 CONTROLSS_OUTPUTXBAR12_G2 Register (Offset = 408h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2419. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8408h

Figure 3-1255. CONTROLSS_OUTPUTXBAR12_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR12_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR12_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR12_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR12_G2_SEL							
R/W							
0h							

Table 3-2420. CONTROLSS_OUTPUTXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR12_G2_SEL	R/W	0h	G2: OUTPUT XBAR12 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.145 CONTROLSS_OUTPUTXBAR12_G3 Register

3.17.2.145.1 CONTROLSS_OUTPUTXBAR12_G3 Register (Offset = 40Ch) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2421. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 840Ch

Figure 3-1256. CONTROLSS_OUTPUTXBAR12_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR12_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR12_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR12_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR12_G3_SEL							
R/W							
0h							

Table 3-2422. CONTROLSS_OUTPUTXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR12_G3_SEL	R/W	0h	G3: OUTPUT XBAR12 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.146 CONTROLSS_OUTPUTXBAR12_G4 Register

3.17.2.146.1 CONTROLSS_OUTPUTXBAR12_G4 Register (Offset = 410h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2423. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8410h

Figure 3-1257. CONTROLSS_OUTPUTXBAR12_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR12_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR12_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR12_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR12_G4_SEL							
R/W							
0h							

Table 3-2424. CONTROLSS_OUTPUTXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR12_G4_SEL	R/W	0h	G4: OUTPUT XBAR12 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.147 CONTROLSS_OUTPUTXBAR12_G5 Register

3.17.2.147.1 CONTROLSS_OUTPUTXBAR12_G5 Register (Offset = 414h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2425. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8414h

Figure 3-1258. CONTROLSS_OUTPUTXBAR12_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR12_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR12_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR12_G5_SEL							
R/W							
0h							

Table 3-2426. CONTROLSS_OUTPUTXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR12_G5_SEL	R/W	0h	G5: OUTPUT XBAR12 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.148 CONTROLSS_OUTPUTXBAR12_G6 Register

3.17.2.148.1 CONTROLSS_OUTPUTXBAR12_G6 Register (Offset = 418h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2427. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8418h

Figure 3-1259. CONTROLSS_OUTPUTXBAR12_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR12_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR12_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR12_G6_SEL							
R/W							
0h							

Table 3-2428. CONTROLSS_OUTPUTXBAR12_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR12_G6_SEL	R/W	0h	G6: OUTPUT XBAR12 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.149 CONTROLSS_OUTPUTXBAR12_G7 Register

3.17.2.149.1 CONTROLSS_OUTPUTXBAR12_G7 Register (Offset = 41Ch) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2429. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 841Ch

Figure 3-1260. CONTROLSS_OUTPUTXBAR12_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OUTPUTXBAR12_G7_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR12_G7_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR12_G7_SEL							
R/W							
0h							

Table 3-2430. CONTROLSS_OUTPUTXBAR12_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR12_G7_SEL	R/W	0h	G7: OUTPUT XBAR12 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.150 CONTROLSS_OUTPUTXBAR12_G8 Register

3.17.2.150.1 CONTROLSS_OUTPUTXBAR12_G8 Register (Offset = 420h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2431. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8420h

Figure 3-1261. CONTROLSS_OUTPUTXBAR12_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR12_G8_SEL			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR12_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR12_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR12_G8_SEL							
R/W							
0h							

Table 3-2432. CONTROLSS_OUTPUTXBAR12_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2432. CONTROLSS_OUTPUTXBAR12_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR12_G8_SEL	R/W	0h	G8: OUTPUT XBAR12 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.151 CONTROLSS_OUTPUTXBAR12_G9 Register

3.17.2.151.1 CONTROLSS_OUTPUTXBAR12_G9 Register (Offset = 424h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2433. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8424h

Figure 3-1262. CONTROLSS_OUTPUTXBAR12_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR12_G9_SEL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
OUTPUTXBAR12_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR12_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR12_G9_SEL							
R/W							
0h							

Table 3-2434. CONTROLSS_OUTPUTXBAR12_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2434. CONTROLSS_OUTPUTXBAR12_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR12_G9_SEL	R/W	0h	G9: OUTPUT XBAR12 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.152 CONTROLSS_OUTPUTXBAR12_G10 Register

3.17.2.152.1 CONTROLSS_OUTPUTXBAR12_G10 Register (Offset = 428h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

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Table 3-2435. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8428h

Figure 3-1263. CONTROLSS_OUTPUTXBAR12_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		OUTPUTXBAR12_G10_SEL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
OUTPUTXBAR12_G10_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR12_G10_SEL							
R/W							
0h							

Table 3-2436. CONTROLSS_OUTPUTXBAR12_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR12_G10_SEL	R/W	0h	G10: OUTPUT XBAR12 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.153 CONTROLSS_OUTPUTXBAR13_G0 Register

3.17.2.153.1 CONTROLSS_OUTPUTXBAR13_G0 Register (Offset = 440h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

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Table 3-2437. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8440h

Figure 3-1264. CONTROLSS_OUTPUTXBAR13_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR13_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR13_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR13_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR13_G0_SEL							
R/W							
0h							

Table 3-2438. CONTROLSS_OUTPUTXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR13_G0_SEL	R/W	0h	G0: PWM XBAR13 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.154 CONTROLSS_OUTPUTXBAR13_G1 Register

3.17.2.154.1 CONTROLSS_OUTPUTXBAR13_G1 Register (Offset = 444h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

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Table 3-2439. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8444h

Figure 3-1265. CONTROLSS_OUTPUTXBAR13_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR13_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR13_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR13_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR13_G1_SEL							
R/W							
0h							

Table 3-2440. CONTROLSS_OUTPUTXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR13_G1_SEL	R/W	0h	G1: OUTPUT XBAR13 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.155 CONTROLSS_OUTPUTXBAR13_G2 Register

3.17.2.155.1 CONTROLSS_OUTPUTXBAR13_G2 Register (Offset = 448h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to Summary Table

Table 3-2441. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8448h

Figure 3-1266. CONTROLSS_OUTPUTXBAR13_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR13_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR13_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR13_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR13_G2_SEL							
R/W							
0h							

Table 3-2442. CONTROLSS_OUTPUTXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR13_G2_SEL	R/W	0h	G2: OUTPUT XBAR13 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.156 CONTROLSS_OUTPUTXBAR13_G3 Register

3.17.2.156.1 CONTROLSS_OUTPUTXBAR13_G3 Register (Offset = 44Ch) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to Summary Table

Table 3-2443. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 844Ch

Figure 3-1267. CONTROLSS_OUTPUTXBAR13_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR13_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR13_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR13_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR13_G3_SEL							
R/W							
0h							

Table 3-2444. CONTROLSS_OUTPUTXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR13_G3_SEL	R/W	0h	G3: OUTPUT XBAR13 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.157 CONTROLSS_OUTPUTXBAR13_G4 Register

3.17.2.157.1 CONTROLSS_OUTPUTXBAR13_G4 Register (Offset = 450h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to Summary Table

Table 3-2445. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8450h

Figure 3-1268. CONTROLSS_OUTPUTXBAR13_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR13_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR13_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR13_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR13_G4_SEL							
R/W							
0h							

Table 3-2446. CONTROLSS_OUTPUTXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR13_G4_SEL	R/W	0h	G4: OUTPUT XBAR13 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.158 CONTROLSS_OUTPUTXBAR13_G5 Register

3.17.2.158.1 CONTROLSS_OUTPUTXBAR13_G5 Register (Offset = 454h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to Summary Table

Table 3-2447. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8454h

Figure 3-1269. CONTROLSS_OUTPUTXBAR13_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR13_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR13_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR13_G5_SEL							
R/W							
0h							

Table 3-2448. CONTROLSS_OUTPUTXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR13_G5_SEL	R/W	0h	G5: OUTPUT XBAR13 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.159 CONTROLSS_OUTPUTXBAR13_G6 Register

3.17.2.159.1 CONTROLSS_OUTPUTXBAR13_G6 Register (Offset = 458h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

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Table 3-2449. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8458h

Figure 3-1270. CONTROLSS_OUTPUTXBAR13_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR13_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR13_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR13_G6_SEL							
R/W							
0h							

Table 3-2450. CONTROLSS_OUTPUTXBAR13_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR13_G6_SEL	R/W	0h	G6: OUTPUT XBAR13 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.160 CONTROLSS_OUTPUTXBAR13_G7 Register

3.17.2.160.1 CONTROLSS_OUTPUTXBAR13_G7 Register (Offset = 45Ch) [reset = 0h]

OUTPUT XBAR 13 Input Select.

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Table 3-2451. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 845Ch

Figure 3-1271. CONTROLSS_OUTPUTXBAR13_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				OUTPUTXBAR13_G7_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR13_G7_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR13_G7_SEL							
R/W							
0h							

Table 3-2452. CONTROLSS_OUTPUTXBAR13_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR13_G7_SEL	R/W	0h	G7: OUTPUT XBAR13 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.161 CONTROLSS_OUTPUTXBAR13_G8 Register

3.17.2.161.1 CONTROLSS_OUTPUTXBAR13_G8 Register (Offset = 460h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

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Table 3-2453. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8460h

Figure 3-1272. CONTROLSS_OUTPUTXBAR13_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR13_G8_SEL			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR13_G8_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR13_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR13_G8_SEL							
R/W							
0h							

Table 3-2454. CONTROLSS_OUTPUTXBAR13_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2454. CONTROLSS_OUTPUTXBAR13_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR13_G8_SEL	R/W	0h	G8: OUTPUT XBAR13 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.162 CONTROLSS_OUTPUTXBAR13_G9 Register

3.17.2.162.1 CONTROLSS_OUTPUTXBAR13_G9 Register (Offset = 464h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

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Table 3-2455. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8464h

Figure 3-1273. CONTROLSS_OUTPUTXBAR13_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR13_G9_SEL	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR13_G9_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR13_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR13_G9_SEL							
R/W							
0h							

Table 3-2456. CONTROLSS_OUTPUTXBAR13_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2456. CONTROLSS_OUTPUTXBAR13_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR13_G9_SEL	R/W	0h	G9: OUTPUT XBAR13 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.163 CONTROLSS_OUTPUTXBAR13_G10 Register

3.17.2.163.1 CONTROLSS_OUTPUTXBAR13_G10 Register (Offset = 468h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

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Table 3-2457. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8468h

Figure 3-1274. CONTROLSS_OUTPUTXBAR13_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		OUTPUTXBAR13_G10_SEL					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR13_G10_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR13_G10_SEL							
R/W							
0h							

Table 3-2458. CONTROLSS_OUTPUTXBAR13_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR13_G10_SEL	R/W	0h	G10: OUTPUT XBAR13 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.164 CONTROLSS_OUTPUTXBAR14_G0 Register

3.17.2.164.1 CONTROLSS_OUTPUTXBAR14_G0 Register (Offset = 480h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to Summary Table

Table 3-2459. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8480h

Figure 3-1275. CONTROLSS_OUTPUTXBAR14_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR14_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR14_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G0_SEL							
R/W							
0h							

Table 3-2460. CONTROLSS_OUTPUTXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR14_G0_SEL	R/W	0h	G0: PWM XBAR14 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.165 CONTROLSS_OUTPUTXBAR14_G1 Register

3.17.2.165.1 CONTROLSS_OUTPUTXBAR14_G1 Register (Offset = 484h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to Summary Table

Table 3-2461. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8484h

Figure 3-1276. CONTROLSS_OUTPUTXBAR14_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR14_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR14_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G1_SEL							
R/W							
0h							

Table 3-2462. CONTROLSS_OUTPUTXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR14_G1_SEL	R/W	0h	G1: OUTPUT XBAR14 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.166 CONTROLSS_OUTPUTXBAR14_G2 Register

3.17.2.166.1 CONTROLSS_OUTPUTXBAR14_G2 Register (Offset = 488h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to Summary Table

Table 3-2463. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8488h

Figure 3-1277. CONTROLSS_OUTPUTXBAR14_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR14_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR14_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G2_SEL							
R/W							
0h							

Table 3-2464. CONTROLSS_OUTPUTXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR14_G2_SEL	R/W	0h	G2: OUTPUT XBAR14 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.167 CONTROLSS_OUTPUTXBAR14_G3 Register

3.17.2.167.1 CONTROLSS_OUTPUTXBAR14_G3 Register (Offset = 48Ch) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to Summary Table

Table 3-2465. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 848Ch

Figure 3-1278. CONTROLSS_OUTPUTXBAR14_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR14_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR14_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G3_SEL							
R/W							
0h							

Table 3-2466. CONTROLSS_OUTPUTXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR14_G3_SEL	R/W	0h	G3: OUTPUT XBAR14 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.168 CONTROLSS_OUTPUTXBAR14_G4 Register

3.17.2.168.1 CONTROLSS_OUTPUTXBAR14_G4 Register (Offset = 490h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to Summary Table

Table 3-2467. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8490h

Figure 3-1279. CONTROLSS_OUTPUTXBAR14_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR14_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR14_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G4_SEL							
R/W							
0h							

Table 3-2468. CONTROLSS_OUTPUTXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR14_G4_SEL	R/W	0h	G4: OUTPUT XBAR14 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.169 CONTROLSS_OUTPUTXBAR14_G5 Register

3.17.2.169.1 CONTROLSS_OUTPUTXBAR14_G5 Register (Offset = 494h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to Summary Table

Table 3-2469. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8494h

Figure 3-1280. CONTROLSS_OUTPUTXBAR14_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR14_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G5_SEL							
R/W							
0h							

Table 3-2470. CONTROLSS_OUTPUTXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR14_G5_SEL	R/W	0h	G5: OUTPUT XBAR14 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.170 CONTROLSS_OUTPUTXBAR14_G6 Register

3.17.2.170.1 CONTROLSS_OUTPUTXBAR14_G6 Register (Offset = 498h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to Summary Table

Table 3-2471. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8498h

Figure 3-1281. CONTROLSS_OUTPUTXBAR14_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR14_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G6_SEL							
R/W							
0h							

Table 3-2472. CONTROLSS_OUTPUTXBAR14_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR14_G6_SEL	R/W	0h	G6: OUTPUT XBAR14 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.171 CONTROLSS_OUTPUTXBAR14_G7 Register

3.17.2.171.1 CONTROLSS_OUTPUTXBAR14_G7 Register (Offset = 49Ch) [reset = 0h]

OUTPUT XBAR 14 Input Select.

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Table 3-2473. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 849Ch

Figure 3-1282. CONTROLSS_OUTPUTXBAR14_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR14_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G7_SEL							
R/W							
0h							

Table 3-2474. CONTROLSS_OUTPUTXBAR14_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR14_G7_SEL	R/W	0h	G7: OUTPUT XBAR14 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.172 CONTROLSS_OUTPUTXBAR14_G8 Register

3.17.2.172.1 CONTROLSS_OUTPUTXBAR14_G8 Register (Offset = 4A0h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

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Table 3-2475. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84A0h

Figure 3-1283. CONTROLSS_OUTPUTXBAR14_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR14_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR14_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G8_SEL							
R/W							
0h							

Table 3-2476. CONTROLSS_OUTPUTXBAR14_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2476. CONTROLSS_OUTPUTXBAR14_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR14_G8_SEL	R/W	0h	G8: OUTPUT XBAR14 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.173 CONTROLSS_OUTPUTXBAR14_G9 Register

3.17.2.173.1 CONTROLSS_OUTPUTXBAR14_G9 Register (Offset = 4A4h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

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Table 3-2477. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84A4h

Figure 3-1284. CONTROLSS_OUTPUTXBAR14_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							OUTPUTXBAR14_G9_SEL
NONE							R/W
0h							0h
23	22	21	20	19	18	17	16
OUTPUTXBAR14_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G9_SEL							
R/W							
0h							

Table 3-2478. CONTROLSS_OUTPUTXBAR14_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2478. CONTROLSS_OUTPUTXBAR14_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR14_G9_SEL	R/W	0h	G9: OUTPUT XBAR14 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.174 CONTROLSS_OUTPUTXBAR14_G10 Register

3.17.2.174.1 CONTROLSS_OUTPUTXBAR14_G10 Register (Offset = 4A8h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

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Table 3-2479. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84A8h

Figure 3-1285. CONTROLSS_OUTPUTXBAR14_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		OUTPUTXBAR14_G10_SEL					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
OUTPUTXBAR14_G10_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR14_G10_SEL							
R/W							
0h							

Table 3-2480. CONTROLSS_OUTPUTXBAR14_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR14_G10_SEL	R/W	0h	G10: OUTPUT XBAR14 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.17.2.175 CONTROLSS_OUTPUTXBAR15_G0 Register

3.17.2.175.1 CONTROLSS_OUTPUTXBAR15_G0 Register (Offset = 4C0h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2481. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84C0h

Figure 3-1286. CONTROLSS_OUTPUTXBAR15_G0 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR15_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR15_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR15_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR15_G0_SEL							
R/W							
0h							

Table 3-2482. CONTROLSS_OUTPUTXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR15_G0_SEL	R/W	0h	G0: PWM XBAR15 G0 input bit select. Input source is PWM[x].TRIPOUT 1:PWM[x] TRIPOUT selected 0:PWM[x] TRIPOUT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.176 CONTROLSS_OUTPUTXBAR15_G1 Register

3.17.2.176.1 CONTROLSS_OUTPUTXBAR15_G1 Register (Offset = 4C4h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2483. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84C4h

Figure 3-1287. CONTROLSS_OUTPUTXBAR15_G1 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR15_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR15_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR15_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR15_G1_SEL							
R/W							
0h							

Table 3-2484. CONTROLSS_OUTPUTXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR15_G1_SEL	R/W	0h	G1: OUTPUT XBAR15 G1 input bit select. Input source is PWM[x].SOCA 1:PWM[x] SOCA selected 0:PWM[x] SOCA is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.177 CONTROLSS_OUTPUTXBAR15_G2 Register

3.17.2.177.1 CONTROLSS_OUTPUTXBAR15_G2 Register (Offset = 4C8h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2485. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84C8h

Figure 3-1288. CONTROLSS_OUTPUTXBAR15_G2 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR15_G2_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OUTPUTXBAR15_G2_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR15_G2_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR15_G2_SEL							
R/W							
0h							

Table 3-2486. CONTROLSS_OUTPUTXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR15_G2_SEL	R/W	0h	G2: OUTPUT XBAR15 G2 input bit select. Input source is PWM[x].SOCB 1:PWM[x] SOCB selected 0:PWM[x] SOCB is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.17.2.178 CONTROLSS_OUTPUTXBAR15_G3 Register

3.17.2.178.1 CONTROLSS_OUTPUTXBAR15_G3 Register (Offset = 4CCh) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2487. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84CCh

Figure 3-1289. CONTROLSS_OUTPUTXBAR15_G3 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR15_G3_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR15_G3_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR15_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR15_G3_SEL							
R/W							
0h							

Table 3-2488. CONTROLSS_OUTPUTXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR15_G3_SEL	R/W	0h	G3: OUTPUT XBAR15 G3 input bit select. Input source is DEL[x].ACTIVE 1:DEL[x] ACTIVE selected 0: DEL[x] ACTIVE is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.179 CONTROLSS_OUTPUTXBAR15_G4 Register

3.17.2.179.1 CONTROLSS_OUTPUTXBAR15_G4 Register (Offset = 4D0h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2489. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84D0h

Figure 3-1290. CONTROLSS_OUTPUTXBAR15_G4 Name Register

31	30	29	28	27	26	25	24
OUTPUTXBAR15_G4_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR15_G4_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR15_G4_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR15_G4_SEL							
R/W							
0h							

Table 3-2490. CONTROLSS_OUTPUTXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	OUTPUTXBAR15_G4_SEL	R/W	0h	G4: OUTPUT XBAR15 G4 input bit select. Input source is DEL[x].TRIP 1:DEL[x] TRIP selected 0: DEL[x] TRIP is de-selected x can have value from 0 to 31 corresponding to each DEL instance

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3.17.2.180 CONTROLSS_OUTPUTXBAR15_G5 Register

3.17.2.180.1 CONTROLSS_OUTPUTXBAR15_G5 Register (Offset = 4D4h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2491. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84D4h

Figure 3-1291. CONTROLSS_OUTPUTXBAR15_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
OUTPUTXBAR15_G5_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR15_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR15_G5_SEL							
R/W							
0h							

Table 3-2492. CONTROLSS_OUTPUTXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	OUTPUTXBAR15_G5_SEL	R/W	0h	G5: OUTPUT XBAR15 G5 input bit select. 0:SDFM0.FILT1CEVT1 1:SDFM0.FILT1CEVT2 2:SDFM0.FILT1COMPHZ 3:SDFM0.FILT2CEVT1 4:SDFM0.FILT2CEVT2 5:SDFM0.FILT2COMPHZ 6:SDFM0.FILT3CEVT1 7:SDFM0.FILT3CEVT2 8:SDFM0.FILT3COMPHZ 9:SDFM0.FILT4CEVT1 10:SDFM0.FILT4CEVT2 11:SDFM0.FILT4COMPHZ 12:SDFM1.FILT1CEVT1 13:SDFM1.FILT1CEVT2 14:SDFM1.FILT1COMPHZ 15:SDFM1.FILT2CEVT1 16:SDFM1.FILT2CEVT2 17:SDFM1.FILT2COMPHZ 18:SDFM1.FILT3CEVT1 19:SDFM1.FILT3CEVT2 20:SDFM1.FILT3COMPHZ 21:SDFM1.FILT4CEVT1 22:SDFM1.FILT4CEVT2 23:SDFM1.FILT4COMPHZ

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3.17.2.181 CONTROLSS_OUTPUTXBAR15_G6 Register

3.17.2.181.1 CONTROLSS_OUTPUTXBAR15_G6 Register (Offset = 4D8h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2493. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84D8h

Figure 3-1292. CONTROLSS_OUTPUTXBAR15_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR15_G6_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR15_G6_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR15_G6_SEL							
R/W							
0h							

Table 3-2494. CONTROLSS_OUTPUTXBAR15_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR15_G6_SEL	R/W	0h	G6: OUTPUT XBAR15 G6 Input Select 0:CMP12SS0.CTRIPOUTL 1:CMP12SS0.CTRIPOUTH 2:CMP12SS1.CTRIPOUTL 3:CMP12SS1.CTRIPOUTH 4:CMP12SS2.CTRIPOUTL 5:CMP12SS2.CTRIPOUTH 6:CMP12SS3.CTRIPOUTL 7:CMP12SS3.CTRIPOUTH 8:CMP12SS4.CTRIPOUTL 9:CMP12SS4.CTRIPOUTH 10:CMP12SS5.CTRIPOUTL 11:CMP12SS5.CTRIPOUTH 12:CMP12SS6.CTRIPOUTL 13:CMP12SS6.CTRIPOUTH 14:CMP12SS7.CTRIPOUTL 15:CMP12SS7.CTRIPOUTH 16:CMP12SS8.CTRIPOUTL 17:CMP12SS8.CTRIPOUTH 18:CMP12SS9.CTRIPOUTL 19:CMP12SS9.CTRIPOUTH

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3.17.2.182 CONTROLSS_OUTPUTXBAR15_G7 Register

3.17.2.182.1 CONTROLSS_OUTPUTXBAR15_G7 Register (Offset = 4DCh) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2495. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84DCh

Figure 3-1293. CONTROLSS_OUTPUTXBAR15_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				OUTPUTXBAR15_G7_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
OUTPUTXBAR15_G7_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR15_G7_SEL							
R/W							
0h							

Table 3-2496. CONTROLSS_OUTPUTXBAR15_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	OUTPUTXBAR15_G7_SEL	R/W	0h	G7: OUTPUT XBAR15 G7 Input Select 0:CMP8SS0.CTRIPOUTL 1:CMP8SS0.CTRIPOUTH 2:CMP8SS1.CTRIPOUTL 3:CMP8SS1.CTRIPOUTH 4:CMP8SS2.CTRIPOUTL 5:CMP8SS2.CTRIPOUTH 6:CMP8SS3.CTRIPOUTL 7:CMP8SS3.CTRIPOUTH 8:CMP8SS4.CTRIPOUTL 9:CMP8SS4.CTRIPOUTH 10:CMP8SS5.CTRIPOUTL 11:CMP8SS5.CTRIPOUTH 12:CMP8SS6.CTRIPOUTL 13:CMP8SS6.CTRIPOUTH 14:CMP8SS7.CTRIPOUTL 15:CMP8SS7.CTRIPOUTH 16:CMP8SS8.CTRIPOUTL 17:CMP8SS8.CTRIPOUTH 18:CMP8SS9.CTRIPOUTL 19:CMP8SS9.CTRIPOUTH

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3.17.2.183 CONTROLSS_OUTPUTXBAR15_G8 Register

3.17.2.183.1 CONTROLSS_OUTPUTXBAR15_G8 Register (Offset = 4E0h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2497. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84E0h

Figure 3-1294. CONTROLSS_OUTPUTXBAR15_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED				OUTPUTXBAR15_G8_SEL			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
OUTPUTXBAR15_G8_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR15_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR15_G8_SEL							
R/W							
0h							

Table 3-2498. CONTROLSS_OUTPUTXBAR15_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved

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Table 3-2498. CONTROLSS_OUTPUTXBAR15_G8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:0	OUTPUTXBAR15_G8_SEL	R/W	0h	G8: OUTPUT XBAR15 G8 Input Select 0:ADC0.EVT1 1:ADC0.EVT2 2:ADC0.EVT3 3:ADC0.EVT4 4:ADC1.EVT1 5:ADC1.EVT2 6:ADC1.EVT3 7:ADC1 EVT4 8:ADC2.EVT1 9:ADC2 EVT2 10:ADC2.EVT3 11:ADC2.EVT4 12:ADC3.EVT1 13:ADC3.EVT2 14:ADC3.EVT3 15:ADC3.EVT4 16:ADC4.EVT1 17:ADC4.EVT2 18:ADC4.EVT3 19:ADC4.EVT4 20:ADCR0.EVT1 21:ADCR0.EVT2 22:ADCR0.EVT3 23:ADCR0.EVT4 24:ADCR1.EVT1 25:ADCR1.EVT2 26:ADCR1.EVT3 27:ADCR1.EVT4

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3.17.2.184 CONTROLSS_OUTPUTXBAR15_G9 Register

3.17.2.184.1 CONTROLSS_OUTPUTXBAR15_G9 Register (Offset = 4E4h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2499. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84E4h

Figure 3-1295. CONTROLSS_OUTPUTXBAR15_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED						OUTPUTXBAR15_G9_SEL	
NONE						R/W	
0h						0h	
23	22	21	20	19	18	17	16
OUTPUTXBAR15_G9_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
OUTPUTXBAR15_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
OUTPUTXBAR15_G9_SEL							
R/W							
0h							

Table 3-2500. CONTROLSS_OUTPUTXBAR15_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved

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Table 3-2500. CONTROLSS_OUTPUTXBAR15_G9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25:0	OUTPUTXBAR15_G9_SEL	R/W	0h	G9: OUTPUT XBAR15 G9 Input Select 0:PWMSyncOutXBAR.SYNCOUT0 1:PWMSyncOutXBAR.SYNCOUT1 2:PWMSyncOutXBAR.SYNCOUT2 3:PWMSyncOutXBAR.SYNCOUT3 4:EQEP0.I_OUT 5:EQEP0.S_OUT 6:EQEP1.I_OUT 7:EQEP1.S_OUT 8:EQEP2.I_OUT 9:EQEP2.S_OUT 10:ECAP0.OUT 11:ECAP1.OUT 12:ECAP2.OUT 13:ECAP3.OUT 14:ECAP4.OUT 15:ECAP5.OUT 16:ECAP6.OUT 17:ECAP7.OUT 18:ECAP8.OUT 19:ECAP9.OUT 20:ECAP10.OUT 21:ECAP11.OUT 22:ECAP12.OUT 23:ECAP13.OUT 24:ECAP14.OUT 25:ECAP15.OUT

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3.17.2.185 CONTROLSS_OUTPUTXBAR15_G10 Register

3.17.2.185.1 CONTROLSS_OUTPUTXBAR15_G10 Register (Offset = 4E8h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to Summary Table

Table 3-2501. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 84E8h

Figure 3-1296. CONTROLSS_OUTPUTXBAR15_G10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		OUTPUTXBAR15_G10_SEL					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
OUTPUTXBAR15_G10_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTPUTXBAR15_G10_SEL							
R/W							
0h							

Table 3-2502. CONTROLSS_OUTPUTXBAR15_G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	OUTPUTXBAR15_G10_SEL	R/W	0h	G10: OUTPUT XBAR15 G10 Input Select [3:0]: FSIRX0.RX_TRIG[3:0] [7:4]: FSIRX1.RX_TRIG[3:0] [11:8]: FSIRX2.RX_TRIG[3:0] [15:12]: FSIRX3.RX_TRIG[3:0] 16:INPUTXBAR.OUT7 17:INPUTXBAR.OUT15 18:INPUTXBAR.OUT23 19:INPUTXBAR.OUT31 20:INTXBAR.OUT7 21:INTXBAR.OUT15

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3.18 CONTROLSS_ICLXBAR

CONTROLSS_ICLXBAR

3.18.1 CONTROLSS_ICLXBAR Summaries

CONTROLSS_ICLXBAR Summaries

Table 3-2503. CONTROLSS Registers, Base Address=502D 4000h, Length=4096

Offset	Length	Register Name	CONTROLSS_ICLXBAR Physical Address
100h	32	CONTROLSS_ICLXBAR0_G0	502D 4100h
104h	32	CONTROLSS_ICLXBAR0_G1	502D 4104h
108h	32	CONTROLSS_ICLXBAR0_G2	502D 4108h
140h	32	CONTROLSS_ICLXBAR1_G0	502D 4140h
144h	32	CONTROLSS_ICLXBAR1_G1	502D 4144h
148h	32	CONTROLSS_ICLXBAR1_G2	502D 4148h
180h	32	CONTROLSS_ICLXBAR2_G0	502D 4180h
184h	32	CONTROLSS_ICLXBAR2_G1	502D 4184h
188h	32	CONTROLSS_ICLXBAR2_G2	502D 4188h
1C0h	32	CONTROLSS_ICLXBAR3_G0	502D 41C0h
1C4h	32	CONTROLSS_ICLXBAR3_G1	502D 41C4h
1C8h	32	CONTROLSS_ICLXBAR3_G2	502D 41C8h
200h	32	CONTROLSS_ICLXBAR4_G0	502D 4200h
204h	32	CONTROLSS_ICLXBAR4_G1	502D 4204h
208h	32	CONTROLSS_ICLXBAR4_G2	502D 4208h
240h	32	CONTROLSS_ICLXBAR5_G0	502D 4240h
244h	32	CONTROLSS_ICLXBAR5_G1	502D 4244h
248h	32	CONTROLSS_ICLXBAR5_G2	502D 4248h
280h	32	CONTROLSS_ICLXBAR6_G0	502D 4280h
284h	32	CONTROLSS_ICLXBAR6_G1	502D 4284h
288h	32	CONTROLSS_ICLXBAR6_G2	502D 4288h
2C0h	32	CONTROLSS_ICLXBAR7_G0	502D 42C0h
2C4h	32	CONTROLSS_ICLXBAR7_G1	502D 42C4h
2C8h	32	CONTROLSS_ICLXBAR7_G2	502D 42C8h
300h	32	CONTROLSS_ICLXBAR8_G0	502D 4300h
304h	32	CONTROLSS_ICLXBAR8_G1	502D 4304h
308h	32	CONTROLSS_ICLXBAR8_G2	502D 4308h
340h	32	CONTROLSS_ICLXBAR9_G0	502D 4340h
344h	32	CONTROLSS_ICLXBAR9_G1	502D 4344h
348h	32	CONTROLSS_ICLXBAR9_G2	502D 4348h
380h	32	CONTROLSS_ICLXBAR10_G0	502D 4380h
384h	32	CONTROLSS_ICLXBAR10_G1	502D 4384h
388h	32	CONTROLSS_ICLXBAR10_G2	502D 4388h
3C0h	32	CONTROLSS_ICLXBAR11_G0	502D 43C0h
3C4h	32	CONTROLSS_ICLXBAR11_G1	502D 43C4h
3C8h	32	CONTROLSS_ICLXBAR11_G2	502D 43C8h
400h	32	CONTROLSS_ICLXBAR12_G0	502D 4400h
404h	32	CONTROLSS_ICLXBAR12_G1	502D 4404h
408h	32	CONTROLSS_ICLXBAR12_G2	502D 4408h

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Table 3-2503. CONTROLSS Registers, Base Address=502D 4000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_ICLXBAR Physical Address
440h	32	CONTROLSS_ICLXBAR13_G0	502D 4440h
444h	32	CONTROLSS_ICLXBAR13_G1	502D 4444h
448h	32	CONTROLSS_ICLXBAR13_G2	502D 4448h
480h	32	CONTROLSS_ICLXBAR14_G0	502D 4480h
484h	32	CONTROLSS_ICLXBAR14_G1	502D 4484h
488h	32	CONTROLSS_ICLXBAR14_G2	502D 4488h
4C0h	32	CONTROLSS_ICLXBAR15_G0	502D 44C0h
4C4h	32	CONTROLSS_ICLXBAR15_G1	502D 44C4h
4C8h	32	CONTROLSS_ICLXBAR15_G2	502D 44C8h

3.18.2 CONTROLSS_ICLXBAR Registers

CONTROLSS_ICLXBAR Registers

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3.18.2.1 CONTROLSS_ICLXBAR0_G0 Register

3.18.2.1.1 CONTROLSS_ICLXBAR0_G0 Register (Offset = 100h) [reset = 0h]

ICL XBAR 0 Input Select.

Return to Summary Table

Table 3-2504. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4100h

Figure 3-1297. CONTROLSS_ICLXBAR0_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR0_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR0_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR0_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR0_G0_SEL							
R/W							
0h							

Table 3-2505. CONTROLSS_ICLXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR0_G0_SEL	R/W	0h	ICL XBAR0 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.2 CONTROLSS_ICLXBAR0_G1 Register

3.18.2.2.1 CONTROLSS_ICLXBAR0_G1 Register (Offset = 104h) [reset = 0h]

ICL XBAR 0 Input Select.

Return to Summary Table

Table 3-2506. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4104h

Figure 3-1298. CONTROLSS_ICLXBAR0_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR0_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR0_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR0_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR0_G1_SEL							
R/W							
0h							

Table 3-2507. CONTROLSS_ICLXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR0_G1_SEL	R/W	0h	ICL XBAR0 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.3 CONTROLSS_ICLXBAR0_G2 Register

3.18.2.3.1 CONTROLSS_ICLXBAR0_G2 Register (Offset = 108h) [reset = 0h]

ICL XBAR 0 Input Select.

Return to Summary Table

Table 3-2508. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4108h

Figure 3-1299. CONTROLSS_ICLXBAR0_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR0_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR0_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR0_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR0_G2_SEL							
R/W							
0h							

Table 3-2509. CONTROLSS_ICLXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR0_G2_SEL	R/W	0h	ICL XBAR0 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.4 CONTROLSS_ICLXBAR1_G0 Register

3.18.2.4.1 CONTROLSS_ICLXBAR1_G0 Register (Offset = 140h) [reset = 0h]

ICL XBAR 1 Input Select.

Return to Summary Table

Table 3-2510. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4140h

Figure 3-1300. CONTROLSS_ICLXBAR1_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR1_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR1_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR1_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR1_G0_SEL							
R/W							
0h							

Table 3-2511. CONTROLSS_ICLXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR1_G0_SEL	R/W	0h	ICL XBAR1 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.5 CONTROLSS_ICLXBAR1_G1 Register

3.18.2.5.1 CONTROLSS_ICLXBAR1_G1 Register (Offset = 144h) [reset = 0h]

ICL XBAR 1 Input Select.

Return to Summary Table

Table 3-2512. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4144h

Figure 3-1301. CONTROLSS_ICLXBAR1_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR1_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR1_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR1_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR1_G1_SEL							
R/W							
0h							

Table 3-2513. CONTROLSS_ICLXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR1_G1_SEL	R/W	0h	ICL XBAR1 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.6 CONTROLSS_ICLXBAR1_G2 Register

3.18.2.6.1 CONTROLSS_ICLXBAR1_G2 Register (Offset = 148h) [reset = 0h]

ICL XBAR 1 Input Select.

Return to Summary Table

Table 3-2514. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4148h

Figure 3-1302. CONTROLSS_ICLXBAR1_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR1_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR1_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR1_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR1_G2_SEL							
R/W							
0h							

Table 3-2515. CONTROLSS_ICLXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR1_G2_SEL	R/W	0h	ICL XBAR1 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.7 CONTROLSS_ICLXBAR2_G0 Register

3.18.2.7.1 CONTROLSS_ICLXBAR2_G0 Register (Offset = 180h) [reset = 0h]

ICL XBAR 2 Input Select.

Return to Summary Table

Table 3-2516. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4180h

Figure 3-1303. CONTROLSS_ICLXBAR2_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR2_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR2_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR2_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR2_G0_SEL							
R/W							
0h							

Table 3-2517. CONTROLSS_ICLXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR2_G0_SEL	R/W	0h	ICL XBAR2 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.8 CONTROLSS_ICLXBAR2_G1 Register

3.18.2.8.1 CONTROLSS_ICLXBAR2_G1 Register (Offset = 184h) [reset = 0h]

ICL XBAR 2 Input Select.

Return to Summary Table

Table 3-2518. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4184h

Figure 3-1304. CONTROLSS_ICLXBAR2_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR2_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR2_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR2_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR2_G1_SEL							
R/W							
0h							

Table 3-2519. CONTROLSS_ICLXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR2_G1_SEL	R/W	0h	ICL XBAR2 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.9 CONTROLSS_ICLXBAR2_G2 Register

3.18.2.9.1 CONTROLSS_ICLXBAR2_G2 Register (Offset = 188h) [reset = 0h]

ICL XBAR 2 Input Select.

Return to Summary Table

Table 3-2520. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4188h

Figure 3-1305. CONTROLSS_ICLXBAR2_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR2_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR2_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR2_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR2_G2_SEL							
R/W							
0h							

Table 3-2521. CONTROLSS_ICLXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR2_G2_SEL	R/W	0h	ICL XBAR2 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.10 CONTROLSS_ICLXBAR3_G0 Register

3.18.2.10.1 CONTROLSS_ICLXBAR3_G0 Register (Offset = 1C0h) [reset = 0h]

ICL XBAR 3 Input Select.

Return to Summary Table

Table 3-2522. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 41C0h

Figure 3-1306. CONTROLSS_ICLXBAR3_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR3_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR3_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR3_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR3_G0_SEL							
R/W							
0h							

Table 3-2523. CONTROLSS_ICLXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR3_G0_SEL	R/W	0h	ICL XBAR3 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.11 CONTROLSS_ICLXBAR3_G1 Register

3.18.2.11.1 CONTROLSS_ICLXBAR3_G1 Register (Offset = 1C4h) [reset = 0h]

ICL XBAR 3 Input Select.

Return to Summary Table

Table 3-2524. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 41C4h

Figure 3-1307. CONTROLSS_ICLXBAR3_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR3_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR3_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR3_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR3_G1_SEL							
R/W							
0h							

Table 3-2525. CONTROLSS_ICLXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR3_G1_SEL	R/W	0h	ICL XBAR3 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.12 CONTROLSS_ICLXBAR3_G2 Register

3.18.2.12.1 CONTROLSS_ICLXBAR3_G2 Register (Offset = 1C8h) [reset = 0h]

ICL XBAR 3 Input Select.

Return to Summary Table

Table 3-2526. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 41C8h

Figure 3-1308. CONTROLSS_ICLXBAR3_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR3_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR3_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR3_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR3_G2_SEL							
R/W							
0h							

Table 3-2527. CONTROLSS_ICLXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR3_G2_SEL	R/W	0h	ICL XBAR3 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.13 CONTROLSS_ICLXBAR4_G0 Register

3.18.2.13.1 CONTROLSS_ICLXBAR4_G0 Register (Offset = 200h) [reset = 0h]

ICL XBAR 4 Input Select.

Return to Summary Table

Table 3-2528. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4200h

Figure 3-1309. CONTROLSS_ICLXBAR4_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR4_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR4_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR4_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR4_G0_SEL							
R/W							
0h							

Table 3-2529. CONTROLSS_ICLXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR4_G0_SEL	R/W	0h	ICL XBAR4 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.14 CONTROLSS_ICLXBAR4_G1 Register

3.18.2.14.1 CONTROLSS_ICLXBAR4_G1 Register (Offset = 204h) [reset = 0h]

ICL XBAR 4 Input Select.

Return to Summary Table

Table 3-2530. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4204h

Figure 3-1310. CONTROLSS_ICLXBAR4_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR4_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR4_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR4_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR4_G1_SEL							
R/W							
0h							

Table 3-2531. CONTROLSS_ICLXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR4_G1_SEL	R/W	0h	ICL XBAR4 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.15 CONTROLSS_ICLXBAR4_G2 Register

3.18.2.15.1 CONTROLSS_ICLXBAR4_G2 Register (Offset = 208h) [reset = 0h]

ICL XBAR 4 Input Select.

Return to Summary Table

Table 3-2532. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4208h

Figure 3-1311. CONTROLSS_ICLXBAR4_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR4_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR4_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR4_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR4_G2_SEL							
R/W							
0h							

Table 3-2533. CONTROLSS_ICLXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR4_G2_SEL	R/W	0h	ICL XBAR4 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.16 CONTROLSS_ICLXBAR5_G0 Register

3.18.2.16.1 CONTROLSS_ICLXBAR5_G0 Register (Offset = 240h) [reset = 0h]

ICL XBAR 5 Input Select.

Return to Summary Table

Table 3-2534. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4240h

Figure 3-1312. CONTROLSS_ICLXBAR5_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR5_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR5_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR5_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR5_G0_SEL							
R/W							
0h							

Table 3-2535. CONTROLSS_ICLXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR5_G0_SEL	R/W	0h	ICL XBAR5 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.17 CONTROLSS_ICLXBAR5_G1 Register

3.18.2.17.1 CONTROLSS_ICLXBAR5_G1 Register (Offset = 244h) [reset = 0h]

ICL XBAR 5 Input Select.

Return to Summary Table

Table 3-2536. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4244h

Figure 3-1313. CONTROLSS_ICLXBAR5_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR5_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR5_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR5_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR5_G1_SEL							
R/W							
0h							

Table 3-2537. CONTROLSS_ICLXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR5_G1_SEL	R/W	0h	ICL XBAR5 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.18 CONTROLSS_ICLXBAR5_G2 Register

3.18.2.18.1 CONTROLSS_ICLXBAR5_G2 Register (Offset = 248h) [reset = 0h]

ICL XBAR 5 Input Select.

Return to Summary Table

Table 3-2538. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4248h

Figure 3-1314. CONTROLSS_ICLXBAR5_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR5_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR5_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR5_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR5_G2_SEL							
R/W							
0h							

Table 3-2539. CONTROLSS_ICLXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR5_G2_SEL	R/W	0h	ICL XBAR5 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.19 CONTROLSS_ICLXBAR6_G0 Register

3.18.2.19.1 CONTROLSS_ICLXBAR6_G0 Register (Offset = 280h) [reset = 0h]

ICL XBAR 6 Input Select.

Return to Summary Table

Table 3-2540. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4280h

Figure 3-1315. CONTROLSS_ICLXBAR6_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR6_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR6_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR6_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR6_G0_SEL							
R/W							
0h							

Table 3-2541. CONTROLSS_ICLXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR6_G0_SEL	R/W	0h	ICL XBAR6 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.20 CONTROLSS_ICLXBAR6_G1 Register

3.18.2.20.1 CONTROLSS_ICLXBAR6_G1 Register (Offset = 284h) [reset = 0h]

ICL XBAR 6 Input Select.

Return to Summary Table

Table 3-2542. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4284h

Figure 3-1316. CONTROLSS_ICLXBAR6_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR6_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR6_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR6_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR6_G1_SEL							
R/W							
0h							

Table 3-2543. CONTROLSS_ICLXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR6_G1_SEL	R/W	0h	ICL XBAR6 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.21 CONTROLSS_ICLXBAR6_G2 Register

3.18.2.21.1 CONTROLSS_ICLXBAR6_G2 Register (Offset = 288h) [reset = 0h]

ICL XBAR 6 Input Select.

Return to Summary Table

Table 3-2544. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4288h

Figure 3-1317. CONTROLSS_ICLXBAR6_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR6_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR6_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR6_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR6_G2_SEL							
R/W							
0h							

Table 3-2545. CONTROLSS_ICLXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR6_G2_SEL	R/W	0h	ICL XBAR6 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.22 CONTROLSS_ICLXBAR7_G0 Register

3.18.2.22.1 CONTROLSS_ICLXBAR7_G0 Register (Offset = 2C0h) [reset = 0h]

ICL XBAR 7 Input Select.

Return to Summary Table

Table 3-2546. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 42C0h

Figure 3-1318. CONTROLSS_ICLXBAR7_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR7_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR7_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR7_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR7_G0_SEL							
R/W							
0h							

Table 3-2547. CONTROLSS_ICLXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR7_G0_SEL	R/W	0h	ICL XBAR7 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.23 CONTROLSS_ICLXBAR7_G1 Register

3.18.2.23.1 CONTROLSS_ICLXBAR7_G1 Register (Offset = 2C4h) [reset = 0h]

ICL XBAR 7 Input Select.

Return to Summary Table

Table 3-2548. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 42C4h

Figure 3-1319. CONTROLSS_ICLXBAR7_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR7_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR7_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR7_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR7_G1_SEL							
R/W							
0h							

Table 3-2549. CONTROLSS_ICLXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR7_G1_SEL	R/W	0h	ICL XBAR7 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.24 CONTROLSS_ICLXBAR7_G2 Register

3.18.2.24.1 CONTROLSS_ICLXBAR7_G2 Register (Offset = 2C8h) [reset = 0h]

ICL XBAR 7 Input Select.

Return to Summary Table

Table 3-2550. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 42C8h

Figure 3-1320. CONTROLSS_ICLXBAR7_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR7_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR7_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR7_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR7_G2_SEL							
R/W							
0h							

Table 3-2551. CONTROLSS_ICLXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR7_G2_SEL	R/W	0h	ICL XBAR7 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.25 CONTROLSS_ICLXBAR8_G0 Register

3.18.2.25.1 CONTROLSS_ICLXBAR8_G0 Register (Offset = 300h) [reset = 0h]

ICL XBAR 8 Input Select.

Return to Summary Table

Table 3-2552. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4300h

Figure 3-1321. CONTROLSS_ICLXBAR8_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR8_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR8_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR8_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR8_G0_SEL							
R/W							
0h							

Table 3-2553. CONTROLSS_ICLXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR8_G0_SEL	R/W	0h	ICL XBAR8 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.26 CONTROLSS_ICLXBAR8_G1 Register

3.18.2.26.1 CONTROLSS_ICLXBAR8_G1 Register (Offset = 304h) [reset = 0h]

ICL XBAR 8 Input Select.

Return to Summary Table

Table 3-2554. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4304h

Figure 3-1322. CONTROLSS_ICLXBAR8_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR8_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR8_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR8_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR8_G1_SEL							
R/W							
0h							

Table 3-2555. CONTROLSS_ICLXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR8_G1_SEL	R/W	0h	ICL XBAR8 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.27 CONTROLSS_ICLXBAR8_G2 Register

3.18.2.27.1 CONTROLSS_ICLXBAR8_G2 Register (Offset = 308h) [reset = 0h]

ICL XBAR 8 Input Select.

Return to Summary Table

Table 3-2556. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4308h

Figure 3-1323. CONTROLSS_ICLXBAR8_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR8_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR8_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR8_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR8_G2_SEL							
R/W							
0h							

Table 3-2557. CONTROLSS_ICLXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR8_G2_SEL	R/W	0h	ICL XBAR8 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.28 CONTROLSS_ICLXBAR9_G0 Register

3.18.2.28.1 CONTROLSS_ICLXBAR9_G0 Register (Offset = 340h) [reset = 0h]

ICL XBAR 9 Input Select.

Return to Summary Table

Table 3-2558. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4340h

Figure 3-1324. CONTROLSS_ICLXBAR9_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR9_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR9_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR9_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR9_G0_SEL							
R/W							
0h							

Table 3-2559. CONTROLSS_ICLXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR9_G0_SEL	R/W	0h	ICL XBAR9 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.29 CONTROLSS_ICLXBAR9_G1 Register

3.18.2.29.1 CONTROLSS_ICLXBAR9_G1 Register (Offset = 344h) [reset = 0h]

ICL XBAR 9 Input Select.

Return to Summary Table

Table 3-2560. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4344h

Figure 3-1325. CONTROLSS_ICLXBAR9_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR9_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR9_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR9_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR9_G1_SEL							
R/W							
0h							

Table 3-2561. CONTROLSS_ICLXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR9_G1_SEL	R/W	0h	ICL XBAR9 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.30 CONTROLSS_ICLXBAR9_G2 Register

3.18.2.30.1 CONTROLSS_ICLXBAR9_G2 Register (Offset = 348h) [reset = 0h]

ICL XBAR 9 Input Select.

Return to Summary Table

Table 3-2562. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4348h

Figure 3-1326. CONTROLSS_ICLXBAR9_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR9_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR9_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR9_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR9_G2_SEL							
R/W							
0h							

Table 3-2563. CONTROLSS_ICLXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR9_G2_SEL	R/W	0h	ICL XBAR9 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.31 CONTROLSS_ICLXBAR10_G0 Register

3.18.2.31.1 CONTROLSS_ICLXBAR10_G0 Register (Offset = 380h) [reset = 0h]

ICL XBAR 10 Input Select.

Return to Summary Table

Table 3-2564. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4380h

Figure 3-1327. CONTROLSS_ICLXBAR10_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR10_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR10_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR10_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR10_G0_SEL							
R/W							
0h							

Table 3-2565. CONTROLSS_ICLXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR10_G0_SEL	R/W	0h	ICL XBAR10 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.32 CONTROLSS_ICLXBAR10_G1 Register

3.18.2.32.1 CONTROLSS_ICLXBAR10_G1 Register (Offset = 384h) [reset = 0h]

ICL XBAR 10 Input Select.

Return to Summary Table

Table 3-2566. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4384h

Figure 3-1328. CONTROLSS_ICLXBAR10_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR10_G1_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ICLXBAR10_G1_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ICLXBAR10_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ICLXBAR10_G1_SEL							
R/W							
0h							

Table 3-2567. CONTROLSS_ICLXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR10_G1_SEL	R/W	0h	ICL XBAR10 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.33 CONTROLSS_ICLXBAR10_G2 Register

3.18.2.33.1 CONTROLSS_ICLXBAR10_G2 Register (Offset = 388h) [reset = 0h]

ICL XBAR 10 Input Select.

Return to Summary Table

Table 3-2568. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4388h

Figure 3-1329. CONTROLSS_ICLXBAR10_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR10_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR10_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR10_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR10_G2_SEL							
R/W							
0h							

Table 3-2569. CONTROLSS_ICLXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR10_G2_SEL	R/W	0h	ICL XBAR10 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.34 CONTROLSS_ICLXBAR11_G0 Register

3.18.2.34.1 CONTROLSS_ICLXBAR11_G0 Register (Offset = 3C0h) [reset = 0h]

ICL XBAR 11 Input Select.

Return to Summary Table

Table 3-2570. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 43C0h

Figure 3-1330. CONTROLSS_ICLXBAR11_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR11_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR11_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR11_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR11_G0_SEL							
R/W							
0h							

Table 3-2571. CONTROLSS_ICLXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR11_G0_SEL	R/W	0h	ICL XBAR11 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.35 CONTROLSS_ICLXBAR11_G1 Register

3.18.2.35.1 CONTROLSS_ICLXBAR11_G1 Register (Offset = 3C4h) [reset = 0h]

ICL XBAR 11 Input Select.

Return to Summary Table

Table 3-2572. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 43C4h

Figure 3-1331. CONTROLSS_ICLXBAR11_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR11_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR11_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR11_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR11_G1_SEL							
R/W							
0h							

Table 3-2573. CONTROLSS_ICLXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR11_G1_SEL	R/W	0h	ICL XBAR11 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.36 CONTROLSS_ICLXBAR11_G2 Register

3.18.2.36.1 CONTROLSS_ICLXBAR11_G2 Register (Offset = 3C8h) [reset = 0h]

ICL XBAR 11 Input Select.

Return to Summary Table

Table 3-2574. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 43C8h

Figure 3-1332. CONTROLSS_ICLXBAR11_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR11_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR11_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR11_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR11_G2_SEL							
R/W							
0h							

Table 3-2575. CONTROLSS_ICLXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR11_G2_SEL	R/W	0h	ICL XBAR11 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.37 CONTROLSS_ICLXBAR12_G0 Register

3.18.2.37.1 CONTROLSS_ICLXBAR12_G0 Register (Offset = 400h) [reset = 0h]

ICL XBAR 12 Input Select.

Return to Summary Table

Table 3-2576. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4400h

Figure 3-1333. CONTROLSS_ICLXBAR12_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR12_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR12_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR12_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR12_G0_SEL							
R/W							
0h							

Table 3-2577. CONTROLSS_ICLXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR12_G0_SEL	R/W	0h	ICL XBAR12 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.38 CONTROLSS_ICLXBAR12_G1 Register

3.18.2.38.1 CONTROLSS_ICLXBAR12_G1 Register (Offset = 404h) [reset = 0h]

ICL XBAR 12 Input Select.

Return to Summary Table

Table 3-2578. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4404h

Figure 3-1334. CONTROLSS_ICLXBAR12_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR12_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR12_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR12_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR12_G1_SEL							
R/W							
0h							

Table 3-2579. CONTROLSS_ICLXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR12_G1_SEL	R/W	0h	ICL XBAR12 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.39 CONTROLSS_ICLXBAR12_G2 Register

3.18.2.39.1 CONTROLSS_ICLXBAR12_G2 Register (Offset = 408h) [reset = 0h]

ICL XBAR 12 Input Select.

Return to Summary Table

Table 3-2580. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4408h

Figure 3-1335. CONTROLSS_ICLXBAR12_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR12_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR12_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR12_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR12_G2_SEL							
R/W							
0h							

Table 3-2581. CONTROLSS_ICLXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR12_G2_SEL	R/W	0h	ICL XBAR12 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.40 CONTROLSS_ICLXBAR13_G0 Register

3.18.2.40.1 CONTROLSS_ICLXBAR13_G0 Register (Offset = 440h) [reset = 0h]

ICL XBAR 13 Input Select.

Return to Summary Table

Table 3-2582. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4440h

Figure 3-1336. CONTROLSS_ICLXBAR13_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR13_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR13_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR13_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR13_G0_SEL							
R/W							
0h							

Table 3-2583. CONTROLSS_ICLXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR13_G0_SEL	R/W	0h	ICL XBAR13 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.41 CONTROLSS_ICLXBAR13_G1 Register

3.18.2.41.1 CONTROLSS_ICLXBAR13_G1 Register (Offset = 444h) [reset = 0h]

ICL XBAR 13 Input Select.

Return to Summary Table

Table 3-2584. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4444h

Figure 3-1337. CONTROLSS_ICLXBAR13_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR13_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR13_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR13_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR13_G1_SEL							
R/W							
0h							

Table 3-2585. CONTROLSS_ICLXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR13_G1_SEL	R/W	0h	ICL XBAR13 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.42 CONTROLSS_ICLXBAR13_G2 Register

3.18.2.42.1 CONTROLSS_ICLXBAR13_G2 Register (Offset = 448h) [reset = 0h]

ICL XBAR 13 Input Select.

Return to Summary Table

Table 3-2586. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4448h

Figure 3-1338. CONTROLSS_ICLXBAR13_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR13_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR13_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR13_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR13_G2_SEL							
R/W							
0h							

Table 3-2587. CONTROLSS_ICLXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR13_G2_SEL	R/W	0h	ICL XBAR13 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.43 CONTROLSS_ICLXBAR14_G0 Register

3.18.2.43.1 CONTROLSS_ICLXBAR14_G0 Register (Offset = 480h) [reset = 0h]

ICL XBAR 14 Input Select.

Return to Summary Table

Table 3-2588. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4480h

Figure 3-1339. CONTROLSS_ICLXBAR14_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR14_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR14_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR14_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR14_G0_SEL							
R/W							
0h							

Table 3-2589. CONTROLSS_ICLXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR14_G0_SEL	R/W	0h	ICL XBAR14 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.44 CONTROLSS_ICLXBAR14_G1 Register

3.18.2.44.1 CONTROLSS_ICLXBAR14_G1 Register (Offset = 484h) [reset = 0h]

ICL XBAR 14 Input Select.

Return to Summary Table

Table 3-2590. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4484h

Figure 3-1340. CONTROLSS_ICLXBAR14_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR14_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR14_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR14_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR14_G1_SEL							
R/W							
0h							

Table 3-2591. CONTROLSS_ICLXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR14_G1_SEL	R/W	0h	ICL XBAR14 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.45 CONTROLSS_ICLXBAR14_G2 Register

3.18.2.45.1 CONTROLSS_ICLXBAR14_G2 Register (Offset = 488h) [reset = 0h]

ICL XBAR 14 Input Select.

Return to Summary Table

Table 3-2592. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4488h

Figure 3-1341. CONTROLSS_ICLXBAR14_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR14_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR14_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR14_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR14_G2_SEL							
R/W							
0h							

Table 3-2593. CONTROLSS_ICLXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR14_G2_SEL	R/W	0h	ICL XBAR14 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.18.2.46 CONTROLSS_ICLXBAR15_G0 Register

3.18.2.46.1 CONTROLSS_ICLXBAR15_G0 Register (Offset = 4C0h) [reset = 0h]

ICL XBAR 15 Input Select .

Return to Summary Table

Table 3-2594. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 44C0h

Figure 3-1342. CONTROLSS_ICLXBAR15_G0 Name Register

31	30	29	28	27	26	25	24
ICLXBAR15_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR15_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR15_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR15_G0_SEL							
R/W							
0h							

Table 3-2595. CONTROLSS_ICLXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR15_G0_SEL	R/W	0h	ICL XBAR15 G0 input bit select. Input source is PWMA hr select 1:PWMA hr bit[x] selected 0:PWMA hr bit[x] is de-selected

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3.18.2.47 CONTROLSS_ICLXBAR15_G1 Register

3.18.2.47.1 CONTROLSS_ICLXBAR15_G1 Register (Offset = 4C4h) [reset = 0h]

ICL XBAR 15 Input Select .

Return to Summary Table

Table 3-2596. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 44C4h

Figure 3-1343. CONTROLSS_ICLXBAR15_G1 Name Register

31	30	29	28	27	26	25	24
ICLXBAR15_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR15_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR15_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR15_G1_SEL							
R/W							
0h							

Table 3-2597. CONTROLSS_ICLXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR15_G1_SEL	R/W	0h	ICL XBAR15 G1 input bit select. Input source is PWMB hr select 1:PWMB hr bit[x] selected 0:PWMB hr bit[x] is de-selected

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3.18.2.48 CONTROLSS_ICLXBAR15_G2 Register

3.18.2.48.1 CONTROLSS_ICLXBAR15_G2 Register (Offset = 4C8h) [reset = 0h]

ICL XBAR 15 Input Select .

Return to Summary Table

Table 3-2598. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 44C8h

Figure 3-1344. CONTROLSS_ICLXBAR15_G2 Name Register

31	30	29	28	27	26	25	24
ICLXBAR15_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
ICLXBAR15_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
ICLXBAR15_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
ICLXBAR15_G2_SEL							
R/W							
0h							

Table 3-2599. CONTROLSS_ICLXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICLXBAR15_G2_SEL	R/W	0h	ICL XBAR15 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.19 CONTROLSS_INTXBAR

CONTROLSS_INTXBAR

3.19.1 CONTROLSS_INTXBAR Summaries

CONTROLSS_INTXBAR Summaries

Table 3-2600. CONTROLSS Registers, Base Address=502D 5000h, Length=2048

Offset	Length	Register Name	CONTROLSS_INTXBAR Physical Address
100h	32	CONTROLSS_INTXBAR0_G0	502D 5100h
104h	32	CONTROLSS_INTXBAR0_G1	502D 5104h
108h	32	CONTROLSS_INTXBAR0_G2	502D 5108h
10Ch	32	CONTROLSS_INTXBAR0_G3	502D 510Ch
110h	32	CONTROLSS_INTXBAR0_G4	502D 5110h
114h	32	CONTROLSS_INTXBAR0_G5	502D 5114h
118h	32	CONTROLSS_INTXBAR0_G6	502D 5118h
11Ch	32	CONTROLSS_INTXBAR0_G7	502D 511Ch
120h	32	CONTROLSS_INTXBAR0_G8	502D 5120h
124h	32	CONTROLSS_INTXBAR0_G9	502D 5124h
140h	32	CONTROLSS_INTXBAR1_G0	502D 5140h
144h	32	CONTROLSS_INTXBAR1_G1	502D 5144h
148h	32	CONTROLSS_INTXBAR1_G2	502D 5148h
14Ch	32	CONTROLSS_INTXBAR1_G3	502D 514Ch
150h	32	CONTROLSS_INTXBAR1_G4	502D 5150h
154h	32	CONTROLSS_INTXBAR1_G5	502D 5154h
158h	32	CONTROLSS_INTXBAR1_G6	502D 5158h
15Ch	32	CONTROLSS_INTXBAR1_G7	502D 515Ch
160h	32	CONTROLSS_INTXBAR1_G8	502D 5160h
164h	32	CONTROLSS_INTXBAR1_G9	502D 5164h
180h	32	CONTROLSS_INTXBAR2_G0	502D 5180h
184h	32	CONTROLSS_INTXBAR2_G1	502D 5184h
188h	32	CONTROLSS_INTXBAR2_G2	502D 5188h
18Ch	32	CONTROLSS_INTXBAR2_G3	502D 518Ch
190h	32	CONTROLSS_INTXBAR2_G4	502D 5190h
194h	32	CONTROLSS_INTXBAR2_G5	502D 5194h
198h	32	CONTROLSS_INTXBAR2_G6	502D 5198h
19Ch	32	CONTROLSS_INTXBAR2_G7	502D 519Ch
1A0h	32	CONTROLSS_INTXBAR2_G8	502D 51A0h
1A4h	32	CONTROLSS_INTXBAR2_G9	502D 51A4h
1C0h	32	CONTROLSS_INTXBAR3_G0	502D 51C0h
1C4h	32	CONTROLSS_INTXBAR3_G1	502D 51C4h
1C8h	32	CONTROLSS_INTXBAR3_G2	502D 51C8h
1CCh	32	CONTROLSS_INTXBAR3_G3	502D 51CCh
1D0h	32	CONTROLSS_INTXBAR3_G4	502D 51D0h
1D4h	32	CONTROLSS_INTXBAR3_G5	502D 51D4h
1D8h	32	CONTROLSS_INTXBAR3_G6	502D 51D8h
1DCh	32	CONTROLSS_INTXBAR3_G7	502D 51DCh
1E0h	32	CONTROLSS_INTXBAR3_G8	502D 51E0h

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Table 3-2600. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)

Offset	Length	Register Name	CONTROLSS_INTXBAR Physical Address
1E4h	32	CONTROLSS_INTXBAR3_G9	502D 51E4h
200h	32	CONTROLSS_INTXBAR4_G0	502D 5200h
204h	32	CONTROLSS_INTXBAR4_G1	502D 5204h
208h	32	CONTROLSS_INTXBAR4_G2	502D 5208h
20Ch	32	CONTROLSS_INTXBAR4_G3	502D 520Ch
210h	32	CONTROLSS_INTXBAR4_G4	502D 5210h
214h	32	CONTROLSS_INTXBAR4_G5	502D 5214h
218h	32	CONTROLSS_INTXBAR4_G6	502D 5218h
21Ch	32	CONTROLSS_INTXBAR4_G7	502D 521Ch
220h	32	CONTROLSS_INTXBAR4_G8	502D 5220h
224h	32	CONTROLSS_INTXBAR4_G9	502D 5224h
240h	32	CONTROLSS_INTXBAR5_G0	502D 5240h
244h	32	CONTROLSS_INTXBAR5_G1	502D 5244h
248h	32	CONTROLSS_INTXBAR5_G2	502D 5248h
24Ch	32	CONTROLSS_INTXBAR5_G3	502D 524Ch
250h	32	CONTROLSS_INTXBAR5_G4	502D 5250h
254h	32	CONTROLSS_INTXBAR5_G5	502D 5254h
258h	32	CONTROLSS_INTXBAR5_G6	502D 5258h
25Ch	32	CONTROLSS_INTXBAR5_G7	502D 525Ch
260h	32	CONTROLSS_INTXBAR5_G8	502D 5260h
264h	32	CONTROLSS_INTXBAR5_G9	502D 5264h
280h	32	CONTROLSS_INTXBAR6_G0	502D 5280h
284h	32	CONTROLSS_INTXBAR6_G1	502D 5284h
288h	32	CONTROLSS_INTXBAR6_G2	502D 5288h
28Ch	32	CONTROLSS_INTXBAR6_G3	502D 528Ch
290h	32	CONTROLSS_INTXBAR6_G4	502D 5290h
294h	32	CONTROLSS_INTXBAR6_G5	502D 5294h
298h	32	CONTROLSS_INTXBAR6_G6	502D 5298h
29Ch	32	CONTROLSS_INTXBAR6_G7	502D 529Ch
2A0h	32	CONTROLSS_INTXBAR6_G8	502D 52A0h
2A4h	32	CONTROLSS_INTXBAR6_G9	502D 52A4h
2C0h	32	CONTROLSS_INTXBAR7_G0	502D 52C0h
2C4h	32	CONTROLSS_INTXBAR7_G1	502D 52C4h
2C8h	32	CONTROLSS_INTXBAR7_G2	502D 52C8h
2CCh	32	CONTROLSS_INTXBAR7_G3	502D 52CCh
2D0h	32	CONTROLSS_INTXBAR7_G4	502D 52D0h
2D4h	32	CONTROLSS_INTXBAR7_G5	502D 52D4h
2D8h	32	CONTROLSS_INTXBAR7_G6	502D 52D8h
2DCh	32	CONTROLSS_INTXBAR7_G7	502D 52DCh
2E0h	32	CONTROLSS_INTXBAR7_G8	502D 52E0h
2E4h	32	CONTROLSS_INTXBAR7_G9	502D 52E4h
300h	32	CONTROLSS_INTXBAR8_G0	502D 5300h
304h	32	CONTROLSS_INTXBAR8_G1	502D 5304h
308h	32	CONTROLSS_INTXBAR8_G2	502D 5308h
30Ch	32	CONTROLSS_INTXBAR8_G3	502D 530Ch
310h	32	CONTROLSS_INTXBAR8_G4	502D 5310h

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Table 3-2600. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)

Offset	Length	Register Name	CONTROLSS_INTXBAR Physical Address
314h	32	CONTROLSS_INTXBAR8_G5	502D 5314h
318h	32	CONTROLSS_INTXBAR8_G6	502D 5318h
31Ch	32	CONTROLSS_INTXBAR8_G7	502D 531Ch
320h	32	CONTROLSS_INTXBAR8_G8	502D 5320h
324h	32	CONTROLSS_INTXBAR8_G9	502D 5324h
340h	32	CONTROLSS_INTXBAR9_G0	502D 5340h
344h	32	CONTROLSS_INTXBAR9_G1	502D 5344h
348h	32	CONTROLSS_INTXBAR9_G2	502D 5348h
34Ch	32	CONTROLSS_INTXBAR9_G3	502D 534Ch
350h	32	CONTROLSS_INTXBAR9_G4	502D 5350h
354h	32	CONTROLSS_INTXBAR9_G5	502D 5354h
358h	32	CONTROLSS_INTXBAR9_G6	502D 5358h
35Ch	32	CONTROLSS_INTXBAR9_G7	502D 535Ch
360h	32	CONTROLSS_INTXBAR9_G8	502D 5360h
364h	32	CONTROLSS_INTXBAR9_G9	502D 5364h
380h	32	CONTROLSS_INTXBAR10_G0	502D 5380h
384h	32	CONTROLSS_INTXBAR10_G1	502D 5384h
388h	32	CONTROLSS_INTXBAR10_G2	502D 5388h
38Ch	32	CONTROLSS_INTXBAR10_G3	502D 538Ch
390h	32	CONTROLSS_INTXBAR10_G4	502D 5390h
394h	32	CONTROLSS_INTXBAR10_G5	502D 5394h
398h	32	CONTROLSS_INTXBAR10_G6	502D 5398h
39Ch	32	CONTROLSS_INTXBAR10_G7	502D 539Ch
3A0h	32	CONTROLSS_INTXBAR10_G8	502D 53A0h
3A4h	32	CONTROLSS_INTXBAR10_G9	502D 53A4h
3C0h	32	CONTROLSS_INTXBAR11_G0	502D 53C0h
3C4h	32	CONTROLSS_INTXBAR11_G1	502D 53C4h
3C8h	32	CONTROLSS_INTXBAR11_G2	502D 53C8h
3CCh	32	CONTROLSS_INTXBAR11_G3	502D 53CCh
3D0h	32	CONTROLSS_INTXBAR11_G4	502D 53D0h
3D4h	32	CONTROLSS_INTXBAR11_G5	502D 53D4h
3D8h	32	CONTROLSS_INTXBAR11_G6	502D 53D8h
3DCh	32	CONTROLSS_INTXBAR11_G7	502D 53DCh
3E0h	32	CONTROLSS_INTXBAR11_G8	502D 53E0h
3E4h	32	CONTROLSS_INTXBAR11_G9	502D 53E4h
400h	32	CONTROLSS_INTXBAR12_G0	502D 5400h
404h	32	CONTROLSS_INTXBAR12_G1	502D 5404h
408h	32	CONTROLSS_INTXBAR12_G2	502D 5408h
40Ch	32	CONTROLSS_INTXBAR12_G3	502D 540Ch
410h	32	CONTROLSS_INTXBAR12_G4	502D 5410h
414h	32	CONTROLSS_INTXBAR12_G5	502D 5414h
418h	32	CONTROLSS_INTXBAR12_G6	502D 5418h
41Ch	32	CONTROLSS_INTXBAR12_G7	502D 541Ch
420h	32	CONTROLSS_INTXBAR12_G8	502D 5420h
424h	32	CONTROLSS_INTXBAR12_G9	502D 5424h
440h	32	CONTROLSS_INTXBAR13_G0	502D 5440h

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Table 3-2600. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)

Offset	Length	Register Name	CONTROLSS_INTXBAR Physical Address
444h	32	CONTROLSS_INTXBAR13_G1	502D 5444h
448h	32	CONTROLSS_INTXBAR13_G2	502D 5448h
44Ch	32	CONTROLSS_INTXBAR13_G3	502D 544Ch
450h	32	CONTROLSS_INTXBAR13_G4	502D 5450h
454h	32	CONTROLSS_INTXBAR13_G5	502D 5454h
458h	32	CONTROLSS_INTXBAR13_G6	502D 5458h
45Ch	32	CONTROLSS_INTXBAR13_G7	502D 545Ch
460h	32	CONTROLSS_INTXBAR13_G8	502D 5460h
464h	32	CONTROLSS_INTXBAR13_G9	502D 5464h
480h	32	CONTROLSS_INTXBAR14_G0	502D 5480h
484h	32	CONTROLSS_INTXBAR14_G1	502D 5484h
488h	32	CONTROLSS_INTXBAR14_G2	502D 5488h
48Ch	32	CONTROLSS_INTXBAR14_G3	502D 548Ch
490h	32	CONTROLSS_INTXBAR14_G4	502D 5490h
494h	32	CONTROLSS_INTXBAR14_G5	502D 5494h
498h	32	CONTROLSS_INTXBAR14_G6	502D 5498h
49Ch	32	CONTROLSS_INTXBAR14_G7	502D 549Ch
4A0h	32	CONTROLSS_INTXBAR14_G8	502D 54A0h
4A4h	32	CONTROLSS_INTXBAR14_G9	502D 54A4h
4C0h	32	CONTROLSS_INTXBAR15_G0	502D 54C0h
4C4h	32	CONTROLSS_INTXBAR15_G1	502D 54C4h
4C8h	32	CONTROLSS_INTXBAR15_G2	502D 54C8h
4CCh	32	CONTROLSS_INTXBAR15_G3	502D 54CCh
4D0h	32	CONTROLSS_INTXBAR15_G4	502D 54D0h
4D4h	32	CONTROLSS_INTXBAR15_G5	502D 54D4h
4D8h	32	CONTROLSS_INTXBAR15_G6	502D 54D8h
4DCh	32	CONTROLSS_INTXBAR15_G7	502D 54DCh
4E0h	32	CONTROLSS_INTXBAR15_G8	502D 54E0h
4E4h	32	CONTROLSS_INTXBAR15_G9	502D 54E4h
500h	32	CONTROLSS_INTXBAR16_G0	502D 5500h
504h	32	CONTROLSS_INTXBAR16_G1	502D 5504h
508h	32	CONTROLSS_INTXBAR16_G2	502D 5508h
50Ch	32	CONTROLSS_INTXBAR16_G3	502D 550Ch
510h	32	CONTROLSS_INTXBAR16_G4	502D 5510h
514h	32	CONTROLSS_INTXBAR16_G5	502D 5514h
518h	32	CONTROLSS_INTXBAR16_G6	502D 5518h
51Ch	32	CONTROLSS_INTXBAR16_G7	502D 551Ch
520h	32	CONTROLSS_INTXBAR16_G8	502D 5520h
524h	32	CONTROLSS_INTXBAR16_G9	502D 5524h
540h	32	CONTROLSS_INTXBAR17_G0	502D 5540h
544h	32	CONTROLSS_INTXBAR17_G1	502D 5544h
548h	32	CONTROLSS_INTXBAR17_G2	502D 5548h
54Ch	32	CONTROLSS_INTXBAR17_G3	502D 554Ch
550h	32	CONTROLSS_INTXBAR17_G4	502D 5550h
554h	32	CONTROLSS_INTXBAR17_G5	502D 5554h
558h	32	CONTROLSS_INTXBAR17_G6	502D 5558h

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Table 3-2600. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)

Offset	Length	Register Name	CONTROLSS_INTXBAR Physical Address
55Ch	32	CONTROLSS_INTXBAR17_G7	502D 555Ch
560h	32	CONTROLSS_INTXBAR17_G8	502D 5560h
564h	32	CONTROLSS_INTXBAR17_G9	502D 5564h
580h	32	CONTROLSS_INTXBAR18_G0	502D 5580h
584h	32	CONTROLSS_INTXBAR18_G1	502D 5584h
588h	32	CONTROLSS_INTXBAR18_G2	502D 5588h
58Ch	32	CONTROLSS_INTXBAR18_G3	502D 558Ch
590h	32	CONTROLSS_INTXBAR18_G4	502D 5590h
594h	32	CONTROLSS_INTXBAR18_G5	502D 5594h
598h	32	CONTROLSS_INTXBAR18_G6	502D 5598h
59Ch	32	CONTROLSS_INTXBAR18_G7	502D 559Ch
5A0h	32	CONTROLSS_INTXBAR18_G8	502D 55A0h
5A4h	32	CONTROLSS_INTXBAR18_G9	502D 55A4h
5C0h	32	CONTROLSS_INTXBAR19_G0	502D 55C0h
5C4h	32	CONTROLSS_INTXBAR19_G1	502D 55C4h
5C8h	32	CONTROLSS_INTXBAR19_G2	502D 55C8h
5CCh	32	CONTROLSS_INTXBAR19_G3	502D 55CCh
5D0h	32	CONTROLSS_INTXBAR19_G4	502D 55D0h
5D4h	32	CONTROLSS_INTXBAR19_G5	502D 55D4h
5D8h	32	CONTROLSS_INTXBAR19_G6	502D 55D8h
5DCh	32	CONTROLSS_INTXBAR19_G7	502D 55DCh
5E0h	32	CONTROLSS_INTXBAR19_G8	502D 55E0h
5E4h	32	CONTROLSS_INTXBAR19_G9	502D 55E4h
600h	32	CONTROLSS_INTXBAR20_G0	502D 5600h
604h	32	CONTROLSS_INTXBAR20_G1	502D 5604h
608h	32	CONTROLSS_INTXBAR20_G2	502D 5608h
60Ch	32	CONTROLSS_INTXBAR20_G3	502D 560Ch
610h	32	CONTROLSS_INTXBAR20_G4	502D 5610h
614h	32	CONTROLSS_INTXBAR20_G5	502D 5614h
618h	32	CONTROLSS_INTXBAR20_G6	502D 5618h
61Ch	32	CONTROLSS_INTXBAR20_G7	502D 561Ch
620h	32	CONTROLSS_INTXBAR20_G8	502D 5620h
624h	32	CONTROLSS_INTXBAR20_G9	502D 5624h
640h	32	CONTROLSS_INTXBAR21_G0	502D 5640h
644h	32	CONTROLSS_INTXBAR21_G1	502D 5644h
648h	32	CONTROLSS_INTXBAR21_G2	502D 5648h
64Ch	32	CONTROLSS_INTXBAR21_G3	502D 564Ch
650h	32	CONTROLSS_INTXBAR21_G4	502D 5650h
654h	32	CONTROLSS_INTXBAR21_G5	502D 5654h
658h	32	CONTROLSS_INTXBAR21_G6	502D 5658h
65Ch	32	CONTROLSS_INTXBAR21_G7	502D 565Ch
660h	32	CONTROLSS_INTXBAR21_G8	502D 5660h
664h	32	CONTROLSS_INTXBAR21_G9	502D 5664h
680h	32	CONTROLSS_INTXBAR22_G0	502D 5680h
684h	32	CONTROLSS_INTXBAR22_G1	502D 5684h
688h	32	CONTROLSS_INTXBAR22_G2	502D 5688h

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Table 3-2600. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)

Offset	Length	Register Name	CONTROLSS_INTXBAR Physical Address
68Ch	32	CONTROLSS_INTXBAR22_G3	502D 568Ch
690h	32	CONTROLSS_INTXBAR22_G4	502D 5690h
694h	32	CONTROLSS_INTXBAR22_G5	502D 5694h
698h	32	CONTROLSS_INTXBAR22_G6	502D 5698h
69Ch	32	CONTROLSS_INTXBAR22_G7	502D 569Ch
6A0h	32	CONTROLSS_INTXBAR22_G8	502D 56A0h
6A4h	32	CONTROLSS_INTXBAR22_G9	502D 56A4h
6C0h	32	CONTROLSS_INTXBAR23_G0	502D 56C0h
6C4h	32	CONTROLSS_INTXBAR23_G1	502D 56C4h
6C8h	32	CONTROLSS_INTXBAR23_G2	502D 56C8h
6CCh	32	CONTROLSS_INTXBAR23_G3	502D 56CCh
6D0h	32	CONTROLSS_INTXBAR23_G4	502D 56D0h
6D4h	32	CONTROLSS_INTXBAR23_G5	502D 56D4h
6D8h	32	CONTROLSS_INTXBAR23_G6	502D 56D8h
6DCh	32	CONTROLSS_INTXBAR23_G7	502D 56DCh
6E0h	32	CONTROLSS_INTXBAR23_G8	502D 56E0h
6E4h	32	CONTROLSS_INTXBAR23_G9	502D 56E4h
700h	32	CONTROLSS_INTXBAR24_G0	502D 5700h
704h	32	CONTROLSS_INTXBAR24_G1	502D 5704h
708h	32	CONTROLSS_INTXBAR24_G2	502D 5708h
70Ch	32	CONTROLSS_INTXBAR24_G3	502D 570Ch
710h	32	CONTROLSS_INTXBAR24_G4	502D 5710h
714h	32	CONTROLSS_INTXBAR24_G5	502D 5714h
718h	32	CONTROLSS_INTXBAR24_G6	502D 5718h
71Ch	32	CONTROLSS_INTXBAR24_G7	502D 571Ch
720h	32	CONTROLSS_INTXBAR24_G8	502D 5720h
724h	32	CONTROLSS_INTXBAR24_G9	502D 5724h
740h	32	CONTROLSS_INTXBAR25_G0	502D 5740h
744h	32	CONTROLSS_INTXBAR25_G1	502D 5744h
748h	32	CONTROLSS_INTXBAR25_G2	502D 5748h
74Ch	32	CONTROLSS_INTXBAR25_G3	502D 574Ch
750h	32	CONTROLSS_INTXBAR25_G4	502D 5750h
754h	32	CONTROLSS_INTXBAR25_G5	502D 5754h
758h	32	CONTROLSS_INTXBAR25_G6	502D 5758h
75Ch	32	CONTROLSS_INTXBAR25_G7	502D 575Ch
760h	32	CONTROLSS_INTXBAR25_G8	502D 5760h
764h	32	CONTROLSS_INTXBAR25_G9	502D 5764h
780h	32	CONTROLSS_INTXBAR26_G0	502D 5780h
784h	32	CONTROLSS_INTXBAR26_G1	502D 5784h
788h	32	CONTROLSS_INTXBAR26_G2	502D 5788h
78Ch	32	CONTROLSS_INTXBAR26_G3	502D 578Ch
790h	32	CONTROLSS_INTXBAR26_G4	502D 5790h
794h	32	CONTROLSS_INTXBAR26_G5	502D 5794h
798h	32	CONTROLSS_INTXBAR26_G6	502D 5798h
79Ch	32	CONTROLSS_INTXBAR26_G7	502D 579Ch
7A0h	32	CONTROLSS_INTXBAR26_G8	502D 57A0h

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Table 3-2600. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)

Offset	Length	Register Name	CONTROLSS_INTXBAR Physical Address
7A4h	32	CONTROLSS_INTXBAR26_G9	502D 57A4h
7C0h	32	CONTROLSS_INTXBAR27_G0	502D 57C0h
7C4h	32	CONTROLSS_INTXBAR27_G1	502D 57C4h
7C8h	32	CONTROLSS_INTXBAR27_G2	502D 57C8h
7CCh	32	CONTROLSS_INTXBAR27_G3	502D 57CCh
7D0h	32	CONTROLSS_INTXBAR27_G4	502D 57D0h
7D4h	32	CONTROLSS_INTXBAR27_G5	502D 57D4h
7D8h	32	CONTROLSS_INTXBAR27_G6	502D 57D8h
7DCh	32	CONTROLSS_INTXBAR27_G7	502D 57DCh
7E0h	32	CONTROLSS_INTXBAR27_G8	502D 57E0h
7E4h	32	CONTROLSS_INTXBAR27_G9	502D 57E4h
800h	32	CONTROLSS_INTXBAR28_G0	502D 5800h
804h	32	CONTROLSS_INTXBAR28_G1	502D 5804h
808h	32	CONTROLSS_INTXBAR28_G2	502D 5808h
80Ch	32	CONTROLSS_INTXBAR28_G3	502D 580Ch
810h	32	CONTROLSS_INTXBAR28_G4	502D 5810h
814h	32	CONTROLSS_INTXBAR28_G5	502D 5814h
818h	32	CONTROLSS_INTXBAR28_G6	502D 5818h
81Ch	32	CONTROLSS_INTXBAR28_G7	502D 581Ch
820h	32	CONTROLSS_INTXBAR28_G8	502D 5820h
824h	32	CONTROLSS_INTXBAR28_G9	502D 5824h
840h	32	CONTROLSS_INTXBAR29_G0	502D 5840h
844h	32	CONTROLSS_INTXBAR29_G1	502D 5844h
848h	32	CONTROLSS_INTXBAR29_G2	502D 5848h
84Ch	32	CONTROLSS_INTXBAR29_G3	502D 584Ch
850h	32	CONTROLSS_INTXBAR29_G4	502D 5850h
854h	32	CONTROLSS_INTXBAR29_G5	502D 5854h
858h	32	CONTROLSS_INTXBAR29_G6	502D 5858h
85Ch	32	CONTROLSS_INTXBAR29_G7	502D 585Ch
860h	32	CONTROLSS_INTXBAR29_G8	502D 5860h
864h	32	CONTROLSS_INTXBAR29_G9	502D 5864h
880h	32	CONTROLSS_INTXBAR30_G0	502D 5880h
884h	32	CONTROLSS_INTXBAR30_G1	502D 5884h
888h	32	CONTROLSS_INTXBAR30_G2	502D 5888h
88Ch	32	CONTROLSS_INTXBAR30_G3	502D 588Ch
890h	32	CONTROLSS_INTXBAR30_G4	502D 5890h
894h	32	CONTROLSS_INTXBAR30_G5	502D 5894h
898h	32	CONTROLSS_INTXBAR30_G6	502D 5898h
89Ch	32	CONTROLSS_INTXBAR30_G7	502D 589Ch
8A0h	32	CONTROLSS_INTXBAR30_G8	502D 58A0h
8A4h	32	CONTROLSS_INTXBAR30_G9	502D 58A4h
8C0h	32	CONTROLSS_INTXBAR31_G0	502D 58C0h
8C4h	32	CONTROLSS_INTXBAR31_G1	502D 58C4h
8C8h	32	CONTROLSS_INTXBAR31_G2	502D 58C8h
8CCh	32	CONTROLSS_INTXBAR31_G3	502D 58CCh
8D0h	32	CONTROLSS_INTXBAR31_G4	502D 58D0h

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Table 3-2600. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)

Offset	Length	Register Name	CONTROLSS_INTXBAR Physical Address
8D4h	32	CONTROLSS_INTXBAR31_G5	502D 58D4h
8D8h	32	CONTROLSS_INTXBAR31_G6	502D 58D8h
8DCh	32	CONTROLSS_INTXBAR31_G7	502D 58DCh
8E0h	32	CONTROLSS_INTXBAR31_G8	502D 58E0h
8E4h	32	CONTROLSS_INTXBAR31_G9	502D 58E4h

3.19.2 CONTROLSS_INTXBAR Registers

CONTROLSS_INTXBAR Registers

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3.19.2.1 CONTROLSS_INTXBAR0_G0 Register

3.19.2.1.1 CONTROLSS_INTXBAR0_G0 Register (Offset = 100h) [reset = 0h]

INT XBAR 0 Input Select.

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Table 3-2601. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5100h

Figure 3-1345. CONTROLSS_INTXBAR0_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR0_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR0_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR0_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR0_G0_SEL							
R/W							
0h							

Table 3-2602. CONTROLSS_INTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR0_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.2 CONTROLSS_INTXBAR0_G1 Register

3.19.2.2.1 CONTROLSS_INTXBAR0_G1 Register (Offset = 104h) [reset = 0h]

INT XBAR 0 Input Select.

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Table 3-2603. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5104h

Figure 3-1346. CONTROLSS_INTXBAR0_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR0_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR0_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR0_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR0_G1_SEL							
R/W							
0h							

Table 3-2604. CONTROLSS_INTXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR0_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.3 CONTROLSS_INTXBAR0_G2 Register

3.19.2.3.1 CONTROLSS_INTXBAR0_G2 Register (Offset = 108h) [reset = 0h]

INT XBAR 0 Input Select.

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Table 3-2605. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5108h

Figure 3-1347. CONTROLSS_INTXBAR0_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR0_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR0_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR0_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR0_G2_SEL							
R/W							
0h							

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Table 3-2606. CONTROLSS_INTXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR0_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.4 CONTROLSS_INTXBAR0_G3 Register

3.19.2.4.1 CONTROLSS_INTXBAR0_G3 Register (Offset = 10Ch) [reset = 0h]

INT XBAR 0 Input Select.

Return to Summary Table

Table 3-2607. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 510Ch

Figure 3-1348. CONTROLSS_INTXBAR0_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR0_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR0_G3_SEL							
R/W							
0h							

Table 3-2608. CONTROLSS_INTXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR0_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.5 CONTROLSS_INTXBAR0_G4 Register

3.19.2.5.1 CONTROLSS_INTXBAR0_G4 Register (Offset = 110h) [reset = 0h]

INT XBAR 0 Input Select.

Return to Summary Table

Table 3-2609. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5110h

Figure 3-1349. CONTROLSS_INTXBAR0_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR0_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR0_G4_SEL							
R/W							
0h							

Table 3-2610. CONTROLSS_INTXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR0_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.6 CONTROLSS_INTXBAR0_G5 Register

3.19.2.6.1 CONTROLSS_INTXBAR0_G5 Register (Offset = 114h) [reset = 0h]

INT XBAR 0 Input Select.

Return to Summary Table

Table 3-2611. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5114h

Figure 3-1350. CONTROLSS_INTXBAR0_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR0_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR0_G5_SEL							
R/W							
0h							

Table 3-2612. CONTROLSS_INTXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR0_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.7 CONTROLSS_INTXBAR0_G6 Register

3.19.2.7.1 CONTROLSS_INTXBAR0_G6 Register (Offset = 118h) [reset = 0h]

INT XBAR 0 Input Select.

Return to Summary Table

Table 3-2613. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5118h

Figure 3-1351. CONTROLSS_INTXBAR0_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					INTXBAR0_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2614. CONTROLSS_INTXBAR0_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR0_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.8 CONTROLSS_INTXBAR0_G7 Register

3.19.2.8.1 CONTROLSS_INTXBAR0_G7 Register (Offset = 11Ch) [reset = 0h]

INT XBAR 0 Input Select.

Return to Summary Table

Table 3-2615. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 511Ch

Figure 3-1352. CONTROLSS_INTXBAR0_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR0_G7_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR0_G7_SEL							
R/W							
0h							

Table 3-2616. CONTROLSS_INTXBAR0_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR0_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.9 CONTROLSS_INTXBAR0_G8 Register

3.19.2.9.1 CONTROLSS_INTXBAR0_G8 Register (Offset = 120h) [reset = 0h]

INT XBAR 0 Input Select.

Return to Summary Table

Table 3-2617. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5120h

Figure 3-1353. CONTROLSS_INTXBAR0_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR0_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR0_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR0_G8_SEL							
R/W							
0h							

Table 3-2618. CONTROLSS_INTXBAR0_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR0_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.10 CONTROLSS_INTXBAR0_G9 Register

3.19.2.10.1 CONTROLSS_INTXBAR0_G9 Register (Offset = 124h) [reset = 0h]

INT XBAR 0 Input Select.

Return to Summary Table

Table 3-2619. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5124h

Figure 3-1354. CONTROLSS_INTXBAR0_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR0_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR0_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR0_G9_SEL							
R/W							
0h							

Table 3-2620. CONTROLSS_INTXBAR0_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR0_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.11 CONTROLSS_INTXBAR1_G0 Register

3.19.2.11.1 CONTROLSS_INTXBAR1_G0 Register (Offset = 140h) [reset = 0h]

INT XBAR 1 Input Select.

Return to Summary Table

Table 3-2621. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5140h

Figure 3-1355. CONTROLSS_INTXBAR1_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR1_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR1_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR1_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR1_G0_SEL							
R/W							
0h							

Table 3-2622. CONTROLSS_INTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR1_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.12 CONTROLSS_INTXBAR1_G1 Register

3.19.2.12.1 CONTROLSS_INTXBAR1_G1 Register (Offset = 144h) [reset = 0h]

INT XBAR 1 Input Select.

Return to Summary Table

Table 3-2623. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5144h

Figure 3-1356. CONTROLSS_INTXBAR1_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR1_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR1_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR1_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR1_G1_SEL							
R/W							
0h							

Table 3-2624. CONTROLSS_INTXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR1_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.13 CONTROLSS_INTXBAR1_G2 Register

3.19.2.13.1 CONTROLSS_INTXBAR1_G2 Register (Offset = 148h) [reset = 0h]

INT XBAR 1 Input Select.

Return to Summary Table

Table 3-2625. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5148h

Figure 3-1357. CONTROLSS_INTXBAR1_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR1_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR1_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR1_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR1_G2_SEL							
R/W							
0h							

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Table 3-2626. CONTROLSS_INTXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR1_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.14 CONTROLSS_INTXBAR1_G3 Register

3.19.2.14.1 CONTROLSS_INTXBAR1_G3 Register (Offset = 14Ch) [reset = 0h]

INT XBAR 1 Input Select.

Return to Summary Table

Table 3-2627. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 514Ch

Figure 3-1358. CONTROLSS_INTXBAR1_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR1_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR1_G3_SEL							
R/W							
0h							

Table 3-2628. CONTROLSS_INTXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR1_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.15 CONTROLSS_INTXBAR1_G4 Register

3.19.2.15.1 CONTROLSS_INTXBAR1_G4 Register (Offset = 150h) [reset = 0h]

INT XBAR 1 Input Select.

Return to Summary Table

Table 3-2629. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5150h

Figure 3-1359. CONTROLSS_INTXBAR1_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR1_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR1_G4_SEL							
R/W							
0h							

Table 3-2630. CONTROLSS_INTXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR1_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.16 CONTROLSS_INTXBAR1_G5 Register

3.19.2.16.1 CONTROLSS_INTXBAR1_G5 Register (Offset = 154h) [reset = 0h]

INT XBAR 1 Input Select.

Return to Summary Table

Table 3-2631. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5154h

Figure 3-1360. CONTROLSS_INTXBAR1_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR1_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR1_G5_SEL							
R/W							
0h							

Table 3-2632. CONTROLSS_INTXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR1_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.17 CONTROLSS_INTXBAR1_G6 Register

3.19.2.17.1 CONTROLSS_INTXBAR1_G6 Register (Offset = 158h) [reset = 0h]

INT XBAR 1 Input Select.

Return to Summary Table

Table 3-2633. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5158h

Figure 3-1361. CONTROLSS_INTXBAR1_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR1_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2634. CONTROLSS_INTXBAR1_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR1_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.18 CONTROLSS_INTXBAR1_G7 Register

3.19.2.18.1 CONTROLSS_INTXBAR1_G7 Register (Offset = 15Ch) [reset = 0h]

INT XBAR 1 Input Select.

Return to Summary Table

Table 3-2635. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 515Ch

Figure 3-1362. CONTROLSS_INTXBAR1_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR1_G7_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR1_G7_SEL							
R/W							
0h							

Table 3-2636. CONTROLSS_INTXBAR1_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR1_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.19 CONTROLSS_INTXBAR1_G8 Register

3.19.2.19.1 CONTROLSS_INTXBAR1_G8 Register (Offset = 160h) [reset = 0h]

INT XBAR 1 Input Select.

Return to Summary Table

Table 3-2637. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5160h

Figure 3-1363. CONTROLSS_INTXBAR1_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR1_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR1_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR1_G8_SEL							
R/W							
0h							

Table 3-2638. CONTROLSS_INTXBAR1_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR1_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.20 CONTROLSS_INTXBAR1_G9 Register

3.19.2.20.1 CONTROLSS_INTXBAR1_G9 Register (Offset = 164h) [reset = 0h]

INT XBAR 1 Input Select.

Return to Summary Table

Table 3-2639. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5164h

Figure 3-1364. CONTROLSS_INTXBAR1_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR1_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR1_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR1_G9_SEL							
R/W							
0h							

Table 3-2640. CONTROLSS_INTXBAR1_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR1_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.21 CONTROLSS_INTXBAR2_G0 Register

3.19.2.21.1 CONTROLSS_INTXBAR2_G0 Register (Offset = 180h) [reset = 0h]

INT XBAR 2 Input Select.

Return to Summary Table

Table 3-2641. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5180h

Figure 3-1365. CONTROLSS_INTXBAR2_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR2_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR2_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR2_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR2_G0_SEL							
R/W							
0h							

Table 3-2642. CONTROLSS_INTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR2_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.22 CONTROLSS_INTXBAR2_G1 Register

3.19.2.22.1 CONTROLSS_INTXBAR2_G1 Register (Offset = 184h) [reset = 0h]

INT XBAR 2 Input Select.

Return to Summary Table

Table 3-2643. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5184h

Figure 3-1366. CONTROLSS_INTXBAR2_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR2_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR2_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR2_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR2_G1_SEL							
R/W							
0h							

Table 3-2644. CONTROLSS_INTXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR2_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.23 CONTROLSS_INTXBAR2_G2 Register

3.19.2.23.1 CONTROLSS_INTXBAR2_G2 Register (Offset = 188h) [reset = 0h]

INT XBAR 2 Input Select.

Return to Summary Table

Table 3-2645. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5188h

Figure 3-1367. CONTROLSS_INTXBAR2_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR2_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR2_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR2_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR2_G2_SEL							
R/W							
0h							

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Table 3-2646. CONTROLSS_INTXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR2_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.24 CONTROLSS_INTXBAR2_G3 Register

3.19.2.24.1 CONTROLSS_INTXBAR2_G3 Register (Offset = 18Ch) [reset = 0h]

INT XBAR 2 Input Select.

Return to Summary Table

Table 3-2647. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 518Ch

Figure 3-1368. CONTROLSS_INTXBAR2_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR2_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR2_G3_SEL							
R/W							
0h							

Table 3-2648. CONTROLSS_INTXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR2_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.25 CONTROLSS_INTXBAR2_G4 Register

3.19.2.25.1 CONTROLSS_INTXBAR2_G4 Register (Offset = 190h) [reset = 0h]

INT XBAR 2 Input Select.

Return to Summary Table

Table 3-2649. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5190h

Figure 3-1369. CONTROLSS_INTXBAR2_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR2_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR2_G4_SEL							
R/W							
0h							

Table 3-2650. CONTROLSS_INTXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR2_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.26 CONTROLSS_INTXBAR2_G5 Register

3.19.2.26.1 CONTROLSS_INTXBAR2_G5 Register (Offset = 194h) [reset = 0h]

INT XBAR 2 Input Select.

Return to Summary Table

Table 3-2651. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5194h

Figure 3-1370. CONTROLSS_INTXBAR2_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR2_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR2_G5_SEL							
R/W							
0h							

Table 3-2652. CONTROLSS_INTXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR2_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.27 CONTROLSS_INTXBAR2_G6 Register

3.19.2.27.1 CONTROLSS_INTXBAR2_G6 Register (Offset = 198h) [reset = 0h]

INT XBAR 2 Input Select.

Return to Summary Table

Table 3-2653. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5198h

Figure 3-1371. CONTROLSS_INTXBAR2_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR2_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2654. CONTROLSS_INTXBAR2_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR2_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.28 CONTROLSS_INTXBAR2_G7 Register

3.19.2.28.1 CONTROLSS_INTXBAR2_G7 Register (Offset = 19Ch) [reset = 0h]

INT XBAR 2 Input Select.

Return to Summary Table

Table 3-2655. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 519Ch

Figure 3-1372. CONTROLSS_INTXBAR2_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR2_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR2_G7_SEL							
R/W							
0h							

Table 3-2656. CONTROLSS_INTXBAR2_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR2_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.29 CONTROLSS_INTXBAR2_G8 Register

3.19.2.29.1 CONTROLSS_INTXBAR2_G8 Register (Offset = 1A0h) [reset = 0h]

INT XBAR 2 Input Select.

Return to Summary Table

Table 3-2657. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51A0h

Figure 3-1373. CONTROLSS_INTXBAR2_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR2_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR2_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR2_G8_SEL							
R/W							
0h							

Table 3-2658. CONTROLSS_INTXBAR2_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR2_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.30 CONTROLSS_INTXBAR2_G9 Register

3.19.2.30.1 CONTROLSS_INTXBAR2_G9 Register (Offset = 1A4h) [reset = 0h]

INT XBAR 2 Input Select.

Return to Summary Table

Table 3-2659. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51A4h

Figure 3-1374. CONTROLSS_INTXBAR2_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR2_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR2_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR2_G9_SEL							
R/W							
0h							

Table 3-2660. CONTROLSS_INTXBAR2_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR2_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.31 CONTROLSS_INTXBAR3_G0 Register

3.19.2.31.1 CONTROLSS_INTXBAR3_G0 Register (Offset = 1C0h) [reset = 0h]

INT XBAR 3 Input Select.

Return to Summary Table

Table 3-2661. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51C0h

Figure 3-1375. CONTROLSS_INTXBAR3_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR3_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR3_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR3_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR3_G0_SEL							
R/W							
0h							

Table 3-2662. CONTROLSS_INTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR3_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.32 CONTROLSS_INTXBAR3_G1 Register

3.19.2.32.1 CONTROLSS_INTXBAR3_G1 Register (Offset = 1C4h) [reset = 0h]

INT XBAR 3 Input Select.

Return to Summary Table

Table 3-2663. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51C4h

Figure 3-1376. CONTROLSS_INTXBAR3_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR3_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR3_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR3_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR3_G1_SEL							
R/W							
0h							

Table 3-2664. CONTROLSS_INTXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR3_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.33 CONTROLSS_INTXBAR3_G2 Register

3.19.2.33.1 CONTROLSS_INTXBAR3_G2 Register (Offset = 1C8h) [reset = 0h]

INT XBAR 3 Input Select.

Return to Summary Table

Table 3-2665. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51C8h

Figure 3-1377. CONTROLSS_INTXBAR3_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR3_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR3_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR3_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR3_G2_SEL							
R/W							
0h							

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Table 3-2666. CONTROLSS_INTXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR3_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.34 CONTROLSS_INTXBAR3_G3 Register

3.19.2.34.1 CONTROLSS_INTXBAR3_G3 Register (Offset = 1CCh) [reset = 0h]

INT XBAR 3 Input Select.

Return to Summary Table

Table 3-2667. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51CCh

Figure 3-1378. CONTROLSS_INTXBAR3_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR3_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR3_G3_SEL							
R/W							
0h							

Table 3-2668. CONTROLSS_INTXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR3_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.35 CONTROLSS_INTXBAR3_G4 Register

3.19.2.35.1 CONTROLSS_INTXBAR3_G4 Register (Offset = 1D0h) [reset = 0h]

INT XBAR 3 Input Select.

Return to Summary Table

Table 3-2669. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51D0h

Figure 3-1379. CONTROLSS_INTXBAR3_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR3_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR3_G4_SEL							
R/W							
0h							

Table 3-2670. CONTROLSS_INTXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR3_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.36 CONTROLSS_INTXBAR3_G5 Register

3.19.2.36.1 CONTROLSS_INTXBAR3_G5 Register (Offset = 1D4h) [reset = 0h]

INT XBAR 3 Input Select.

Return to Summary Table

Table 3-2671. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51D4h

Figure 3-1380. CONTROLSS_INTXBAR3_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR3_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR3_G5_SEL							
R/W							
0h							

Table 3-2672. CONTROLSS_INTXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR3_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.37 CONTROLSS_INTXBAR3_G6 Register

3.19.2.37.1 CONTROLSS_INTXBAR3_G6 Register (Offset = 1D8h) [reset = 0h]

INT XBAR 3 Input Select.

Return to Summary Table

Table 3-2673. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51D8h

Figure 3-1381. CONTROLSS_INTXBAR3_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR3_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2674. CONTROLSS_INTXBAR3_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR3_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.38 CONTROLSS_INTXBAR3_G7 Register

3.19.2.38.1 CONTROLSS_INTXBAR3_G7 Register (Offset = 1DCh) [reset = 0h]

INT XBAR 3 Input Select.

Return to Summary Table

Table 3-2675. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51DCh

Figure 3-1382. CONTROLSS_INTXBAR3_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR3_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR3_G7_SEL							
R/W							
0h							

Table 3-2676. CONTROLSS_INTXBAR3_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR3_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.39 CONTROLSS_INTXBAR3_G8 Register

3.19.2.39.1 CONTROLSS_INTXBAR3_G8 Register (Offset = 1E0h) [reset = 0h]

INT XBAR 3 Input Select.

Return to Summary Table

Table 3-2677. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51E0h

Figure 3-1383. CONTROLSS_INTXBAR3_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR3_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR3_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR3_G8_SEL							
R/W							
0h							

Table 3-2678. CONTROLSS_INTXBAR3_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR3_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.40 CONTROLSS_INTXBAR3_G9 Register

3.19.2.40.1 CONTROLSS_INTXBAR3_G9 Register (Offset = 1E4h) [reset = 0h]

INT XBAR 3 Input Select.

Return to Summary Table

Table 3-2679. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 51E4h

Figure 3-1384. CONTROLSS_INTXBAR3_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR3_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR3_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR3_G9_SEL							
R/W							
0h							

Table 3-2680. CONTROLSS_INTXBAR3_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR3_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.41 CONTROLSS_INTXBAR4_G0 Register

3.19.2.41.1 CONTROLSS_INTXBAR4_G0 Register (Offset = 200h) [reset = 0h]

INT XBAR 4 Input Select.

Return to Summary Table

Table 3-2681. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5200h

Figure 3-1385. CONTROLSS_INTXBAR4_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR4_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR4_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR4_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR4_G0_SEL							
R/W							
0h							

Table 3-2682. CONTROLSS_INTXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR4_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.42 CONTROLSS_INTXBAR4_G1 Register

3.19.2.42.1 CONTROLSS_INTXBAR4_G1 Register (Offset = 204h) [reset = 0h]

INT XBAR 4 Input Select.

Return to Summary Table

Table 3-2683. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5204h

Figure 3-1386. CONTROLSS_INTXBAR4_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR4_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR4_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR4_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR4_G1_SEL							
R/W							
0h							

Table 3-2684. CONTROLSS_INTXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR4_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.43 CONTROLSS_INTXBAR4_G2 Register

3.19.2.43.1 CONTROLSS_INTXBAR4_G2 Register (Offset = 208h) [reset = 0h]

INT XBAR 4 Input Select.

Return to Summary Table

Table 3-2685. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5208h

Figure 3-1387. CONTROLSS_INTXBAR4_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR4_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR4_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR4_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR4_G2_SEL							
R/W							
0h							

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Table 3-2686. CONTROLSS_INTXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR4_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.44 CONTROLSS_INTXBAR4_G3 Register

3.19.2.44.1 CONTROLSS_INTXBAR4_G3 Register (Offset = 20Ch) [reset = 0h]

INT XBAR 4 Input Select.

Return to Summary Table

Table 3-2687. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 520Ch

Figure 3-1388. CONTROLSS_INTXBAR4_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR4_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR4_G3_SEL							
R/W							
0h							

Table 3-2688. CONTROLSS_INTXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR4_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.45 CONTROLSS_INTXBAR4_G4 Register

3.19.2.45.1 CONTROLSS_INTXBAR4_G4 Register (Offset = 210h) [reset = 0h]

INT XBAR 4 Input Select.

Return to Summary Table

Table 3-2689. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5210h

Figure 3-1389. CONTROLSS_INTXBAR4_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR4_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR4_G4_SEL							
R/W							
0h							

Table 3-2690. CONTROLSS_INTXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR4_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.46 CONTROLSS_INTXBAR4_G5 Register

3.19.2.46.1 CONTROLSS_INTXBAR4_G5 Register (Offset = 214h) [reset = 0h]

INT XBAR 4 Input Select.

Return to Summary Table

Table 3-2691. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5214h

Figure 3-1390. CONTROLSS_INTXBAR4_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR4_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR4_G5_SEL							
R/W							
0h							

Table 3-2692. CONTROLSS_INTXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR4_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.47 CONTROLSS_INTXBAR4_G6 Register

3.19.2.47.1 CONTROLSS_INTXBAR4_G6 Register (Offset = 218h) [reset = 0h]

INT XBAR 4 Input Select.

Return to Summary Table

Table 3-2693. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5218h

Figure 3-1391. CONTROLSS_INTXBAR4_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR4_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2694. CONTROLSS_INTXBAR4_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR4_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.48 CONTROLSS_INTXBAR4_G7 Register

3.19.2.48.1 CONTROLSS_INTXBAR4_G7 Register (Offset = 21Ch) [reset = 0h]

INT XBAR 4 Input Select.

Return to Summary Table

Table 3-2695. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 521Ch

Figure 3-1392. CONTROLSS_INTXBAR4_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR4_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR4_G7_SEL							
R/W							
0h							

Table 3-2696. CONTROLSS_INTXBAR4_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR4_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.49 CONTROLSS_INTXBAR4_G8 Register

3.19.2.49.1 CONTROLSS_INTXBAR4_G8 Register (Offset = 220h) [reset = 0h]

INT XBAR 4 Input Select.

Return to Summary Table

Table 3-2697. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5220h

Figure 3-1393. CONTROLSS_INTXBAR4_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR4_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR4_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR4_G8_SEL							
R/W							
0h							

Table 3-2698. CONTROLSS_INTXBAR4_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR4_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.50 CONTROLSS_INTXBAR4_G9 Register

3.19.2.50.1 CONTROLSS_INTXBAR4_G9 Register (Offset = 224h) [reset = 0h]

INT XBAR 4 Input Select.

Return to Summary Table

Table 3-2699. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5224h

Figure 3-1394. CONTROLSS_INTXBAR4_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR4_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR4_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR4_G9_SEL							
R/W							
0h							

Table 3-2700. CONTROLSS_INTXBAR4_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR4_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.51 CONTROLSS_INTXBAR5_G0 Register

3.19.2.51.1 CONTROLSS_INTXBAR5_G0 Register (Offset = 240h) [reset = 0h]

INT XBAR 5 Input Select.

Return to Summary Table

Table 3-2701. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5240h

Figure 3-1395. CONTROLSS_INTXBAR5_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR5_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR5_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR5_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR5_G0_SEL							
R/W							
0h							

Table 3-2702. CONTROLSS_INTXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR5_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.52 CONTROLSS_INTXBAR5_G1 Register

3.19.2.52.1 CONTROLSS_INTXBAR5_G1 Register (Offset = 244h) [reset = 0h]

INT XBAR 5 Input Select.

Return to Summary Table

Table 3-2703. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5244h

Figure 3-1396. CONTROLSS_INTXBAR5_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR5_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR5_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR5_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR5_G1_SEL							
R/W							
0h							

Table 3-2704. CONTROLSS_INTXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR5_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.53 CONTROLSS_INTXBAR5_G2 Register

3.19.2.53.1 CONTROLSS_INTXBAR5_G2 Register (Offset = 248h) [reset = 0h]

INT XBAR 5 Input Select.

Return to Summary Table

Table 3-2705. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5248h

Figure 3-1397. CONTROLSS_INTXBAR5_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR5_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR5_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR5_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR5_G2_SEL							
R/W							
0h							

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Table 3-2706. CONTROLSS_INTXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR5_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.54 CONTROLSS_INTXBAR5_G3 Register

3.19.2.54.1 CONTROLSS_INTXBAR5_G3 Register (Offset = 24Ch) [reset = 0h]

INT XBAR 5 Input Select.

Return to Summary Table

Table 3-2707. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 524Ch

Figure 3-1398. CONTROLSS_INTXBAR5_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR5_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR5_G3_SEL							
R/W							
0h							

Table 3-2708. CONTROLSS_INTXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR5_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.55 CONTROLSS_INTXBAR5_G4 Register

3.19.2.55.1 CONTROLSS_INTXBAR5_G4 Register (Offset = 250h) [reset = 0h]

INT XBAR 5 Input Select.

Return to Summary Table

Table 3-2709. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5250h

Figure 3-1399. CONTROLSS_INTXBAR5_G4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">INTXBAR5_G4_SEL</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">INTXBAR5_G4_SEL</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 3-2710. CONTROLSS_INTXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR5_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.56 CONTROLSS_INTXBAR5_G5 Register

3.19.2.56.1 CONTROLSS_INTXBAR5_G5 Register (Offset = 254h) [reset = 0h]

INT XBAR 5 Input Select.

Return to Summary Table

Table 3-2711. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5254h

Figure 3-1400. CONTROLSS_INTXBAR5_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR5_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR5_G5_SEL							
R/W							
0h							

Table 3-2712. CONTROLSS_INTXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR5_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.57 CONTROLSS_INTXBAR5_G6 Register

3.19.2.57.1 CONTROLSS_INTXBAR5_G6 Register (Offset = 258h) [reset = 0h]

INT XBAR 5 Input Select.

Return to Summary Table

Table 3-2713. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5258h

Figure 3-1401. CONTROLSS_INTXBAR5_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR5_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2714. CONTROLSS_INTXBAR5_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR5_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.58 CONTROLSS_INTXBAR5_G7 Register

3.19.2.58.1 CONTROLSS_INTXBAR5_G7 Register (Offset = 25Ch) [reset = 0h]

INT XBAR 5 Input Select.

Return to Summary Table

Table 3-2715. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 525Ch

Figure 3-1402. CONTROLSS_INTXBAR5_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR5_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR5_G7_SEL							
R/W							
0h							

Table 3-2716. CONTROLSS_INTXBAR5_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR5_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.59 CONTROLSS_INTXBAR5_G8 Register

3.19.2.59.1 CONTROLSS_INTXBAR5_G8 Register (Offset = 260h) [reset = 0h]

INT XBAR 5 Input Select.

Return to Summary Table

Table 3-2717. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5260h

Figure 3-1403. CONTROLSS_INTXBAR5_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR5_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR5_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR5_G8_SEL							
R/W							
0h							

Table 3-2718. CONTROLSS_INTXBAR5_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR5_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.60 CONTROLSS_INTXBAR5_G9 Register

3.19.2.60.1 CONTROLSS_INTXBAR5_G9 Register (Offset = 264h) [reset = 0h]

INT XBAR 5 Input Select.

Return to Summary Table

Table 3-2719. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5264h

Figure 3-1404. CONTROLSS_INTXBAR5_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR5_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR5_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR5_G9_SEL							
R/W							
0h							

Table 3-2720. CONTROLSS_INTXBAR5_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR5_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.61 CONTROLSS_INTXBAR6_G0 Register

3.19.2.61.1 CONTROLSS_INTXBAR6_G0 Register (Offset = 280h) [reset = 0h]

INT XBAR 6 Input Select.

Return to Summary Table

Table 3-2721. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5280h

Figure 3-1405. CONTROLSS_INTXBAR6_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR6_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR6_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR6_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR6_G0_SEL							
R/W							
0h							

Table 3-2722. CONTROLSS_INTXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR6_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.62 CONTROLSS_INTXBAR6_G1 Register

3.19.2.62.1 CONTROLSS_INTXBAR6_G1 Register (Offset = 284h) [reset = 0h]

INT XBAR 6 Input Select.

Return to Summary Table

Table 3-2723. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5284h

Figure 3-1406. CONTROLSS_INTXBAR6_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR6_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR6_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR6_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR6_G1_SEL							
R/W							
0h							

Table 3-2724. CONTROLSS_INTXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR6_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.63 CONTROLSS_INTXBAR6_G2 Register

3.19.2.63.1 CONTROLSS_INTXBAR6_G2 Register (Offset = 288h) [reset = 0h]

INT XBAR 6 Input Select.

Return to Summary Table

Table 3-2725. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5288h

Figure 3-1407. CONTROLSS_INTXBAR6_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR6_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR6_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR6_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR6_G2_SEL							
R/W							
0h							

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Table 3-2726. CONTROLSS_INTXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR6_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.64 CONTROLSS_INTXBAR6_G3 Register

3.19.2.64.1 CONTROLSS_INTXBAR6_G3 Register (Offset = 28Ch) [reset = 0h]

INT XBAR 6 Input Select.

Return to Summary Table

Table 3-2727. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 528Ch

Figure 3-1408. CONTROLSS_INTXBAR6_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR6_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR6_G3_SEL							
R/W							
0h							

Table 3-2728. CONTROLSS_INTXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR6_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.65 CONTROLSS_INTXBAR6_G4 Register

3.19.2.65.1 CONTROLSS_INTXBAR6_G4 Register (Offset = 290h) [reset = 0h]

INT XBAR 6 Input Select.

Return to Summary Table

Table 3-2729. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5290h

Figure 3-1409. CONTROLSS_INTXBAR6_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR6_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR6_G4_SEL							
R/W							
0h							

Table 3-2730. CONTROLSS_INTXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR6_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.66 CONTROLSS_INTXBAR6_G5 Register

3.19.2.66.1 CONTROLSS_INTXBAR6_G5 Register (Offset = 294h) [reset = 0h]

INT XBAR 6 Input Select.

Return to Summary Table

Table 3-2731. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5294h

Figure 3-1410. CONTROLSS_INTXBAR6_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR6_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR6_G5_SEL							
R/W							
0h							

Table 3-2732. CONTROLSS_INTXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR6_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.67 CONTROLSS_INTXBAR6_G6 Register

3.19.2.67.1 CONTROLSS_INTXBAR6_G6 Register (Offset = 298h) [reset = 0h]

INT XBAR 6 Input Select.

Return to Summary Table

Table 3-2733. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5298h

Figure 3-1411. CONTROLSS_INTXBAR6_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR6_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2734. CONTROLSS_INTXBAR6_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR6_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.68 CONTROLSS_INTXBAR6_G7 Register

3.19.2.68.1 CONTROLSS_INTXBAR6_G7 Register (Offset = 29Ch) [reset = 0h]

INT XBAR 6 Input Select.

Return to Summary Table

Table 3-2735. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 529Ch

Figure 3-1412. CONTROLSS_INTXBAR6_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR6_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR6_G7_SEL							
R/W							
0h							

Table 3-2736. CONTROLSS_INTXBAR6_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR6_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.69 CONTROLSS_INTXBAR6_G8 Register

3.19.2.69.1 CONTROLSS_INTXBAR6_G8 Register (Offset = 2A0h) [reset = 0h]

INT XBAR 6 Input Select.

Return to Summary Table

Table 3-2737. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52A0h

Figure 3-1413. CONTROLSS_INTXBAR6_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR6_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR6_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR6_G8_SEL							
R/W							
0h							

Table 3-2738. CONTROLSS_INTXBAR6_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR6_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.70 CONTROLSS_INTXBAR6_G9 Register

3.19.2.70.1 CONTROLSS_INTXBAR6_G9 Register (Offset = 2A4h) [reset = 0h]

INT XBAR 6 Input Select.

Return to Summary Table

Table 3-2739. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52A4h

Figure 3-1414. CONTROLSS_INTXBAR6_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR6_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR6_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR6_G9_SEL							
R/W							
0h							

Table 3-2740. CONTROLSS_INTXBAR6_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR6_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.71 CONTROLSS_INTXBAR7_G0 Register

3.19.2.71.1 CONTROLSS_INTXBAR7_G0 Register (Offset = 2C0h) [reset = 0h]

INT XBAR 7 Input Select.

Return to Summary Table

Table 3-2741. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52C0h

Figure 3-1415. CONTROLSS_INTXBAR7_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR7_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR7_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR7_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR7_G0_SEL							
R/W							
0h							

Table 3-2742. CONTROLSS_INTXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR7_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.72 CONTROLSS_INTXBAR7_G1 Register

3.19.2.72.1 CONTROLSS_INTXBAR7_G1 Register (Offset = 2C4h) [reset = 0h]

INT XBAR 7 Input Select.

Return to Summary Table

Table 3-2743. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52C4h

Figure 3-1416. CONTROLSS_INTXBAR7_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR7_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR7_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR7_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR7_G1_SEL							
R/W							
0h							

Table 3-2744. CONTROLSS_INTXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR7_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.73 CONTROLSS_INTXBAR7_G2 Register

3.19.2.73.1 CONTROLSS_INTXBAR7_G2 Register (Offset = 2C8h) [reset = 0h]

INT XBAR 7 Input Select.

Return to Summary Table

Table 3-2745. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52C8h

Figure 3-1417. CONTROLSS_INTXBAR7_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR7_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR7_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR7_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR7_G2_SEL							
R/W							
0h							

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Table 3-2746. CONTROLSS_INTXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR7_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.74 CONTROLSS_INTXBAR7_G3 Register

3.19.2.74.1 CONTROLSS_INTXBAR7_G3 Register (Offset = 2CCh) [reset = 0h]

INT XBAR 7 Input Select.

Return to Summary Table

Table 3-2747. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52CCh

Figure 3-1418. CONTROLSS_INTXBAR7_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR7_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR7_G3_SEL							
R/W							
0h							

Table 3-2748. CONTROLSS_INTXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR7_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.75 CONTROLSS_INTXBAR7_G4 Register

3.19.2.75.1 CONTROLSS_INTXBAR7_G4 Register (Offset = 2D0h) [reset = 0h]

INT XBAR 7 Input Select.

Return to Summary Table

Table 3-2749. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52D0h

Figure 3-1419. CONTROLSS_INTXBAR7_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR7_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR7_G4_SEL							
R/W							
0h							

Table 3-2750. CONTROLSS_INTXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR7_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.76 CONTROLSS_INTXBAR7_G5 Register

3.19.2.76.1 CONTROLSS_INTXBAR7_G5 Register (Offset = 2D4h) [reset = 0h]

INT XBAR 7 Input Select.

Return to Summary Table

Table 3-2751. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52D4h

Figure 3-1420. CONTROLSS_INTXBAR7_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR7_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR7_G5_SEL							
R/W							
0h							

Table 3-2752. CONTROLSS_INTXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR7_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.77 CONTROLSS_INTXBAR7_G6 Register

3.19.2.77.1 CONTROLSS_INTXBAR7_G6 Register (Offset = 2D8h) [reset = 0h]

INT XBAR 7 Input Select.

Return to Summary Table

Table 3-2753. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52D8h

Figure 3-1421. CONTROLSS_INTXBAR7_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR7_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2754. CONTROLSS_INTXBAR7_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR7_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.78 CONTROLSS_INTXBAR7_G7 Register

3.19.2.78.1 CONTROLSS_INTXBAR7_G7 Register (Offset = 2DCh) [reset = 0h]

INT XBAR 7 Input Select.

Return to Summary Table

Table 3-2755. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52DCh

Figure 3-1422. CONTROLSS_INTXBAR7_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR7_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR7_G7_SEL							
R/W							
0h							

Table 3-2756. CONTROLSS_INTXBAR7_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR7_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.79 CONTROLSS_INTXBAR7_G8 Register

3.19.2.79.1 CONTROLSS_INTXBAR7_G8 Register (Offset = 2E0h) [reset = 0h]

INT XBAR 7 Input Select.

Return to Summary Table

Table 3-2757. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52E0h

Figure 3-1423. CONTROLSS_INTXBAR7_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR7_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR7_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR7_G8_SEL							
R/W							
0h							

Table 3-2758. CONTROLSS_INTXBAR7_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR7_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.80 CONTROLSS_INTXBAR7_G9 Register

3.19.2.80.1 CONTROLSS_INTXBAR7_G9 Register (Offset = 2E4h) [reset = 0h]

INT XBAR 7 Input Select.

Return to Summary Table

Table 3-2759. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 52E4h

Figure 3-1424. CONTROLSS_INTXBAR7_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR7_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR7_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR7_G9_SEL							
R/W							
0h							

Table 3-2760. CONTROLSS_INTXBAR7_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR7_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.81 CONTROLSS_INTXBAR8_G0 Register

3.19.2.81.1 CONTROLSS_INTXBAR8_G0 Register (Offset = 300h) [reset = 0h]

INT XBAR 8 Input Select.

Return to Summary Table

Table 3-2761. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5300h

Figure 3-1425. CONTROLSS_INTXBAR8_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR8_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR8_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR8_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR8_G0_SEL							
R/W							
0h							

Table 3-2762. CONTROLSS_INTXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR8_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.82 CONTROLSS_INTXBAR8_G1 Register

3.19.2.82.1 CONTROLSS_INTXBAR8_G1 Register (Offset = 304h) [reset = 0h]

INT XBAR 8 Input Select.

Return to Summary Table

Table 3-2763. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5304h

Figure 3-1426. CONTROLSS_INTXBAR8_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR8_G1_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTXBAR8_G1_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR8_G1_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR8_G1_SEL							
R/W							
0h							

Table 3-2764. CONTROLSS_INTXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR8_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.83 CONTROLSS_INTXBAR8_G2 Register

3.19.2.83.1 CONTROLSS_INTXBAR8_G2 Register (Offset = 308h) [reset = 0h]

INT XBAR 8 Input Select.

Return to Summary Table

Table 3-2765. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5308h

Figure 3-1427. CONTROLSS_INTXBAR8_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR8_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR8_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR8_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR8_G2_SEL							
R/W							
0h							

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Table 3-2766. CONTROLSS_INTXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR8_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.84 CONTROLSS_INTXBAR8_G3 Register

3.19.2.84.1 CONTROLSS_INTXBAR8_G3 Register (Offset = 30Ch) [reset = 0h]

INT XBAR 8 Input Select.

Return to Summary Table

Table 3-2767. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 530Ch

Figure 3-1428. CONTROLSS_INTXBAR8_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR8_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR8_G3_SEL							
R/W							
0h							

Table 3-2768. CONTROLSS_INTXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR8_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.85 CONTROLSS_INTXBAR8_G4 Register

3.19.2.85.1 CONTROLSS_INTXBAR8_G4 Register (Offset = 310h) [reset = 0h]

INT XBAR 8 Input Select.

Return to Summary Table

Table 3-2769. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5310h

Figure 3-1429. CONTROLSS_INTXBAR8_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR8_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR8_G4_SEL							
R/W							
0h							

Table 3-2770. CONTROLSS_INTXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR8_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.86 CONTROLSS_INTXBAR8_G5 Register

3.19.2.86.1 CONTROLSS_INTXBAR8_G5 Register (Offset = 314h) [reset = 0h]

INT XBAR 8 Input Select.

Return to Summary Table

Table 3-2771. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5314h

Figure 3-1430. CONTROLSS_INTXBAR8_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR8_G5_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR8_G5_SEL							
R/W							
0h							

Table 3-2772. CONTROLSS_INTXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR8_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.87 CONTROLSS_INTXBAR8_G6 Register

3.19.2.87.1 CONTROLSS_INTXBAR8_G6 Register (Offset = 318h) [reset = 0h]

INT XBAR 8 Input Select.

Return to Summary Table

Table 3-2773. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5318h

Figure 3-1431. CONTROLSS_INTXBAR8_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					INTXBAR8_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2774. CONTROLSS_INTXBAR8_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR8_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.88 CONTROLSS_INTXBAR8_G7 Register

3.19.2.88.1 CONTROLSS_INTXBAR8_G7 Register (Offset = 31Ch) [reset = 0h]

INT XBAR 8 Input Select.

Return to Summary Table

Table 3-2775. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 531Ch

Figure 3-1432. CONTROLSS_INTXBAR8_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR8_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR8_G7_SEL							
R/W							
0h							

Table 3-2776. CONTROLSS_INTXBAR8_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR8_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.89 CONTROLSS_INTXBAR8_G8 Register

3.19.2.89.1 CONTROLSS_INTXBAR8_G8 Register (Offset = 320h) [reset = 0h]

INT XBAR 8 Input Select.

Return to Summary Table

Table 3-2777. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5320h

Figure 3-1433. CONTROLSS_INTXBAR8_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR8_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR8_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR8_G8_SEL							
R/W							
0h							

Table 3-2778. CONTROLSS_INTXBAR8_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR8_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.90 CONTROLSS_INTXBAR8_G9 Register

3.19.2.90.1 CONTROLSS_INTXBAR8_G9 Register (Offset = 324h) [reset = 0h]

INT XBAR 8 Input Select.

Return to Summary Table

Table 3-2779. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5324h

Figure 3-1434. CONTROLSS_INTXBAR8_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR8_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR8_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR8_G9_SEL							
R/W							
0h							

Table 3-2780. CONTROLSS_INTXBAR8_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR8_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.91 CONTROLSS_INTXBAR9_G0 Register

3.19.2.91.1 CONTROLSS_INTXBAR9_G0 Register (Offset = 340h) [reset = 0h]

INT XBAR 9 Input Select.

Return to Summary Table

Table 3-2781. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5340h

Figure 3-1435. CONTROLSS_INTXBAR9_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR9_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR9_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR9_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR9_G0_SEL							
R/W							
0h							

Table 3-2782. CONTROLSS_INTXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR9_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.92 CONTROLSS_INTXBAR9_G1 Register

3.19.2.92.1 CONTROLSS_INTXBAR9_G1 Register (Offset = 344h) [reset = 0h]

INT XBAR 9 Input Select.

Return to Summary Table

Table 3-2783. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5344h

Figure 3-1436. CONTROLSS_INTXBAR9_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR9_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR9_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR9_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR9_G1_SEL							
R/W							
0h							

Table 3-2784. CONTROLSS_INTXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR9_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.93 CONTROLSS_INTXBAR9_G2 Register

3.19.2.93.1 CONTROLSS_INTXBAR9_G2 Register (Offset = 348h) [reset = 0h]

INT XBAR 9 Input Select.

Return to Summary Table

Table 3-2785. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5348h

Figure 3-1437. CONTROLSS_INTXBAR9_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR9_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR9_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR9_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR9_G2_SEL							
R/W							
0h							

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Table 3-2786. CONTROLSS_INTXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR9_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.94 CONTROLSS_INTXBAR9_G3 Register

3.19.2.94.1 CONTROLSS_INTXBAR9_G3 Register (Offset = 34Ch) [reset = 0h]

INT XBAR 9 Input Select.

Return to Summary Table

Table 3-2787. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 534Ch

Figure 3-1438. CONTROLSS_INTXBAR9_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR9_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR9_G3_SEL							
R/W							
0h							

Table 3-2788. CONTROLSS_INTXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR9_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.95 CONTROLSS_INTXBAR9_G4 Register

3.19.2.95.1 CONTROLSS_INTXBAR9_G4 Register (Offset = 350h) [reset = 0h]

INT XBAR 9 Input Select.

Return to Summary Table

Table 3-2789. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5350h

Figure 3-1439. CONTROLSS_INTXBAR9_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR9_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR9_G4_SEL							
R/W							
0h							

Table 3-2790. CONTROLSS_INTXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR9_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.96 CONTROLSS_INTXBAR9_G5 Register

3.19.2.96.1 CONTROLSS_INTXBAR9_G5 Register (Offset = 354h) [reset = 0h]

INT XBAR 9 Input Select.

Return to Summary Table

Table 3-2791. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5354h

Figure 3-1440. CONTROLSS_INTXBAR9_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR9_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR9_G5_SEL							
R/W							
0h							

Table 3-2792. CONTROLSS_INTXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR9_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.97 CONTROLSS_INTXBAR9_G6 Register

3.19.2.97.1 CONTROLSS_INTXBAR9_G6 Register (Offset = 358h) [reset = 0h]

INT XBAR 9 Input Select.

Return to Summary Table

Table 3-2793. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5358h

Figure 3-1441. CONTROLSS_INTXBAR9_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					INTXBAR9_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2794. CONTROLSS_INTXBAR9_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR9_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.98 CONTROLSS_INTXBAR9_G7 Register

3.19.2.98.1 CONTROLSS_INTXBAR9_G7 Register (Offset = 35Ch) [reset = 0h]

INT XBAR 9 Input Select.

Return to Summary Table

Table 3-2795. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 535Ch

Figure 3-1442. CONTROLSS_INTXBAR9_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR9_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR9_G7_SEL							
R/W							
0h							

Table 3-2796. CONTROLSS_INTXBAR9_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR9_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.99 CONTROLSS_INTXBAR9_G8 Register

3.19.2.99.1 CONTROLSS_INTXBAR9_G8 Register (Offset = 360h) [reset = 0h]

INT XBAR 9 Input Select.

Return to Summary Table

Table 3-2797. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5360h

Figure 3-1443. CONTROLSS_INTXBAR9_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR9_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR9_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR9_G8_SEL							
R/W							
0h							

Table 3-2798. CONTROLSS_INTXBAR9_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR9_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.100 CONTROLSS_INTXBAR9_G9 Register

3.19.2.100.1 CONTROLSS_INTXBAR9_G9 Register (Offset = 364h) [reset = 0h]

INT XBAR 9 Input Select.

Return to Summary Table

Table 3-2799. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5364h

Figure 3-1444. CONTROLSS_INTXBAR9_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR9_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR9_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR9_G9_SEL							
R/W							
0h							

Table 3-2800. CONTROLSS_INTXBAR9_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR9_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.101 CONTROLSS_INTXBAR10_G0 Register

3.19.2.101.1 CONTROLSS_INTXBAR10_G0 Register (Offset = 380h) [reset = 0h]

INT XBAR 10 Input Select.

Return to Summary Table

Table 3-2801. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5380h

Figure 3-1445. CONTROLSS_INTXBAR10_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR10_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR10_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR10_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR10_G0_SEL							
R/W							
0h							

Table 3-2802. CONTROLSS_INTXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR10_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.102 CONTROLSS_INTXBAR10_G1 Register

3.19.2.102.1 CONTROLSS_INTXBAR10_G1 Register (Offset = 384h) [reset = 0h]

INT XBAR 10 Input Select.

Return to Summary Table

Table 3-2803. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5384h

Figure 3-1446. CONTROLSS_INTXBAR10_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR10_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR10_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR10_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR10_G1_SEL							
R/W							
0h							

Table 3-2804. CONTROLSS_INTXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR10_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.103 CONTROLSS_INTXBAR10_G2 Register

3.19.2.103.1 CONTROLSS_INTXBAR10_G2 Register (Offset = 388h) [reset = 0h]

INT XBAR 10 Input Select.

Return to Summary Table

Table 3-2805. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5388h

Figure 3-1447. CONTROLSS_INTXBAR10_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR10_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR10_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR10_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR10_G2_SEL							
R/W							
0h							

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Table 3-2806. CONTROLSS_INTXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR10_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.104 CONTROLSS_INTXBAR10_G3 Register

3.19.2.104.1 CONTROLSS_INTXBAR10_G3 Register (Offset = 38Ch) [reset = 0h]

INT XBAR 10 Input Select.

Return to Summary Table

Table 3-2807. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 538Ch

Figure 3-1448. CONTROLSS_INTXBAR10_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR10_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR10_G3_SEL							
R/W							
0h							

Table 3-2808. CONTROLSS_INTXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR10_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.105 CONTROLSS_INTXBAR10_G4 Register

3.19.2.105.1 CONTROLSS_INTXBAR10_G4 Register (Offset = 390h) [reset = 0h]

INT XBAR 10 Input Select.

Return to Summary Table

Table 3-2809. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5390h

Figure 3-1449. CONTROLSS_INTXBAR10_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR10_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR10_G4_SEL							
R/W							
0h							

Table 3-2810. CONTROLSS_INTXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR10_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.106 CONTROLSS_INTXBAR10_G5 Register

3.19.2.106.1 CONTROLSS_INTXBAR10_G5 Register (Offset = 394h) [reset = 0h]

INT XBAR 10 Input Select.

Return to Summary Table

Table 3-2811. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5394h

Figure 3-1450. CONTROLSS_INTXBAR10_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR10_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR10_G5_SEL							
R/W							
0h							

Table 3-2812. CONTROLSS_INTXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR10_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.107 CONTROLSS_INTXBAR10_G6 Register

3.19.2.107.1 CONTROLSS_INTXBAR10_G6 Register (Offset = 398h) [reset = 0h]

INT XBAR 10 Input Select.

Return to Summary Table

Table 3-2813. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5398h

Figure 3-1451. CONTROLSS_INTXBAR10_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					INTXBAR10_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2814. CONTROLSS_INTXBAR10_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR10_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.108 CONTROLSS_INTXBAR10_G7 Register

3.19.2.108.1 CONTROLSS_INTXBAR10_G7 Register (Offset = 39Ch) [reset = 0h]

INT XBAR 10 Input Select.

Return to Summary Table

Table 3-2815. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 539Ch

Figure 3-1452. CONTROLSS_INTXBAR10_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR10_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR10_G7_SEL							
R/W							
0h							

Table 3-2816. CONTROLSS_INTXBAR10_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR10_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.109 CONTROLSS_INTXBAR10_G8 Register

3.19.2.109.1 CONTROLSS_INTXBAR10_G8 Register (Offset = 3A0h) [reset = 0h]

INT XBAR 10 Input Select.

Return to Summary Table

Table 3-2817. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53A0h

Figure 3-1453. CONTROLSS_INTXBAR10_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR10_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR10_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR10_G8_SEL							
R/W							
0h							

Table 3-2818. CONTROLSS_INTXBAR10_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR10_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.110 CONTROLSS_INTXBAR10_G9 Register

3.19.2.110.1 CONTROLSS_INTXBAR10_G9 Register (Offset = 3A4h) [reset = 0h]

INT XBAR 10 Input Select.

Return to Summary Table

Table 3-2819. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53A4h

Figure 3-1454. CONTROLSS_INTXBAR10_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR10_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR10_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR10_G9_SEL							
R/W							
0h							

Table 3-2820. CONTROLSS_INTXBAR10_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR10_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.111 CONTROLSS_INTXBAR11_G0 Register

3.19.2.111.1 CONTROLSS_INTXBAR11_G0 Register (Offset = 3C0h) [reset = 0h]

INT XBAR 11 Input Select.

Return to Summary Table

Table 3-2821. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53C0h

Figure 3-1455. CONTROLSS_INTXBAR11_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR11_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR11_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR11_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR11_G0_SEL							
R/W							
0h							

Table 3-2822. CONTROLSS_INTXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR11_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.112 CONTROLSS_INTXBAR11_G1 Register

3.19.2.112.1 CONTROLSS_INTXBAR11_G1 Register (Offset = 3C4h) [reset = 0h]

INT XBAR 11 Input Select.

Return to Summary Table

Table 3-2823. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53C4h

Figure 3-1456. CONTROLSS_INTXBAR11_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR11_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR11_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR11_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR11_G1_SEL							
R/W							
0h							

Table 3-2824. CONTROLSS_INTXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR11_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.113 CONTROLSS_INTXBAR11_G2 Register

3.19.2.113.1 CONTROLSS_INTXBAR11_G2 Register (Offset = 3C8h) [reset = 0h]

INT XBAR 11 Input Select.

Return to Summary Table

Table 3-2825. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53C8h

Figure 3-1457. CONTROLSS_INTXBAR11_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR11_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR11_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR11_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR11_G2_SEL							
R/W							
0h							

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Table 3-2826. CONTROLSS_INTXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR11_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.114 CONTROLSS_INTXBAR11_G3 Register

3.19.2.114.1 CONTROLSS_INTXBAR11_G3 Register (Offset = 3CCh) [reset = 0h]

INT XBAR 11 Input Select.

Return to Summary Table

Table 3-2827. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53CCh

Figure 3-1458. CONTROLSS_INTXBAR11_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR11_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR11_G3_SEL							
R/W							
0h							

Table 3-2828. CONTROLSS_INTXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR11_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.115 CONTROLSS_INTXBAR11_G4 Register

3.19.2.115.1 CONTROLSS_INTXBAR11_G4 Register (Offset = 3D0h) [reset = 0h]

INT XBAR 11 Input Select.

Return to Summary Table

Table 3-2829. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53D0h

Figure 3-1459. CONTROLSS_INTXBAR11_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR11_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR11_G4_SEL							
R/W							
0h							

Table 3-2830. CONTROLSS_INTXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR11_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.116 CONTROLSS_INTXBAR11_G5 Register

3.19.2.116.1 CONTROLSS_INTXBAR11_G5 Register (Offset = 3D4h) [reset = 0h]

INT XBAR 11 Input Select.

Return to Summary Table

Table 3-2831. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53D4h

Figure 3-1460. CONTROLSS_INTXBAR11_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR11_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR11_G5_SEL							
R/W							
0h							

Table 3-2832. CONTROLSS_INTXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR11_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.117 CONTROLSS_INTXBAR11_G6 Register

3.19.2.117.1 CONTROLSS_INTXBAR11_G6 Register (Offset = 3D8h) [reset = 0h]

INT XBAR 11 Input Select.

Return to Summary Table

Table 3-2833. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53D8h

Figure 3-1461. CONTROLSS_INTXBAR11_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR11_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2834. CONTROLSS_INTXBAR11_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR11_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.118 CONTROLSS_INTXBAR11_G7 Register

3.19.2.118.1 CONTROLSS_INTXBAR11_G7 Register (Offset = 3DCh) [reset = 0h]

INT XBAR 11 Input Select.

Return to Summary Table

Table 3-2835. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53DCh

Figure 3-1462. CONTROLSS_INTXBAR11_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR11_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR11_G7_SEL							
R/W							
0h							

Table 3-2836. CONTROLSS_INTXBAR11_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR11_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.119 CONTROLSS_INTXBAR11_G8 Register

3.19.2.119.1 CONTROLSS_INTXBAR11_G8 Register (Offset = 3E0h) [reset = 0h]

INT XBAR 11 Input Select.

Return to Summary Table

Table 3-2837. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53E0h

Figure 3-1463. CONTROLSS_INTXBAR11_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR11_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR11_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR11_G8_SEL							
R/W							
0h							

Table 3-2838. CONTROLSS_INTXBAR11_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR11_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.120 CONTROLSS_INTXBAR11_G9 Register

3.19.2.120.1 CONTROLSS_INTXBAR11_G9 Register (Offset = 3E4h) [reset = 0h]

INT XBAR 11 Input Select.

Return to Summary Table

Table 3-2839. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 53E4h

Figure 3-1464. CONTROLSS_INTXBAR11_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR11_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR11_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR11_G9_SEL							
R/W							
0h							

Table 3-2840. CONTROLSS_INTXBAR11_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR11_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.121 CONTROLSS_INTXBAR12_G0 Register

3.19.2.121.1 CONTROLSS_INTXBAR12_G0 Register (Offset = 400h) [reset = 0h]

INT XBAR 12 Input Select.

Return to Summary Table

Table 3-2841. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5400h

Figure 3-1465. CONTROLSS_INTXBAR12_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR12_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR12_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR12_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR12_G0_SEL							
R/W							
0h							

Table 3-2842. CONTROLSS_INTXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR12_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.122 CONTROLSS_INTXBAR12_G1 Register

3.19.2.122.1 CONTROLSS_INTXBAR12_G1 Register (Offset = 404h) [reset = 0h]

INT XBAR 12 Input Select.

Return to Summary Table

Table 3-2843. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5404h

Figure 3-1466. CONTROLSS_INTXBAR12_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR12_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR12_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR12_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR12_G1_SEL							
R/W							
0h							

Table 3-2844. CONTROLSS_INTXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR12_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.123 CONTROLSS_INTXBAR12_G2 Register

3.19.2.123.1 CONTROLSS_INTXBAR12_G2 Register (Offset = 408h) [reset = 0h]

INT XBAR 12 Input Select.

Return to Summary Table

Table 3-2845. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5408h

Figure 3-1467. CONTROLSS_INTXBAR12_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR12_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR12_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR12_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR12_G2_SEL							
R/W							
0h							

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Table 3-2846. CONTROLSS_INTXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR12_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.124 CONTROLSS_INTXBAR12_G3 Register

3.19.2.124.1 CONTROLSS_INTXBAR12_G3 Register (Offset = 40Ch) [reset = 0h]

INT XBAR 12 Input Select.

Return to Summary Table

Table 3-2847. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 540Ch

Figure 3-1468. CONTROLSS_INTXBAR12_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR12_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR12_G3_SEL							
R/W							
0h							

Table 3-2848. CONTROLSS_INTXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR12_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.125 CONTROLSS_INTXBAR12_G4 Register

3.19.2.125.1 CONTROLSS_INTXBAR12_G4 Register (Offset = 410h) [reset = 0h]

INT XBAR 12 Input Select.

Return to Summary Table

Table 3-2849. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5410h

Figure 3-1469. CONTROLSS_INTXBAR12_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR12_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR12_G4_SEL							
R/W							
0h							

Table 3-2850. CONTROLSS_INTXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR12_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.126 CONTROLSS_INTXBAR12_G5 Register

3.19.2.126.1 CONTROLSS_INTXBAR12_G5 Register (Offset = 414h) [reset = 0h]

INT XBAR 12 Input Select.

Return to Summary Table

Table 3-2851. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5414h

Figure 3-1470. CONTROLSS_INTXBAR12_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR12_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR12_G5_SEL							
R/W							
0h							

Table 3-2852. CONTROLSS_INTXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR12_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.127 CONTROLSS_INTXBAR12_G6 Register

3.19.2.127.1 CONTROLSS_INTXBAR12_G6 Register (Offset = 418h) [reset = 0h]

INT XBAR 12 Input Select.

Return to Summary Table

Table 3-2853. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5418h

Figure 3-1471. CONTROLSS_INTXBAR12_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR12_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2854. CONTROLSS_INTXBAR12_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR12_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.128 CONTROLSS_INTXBAR12_G7 Register

3.19.2.128.1 CONTROLSS_INTXBAR12_G7 Register (Offset = 41Ch) [reset = 0h]

INT XBAR 12 Input Select.

Return to Summary Table

Table 3-2855. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 541Ch

Figure 3-1472. CONTROLSS_INTXBAR12_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR12_G7_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR12_G7_SEL							
R/W							
0h							

Table 3-2856. CONTROLSS_INTXBAR12_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR12_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.129 CONTROLSS_INTXBAR12_G8 Register

3.19.2.129.1 CONTROLSS_INTXBAR12_G8 Register (Offset = 420h) [reset = 0h]

INT XBAR 12 Input Select.

Return to Summary Table

Table 3-2857. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5420h

Figure 3-1473. CONTROLSS_INTXBAR12_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR12_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR12_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR12_G8_SEL							
R/W							
0h							

Table 3-2858. CONTROLSS_INTXBAR12_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR12_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.130 CONTROLSS_INTXBAR12_G9 Register

3.19.2.130.1 CONTROLSS_INTXBAR12_G9 Register (Offset = 424h) [reset = 0h]

INT XBAR 12 Input Select.

Return to Summary Table

Table 3-2859. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5424h

Figure 3-1474. CONTROLSS_INTXBAR12_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR12_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR12_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR12_G9_SEL							
R/W							
0h							

Table 3-2860. CONTROLSS_INTXBAR12_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR12_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.131 CONTROLSS_INTXBAR13_G0 Register

3.19.2.131.1 CONTROLSS_INTXBAR13_G0 Register (Offset = 440h) [reset = 0h]

INT XBAR 13 Input Select.

Return to Summary Table

Table 3-2861. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5440h

Figure 3-1475. CONTROLSS_INTXBAR13_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR13_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR13_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR13_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR13_G0_SEL							
R/W							
0h							

Table 3-2862. CONTROLSS_INTXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR13_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.132 CONTROLSS_INTXBAR13_G1 Register

3.19.2.132.1 CONTROLSS_INTXBAR13_G1 Register (Offset = 444h) [reset = 0h]

INT XBAR 13 Input Select.

Return to Summary Table

Table 3-2863. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5444h

Figure 3-1476. CONTROLSS_INTXBAR13_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR13_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR13_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR13_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR13_G1_SEL							
R/W							
0h							

Table 3-2864. CONTROLSS_INTXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR13_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.133 CONTROLSS_INTXBAR13_G2 Register

3.19.2.133.1 CONTROLSS_INTXBAR13_G2 Register (Offset = 448h) [reset = 0h]

INT XBAR 13 Input Select.

Return to Summary Table

Table 3-2865. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5448h

Figure 3-1477. CONTROLSS_INTXBAR13_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR13_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR13_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR13_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR13_G2_SEL							
R/W							
0h							

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Table 3-2866. CONTROLSS_INTXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR13_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.134 CONTROLSS_INTXBAR13_G3 Register

3.19.2.134.1 CONTROLSS_INTXBAR13_G3 Register (Offset = 44Ch) [reset = 0h]

INT XBAR 13 Input Select.

Return to Summary Table

Table 3-2867. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 544Ch

Figure 3-1478. CONTROLSS_INTXBAR13_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR13_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR13_G3_SEL							
R/W							
0h							

Table 3-2868. CONTROLSS_INTXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR13_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.135 CONTROLSS_INTXBAR13_G4 Register

3.19.2.135.1 CONTROLSS_INTXBAR13_G4 Register (Offset = 450h) [reset = 0h]

INT XBAR 13 Input Select.

Return to Summary Table

Table 3-2869. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5450h

Figure 3-1479. CONTROLSS_INTXBAR13_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR13_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR13_G4_SEL							
R/W							
0h							

Table 3-2870. CONTROLSS_INTXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR13_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.136 CONTROLSS_INTXBAR13_G5 Register

3.19.2.136.1 CONTROLSS_INTXBAR13_G5 Register (Offset = 454h) [reset = 0h]

INT XBAR 13 Input Select.

Return to Summary Table

Table 3-2871. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5454h

Figure 3-1480. CONTROLSS_INTXBAR13_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR13_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR13_G5_SEL							
R/W							
0h							

Table 3-2872. CONTROLSS_INTXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR13_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.137 CONTROLSS_INTXBAR13_G6 Register

3.19.2.137.1 CONTROLSS_INTXBAR13_G6 Register (Offset = 458h) [reset = 0h]

INT XBAR 13 Input Select.

Return to Summary Table

Table 3-2873. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5458h

Figure 3-1481. CONTROLSS_INTXBAR13_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR13_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2874. CONTROLSS_INTXBAR13_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR13_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.138 CONTROLSS_INTXBAR13_G7 Register

3.19.2.138.1 CONTROLSS_INTXBAR13_G7 Register (Offset = 45Ch) [reset = 0h]

INT XBAR 13 Input Select.

Return to Summary Table

Table 3-2875. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 545Ch

Figure 3-1482. CONTROLSS_INTXBAR13_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR13_G7_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR13_G7_SEL							
R/W							
0h							

Table 3-2876. CONTROLSS_INTXBAR13_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR13_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.139 CONTROLSS_INTXBAR13_G8 Register

3.19.2.139.1 CONTROLSS_INTXBAR13_G8 Register (Offset = 460h) [reset = 0h]

INT XBAR 13 Input Select.

Return to Summary Table

Table 3-2877. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5460h

Figure 3-1483. CONTROLSS_INTXBAR13_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR13_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR13_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR13_G8_SEL							
R/W							
0h							

Table 3-2878. CONTROLSS_INTXBAR13_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR13_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.140 CONTROLSS_INTXBAR13_G9 Register

3.19.2.140.1 CONTROLSS_INTXBAR13_G9 Register (Offset = 464h) [reset = 0h]

INT XBAR 13 Input Select.

Return to Summary Table

Table 3-2879. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5464h

Figure 3-1484. CONTROLSS_INTXBAR13_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR13_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR13_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR13_G9_SEL							
R/W							
0h							

Table 3-2880. CONTROLSS_INTXBAR13_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR13_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.141 CONTROLSS_INTXBAR14_G0 Register

3.19.2.141.1 CONTROLSS_INTXBAR14_G0 Register (Offset = 480h) [reset = 0h]

INT XBAR 14 Input Select.

Return to Summary Table

Table 3-2881. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5480h

Figure 3-1485. CONTROLSS_INTXBAR14_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR14_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR14_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR14_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR14_G0_SEL							
R/W							
0h							

Table 3-2882. CONTROLSS_INTXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR14_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.142 CONTROLSS_INTXBAR14_G1 Register

3.19.2.142.1 CONTROLSS_INTXBAR14_G1 Register (Offset = 484h) [reset = 0h]

INT XBAR 14 Input Select.

Return to Summary Table

Table 3-2883. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5484h

Figure 3-1486. CONTROLSS_INTXBAR14_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR14_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR14_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR14_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR14_G1_SEL							
R/W							
0h							

Table 3-2884. CONTROLSS_INTXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR14_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.143 CONTROLSS_INTXBAR14_G2 Register

3.19.2.143.1 CONTROLSS_INTXBAR14_G2 Register (Offset = 488h) [reset = 0h]

INT XBAR 14 Input Select.

Return to Summary Table

Table 3-2885. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5488h

Figure 3-1487. CONTROLSS_INTXBAR14_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR14_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR14_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR14_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR14_G2_SEL							
R/W							
0h							

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Table 3-2886. CONTROLSS_INTXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR14_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.144 CONTROLSS_INTXBAR14_G3 Register

3.19.2.144.1 CONTROLSS_INTXBAR14_G3 Register (Offset = 48Ch) [reset = 0h]

INT XBAR 14 Input Select.

Return to Summary Table

Table 3-2887. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 548Ch

Figure 3-1488. CONTROLSS_INTXBAR14_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR14_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR14_G3_SEL							
R/W							
0h							

Table 3-2888. CONTROLSS_INTXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR14_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.145 CONTROLSS_INTXBAR14_G4 Register

3.19.2.145.1 CONTROLSS_INTXBAR14_G4 Register (Offset = 490h) [reset = 0h]

INT XBAR 14 Input Select.

Return to Summary Table

Table 3-2889. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5490h

Figure 3-1489. CONTROLSS_INTXBAR14_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR14_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR14_G4_SEL							
R/W							
0h							

Table 3-2890. CONTROLSS_INTXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR14_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.146 CONTROLSS_INTXBAR14_G5 Register

3.19.2.146.1 CONTROLSS_INTXBAR14_G5 Register (Offset = 494h) [reset = 0h]

INT XBAR 14 Input Select.

Return to Summary Table

Table 3-2891. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5494h

Figure 3-1490. CONTROLSS_INTXBAR14_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR14_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR14_G5_SEL							
R/W							
0h							

Table 3-2892. CONTROLSS_INTXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR14_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.147 CONTROLSS_INTXBAR14_G6 Register

3.19.2.147.1 CONTROLSS_INTXBAR14_G6 Register (Offset = 498h) [reset = 0h]

INT XBAR 14 Input Select.

Return to Summary Table

Table 3-2893. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5498h

Figure 3-1491. CONTROLSS_INTXBAR14_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR14_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2894. CONTROLSS_INTXBAR14_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR14_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.148 CONTROLSS_INTXBAR14_G7 Register

3.19.2.148.1 CONTROLSS_INTXBAR14_G7 Register (Offset = 49Ch) [reset = 0h]

INT XBAR 14 Input Select.

Return to Summary Table

Table 3-2895. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 549Ch

Figure 3-1492. CONTROLSS_INTXBAR14_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR14_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR14_G7_SEL							
R/W							
0h							

Table 3-2896. CONTROLSS_INTXBAR14_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR14_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.149 CONTROLSS_INTXBAR14_G8 Register

3.19.2.149.1 CONTROLSS_INTXBAR14_G8 Register (Offset = 4A0h) [reset = 0h]

INT XBAR 14 Input Select.

Return to Summary Table

Table 3-2897. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54A0h

Figure 3-1493. CONTROLSS_INTXBAR14_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR14_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR14_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR14_G8_SEL							
R/W							
0h							

Table 3-2898. CONTROLSS_INTXBAR14_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR14_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.150 CONTROLSS_INTXBAR14_G9 Register

3.19.2.150.1 CONTROLSS_INTXBAR14_G9 Register (Offset = 4A4h) [reset = 0h]

INT XBAR 14 Input Select.

Return to Summary Table

Table 3-2899. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54A4h

Figure 3-1494. CONTROLSS_INTXBAR14_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR14_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR14_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR14_G9_SEL							
R/W							
0h							

Table 3-2900. CONTROLSS_INTXBAR14_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR14_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.151 CONTROLSS_INTXBAR15_G0 Register

3.19.2.151.1 CONTROLSS_INTXBAR15_G0 Register (Offset = 4C0h) [reset = 0h]

INT XBAR 15 Input Select.

Return to Summary Table

Table 3-2901. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54C0h

Figure 3-1495. CONTROLSS_INTXBAR15_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR15_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR15_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR15_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR15_G0_SEL							
R/W							
0h							

Table 3-2902. CONTROLSS_INTXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR15_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.152 CONTROLSS_INTXBAR15_G1 Register

3.19.2.152.1 CONTROLSS_INTXBAR15_G1 Register (Offset = 4C4h) [reset = 0h]

INT XBAR 15 Input Select.

Return to Summary Table

Table 3-2903. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54C4h

Figure 3-1496. CONTROLSS_INTXBAR15_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR15_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR15_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR15_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR15_G1_SEL							
R/W							
0h							

Table 3-2904. CONTROLSS_INTXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR15_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.153 CONTROLSS_INTXBAR15_G2 Register

3.19.2.153.1 CONTROLSS_INTXBAR15_G2 Register (Offset = 4C8h) [reset = 0h]

INT XBAR 15 Input Select.

Return to Summary Table

Table 3-2905. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54C8h

Figure 3-1497. CONTROLSS_INTXBAR15_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR15_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR15_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR15_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR15_G2_SEL							
R/W							
0h							

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Table 3-2906. CONTROLSS_INTXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR15_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.154 CONTROLSS_INTXBAR15_G3 Register

3.19.2.154.1 CONTROLSS_INTXBAR15_G3 Register (Offset = 4CCh) [reset = 0h]

INT XBAR 15 Input Select.

Return to Summary Table

Table 3-2907. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54CCh

Figure 3-1498. CONTROLSS_INTXBAR15_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR15_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR15_G3_SEL							
R/W							
0h							

Table 3-2908. CONTROLSS_INTXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR15_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.155 CONTROLSS_INTXBAR15_G4 Register

3.19.2.155.1 CONTROLSS_INTXBAR15_G4 Register (Offset = 4D0h) [reset = 0h]

INT XBAR 15 Input Select.

Return to Summary Table

Table 3-2909. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54D0h

Figure 3-1499. CONTROLSS_INTXBAR15_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR15_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR15_G4_SEL							
R/W							
0h							

Table 3-2910. CONTROLSS_INTXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR15_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.156 CONTROLSS_INTXBAR15_G5 Register

3.19.2.156.1 CONTROLSS_INTXBAR15_G5 Register (Offset = 4D4h) [reset = 0h]

INT XBAR 15 Input Select.

Return to Summary Table

Table 3-2911. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54D4h

Figure 3-1500. CONTROLSS_INTXBAR15_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR15_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR15_G5_SEL							
R/W							
0h							

Table 3-2912. CONTROLSS_INTXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR15_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.157 CONTROLSS_INTXBAR15_G6 Register

3.19.2.157.1 CONTROLSS_INTXBAR15_G6 Register (Offset = 4D8h) [reset = 0h]

INT XBAR 15 Input Select.

Return to Summary Table

Table 3-2913. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54D8h

Figure 3-1501. CONTROLSS_INTXBAR15_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR15_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2914. CONTROLSS_INTXBAR15_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR15_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.158 CONTROLSS_INTXBAR15_G7 Register

3.19.2.158.1 CONTROLSS_INTXBAR15_G7 Register (Offset = 4DCh) [reset = 0h]

INT XBAR 15 Input Select.

Return to Summary Table

Table 3-2915. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54DCh

Figure 3-1502. CONTROLSS_INTXBAR15_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR15_G7_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR15_G7_SEL							
R/W							
0h							

Table 3-2916. CONTROLSS_INTXBAR15_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR15_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.159 CONTROLSS_INTXBAR15_G8 Register

3.19.2.159.1 CONTROLSS_INTXBAR15_G8 Register (Offset = 4E0h) [reset = 0h]

INT XBAR 15 Input Select.

Return to Summary Table

Table 3-2917. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54E0h

Figure 3-1503. CONTROLSS_INTXBAR15_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR15_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR15_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR15_G8_SEL							
R/W							
0h							

Table 3-2918. CONTROLSS_INTXBAR15_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR15_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.160 CONTROLSS_INTXBAR15_G9 Register

3.19.2.160.1 CONTROLSS_INTXBAR15_G9 Register (Offset = 4E4h) [reset = 0h]

INT XBAR 15 Input Select.

Return to Summary Table

Table 3-2919. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 54E4h

Figure 3-1504. CONTROLSS_INTXBAR15_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR15_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR15_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR15_G9_SEL							
R/W							
0h							

Table 3-2920. CONTROLSS_INTXBAR15_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR15_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.161 CONTROLSS_INTXBAR16_G0 Register

3.19.2.161.1 CONTROLSS_INTXBAR16_G0 Register (Offset = 500h) [reset = 0h]

INT XBAR 16 Input Select.

Return to Summary Table

Table 3-2921. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5500h

Figure 3-1505. CONTROLSS_INTXBAR16_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR16_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR16_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR16_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR16_G0_SEL							
R/W							
0h							

Table 3-2922. CONTROLSS_INTXBAR16_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR16_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.162 CONTROLSS_INTXBAR16_G1 Register

3.19.2.162.1 CONTROLSS_INTXBAR16_G1 Register (Offset = 504h) [reset = 0h]

INT XBAR 16 Input Select.

Return to Summary Table

Table 3-2923. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5504h

Figure 3-1506. CONTROLSS_INTXBAR16_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR16_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR16_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR16_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR16_G1_SEL							
R/W							
0h							

Table 3-2924. CONTROLSS_INTXBAR16_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR16_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.163 CONTROLSS_INTXBAR16_G2 Register

3.19.2.163.1 CONTROLSS_INTXBAR16_G2 Register (Offset = 508h) [reset = 0h]

INT XBAR 16 Input Select.

Return to Summary Table

Table 3-2925. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5508h

Figure 3-1507. CONTROLSS_INTXBAR16_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR16_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR16_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR16_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR16_G2_SEL							
R/W							
0h							

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Table 3-2926. CONTROLSS_INTXBAR16_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR16_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.164 CONTROLSS_INTXBAR16_G3 Register

3.19.2.164.1 CONTROLSS_INTXBAR16_G3 Register (Offset = 50Ch) [reset = 0h]

INT XBAR 16 Input Select.

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Table 3-2927. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 550Ch

Figure 3-1508. CONTROLSS_INTXBAR16_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR16_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR16_G3_SEL							
R/W							
0h							

Table 3-2928. CONTROLSS_INTXBAR16_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR16_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.165 CONTROLSS_INTXBAR16_G4 Register

3.19.2.165.1 CONTROLSS_INTXBAR16_G4 Register (Offset = 510h) [reset = 0h]

INT XBAR 16 Input Select.

Return to Summary Table

Table 3-2929. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5510h

Figure 3-1509. CONTROLSS_INTXBAR16_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR16_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR16_G4_SEL							
R/W							
0h							

Table 3-2930. CONTROLSS_INTXBAR16_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR16_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.166 CONTROLSS_INTXBAR16_G5 Register

3.19.2.166.1 CONTROLSS_INTXBAR16_G5 Register (Offset = 514h) [reset = 0h]

INT XBAR 16 Input Select.

Return to Summary Table

Table 3-2931. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5514h

Figure 3-1510. CONTROLSS_INTXBAR16_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR16_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR16_G5_SEL							
R/W							
0h							

Table 3-2932. CONTROLSS_INTXBAR16_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR16_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.167 CONTROLSS_INTXBAR16_G6 Register

3.19.2.167.1 CONTROLSS_INTXBAR16_G6 Register (Offset = 518h) [reset = 0h]

INT XBAR 16 Input Select.

Return to Summary Table

Table 3-2933. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5518h

Figure 3-1511. CONTROLSS_INTXBAR16_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR16_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2934. CONTROLSS_INTXBAR16_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR16_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.168 CONTROLSS_INTXBAR16_G7 Register

3.19.2.168.1 CONTROLSS_INTXBAR16_G7 Register (Offset = 51Ch) [reset = 0h]

INT XBAR 16 Input Select.

Return to Summary Table

Table 3-2935. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 551Ch

Figure 3-1512. CONTROLSS_INTXBAR16_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR16_G7_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR16_G7_SEL							
R/W							
0h							

Table 3-2936. CONTROLSS_INTXBAR16_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR16_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.169 CONTROLSS_INTXBAR16_G8 Register

3.19.2.169.1 CONTROLSS_INTXBAR16_G8 Register (Offset = 520h) [reset = 0h]

INT XBAR 16 Input Select.

Return to Summary Table

Table 3-2937. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5520h

Figure 3-1513. CONTROLSS_INTXBAR16_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR16_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR16_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR16_G8_SEL							
R/W							
0h							

Table 3-2938. CONTROLSS_INTXBAR16_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR16_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.170 CONTROLSS_INTXBAR16_G9 Register

3.19.2.170.1 CONTROLSS_INTXBAR16_G9 Register (Offset = 524h) [reset = 0h]

INT XBAR 16 Input Select.

Return to Summary Table

Table 3-2939. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5524h

Figure 3-1514. CONTROLSS_INTXBAR16_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR16_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR16_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR16_G9_SEL							
R/W							
0h							

Table 3-2940. CONTROLSS_INTXBAR16_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR16_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.171 CONTROLSS_INTXBAR17_G0 Register

3.19.2.171.1 CONTROLSS_INTXBAR17_G0 Register (Offset = 540h) [reset = 0h]

INT XBAR 17 Input Select.

Return to Summary Table

Table 3-2941. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5540h

Figure 3-1515. CONTROLSS_INTXBAR17_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR17_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR17_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR17_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR17_G0_SEL							
R/W							
0h							

Table 3-2942. CONTROLSS_INTXBAR17_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR17_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.172 CONTROLSS_INTXBAR17_G1 Register

3.19.2.172.1 CONTROLSS_INTXBAR17_G1 Register (Offset = 544h) [reset = 0h]

INT XBAR 17 Input Select.

Return to Summary Table

Table 3-2943. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5544h

Figure 3-1516. CONTROLSS_INTXBAR17_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR17_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR17_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR17_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR17_G1_SEL							
R/W							
0h							

Table 3-2944. CONTROLSS_INTXBAR17_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR17_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.173 CONTROLSS_INTXBAR17_G2 Register

3.19.2.173.1 CONTROLSS_INTXBAR17_G2 Register (Offset = 548h) [reset = 0h]

INT XBAR 17 Input Select.

Return to Summary Table

Table 3-2945. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5548h

Figure 3-1517. CONTROLSS_INTXBAR17_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR17_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR17_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR17_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR17_G2_SEL							
R/W							
0h							

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Table 3-2946. CONTROLSS_INTXBAR17_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR17_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.174 CONTROLSS_INTXBAR17_G3 Register

3.19.2.174.1 CONTROLSS_INTXBAR17_G3 Register (Offset = 54Ch) [reset = 0h]

INT XBAR 17 Input Select.

Return to Summary Table

Table 3-2947. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 554Ch

Figure 3-1518. CONTROLSS_INTXBAR17_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR17_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR17_G3_SEL							
R/W							
0h							

Table 3-2948. CONTROLSS_INTXBAR17_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR17_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.175 CONTROLSS_INTXBAR17_G4 Register

3.19.2.175.1 CONTROLSS_INTXBAR17_G4 Register (Offset = 550h) [reset = 0h]

INT XBAR 17 Input Select.

Return to Summary Table

Table 3-2949. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5550h

Figure 3-1519. CONTROLSS_INTXBAR17_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR17_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR17_G4_SEL							
R/W							
0h							

Table 3-2950. CONTROLSS_INTXBAR17_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR17_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.176 CONTROLSS_INTXBAR17_G5 Register

3.19.2.176.1 CONTROLSS_INTXBAR17_G5 Register (Offset = 554h) [reset = 0h]

INT XBAR 17 Input Select.

Return to Summary Table

Table 3-2951. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5554h

Figure 3-1520. CONTROLSS_INTXBAR17_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR17_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR17_G5_SEL							
R/W							
0h							

Table 3-2952. CONTROLSS_INTXBAR17_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR17_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.177 CONTROLSS_INTXBAR17_G6 Register

3.19.2.177.1 CONTROLSS_INTXBAR17_G6 Register (Offset = 558h) [reset = 0h]

INT XBAR 17 Input Select.

Return to Summary Table

Table 3-2953. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5558h

Figure 3-1521. CONTROLSS_INTXBAR17_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR17_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2954. CONTROLSS_INTXBAR17_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR17_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.178 CONTROLSS_INTXBAR17_G7 Register

3.19.2.178.1 CONTROLSS_INTXBAR17_G7 Register (Offset = 55Ch) [reset = 0h]

INT XBAR 17 Input Select.

Return to Summary Table

Table 3-2955. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 555Ch

Figure 3-1522. CONTROLSS_INTXBAR17_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR17_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR17_G7_SEL							
R/W							
0h							

Table 3-2956. CONTROLSS_INTXBAR17_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR17_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.179 CONTROLSS_INTXBAR17_G8 Register

3.19.2.179.1 CONTROLSS_INTXBAR17_G8 Register (Offset = 560h) [reset = 0h]

INT XBAR 17 Input Select.

Return to Summary Table

Table 3-2957. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5560h

Figure 3-1523. CONTROLSS_INTXBAR17_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR17_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR17_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR17_G8_SEL							
R/W							
0h							

Table 3-2958. CONTROLSS_INTXBAR17_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR17_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.180 CONTROLSS_INTXBAR17_G9 Register

3.19.2.180.1 CONTROLSS_INTXBAR17_G9 Register (Offset = 564h) [reset = 0h]

INT XBAR 17 Input Select.

Return to Summary Table

Table 3-2959. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5564h

Figure 3-1524. CONTROLSS_INTXBAR17_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR17_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR17_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR17_G9_SEL							
R/W							
0h							

Table 3-2960. CONTROLSS_INTXBAR17_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR17_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.181 CONTROLSS_INTXBAR18_G0 Register

3.19.2.181.1 CONTROLSS_INTXBAR18_G0 Register (Offset = 580h) [reset = 0h]

INT XBAR 18 Input Select.

Return to Summary Table

Table 3-2961. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5580h

Figure 3-1525. CONTROLSS_INTXBAR18_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR18_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR18_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR18_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR18_G0_SEL							
R/W							
0h							

Table 3-2962. CONTROLSS_INTXBAR18_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR18_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.182 CONTROLSS_INTXBAR18_G1 Register

3.19.2.182.1 CONTROLSS_INTXBAR18_G1 Register (Offset = 584h) [reset = 0h]

INT XBAR 18 Input Select.

Return to Summary Table

Table 3-2963. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5584h

Figure 3-1526. CONTROLSS_INTXBAR18_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR18_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR18_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR18_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR18_G1_SEL							
R/W							
0h							

Table 3-2964. CONTROLSS_INTXBAR18_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR18_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.183 CONTROLSS_INTXBAR18_G2 Register

3.19.2.183.1 CONTROLSS_INTXBAR18_G2 Register (Offset = 588h) [reset = 0h]

INT XBAR 18 Input Select.

Return to Summary Table

Table 3-2965. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5588h

Figure 3-1527. CONTROLSS_INTXBAR18_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR18_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR18_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR18_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR18_G2_SEL							
R/W							
0h							

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Table 3-2966. CONTROLSS_INTXBAR18_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR18_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.184 CONTROLSS_INTXBAR18_G3 Register

3.19.2.184.1 CONTROLSS_INTXBAR18_G3 Register (Offset = 58Ch) [reset = 0h]

INT XBAR 18 Input Select.

Return to Summary Table

Table 3-2967. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 558Ch

Figure 3-1528. CONTROLSS_INTXBAR18_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR18_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR18_G3_SEL							
R/W							
0h							

Table 3-2968. CONTROLSS_INTXBAR18_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR18_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.185 CONTROLSS_INTXBAR18_G4 Register

3.19.2.185.1 CONTROLSS_INTXBAR18_G4 Register (Offset = 590h) [reset = 0h]

INT XBAR 18 Input Select.

Return to Summary Table

Table 3-2969. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5590h

Figure 3-1529. CONTROLSS_INTXBAR18_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR18_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR18_G4_SEL							
R/W							
0h							

Table 3-2970. CONTROLSS_INTXBAR18_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR18_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.186 CONTROLSS_INTXBAR18_G5 Register

3.19.2.186.1 CONTROLSS_INTXBAR18_G5 Register (Offset = 594h) [reset = 0h]

INT XBAR 18 Input Select.

Return to Summary Table

Table 3-2971. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5594h

Figure 3-1530. CONTROLSS_INTXBAR18_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR18_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR18_G5_SEL							
R/W							
0h							

Table 3-2972. CONTROLSS_INTXBAR18_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR18_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.187 CONTROLSS_INTXBAR18_G6 Register

3.19.2.187.1 CONTROLSS_INTXBAR18_G6 Register (Offset = 598h) [reset = 0h]

INT XBAR 18 Input Select.

Return to Summary Table

Table 3-2973. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5598h

Figure 3-1531. CONTROLSS_INTXBAR18_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR18_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2974. CONTROLSS_INTXBAR18_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR18_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.188 CONTROLSS_INTXBAR18_G7 Register

3.19.2.188.1 CONTROLSS_INTXBAR18_G7 Register (Offset = 59Ch) [reset = 0h]

INT XBAR 18 Input Select.

Return to Summary Table

Table 3-2975. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 559Ch

Figure 3-1532. CONTROLSS_INTXBAR18_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR18_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR18_G7_SEL							
R/W							
0h							

Table 3-2976. CONTROLSS_INTXBAR18_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR18_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.189 CONTROLSS_INTXBAR18_G8 Register

3.19.2.189.1 CONTROLSS_INTXBAR18_G8 Register (Offset = 5A0h) [reset = 0h]

INT XBAR 18 Input Select.

Return to Summary Table

Table 3-2977. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55A0h

Figure 3-1533. CONTROLSS_INTXBAR18_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR18_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR18_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR18_G8_SEL							
R/W							
0h							

Table 3-2978. CONTROLSS_INTXBAR18_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR18_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.190 CONTROLSS_INTXBAR18_G9 Register

3.19.2.190.1 CONTROLSS_INTXBAR18_G9 Register (Offset = 5A4h) [reset = 0h]

INT XBAR 18 Input Select.

Return to Summary Table

Table 3-2979. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55A4h

Figure 3-1534. CONTROLSS_INTXBAR18_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR18_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR18_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR18_G9_SEL							
R/W							
0h							

Table 3-2980. CONTROLSS_INTXBAR18_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR18_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.191 CONTROLSS_INTXBAR19_G0 Register

3.19.2.191.1 CONTROLSS_INTXBAR19_G0 Register (Offset = 5C0h) [reset = 0h]

INT XBAR 19 Input Select.

Return to Summary Table

Table 3-2981. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55C0h

Figure 3-1535. CONTROLSS_INTXBAR19_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR19_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR19_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR19_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR19_G0_SEL							
R/W							
0h							

Table 3-2982. CONTROLSS_INTXBAR19_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR19_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.192 CONTROLSS_INTXBAR19_G1 Register

3.19.2.192.1 CONTROLSS_INTXBAR19_G1 Register (Offset = 5C4h) [reset = 0h]

INT XBAR 19 Input Select.

Return to Summary Table

Table 3-2983. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55C4h

Figure 3-1536. CONTROLSS_INTXBAR19_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR19_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR19_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR19_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR19_G1_SEL							
R/W							
0h							

Table 3-2984. CONTROLSS_INTXBAR19_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR19_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.193 CONTROLSS_INTXBAR19_G2 Register

3.19.2.193.1 CONTROLSS_INTXBAR19_G2 Register (Offset = 5C8h) [reset = 0h]

INT XBAR 19 Input Select.

Return to Summary Table

Table 3-2985. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55C8h

Figure 3-1537. CONTROLSS_INTXBAR19_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR19_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR19_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR19_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR19_G2_SEL							
R/W							
0h							

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Table 3-2986. CONTROLSS_INTXBAR19_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR19_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.194 CONTROLSS_INTXBAR19_G3 Register

3.19.2.194.1 CONTROLSS_INTXBAR19_G3 Register (Offset = 5CCh) [reset = 0h]

INT XBAR 19 Input Select.

Return to Summary Table

Table 3-2987. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55CCh

Figure 3-1538. CONTROLSS_INTXBAR19_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR19_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR19_G3_SEL							
R/W							
0h							

Table 3-2988. CONTROLSS_INTXBAR19_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR19_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.195 CONTROLSS_INTXBAR19_G4 Register

3.19.2.195.1 CONTROLSS_INTXBAR19_G4 Register (Offset = 5D0h) [reset = 0h]

INT XBAR 19 Input Select.

Return to Summary Table

Table 3-2989. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55D0h

Figure 3-1539. CONTROLSS_INTXBAR19_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR19_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR19_G4_SEL							
R/W							
0h							

Table 3-2990. CONTROLSS_INTXBAR19_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR19_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.196 CONTROLSS_INTXBAR19_G5 Register

3.19.2.196.1 CONTROLSS_INTXBAR19_G5 Register (Offset = 5D4h) [reset = 0h]

INT XBAR 19 Input Select.

Return to Summary Table

Table 3-2991. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55D4h

Figure 3-1540. CONTROLSS_INTXBAR19_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR19_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR19_G5_SEL							
R/W							
0h							

Table 3-2992. CONTROLSS_INTXBAR19_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR19_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.197 CONTROLSS_INTXBAR19_G6 Register

3.19.2.197.1 CONTROLSS_INTXBAR19_G6 Register (Offset = 5D8h) [reset = 0h]

INT XBAR 19 Input Select.

Return to Summary Table

Table 3-2993. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55D8h

Figure 3-1541. CONTROLSS_INTXBAR19_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR19_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-2994. CONTROLSS_INTXBAR19_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR19_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.198 CONTROLSS_INTXBAR19_G7 Register

3.19.2.198.1 CONTROLSS_INTXBAR19_G7 Register (Offset = 5DCh) [reset = 0h]

INT XBAR 19 Input Select.

Return to Summary Table

Table 3-2995. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55DCh

Figure 3-1542. CONTROLSS_INTXBAR19_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR19_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR19_G7_SEL							
R/W							
0h							

Table 3-2996. CONTROLSS_INTXBAR19_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR19_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.199 CONTROLSS_INTXBAR19_G8 Register

3.19.2.199.1 CONTROLSS_INTXBAR19_G8 Register (Offset = 5E0h) [reset = 0h]

INT XBAR 19 Input Select.

Return to Summary Table

Table 3-2997. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55E0h

Figure 3-1543. CONTROLSS_INTXBAR19_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR19_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR19_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR19_G8_SEL							
R/W							
0h							

Table 3-2998. CONTROLSS_INTXBAR19_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR19_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.200 CONTROLSS_INTXBAR19_G9 Register

3.19.2.200.1 CONTROLSS_INTXBAR19_G9 Register (Offset = 5E4h) [reset = 0h]

INT XBAR 19 Input Select.

Return to Summary Table

Table 3-2999. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 55E4h

Figure 3-1544. CONTROLSS_INTXBAR19_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR19_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR19_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR19_G9_SEL							
R/W							
0h							

Table 3-3000. CONTROLSS_INTXBAR19_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR19_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.201 CONTROLSS_INTXBAR20_G0 Register

3.19.2.201.1 CONTROLSS_INTXBAR20_G0 Register (Offset = 600h) [reset = 0h]

INT XBAR 20 Input Select.

Return to Summary Table

Table 3-3001. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5600h

Figure 3-1545. CONTROLSS_INTXBAR20_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR20_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR20_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR20_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR20_G0_SEL							
R/W							
0h							

Table 3-3002. CONTROLSS_INTXBAR20_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR20_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.202 CONTROLSS_INTXBAR20_G1 Register

3.19.2.202.1 CONTROLSS_INTXBAR20_G1 Register (Offset = 604h) [reset = 0h]

INT XBAR 20 Input Select.

Return to Summary Table

Table 3-3003. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5604h

Figure 3-1546. CONTROLSS_INTXBAR20_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR20_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR20_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR20_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR20_G1_SEL							
R/W							
0h							

Table 3-3004. CONTROLSS_INTXBAR20_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR20_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.203 CONTROLSS_INTXBAR20_G2 Register

3.19.2.203.1 CONTROLSS_INTXBAR20_G2 Register (Offset = 608h) [reset = 0h]

INT XBAR 20 Input Select.

Return to Summary Table

Table 3-3005. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5608h

Figure 3-1547. CONTROLSS_INTXBAR20_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR20_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR20_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR20_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR20_G2_SEL							
R/W							
0h							

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Table 3-3006. CONTROLSS_INTXBAR20_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR20_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.204 CONTROLSS_INTXBAR20_G3 Register

3.19.2.204.1 CONTROLSS_INTXBAR20_G3 Register (Offset = 60Ch) [reset = 0h]

INT XBAR 20 Input Select.

Return to Summary Table

Table 3-3007. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 560Ch

Figure 3-1548. CONTROLSS_INTXBAR20_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR20_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR20_G3_SEL							
R/W							
0h							

Table 3-3008. CONTROLSS_INTXBAR20_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR20_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.205 CONTROLSS_INTXBAR20_G4 Register

3.19.2.205.1 CONTROLSS_INTXBAR20_G4 Register (Offset = 610h) [reset = 0h]

INT XBAR 20 Input Select.

Return to Summary Table

Table 3-3009. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5610h

Figure 3-1549. CONTROLSS_INTXBAR20_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR20_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR20_G4_SEL							
R/W							
0h							

Table 3-3010. CONTROLSS_INTXBAR20_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR20_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.206 CONTROLSS_INTXBAR20_G5 Register

3.19.2.206.1 CONTROLSS_INTXBAR20_G5 Register (Offset = 614h) [reset = 0h]

INT XBAR 20 Input Select.

Return to Summary Table

Table 3-3011. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5614h

Figure 3-1550. CONTROLSS_INTXBAR20_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR20_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR20_G5_SEL							
R/W							
0h							

Table 3-3012. CONTROLSS_INTXBAR20_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR20_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.207 CONTROLSS_INTXBAR20_G6 Register

3.19.2.207.1 CONTROLSS_INTXBAR20_G6 Register (Offset = 618h) [reset = 0h]

INT XBAR 20 Input Select.

Return to Summary Table

Table 3-3013. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5618h

Figure 3-1551. CONTROLSS_INTXBAR20_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR20_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3014. CONTROLSS_INTXBAR20_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR20_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.208 CONTROLSS_INTXBAR20_G7 Register

3.19.2.208.1 CONTROLSS_INTXBAR20_G7 Register (Offset = 61Ch) [reset = 0h]

INT XBAR 20 Input Select.

Return to Summary Table

Table 3-3015. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 561Ch

Figure 3-1552. CONTROLSS_INTXBAR20_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR20_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR20_G7_SEL							
R/W							
0h							

Table 3-3016. CONTROLSS_INTXBAR20_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR20_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.209 CONTROLSS_INTXBAR20_G8 Register

3.19.2.209.1 CONTROLSS_INTXBAR20_G8 Register (Offset = 620h) [reset = 0h]

INT XBAR 20 Input Select.

Return to Summary Table

Table 3-3017. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5620h

Figure 3-1553. CONTROLSS_INTXBAR20_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR20_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR20_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR20_G8_SEL							
R/W							
0h							

Table 3-3018. CONTROLSS_INTXBAR20_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR20_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.210 CONTROLSS_INTXBAR20_G9 Register

3.19.2.210.1 CONTROLSS_INTXBAR20_G9 Register (Offset = 624h) [reset = 0h]

INT XBAR 20 Input Select.

Return to Summary Table

Table 3-3019. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5624h

Figure 3-1554. CONTROLSS_INTXBAR20_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR20_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR20_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR20_G9_SEL							
R/W							
0h							

Table 3-3020. CONTROLSS_INTXBAR20_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR20_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.211 CONTROLSS_INTXBAR21_G0 Register

3.19.2.211.1 CONTROLSS_INTXBAR21_G0 Register (Offset = 640h) [reset = 0h]

INT XBAR 21 Input Select.

Return to Summary Table

Table 3-3021. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5640h

Figure 3-1555. CONTROLSS_INTXBAR21_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR21_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR21_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR21_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR21_G0_SEL							
R/W							
0h							

Table 3-3022. CONTROLSS_INTXBAR21_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR21_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.212 CONTROLSS_INTXBAR21_G1 Register

3.19.2.212.1 CONTROLSS_INTXBAR21_G1 Register (Offset = 644h) [reset = 0h]

INT XBAR 21 Input Select.

Return to Summary Table

Table 3-3023. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5644h

Figure 3-1556. CONTROLSS_INTXBAR21_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR21_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR21_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR21_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR21_G1_SEL							
R/W							
0h							

Table 3-3024. CONTROLSS_INTXBAR21_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR21_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.213 CONTROLSS_INTXBAR21_G2 Register

3.19.2.213.1 CONTROLSS_INTXBAR21_G2 Register (Offset = 648h) [reset = 0h]

INT XBAR 21 Input Select.

Return to Summary Table

Table 3-3025. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5648h

Figure 3-1557. CONTROLSS_INTXBAR21_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR21_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR21_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR21_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR21_G2_SEL							
R/W							
0h							

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Table 3-3026. CONTROLSS_INTXBAR21_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR21_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.214 CONTROLSS_INTXBAR21_G3 Register

3.19.2.214.1 CONTROLSS_INTXBAR21_G3 Register (Offset = 64Ch) [reset = 0h]

INT XBAR 21 Input Select.

Return to Summary Table

Table 3-3027. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 564Ch

Figure 3-1558. CONTROLSS_INTXBAR21_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR21_G3_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR21_G3_SEL							
R/W							
0h							

Table 3-3028. CONTROLSS_INTXBAR21_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR21_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.215 CONTROLSS_INTXBAR21_G4 Register

3.19.2.215.1 CONTROLSS_INTXBAR21_G4 Register (Offset = 650h) [reset = 0h]

INT XBAR 21 Input Select.

Return to Summary Table

Table 3-3029. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5650h

Figure 3-1559. CONTROLSS_INTXBAR21_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR21_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR21_G4_SEL							
R/W							
0h							

Table 3-3030. CONTROLSS_INTXBAR21_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR21_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.216 CONTROLSS_INTXBAR21_G5 Register

3.19.2.216.1 CONTROLSS_INTXBAR21_G5 Register (Offset = 654h) [reset = 0h]

INT XBAR 21 Input Select.

Return to Summary Table

Table 3-3031. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5654h

Figure 3-1560. CONTROLSS_INTXBAR21_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR21_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR21_G5_SEL							
R/W							
0h							

Table 3-3032. CONTROLSS_INTXBAR21_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR21_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.217 CONTROLSS_INTXBAR21_G6 Register

3.19.2.217.1 CONTROLSS_INTXBAR21_G6 Register (Offset = 658h) [reset = 0h]

INT XBAR 21 Input Select.

Return to Summary Table

Table 3-3033. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5658h

Figure 3-1561. CONTROLSS_INTXBAR21_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR21_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3034. CONTROLSS_INTXBAR21_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR21_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.218 CONTROLSS_INTXBAR21_G7 Register

3.19.2.218.1 CONTROLSS_INTXBAR21_G7 Register (Offset = 65Ch) [reset = 0h]

INT XBAR 21 Input Select.

Return to Summary Table

Table 3-3035. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 565Ch

Figure 3-1562. CONTROLSS_INTXBAR21_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR21_G7_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR21_G7_SEL							
R/W							
0h							

Table 3-3036. CONTROLSS_INTXBAR21_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR21_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.219 CONTROLSS_INTXBAR21_G8 Register

3.19.2.219.1 CONTROLSS_INTXBAR21_G8 Register (Offset = 660h) [reset = 0h]

INT XBAR 21 Input Select.

Return to Summary Table

Table 3-3037. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5660h

Figure 3-1563. CONTROLSS_INTXBAR21_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR21_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR21_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR21_G8_SEL							
R/W							
0h							

Table 3-3038. CONTROLSS_INTXBAR21_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR21_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.220 CONTROLSS_INTXBAR21_G9 Register

3.19.2.220.1 CONTROLSS_INTXBAR21_G9 Register (Offset = 664h) [reset = 0h]

INT XBAR 21 Input Select.

Return to Summary Table

Table 3-3039. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5664h

Figure 3-1564. CONTROLSS_INTXBAR21_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR21_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR21_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR21_G9_SEL							
R/W							
0h							

Table 3-3040. CONTROLSS_INTXBAR21_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR21_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.221 CONTROLSS_INTXBAR22_G0 Register

3.19.2.221.1 CONTROLSS_INTXBAR22_G0 Register (Offset = 680h) [reset = 0h]

INT XBAR 22 Input Select.

Return to Summary Table

Table 3-3041. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5680h

Figure 3-1565. CONTROLSS_INTXBAR22_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR22_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR22_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR22_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR22_G0_SEL							
R/W							
0h							

Table 3-3042. CONTROLSS_INTXBAR22_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR22_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.222 CONTROLSS_INTXBAR22_G1 Register

3.19.2.222.1 CONTROLSS_INTXBAR22_G1 Register (Offset = 684h) [reset = 0h]

INT XBAR 22 Input Select.

Return to Summary Table

Table 3-3043. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5684h

Figure 3-1566. CONTROLSS_INTXBAR22_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR22_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR22_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR22_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR22_G1_SEL							
R/W							
0h							

Table 3-3044. CONTROLSS_INTXBAR22_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR22_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.223 CONTROLSS_INTXBAR22_G2 Register

3.19.2.223.1 CONTROLSS_INTXBAR22_G2 Register (Offset = 688h) [reset = 0h]

INT XBAR 22 Input Select.

Return to Summary Table

Table 3-3045. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5688h

Figure 3-1567. CONTROLSS_INTXBAR22_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR22_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR22_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR22_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR22_G2_SEL							
R/W							
0h							

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Table 3-3046. CONTROLSS_INTXBAR22_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR22_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.224 CONTROLSS_INTXBAR22_G3 Register

3.19.2.224.1 CONTROLSS_INTXBAR22_G3 Register (Offset = 68Ch) [reset = 0h]

INT XBAR 22 Input Select.

Return to Summary Table

Table 3-3047. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 568Ch

Figure 3-1568. CONTROLSS_INTXBAR22_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR22_G3_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR22_G3_SEL							
R/W							
0h							

Table 3-3048. CONTROLSS_INTXBAR22_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR22_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.225 CONTROLSS_INTXBAR22_G4 Register

3.19.2.225.1 CONTROLSS_INTXBAR22_G4 Register (Offset = 690h) [reset = 0h]

INT XBAR 22 Input Select.

Return to Summary Table

Table 3-3049. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5690h

Figure 3-1569. CONTROLSS_INTXBAR22_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR22_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR22_G4_SEL							
R/W							
0h							

Table 3-3050. CONTROLSS_INTXBAR22_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR22_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.226 CONTROLSS_INTXBAR22_G5 Register

3.19.2.226.1 CONTROLSS_INTXBAR22_G5 Register (Offset = 694h) [reset = 0h]

INT XBAR 22 Input Select.

Return to Summary Table

Table 3-3051. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5694h

Figure 3-1570. CONTROLSS_INTXBAR22_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR22_G5_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR22_G5_SEL							
R/W							
0h							

Table 3-3052. CONTROLSS_INTXBAR22_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR22_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.227 CONTROLSS_INTXBAR22_G6 Register

3.19.2.227.1 CONTROLSS_INTXBAR22_G6 Register (Offset = 698h) [reset = 0h]

INT XBAR 22 Input Select.

Return to Summary Table

Table 3-3053. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5698h

Figure 3-1571. CONTROLSS_INTXBAR22_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR22_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3054. CONTROLSS_INTXBAR22_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR22_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.228 CONTROLSS_INTXBAR22_G7 Register

3.19.2.228.1 CONTROLSS_INTXBAR22_G7 Register (Offset = 69Ch) [reset = 0h]

INT XBAR 22 Input Select.

Return to Summary Table

Table 3-3055. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 569Ch

Figure 3-1572. CONTROLSS_INTXBAR22_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR22_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR22_G7_SEL							
R/W							
0h							

Table 3-3056. CONTROLSS_INTXBAR22_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR22_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.229 CONTROLSS_INTXBAR22_G8 Register

3.19.2.229.1 CONTROLSS_INTXBAR22_G8 Register (Offset = 6A0h) [reset = 0h]

INT XBAR 22 Input Select.

Return to Summary Table

Table 3-3057. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56A0h

Figure 3-1573. CONTROLSS_INTXBAR22_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR22_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR22_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR22_G8_SEL							
R/W							
0h							

Table 3-3058. CONTROLSS_INTXBAR22_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR22_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.230 CONTROLSS_INTXBAR22_G9 Register

3.19.2.230.1 CONTROLSS_INTXBAR22_G9 Register (Offset = 6A4h) [reset = 0h]

INT XBAR 22 Input Select.

Return to Summary Table

Table 3-3059. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56A4h

Figure 3-1574. CONTROLSS_INTXBAR22_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR22_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR22_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR22_G9_SEL							
R/W							
0h							

Table 3-3060. CONTROLSS_INTXBAR22_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR22_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.231 CONTROLSS_INTXBAR23_G0 Register

3.19.2.231.1 CONTROLSS_INTXBAR23_G0 Register (Offset = 6C0h) [reset = 0h]

INT XBAR 23 Input Select.

Return to Summary Table

Table 3-3061. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56C0h

Figure 3-1575. CONTROLSS_INTXBAR23_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR23_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR23_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR23_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR23_G0_SEL							
R/W							
0h							

Table 3-3062. CONTROLSS_INTXBAR23_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR23_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.232 CONTROLSS_INTXBAR23_G1 Register

3.19.2.232.1 CONTROLSS_INTXBAR23_G1 Register (Offset = 6C4h) [reset = 0h]

INT XBAR 23 Input Select.

Return to Summary Table

Table 3-3063. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56C4h

Figure 3-1576. CONTROLSS_INTXBAR23_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR23_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR23_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR23_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR23_G1_SEL							
R/W							
0h							

Table 3-3064. CONTROLSS_INTXBAR23_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR23_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.233 CONTROLSS_INTXBAR23_G2 Register

3.19.2.233.1 CONTROLSS_INTXBAR23_G2 Register (Offset = 6C8h) [reset = 0h]

INT XBAR 23 Input Select.

Return to Summary Table

Table 3-3065. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56C8h

Figure 3-1577. CONTROLSS_INTXBAR23_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR23_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR23_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR23_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR23_G2_SEL							
R/W							
0h							

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Table 3-3066. CONTROLSS_INTXBAR23_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR23_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.234 CONTROLSS_INTXBAR23_G3 Register

3.19.2.234.1 CONTROLSS_INTXBAR23_G3 Register (Offset = 6CCh) [reset = 0h]

INT XBAR 23 Input Select.

Return to Summary Table

Table 3-3067. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56CCh

Figure 3-1578. CONTROLSS_INTXBAR23_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR23_G3_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR23_G3_SEL							
R/W							
0h							

Table 3-3068. CONTROLSS_INTXBAR23_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR23_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.235 CONTROLSS_INTXBAR23_G4 Register

3.19.2.235.1 CONTROLSS_INTXBAR23_G4 Register (Offset = 6D0h) [reset = 0h]

INT XBAR 23 Input Select.

Return to Summary Table

Table 3-3069. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56D0h

Figure 3-1579. CONTROLSS_INTXBAR23_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR23_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR23_G4_SEL							
R/W							
0h							

Table 3-3070. CONTROLSS_INTXBAR23_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR23_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.236 CONTROLSS_INTXBAR23_G5 Register

3.19.2.236.1 CONTROLSS_INTXBAR23_G5 Register (Offset = 6D4h) [reset = 0h]

INT XBAR 23 Input Select.

Return to Summary Table

Table 3-3071. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56D4h

Figure 3-1580. CONTROLSS_INTXBAR23_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR23_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR23_G5_SEL							
R/W							
0h							

Table 3-3072. CONTROLSS_INTXBAR23_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR23_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.237 CONTROLSS_INTXBAR23_G6 Register

3.19.2.237.1 CONTROLSS_INTXBAR23_G6 Register (Offset = 6D8h) [reset = 0h]

INT XBAR 23 Input Select.

Return to Summary Table

Table 3-3073. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56D8h

Figure 3-1581. CONTROLSS_INTXBAR23_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					INTXBAR23_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3074. CONTROLSS_INTXBAR23_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR23_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.238 CONTROLSS_INTXBAR23_G7 Register

3.19.2.238.1 CONTROLSS_INTXBAR23_G7 Register (Offset = 6DCh) [reset = 0h]

INT XBAR 23 Input Select.

Return to Summary Table

Table 3-3075. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56DCh

Figure 3-1582. CONTROLSS_INTXBAR23_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR23_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR23_G7_SEL							
R/W							
0h							

Table 3-3076. CONTROLSS_INTXBAR23_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR23_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.239 CONTROLSS_INTXBAR23_G8 Register

3.19.2.239.1 CONTROLSS_INTXBAR23_G8 Register (Offset = 6E0h) [reset = 0h]

INT XBAR 23 Input Select.

Return to Summary Table

Table 3-3077. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56E0h

Figure 3-1583. CONTROLSS_INTXBAR23_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR23_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR23_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR23_G8_SEL							
R/W							
0h							

Table 3-3078. CONTROLSS_INTXBAR23_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR23_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.240 CONTROLSS_INTXBAR23_G9 Register

3.19.2.240.1 CONTROLSS_INTXBAR23_G9 Register (Offset = 6E4h) [reset = 0h]

INT XBAR 23 Input Select.

Return to Summary Table

Table 3-3079. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 56E4h

Figure 3-1584. CONTROLSS_INTXBAR23_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR23_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR23_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR23_G9_SEL							
R/W							
0h							

Table 3-3080. CONTROLSS_INTXBAR23_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR23_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.241 CONTROLSS_INTXBAR24_G0 Register

3.19.2.241.1 CONTROLSS_INTXBAR24_G0 Register (Offset = 700h) [reset = 0h]

INT XBAR 24 Input Select.

Return to Summary Table

Table 3-3081. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5700h

Figure 3-1585. CONTROLSS_INTXBAR24_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR24_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR24_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR24_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR24_G0_SEL							
R/W							
0h							

Table 3-3082. CONTROLSS_INTXBAR24_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR24_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.242 CONTROLSS_INTXBAR24_G1 Register

3.19.2.242.1 CONTROLSS_INTXBAR24_G1 Register (Offset = 704h) [reset = 0h]

INT XBAR 24 Input Select.

Return to Summary Table

Table 3-3083. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5704h

Figure 3-1586. CONTROLSS_INTXBAR24_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR24_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR24_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR24_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR24_G1_SEL							
R/W							
0h							

Table 3-3084. CONTROLSS_INTXBAR24_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR24_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.243 CONTROLSS_INTXBAR24_G2 Register

3.19.2.243.1 CONTROLSS_INTXBAR24_G2 Register (Offset = 708h) [reset = 0h]

INT XBAR 24 Input Select.

Return to Summary Table

Table 3-3085. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5708h

Figure 3-1587. CONTROLSS_INTXBAR24_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR24_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR24_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR24_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR24_G2_SEL							
R/W							
0h							

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Table 3-3086. CONTROLSS_INTXBAR24_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR24_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.244 CONTROLSS_INTXBAR24_G3 Register

3.19.2.244.1 CONTROLSS_INTXBAR24_G3 Register (Offset = 70Ch) [reset = 0h]

INT XBAR 24 Input Select.

Return to Summary Table

Table 3-3087. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 570Ch

Figure 3-1588. CONTROLSS_INTXBAR24_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR24_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR24_G3_SEL							
R/W							
0h							

Table 3-3088. CONTROLSS_INTXBAR24_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR24_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.245 CONTROLSS_INTXBAR24_G4 Register

3.19.2.245.1 CONTROLSS_INTXBAR24_G4 Register (Offset = 710h) [reset = 0h]

INT XBAR 24 Input Select.

Return to Summary Table

Table 3-3089. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5710h

Figure 3-1589. CONTROLSS_INTXBAR24_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR24_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR24_G4_SEL							
R/W							
0h							

Table 3-3090. CONTROLSS_INTXBAR24_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR24_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.246 CONTROLSS_INTXBAR24_G5 Register

3.19.2.246.1 CONTROLSS_INTXBAR24_G5 Register (Offset = 714h) [reset = 0h]

INT XBAR 24 Input Select.

Return to Summary Table

Table 3-3091. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5714h

Figure 3-1590. CONTROLSS_INTXBAR24_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR24_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR24_G5_SEL							
R/W							
0h							

Table 3-3092. CONTROLSS_INTXBAR24_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR24_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.247 CONTROLSS_INTXBAR24_G6 Register

3.19.2.247.1 CONTROLSS_INTXBAR24_G6 Register (Offset = 718h) [reset = 0h]

INT XBAR 24 Input Select.

Return to Summary Table

Table 3-3093. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5718h

Figure 3-1591. CONTROLSS_INTXBAR24_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR24_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3094. CONTROLSS_INTXBAR24_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR24_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.248 CONTROLSS_INTXBAR24_G7 Register

3.19.2.248.1 CONTROLSS_INTXBAR24_G7 Register (Offset = 71Ch) [reset = 0h]

INT XBAR 24 Input Select.

Return to Summary Table

Table 3-3095. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 571Ch

Figure 3-1592. CONTROLSS_INTXBAR24_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR24_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR24_G7_SEL							
R/W							
0h							

Table 3-3096. CONTROLSS_INTXBAR24_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR24_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.249 CONTROLSS_INTXBAR24_G8 Register

3.19.2.249.1 CONTROLSS_INTXBAR24_G8 Register (Offset = 720h) [reset = 0h]

INT XBAR 24 Input Select.

Return to Summary Table

Table 3-3097. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5720h

Figure 3-1593. CONTROLSS_INTXBAR24_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR24_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR24_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR24_G8_SEL							
R/W							
0h							

Table 3-3098. CONTROLSS_INTXBAR24_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR24_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.250 CONTROLSS_INTXBAR24_G9 Register

3.19.2.250.1 CONTROLSS_INTXBAR24_G9 Register (Offset = 724h) [reset = 0h]

INT XBAR 24 Input Select.

Return to Summary Table

Table 3-3099. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5724h

Figure 3-1594. CONTROLSS_INTXBAR24_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR24_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR24_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR24_G9_SEL							
R/W							
0h							

Table 3-3100. CONTROLSS_INTXBAR24_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR24_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.251 CONTROLSS_INTXBAR25_G0 Register

3.19.2.251.1 CONTROLSS_INTXBAR25_G0 Register (Offset = 740h) [reset = 0h]

INT XBAR 25 Input Select.

Return to Summary Table

Table 3-3101. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5740h

Figure 3-1595. CONTROLSS_INTXBAR25_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR25_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR25_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR25_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR25_G0_SEL							
R/W							
0h							

Table 3-3102. CONTROLSS_INTXBAR25_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR25_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.252 CONTROLSS_INTXBAR25_G1 Register

3.19.2.252.1 CONTROLSS_INTXBAR25_G1 Register (Offset = 744h) [reset = 0h]

INT XBAR 25 Input Select.

Return to Summary Table

Table 3-3103. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5744h

Figure 3-1596. CONTROLSS_INTXBAR25_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR25_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR25_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR25_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR25_G1_SEL							
R/W							
0h							

Table 3-3104. CONTROLSS_INTXBAR25_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR25_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.253 CONTROLSS_INTXBAR25_G2 Register

3.19.2.253.1 CONTROLSS_INTXBAR25_G2 Register (Offset = 748h) [reset = 0h]

INT XBAR 25 Input Select.

Return to Summary Table

Table 3-3105. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5748h

Figure 3-1597. CONTROLSS_INTXBAR25_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR25_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR25_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR25_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR25_G2_SEL							
R/W							
0h							

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Table 3-3106. CONTROLSS_INTXBAR25_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR25_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.254 CONTROLSS_INTXBAR25_G3 Register

3.19.2.254.1 CONTROLSS_INTXBAR25_G3 Register (Offset = 74Ch) [reset = 0h]

INT XBAR 25 Input Select.

Return to Summary Table

Table 3-3107. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 574Ch

Figure 3-1598. CONTROLSS_INTXBAR25_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR25_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR25_G3_SEL							
R/W							
0h							

Table 3-3108. CONTROLSS_INTXBAR25_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR25_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.255 CONTROLSS_INTXBAR25_G4 Register

3.19.2.255.1 CONTROLSS_INTXBAR25_G4 Register (Offset = 750h) [reset = 0h]

INT XBAR 25 Input Select.

Return to Summary Table

Table 3-3109. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5750h

Figure 3-1599. CONTROLSS_INTXBAR25_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR25_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR25_G4_SEL							
R/W							
0h							

Table 3-3110. CONTROLSS_INTXBAR25_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR25_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.256 CONTROLSS_INTXBAR25_G5 Register

3.19.2.256.1 CONTROLSS_INTXBAR25_G5 Register (Offset = 754h) [reset = 0h]

INT XBAR 25 Input Select.

Return to Summary Table

Table 3-3111. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5754h

Figure 3-1600. CONTROLSS_INTXBAR25_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR25_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR25_G5_SEL							
R/W							
0h							

Table 3-3112. CONTROLSS_INTXBAR25_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR25_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.257 CONTROLSS_INTXBAR25_G6 Register

3.19.2.257.1 CONTROLSS_INTXBAR25_G6 Register (Offset = 758h) [reset = 0h]

INT XBAR 25 Input Select.

Return to Summary Table

Table 3-3113. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5758h

Figure 3-1601. CONTROLSS_INTXBAR25_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR25_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3114. CONTROLSS_INTXBAR25_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR25_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.258 CONTROLSS_INTXBAR25_G7 Register

3.19.2.258.1 CONTROLSS_INTXBAR25_G7 Register (Offset = 75Ch) [reset = 0h]

INT XBAR 25 Input Select.

Return to Summary Table

Table 3-3115. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 575Ch

Figure 3-1602. CONTROLSS_INTXBAR25_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR25_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR25_G7_SEL							
R/W							
0h							

Table 3-3116. CONTROLSS_INTXBAR25_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR25_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.259 CONTROLSS_INTXBAR25_G8 Register

3.19.2.259.1 CONTROLSS_INTXBAR25_G8 Register (Offset = 760h) [reset = 0h]

INT XBAR 25 Input Select.

Return to Summary Table

Table 3-3117. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5760h

Figure 3-1603. CONTROLSS_INTXBAR25_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR25_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR25_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR25_G8_SEL							
R/W							
0h							

Table 3-3118. CONTROLSS_INTXBAR25_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR25_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.260 CONTROLSS_INTXBAR25_G9 Register

3.19.2.260.1 CONTROLSS_INTXBAR25_G9 Register (Offset = 764h) [reset = 0h]

INT XBAR 25 Input Select.

Return to Summary Table

Table 3-3119. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5764h

Figure 3-1604. CONTROLSS_INTXBAR25_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR25_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR25_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR25_G9_SEL							
R/W							
0h							

Table 3-3120. CONTROLSS_INTXBAR25_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR25_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.261 CONTROLSS_INTXBAR26_G0 Register

3.19.2.261.1 CONTROLSS_INTXBAR26_G0 Register (Offset = 780h) [reset = 0h]

INT XBAR 26 Input Select.

Return to Summary Table

Table 3-3121. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5780h

Figure 3-1605. CONTROLSS_INTXBAR26_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR26_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR26_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR26_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR26_G0_SEL							
R/W							
0h							

Table 3-3122. CONTROLSS_INTXBAR26_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR26_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.262 CONTROLSS_INTXBAR26_G1 Register

3.19.2.262.1 CONTROLSS_INTXBAR26_G1 Register (Offset = 784h) [reset = 0h]

INT XBAR 26 Input Select.

Return to Summary Table

Table 3-3123. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5784h

Figure 3-1606. CONTROLSS_INTXBAR26_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR26_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR26_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR26_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR26_G1_SEL							
R/W							
0h							

Table 3-3124. CONTROLSS_INTXBAR26_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR26_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.263 CONTROLSS_INTXBAR26_G2 Register

3.19.2.263.1 CONTROLSS_INTXBAR26_G2 Register (Offset = 788h) [reset = 0h]

INT XBAR 26 Input Select.

Return to Summary Table

Table 3-3125. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5788h

Figure 3-1607. CONTROLSS_INTXBAR26_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR26_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR26_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR26_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR26_G2_SEL							
R/W							
0h							

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Table 3-3126. CONTROLSS_INTXBAR26_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR26_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.264 CONTROLSS_INTXBAR26_G3 Register

3.19.2.264.1 CONTROLSS_INTXBAR26_G3 Register (Offset = 78Ch) [reset = 0h]

INT XBAR 26 Input Select.

Return to Summary Table

Table 3-3127. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 578Ch

Figure 3-1608. CONTROLSS_INTXBAR26_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR26_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR26_G3_SEL							
R/W							
0h							

Table 3-3128. CONTROLSS_INTXBAR26_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR26_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.265 CONTROLSS_INTXBAR26_G4 Register

3.19.2.265.1 CONTROLSS_INTXBAR26_G4 Register (Offset = 790h) [reset = 0h]

INT XBAR 26 Input Select.

Return to Summary Table

Table 3-3129. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5790h

Figure 3-1609. CONTROLSS_INTXBAR26_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR26_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR26_G4_SEL							
R/W							
0h							

Table 3-3130. CONTROLSS_INTXBAR26_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR26_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.266 CONTROLSS_INTXBAR26_G5 Register

3.19.2.266.1 CONTROLSS_INTXBAR26_G5 Register (Offset = 794h) [reset = 0h]

INT XBAR 26 Input Select.

Return to Summary Table

Table 3-3131. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5794h

Figure 3-1610. CONTROLSS_INTXBAR26_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR26_G5_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR26_G5_SEL							
R/W							
0h							

Table 3-3132. CONTROLSS_INTXBAR26_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR26_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.267 CONTROLSS_INTXBAR26_G6 Register

3.19.2.267.1 CONTROLSS_INTXBAR26_G6 Register (Offset = 798h) [reset = 0h]

INT XBAR 26 Input Select.

Return to Summary Table

Table 3-3133. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5798h

Figure 3-1611. CONTROLSS_INTXBAR26_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					INTXBAR26_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3134. CONTROLSS_INTXBAR26_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR26_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.268 CONTROLSS_INTXBAR26_G7 Register

3.19.2.268.1 CONTROLSS_INTXBAR26_G7 Register (Offset = 79Ch) [reset = 0h]

INT XBAR 26 Input Select.

Return to Summary Table

Table 3-3135. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 579Ch

Figure 3-1612. CONTROLSS_INTXBAR26_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR26_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR26_G7_SEL							
R/W							
0h							

Table 3-3136. CONTROLSS_INTXBAR26_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR26_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.269 CONTROLSS_INTXBAR26_G8 Register

3.19.2.269.1 CONTROLSS_INTXBAR26_G8 Register (Offset = 7A0h) [reset = 0h]

INT XBAR 26 Input Select.

Return to Summary Table

Table 3-3137. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57A0h

Figure 3-1613. CONTROLSS_INTXBAR26_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR26_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR26_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR26_G8_SEL							
R/W							
0h							

Table 3-3138. CONTROLSS_INTXBAR26_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR26_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.270 CONTROLSS_INTXBAR26_G9 Register

3.19.2.270.1 CONTROLSS_INTXBAR26_G9 Register (Offset = 7A4h) [reset = 0h]

INT XBAR 26 Input Select.

Return to Summary Table

Table 3-3139. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57A4h

Figure 3-1614. CONTROLSS_INTXBAR26_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR26_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR26_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR26_G9_SEL							
R/W							
0h							

Table 3-3140. CONTROLSS_INTXBAR26_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR26_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.271 CONTROLSS_INTXBAR27_G0 Register

3.19.2.271.1 CONTROLSS_INTXBAR27_G0 Register (Offset = 7C0h) [reset = 0h]

INT XBAR 27 Input Select.

Return to Summary Table

Table 3-3141. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57C0h

Figure 3-1615. CONTROLSS_INTXBAR27_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR27_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR27_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR27_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR27_G0_SEL							
R/W							
0h							

Table 3-3142. CONTROLSS_INTXBAR27_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR27_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.272 CONTROLSS_INTXBAR27_G1 Register

3.19.2.272.1 CONTROLSS_INTXBAR27_G1 Register (Offset = 7C4h) [reset = 0h]

INT XBAR 27 Input Select.

Return to Summary Table

Table 3-3143. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57C4h

Figure 3-1616. CONTROLSS_INTXBAR27_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR27_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR27_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR27_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR27_G1_SEL							
R/W							
0h							

Table 3-3144. CONTROLSS_INTXBAR27_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR27_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.273 CONTROLSS_INTXBAR27_G2 Register

3.19.2.273.1 CONTROLSS_INTXBAR27_G2 Register (Offset = 7C8h) [reset = 0h]

INT XBAR 27 Input Select.

Return to Summary Table

Table 3-3145. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57C8h

Figure 3-1617. CONTROLSS_INTXBAR27_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR27_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR27_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR27_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR27_G2_SEL							
R/W							
0h							

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Table 3-3146. CONTROLSS_INTXBAR27_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR27_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.274 CONTROLSS_INTXBAR27_G3 Register

3.19.2.274.1 CONTROLSS_INTXBAR27_G3 Register (Offset = 7CCh) [reset = 0h]

INT XBAR 27 Input Select.

Return to Summary Table

Table 3-3147. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57CCh

Figure 3-1618. CONTROLSS_INTXBAR27_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR27_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR27_G3_SEL							
R/W							
0h							

Table 3-3148. CONTROLSS_INTXBAR27_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR27_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.275 CONTROLSS_INTXBAR27_G4 Register

3.19.2.275.1 CONTROLSS_INTXBAR27_G4 Register (Offset = 7D0h) [reset = 0h]

INT XBAR 27 Input Select.

Return to Summary Table

Table 3-3149. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57D0h

Figure 3-1619. CONTROLSS_INTXBAR27_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR27_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR27_G4_SEL							
R/W							
0h							

Table 3-3150. CONTROLSS_INTXBAR27_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR27_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.276 CONTROLSS_INTXBAR27_G5 Register

3.19.2.276.1 CONTROLSS_INTXBAR27_G5 Register (Offset = 7D4h) [reset = 0h]

INT XBAR 27 Input Select.

Return to Summary Table

Table 3-3151. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57D4h

Figure 3-1620. CONTROLSS_INTXBAR27_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR27_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR27_G5_SEL							
R/W							
0h							

Table 3-3152. CONTROLSS_INTXBAR27_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR27_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.277 CONTROLSS_INTXBAR27_G6 Register

3.19.2.277.1 CONTROLSS_INTXBAR27_G6 Register (Offset = 7D8h) [reset = 0h]

INT XBAR 27 Input Select.

Return to Summary Table

Table 3-3153. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57D8h

Figure 3-1621. CONTROLSS_INTXBAR27_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR27_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3154. CONTROLSS_INTXBAR27_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR27_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.278 CONTROLSS_INTXBAR27_G7 Register

3.19.2.278.1 CONTROLSS_INTXBAR27_G7 Register (Offset = 7DCh) [reset = 0h]

INT XBAR 27 Input Select.

Return to Summary Table

Table 3-3155. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57DCh

Figure 3-1622. CONTROLSS_INTXBAR27_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR27_G7_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR27_G7_SEL							
R/W							
0h							

Table 3-3156. CONTROLSS_INTXBAR27_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR27_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.279 CONTROLSS_INTXBAR27_G8 Register

3.19.2.279.1 CONTROLSS_INTXBAR27_G8 Register (Offset = 7E0h) [reset = 0h]

INT XBAR 27 Input Select.

Return to Summary Table

Table 3-3157. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57E0h

Figure 3-1623. CONTROLSS_INTXBAR27_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR27_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR27_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR27_G8_SEL							
R/W							
0h							

Table 3-3158. CONTROLSS_INTXBAR27_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR27_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.280 CONTROLSS_INTXBAR27_G9 Register

3.19.2.280.1 CONTROLSS_INTXBAR27_G9 Register (Offset = 7E4h) [reset = 0h]

INT XBAR 27 Input Select.

Return to Summary Table

Table 3-3159. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 57E4h

Figure 3-1624. CONTROLSS_INTXBAR27_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR27_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR27_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR27_G9_SEL							
R/W							
0h							

Table 3-3160. CONTROLSS_INTXBAR27_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR27_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.281 CONTROLSS_INTXBAR28_G0 Register

3.19.2.281.1 CONTROLSS_INTXBAR28_G0 Register (Offset = 800h) [reset = 0h]

INT XBAR 28 Input Select.

Return to Summary Table

Table 3-3161. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5800h

Figure 3-1625. CONTROLSS_INTXBAR28_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR28_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR28_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR28_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR28_G0_SEL							
R/W							
0h							

Table 3-3162. CONTROLSS_INTXBAR28_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR28_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.282 CONTROLSS_INTXBAR28_G1 Register

3.19.2.282.1 CONTROLSS_INTXBAR28_G1 Register (Offset = 804h) [reset = 0h]

INT XBAR 28 Input Select.

Return to Summary Table

Table 3-3163. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5804h

Figure 3-1626. CONTROLSS_INTXBAR28_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR28_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR28_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR28_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR28_G1_SEL							
R/W							
0h							

Table 3-3164. CONTROLSS_INTXBAR28_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR28_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.283 CONTROLSS_INTXBAR28_G2 Register

3.19.2.283.1 CONTROLSS_INTXBAR28_G2 Register (Offset = 808h) [reset = 0h]

INT XBAR 28 Input Select.

Return to Summary Table

Table 3-3165. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5808h

Figure 3-1627. CONTROLSS_INTXBAR28_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR28_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR28_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR28_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR28_G2_SEL							
R/W							
0h							

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Table 3-3166. CONTROLSS_INTXBAR28_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR28_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.284 CONTROLSS_INTXBAR28_G3 Register

3.19.2.284.1 CONTROLSS_INTXBAR28_G3 Register (Offset = 80Ch) [reset = 0h]

INT XBAR 28 Input Select.

Return to Summary Table

Table 3-3167. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 580Ch

Figure 3-1628. CONTROLSS_INTXBAR28_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR28_G3_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR28_G3_SEL							
R/W							
0h							

Table 3-3168. CONTROLSS_INTXBAR28_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR28_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.285 CONTROLSS_INTXBAR28_G4 Register

3.19.2.285.1 CONTROLSS_INTXBAR28_G4 Register (Offset = 810h) [reset = 0h]

INT XBAR 28 Input Select.

Return to Summary Table

Table 3-3169. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5810h

Figure 3-1629. CONTROLSS_INTXBAR28_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR28_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR28_G4_SEL							
R/W							
0h							

Table 3-3170. CONTROLSS_INTXBAR28_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR28_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.286 CONTROLSS_INTXBAR28_G5 Register

3.19.2.286.1 CONTROLSS_INTXBAR28_G5 Register (Offset = 814h) [reset = 0h]

INT XBAR 28 Input Select.

Return to Summary Table

Table 3-3171. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5814h

Figure 3-1630. CONTROLSS_INTXBAR28_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR28_G5_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR28_G5_SEL							
R/W							
0h							

Table 3-3172. CONTROLSS_INTXBAR28_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR28_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.287 CONTROLSS_INTXBAR28_G6 Register

3.19.2.287.1 CONTROLSS_INTXBAR28_G6 Register (Offset = 818h) [reset = 0h]

INT XBAR 28 Input Select.

Return to Summary Table

Table 3-3173. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5818h

Figure 3-1631. CONTROLSS_INTXBAR28_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR28_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3174. CONTROLSS_INTXBAR28_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR28_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.288 CONTROLSS_INTXBAR28_G7 Register

3.19.2.288.1 CONTROLSS_INTXBAR28_G7 Register (Offset = 81Ch) [reset = 0h]

INT XBAR 28 Input Select.

Return to Summary Table

Table 3-3175. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 581Ch

Figure 3-1632. CONTROLSS_INTXBAR28_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR28_G7_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR28_G7_SEL							
R/W							
0h							

Table 3-3176. CONTROLSS_INTXBAR28_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR28_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.289 CONTROLSS_INTXBAR28_G8 Register

3.19.2.289.1 CONTROLSS_INTXBAR28_G8 Register (Offset = 820h) [reset = 0h]

INT XBAR 28 Input Select.

Return to Summary Table

Table 3-3177. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5820h

Figure 3-1633. CONTROLSS_INTXBAR28_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR28_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR28_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR28_G8_SEL							
R/W							
0h							

Table 3-3178. CONTROLSS_INTXBAR28_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR28_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.290 CONTROLSS_INTXBAR28_G9 Register

3.19.2.290.1 CONTROLSS_INTXBAR28_G9 Register (Offset = 824h) [reset = 0h]

INT XBAR 28 Input Select.

Return to Summary Table

Table 3-3179. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5824h

Figure 3-1634. CONTROLSS_INTXBAR28_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR28_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR28_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR28_G9_SEL							
R/W							
0h							

Table 3-3180. CONTROLSS_INTXBAR28_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR28_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.291 CONTROLSS_INTXBAR29_G0 Register

3.19.2.291.1 CONTROLSS_INTXBAR29_G0 Register (Offset = 840h) [reset = 0h]

INT XBAR 29 Input Select.

Return to Summary Table

Table 3-3181. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5840h

Figure 3-1635. CONTROLSS_INTXBAR29_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR29_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR29_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR29_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR29_G0_SEL							
R/W							
0h							

Table 3-3182. CONTROLSS_INTXBAR29_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR29_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.292 CONTROLSS_INTXBAR29_G1 Register

3.19.2.292.1 CONTROLSS_INTXBAR29_G1 Register (Offset = 844h) [reset = 0h]

INT XBAR 29 Input Select.

Return to Summary Table

Table 3-3183. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5844h

Figure 3-1636. CONTROLSS_INTXBAR29_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR29_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR29_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR29_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR29_G1_SEL							
R/W							
0h							

Table 3-3184. CONTROLSS_INTXBAR29_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR29_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.293 CONTROLSS_INTXBAR29_G2 Register

3.19.2.293.1 CONTROLSS_INTXBAR29_G2 Register (Offset = 848h) [reset = 0h]

INT XBAR 29 Input Select.

Return to Summary Table

Table 3-3185. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5848h

Figure 3-1637. CONTROLSS_INTXBAR29_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR29_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR29_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR29_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR29_G2_SEL							
R/W							
0h							

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Table 3-3186. CONTROLSS_INTXBAR29_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR29_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.294 CONTROLSS_INTXBAR29_G3 Register

3.19.2.294.1 CONTROLSS_INTXBAR29_G3 Register (Offset = 84Ch) [reset = 0h]

INT XBAR 29 Input Select.

Return to Summary Table

Table 3-3187. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 584Ch

Figure 3-1638. CONTROLSS_INTXBAR29_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR29_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR29_G3_SEL							
R/W							
0h							

Table 3-3188. CONTROLSS_INTXBAR29_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR29_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.295 CONTROLSS_INTXBAR29_G4 Register

3.19.2.295.1 CONTROLSS_INTXBAR29_G4 Register (Offset = 850h) [reset = 0h]

INT XBAR 29 Input Select.

Return to Summary Table

Table 3-3189. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5850h

Figure 3-1639. CONTROLSS_INTXBAR29_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR29_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR29_G4_SEL							
R/W							
0h							

Table 3-3190. CONTROLSS_INTXBAR29_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR29_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.296 CONTROLSS_INTXBAR29_G5 Register

3.19.2.296.1 CONTROLSS_INTXBAR29_G5 Register (Offset = 854h) [reset = 0h]

INT XBAR 29 Input Select.

Return to Summary Table

Table 3-3191. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5854h

Figure 3-1640. CONTROLSS_INTXBAR29_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR29_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR29_G5_SEL							
R/W							
0h							

Table 3-3192. CONTROLSS_INTXBAR29_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR29_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.297 CONTROLSS_INTXBAR29_G6 Register

3.19.2.297.1 CONTROLSS_INTXBAR29_G6 Register (Offset = 858h) [reset = 0h]

INT XBAR 29 Input Select.

Return to Summary Table

Table 3-3193. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5858h

Figure 3-1641. CONTROLSS_INTXBAR29_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					INTXBAR29_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3194. CONTROLSS_INTXBAR29_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR29_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.298 CONTROLSS_INTXBAR29_G7 Register

3.19.2.298.1 CONTROLSS_INTXBAR29_G7 Register (Offset = 85Ch) [reset = 0h]

INT XBAR 29 Input Select.

Return to Summary Table

Table 3-3195. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 585Ch

Figure 3-1642. CONTROLSS_INTXBAR29_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR29_G7_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR29_G7_SEL							
R/W							
0h							

Table 3-3196. CONTROLSS_INTXBAR29_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR29_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.299 CONTROLSS_INTXBAR29_G8 Register

3.19.2.299.1 CONTROLSS_INTXBAR29_G8 Register (Offset = 860h) [reset = 0h]

INT XBAR 29 Input Select.

Return to Summary Table

Table 3-3197. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5860h

Figure 3-1643. CONTROLSS_INTXBAR29_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR29_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR29_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR29_G8_SEL							
R/W							
0h							

Table 3-3198. CONTROLSS_INTXBAR29_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR29_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.300 CONTROLSS_INTXBAR29_G9 Register

3.19.2.300.1 CONTROLSS_INTXBAR29_G9 Register (Offset = 864h) [reset = 0h]

INT XBAR 29 Input Select.

Return to Summary Table

Table 3-3199. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5864h

Figure 3-1644. CONTROLSS_INTXBAR29_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR29_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR29_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR29_G9_SEL							
R/W							
0h							

Table 3-3200. CONTROLSS_INTXBAR29_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR29_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.301 CONTROLSS_INTXBAR30_G0 Register

3.19.2.301.1 CONTROLSS_INTXBAR30_G0 Register (Offset = 880h) [reset = 0h]

INT XBAR 30 Input Select.

Return to Summary Table

Table 3-3201. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5880h

Figure 3-1645. CONTROLSS_INTXBAR30_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR30_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR30_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR30_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR30_G0_SEL							
R/W							
0h							

Table 3-3202. CONTROLSS_INTXBAR30_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR30_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.302 CONTROLSS_INTXBAR30_G1 Register

3.19.2.302.1 CONTROLSS_INTXBAR30_G1 Register (Offset = 884h) [reset = 0h]

INT XBAR 30 Input Select.

Return to Summary Table

Table 3-3203. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5884h

Figure 3-1646. CONTROLSS_INTXBAR30_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR30_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR30_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR30_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR30_G1_SEL							
R/W							
0h							

Table 3-3204. CONTROLSS_INTXBAR30_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR30_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.303 CONTROLSS_INTXBAR30_G2 Register

3.19.2.303.1 CONTROLSS_INTXBAR30_G2 Register (Offset = 888h) [reset = 0h]

INT XBAR 30 Input Select.

Return to Summary Table

Table 3-3205. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5888h

Figure 3-1647. CONTROLSS_INTXBAR30_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR30_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR30_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR30_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR30_G2_SEL							
R/W							
0h							

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Table 3-3206. CONTROLSS_INTXBAR30_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR30_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.304 CONTROLSS_INTXBAR30_G3 Register

3.19.2.304.1 CONTROLSS_INTXBAR30_G3 Register (Offset = 88Ch) [reset = 0h]

INT XBAR 30 Input Select.

Return to Summary Table

Table 3-3207. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 588Ch

Figure 3-1648. CONTROLSS_INTXBAR30_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR30_G3_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR30_G3_SEL							
R/W							
0h							

Table 3-3208. CONTROLSS_INTXBAR30_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR30_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.305 CONTROLSS_INTXBAR30_G4 Register

3.19.2.305.1 CONTROLSS_INTXBAR30_G4 Register (Offset = 890h) [reset = 0h]

INT XBAR 30 Input Select.

Return to Summary Table

Table 3-3209. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5890h

Figure 3-1649. CONTROLSS_INTXBAR30_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						INTXBAR30_G4_SEL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR30_G4_SEL							
R/W							
0h							

Table 3-3210. CONTROLSS_INTXBAR30_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR30_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.306 CONTROLSS_INTXBAR30_G5 Register

3.19.2.306.1 CONTROLSS_INTXBAR30_G5 Register (Offset = 894h) [reset = 0h]

INT XBAR 30 Input Select.

Return to Summary Table

Table 3-3211. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5894h

Figure 3-1650. CONTROLSS_INTXBAR30_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR30_G5_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR30_G5_SEL							
R/W							
0h							

Table 3-3212. CONTROLSS_INTXBAR30_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR30_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.307 CONTROLSS_INTXBAR30_G6 Register

3.19.2.307.1 CONTROLSS_INTXBAR30_G6 Register (Offset = 898h) [reset = 0h]

INT XBAR 30 Input Select.

Return to Summary Table

Table 3-3213. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5898h

Figure 3-1651. CONTROLSS_INTXBAR30_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR30_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3214. CONTROLSS_INTXBAR30_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR30_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.308 CONTROLSS_INTXBAR30_G7 Register

3.19.2.308.1 CONTROLSS_INTXBAR30_G7 Register (Offset = 89Ch) [reset = 0h]

INT XBAR 30 Input Select.

Return to Summary Table

Table 3-3215. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 589Ch

Figure 3-1652. CONTROLSS_INTXBAR30_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR30_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR30_G7_SEL							
R/W							
0h							

Table 3-3216. CONTROLSS_INTXBAR30_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR30_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.309 CONTROLSS_INTXBAR30_G8 Register

3.19.2.309.1 CONTROLSS_INTXBAR30_G8 Register (Offset = 8A0h) [reset = 0h]

INT XBAR 30 Input Select.

Return to Summary Table

Table 3-3217. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58A0h

Figure 3-1653. CONTROLSS_INTXBAR30_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR30_G8_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR30_G8_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR30_G8_SEL							
R/W							
0h							

Table 3-3218. CONTROLSS_INTXBAR30_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR30_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.310 CONTROLSS_INTXBAR30_G9 Register

3.19.2.310.1 CONTROLSS_INTXBAR30_G9 Register (Offset = 8A4h) [reset = 0h]

INT XBAR 30 Input Select.

Return to Summary Table

Table 3-3219. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58A4h

Figure 3-1654. CONTROLSS_INTXBAR30_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				INTXBAR30_G9_SEL			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR30_G9_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR30_G9_SEL							
R/W							
0h							

Table 3-3220. CONTROLSS_INTXBAR30_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR30_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.19.2.311 CONTROLSS_INTXBAR31_G0 Register

3.19.2.311.1 CONTROLSS_INTXBAR31_G0 Register (Offset = 8C0h) [reset = 0h]

INT XBAR 31 Input Select.

Return to Summary Table

Table 3-3221. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58C0h

Figure 3-1655. CONTROLSS_INTXBAR31_G0 Name Register

31	30	29	28	27	26	25	24
INTXBAR31_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR31_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR31_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR31_G0_SEL							
R/W							
0h							

Table 3-3222. CONTROLSS_INTXBAR31_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR31_G0_SEL	R/W	0h	EPWM INT interrupt to corresponding XBAR 1:PWMx.INT is selected 0:PWMx.INT is de-selected x can have value from 0 to 31 corresponding to each PWM instance

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3.19.2.312 CONTROLSS_INTXBAR31_G1 Register

3.19.2.312.1 CONTROLSS_INTXBAR31_G1 Register (Offset = 8C4h) [reset = 0h]

INT XBAR 31 Input Select.

Return to Summary Table

Table 3-3223. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58C4h

Figure 3-1656. CONTROLSS_INTXBAR31_G1 Name Register

31	30	29	28	27	26	25	24
INTXBAR31_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR31_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR31_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR31_G1_SEL							
R/W							
0h							

Table 3-3224. CONTROLSS_INTXBAR31_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR31_G1_SEL	R/W	0h	EPWM TZINT interrupt to corresponding XBAR 1:PWMx.TZINT is selected 0:PWMx.TZINT is de-selected

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3.19.2.313 CONTROLSS_INTXBAR31_G2 Register

3.19.2.313.1 CONTROLSS_INTXBAR31_G2 Register (Offset = 8C8h) [reset = 0h]

INT XBAR 31 Input Select.

Return to Summary Table

Table 3-3225. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58C8h

Figure 3-1657. CONTROLSS_INTXBAR31_G2 Name Register

31	30	29	28	27	26	25	24
INTXBAR31_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
INTXBAR31_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
INTXBAR31_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR31_G2_SEL							
R/W							
0h							

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Table 3-3226. CONTROLSS_INTXBAR31_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	INTXBAR31_G2_SEL	R/W	0h	Corresponding INT XBAR G2 Input Select Bit 0:ADC0.INT1 Bit 1:ADC0.INT2 Bit 2:ADC0.INT3 Bit 3:ADC0.INT4 Bit 4:ADC0.EVTINT Bit 5:ADC1.INT1 Bit 6:ADC1.INT2 Bit 7:ADC1.INT3 Bit 8:ADC1.INT4 Bit 9:ADC1.EVTINT Bit 10:ADC2.INT1 Bit 11:ADC2.INT2 Bit 12:ADC2.INT3 Bit 13:ADC2.INT4 Bit 14:ADC2.EVTINT Bit 15:ADC3.INT1 Bit 16:ADC3.INT2 Bit 17:ADC3.INT3 Bit 18:ADC3.INT4 Bit 19:ADC3.EVTINT Bit 20:ADC4.INT1 Bit 21:ADC4.INT2 Bit 22:ADC4.INT3 Bit 23:ADC4.INT4 Bit 24:ADC4.EVTINT Bit 25 30:Reserved Bit 31:ASC_AGG0.INT

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3.19.2.314 CONTROLSS_INTXBAR31_G3 Register

3.19.2.314.1 CONTROLSS_INTXBAR31_G3 Register (Offset = 8CCh) [reset = 0h]

INT XBAR 31 Input Select.

Return to Summary Table

Table 3-3227. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58CCh

Figure 3-1658. CONTROLSS_INTXBAR31_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
INTXBAR31_G3_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR31_G3_SEL							
R/W							
0h							

Table 3-3228. CONTROLSS_INTXBAR31_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR31_G3_SEL	R/W	0h	Corresponding INT XBAR G3 Input Select 0:FSIRX0.INT1N 1:FSIRX0.INT2N 2:FSIRX1.INT1N 3:FSIRX1.INT2N 4:FSIRX2.INT1N 5:FSIRX2.INT2N 6:FSIRX3.INT1N 7:FSIRX3.INT2N 8:FSITX0.INT1N 9:FSITX0.INT2N 10:FSITX1.INT1N 11:FSITX1.INT2N 12:FSITX2.INT1N 13:FSITX2.INT2N 14:FSITX3.INT1N 15:FSITX3.INT2N

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3.19.2.315 CONTROLSS_INTXBAR31_G4 Register

3.19.2.315.1 CONTROLSS_INTXBAR31_G4 Register (Offset = 8D0h) [reset = 0h]

INT XBAR 31 Input Select.

Return to Summary Table

Table 3-3229. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58D0h

Figure 3-1659. CONTROLSS_INTXBAR31_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR31_G4_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR31_G4_SEL							
R/W							
0h							

Table 3-3230. CONTROLSS_INTXBAR31_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR31_G4_SEL	R/W	0h	Corresponding INT XBAR G4 Input Select 0:SD0.ERR 1:SD0.FILT1.DRINT 2:SD0.FILT2.DRINT 3:SD0.FILT3.DRINT 4:SD0.FILT4.DRINT 5:SD1.ERR 6:SD1.FILT1.DRINT 7:SD1.FILT2.DRINT 8:SD1.FILT3.DRINT 9:SD1.FILT4.DRINT

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3.19.2.316 CONTROLSS_INTXBAR31_G5 Register

3.19.2.316.1 CONTROLSS_INTXBAR31_G5 Register (Offset = 8D4h) [reset = 0h]

INT XBAR 31 Input Select.

Return to Summary Table

Table 3-3231. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58D4h

Figure 3-1660. CONTROLSS_INTXBAR31_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INTXBAR31_G5_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTXBAR31_G5_SEL							
R/W							
0h							

Table 3-3232. CONTROLSS_INTXBAR31_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	INTXBAR31_G5_SEL	R/W	0h	Corresponding INT XBAR G5 Input Select 0:ECAP0.INT 1:ECAP1.INT 2:ECAP2.INT 3:ECAP3.INT 4:ECAP4.INT 5:ECAP5.INT 6:ECAP6.INT 7:ECAP7.INT 8:ECAP8.INT 9:ECAP9.INT 10:ECAP10.INT 11:ECAP11.INT 12:ECAP12.INT 13:ECAP13.INT 14:ECAP14.INT 15:ECAP15.INT

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3.19.2.317 CONTROLSS_INTXBAR31_G6 Register

3.19.2.317.1 CONTROLSS_INTXBAR31_G6 Register (Offset = 8D8h) [reset = 0h]

INT XBAR 31 Input Select.

Return to Summary Table

Table 3-3233. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58D8h

Figure 3-1661. CONTROLSS_INTXBAR31_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					INTXBAR31_G6_SEL		
NONE					R/W		
0h					0h		

Table 3-3234. CONTROLSS_INTXBAR31_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	INTXBAR31_G6_SEL	R/W	0h	Corresponding INT XBAR G6 Input Select 0:EQEP0.INT 1:EQEP1.INT 2:EQEP2.INT

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3.19.2.318 CONTROLSS_INTXBAR31_G7 Register

3.19.2.318.1 CONTROLSS_INTXBAR31_G7 Register (Offset = 8DCh) [reset = 0h]

INT XBAR 31 Input Select.

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Table 3-3235. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58DCh

Figure 3-1662. CONTROLSS_INTXBAR31_G7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						INTXBAR31_G7_SEL	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
INTXBAR31_G7_SEL							
R/W							
0h							

Table 3-3236. CONTROLSS_INTXBAR31_G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	INTXBAR31_G7_SEL	R/W	0h	Corresponding INT XBAR G7 Input Select Bit 0:ADCR0.INT1 Bit 1:ADCR0.INT2 Bit 2:ADCR0.INT3 Bit 3:ADCR0.INT4 Bit 4:ADCR0.EVTINT Bit 5:ADCR1.INT1 Bit 6:ADCR1.INT2 Bit 7:ADCR1.INT3 Bit 8:ADCR1.INT4 Bit 9:ADCR1.EVTINT Bit 10 31:Reserved

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3.19.2.319 CONTROLSS_INTXBAR31_G8 Register

3.19.2.319.1 CONTROLSS_INTXBAR31_G8 Register (Offset = 8E0h) [reset = 0h]

INT XBAR 31 Input Select.

Return to Summary Table

Table 3-3237. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58E0h

Figure 3-1663. CONTROLSS_INTXBAR31_G8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR31_G8_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR31_G8_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR31_G8_SEL							
R/W							
0h							

Table 3-3238. CONTROLSS_INTXBAR31_G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR31_G8_SEL	R/W	0h	Corresponding INT XBAR G8 Input Select 0:CMP12SSA0.CTRIPL 1:CMP12SSA0.CTRIPH 2:CMP12SSA1.CTRIPL 3:CMP12SSA1.CTRIPH 4:CMP12SSA2.CTRIPL 5:CMP12SSA2.CTRIPH 6:CMP12SSA3.CTRIPL 7:CMP12SSA3.CTRIPH 8:CMP12SSA4.CTRIPL 9:CMP12SSA4.CTRIPH 10:CMP12SSA5.CTRIPL 11:CMP12SSA5.CTRIPH 12:CMP12SSA6.CTRIPL 13:CMP12SSA6.CTRIPH 14:CMP12SSA7.CTRIPL 15:CMP12SSA7.CTRIPH 16:CMP12SSA8.CTRIPL 17:CMP12SSA8.CTRIPH 18:CMP12SSA9.CTRIPL 19:CMP12SSA9.CTRIPH

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3.19.2.320 CONTROLSS_INTXBAR31_G9 Register

3.19.2.320.1 CONTROLSS_INTXBAR31_G9 Register (Offset = 8E4h) [reset = 0h]

INT XBAR 31 Input Select.

Return to Summary Table

Table 3-3239. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 58E4h

Figure 3-1664. CONTROLSS_INTXBAR31_G9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				INTXBAR31_G9_SEL			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
INTXBAR31_G9_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
INTXBAR31_G9_SEL							
R/W							
0h							

Table 3-3240. CONTROLSS_INTXBAR31_G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	INTXBAR31_G9_SEL	R/W	0h	Corresponding INT XBAR G9 Input Select 0:CMP12SSB0.CTRIPL 1:CMP12SSB0.CTRIPH 2:CMP12SSB1.CTRIPL 3:CMP12SSB1.CTRIPH 4:CMP12SSB2.CTRIPL 5:CMP12SSB2.CTRIPH 6:CMP12SSB3.CTRIPL 7:CMP12SSB3.CTRIPH 8:CMP12SSB4.CTRIPL 9:CMP12SSB4.CTRIPH 10:CMP12SSB5.CTRIPL 11:CMP12SSB5.CTRIPH 12:CMP12SSB6.CTRIPL 13:CMP12SSB6.CTRIPH 14:CMP12SSB7.CTRIPL 15:CMP12SSB7.CTRIPH 16:CMP12SSB8.CTRIPL 17:CMP12SSB8.CTRIPH 18:CMP12SSB9.CTRIPL 19:CMP12SSB9.CTRIPH

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3.20 CONTROLSS_INPUTXBAR

CONTROLSS_INPUTXBAR

3.20.1 CONTROLSS_INPUTXBAR Summaries

CONTROLSS_INPUTXBAR Summaries

Table 3-3241. CONTROLSS Registers, Base Address=502D 0000h, Length=4096

Offset	Length	Register Name	CONTROLSS_INPUTXBAR Physical Address
100h	32	CONTROLSS_INPUTXBAR0_GSEL	502D 0100h
104h	32	CONTROLSS_INPUTXBAR0_G0	502D 0104h
108h	32	CONTROLSS_INPUTXBAR0_G1	502D 0108h
10Ch	32	CONTROLSS_INPUTXBAR0_G2	502D 010Ch
140h	32	CONTROLSS_INPUTXBAR1_GSEL	502D 0140h
144h	32	CONTROLSS_INPUTXBAR1_G0	502D 0144h
148h	32	CONTROLSS_INPUTXBAR1_G1	502D 0148h
14Ch	32	CONTROLSS_INPUTXBAR1_G2	502D 014Ch
180h	32	CONTROLSS_INPUTXBAR2_GSEL	502D 0180h
184h	32	CONTROLSS_INPUTXBAR2_G0	502D 0184h
188h	32	CONTROLSS_INPUTXBAR2_G1	502D 0188h
18Ch	32	CONTROLSS_INPUTXBAR2_G2	502D 018Ch
1C0h	32	CONTROLSS_INPUTXBAR3_GSEL	502D 01C0h
1C4h	32	CONTROLSS_INPUTXBAR3_G0	502D 01C4h
1C8h	32	CONTROLSS_INPUTXBAR3_G1	502D 01C8h
1CCh	32	CONTROLSS_INPUTXBAR3_G2	502D 01CCh
200h	32	CONTROLSS_INPUTXBAR4_GSEL	502D 0200h
204h	32	CONTROLSS_INPUTXBAR4_G0	502D 0204h
208h	32	CONTROLSS_INPUTXBAR4_G1	502D 0208h
20Ch	32	CONTROLSS_INPUTXBAR4_G2	502D 020Ch
240h	32	CONTROLSS_INPUTXBAR5_GSEL	502D 0240h
244h	32	CONTROLSS_INPUTXBAR5_G0	502D 0244h
248h	32	CONTROLSS_INPUTXBAR5_G1	502D 0248h
24Ch	32	CONTROLSS_INPUTXBAR5_G2	502D 024Ch
280h	32	CONTROLSS_INPUTXBAR6_GSEL	502D 0280h
284h	32	CONTROLSS_INPUTXBAR6_G0	502D 0284h
288h	32	CONTROLSS_INPUTXBAR6_G1	502D 0288h
28Ch	32	CONTROLSS_INPUTXBAR6_G2	502D 028Ch
2C0h	32	CONTROLSS_INPUTXBAR7_GSEL	502D 02C0h
2C4h	32	CONTROLSS_INPUTXBAR7_G0	502D 02C4h
2C8h	32	CONTROLSS_INPUTXBAR7_G1	502D 02C8h
2CCh	32	CONTROLSS_INPUTXBAR7_G2	502D 02CCh
300h	32	CONTROLSS_INPUTXBAR8_GSEL	502D 0300h
304h	32	CONTROLSS_INPUTXBAR8_G0	502D 0304h
308h	32	CONTROLSS_INPUTXBAR8_G1	502D 0308h
30Ch	32	CONTROLSS_INPUTXBAR8_G2	502D 030Ch
340h	32	CONTROLSS_INPUTXBAR9_GSEL	502D 0340h
344h	32	CONTROLSS_INPUTXBAR9_G0	502D 0344h
348h	32	CONTROLSS_INPUTXBAR9_G1	502D 0348h

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Table 3-3241. CONTROLSS Registers, Base Address=502D 0000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_INPUTXBAR Physical Address
34Ch	32	CONTROLSS_INPUTXBAR9_G2	502D 034Ch
380h	32	CONTROLSS_INPUTXBAR10_GSEL	502D 0380h
384h	32	CONTROLSS_INPUTXBAR10_G0	502D 0384h
388h	32	CONTROLSS_INPUTXBAR10_G1	502D 0388h
38Ch	32	CONTROLSS_INPUTXBAR10_G2	502D 038Ch
3C0h	32	CONTROLSS_INPUTXBAR11_GSEL	502D 03C0h
3C4h	32	CONTROLSS_INPUTXBAR11_G0	502D 03C4h
3C8h	32	CONTROLSS_INPUTXBAR11_G1	502D 03C8h
3CCh	32	CONTROLSS_INPUTXBAR11_G2	502D 03CCh
400h	32	CONTROLSS_INPUTXBAR12_GSEL	502D 0400h
404h	32	CONTROLSS_INPUTXBAR12_G0	502D 0404h
408h	32	CONTROLSS_INPUTXBAR12_G1	502D 0408h
40Ch	32	CONTROLSS_INPUTXBAR12_G2	502D 040Ch
440h	32	CONTROLSS_INPUTXBAR13_GSEL	502D 0440h
444h	32	CONTROLSS_INPUTXBAR13_G0	502D 0444h
448h	32	CONTROLSS_INPUTXBAR13_G1	502D 0448h
44Ch	32	CONTROLSS_INPUTXBAR13_G2	502D 044Ch
480h	32	CONTROLSS_INPUTXBAR14_GSEL	502D 0480h
484h	32	CONTROLSS_INPUTXBAR14_G0	502D 0484h
488h	32	CONTROLSS_INPUTXBAR14_G1	502D 0488h
48Ch	32	CONTROLSS_INPUTXBAR14_G2	502D 048Ch
4C0h	32	CONTROLSS_INPUTXBAR15_GSEL	502D 04C0h
4C4h	32	CONTROLSS_INPUTXBAR15_G0	502D 04C4h
4C8h	32	CONTROLSS_INPUTXBAR15_G1	502D 04C8h
4CCh	32	CONTROLSS_INPUTXBAR15_G2	502D 04CCh
500h	32	CONTROLSS_INPUTXBAR16_GSEL	502D 0500h
504h	32	CONTROLSS_INPUTXBAR16_G0	502D 0504h
508h	32	CONTROLSS_INPUTXBAR16_G1	502D 0508h
50Ch	32	CONTROLSS_INPUTXBAR16_G2	502D 050Ch
540h	32	CONTROLSS_INPUTXBAR17_GSEL	502D 0540h
544h	32	CONTROLSS_INPUTXBAR17_G0	502D 0544h
548h	32	CONTROLSS_INPUTXBAR17_G1	502D 0548h
54Ch	32	CONTROLSS_INPUTXBAR17_G2	502D 054Ch
580h	32	CONTROLSS_INPUTXBAR18_GSEL	502D 0580h
584h	32	CONTROLSS_INPUTXBAR18_G0	502D 0584h
588h	32	CONTROLSS_INPUTXBAR18_G1	502D 0588h
58Ch	32	CONTROLSS_INPUTXBAR18_G2	502D 058Ch
5C0h	32	CONTROLSS_INPUTXBAR19_GSEL	502D 05C0h
5C4h	32	CONTROLSS_INPUTXBAR19_G0	502D 05C4h
5C8h	32	CONTROLSS_INPUTXBAR19_G1	502D 05C8h
5CCh	32	CONTROLSS_INPUTXBAR19_G2	502D 05CCh
600h	32	CONTROLSS_INPUTXBAR20_GSEL	502D 0600h
604h	32	CONTROLSS_INPUTXBAR20_G0	502D 0604h
608h	32	CONTROLSS_INPUTXBAR20_G1	502D 0608h
60Ch	32	CONTROLSS_INPUTXBAR20_G2	502D 060Ch
640h	32	CONTROLSS_INPUTXBAR21_GSEL	502D 0640h

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Table 3-3241. CONTROLSS Registers, Base Address=502D 0000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_INPUTXBAR Physical Address
644h	32	CONTROLSS_INPUTXBAR21_G0	502D 0644h
648h	32	CONTROLSS_INPUTXBAR21_G1	502D 0648h
64Ch	32	CONTROLSS_INPUTXBAR21_G2	502D 064Ch
680h	32	CONTROLSS_INPUTXBAR22_GSEL	502D 0680h
684h	32	CONTROLSS_INPUTXBAR22_G0	502D 0684h
688h	32	CONTROLSS_INPUTXBAR22_G1	502D 0688h
68Ch	32	CONTROLSS_INPUTXBAR22_G2	502D 068Ch
6C0h	32	CONTROLSS_INPUTXBAR23_GSEL	502D 06C0h
6C4h	32	CONTROLSS_INPUTXBAR23_G0	502D 06C4h
6C8h	32	CONTROLSS_INPUTXBAR23_G1	502D 06C8h
6CCh	32	CONTROLSS_INPUTXBAR23_G2	502D 06CCh
700h	32	CONTROLSS_INPUTXBAR24_GSEL	502D 0700h
704h	32	CONTROLSS_INPUTXBAR24_G0	502D 0704h
708h	32	CONTROLSS_INPUTXBAR24_G1	502D 0708h
70Ch	32	CONTROLSS_INPUTXBAR24_G2	502D 070Ch
740h	32	CONTROLSS_INPUTXBAR25_GSEL	502D 0740h
744h	32	CONTROLSS_INPUTXBAR25_G0	502D 0744h
748h	32	CONTROLSS_INPUTXBAR25_G1	502D 0748h
74Ch	32	CONTROLSS_INPUTXBAR25_G2	502D 074Ch
780h	32	CONTROLSS_INPUTXBAR26_GSEL	502D 0780h
784h	32	CONTROLSS_INPUTXBAR26_G0	502D 0784h
788h	32	CONTROLSS_INPUTXBAR26_G1	502D 0788h
78Ch	32	CONTROLSS_INPUTXBAR26_G2	502D 078Ch
7C0h	32	CONTROLSS_INPUTXBAR27_GSEL	502D 07C0h
7C4h	32	CONTROLSS_INPUTXBAR27_G0	502D 07C4h
7C8h	32	CONTROLSS_INPUTXBAR27_G1	502D 07C8h
7CCh	32	CONTROLSS_INPUTXBAR27_G2	502D 07CCh
800h	32	CONTROLSS_INPUTXBAR28_GSEL	502D 0800h
804h	32	CONTROLSS_INPUTXBAR28_G0	502D 0804h
808h	32	CONTROLSS_INPUTXBAR28_G1	502D 0808h
80Ch	32	CONTROLSS_INPUTXBAR28_G2	502D 080Ch
840h	32	CONTROLSS_INPUTXBAR29_GSEL	502D 0840h
844h	32	CONTROLSS_INPUTXBAR29_G0	502D 0844h
848h	32	CONTROLSS_INPUTXBAR29_G1	502D 0848h
84Ch	32	CONTROLSS_INPUTXBAR29_G2	502D 084Ch
880h	32	CONTROLSS_INPUTXBAR30_GSEL	502D 0880h
884h	32	CONTROLSS_INPUTXBAR30_G0	502D 0884h
888h	32	CONTROLSS_INPUTXBAR30_G1	502D 0888h
88Ch	32	CONTROLSS_INPUTXBAR30_G2	502D 088Ch
8C0h	32	CONTROLSS_INPUTXBAR31_GSEL	502D 08C0h
8C4h	32	CONTROLSS_INPUTXBAR31_G0	502D 08C4h
8C8h	32	CONTROLSS_INPUTXBAR31_G1	502D 08C8h
8CCh	32	CONTROLSS_INPUTXBAR31_G2	502D 08CCh

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3.20.2 CONTROLSS_INPUTXBAR Registers

CONTROLSS_INPUTXBAR Registers

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3.20.2.1 CONTROLSS_INPUTXBAR0_GSEL Register

3.20.2.1.1 CONTROLSS_INPUTXBAR0_GSEL Register (Offset = 100h) [reset = 0h]

INPUT XBAR0 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3242. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0100h

Figure 3-1665. CONTROLSS_INPUTXBAR0_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						INPUTXBAR0_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3243. CONTROLSS_INPUTXBAR0_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR0_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.2 CONTROLSS_INPUTXBAR0_G0 Register

3.20.2.2.1 CONTROLSS_INPUTXBAR0_G0 Register (Offset = 104h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3244. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0104h

Figure 3-1666. CONTROLSS_INPUTXBAR0_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR0_G0_SEL							
R/W							
0h							

Table 3-3245. CONTROLSS_INPUTXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR0_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.3 CONTROLSS_INPUTXBAR0_G1 Register

3.20.2.3.1 CONTROLSS_INPUTXBAR0_G1 Register (Offset = 108h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3246. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0108h

Figure 3-1667. CONTROLSS_INPUTXBAR0_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR0_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3247. CONTROLSS_INPUTXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR0_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.4 CONTROLSS_INPUTXBAR0_G2 Register

3.20.2.4.1 CONTROLSS_INPUTXBAR0_G2 Register (Offset = 10Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3248. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 010Ch

Figure 3-1668. CONTROLSS_INPUTXBAR0_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR0_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3249. CONTROLSS_INPUTXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR0_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.5 CONTROLSS_INPUTXBAR1_GSEL Register

3.20.2.5.1 CONTROLSS_INPUTXBAR1_GSEL Register (Offset = 140h) [reset = 0h]

INPUT XBAR1 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3250. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0140h

Figure 3-1669. CONTROLSS_INPUTXBAR1_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR1_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3251. CONTROLSS_INPUTXBAR1_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR1_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.6 CONTROLSS_INPUTXBAR1_G0 Register

3.20.2.6.1 CONTROLSS_INPUTXBAR1_G0 Register (Offset = 144h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3252. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0144h

Figure 3-1670. CONTROLSS_INPUTXBAR1_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR1_G0_SEL							
R/W							
0h							

Table 3-3253. CONTROLSS_INPUTXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR1_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.7 CONTROLSS_INPUTXBAR1_G1 Register

3.20.2.7.1 CONTROLSS_INPUTXBAR1_G1 Register (Offset = 148h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3254. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0148h

Figure 3-1671. CONTROLSS_INPUTXBAR1_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR1_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3255. CONTROLSS_INPUTXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR1_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.8 CONTROLSS_INPUTXBAR1_G2 Register

3.20.2.8.1 CONTROLSS_INPUTXBAR1_G2 Register (Offset = 14Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3256. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 014Ch

Figure 3-1672. CONTROLSS_INPUTXBAR1_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR1_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3257. CONTROLSS_INPUTXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR1_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.9 CONTROLSS_INPUTXBAR2_GSEL Register

3.20.2.9.1 CONTROLSS_INPUTXBAR2_GSEL Register (Offset = 180h) [reset = 0h]

INPUT XBAR2 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3258. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0180h

Figure 3-1673. CONTROLSS_INPUTXBAR2_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR2_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3259. CONTROLSS_INPUTXBAR2_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR2_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.10 CONTROLSS_INPUTXBAR2_G0 Register

3.20.2.10.1 CONTROLSS_INPUTXBAR2_G0 Register (Offset = 184h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3260. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0184h

Figure 3-1674. CONTROLSS_INPUTXBAR2_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR2_G0_SEL							
R/W							
0h							

Table 3-3261. CONTROLSS_INPUTXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR2_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.11 CONTROLSS_INPUTXBAR2_G1 Register

3.20.2.11.1 CONTROLSS_INPUTXBAR2_G1 Register (Offset = 188h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3262. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0188h

Figure 3-1675. CONTROLSS_INPUTXBAR2_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR2_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3263. CONTROLSS_INPUTXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR2_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.12 CONTROLSS_INPUTXBAR2_G2 Register

3.20.2.12.1 CONTROLSS_INPUTXBAR2_G2 Register (Offset = 18Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3264. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 018Ch

Figure 3-1676. CONTROLSS_INPUTXBAR2_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR2_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3265. CONTROLSS_INPUTXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR2_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.13 CONTROLSS_INPUTXBAR3_GSEL Register

3.20.2.13.1 CONTROLSS_INPUTXBAR3_GSEL Register (Offset = 1C0h) [reset = 0h]

INPUT XBAR3 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3266. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 01C0h

Figure 3-1677. CONTROLSS_INPUTXBAR3_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR3_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3267. CONTROLSS_INPUTXBAR3_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR3_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.14 CONTROLSS_INPUTXBAR3_G0 Register

3.20.2.14.1 CONTROLSS_INPUTXBAR3_G0 Register (Offset = 1C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3268. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 01C4h

Figure 3-1678. CONTROLSS_INPUTXBAR3_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR3_G0_SEL							
R/W							
0h							

Table 3-3269. CONTROLSS_INPUTXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR3_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.15 CONTROLSS_INPUTXBAR3_G1 Register

3.20.2.15.1 CONTROLSS_INPUTXBAR3_G1 Register (Offset = 1C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3270. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 01C8h

Figure 3-1679. CONTROLSS_INPUTXBAR3_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR3_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3271. CONTROLSS_INPUTXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR3_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.16 CONTROLSS_INPUTXBAR3_G2 Register

3.20.2.16.1 CONTROLSS_INPUTXBAR3_G2 Register (Offset = 1CCh) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3272. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 01CCh

Figure 3-1680. CONTROLSS_INPUTXBAR3_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR3_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3273. CONTROLSS_INPUTXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR3_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.17 CONTROLSS_INPUTXBAR4_GSEL Register

3.20.2.17.1 CONTROLSS_INPUTXBAR4_GSEL Register (Offset = 200h) [reset = 0h]

INPUT XBAR4 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3274. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0200h

Figure 3-1681. CONTROLSS_INPUTXBAR4_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR4_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3275. CONTROLSS_INPUTXBAR4_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR4_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.18 CONTROLSS_INPUTXBAR4_G0 Register

3.20.2.18.1 CONTROLSS_INPUTXBAR4_G0 Register (Offset = 204h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3276. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0204h

Figure 3-1682. CONTROLSS_INPUTXBAR4_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR4_G0_SEL							
R/W							
0h							

Table 3-3277. CONTROLSS_INPUTXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR4_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.19 CONTROLSS_INPUTXBAR4_G1 Register

3.20.2.19.1 CONTROLSS_INPUTXBAR4_G1 Register (Offset = 208h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3278. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0208h

Figure 3-1683. CONTROLSS_INPUTXBAR4_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR4_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3279. CONTROLSS_INPUTXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR4_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.20 CONTROLSS_INPUTXBAR4_G2 Register

3.20.2.20.1 CONTROLSS_INPUTXBAR4_G2 Register (Offset = 20Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3280. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 020Ch

Figure 3-1684. CONTROLSS_INPUTXBAR4_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR4_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3281. CONTROLSS_INPUTXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR4_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.21 CONTROLSS_INPUTXBAR5_GSEL Register

3.20.2.21.1 CONTROLSS_INPUTXBAR5_GSEL Register (Offset = 240h) [reset = 0h]

INPUT XBAR5 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3282. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0240h

Figure 3-1685. CONTROLSS_INPUTXBAR5_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR5_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3283. CONTROLSS_INPUTXBAR5_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR5_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.22 CONTROLSS_INPUTXBAR5_G0 Register

3.20.2.22.1 CONTROLSS_INPUTXBAR5_G0 Register (Offset = 244h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3284. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0244h

Figure 3-1686. CONTROLSS_INPUTXBAR5_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR5_G0_SEL							
R/W							
0h							

Table 3-3285. CONTROLSS_INPUTXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR5_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.23 CONTROLSS_INPUTXBAR5_G1 Register

3.20.2.23.1 CONTROLSS_INPUTXBAR5_G1 Register (Offset = 248h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3286. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0248h

Figure 3-1687. CONTROLSS_INPUTXBAR5_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR5_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3287. CONTROLSS_INPUTXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR5_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.24 CONTROLSS_INPUTXBAR5_G2 Register

3.20.2.24.1 CONTROLSS_INPUTXBAR5_G2 Register (Offset = 24Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3288. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 024Ch

Figure 3-1688. CONTROLSS_INPUTXBAR5_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR5_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3289. CONTROLSS_INPUTXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR5_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.25 CONTROLSS_INPUTXBAR6_GSEL Register

3.20.2.25.1 CONTROLSS_INPUTXBAR6_GSEL Register (Offset = 280h) [reset = 0h]

INPUT XBAR6 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3290. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0280h

Figure 3-1689. CONTROLSS_INPUTXBAR6_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						INPUTXBAR6_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3291. CONTROLSS_INPUTXBAR6_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR6_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.26 CONTROLSS_INPUTXBAR6_G0 Register

3.20.2.26.1 CONTROLSS_INPUTXBAR6_G0 Register (Offset = 284h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3292. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0284h

Figure 3-1690. CONTROLSS_INPUTXBAR6_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INPUTXBAR6_G0_SEL							
R/W							
0h							

Table 3-3293. CONTROLSS_INPUTXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR6_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.27 CONTROLSS_INPUTXBAR6_G1 Register

3.20.2.27.1 CONTROLSS_INPUTXBAR6_G1 Register (Offset = 288h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3294. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0288h

Figure 3-1691. CONTROLSS_INPUTXBAR6_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR6_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3295. CONTROLSS_INPUTXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR6_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.28 CONTROLSS_INPUTXBAR6_G2 Register

3.20.2.28.1 CONTROLSS_INPUTXBAR6_G2 Register (Offset = 28Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3296. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 028Ch

Figure 3-1692. CONTROLSS_INPUTXBAR6_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR6_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3297. CONTROLSS_INPUTXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR6_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.29 CONTROLSS_INPUTXBAR7_GSEL Register

3.20.2.29.1 CONTROLSS_INPUTXBAR7_GSEL Register (Offset = 2C0h) [reset = 0h]

INPUT XBAR7 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3298. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 02C0h

Figure 3-1693. CONTROLSS_INPUTXBAR7_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR7_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3299. CONTROLSS_INPUTXBAR7_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR7_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.30 CONTROLSS_INPUTXBAR7_G0 Register

3.20.2.30.1 CONTROLSS_INPUTXBAR7_G0 Register (Offset = 2C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3300. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 02C4h

Figure 3-1694. CONTROLSS_INPUTXBAR7_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR7_G0_SEL							
R/W							
0h							

Table 3-3301. CONTROLSS_INPUTXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR7_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.31 CONTROLSS_INPUTXBAR7_G1 Register

3.20.2.31.1 CONTROLSS_INPUTXBAR7_G1 Register (Offset = 2C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3302. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 02C8h

Figure 3-1695. CONTROLSS_INPUTXBAR7_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR7_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3303. CONTROLSS_INPUTXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR7_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.32 CONTROLSS_INPUTXBAR7_G2 Register

3.20.2.32.1 CONTROLSS_INPUTXBAR7_G2 Register (Offset = 2CCh) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3304. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 02CCh

Figure 3-1696. CONTROLSS_INPUTXBAR7_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR7_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3305. CONTROLSS_INPUTXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR7_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.33 CONTROLSS_INPUTXBAR8_GSEL Register

3.20.2.33.1 CONTROLSS_INPUTXBAR8_GSEL Register (Offset = 300h) [reset = 0h]

INPUT XBAR8 Input Select
0 : GPI
1: ICSS GPO port.

Return to Summary Table

Table 3-3306. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0300h

Figure 3-1697. CONTROLSS_INPUTXBAR8_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR8_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3307. CONTROLSS_INPUTXBAR8_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR8_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.34 CONTROLSS_INPUTXBAR8_G0 Register

3.20.2.34.1 CONTROLSS_INPUTXBAR8_G0 Register (Offset = 304h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3308. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0304h

Figure 3-1698. CONTROLSS_INPUTXBAR8_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR8_G0_SEL							
R/W							
0h							

Table 3-3309. CONTROLSS_INPUTXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR8_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.35 CONTROLSS_INPUTXBAR8_G1 Register

3.20.2.35.1 CONTROLSS_INPUTXBAR8_G1 Register (Offset = 308h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3310. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0308h

Figure 3-1699. CONTROLSS_INPUTXBAR8_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR8_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3311. CONTROLSS_INPUTXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR8_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.36 CONTROLSS_INPUTXBAR8_G2 Register

3.20.2.36.1 CONTROLSS_INPUTXBAR8_G2 Register (Offset = 30Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3312. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 030Ch

Figure 3-1700. CONTROLSS_INPUTXBAR8_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR8_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3313. CONTROLSS_INPUTXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR8_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.37 CONTROLSS_INPUTXBAR9_GSEL Register

3.20.2.37.1 CONTROLSS_INPUTXBAR9_GSEL Register (Offset = 340h) [reset = 0h]

INPUT XBAR9 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3314. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0340h

Figure 3-1701. CONTROLSS_INPUTXBAR9_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						INPUTXBAR9_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3315. CONTROLSS_INPUTXBAR9_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR9_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.38 CONTROLSS_INPUTXBAR9_G0 Register

3.20.2.38.1 CONTROLSS_INPUTXBAR9_G0 Register (Offset = 344h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3316. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0344h

Figure 3-1702. CONTROLSS_INPUTXBAR9_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR9_G0_SEL							
R/W							
0h							

Table 3-3317. CONTROLSS_INPUTXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR9_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.39 CONTROLSS_INPUTXBAR9_G1 Register

3.20.2.39.1 CONTROLSS_INPUTXBAR9_G1 Register (Offset = 348h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3318. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0348h

Figure 3-1703. CONTROLSS_INPUTXBAR9_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR9_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3319. CONTROLSS_INPUTXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR9_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.40 CONTROLSS_INPUTXBAR9_G2 Register

3.20.2.40.1 CONTROLSS_INPUTXBAR9_G2 Register (Offset = 34Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3320. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 034Ch

Figure 3-1704. CONTROLSS_INPUTXBAR9_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR9_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3321. CONTROLSS_INPUTXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR9_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.41 CONTROLSS_INPUTXBAR10_GSEL Register

3.20.2.41.1 CONTROLSS_INPUTXBAR10_GSEL Register (Offset = 380h) [reset = 0h]

INPUT XBAR10 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3322. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0380h

Figure 3-1705. CONTROLSS_INPUTXBAR10_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						INPUTXBAR10_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3323. CONTROLSS_INPUTXBAR10_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR10_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.42 CONTROLSS_INPUTXBAR10_G0 Register

3.20.2.42.1 CONTROLSS_INPUTXBAR10_G0 Register (Offset = 384h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3324. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0384h

Figure 3-1706. CONTROLSS_INPUTXBAR10_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR10_G0_SEL							
R/W							
0h							

Table 3-3325. CONTROLSS_INPUTXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR10_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.43 CONTROLSS_INPUTXBAR10_G1 Register

3.20.2.43.1 CONTROLSS_INPUTXBAR10_G1 Register (Offset = 388h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3326. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0388h

Figure 3-1707. CONTROLSS_INPUTXBAR10_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR10_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3327. CONTROLSS_INPUTXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR10_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.44 CONTROLSS_INPUTXBAR10_G2 Register

3.20.2.44.1 CONTROLSS_INPUTXBAR10_G2 Register (Offset = 38Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3328. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 038Ch

Figure 3-1708. CONTROLSS_INPUTXBAR10_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR10_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3329. CONTROLSS_INPUTXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR10_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.45 CONTROLSS_INPUTXBAR11_GSEL Register

3.20.2.45.1 CONTROLSS_INPUTXBAR11_GSEL Register (Offset = 3C0h) [reset = 0h]

INPUT XBAR11 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3330. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 03C0h

Figure 3-1709. CONTROLSS_INPUTXBAR11_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR11_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3331. CONTROLSS_INPUTXBAR11_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR11_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.46 CONTROLSS_INPUTXBAR11_G0 Register

3.20.2.46.1 CONTROLSS_INPUTXBAR11_G0 Register (Offset = 3C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3332. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 03C4h

Figure 3-1710. CONTROLSS_INPUTXBAR11_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR11_G0_SEL							
R/W							
0h							

Table 3-3333. CONTROLSS_INPUTXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR11_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.47 CONTROLSS_INPUTXBAR11_G1 Register

3.20.2.47.1 CONTROLSS_INPUTXBAR11_G1 Register (Offset = 3C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3334. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 03C8h

Figure 3-1711. CONTROLSS_INPUTXBAR11_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR11_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3335. CONTROLSS_INPUTXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR11_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.48 CONTROLSS_INPUTXBAR11_G2 Register

3.20.2.48.1 CONTROLSS_INPUTXBAR11_G2 Register (Offset = 3CCh) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3336. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 03CCh

Figure 3-1712. CONTROLSS_INPUTXBAR11_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR11_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3337. CONTROLSS_INPUTXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR11_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.49 CONTROLSS_INPUTXBAR12_GSEL Register

3.20.2.49.1 CONTROLSS_INPUTXBAR12_GSEL Register (Offset = 400h) [reset = 0h]

INPUT XBAR12 Input Select
0 : GPI
1: ICSS GPO port.

Return to Summary Table

Table 3-3338. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0400h

Figure 3-1713. CONTROLSS_INPUTXBAR12_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR12_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3339. CONTROLSS_INPUTXBAR12_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR12_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.50 CONTROLSS_INPUTXBAR12_G0 Register

3.20.2.50.1 CONTROLSS_INPUTXBAR12_G0 Register (Offset = 404h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to Summary Table

Table 3-3340. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0404h

Figure 3-1714. CONTROLSS_INPUTXBAR12_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR12_G0_SEL							
R/W							
0h							

Table 3-3341. CONTROLSS_INPUTXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR12_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.51 CONTROLSS_INPUTXBAR12_G1 Register

3.20.2.51.1 CONTROLSS_INPUTXBAR12_G1 Register (Offset = 408h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3342. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0408h

Figure 3-1715. CONTROLSS_INPUTXBAR12_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR12_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3343. CONTROLSS_INPUTXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR12_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.52 CONTROLSS_INPUTXBAR12_G2 Register

3.20.2.52.1 CONTROLSS_INPUTXBAR12_G2 Register (Offset = 40Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3344. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 040Ch

Figure 3-1716. CONTROLSS_INPUTXBAR12_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR12_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3345. CONTROLSS_INPUTXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR12_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.53 CONTROLSS_INPUTXBAR13_GSEL Register

3.20.2.53.1 CONTROLSS_INPUTXBAR13_GSEL Register (Offset = 440h) [reset = 0h]

INPUT XBAR13 Input Select
0 : GPI
1: ICSS GPO port.

Return to Summary Table

Table 3-3346. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0440h

Figure 3-1717. CONTROLSS_INPUTXBAR13_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						INPUTXBAR13_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3347. CONTROLSS_INPUTXBAR13_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR13_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.54 CONTROLSS_INPUTXBAR13_G0 Register

3.20.2.54.1 CONTROLSS_INPUTXBAR13_G0 Register (Offset = 444h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3348. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0444h

Figure 3-1718. CONTROLSS_INPUTXBAR13_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR13_G0_SEL							
R/W							
0h							

Table 3-3349. CONTROLSS_INPUTXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR13_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.55 CONTROLSS_INPUTXBAR13_G1 Register

3.20.2.55.1 CONTROLSS_INPUTXBAR13_G1 Register (Offset = 448h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3350. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0448h

Figure 3-1719. CONTROLSS_INPUTXBAR13_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR13_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3351. CONTROLSS_INPUTXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR13_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.56 CONTROLSS_INPUTXBAR13_G2 Register

3.20.2.56.1 CONTROLSS_INPUTXBAR13_G2 Register (Offset = 44Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3352. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 044Ch

Figure 3-1720. CONTROLSS_INPUTXBAR13_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR13_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3353. CONTROLSS_INPUTXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR13_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.57 CONTROLSS_INPUTXBAR14_GSEL Register

3.20.2.57.1 CONTROLSS_INPUTXBAR14_GSEL Register (Offset = 480h) [reset = 0h]

INPUT XBAR14 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3354. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0480h

Figure 3-1721. CONTROLSS_INPUTXBAR14_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR14_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3355. CONTROLSS_INPUTXBAR14_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR14_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.58 CONTROLSS_INPUTXBAR14_G0 Register

3.20.2.58.1 CONTROLSS_INPUTXBAR14_G0 Register (Offset = 484h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3356. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0484h

Figure 3-1722. CONTROLSS_INPUTXBAR14_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR14_G0_SEL							
R/W							
0h							

Table 3-3357. CONTROLSS_INPUTXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR14_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.59 CONTROLSS_INPUTXBAR14_G1 Register

3.20.2.59.1 CONTROLSS_INPUTXBAR14_G1 Register (Offset = 488h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3358. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0488h

Figure 3-1723. CONTROLSS_INPUTXBAR14_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR14_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3359. CONTROLSS_INPUTXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR14_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.60 CONTROLSS_INPUTXBAR14_G2 Register

3.20.2.60.1 CONTROLSS_INPUTXBAR14_G2 Register (Offset = 48Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3360. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 048Ch

Figure 3-1724. CONTROLSS_INPUTXBAR14_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR14_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3361. CONTROLSS_INPUTXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR14_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.61 CONTROLSS_INPUTXBAR15_GSEL Register

3.20.2.61.1 CONTROLSS_INPUTXBAR15_GSEL Register (Offset = 4C0h) [reset = 0h]

INPUT XBAR15 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3362. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 04C0h

Figure 3-1725. CONTROLSS_INPUTXBAR15_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR15_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3363. CONTROLSS_INPUTXBAR15_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR15_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.62 CONTROLSS_INPUTXBAR15_G0 Register

3.20.2.62.1 CONTROLSS_INPUTXBAR15_G0 Register (Offset = 4C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3364. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 04C4h

Figure 3-1726. CONTROLSS_INPUTXBAR15_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR15_G0_SEL							
R/W							
0h							

Table 3-3365. CONTROLSS_INPUTXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR15_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.63 CONTROLSS_INPUTXBAR15_G1 Register

3.20.2.63.1 CONTROLSS_INPUTXBAR15_G1 Register (Offset = 4C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3366. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 04C8h

Figure 3-1727. CONTROLSS_INPUTXBAR15_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR15_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3367. CONTROLSS_INPUTXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR15_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.64 CONTROLSS_INPUTXBAR15_G2 Register

3.20.2.64.1 CONTROLSS_INPUTXBAR15_G2 Register (Offset = 4CCh) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3368. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 04CCh

Figure 3-1728. CONTROLSS_INPUTXBAR15_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR15_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3369. CONTROLSS_INPUTXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR15_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.65 CONTROLSS_INPUTXBAR16_GSEL Register

3.20.2.65.1 CONTROLSS_INPUTXBAR16_GSEL Register (Offset = 500h) [reset = 0h]

INPUT XBAR16 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3370. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0500h

Figure 3-1729. CONTROLSS_INPUTXBAR16_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR16_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3371. CONTROLSS_INPUTXBAR16_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR16_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.66 CONTROLSS_INPUTXBAR16_G0 Register

3.20.2.66.1 CONTROLSS_INPUTXBAR16_G0 Register (Offset = 504h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3372. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0504h

Figure 3-1730. CONTROLSS_INPUTXBAR16_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR16_G0_SEL							
R/W							
0h							

Table 3-3373. CONTROLSS_INPUTXBAR16_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR16_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.67 CONTROLSS_INPUTXBAR16_G1 Register

3.20.2.67.1 CONTROLSS_INPUTXBAR16_G1 Register (Offset = 508h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3374. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0508h

Figure 3-1731. CONTROLSS_INPUTXBAR16_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR16_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3375. CONTROLSS_INPUTXBAR16_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR16_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.68 CONTROLSS_INPUTXBAR16_G2 Register

3.20.2.68.1 CONTROLSS_INPUTXBAR16_G2 Register (Offset = 50Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3376. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 050Ch

Figure 3-1732. CONTROLSS_INPUTXBAR16_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				INPUTXBAR16_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3377. CONTROLSS_INPUTXBAR16_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR16_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.69 CONTROLSS_INPUTXBAR17_GSEL Register

3.20.2.69.1 CONTROLSS_INPUTXBAR17_GSEL Register (Offset = 540h) [reset = 0h]

INPUT XBAR17 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3378. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0540h

Figure 3-1733. CONTROLSS_INPUTXBAR17_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR17_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3379. CONTROLSS_INPUTXBAR17_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR17_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.70 CONTROLSS_INPUTXBAR17_G0 Register

3.20.2.70.1 CONTROLSS_INPUTXBAR17_G0 Register (Offset = 544h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3380. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0544h

Figure 3-1734. CONTROLSS_INPUTXBAR17_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR17_G0_SEL							
R/W							
0h							

Table 3-3381. CONTROLSS_INPUTXBAR17_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR17_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.71 CONTROLSS_INPUTXBAR17_G1 Register

3.20.2.71.1 CONTROLSS_INPUTXBAR17_G1 Register (Offset = 548h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3382. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0548h

Figure 3-1735. CONTROLSS_INPUTXBAR17_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR17_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3383. CONTROLSS_INPUTXBAR17_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR17_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.72 CONTROLSS_INPUTXBAR17_G2 Register

3.20.2.72.1 CONTROLSS_INPUTXBAR17_G2 Register (Offset = 54Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3384. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 054Ch

Figure 3-1736. CONTROLSS_INPUTXBAR17_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				INPUTXBAR17_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3385. CONTROLSS_INPUTXBAR17_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR17_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.73 CONTROLSS_INPUTXBAR18_GSEL Register

3.20.2.73.1 CONTROLSS_INPUTXBAR18_GSEL Register (Offset = 580h) [reset = 0h]

INPUT XBAR18 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3386. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0580h

Figure 3-1737. CONTROLSS_INPUTXBAR18_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR18_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3387. CONTROLSS_INPUTXBAR18_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR18_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.74 CONTROLSS_INPUTXBAR18_G0 Register

3.20.2.74.1 CONTROLSS_INPUTXBAR18_G0 Register (Offset = 584h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3388. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0584h

Figure 3-1738. CONTROLSS_INPUTXBAR18_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR18_G0_SEL							
R/W							
0h							

Table 3-3389. CONTROLSS_INPUTXBAR18_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR18_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.75 CONTROLSS_INPUTXBAR18_G1 Register

3.20.2.75.1 CONTROLSS_INPUTXBAR18_G1 Register (Offset = 588h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3390. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0588h

Figure 3-1739. CONTROLSS_INPUTXBAR18_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR18_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3391. CONTROLSS_INPUTXBAR18_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR18_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.76 CONTROLSS_INPUTXBAR18_G2 Register

3.20.2.76.1 CONTROLSS_INPUTXBAR18_G2 Register (Offset = 58Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3392. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 058Ch

Figure 3-1740. CONTROLSS_INPUTXBAR18_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				INPUTXBAR18_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3393. CONTROLSS_INPUTXBAR18_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR18_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.77 CONTROLSS_INPUTXBAR19_GSEL Register

3.20.2.77.1 CONTROLSS_INPUTXBAR19_GSEL Register (Offset = 5C0h) [reset = 0h]

INPUT XBAR19 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3394. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 05C0h

Figure 3-1741. CONTROLSS_INPUTXBAR19_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR19_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3395. CONTROLSS_INPUTXBAR19_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR19_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.78 CONTROLSS_INPUTXBAR19_G0 Register

3.20.2.78.1 CONTROLSS_INPUTXBAR19_G0 Register (Offset = 5C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3396. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 05C4h

Figure 3-1742. CONTROLSS_INPUTXBAR19_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR19_G0_SEL							
R/W							
0h							

Table 3-3397. CONTROLSS_INPUTXBAR19_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR19_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.79 CONTROLSS_INPUTXBAR19_G1 Register

3.20.2.79.1 CONTROLSS_INPUTXBAR19_G1 Register (Offset = 5C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3398. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 05C8h

Figure 3-1743. CONTROLSS_INPUTXBAR19_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR19_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3399. CONTROLSS_INPUTXBAR19_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR19_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.80 CONTROLSS_INPUTXBAR19_G2 Register

3.20.2.80.1 CONTROLSS_INPUTXBAR19_G2 Register (Offset = 5CCh) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3400. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 05CCh

Figure 3-1744. CONTROLSS_INPUTXBAR19_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR19_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3401. CONTROLSS_INPUTXBAR19_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR19_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.81 CONTROLSS_INPUTXBAR20_GSEL Register

3.20.2.81.1 CONTROLSS_INPUTXBAR20_GSEL Register (Offset = 600h) [reset = 0h]

INPUT XBAR20 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3402. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0600h

Figure 3-1745. CONTROLSS_INPUTXBAR20_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR20_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3403. CONTROLSS_INPUTXBAR20_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR20_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.82 CONTROLSS_INPUTXBAR20_G0 Register

3.20.2.82.1 CONTROLSS_INPUTXBAR20_G0 Register (Offset = 604h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3404. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0604h

Figure 3-1746. CONTROLSS_INPUTXBAR20_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR20_G0_SEL							
R/W							
0h							

Table 3-3405. CONTROLSS_INPUTXBAR20_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR20_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.83 CONTROLSS_INPUTXBAR20_G1 Register

3.20.2.83.1 CONTROLSS_INPUTXBAR20_G1 Register (Offset = 608h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3406. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0608h

Figure 3-1747. CONTROLSS_INPUTXBAR20_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR20_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3407. CONTROLSS_INPUTXBAR20_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR20_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.84 CONTROLSS_INPUTXBAR20_G2 Register

3.20.2.84.1 CONTROLSS_INPUTXBAR20_G2 Register (Offset = 60Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3408. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 060Ch

Figure 3-1748. CONTROLSS_INPUTXBAR20_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR20_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3409. CONTROLSS_INPUTXBAR20_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR20_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.85 CONTROLSS_INPUTXBAR21_GSEL Register

3.20.2.85.1 CONTROLSS_INPUTXBAR21_GSEL Register (Offset = 640h) [reset = 0h]

INPUT XBAR21 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3410. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0640h

Figure 3-1749. CONTROLSS_INPUTXBAR21_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR21_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3411. CONTROLSS_INPUTXBAR21_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR21_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.86 CONTROLSS_INPUTXBAR21_G0 Register

3.20.2.86.1 CONTROLSS_INPUTXBAR21_G0 Register (Offset = 644h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3412. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0644h

Figure 3-1750. CONTROLSS_INPUTXBAR21_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR21_G0_SEL							
R/W							
0h							

Table 3-3413. CONTROLSS_INPUTXBAR21_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR21_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.87 CONTROLSS_INPUTXBAR21_G1 Register

3.20.2.87.1 CONTROLSS_INPUTXBAR21_G1 Register (Offset = 648h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3414. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0648h

Figure 3-1751. CONTROLSS_INPUTXBAR21_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR21_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3415. CONTROLSS_INPUTXBAR21_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR21_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.88 CONTROLSS_INPUTXBAR21_G2 Register

3.20.2.88.1 CONTROLSS_INPUTXBAR21_G2 Register (Offset = 64Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3416. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 064Ch

Figure 3-1752. CONTROLSS_INPUTXBAR21_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR21_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3417. CONTROLSS_INPUTXBAR21_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR21_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.89 CONTROLSS_INPUTXBAR22_GSEL Register

3.20.2.89.1 CONTROLSS_INPUTXBAR22_GSEL Register (Offset = 680h) [reset = 0h]

INPUT XBAR22 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3418. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0680h

Figure 3-1753. CONTROLSS_INPUTXBAR22_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR22_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3419. CONTROLSS_INPUTXBAR22_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR22_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.90 CONTROLSS_INPUTXBAR22_G0 Register

3.20.2.90.1 CONTROLSS_INPUTXBAR22_G0 Register (Offset = 684h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3420. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0684h

Figure 3-1754. CONTROLSS_INPUTXBAR22_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR22_G0_SEL							
R/W							
0h							

Table 3-3421. CONTROLSS_INPUTXBAR22_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR22_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.91 CONTROLSS_INPUTXBAR22_G1 Register

3.20.2.91.1 CONTROLSS_INPUTXBAR22_G1 Register (Offset = 688h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3422. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0688h

Figure 3-1755. CONTROLSS_INPUTXBAR22_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR22_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3423. CONTROLSS_INPUTXBAR22_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR22_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.92 CONTROLSS_INPUTXBAR22_G2 Register

3.20.2.92.1 CONTROLSS_INPUTXBAR22_G2 Register (Offset = 68Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3424. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 068Ch

Figure 3-1756. CONTROLSS_INPUTXBAR22_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR22_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3425. CONTROLSS_INPUTXBAR22_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR22_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.93 CONTROLSS_INPUTXBAR23_GSEL Register

3.20.2.93.1 CONTROLSS_INPUTXBAR23_GSEL Register (Offset = 6C0h) [reset = 0h]

INPUT XBAR23 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3426. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 06C0h

Figure 3-1757. CONTROLSS_INPUTXBAR23_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR23_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3427. CONTROLSS_INPUTXBAR23_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR23_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.94 CONTROLSS_INPUTXBAR23_G0 Register

3.20.2.94.1 CONTROLSS_INPUTXBAR23_G0 Register (Offset = 6C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3428. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 06C4h

Figure 3-1758. CONTROLSS_INPUTXBAR23_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR23_G0_SEL							
R/W							
0h							

Table 3-3429. CONTROLSS_INPUTXBAR23_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR23_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.95 CONTROLSS_INPUTXBAR23_G1 Register

3.20.2.95.1 CONTROLSS_INPUTXBAR23_G1 Register (Offset = 6C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3430. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 06C8h

Figure 3-1759. CONTROLSS_INPUTXBAR23_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR23_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3431. CONTROLSS_INPUTXBAR23_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR23_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.96 CONTROLSS_INPUTXBAR23_G2 Register

3.20.2.96.1 CONTROLSS_INPUTXBAR23_G2 Register (Offset = 6CCh) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3432. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 06CCh

Figure 3-1760. CONTROLSS_INPUTXBAR23_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				INPUTXBAR23_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3433. CONTROLSS_INPUTXBAR23_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR23_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.97 CONTROLSS_INPUTXBAR24_GSEL Register

3.20.2.97.1 CONTROLSS_INPUTXBAR24_GSEL Register (Offset = 700h) [reset = 0h]

INPUT XBAR24 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3434. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0700h

Figure 3-1761. CONTROLSS_INPUTXBAR24_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR24_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3435. CONTROLSS_INPUTXBAR24_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR24_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.98 CONTROLSS_INPUTXBAR24_G0 Register

3.20.2.98.1 CONTROLSS_INPUTXBAR24_G0 Register (Offset = 704h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3436. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0704h

Figure 3-1762. CONTROLSS_INPUTXBAR24_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR24_G0_SEL							
R/W							
0h							

Table 3-3437. CONTROLSS_INPUTXBAR24_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR24_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.99 CONTROLSS_INPUTXBAR24_G1 Register

3.20.2.99.1 CONTROLSS_INPUTXBAR24_G1 Register (Offset = 708h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3438. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0708h

Figure 3-1763. CONTROLSS_INPUTXBAR24_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR24_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3439. CONTROLSS_INPUTXBAR24_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR24_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.100 CONTROLSS_INPUTXBAR24_G2 Register

3.20.2.100.1 CONTROLSS_INPUTXBAR24_G2 Register (Offset = 70Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3440. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 070Ch

Figure 3-1764. CONTROLSS_INPUTXBAR24_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR24_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3441. CONTROLSS_INPUTXBAR24_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR24_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.101 CONTROLSS_INPUTXBAR25_GSEL Register

3.20.2.101.1 CONTROLSS_INPUTXBAR25_GSEL Register (Offset = 740h) [reset = 0h]

INPUT XBAR25 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3442. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0740h

Figure 3-1765. CONTROLSS_INPUTXBAR25_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR25_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3443. CONTROLSS_INPUTXBAR25_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR25_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.102 CONTROLSS_INPUTXBAR25_G0 Register

3.20.2.102.1 CONTROLSS_INPUTXBAR25_G0 Register (Offset = 744h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3444. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0744h

Figure 3-1766. CONTROLSS_INPUTXBAR25_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR25_G0_SEL							
R/W							
0h							

Table 3-3445. CONTROLSS_INPUTXBAR25_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR25_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.103 CONTROLSS_INPUTXBAR25_G1 Register

3.20.2.103.1 CONTROLSS_INPUTXBAR25_G1 Register (Offset = 748h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3446. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0748h

Figure 3-1767. CONTROLSS_INPUTXBAR25_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR25_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3447. CONTROLSS_INPUTXBAR25_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR25_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.104 CONTROLSS_INPUTXBAR25_G2 Register

3.20.2.104.1 CONTROLSS_INPUTXBAR25_G2 Register (Offset = 74Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3448. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 074Ch

Figure 3-1768. CONTROLSS_INPUTXBAR25_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR25_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3449. CONTROLSS_INPUTXBAR25_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR25_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.105 CONTROLSS_INPUTXBAR26_GSEL Register

3.20.2.105.1 CONTROLSS_INPUTXBAR26_GSEL Register (Offset = 780h) [reset = 0h]

INPUT XBAR26 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3450. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0780h

Figure 3-1769. CONTROLSS_INPUTXBAR26_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						INPUTXBAR26_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3451. CONTROLSS_INPUTXBAR26_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR26_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.106 CONTROLSS_INPUTXBAR26_G0 Register

3.20.2.106.1 CONTROLSS_INPUTXBAR26_G0 Register (Offset = 784h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3452. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0784h

Figure 3-1770. CONTROLSS_INPUTXBAR26_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR26_G0_SEL							
R/W							
0h							

Table 3-3453. CONTROLSS_INPUTXBAR26_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR26_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.107 CONTROLSS_INPUTXBAR26_G1 Register

3.20.2.107.1 CONTROLSS_INPUTXBAR26_G1 Register (Offset = 788h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3454. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0788h

Figure 3-1771. CONTROLSS_INPUTXBAR26_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR26_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3455. CONTROLSS_INPUTXBAR26_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR26_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.108 CONTROLSS_INPUTXBAR26_G2 Register

3.20.2.108.1 CONTROLSS_INPUTXBAR26_G2 Register (Offset = 78Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3456. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 078Ch

Figure 3-1772. CONTROLSS_INPUTXBAR26_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR26_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3457. CONTROLSS_INPUTXBAR26_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR26_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.109 CONTROLSS_INPUTXBAR27_GSEL Register

3.20.2.109.1 CONTROLSS_INPUTXBAR27_GSEL Register (Offset = 7C0h) [reset = 0h]

INPUT XBAR27 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3458. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 07C0h

Figure 3-1773. CONTROLSS_INPUTXBAR27_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR27_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3459. CONTROLSS_INPUTXBAR27_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR27_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.110 CONTROLSS_INPUTXBAR27_G0 Register

3.20.2.110.1 CONTROLSS_INPUTXBAR27_G0 Register (Offset = 7C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3460. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 07C4h

Figure 3-1774. CONTROLSS_INPUTXBAR27_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR27_G0_SEL							
R/W							
0h							

Table 3-3461. CONTROLSS_INPUTXBAR27_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR27_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.111 CONTROLSS_INPUTXBAR27_G1 Register

3.20.2.111.1 CONTROLSS_INPUTXBAR27_G1 Register (Offset = 7C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3462. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 07C8h

Figure 3-1775. CONTROLSS_INPUTXBAR27_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR27_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3463. CONTROLSS_INPUTXBAR27_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR27_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.112 CONTROLSS_INPUTXBAR27_G2 Register

3.20.2.112.1 CONTROLSS_INPUTXBAR27_G2 Register (Offset = 7CCh) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3464. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 07CCh

Figure 3-1776. CONTROLSS_INPUTXBAR27_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR27_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3465. CONTROLSS_INPUTXBAR27_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR27_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.113 CONTROLSS_INPUTXBAR28_GSEL Register

3.20.2.113.1 CONTROLSS_INPUTXBAR28_GSEL Register (Offset = 800h) [reset = 0h]

INPUT XBAR28 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3466. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0800h

Figure 3-1777. CONTROLSS_INPUTXBAR28_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR28_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3467. CONTROLSS_INPUTXBAR28_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR28_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.114 CONTROLSS_INPUTXBAR28_G0 Register

3.20.2.114.1 CONTROLSS_INPUTXBAR28_G0 Register (Offset = 804h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3468. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0804h

Figure 3-1778. CONTROLSS_INPUTXBAR28_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR28_G0_SEL							
R/W							
0h							

Table 3-3469. CONTROLSS_INPUTXBAR28_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR28_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.115 CONTROLSS_INPUTXBAR28_G1 Register

3.20.2.115.1 CONTROLSS_INPUTXBAR28_G1 Register (Offset = 808h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3470. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0808h

Figure 3-1779. CONTROLSS_INPUTXBAR28_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR28_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3471. CONTROLSS_INPUTXBAR28_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR28_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.116 CONTROLSS_INPUTXBAR28_G2 Register

3.20.2.116.1 CONTROLSS_INPUTXBAR28_G2 Register (Offset = 80Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3472. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 080Ch

Figure 3-1780. CONTROLSS_INPUTXBAR28_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				INPUTXBAR28_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3473. CONTROLSS_INPUTXBAR28_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR28_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.117 CONTROLSS_INPUTXBAR29_GSEL Register

3.20.2.117.1 CONTROLSS_INPUTXBAR29_GSEL Register (Offset = 840h) [reset = 0h]

INPUT XBAR29 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3474. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0840h

Figure 3-1781. CONTROLSS_INPUTXBAR29_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR29_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3475. CONTROLSS_INPUTXBAR29_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR29_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.118 CONTROLSS_INPUTXBAR29_G0 Register

3.20.2.118.1 CONTROLSS_INPUTXBAR29_G0 Register (Offset = 844h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3476. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0844h

Figure 3-1782. CONTROLSS_INPUTXBAR29_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR29_G0_SEL							
R/W							
0h							

Table 3-3477. CONTROLSS_INPUTXBAR29_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR29_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.119 CONTROLSS_INPUTXBAR29_G1 Register

3.20.2.119.1 CONTROLSS_INPUTXBAR29_G1 Register (Offset = 848h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3478. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0848h

Figure 3-1783. CONTROLSS_INPUTXBAR29_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR29_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3479. CONTROLSS_INPUTXBAR29_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR29_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.120 CONTROLSS_INPUTXBAR29_G2 Register

3.20.2.120.1 CONTROLSS_INPUTXBAR29_G2 Register (Offset = 84Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3480. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 084Ch

Figure 3-1784. CONTROLSS_INPUTXBAR29_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				INPUTXBAR29_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3481. CONTROLSS_INPUTXBAR29_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR29_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.121 CONTROLSS_INPUTXBAR30_GSEL Register

3.20.2.121.1 CONTROLSS_INPUTXBAR30_GSEL Register (Offset = 880h) [reset = 0h]

INPUT XBAR30 Input Select
0 : GPI
1: ICSS GPO port.

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Table 3-3482. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0880h

Figure 3-1785. CONTROLSS_INPUTXBAR30_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR30_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3483. CONTROLSS_INPUTXBAR30_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR30_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.122 CONTROLSS_INPUTXBAR30_G0 Register

3.20.2.122.1 CONTROLSS_INPUTXBAR30_G0 Register (Offset = 884h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3484. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0884h

Figure 3-1786. CONTROLSS_INPUTXBAR30_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR30_G0_SEL							
R/W							
0h							

Table 3-3485. CONTROLSS_INPUTXBAR30_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR30_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.123 CONTROLSS_INPUTXBAR30_G1 Register

3.20.2.123.1 CONTROLSS_INPUTXBAR30_G1 Register (Offset = 888h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3486. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0888h

Figure 3-1787. CONTROLSS_INPUTXBAR30_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			INPUTXBAR30_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3487. CONTROLSS_INPUTXBAR30_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR30_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.124 CONTROLSS_INPUTXBAR30_G2 Register

3.20.2.124.1 CONTROLSS_INPUTXBAR30_G2 Register (Offset = 88Ch) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3488. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 088Ch

Figure 3-1788. CONTROLSS_INPUTXBAR30_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				INPUTXBAR30_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3489. CONTROLSS_INPUTXBAR30_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR30_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.20.2.125 CONTROLSS_INPUTXBAR31_GSEL Register

3.20.2.125.1 CONTROLSS_INPUTXBAR31_GSEL Register (Offset = 8C0h) [reset = 0h]

INPUT XBAR31 Input Select
0 : GPI
1: ICSS GPO port.

Return to Summary Table

Table 3-3490. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 08C0h

Figure 3-1789. CONTROLSS_INPUTXBAR31_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						INPUTXBAR31_GSEL_GSEL	
NONE						R/W	
0h						0h	

Table 3-3491. CONTROLSS_INPUTXBAR31_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	INPUTXBAR31_GSEL_GSEL	R/W	0h	Select input source Group: 0 G0 selected 1 G1 selected 2 G2 selected

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3.20.2.126 CONTROLSS_INPUTXBAR31_G0 Register

3.20.2.126.1 CONTROLSS_INPUTXBAR31_G0 Register (Offset = 8C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

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Table 3-3492. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 08C4h

Figure 3-1790. CONTROLSS_INPUTXBAR31_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
INPUTXBAR31_G0_SEL							
R/W							
0h							

Table 3-3493. CONTROLSS_INPUTXBAR31_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	INPUTXBAR31_G0_SEL	R/W	0h	Select input source: 0 G0.0 selected .. x G0.x selected

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3.20.2.127 CONTROLSS_INPUTXBAR31_G1 Register

3.20.2.127.1 CONTROLSS_INPUTXBAR31_G1 Register (Offset = 8C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

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Table 3-3494. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 08C8h

Figure 3-1791. CONTROLSS_INPUTXBAR31_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			INPUTXBAR31_G1_SEL				
NONE			R/W				
0h			0h				

Table 3-3495. CONTROLSS_INPUTXBAR31_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	INPUTXBAR31_G1_SEL	R/W	0h	Select input source: 0 G1.0 selected .. 31 G1.31 selected

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3.20.2.128 CONTROLSS_INPUTXBAR31_G2 Register

3.20.2.128.1 CONTROLSS_INPUTXBAR31_G2 Register (Offset = 8CCh) [reset = 0h]

OUTPUTXBAR port selection - OUTPUTXBAR[15:0].

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Table 3-3496. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 08CCh

Figure 3-1792. CONTROLSS_INPUTXBAR31_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				INPUTXBAR31_G2_SEL			
NONE				R/W			
0h				0h			

Table 3-3497. CONTROLSS_INPUTXBAR31_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	INPUTXBAR31_G2_SEL	R/W	0h	Select input source: 0 G2.0 selected .. 15 G2.15 selected

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3.21 CONTROLSS_MDLXBAR

CONTROLSS_MDLXBAR

3.21.1 CONTROLSS_MDLXBAR Summaries

CONTROLSS_MDLXBAR Summaries

Table 3-3498. CONTROLSS Registers, Base Address=502D 3000h, Length=4096

Offset	Length	Register Name	CONTROLSS_MDLXBAR Physical Address
100h	32	CONTROLSS_MDLXBAR0_G0	502D 3100h
104h	32	CONTROLSS_MDLXBAR0_G1	502D 3104h
108h	32	CONTROLSS_MDLXBAR0_G2	502D 3108h
140h	32	CONTROLSS_MDLXBAR1_G0	502D 3140h
144h	32	CONTROLSS_MDLXBAR1_G1	502D 3144h
148h	32	CONTROLSS_MDLXBAR1_G2	502D 3148h
180h	32	CONTROLSS_MDLXBAR2_G0	502D 3180h
184h	32	CONTROLSS_MDLXBAR2_G1	502D 3184h
188h	32	CONTROLSS_MDLXBAR2_G2	502D 3188h
1C0h	32	CONTROLSS_MDLXBAR3_G0	502D 31C0h
1C4h	32	CONTROLSS_MDLXBAR3_G1	502D 31C4h
1C8h	32	CONTROLSS_MDLXBAR3_G2	502D 31C8h
200h	32	CONTROLSS_MDLXBAR4_G0	502D 3200h
204h	32	CONTROLSS_MDLXBAR4_G1	502D 3204h
208h	32	CONTROLSS_MDLXBAR4_G2	502D 3208h
240h	32	CONTROLSS_MDLXBAR5_G0	502D 3240h
244h	32	CONTROLSS_MDLXBAR5_G1	502D 3244h
248h	32	CONTROLSS_MDLXBAR5_G2	502D 3248h
280h	32	CONTROLSS_MDLXBAR6_G0	502D 3280h
284h	32	CONTROLSS_MDLXBAR6_G1	502D 3284h
288h	32	CONTROLSS_MDLXBAR6_G2	502D 3288h
2C0h	32	CONTROLSS_MDLXBAR7_G0	502D 32C0h
2C4h	32	CONTROLSS_MDLXBAR7_G1	502D 32C4h
2C8h	32	CONTROLSS_MDLXBAR7_G2	502D 32C8h
300h	32	CONTROLSS_MDLXBAR8_G0	502D 3300h
304h	32	CONTROLSS_MDLXBAR8_G1	502D 3304h
308h	32	CONTROLSS_MDLXBAR8_G2	502D 3308h
340h	32	CONTROLSS_MDLXBAR9_G0	502D 3340h
344h	32	CONTROLSS_MDLXBAR9_G1	502D 3344h
348h	32	CONTROLSS_MDLXBAR9_G2	502D 3348h
380h	32	CONTROLSS_MDLXBAR10_G0	502D 3380h
384h	32	CONTROLSS_MDLXBAR10_G1	502D 3384h
388h	32	CONTROLSS_MDLXBAR10_G2	502D 3388h
3C0h	32	CONTROLSS_MDLXBAR11_G0	502D 33C0h
3C4h	32	CONTROLSS_MDLXBAR11_G1	502D 33C4h
3C8h	32	CONTROLSS_MDLXBAR11_G2	502D 33C8h
400h	32	CONTROLSS_MDLXBAR12_G0	502D 3400h
404h	32	CONTROLSS_MDLXBAR12_G1	502D 3404h
408h	32	CONTROLSS_MDLXBAR12_G2	502D 3408h

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Table 3-3498. CONTROLSS Registers, Base Address=502D 3000h, Length=4096 (continued)

Offset	Length	Register Name	CONTROLSS_MDLXBAR Physical Address
440h	32	CONTROLSS_MDLXBAR13_G0	502D 3440h
444h	32	CONTROLSS_MDLXBAR13_G1	502D 3444h
448h	32	CONTROLSS_MDLXBAR13_G2	502D 3448h
480h	32	CONTROLSS_MDLXBAR14_G0	502D 3480h
484h	32	CONTROLSS_MDLXBAR14_G1	502D 3484h
488h	32	CONTROLSS_MDLXBAR14_G2	502D 3488h
4C0h	32	CONTROLSS_MDLXBAR15_G0	502D 34C0h
4C4h	32	CONTROLSS_MDLXBAR15_G1	502D 34C4h
4C8h	32	CONTROLSS_MDLXBAR15_G2	502D 34C8h

3.21.2 CONTROLSS_MDLXBAR Registers

CONTROLSS_MDLXBAR Registers

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3.21.2.1 CONTROLSS_MDLXBAR0_G0 Register

3.21.2.1.1 CONTROLSS_MDLXBAR0_G0 Register (Offset = 100h) [reset = 0h]

MDL XBAR 0 Input Select.

Return to Summary Table

Table 3-3499. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3100h

Figure 3-1793. CONTROLSS_MDLXBAR0_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR0_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR0_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR0_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR0_G0_SEL							
R/W							
0h							

Table 3-3500. CONTROLSS_MDLXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR0_G0_SEL	R/W	0h	MDL XBAR0 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.2 CONTROLSS_MDLXBAR0_G1 Register

3.21.2.2.1 CONTROLSS_MDLXBAR0_G1 Register (Offset = 104h) [reset = 0h]

MDL XBAR 0 Input Select.

Return to Summary Table

Table 3-3501. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3104h

Figure 3-1794. CONTROLSS_MDLXBAR0_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR0_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR0_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR0_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR0_G1_SEL							
R/W							
0h							

Table 3-3502. CONTROLSS_MDLXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR0_G1_SEL	R/W	0h	MDL XBAR0 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.3 CONTROLSS_MDLXBAR0_G2 Register

3.21.2.3.1 CONTROLSS_MDLXBAR0_G2 Register (Offset = 108h) [reset = 0h]

MDL XBAR 0 Input Select.

Return to Summary Table

Table 3-3503. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3108h

Figure 3-1795. CONTROLSS_MDLXBAR0_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR0_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR0_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR0_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR0_G2_SEL							
R/W							
0h							

Table 3-3504. CONTROLSS_MDLXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR0_G2_SEL	R/W	0h	MDL XBAR0 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.4 CONTROLSS_MDLXBAR1_G0 Register

3.21.2.4.1 CONTROLSS_MDLXBAR1_G0 Register (Offset = 140h) [reset = 0h]

MDL XBAR 1 Input Select.

Return to Summary Table

Table 3-3505. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3140h

Figure 3-1796. CONTROLSS_MDLXBAR1_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR1_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR1_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR1_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR1_G0_SEL							
R/W							
0h							

Table 3-3506. CONTROLSS_MDLXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR1_G0_SEL	R/W	0h	MDL XBAR1 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.5 CONTROLSS_MDLXBAR1_G1 Register

3.21.2.5.1 CONTROLSS_MDLXBAR1_G1 Register (Offset = 144h) [reset = 0h]

MDL XBAR 1 Input Select.

Return to Summary Table

Table 3-3507. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3144h

Figure 3-1797. CONTROLSS_MDLXBAR1_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR1_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR1_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR1_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR1_G1_SEL							
R/W							
0h							

Table 3-3508. CONTROLSS_MDLXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR1_G1_SEL	R/W	0h	MDL XBAR1 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.6 CONTROLSS_MDLXBAR1_G2 Register

3.21.2.6.1 CONTROLSS_MDLXBAR1_G2 Register (Offset = 148h) [reset = 0h]

MDL XBAR 1 Input Select.

Return to Summary Table

Table 3-3509. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3148h

Figure 3-1798. CONTROLSS_MDLXBAR1_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR1_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR1_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR1_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR1_G2_SEL							
R/W							
0h							

Table 3-3510. CONTROLSS_MDLXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR1_G2_SEL	R/W	0h	MDL XBAR1 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.7 CONTROLSS_MDLXBAR2_G0 Register

3.21.2.7.1 CONTROLSS_MDLXBAR2_G0 Register (Offset = 180h) [reset = 0h]

MDL XBAR 2 Input Select.

Return to Summary Table

Table 3-3511. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3180h

Figure 3-1799. CONTROLSS_MDLXBAR2_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR2_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR2_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR2_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR2_G0_SEL							
R/W							
0h							

Table 3-3512. CONTROLSS_MDLXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR2_G0_SEL	R/W	0h	MDL XBAR2 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.8 CONTROLSS_MDLXBAR2_G1 Register

3.21.2.8.1 CONTROLSS_MDLXBAR2_G1 Register (Offset = 184h) [reset = 0h]

MDL XBAR 2 Input Select.

Return to Summary Table

Table 3-3513. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3184h

Figure 3-1800. CONTROLSS_MDLXBAR2_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR2_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR2_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR2_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR2_G1_SEL							
R/W							
0h							

Table 3-3514. CONTROLSS_MDLXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR2_G1_SEL	R/W	0h	MDL XBAR2 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.9 CONTROLSS_MDLXBAR2_G2 Register

3.21.2.9.1 CONTROLSS_MDLXBAR2_G2 Register (Offset = 188h) [reset = 0h]

MDL XBAR 2 Input Select.

Return to Summary Table

Table 3-3515. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3188h

Figure 3-1801. CONTROLSS_MDLXBAR2_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR2_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR2_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR2_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR2_G2_SEL							
R/W							
0h							

Table 3-3516. CONTROLSS_MDLXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR2_G2_SEL	R/W	0h	MDL XBAR2 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.10 CONTROLSS_MDLXBAR3_G0 Register

3.21.2.10.1 CONTROLSS_MDLXBAR3_G0 Register (Offset = 1C0h) [reset = 0h]

MDL XBAR 3 Input Select.

Return to Summary Table

Table 3-3517. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 31C0h

Figure 3-1802. CONTROLSS_MDLXBAR3_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR3_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR3_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR3_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR3_G0_SEL							
R/W							
0h							

Table 3-3518. CONTROLSS_MDLXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR3_G0_SEL	R/W	0h	MDL XBAR3 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.11 CONTROLSS_MDLXBAR3_G1 Register

3.21.2.11.1 CONTROLSS_MDLXBAR3_G1 Register (Offset = 1C4h) [reset = 0h]

MDL XBAR 3 Input Select.

Return to Summary Table

Table 3-3519. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 31C4h

Figure 3-1803. CONTROLSS_MDLXBAR3_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR3_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR3_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR3_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR3_G1_SEL							
R/W							
0h							

Table 3-3520. CONTROLSS_MDLXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR3_G1_SEL	R/W	0h	MDL XBAR3 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.12 CONTROLSS_MDLXBAR3_G2 Register

3.21.2.12.1 CONTROLSS_MDLXBAR3_G2 Register (Offset = 1C8h) [reset = 0h]

MDL XBAR 3 Input Select.

Return to Summary Table

Table 3-3521. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 31C8h

Figure 3-1804. CONTROLSS_MDLXBAR3_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR3_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR3_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR3_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR3_G2_SEL							
R/W							
0h							

Table 3-3522. CONTROLSS_MDLXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR3_G2_SEL	R/W	0h	MDL XBAR3 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.13 CONTROLSS_MDLXBAR4_G0 Register

3.21.2.13.1 CONTROLSS_MDLXBAR4_G0 Register (Offset = 200h) [reset = 0h]

MDL XBAR 4 Input Select.

Return to Summary Table

Table 3-3523. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3200h

Figure 3-1805. CONTROLSS_MDLXBAR4_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR4_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR4_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR4_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR4_G0_SEL							
R/W							
0h							

Table 3-3524. CONTROLSS_MDLXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR4_G0_SEL	R/W	0h	MDL XBAR4 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.14 CONTROLSS_MDLXBAR4_G1 Register

3.21.2.14.1 CONTROLSS_MDLXBAR4_G1 Register (Offset = 204h) [reset = 0h]

MDL XBAR 4 Input Select.

Return to Summary Table

Table 3-3525. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3204h

Figure 3-1806. CONTROLSS_MDLXBAR4_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR4_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR4_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR4_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR4_G1_SEL							
R/W							
0h							

Table 3-3526. CONTROLSS_MDLXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR4_G1_SEL	R/W	0h	MDL XBAR4 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.15 CONTROLSS_MDLXBAR4_G2 Register

3.21.2.15.1 CONTROLSS_MDLXBAR4_G2 Register (Offset = 208h) [reset = 0h]

MDL XBAR 4 Input Select.

Return to Summary Table

Table 3-3527. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3208h

Figure 3-1807. CONTROLSS_MDLXBAR4_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR4_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR4_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR4_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR4_G2_SEL							
R/W							
0h							

Table 3-3528. CONTROLSS_MDLXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR4_G2_SEL	R/W	0h	MDL XBAR4 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.16 CONTROLSS_MDLXBAR5_G0 Register

3.21.2.16.1 CONTROLSS_MDLXBAR5_G0 Register (Offset = 240h) [reset = 0h]

MDL XBAR 5 Input Select.

Return to Summary Table

Table 3-3529. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3240h

Figure 3-1808. CONTROLSS_MDLXBAR5_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR5_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR5_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR5_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR5_G0_SEL							
R/W							
0h							

Table 3-3530. CONTROLSS_MDLXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR5_G0_SEL	R/W	0h	MDL XBAR5 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.17 CONTROLSS_MDLXBAR5_G1 Register

3.21.2.17.1 CONTROLSS_MDLXBAR5_G1 Register (Offset = 244h) [reset = 0h]

MDL XBAR 5 Input Select.

Return to Summary Table

Table 3-3531. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3244h

Figure 3-1809. CONTROLSS_MDLXBAR5_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR5_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR5_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR5_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR5_G1_SEL							
R/W							
0h							

Table 3-3532. CONTROLSS_MDLXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR5_G1_SEL	R/W	0h	MDL XBAR5 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.18 CONTROLSS_MDLXBAR5_G2 Register

3.21.2.18.1 CONTROLSS_MDLXBAR5_G2 Register (Offset = 248h) [reset = 0h]

MDL XBAR 5 Input Select.

Return to Summary Table

Table 3-3533. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3248h

Figure 3-1810. CONTROLSS_MDLXBAR5_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR5_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR5_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR5_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR5_G2_SEL							
R/W							
0h							

Table 3-3534. CONTROLSS_MDLXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR5_G2_SEL	R/W	0h	MDL XBAR5 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.19 CONTROLSS_MDLXBAR6_G0 Register

3.21.2.19.1 CONTROLSS_MDLXBAR6_G0 Register (Offset = 280h) [reset = 0h]

MDL XBAR 6 Input Select.

Return to Summary Table

Table 3-3535. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3280h

Figure 3-1811. CONTROLSS_MDLXBAR6_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR6_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR6_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR6_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR6_G0_SEL							
R/W							
0h							

Table 3-3536. CONTROLSS_MDLXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR6_G0_SEL	R/W	0h	MDL XBAR6 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.20 CONTROLSS_MDLXBAR6_G1 Register

3.21.2.20.1 CONTROLSS_MDLXBAR6_G1 Register (Offset = 284h) [reset = 0h]

MDL XBAR 6 Input Select.

Return to Summary Table

Table 3-3537. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3284h

Figure 3-1812. CONTROLSS_MDLXBAR6_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR6_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR6_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR6_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR6_G1_SEL							
R/W							
0h							

Table 3-3538. CONTROLSS_MDLXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR6_G1_SEL	R/W	0h	MDL XBAR6 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.21 CONTROLSS_MDLXBAR6_G2 Register

3.21.2.21.1 CONTROLSS_MDLXBAR6_G2 Register (Offset = 288h) [reset = 0h]

MDL XBAR 6 Input Select.

Return to Summary Table

Table 3-3539. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3288h

Figure 3-1813. CONTROLSS_MDLXBAR6_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR6_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR6_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR6_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR6_G2_SEL							
R/W							
0h							

Table 3-3540. CONTROLSS_MDLXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR6_G2_SEL	R/W	0h	MDL XBAR6 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.22 CONTROLSS_MDLXBAR7_G0 Register

3.21.2.22.1 CONTROLSS_MDLXBAR7_G0 Register (Offset = 2C0h) [reset = 0h]

MDL XBAR 7 Input Select.

Return to Summary Table

Table 3-3541. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 32C0h

Figure 3-1814. CONTROLSS_MDLXBAR7_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR7_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR7_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR7_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR7_G0_SEL							
R/W							
0h							

Table 3-3542. CONTROLSS_MDLXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR7_G0_SEL	R/W	0h	MDL XBAR7 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.23 CONTROLSS_MDLXBAR7_G1 Register

3.21.2.23.1 CONTROLSS_MDLXBAR7_G1 Register (Offset = 2C4h) [reset = 0h]

MDL XBAR 7 Input Select.

Return to Summary Table

Table 3-3543. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 32C4h

Figure 3-1815. CONTROLSS_MDLXBAR7_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR7_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR7_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR7_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR7_G1_SEL							
R/W							
0h							

Table 3-3544. CONTROLSS_MDLXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR7_G1_SEL	R/W	0h	MDL XBAR7 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.24 CONTROLSS_MDLXBAR7_G2 Register

3.21.2.24.1 CONTROLSS_MDLXBAR7_G2 Register (Offset = 2C8h) [reset = 0h]

MDL XBAR 7 Input Select.

Return to Summary Table

Table 3-3545. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 32C8h

Figure 3-1816. CONTROLSS_MDLXBAR7_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR7_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR7_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR7_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR7_G2_SEL							
R/W							
0h							

Table 3-3546. CONTROLSS_MDLXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR7_G2_SEL	R/W	0h	MDL XBAR7 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.25 CONTROLSS_MDLXBAR8_G0 Register

3.21.2.25.1 CONTROLSS_MDLXBAR8_G0 Register (Offset = 300h) [reset = 0h]

MDL XBAR 8 Input Select.

Return to Summary Table

Table 3-3547. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3300h

Figure 3-1817. CONTROLSS_MDLXBAR8_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR8_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR8_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR8_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR8_G0_SEL							
R/W							
0h							

Table 3-3548. CONTROLSS_MDLXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR8_G0_SEL	R/W	0h	MDL XBAR8 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.26 CONTROLSS_MDLXBAR8_G1 Register

3.21.2.26.1 CONTROLSS_MDLXBAR8_G1 Register (Offset = 304h) [reset = 0h]

MDL XBAR 8 Input Select.

Return to Summary Table

Table 3-3549. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3304h

Figure 3-1818. CONTROLSS_MDLXBAR8_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR8_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR8_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR8_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR8_G1_SEL							
R/W							
0h							

Table 3-3550. CONTROLSS_MDLXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR8_G1_SEL	R/W	0h	MDL XBAR8 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.27 CONTROLSS_MDLXBAR8_G2 Register

3.21.2.27.1 CONTROLSS_MDLXBAR8_G2 Register (Offset = 308h) [reset = 0h]

MDL XBAR 8 Input Select.

Return to Summary Table

Table 3-3551. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3308h

Figure 3-1819. CONTROLSS_MDLXBAR8_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR8_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR8_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR8_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR8_G2_SEL							
R/W							
0h							

Table 3-3552. CONTROLSS_MDLXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR8_G2_SEL	R/W	0h	MDL XBAR8 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.28 CONTROLSS_MDLXBAR9_G0 Register

3.21.2.28.1 CONTROLSS_MDLXBAR9_G0 Register (Offset = 340h) [reset = 0h]

MDL XBAR 9 Input Select.

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Table 3-3553. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3340h

Figure 3-1820. CONTROLSS_MDLXBAR9_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR9_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR9_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR9_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR9_G0_SEL							
R/W							
0h							

Table 3-3554. CONTROLSS_MDLXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR9_G0_SEL	R/W	0h	MDL XBAR9 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.29 CONTROLSS_MDLXBAR9_G1 Register

3.21.2.29.1 CONTROLSS_MDLXBAR9_G1 Register (Offset = 344h) [reset = 0h]

MDL XBAR 9 Input Select.

Return to Summary Table

Table 3-3555. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3344h

Figure 3-1821. CONTROLSS_MDLXBAR9_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR9_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR9_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR9_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR9_G1_SEL							
R/W							
0h							

Table 3-3556. CONTROLSS_MDLXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR9_G1_SEL	R/W	0h	MDL XBAR9 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.30 CONTROLSS_MDLXBAR9_G2 Register

3.21.2.30.1 CONTROLSS_MDLXBAR9_G2 Register (Offset = 348h) [reset = 0h]

MDL XBAR 9 Input Select.

Return to Summary Table

Table 3-3557. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3348h

Figure 3-1822. CONTROLSS_MDLXBAR9_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR9_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR9_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR9_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR9_G2_SEL							
R/W							
0h							

Table 3-3558. CONTROLSS_MDLXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR9_G2_SEL	R/W	0h	MDL XBAR9 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.31 CONTROLSS_MDLXBAR10_G0 Register

3.21.2.31.1 CONTROLSS_MDLXBAR10_G0 Register (Offset = 380h) [reset = 0h]

MDL XBAR 10 Input Select.

Return to Summary Table

Table 3-3559. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3380h

Figure 3-1823. CONTROLSS_MDLXBAR10_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR10_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR10_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR10_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR10_G0_SEL							
R/W							
0h							

Table 3-3560. CONTROLSS_MDLXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR10_G0_SEL	R/W	0h	MDL XBAR10 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.32 CONTROLSS_MDLXBAR10_G1 Register

3.21.2.32.1 CONTROLSS_MDLXBAR10_G1 Register (Offset = 384h) [reset = 0h]

MDL XBAR 10 Input Select.

Return to Summary Table

Table 3-3561. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3384h

Figure 3-1824. CONTROLSS_MDLXBAR10_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR10_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR10_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR10_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR10_G1_SEL							
R/W							
0h							

Table 3-3562. CONTROLSS_MDLXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR10_G1_SEL	R/W	0h	MDL XBAR10 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.33 CONTROLSS_MDLXBAR10_G2 Register

3.21.2.33.1 CONTROLSS_MDLXBAR10_G2 Register (Offset = 388h) [reset = 0h]

MDL XBAR 10 Input Select.

Return to Summary Table

Table 3-3563. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3388h

Figure 3-1825. CONTROLSS_MDLXBAR10_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR10_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR10_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR10_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR10_G2_SEL							
R/W							
0h							

Table 3-3564. CONTROLSS_MDLXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR10_G2_SEL	R/W	0h	MDL XBAR10 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.34 CONTROLSS_MDLXBAR11_G0 Register

3.21.2.34.1 CONTROLSS_MDLXBAR11_G0 Register (Offset = 3C0h) [reset = 0h]

MDL XBAR 11 Input Select.

Return to Summary Table

Table 3-3565. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 33C0h

Figure 3-1826. CONTROLSS_MDLXBAR11_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR11_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR11_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR11_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR11_G0_SEL							
R/W							
0h							

Table 3-3566. CONTROLSS_MDLXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR11_G0_SEL	R/W	0h	MDL XBAR11 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.35 CONTROLSS_MDLXBAR11_G1 Register

3.21.2.35.1 CONTROLSS_MDLXBAR11_G1 Register (Offset = 3C4h) [reset = 0h]

MDL XBAR 11 Input Select.

Return to Summary Table

Table 3-3567. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 33C4h

Figure 3-1827. CONTROLSS_MDLXBAR11_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR11_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR11_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR11_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR11_G1_SEL							
R/W							
0h							

Table 3-3568. CONTROLSS_MDLXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR11_G1_SEL	R/W	0h	MDL XBAR11 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.36 CONTROLSS_MDLXBAR11_G2 Register

3.21.2.36.1 CONTROLSS_MDLXBAR11_G2 Register (Offset = 3C8h) [reset = 0h]

MDL XBAR 11 Input Select.

Return to Summary Table

Table 3-3569. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 33C8h

Figure 3-1828. CONTROLSS_MDLXBAR11_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR11_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR11_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR11_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR11_G2_SEL							
R/W							
0h							

Table 3-3570. CONTROLSS_MDLXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR11_G2_SEL	R/W	0h	MDL XBAR11 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.37 CONTROLSS_MDLXBAR12_G0 Register

3.21.2.37.1 CONTROLSS_MDLXBAR12_G0 Register (Offset = 400h) [reset = 0h]

MDL XBAR 12 Input Select.

Return to Summary Table

Table 3-3571. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3400h

Figure 3-1829. CONTROLSS_MDLXBAR12_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR12_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR12_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR12_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR12_G0_SEL							
R/W							
0h							

Table 3-3572. CONTROLSS_MDLXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR12_G0_SEL	R/W	0h	MDL XBAR12 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.38 CONTROLSS_MDLXBAR12_G1 Register

3.21.2.38.1 CONTROLSS_MDLXBAR12_G1 Register (Offset = 404h) [reset = 0h]

MDL XBAR 12 Input Select.

Return to Summary Table

Table 3-3573. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3404h

Figure 3-1830. CONTROLSS_MDLXBAR12_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR12_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR12_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR12_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR12_G1_SEL							
R/W							
0h							

Table 3-3574. CONTROLSS_MDLXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR12_G1_SEL	R/W	0h	MDL XBAR12 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.39 CONTROLSS_MDLXBAR12_G2 Register

3.21.2.39.1 CONTROLSS_MDLXBAR12_G2 Register (Offset = 408h) [reset = 0h]

MDL XBAR 12 Input Select.

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Table 3-3575. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3408h

Figure 3-1831. CONTROLSS_MDLXBAR12_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR12_G2_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MDLXBAR12_G2_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MDLXBAR12_G2_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MDLXBAR12_G2_SEL							
R/W							
0h							

Table 3-3576. CONTROLSS_MDLXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR12_G2_SEL	R/W	0h	MDL XBAR12 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.40 CONTROLSS_MDLXBAR13_G0 Register

3.21.2.40.1 CONTROLSS_MDLXBAR13_G0 Register (Offset = 440h) [reset = 0h]

MDL XBAR 13 Input Select.

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Table 3-3577. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3440h

Figure 3-1832. CONTROLSS_MDLXBAR13_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR13_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR13_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR13_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR13_G0_SEL							
R/W							
0h							

Table 3-3578. CONTROLSS_MDLXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR13_G0_SEL	R/W	0h	MDL XBAR13 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.41 CONTROLSS_MDLXBAR13_G1 Register

3.21.2.41.1 CONTROLSS_MDLXBAR13_G1 Register (Offset = 444h) [reset = 0h]

MDL XBAR 13 Input Select.

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Table 3-3579. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3444h

Figure 3-1833. CONTROLSS_MDLXBAR13_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR13_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR13_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR13_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR13_G1_SEL							
R/W							
0h							

Table 3-3580. CONTROLSS_MDLXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR13_G1_SEL	R/W	0h	MDL XBAR13 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.42 CONTROLSS_MDLXBAR13_G2 Register

3.21.2.42.1 CONTROLSS_MDLXBAR13_G2 Register (Offset = 448h) [reset = 0h]

MDL XBAR 13 Input Select.

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Table 3-3581. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3448h

Figure 3-1834. CONTROLSS_MDLXBAR13_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR13_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR13_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR13_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR13_G2_SEL							
R/W							
0h							

Table 3-3582. CONTROLSS_MDLXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR13_G2_SEL	R/W	0h	MDL XBAR13 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.43 CONTROLSS_MDLXBAR14_G0 Register

3.21.2.43.1 CONTROLSS_MDLXBAR14_G0 Register (Offset = 480h) [reset = 0h]

MDL XBAR 14 Input Select.

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Table 3-3583. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3480h

Figure 3-1835. CONTROLSS_MDLXBAR14_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR14_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR14_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR14_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR14_G0_SEL							
R/W							
0h							

Table 3-3584. CONTROLSS_MDLXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR14_G0_SEL	R/W	0h	MDL XBAR14 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.44 CONTROLSS_MDLXBAR14_G1 Register

3.21.2.44.1 CONTROLSS_MDLXBAR14_G1 Register (Offset = 484h) [reset = 0h]

MDL XBAR 14 Input Select.

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Table 3-3585. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3484h

Figure 3-1836. CONTROLSS_MDLXBAR14_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR14_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR14_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR14_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR14_G1_SEL							
R/W							
0h							

Table 3-3586. CONTROLSS_MDLXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR14_G1_SEL	R/W	0h	MDL XBAR14 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.45 CONTROLSS_MDLXBAR14_G2 Register

3.21.2.45.1 CONTROLSS_MDLXBAR14_G2 Register (Offset = 488h) [reset = 0h]

MDL XBAR 14 Input Select.

Return to Summary Table

Table 3-3587. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3488h

Figure 3-1837. CONTROLSS_MDLXBAR14_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR14_G2_SEL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MDLXBAR14_G2_SEL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MDLXBAR14_G2_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MDLXBAR14_G2_SEL							
R/W							
0h							

Table 3-3588. CONTROLSS_MDLXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR14_G2_SEL	R/W	0h	MDL XBAR14 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.21.2.46 CONTROLSS_MDLXBAR15_G0 Register

3.21.2.46.1 CONTROLSS_MDLXBAR15_G0 Register (Offset = 4C0h) [reset = 0h]

MDL XBAR 15 Input Select .

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Table 3-3589. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 34C0h

Figure 3-1838. CONTROLSS_MDLXBAR15_G0 Name Register

31	30	29	28	27	26	25	24
MDLXBAR15_G0_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR15_G0_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR15_G0_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR15_G0_SEL							
R/W							
0h							

Table 3-3590. CONTROLSS_MDLXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR15_G0_SEL	R/W	0h	MDL XBAR15 G0 input bit select. Input source is PWMA sclk select 1:PWMA sclk bit[x] selected 0:PWMA sclk bit[x] is de-selected

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3.21.2.47 CONTROLSS_MDLXBAR15_G1 Register

3.21.2.47.1 CONTROLSS_MDLXBAR15_G1 Register (Offset = 4C4h) [reset = 0h]

MDL XBAR 15 Input Select .

Return to Summary Table

Table 3-3591. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 34C4h

Figure 3-1839. CONTROLSS_MDLXBAR15_G1 Name Register

31	30	29	28	27	26	25	24
MDLXBAR15_G1_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR15_G1_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR15_G1_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR15_G1_SEL							
R/W							
0h							

Table 3-3592. CONTROLSS_MDLXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR15_G1_SEL	R/W	0h	MDL XBAR15 G1 input bit select. Input source is PWMB sclk select 1:PWMB sclk bit[x] selected 0:PWMB sclk bit[x] is de-selected

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3.21.2.48 CONTROLSS_MDLXBAR15_G2 Register

3.21.2.48.1 CONTROLSS_MDLXBAR15_G2 Register (Offset = 4C8h) [reset = 0h]

MDL XBAR 15 Input Select .

Return to Summary Table

Table 3-3593. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 34C8h

Figure 3-1840. CONTROLSS_MDLXBAR15_G2 Name Register

31	30	29	28	27	26	25	24
MDLXBAR15_G2_SEL							
R/W							
0h							
23	22	21	20	19	18	17	16
MDLXBAR15_G2_SEL							
R/W							
0h							
15	14	13	12	11	10	9	8
MDLXBAR15_G2_SEL							
R/W							
0h							
7	6	5	4	3	2	1	0
MDLXBAR15_G2_SEL							
R/W							
0h							

Table 3-3594. CONTROLSS_MDLXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MDLXBAR15_G2_SEL	R/W	0h	MDL XBAR15 G2 input bit select. Input source is ICSS GPO select y=0 when x =0 to 15, y=1 when x=16 to 31 1:ICSS_PORT[y].GPO[x] selected. 0:ICSS_PORT[y].GPO[x] is de-selected

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3.22 SDFM

SDFM

3.22.1 SDFM Summaries

SDFM Summaries

Table 3-3595. SDFM Registers, Base Address=5026 8000h, Length=4096

Offset	Length	Register Name	SDFM0 Physical Address	SDFM1 Physical Address
0h	32	SDFM_SDIFLG	5026 8000h	5026 9000h
4h	32	SDFM_SDIFLGCLR	5026 8004h	5026 9004h
8h	16	SDFM_SDCTL	5026 8008h	5026 9008h
Ch	16	SDFM_SDMFILEN	5026 800Ch	5026 900Ch
Eh	16	SDFM_SDSTATUS	5026 800Eh	5026 900Eh
10h	16	SDFM_SDINTMODE	5026 8010h	5026 9010h
20h	16	SDFM_SDCTLPARM1	5026 8020h	5026 9020h
22h	16	SDFM_SDDFPARM1	5026 8022h	5026 9022h
24h	16	SDFM_SDDPARM1	5026 8024h	5026 9024h
26h	16	SDFM_SDFLT1CMPH1	5026 8026h	5026 9026h
28h	16	SDFM_SDFLT1CMPL1	5026 8028h	5026 9028h
2Ah	16	SDFM_SDCPARM1	5026 802Ah	5026 902Ah
2Ch	32	SDFM_SDDATA1	5026 802Ch	5026 902Ch
30h	32	SDFM_SDDATFIFO1	5026 8030h	5026 9030h
34h	16	SDFM_SDCDATA1	5026 8034h	5026 9034h
36h	16	SDFM_SDFLT1CMPH2	5026 8036h	5026 9036h
38h	16	SDFM_SDFLT1CMPHZ	5026 8038h	5026 9038h
3Ah	16	SDFM_SDFIFOCTL1	5026 803Ah	5026 903Ah
3Ch	16	SDFM_SDSYNC1	5026 803Ch	5026 903Ch
3Eh	16	SDFM_SDFLT1CMPL2	5026 803Eh	5026 903Eh
40h	16	SDFM_SDCTLPARM2	5026 8040h	5026 9040h
42h	16	SDFM_SDDFPARM2	5026 8042h	5026 9042h
44h	16	SDFM_SDDPARM2	5026 8044h	5026 9044h
46h	16	SDFM_SDFLT2CMPH1	5026 8046h	5026 9046h
48h	16	SDFM_SDFLT2CMPL1	5026 8048h	5026 9048h
4Ah	16	SDFM_SDCPARM2	5026 804Ah	5026 904Ah
4Ch	32	SDFM_SDDATA2	5026 804Ch	5026 904Ch
50h	32	SDFM_SDDATFIFO2	5026 8050h	5026 9050h
54h	16	SDFM_SDCDATA2	5026 8054h	5026 9054h
56h	16	SDFM_SDFLT2CMPH2	5026 8056h	5026 9056h
58h	16	SDFM_SDFLT2CMPHZ	5026 8058h	5026 9058h
5Ah	16	SDFM_SDFIFOCTL2	5026 805Ah	5026 905Ah
5Ch	16	SDFM_SDSYNC2	5026 805Ch	5026 905Ch
5Eh	16	SDFM_SDFLT2CMPL2	5026 805Eh	5026 905Eh
60h	16	SDFM_SDCTLPARM3	5026 8060h	5026 9060h
62h	16	SDFM_SDDFPARM3	5026 8062h	5026 9062h
64h	16	SDFM_SDDPARM3	5026 8064h	5026 9064h
66h	16	SDFM_SDFLT3CMPH1	5026 8066h	5026 9066h
68h	16	SDFM_SDFLT3CMPL1	5026 8068h	5026 9068h
6Ah	16	SDFM_SDCPARM3	5026 806Ah	5026 906Ah

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Table 3-3595. SDFM Registers, Base Address=5026 8000h, Length=4096 (continued)

Offset	Length	Register Name	SDFM0 Physical Address	SDFM1 Physical Address
6Ch	32	SDFM_SDDATA3	5026 806Ch	5026 906Ch
70h	32	SDFM_SDDATFIFO3	5026 8070h	5026 9070h
74h	16	SDFM_SDCDATA3	5026 8074h	5026 9074h
76h	16	SDFM_SDFLT3CMPH2	5026 8076h	5026 9076h
78h	16	SDFM_SDFLT3CMPHZ	5026 8078h	5026 9078h
7Ah	16	SDFM_SDFIFOCTL3	5026 807Ah	5026 907Ah
7Ch	16	SDFM_SDSYNC3	5026 807Ch	5026 907Ch
7Eh	16	SDFM_SDFLT3CMPL2	5026 807Eh	5026 907Eh
80h	16	SDFM_SDCTLPARM4	5026 8080h	5026 9080h
82h	16	SDFM_SDDFPARM4	5026 8082h	5026 9082h
84h	16	SDFM_SDDPARM4	5026 8084h	5026 9084h
86h	16	SDFM_SDFLT4CMPH1	5026 8086h	5026 9086h
88h	16	SDFM_SDFLT4CMPL1	5026 8088h	5026 9088h
8Ah	16	SDFM_SDCPARM4	5026 808Ah	5026 908Ah
8Ch	32	SDFM_SDDATA4	5026 808Ch	5026 908Ch
90h	32	SDFM_SDDATFIFO4	5026 8090h	5026 9090h
94h	16	SDFM_SDCDATA4	5026 8094h	5026 9094h
96h	16	SDFM_SDFLT4CMPH2	5026 8096h	5026 9096h
98h	16	SDFM_SDFLT4CMPHZ	5026 8098h	5026 9098h
9Ah	16	SDFM_SDFIFOCTL4	5026 809Ah	5026 909Ah
9Ch	16	SDFM_SDSYNC4	5026 809Ch	5026 909Ch
9Eh	16	SDFM_SDFLT4CMPL2	5026 809Eh	5026 909Eh
C0h	16	SDFM_SDCOMP1CTL	5026 80C0h	5026 90C0h
C2h	16	SDFM_SDCOMP1EVT2FLTCTL	5026 80C2h	5026 90C2h
C4h	16	SDFM_SDCOMP1EVT2FLTCLKCTL	5026 80C4h	5026 90C4h
C6h	16	SDFM_SDCOMP1EVT1FLTCTL	5026 80C6h	5026 90C6h
C8h	16	SDFM_SDCOMP1EVT1FLTCLKCTL	5026 80C8h	5026 90C8h
CEh	16	SDFM_SDCOMP1LOCK	5026 80CEh	5026 90CEh
D0h	16	SDFM_SDCOMP2CTL	5026 80D0h	5026 90D0h
D2h	16	SDFM_SDCOMP2EVT2FLTCTL	5026 80D2h	5026 90D2h
D4h	16	SDFM_SDCOMP2EVT2FLTCLKCTL	5026 80D4h	5026 90D4h
D6h	16	SDFM_SDCOMP2EVT1FLTCTL	5026 80D6h	5026 90D6h
D8h	16	SDFM_SDCOMP2EVT1FLTCLKCTL	5026 80D8h	5026 90D8h
DEh	16	SDFM_SDCOMP2LOCK	5026 80DEh	5026 90DEh
E0h	16	SDFM_SDCOMP3CTL	5026 80E0h	5026 90E0h
E2h	16	SDFM_SDCOMP3EVT2FLTCTL	5026 80E2h	5026 90E2h
E4h	16	SDFM_SDCOMP3EVT2FLTCLKCTL	5026 80E4h	5026 90E4h
E6h	16	SDFM_SDCOMP3EVT1FLTCTL	5026 80E6h	5026 90E6h
E8h	16	SDFM_SDCOMP3EVT1FLTCLKCTL	5026 80E8h	5026 90E8h
EEh	16	SDFM_SDCOMP3LOCK	5026 80EEh	5026 90EEh
F0h	16	SDFM_SDCOMP4CTL	5026 80F0h	5026 90F0h
F2h	16	SDFM_SDCOMP4EVT2FLTCTL	5026 80F2h	5026 90F2h
F4h	16	SDFM_SDCOMP4EVT2FLTCLKCTL	5026 80F4h	5026 90F4h
F6h	16	SDFM_SDCOMP4EVT1FLTCTL	5026 80F6h	5026 90F6h
F8h	16	SDFM_SDCOMP4EVT1FLTCLKCTL	5026 80F8h	5026 90F8h
FEh	16	SDFM_SDCOMP4LOCK	5026 80FEh	5026 90FEh

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3.22.2 SDFM Registers

SDFM Registers

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3.22.2.1 SDFM_SDIFLG Register

3.22.2.1.1 SDFM_SDIFLG Register (Offset = 0h) [reset = 0h]

SD Interrupt Flag Register.

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Table 3-3596. Instance Table

Instance Name	Physical Address
SDFM0	5026 8000h
SDFM1	5026 9000h

Figure 3-1841. SDFM_SDIFLG Name Register

31	30	29	28	27	26	25	24
MIF	RESERVED_1						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
SDFFINT4	SDFFINT3	SDFFINT2	SDFFINT1	SDFFOVF4	SDFFOVF3	SDFFOVF2	SDFFOVF1
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
FLT4_FLG_CEVT2	FLT4_FLG_CEVT1	FLT3_FLG_CEVT2	FLT3_FLG_CEVT1	FLT2_FLG_CEVT2	FLT2_FLG_CEVT1	FLT1_FLG_CEVT2	FLT1_FLG_CEVT1
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-3597. SDFM_SDIFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	R	0h	Set whenever any "error" interrupt [MF1-4,IFL1-4,IFH1-4,SDFFOVF1-4] is active
30:24	RESERVED_1	R	0h	Reserved
23	SDFFINT4	R	0h	SDFIFO data ready interrupt for Ch4
22	SDFFINT3	R	0h	SDFIFO data ready interrupt for Ch3
21	SDFFINT2	R	0h	SDFIFO data ready interrupt for Ch2
20	SDFFINT1	R	0h	SDFIFO data ready interrupt for Ch1 0: SDFIFO data ready interrupt has NOT occurred 1: SDFIFO data ready interrupt has occurred
19	SDFFOVF4	R	0h	FIFO Overflow Flag for Ch4
18	SDFFOVF3	R	0h	FIFO Overflow Flag for Ch3
17	SDFFOVF2	R	0h	FIFO Overflow Flag for Ch2
16	SDFFOVF1	R	0h	FIFO Overflow Flag for Ch1 0 - FIFO has not overflowed 1 - FIFO overflowed. # words received in FIFO ' FIFO depth [16], NEW word is lost
15	AF4	R	0h	Acknowledge flag for Filter 4 0:No new data available for Filter [in non-FIFO mode] 1:New data available for Filter [in non-FIFO mode]

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Table 3-3597. SDFM_SDIFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	AF3	R	0h	Acknowledge flag for Filter 3 0:No new data available for Filter [in non-FIFO mode] 1:New data available for Filter [in non-FIFO mode]
13	AF2	R	0h	Acknowledge flag for Filter 2 0:No new data available for Filter [in non-FIFO mode] 1:New data available for Filter [in non-FIFO mode]
12	AF1	R	0h	Acknowledge flag for Filter 1 0:No new data available for Filter [in non-FIFO mode] 1:New data available for Filter [in non-FIFO mode]
11	MF4	R	0h	Modulator Failure for Filter 4 0:Modulator is operating normally for Filter 1:Modulator failure for Filter
10	MF3	R	0h	Modulator Failure for Filter 3 0:Modulator is operating normally for Filter 1:Modulator failure for Filter
9	MF2	R	0h	Modulator Failure for Filter 2 0:Modulator is operating normally for Filter 1:Modulator failure for Filter
8	MF1	R	0h	Modulator Failure for Filter 1 0:Modulator is operating normally for Filter 1:Modulator failure for Filter
7	FLT4_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter4 0:CEVT2 event has not occured 1:CEVT2 event has occurred
6	FLT4_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter4 0:CEVT1 event has not occured 1:CEVT1 event has occurred
5	FLT3_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter3 0:CEVT2 event has not occured 1:CEVT2 event has occurred
4	FLT3_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter3 0:CEVT1 event has not occured 1:CEVT1 event has occurred
3	FLT2_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter2 0:CEVT2 event has not occured 1:CEVT2 event has occurred
2	FLT2_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter2 0:CEVT1 event has not occured 1:CEVT1 event has occurred
1	FLT1_FLG_CEVT2	R	0h	CEVT2 Interrupt flag for filter1 0:CEVT2 event has not occured 1:CEVT2 event has occurred
0	FLT1_FLG_CEVT1	R	0h	CEVT1 Interrupt flag for filter1 0:CEVT1 event has not occured 1:CEVT1 event has occurred

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3.22.2.2 SDFM_SDIFLGCLR Register

3.22.2.2.1 SDFM_SDIFLGCLR Register (Offset = 4h) [reset = 0h]

SD Module Interrupt Flag Clear Bits:
Writing a "1" will clear the respective flag bit in the SDIFLG register.
Writes of "0" are ignored.
Note: If user writes a "1" to clear a bit on the same cycle that the hardware is trying to set the bit to "1", then hardware has priority and the bit will not be cleared.

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Table 3-3598. Instance Table

Instance Name	Physical Address
SDFM0	5026 8004h
SDFM1	5026 9004h

Figure 3-1842. SDFM_SDIFLGCLR Name Register

31	30	29	28	27	26	25	24
MIF	RESERVED_1						
R/W1TS	R						
0h	0h						
23	22	21	20	19	18	17	16
SDFFINT4	SDFFINT3	SDFFINT2	SDFFINT1	SDFFOVF4	SDFFOVF3	SDFFOVF2	SDFFOVF1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
AF4	AF3	AF2	AF1	MF4	MF3	MF2	MF1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
FLT4_FLG_CEVT2	FLT4_FLG_CEVT1	FLT3_FLG_CEVT2	FLT3_FLG_CEVT1	FLT2_FLG_CEVT2	FLT2_FLG_CEVT1	FLT1_FLG_CEVT2	FLT1_FLG_CEVT1
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 3-3599. SDFM_SDIFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	R/W1TS	0h	Flag-clear bit for SDFM Master Interrupt flag. Writing a 1 to clear MIF flag in SDIFLG register Writes of "0" are ignored. Note: If the MIF flag is cleared and other Interrupts are still pending, MIF will again be set to 1 on the following SysClk cycle, and the INT output will be reasserted [pulsed low]
30:24	RESERVED_1	R	0h	Reserved
23	SDFFINT4	R/W1TS	0h	SDFIFO data ready Interrupt flag-clear bit for Ch4
22	SDFFINT3	R/W1TS	0h	SDFIFO data ready Interrupt flag-clear bit for Ch3
21	SDFFINT2	R/W1TS	0h	SDFIFO data ready Interrupt flag-clear bit for Ch2
20	SDFFINT1	R/W1TS	0h	SDFIFO data ready Interrupt flag-clear bit for Ch1
19	SDFFOVF4	R/W1TS	0h	SDFIFO overflow clear Ch4
18	SDFFOVF3	R/W1TS	0h	SDFIFO overflow clear Ch3
17	SDFFOVF2	R/W1TS	0h	SDFIFO overflow clear Ch2
16	SDFFOVF1	R/W1TS	0h	SDFIFO overflow clear Ch1
15	AF4	R/W1TS	0h	Flag-clear bit for Acknowledge flag for Filter 4

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Table 3-3599. SDFM_SDIFLGCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	AF3	R/W1TS	0h	Flag Clear bit for AF3
13	AF2	R/W1TS	0h	Flag Clear bit for AF2
12	AF1	R/W1TS	0h	Flag Clear bit for AF1
11	MF4	R/W1TS	0h	Flag Clear bit for MF4
10	MF3	R/W1TS	0h	Flag Clear bit for MF3
9	MF2	R/W1TS	0h	Flag Clear bit for MF2
8	MF1	R/W1TS	0h	Flag Clear bit for MF1
7	FLT4_FLG_CEVT2	R/W1TS	0h	Flag Clear bit for FLT4_FLG_CEVT2
6	FLT4_FLG_CEVT1	R/W1TS	0h	Flag Clear bit for FLT4_FLG_CEVT1
5	FLT3_FLG_CEVT2	R/W1TS	0h	Flag Clear bit for FLT3_FLG_CEVT2
4	FLT3_FLG_CEVT1	R/W1TS	0h	Flag Clear bit for FLT3_FLG_CEVT1
3	FLT2_FLG_CEVT2	R/W1TS	0h	Flag Clear bit for FLT2_FLG_CEVT2
2	FLT2_FLG_CEVT1	R/W1TS	0h	Flag Clear bit for FLT2_FLG_CEVT1
1	FLT1_FLG_CEVT2	R/W1TS	0h	Flag Clear bit for FLT1_FLG_CEVT2
0	FLT1_FLG_CEVT1	R/W1TS	0h	Flag Clear bit for FLT1_FLG_CEVT1

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3.22.2.3 SDFM_SDCTL Register

3.22.2.3.1 SDFM_SDCTL Register (Offset = 8h) [reset = 0h]

SD Control Register.

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Table 3-3600. Instance Table

Instance Name	Physical Address
SDFM0	5026 8008h
SDFM1	5026 9008h

Figure 3-1843. SDFM_SDCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_3	RESERVED_2	MIE	RESERVED_1				
R	R	R/W	R				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				HZ4	HZ3	HZ2	HZ1
R				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h

Table 3-3601. SDFM_SDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_3	R	0h	Reserved
14	RESERVED_2	R	0h	Reserved
13	MIE	R/W	0h	Master SDy_ERR interrupt enable 0:SDy_ERR Interrupt and interrupt flags are disabled 1:SDy_ERR Interrupt and interrupt flags are enabled
12:4	RESERVED_1	R	0h	Reserved
3	HZ4	R/W1TS	0h	Flag Clear bit for HZ4
2	HZ3	R/W1TS	0h	Flag Clear bit for HZ3
1	HZ2	R/W1TS	0h	Flag Clear bit for HZ2
0	HZ1	R/W1TS	0h	Flag Clear bit for HZ1

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3.22.2.4 SDFM_SDMFILEN Register

3.22.2.4.1 SDFM_SDMFILEN Register (Offset = Ch) [reset = 0h]

SD Master Filter Enable.

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Table 3-3602. Instance Table

Instance Name	Physical Address
SDFM0	5026 800Ch
SDFM1	5026 900Ch

Figure 3-1844. SDFM_SDMFILEN Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_7</td><td>RESERVED_6</td><td>MFE</td><td>RESERVED_5</td><td>RESERVED_4</td><td>RESERVED_3</td></tr>
<tr><td colspan="3">R</td><td>R</td><td>R/W</td><td>R</td><td>R</td><td>R</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED_3</td><td colspan="3">RESERVED_2</td><td colspan="4">RESERVED_1</td></tr>
<tr><td>R</td><td colspan="3">R</td><td colspan="4">R</td></tr>
<tr><td>0h</td><td colspan="3">0h</td><td colspan="4">0h</td></tr>
</table>

Table 3-3603. SDFM_SDMFILEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_7	R	0h	Reserved
12	RESERVED_6	R	0h	Reserved
11	MFE	R/W	0h	Master Filter Enable 0:All the four data filter units of SDFM module are disabled. All FIFOs are cleared 1:Data filter units can be enabled if bit FEN is '1'.
10	RESERVED_5	R	0h	Reserved
9	RESERVED_4	R	0h	Reserved
8:7	RESERVED_3	R	0h	Reserved
6:4	RESERVED_2	R	0h	Reserved
3:0	RESERVED_1	R	0h	Reserved

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3.22.2.5 SDFM_SDSTATUS Register

3.22.2.5.1 SDFM_SDSTATUS Register (Offset = Eh) [reset = 0h]

SD Status Register.

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Table 3-3604. Instance Table

Instance Name	Physical Address
SDFM0	5026 800Eh
SDFM1	5026 900Eh

Figure 3-1845. SDFM_SDSTATUS Name Register

15	14	13	12	11	10	9	8
RESERVED_9	RESERVED_8	RESERVED_7	RESERVED_6	RESERVED_5	RESERVED_4	RESERVED_3	RESERVED_2
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1				HZ4	HZ3	HZ2	HZ1
R				R	R	R	R
0h				0h	0h	0h	0h

Table 3-3605. SDFM_SDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_9	R	0h	Reserved
14	RESERVED_8	R	0h	Reserved
13	RESERVED_7	R	0h	Reserved
12	RESERVED_6	R	0h	Reserved
11	RESERVED_5	R	0h	Reserved
10	RESERVED_4	R	0h	Reserved
9	RESERVED_3	R	0h	Reserved
8	RESERVED_2	R	0h	Reserved
7:4	RESERVED_1	R	0h	Reserved
3	HZ4	R	0h	High-level Threshold crossing [Z] flag Ch4 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0:Comparator filter output ' SDCMPHZ4.HLTZ 1:Comparator filter output '= SDCMPHZ4.HLTZ
2	HZ3	R	0h	High-level Threshold crossing [Z] flag Ch3 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0:Comparator filter output ' SDCMPHZ3.HLTZ 1:Comparator filter output '= SDCMPHZ3.HLTZ
1	HZ2	R	0h	High-level Threshold crossing [Z] flag Ch2 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0:Comparator filter output ' SDCMPHZ2.HLTZ 1:Comparator filter output '= SDCMPHZ2.HLTZ

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Table 3-3605. SDFM_SDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HZ1	R	0h	High-level Threshold crossing [Z] flag Ch1 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0:Comparator filter output ' SDCMPHZ1.HLTZ 1:Comparator filter output '= SDCMPHZ1.HLTZ

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3.22.2.6 SDFM_SDINTMODE Register

3.22.2.6.1 SDFM_SDINTMODE Register (Offset = 10h) [reset = 0h]

SD Interrupt Mode register.

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Table 3-3606. Instance Table

Instance Name	Physical Address
SDFM0	5026 8010h
SDFM1	5026 9010h

Figure 3-1846. SDFM_SDINTMODE Name Register

15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							SDINTMODESEL
R							R/W
0h							0h

Table 3-3607. SDFM_SDINTMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED_1	R	0h	Reserved
0	SDINTMODESEL	R/W	0h	CompxH/L events interrupt mode select 0 CompxH/L events are treated as edge signals, rise-edge detect will be done to qualify the event for interrupt generation 1 CompxH/L events are treated as level signals. Rise-edge detect will not be performed and interrupt will be re-asserted if the event remains asserted.

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3.22.2.7 SDFM_SDCTLPARM1 Register

3.22.2.7.1 SDFM_SDCTLPARM1 Register (Offset = 20h) [reset = 0h]

Control Parameter Register for Ch1.

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Table 3-3608. Instance Table

Instance Name	Physical Address
SDFM0	5026 8020h
SDFM1	5026 9020h

Figure 3-1847. SDFM_SDCTLPARM1 Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_3	SDDATASYNC	RESERVED_2	SDCLKSYNC	SDCLKSEL	RESERVED_1	MOD	
R	R/W	R	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 3-3609. SDFM_SDCTLPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_4	R	0h	Reserved
7	RESERVED_3	R	0h	Reserved
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1:SD Data is passed through a synchronizer.
5	RESERVED_2	R	0h	Reserved
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1:SD Clock is passed through a synchronizer.
3	SDCLKSEL	R/W	0h	SD1 Clock source select. 0:Clock source to SDFM filter is its channel clock. 1:Clock source to SDFM filter is SD1 filter clock.
2	RESERVED_1	R/W	0h	Reserved
1:0	MOD	R/W	0h	Modulator clock modes 0:Mode 0:Modulator clock running at 1x data rate 1:Reserved 2:Reserved 3:Reserved

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3.22.2.8 SDFM_SDDFPARM1 Register

3.22.2.8.1 SDFM_SDDFPARM1 Register (Offset = 22h) [reset = 0h]

Data Filter Parameter Register for Ch1.

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Table 3-3610. Instance Table

Instance Name	Physical Address
SDFM0	5026 8022h
SDFM1	5026 9022h

Figure 3-1848. SDFM_SDDFPARM1 Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED_1</td><td>SDSYNCEN</td><td colspan="2">SST</td><td>AE</td><td>FEN</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="2">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DOSR</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 3-3611. SDFM_SDDFPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	SDSYNCEN	R/W	0h	PWM synchronization [SDSYNC] of data filter 0:PWM synchronization of data filter is disabled 1:PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11:10	SST	R/W	0h	Data filter structure 00:Data filter runs with a Sincfast structure 01:Data filter runs with a Sinc1 structure 10:Data filter runs with a Sinc2 structure 11:Data filter runs with a Sinc3 structure
9	AE	R/W	0h	Data filter Acknowledge Enable 0:Acknowledge flag is disabled for the particular filter 1:Acknowledge flag is enabled for the particular filter
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7:0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

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3.22.2.9 SDFM_SDDPARM1 Register

3.22.2.9.1 SDFM_SDDPARM1 Register (Offset = 24h) [reset = 0h]

Data Parameter Register for Ch1.

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Table 3-3612. Instance Table

Instance Name	Physical Address
SDFM0	5026 8024h
SDFM1	5026 9024h

Figure 3-1849. SDFM_SDDPARM1 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED_1	
R/W					R/W	R	
0h					0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							
R							
0h							

Table 3-3613. SDFM_SDDPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	R/W	0h	Data filter Data representation 0:Data stored in 16b2's complement 1:Data stored in 32b2's complement
9:0	RESERVED_1	R	0h	Reserved

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3.22.2.10 SDFM_SDFLT1CMPH1 Register

3.22.2.10.1 SDFM_SDFLT1CMPH1 Register (Offset = 26h) [reset = 7FFFh]

High-level Threshold Register for Ch1.

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Table 3-3614. Instance Table

Instance Name	Physical Address
SDFM0	5026 8026h
SDFM1	5026 9026h

Figure 3-1850. SDFM_SDFLT1CMPH1 Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED_1</td><td colspan="7">HLT</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">7FFFh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">HLT</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7FFFh</td></tr>
</table>

Table 3-3615. SDFM_SDFLT1CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output.

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3.22.2.11 SDFM_SDFLT1CMPL1 Register

3.22.2.11.1 SDFM_SDFLT1CMPL1 Register (Offset = 28h) [reset = 0h]

Low-level Threshold Register for Ch1.

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Table 3-3616. Instance Table

Instance Name	Physical Address
SDFM0	5026 8028h
SDFM1	5026 9028h

Figure 3-1851. SDFM_SDFLT1CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LLT							
R/W							
0h							

Table 3-3617. SDFM_SDFLT1CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output.

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3.22.2.12 SDFM_SDCPARM1 Register

3.22.2.12.1 SDFM_SDCPARM1 Register (Offset = 2Ah) [reset = 0h]

Comparator Filter Parameter Register for Ch1.

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Table 3-3618. Instance Table

Instance Name	Physical Address
SDFM0	5026 802Ah
SDFM1	5026 902Ah

Figure 3-1852. SDFM_SDCPARM1 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W		R/W	R/W		R/W	R/W	R/W
0h		0h	0h		0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 3-3619. SDFM_SDCPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01:COMPL1 OR COMPH1 10:COMPL2 11:COMPL2 OR COMPH2
13	CEN	R/W	0h	Comparator Filter enable 0:Disable comparator filter 1:Enable comparator filter
12:11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01:COMPL1 OR COMPH1 10:COMPH2 11:COMPL2 OR COMPH2
10	HZEN	R/W	0h	High level [Z] Threshold crossing output enable 0:Disable Higher level Threshold [Z] crossing 1:Enable Higher level Threhold [Z] crossing
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0:Disable modulator failure interrupt and its flag 1:Enable modulator failure interrupt and its flag
8:7	CS1_CS0	R/W	0h	Comparator filter structure 00:Comparator filter runs with a sincfast structure 01:Comparator filter runs with a Sinc1 structure 10:Comparator filter runs with a Sinc2 structure 11:Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0:Disable CEVT2 interrupt 1:Enable CEVT2 interrupt
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0:Disable CEVT1 interrupt 1:Enable CEVT1 interrupt
4:0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

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3.22.2.13 SDFM_SDDATA1 Register

3.22.2.13.1 SDFM_SDDATA1 Register (Offset = 2Ch) [reset = 0h]

Data Filter Data Register (16 or 32bit) for Ch1.

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Table 3-3620. Instance Table

Instance Name	Physical Address
SDFM0	5026 802Ch
SDFM1	5026 902Ch

Figure 3-1853. SDFM_SDDATA1 Name Register

31	30	29	28	27	26	25	24
DATA32HI							
R							
0h							
23	22	21	20	19	18	17	16
DATA32HI							
R							
0h							
15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Table 3-3621. SDFM_SDDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16bin 32bmode, 16-bit Data in 16bmode
15:0	DATA16	R	0h	Lo-order 16bin 32bmode

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3.22.2.14 SDFM_SDDATFIFO1 Register

3.22.2.14.1 SDFM_SDDATFIFO1 Register (Offset = 30h) [reset = 0h]

Filter Data FIFO Output(32b) for Ch1.

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Table 3-3622. Instance Table

Instance Name	Physical Address
SDFM0	5026 8030h
SDFM1	5026 9030h

Figure 3-1854. SDFM_SDDATFIFO1 Name Register

31	30	29	28	27	26	25	24
DATA32HI							
R							
0h							
23	22	21	20	19	18	17	16
DATA32HI							
R							
0h							
15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Table 3-3623. SDFM_SDDATFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16bin 32bmode, 16-bit Data in 16bmode
15:0	DATA16	R	0h	Lo-order 16bin 32bmode

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3.22.2.15 SDFM_SDCDATA1 Register

3.22.2.15.1 SDFM_SDCDATA1 Register (Offset = 34h) [reset = 0h]

Comparator Filter Data Register (16b) for Ch1.

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Table 3-3624. Instance Table

Instance Name	Physical Address
SDFM0	5026 8034h
SDFM1	5026 9034h

Figure 3-1855. SDFM_SDCDATA1 Name Register

15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA16							
R							
0h							

Table 3-3625. SDFM_SDCDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA16	R	0h	Comparator Data output - 16bonly

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3.22.2.16 SDFM_SDFLT1CMPH2 Register

3.22.2.16.1 SDFM_SDFLT1CMPH2 Register (Offset = 36h) [reset = 7FFFh]

Second high level threhold for CH1.

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Table 3-3626. Instance Table

Instance Name	Physical Address
SDFM0	5026 8036h
SDFM1	5026 9036h

Figure 3-1856. SDFM_SDFLT1CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT2						
R	R/W						
0h	7FFFh						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HLT2							
R/W							
7FFFh							

Table 3-3627. SDFM_SDFLT1CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output.

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3.22.2.17 SDFM_SDFLT1CMPHZ Register

3.22.2.17.1 SDFM_SDFLT1CMPHZ Register (Offset = 38h) [reset = 0h]

High-level (Z) Threshold Register for Ch1.

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Table 3-3628. Instance Table

Instance Name	Physical Address
SDFM0	5026 8038h
SDFM1	5026 9038h

Figure 3-1857. SDFM_SDFLT1CMPHZ Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED_1</td><td colspan="7">HLTZ</td></tr>
<tr><td>R</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">HLTZ</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 3-3629. SDFM_SDFLT1CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLTZ	R/W	0h	Unsigned High-level threshold [Z] for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

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3.22.2.18 SDFM_SDFIFOCTL1 Register

3.22.2.18.1 SDFM_SDFIFOCTL1 Register (Offset = 3Ah) [reset = 0h]

FIFO Control Register for Ch1.

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Table 3-3630. Instance Table

Instance Name	Physical Address
SDFM0	5026 803Ah
SDFM1	5026 903Ah

Figure 3-1858. SDFM_SDFIFOCTL1 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED_2	SDFFST		
R/W	R/W	R/W	R/W	R	R		
0h	0h	0h	0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDFFST		RESERVED_1	SDFFIL				
R		R	R/W				
0h		0h	0h				

Table 3-3631. SDFM_SDFIFOCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0:SDFIFO Overflow condition will not generate an interrupt 1:SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	R/W	0h	Data-Ready Interrupt [DRINT] source select 0 = AF1 [Select non-FIFO data-ready interrupt] 1 = SDFFINT1 [Select FIFO data-ready interrupt]
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable
11	RESERVED_2	R	0h	Reserved
10:6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED_1	R	0h	Reserved
4:0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status [SDFFST] '= FIFO level [SDFFIL]

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3.22.2.19 SDFM_SDSYNC1 Register

3.22.2.19.1 SDFM_SDSYNC1 Register (Offset = 3Ch) [reset = 400h]

SD Filter Sync control for Ch1.

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Table 3-3632. Instance Table

Instance Name	Physical Address
SDFM0	5026 803Ch
SDFM1	5026 903Ch

Figure 3-1859. SDFM_SDSYNC1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R					R/W	R/W	R/W
0h					1h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WTSYNFLG	WTSYNCEN	SYNCSEL					
R	R/W	R/W					
0h	0h	0h					

Table 3-3633. SDFM_SDSYNC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0:WTSYNFLG can only be cleared manually [using WTSYNCLR bit] 1:WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0:SDFIFO is not automaticaly cleared upon receiving SDSYNC 1:SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	R/W	0h	Wait-for-Sync Flag Clear [always reads 0] 0:Write of 0 has no effect 1:Write of 1 clears WTSYNFLG
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0:SDSYNC event has not occurred 1:SDSYNC event occurred.
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0:Incoming Data written to SDFIFO on every Data-Ready [DR] Event 1:Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5:0	SYNCSEL	R/W	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

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3.22.2.20 SDFM_SDFLT1CMPL2 Register

3.22.2.20.1 SDFM_SDFLT1CMPL2 Register (Offset = 3Eh) [reset = 0h]

Second low level threhold for CH1.

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Table 3-3634. Instance Table

Instance Name	Physical Address
SDFM0	5026 803Eh
SDFM1	5026 903Eh

Figure 3-1860. SDFM_SDFLT1CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT2						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LLT2							
R/W							
0h							

Table 3-3635. SDFM_SDFLT1CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output.

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3.22.2.21 SDFM_SDCTLPARM2 Register

3.22.2.21.1 SDFM_SDCTLPARM2 Register (Offset = 40h) [reset = 0h]

Control Parameter Register for Ch2.

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Table 3-3636. Instance Table

Instance Name	Physical Address
SDFM0	5026 8040h
SDFM1	5026 9040h

Figure 3-1861. SDFM_SDCTLPARM2 Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_3	SDDATASYNC	RESERVED_2	SDCLKSYNC	SDCLKSEL	RESERVED_1	MOD	
R	R/W	R	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 3-3637. SDFM_SDCTLPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_4	R	0h	Reserved
7	RESERVED_3	R	0h	Reserved
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1:SD Data is passed through a synchronizer.
5	RESERVED_2	R	0h	Reserved
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1:SD Clock is passed through a synchronizer.
3	SDCLKSEL	R/W	0h	SD2 Clock source select. 0:Clock source to SDFM filter is its channel clock. 1:Clock source to SDFM filter is SD1 filter clock.
2	RESERVED_1	R/W	0h	Reserved
1:0	MOD	R/W	0h	Modulator clock modes 0:Mode 0:Modulator clock running at 1x data rate 1:Reserved 2:Reserved 3:Reserved

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3.22.2.22 SDFM_SDDFPARM2 Register

3.22.2.22.1 SDFM_SDDFPARM2 Register (Offset = 42h) [reset = 0h]

Data Filter Parameter Register for Ch2.

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Table 3-3638. Instance Table

Instance Name	Physical Address
SDFM0	5026 8042h
SDFM1	5026 9042h

Figure 3-1862. SDFM_SDDFPARM2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			SDSYNCEN	SST		AE	FEN
R			R/W	R/W		R/W	R/W
0h			0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DOSR							
R/W							
0h							

Table 3-3639. SDFM_SDDFPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	SDSYNCEN	R/W	0h	PWM synchronization [SDSYNC] of data filter 0:PWM synchronization of data filter is disabled 1:PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11:10	SST	R/W	0h	Data filter structure 00:Data filter runs with a Sincfast structure 01:Data filter runs with a Sinc1 structure 10:Data filter runs with a Sinc2 structure 11:Data filter runs with a Sinc3 structure
9	AE	R/W	0h	Data filter Acknowledge Enable 0:Acknowledge flag is disabled for the particular filter 1:Acknowledge flag is enabled for the particular filter
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7:0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

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3.22.2.23 SDFM_SDDPARM2 Register

3.22.2.23.1 SDFM_SDDPARM2 Register (Offset = 44h) [reset = 0h]

Data Parameter Register for Ch2.

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Table 3-3640. Instance Table

Instance Name	Physical Address
SDFM0	5026 8044h
SDFM1	5026 9044h

Figure 3-1863. SDFM_SDDPARM2 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED_1	
R/W					R/W	R	
0h					0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							
R							
0h							

Table 3-3641. SDFM_SDDPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	R/W	0h	Data filter Data representation 0:Data stored in 16b2's complement 1:Data stored in 32b2's complement
9:0	RESERVED_1	R	0h	Reserved

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3.22.2.24 SDFM_SDFLT2CMPH1 Register

3.22.2.24.1 SDFM_SDFLT2CMPH1 Register (Offset = 46h) [reset = 7FFFh]

High-level Threshold Register for Ch2.

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Table 3-3642. Instance Table

Instance Name	Physical Address
SDFM0	5026 8046h
SDFM1	5026 9046h

Figure 3-1864. SDFM_SDFLT2CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT						
R	R/W						
0h	7FFFh						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HLT							
R/W							
7FFFh							

Table 3-3643. SDFM_SDFLT2CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output.

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3.22.2.25 SDFM_SDFLT2CMPL1 Register

3.22.2.25.1 SDFM_SDFLT2CMPL1 Register (Offset = 48h) [reset = 0h]

Low-level Threshold Register for Ch2.

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Table 3-3644. Instance Table

Instance Name	Physical Address
SDFM0	5026 8048h
SDFM1	5026 9048h

Figure 3-1865. SDFM_SDFLT2CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LLT							
R/W							
0h							

Table 3-3645. SDFM_SDFLT2CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output.

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3.22.2.26 SDFM_SDCPARM2 Register

3.22.2.26.1 SDFM_SDCPARM2 Register (Offset = 4Ah) [reset = 0h]

Comparator Filter Parameter Register for Ch2.

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Table 3-3646. Instance Table

Instance Name	Physical Address
SDFM0	5026 804Ah
SDFM1	5026 904Ah

Figure 3-1866. SDFM_SDCPARM2 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W		R/W	R/W		R/W	R/W	R/W
0h		0h	0h		0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 3-3647. SDFM_SDCPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01:COMPL1 OR COMPH1 10:COMPL2 11:COMPL2 OR COMPH2
13	CEN	R/W	0h	Comparator Filter enable 0:Disable comparator filter 1:Enable comparator filter
12:11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01:COMPL1 OR COMPH1 10:COMPH2 11:COMPL2 OR COMPH2
10	HZEN	R/W	0h	High level [Z] Threshold crossing output enable 0:Disable Higher level Threshold [Z] crossing 1:Enable Higher level Threhold [Z] crossing
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0:Disable modulator failure interrupt and its flag 1:Enable modulator failure interrupt and its flag
8:7	CS1_CS0	R/W	0h	Comparator filter structure 00:Comparator filter runs with a sincfast structure 01:Comparator filter runs with a Sinc1 structure 10:Comparator filter runs with a Sinc2 structure 11:Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0:Disable CEVT2 interrupt 1:Enable CEVT2 interrupt
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0:Disable CEVT1 interrupt 1:Enable CEVT1 interrupt
4:0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

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3.22.2.27 SDFM_SDDATA2 Register

3.22.2.27.1 SDFM_SDDATA2 Register (Offset = 4Ch) [reset = 0h]

Data Filter Data Register (16 or 32bit) for Ch2.

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Table 3-3648. Instance Table

Instance Name	Physical Address
SDFM0	5026 804Ch
SDFM1	5026 904Ch

Figure 3-1867. SDFM_SDDATA2 Name Register

31	30	29	28	27	26	25	24
DATA32HI							
R							
0h							
23	22	21	20	19	18	17	16
DATA32HI							
R							
0h							
15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Table 3-3649. SDFM_SDDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16bin 32bmode, 16-bit Data in 16bmode
15:0	DATA16	R	0h	Lo-order 16bin 32bmode

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3.22.2.28 SDFM_SDDATFIFO2 Register

3.22.2.28.1 SDFM_SDDATFIFO2 Register (Offset = 50h) [reset = 0h]

Filter Data FIFO Output(32b) for Ch2.

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Table 3-3650. Instance Table

Instance Name	Physical Address
SDFM0	5026 8050h
SDFM1	5026 9050h

Figure 3-1868. SDFM_SDDATFIFO2 Name Register

31	30	29	28	27	26	25	24
DATA32HI							
R							
0h							
23	22	21	20	19	18	17	16
DATA32HI							
R							
0h							
15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Table 3-3651. SDFM_SDDATFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16bin 32bmode, 16-bit Data in 16bmode
15:0	DATA16	R	0h	Lo-order 16bin 32bmode

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3.22.2.29 SDFM_SDCDATA2 Register

3.22.2.29.1 SDFM_SDCDATA2 Register (Offset = 54h) [reset = 0h]

Comparator Filter Data Register (16b) for Ch2.

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Table 3-3652. Instance Table

Instance Name	Physical Address
SDFM0	5026 8054h
SDFM1	5026 9054h

Figure 3-1869. SDFM_SDCDATA2 Name Register

15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA16							
R							
0h							

Table 3-3653. SDFM_SDCDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA16	R	0h	Comparator Data output - 16bonly

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3.22.2.30 SDFM_SDFLT2CMPH2 Register

3.22.2.30.1 SDFM_SDFLT2CMPH2 Register (Offset = 56h) [reset = 7FFFh]

Second high level threhold for CH2.

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Table 3-3654. Instance Table

Instance Name	Physical Address
SDFM0	5026 8056h
SDFM1	5026 9056h

Figure 3-1870. SDFM_SDFLT2CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT2						
R	R/W						
0h	7FFFh						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HLT2							
R/W							
7FFFh							

Table 3-3655. SDFM_SDFLT2CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output.

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3.22.2.31 SDFM_SDFLT2CMPHZ Register

3.22.2.31.1 SDFM_SDFLT2CMPHZ Register (Offset = 58h) [reset = 0h]

High-level (Z) Threshold Register for Ch2.

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Table 3-3656. Instance Table

Instance Name	Physical Address
SDFM0	5026 8058h
SDFM1	5026 9058h

Figure 3-1871. SDFM_SDFLT2CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLTZ						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HLTZ							
R/W							
0h							

Table 3-3657. SDFM_SDFLT2CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLTZ	R/W	0h	Unsigned High-level threshold [Z] for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

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3.22.2.32 SDFM_SDFIFOCTL2 Register

3.22.2.32.1 SDFM_SDFIFOCTL2 Register (Offset = 5Ah) [reset = 0h]

FIFO Control Register for Ch2.

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Table 3-3658. Instance Table

Instance Name	Physical Address
SDFM0	5026 805Ah
SDFM1	5026 905Ah

Figure 3-1872. SDFM_SDFIFOCTL2 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED_2	SDFFST		
R/W	R/W	R/W	R/W	R	R		
0h	0h	0h	0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDFFST		RESERVED_1	SDFFIL				
R		R	R/W				
0h		0h	0h				

Table 3-3659. SDFM_SDFIFOCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0:SDFIFO Overflow condition will not generate an interrupt 1:SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	R/W	0h	Data-Ready Interrupt [DRINT] source select 0 = AF1 [Select non-FIFO data-ready interrupt] 1 = SDFFINT1 [Select FIFO data-ready interrupt]
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable
11	RESERVED_2	R	0h	Reserved
10:6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED_1	R	0h	Reserved
4:0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status [SDFFST] '= FIFO level [SDFFIL]

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3.22.2.33 SDFM_SDSYNC2 Register

3.22.2.33.1 SDFM_SDSYNC2 Register (Offset = 5Ch) [reset = 400h]

SD Filter Sync control for Ch2.

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Table 3-3660. Instance Table

Instance Name	Physical Address
SDFM0	5026 805Ch
SDFM1	5026 905Ch

Figure 3-1873. SDFM_SDSYNC2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R					R/W	R/W	R/W
0h					1h	0h	0h

7	6	5	4	3	2	1	0
WTSYNFLG	WTSYNCEN	SYNCSEL					
R	R/W	R/W					
0h	0h	0h					

Table 3-3661. SDFM_SDSYNC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0:WTSYNFLG can only be cleared manually [using WTSYNCLR bit] 1:WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0:SDFIFO is not automaticaly cleared upon receiving SDSYNC 1:SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	R/W	0h	Wait-for-Sync Flag Clear [always reads 0] 0:Write of 0 has no effect 1:Write of 1 clears WTSYNFLG
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0:SDSYNC event has not occurred 1:SDSYNC event occurred.
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0:Incoming Data written to SDFIFO on every Data-Ready [DR] Event 1:Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5:0	SYNCSEL	R/W	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

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3.22.2.34 SDFM_SDFLT2CMPL2 Register

3.22.2.34.1 SDFM_SDFLT2CMPL2 Register (Offset = 5Eh) [reset = 0h]

Second low level threhold for CH2.

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Table 3-3662. Instance Table

Instance Name	Physical Address
SDFM0	5026 805Eh
SDFM1	5026 905Eh

Figure 3-1874. SDFM_SDFLT2CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT2						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
LLT2							
R/W							
0h							

Table 3-3663. SDFM_SDFLT2CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output.

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3.22.2.35 SDFM_SDCTLPARM3 Register

3.22.2.35.1 SDFM_SDCTLPARM3 Register (Offset = 60h) [reset = 0h]

Control Parameter Register for Ch3.

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Table 3-3664. Instance Table

Instance Name	Physical Address
SDFM0	5026 8060h
SDFM1	5026 9060h

Figure 3-1875. SDFM_SDCTLPARM3 Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_3	SDDATASYNC	RESERVED_2	SDCLKSYNC	SDCLKSEL	RESERVED_1	MOD	
R	R/W	R	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 3-3665. SDFM_SDCTLPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_4	R	0h	Reserved
7	RESERVED_3	R	0h	Reserved
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1:SD Data is passed through a synchronizer.
5	RESERVED_2	R	0h	Reserved
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1:SD Clock is passed through a synchronizer.
3	SDCLKSEL	R/W	0h	SD3 Clock source select. 0:Clock source to SDFM filter is its channel clock. 1:Clock source to SDFM filter is SD1 filter clock.
2	RESERVED_1	R/W	0h	Reserved
1:0	MOD	R/W	0h	Modulator clock modes 0:Mode 0:Modulator clock running at 1x data rate 1:Reserved 2:Reserved 3:Reserved

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3.22.2.36 SDFM_SDDFPARM3 Register

3.22.2.36.1 SDFM_SDDFPARM3 Register (Offset = 62h) [reset = 0h]

Data Filter Parameter Register for Ch3.

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Table 3-3666. Instance Table

Instance Name	Physical Address
SDFM0	5026 8062h
SDFM1	5026 9062h

Figure 3-1876. SDFM_SDDFPARM3 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			SDSYNCEN	SST		AE	FEN
R			R/W	R/W		R/W	R/W
0h			0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DOSR							
R/W							
0h							

Table 3-3667. SDFM_SDDFPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	SDSYNCEN	R/W	0h	PWM synchronization [SDSYNC] of data filter 0:PWM synchronization of data filter is disabled 1:PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11:10	SST	R/W	0h	Data filter structure 00:Data filter runs with a Sincfast structure 01:Data filter runs with a Sinc1 structure 10:Data filter runs with a Sinc2 structure 11:Data filter runs with a Sinc3 structure
9	AE	R/W	0h	Data filter Acknowledge Enable 0:Acknowledge flag is disabled for the particular filter 1:Acknowledge flag is enabled for the particular filter
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7:0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

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3.22.2.37 SDFM_SDDPARM3 Register

3.22.2.37.1 SDFM_SDDPARM3 Register (Offset = 64h) [reset = 0h]

Data Parameter Register for Ch3.

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Table 3-3668. Instance Table

Instance Name	Physical Address
SDFM0	5026 8064h
SDFM1	5026 9064h

Figure 3-1877. SDFM_SDDPARM3 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED_1	
R/W					R/W	R	
0h					0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							
R							
0h							

Table 3-3669. SDFM_SDDPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	R/W	0h	Data filter Data representation 0:Data stored in 16b2's complement 1:Data stored in 32b2's complement
9:0	RESERVED_1	R	0h	Reserved

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3.22.2.38 SDFM_SDFLT3CMPH1 Register

3.22.2.38.1 SDFM_SDFLT3CMPH1 Register (Offset = 66h) [reset = 7FFFh]

High-level Threshold Register for Ch3.

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Table 3-3670. Instance Table

Instance Name	Physical Address
SDFM0	5026 8066h
SDFM1	5026 9066h

Figure 3-1878. SDFM_SDFLT3CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT						
R	R/W						
0h	7FFFh						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HLT							
R/W							
7FFFh							

Table 3-3671. SDFM_SDFLT3CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output.

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3.22.2.39 SDFM_SDFLT3CMPL1 Register

3.22.2.39.1 SDFM_SDFLT3CMPL1 Register (Offset = 68h) [reset = 0h]

Low-level Threshold Register for Ch3.

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Table 3-3672. Instance Table

Instance Name	Physical Address
SDFM0	5026 8068h
SDFM1	5026 9068h

Figure 3-1879. SDFM_SDFLT3CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LLT							
R/W							
0h							

Table 3-3673. SDFM_SDFLT3CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output.

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3.22.2.40 SDFM_SDCPARM3 Register

3.22.2.40.1 SDFM_SDCPARM3 Register (Offset = 6Ah) [reset = 0h]

Comparator Filter Parameter Register for Ch3.

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Table 3-3674. Instance Table

Instance Name	Physical Address
SDFM0	5026 806Ah
SDFM1	5026 906Ah

Figure 3-1880. SDFM_SDCPARM3 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W		R/W	R/W		R/W	R/W	R/W
0h		0h	0h		0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 3-3675. SDFM_SDCPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01:COMPL1 OR COMPH1 10:COMPL2 11:COMPL2 OR COMPH2
13	CEN	R/W	0h	Comparator Filter enable 0:Disable comparator filter 1:Enable comparator filter
12:11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01:COMPL1 OR COMPH1 10:COMPH2 11:COMPL2 OR COMPH2
10	HZEN	R/W	0h	High level [Z] Threshold crossing output enable 0:Disable Higher level Threshold [Z] crossing 1:Enable Higher level Threhold [Z] crossing
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0:Disable modulator failure interrupt and its flag 1:Enable modulator failure interrupt and its flag
8:7	CS1_CS0	R/W	0h	Comparator filter structure 00:Comparator filter runs with a sincfast structure 01:Comparator filter runs with a Sinc1 structure 10:Comparator filter runs with a Sinc2 structure 11:Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0:Disable CEVT2 interrupt 1:Enable CEVT2 interrupt
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0:Disable CEVT1 interrupt 1:Enable CEVT1 interrupt
4:0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

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3.22.2.41 SDFM_SDDATA3 Register

3.22.2.41.1 SDFM_SDDATA3 Register (Offset = 6Ch) [reset = 0h]

Data Filter Data Register (16 or 32bit) for Ch3.

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Table 3-3676. Instance Table

Instance Name	Physical Address
SDFM0	5026 806Ch
SDFM1	5026 906Ch

Figure 3-1881. SDFM_SDDATA3 Name Register

31	30	29	28	27	26	25	24
DATA32HI							
R							
0h							
23	22	21	20	19	18	17	16
DATA32HI							
R							
0h							
15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Table 3-3677. SDFM_SDDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16bin 32bmode, 16-bit Data in 16bmode
15:0	DATA16	R	0h	Lo-order 16bin 32bmode

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3.22.2.42 SDFM_SDDATFIFO3 Register

3.22.2.42.1 SDFM_SDDATFIFO3 Register (Offset = 70h) [reset = 0h]

Filter Data FIFO Output(32b) for Ch3.

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Table 3-3678. Instance Table

Instance Name	Physical Address
SDFM0	5026 8070h
SDFM1	5026 9070h

Figure 3-1882. SDFM_SDDATFIFO3 Name Register

31	30	29	28	27	26	25	24
DATA32HI							
R							
0h							
23	22	21	20	19	18	17	16
DATA32HI							
R							
0h							
15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Table 3-3679. SDFM_SDDATFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16bin 32bmode, 16-bit Data in 16bmode
15:0	DATA16	R	0h	Lo-order 16bin 32bmode

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3.22.2.43 SDFM_SDCDATA3 Register

3.22.2.43.1 SDFM_SDCDATA3 Register (Offset = 74h) [reset = 0h]

Comparator Filter Data Register (16b) for Ch3.

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Table 3-3680. Instance Table

Instance Name	Physical Address
SDFM0	5026 8074h
SDFM1	5026 9074h

Figure 3-1883. SDFM_SDCDATA3 Name Register

15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Table 3-3681. SDFM_SDCDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA16	R	0h	Comparator Data output - 16bonly

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3.22.2.44 SDFM_SDFLT3CMPH2 Register

3.22.2.44.1 SDFM_SDFLT3CMPH2 Register (Offset = 76h) [reset = 7FFFh]

Second high level threhold for CH3.

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Table 3-3682. Instance Table

Instance Name	Physical Address
SDFM0	5026 8076h
SDFM1	5026 9076h

Figure 3-1884. SDFM_SDFLT3CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT2						
R	R/W						
0h	7FFFh						
7	6	5	4	3	2	1	0
HLT2							
R/W							
7FFFh							

Table 3-3683. SDFM_SDFLT3CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output.

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3.22.2.45 SDFM_SDFLT3CMPHZ Register

3.22.2.45.1 SDFM_SDFLT3CMPHZ Register (Offset = 78h) [reset = 0h]

High-level (Z) Threshold Register for Ch3.

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Table 3-3684. Instance Table

Instance Name	Physical Address
SDFM0	5026 8078h
SDFM1	5026 9078h

Figure 3-1885. SDFM_SDFLT3CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLTZ						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
HLTZ							
R/W							
0h							

Table 3-3685. SDFM_SDFLT3CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLTZ	R/W	0h	Unsigned High-level threshold [Z] for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

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3.22.2.46 SDFM_SDFIFOCTL3 Register

3.22.2.46.1 SDFM_SDFIFOCTL3 Register (Offset = 7Ah) [reset = 0h]

FIFO Control Register for Ch3.

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Table 3-3686. Instance Table

Instance Name	Physical Address
SDFM0	5026 807Ah
SDFM1	5026 907Ah

Figure 3-1886. SDFM_SDFIFOCTL3 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED_2	SDFFST		
R/W	R/W	R/W	R/W	R	R		
0h	0h	0h	0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDFFST		RESERVED_1	SDFFIL				
R		R	R/W				
0h		0h	0h				

Table 3-3687. SDFM_SDFIFOCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0:SDFIFO Overflow condition will not generate an interrupt 1:SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	R/W	0h	Data-Ready Interrupt [DRINT] source select 0 = AF1 [Select non-FIFO data-ready interrupt] 1 = SDFFINT1 [Select FIFO data-ready interrupt]
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable
11	RESERVED_2	R	0h	Reserved
10:6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED_1	R	0h	Reserved
4:0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status [SDFFST] '= FIFO level [SDFFIL]

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3.22.2.47 SDFM_SDSYNC3 Register

3.22.2.47.1 SDFM_SDSYNC3 Register (Offset = 7Ch) [reset = 400h]

SD Filter Sync control for Ch3.

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Table 3-3688. Instance Table

Instance Name	Physical Address
SDFM0	5026 807Ch
SDFM1	5026 907Ch

Figure 3-1887. SDFM_SDSYNC3 Name Register

15	14	13	12	11	10	9	8
RESERVED_1					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R					R/W	R/W	R/W
0h					1h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WTSYNFLG	WTSYNCEN	SYNCSEL					
R	R/W	R/W					
0h	0h	0h					

Table 3-3689. SDFM_SDSYNC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0:WTSYNFLG can only be cleared manually [using WTSYNCLR bit] 1:WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0:SDFIFO is not automaticaly cleared upon receiving SDSYNC 1:SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	R/W	0h	Wait-for-Sync Flag Clear [always reads 0] 0:Write of 0 has no effect 1:Write of 1 clears WTSYNFLG
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0:SDSYNC event has not occurred 1:SDSYNC event occurred.
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0:Incoming Data written to SDFIFO on every Data-Ready [DR] Event 1:Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5:0	SYNCSEL	R/W	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

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3.22.2.48 SDFM_SDFLT3CMPL2 Register

3.22.2.48.1 SDFM_SDFLT3CMPL2 Register (Offset = 7Eh) [reset = 0h]

Second low level threhold for CH3.

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Table 3-3690. Instance Table

Instance Name	Physical Address
SDFM0	5026 807Eh
SDFM1	5026 907Eh

Figure 3-1888. SDFM_SDFLT3CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT2						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LLT2							
R/W							
0h							

Table 3-3691. SDFM_SDFLT3CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output.

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3.22.2.49 SDFM_SDCTLPARM4 Register

3.22.2.49.1 SDFM_SDCTLPARM4 Register (Offset = 80h) [reset = 0h]

Control Parameter Register for Ch4.

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Table 3-3692. Instance Table

Instance Name	Physical Address
SDFM0	5026 8080h
SDFM1	5026 9080h

Figure 3-1889. SDFM_SDCTLPARM4 Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_3	SDDATASYNC	RESERVED_2	SDCLKSYNC	SDCLKSEL	RESERVED_1	MOD	
R	R/W	R	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 3-3693. SDFM_SDCTLPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED_4	R	0h	Reserved
7	RESERVED_3	R	0h	Reserved
6	SDDATASYNC	R/W	0h	0: SD Data is not passed through a synchronizer. 1:SD Data is passed through a synchronizer.
5	RESERVED_2	R	0h	Reserved
4	SDCLKSYNC	R/W	0h	0: SD Clock is not passed through a synchronizer. 1:SD Clock is passed through a synchronizer.
3	SDCLKSEL	R/W	0h	SD4 Clock source select. 0:Clock source to SDFM filter is its channel clock. 1:Clock source to SDFM filter is SD1 filter clock.
2	RESERVED_1	R/W	0h	Reserved
1:0	MOD	R/W	0h	Modulator clock modes 0:Mode 0:Modulator clock running at 1x data rate 1:Reserved 2:Reserved 3:Reserved

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3.22.2.50 SDFM_SDDFPARM4 Register

3.22.2.50.1 SDFM_SDDFPARM4 Register (Offset = 82h) [reset = 0h]

Data Filter Parameter Register for Ch4.

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Table 3-3694. Instance Table

Instance Name	Physical Address
SDFM0	5026 8082h
SDFM1	5026 9082h

Figure 3-1890. SDFM_SDDFPARM4 Name Register

15	14	13	12	11	10	9	8
RESERVED_1			SDSYNCEN	SST		AE	FEN
R			R/W	R/W		R/W	R/W
0h			0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DOSR							
R/W							
0h							

Table 3-3695. SDFM_SDDFPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED_1	R	0h	Reserved
12	SDSYNCEN	R/W	0h	PWM synchronization [SDSYNC] of data filter 0:PWM synchronization of data filter is disabled 1:PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11:10	SST	R/W	0h	Data filter structure 00:Data filter runs with a Sincfast structure 01:Data filter runs with a Sinc1 structure 10:Data filter runs with a Sinc2 structure 11:Data filter runs with a Sinc3 structure
9	AE	R/W	0h	Data filter Acknowledge Enable 0:Acknowledge flag is disabled for the particular filter 1:Acknowledge flag is enabled for the particular filter
8	FEN	R/W	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7:0	DOSR	R/W	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

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3.22.2.51 SDFM_SDDPARM4 Register

3.22.2.51.1 SDFM_SDDPARM4 Register (Offset = 84h) [reset = 0h]

Data Parameter Register for Ch4.

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Table 3-3696. Instance Table

Instance Name	Physical Address
SDFM0	5026 8084h
SDFM1	5026 9084h

Figure 3-1891. SDFM_SDDPARM4 Name Register

15	14	13	12	11	10	9	8
SH					DR	RESERVED_1	
R/W					R/W	R	
0h					0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							
R							
0h							

Table 3-3697. SDFM_SDDPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	SH	R/W	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	R/W	0h	Data filter Data representation 0:Data stored in 16b2's complement 1:Data stored in 32b2's complement
9:0	RESERVED_1	R	0h	Reserved

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3.22.2.52 SDFM_SDFLT4CMPH1 Register

3.22.2.52.1 SDFM_SDFLT4CMPH1 Register (Offset = 86h) [reset = 7FFFh]

High-level Threshold Register for Ch4.

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Table 3-3698. Instance Table

Instance Name	Physical Address
SDFM0	5026 8086h
SDFM1	5026 9086h

Figure 3-1892. SDFM_SDFLT4CMPH1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT						
R	R/W						
0h	7FFFh						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HLT							
R/W							
7FFFh							

Table 3-3699. SDFM_SDFLT4CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLT	R/W	7FFFh	Unsigned high-level threshold for the comparator filter output.

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3.22.2.53 SDFM_SDFLT4CMPL1 Register

3.22.2.53.1 SDFM_SDFLT4CMPL1 Register (Offset = 88h) [reset = 0h]

Low-level Threshold Register for Ch4.

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Table 3-3700. Instance Table

Instance Name	Physical Address
SDFM0	5026 8088h
SDFM1	5026 9088h

Figure 3-1893. SDFM_SDFLT4CMPL1 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LLT							
R/W							
0h							

Table 3-3701. SDFM_SDFLT4CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	LLT	R/W	0h	Unsigned low-level threshold for the comparator filter output.

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3.22.2.54 SDFM_SDCPARM4 Register

3.22.2.54.1 SDFM_SDCPARM4 Register (Offset = 8Ah) [reset = 0h]

Comparator Filter Parameter Register for Ch4.

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Table 3-3702. Instance Table

Instance Name	Physical Address
SDFM0	5026 808Ah
SDFM1	5026 908Ah

Figure 3-1894. SDFM_SDCPARM4 Name Register

15	14	13	12	11	10	9	8
CEVT2SEL		CEN	CEVT1SEL		HZEN	MFIE	CS1_CS0
R/W		R/W	R/W		R/W	R/W	R/W
0h		0h	0h		0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CS1_CS0	EN_CEVT2	EN_CEVT1	COSR				
R/W	R/W	R/W	R/W				
0h	0h	0h	0h				

Table 3-3703. SDFM_SDCPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CEVT2SEL	R/W	0h	Comparator Event2 Select 00: COMPL1 01:COMPL1 OR COMPH1 10:COMPL2 11:COMPL2 OR COMPH2
13	CEN	R/W	0h	Comparator Filter enable 0:Disable comparator filter 1:Enable comparator filter
12:11	CEVT1SEL	R/W	0h	Comparator Event1 Select 00: COMPH1 01:COMPL1 OR COMPH1 10:COMPH2 11:COMPL2 OR COMPH2
10	HZEN	R/W	0h	High level [Z] Threshold crossing output enable 0:Disable Higher level Threshold [Z] crossing 1:Enable Higher level Threhold [Z] crossing
9	MFIE	R/W	0h	Modulator Failure Interrupt Enable 0:Disable modulator failure interrupt and its flag 1:Enable modulator failure interrupt and its flag
8:7	CS1_CS0	R/W	0h	Comparator filter structure 00:Comparator filter runs with a sincfast structure 01:Comparator filter runs with a Sinc1 structure 10:Comparator filter runs with a Sinc2 structure 11:Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	R/W	0h	CEVT2 interrupt enable 0:Disable CEVT2 interrupt 1:Enable CEVT2 interrupt
5	EN_CEVT1	R/W	0h	CEVT1 interrupt enable 0:Disable CEVT1 interrupt 1:Enable CEVT1 interrupt
4:0	COSR	R/W	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

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3.22.2.55 SDFM_SDDATA4 Register

3.22.2.55.1 SDFM_SDDATA4 Register (Offset = 8Ch) [reset = 0h]

Data Filter Data Register (16 or 32bit) for Ch4.

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Table 3-3704. Instance Table

Instance Name	Physical Address
SDFM0	5026 808Ch
SDFM1	5026 908Ch

Figure 3-1895. SDFM_SDDATA4 Name Register

31	30	29	28	27	26	25	24
DATA32HI							
R							
0h							
23	22	21	20	19	18	17	16
DATA32HI							
R							
0h							
15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Table 3-3705. SDFM_SDDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16bin 32bmode, 16-bit Data in 16bmode
15:0	DATA16	R	0h	Lo-order 16bin 32bmode

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3.22.2.56 SDFM_SDDATFIFO4 Register

3.22.2.56.1 SDFM_SDDATFIFO4 Register (Offset = 90h) [reset = 0h]

Filter Data FIFO Output(32b) for Ch4.

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Table 3-3706. Instance Table

Instance Name	Physical Address
SDFM0	5026 8090h
SDFM1	5026 9090h

Figure 3-1896. SDFM_SDDATFIFO4 Name Register

31	30	29	28	27	26	25	24
DATA32HI							
R							
0h							
23	22	21	20	19	18	17	16
DATA32HI							
R							
0h							
15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Table 3-3707. SDFM_SDDATFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DATA32HI	R	0h	Hi-order 16bin 32bmode, 16-bit Data in 16bmode
15:0	DATA16	R	0h	Lo-order 16bin 32bmode

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3.22.2.57 SDFM_SDCDATA4 Register

3.22.2.57.1 SDFM_SDCDATA4 Register (Offset = 94h) [reset = 0h]

Comparator Filter Data Register (16b) for Ch4.

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Table 3-3708. Instance Table

Instance Name	Physical Address
SDFM0	5026 8094h
SDFM1	5026 9094h

Figure 3-1897. SDFM_SDCDATA4 Name Register

15	14	13	12	11	10	9	8
DATA16							
R							
0h							
7	6	5	4	3	2	1	0
DATA16							
R							
0h							

Table 3-3709. SDFM_SDCDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DATA16	R	0h	Comparator Data output - 16bonly

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3.22.2.58 SDFM_SDFLT4CMPH2 Register

3.22.2.58.1 SDFM_SDFLT4CMPH2 Register (Offset = 96h) [reset = 7FFFh]

Second high level threhold for CH4.

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Table 3-3710. Instance Table

Instance Name	Physical Address
SDFM0	5026 8096h
SDFM1	5026 9096h

Figure 3-1898. SDFM_SDFLT4CMPH2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLT2						
R	R/W						
0h	7FFFh						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HLT2							
R/W							
7FFFh							

Table 3-3711. SDFM_SDFLT4CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLT2	R/W	7FFFh	Second Unsigned high-level threshold for the comparator filter output.

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3.22.2.59 SDFM_SDFLT4CMPHZ Register

3.22.2.59.1 SDFM_SDFLT4CMPHZ Register (Offset = 98h) [reset = 0h]

High-level (Z) Threshold Register for Ch4.

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Table 3-3712. Instance Table

Instance Name	Physical Address
SDFM0	5026 8098h
SDFM1	5026 9098h

Figure 3-1899. SDFM_SDFLT4CMPHZ Name Register

15	14	13	12	11	10	9	8
RESERVED_1	HLTZ						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HLTZ							
R/W							
0h							

Table 3-3713. SDFM_SDFLT4CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	HLTZ	R/W	0h	Unsigned High-level threshold [Z] for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

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3.22.2.60 SDFM_SDFIFOCTL4 Register

3.22.2.60.1 SDFM_SDFIFOCTL4 Register (Offset = 9Ah) [reset = 0h]

FIFO Control Register for Ch4.

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Table 3-3714. Instance Table

Instance Name	Physical Address
SDFM0	5026 809Ah
SDFM1	5026 909Ah

Figure 3-1900. SDFM_SDFIFOCTL4 Name Register

15	14	13	12	11	10	9	8
OVFIEN	DRINTSEL	FFEN	FFIEN	RESERVED_2	SDFFST		
R/W	R/W	R/W	R/W	R	R		
0h	0h	0h	0h	0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDFFST		RESERVED_1	SDFFIL				
R		R	R/W				
0h		0h	0h				

Table 3-3715. SDFM_SDFIFOCTL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	R/W	0h	SDFIFO Overflow interrupt enable 0:SDFIFO Overflow condition will not generate an interrupt 1:SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	R/W	0h	Data-Ready Interrupt [DRINT] source select 0 = AF1 [Select non-FIFO data-ready interrupt] 1 = SDFFINT1 [Select FIFO data-ready interrupt]
13	FFEN	R/W	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	R/W	0h	SDFIFO data ready Interrupt Enable
11	RESERVED_2	R	0h	Reserved
10:6	SDFFST	R	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED_1	R	0h	Reserved
4:0	SDFFIL	R/W	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status [SDFFST] '= FIFO level [SDFFIL]

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3.22.2.61 SDFM_SDSYNC4 Register

3.22.2.61.1 SDFM_SDSYNC4 Register (Offset = 9Ch) [reset = 400h]

SD Filter Sync control for Ch4.

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Table 3-3716. Instance Table

Instance Name	Physical Address
SDFM0	5026 809Ch
SDFM1	5026 909Ch

Figure 3-1901. SDFM_SDSYNC4 Name Register

15	14	13	12	11	10	9	8
RESERVED_1					WTSCLREN	FFSYNCCLREN	WTSYNCLR
R					R/W	R/W	R/W
0h					1h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WTSYNFLG	WTSYNCEN	SYNCSEL					
R	R/W	R/W					
0h	0h	0h					

Table 3-3717. SDFM_SDSYNC4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED_1	R	0h	Reserved
10	WTSCLREN	R/W	1h	WTSYNFLG Clear-on-FIFOINT Enable 0:WTSYNFLG can only be cleared manually [using WTSYNCLR bit] 1:WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	R/W	0h	FIFO Clear-on-SDSYNC Enable 0:SDFIFO is not automaticaly cleared upon receiving SDSYNC 1:SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	R/W	0h	Wait-for-Sync Flag Clear [always reads 0] 0:Write of 0 has no effect 1:Write of 1 clears WTSYNFLG
7	WTSYNFLG	R	0h	Wait-for-Sync Flag 0:SDSYNC event has not occurred 1:SDSYNC event occurred.
6	WTSYNCEN	R/W	0h	Wait-for-Sync Enable 0:Incoming Data written to SDFIFO on every Data-Ready [DR] Event 1:Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5:0	SYNCSEL	R/W	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

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3.22.2.62 SDFM_SDFLT4CMPL2 Register

3.22.2.62.1 SDFM_SDFLT4CMPL2 Register (Offset = 9Eh) [reset = 0h]

Second low level threhold for CH4.

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Table 3-3718. Instance Table

Instance Name	Physical Address
SDFM0	5026 809Eh
SDFM1	5026 909Eh

Figure 3-1902. SDFM_SDFLT4CMPL2 Name Register

15	14	13	12	11	10	9	8
RESERVED_1	LLT2						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LLT2							
R/W							
0h							

Table 3-3719. SDFM_SDFLT4CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_1	R	0h	Reserved
14:0	LLT2	R/W	0h	Second Unsigned low-level threshold for the comparator filter output.

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3.22.2.63 SDFM_SDCOMP1CTL Register

3.22.2.63.1 SDFM_SDCOMP1CTL Register (Offset = C0h) [reset = 0h]

SD Comparator event filter1 Control Register.

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Table 3-3720. Instance Table

Instance Name	Physical Address
SDFM0	5026 80C0h
SDFM1	5026 90C0h

Figure 3-1903. SDFM_SDCOMP1CTL Name Register

15	14	13	12	11	10	9	8
RESERVED_10	RESERVED_9	RESERVED_8		CEVT2DIGFILTSEL		RESERVED_7	RESERVED_6
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h
7	6	5	4	3	2	1	0
RESERVED_5	RESERVED_4	RESERVED_3		CEVT1DIGFILTSEL		RESERVED_2	RESERVED_1
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h

Table 3-3721. SDFM_SDCOMP1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_10	R	0h	Reserved
14	RESERVED_9	R	0h	Reserved
13:12	RESERVED_8	R	0h	Reserved
11:10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED_7	R	0h	Reserved
8	RESERVED_6	R	0h	Reserved
7	RESERVED_5	R	0h	Reserved
6	RESERVED_4	R	0h	Reserved
5:4	RESERVED_3	R	0h	Reserved
3:2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED_2	R	0h	Reserved
0	RESERVED_1	R	0h	Reserved

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3.22.2.64 SDFM_SDCOMP1EVT2FLTCTL Register

3.22.2.64.1 SDFM_SDCOMP1EVT2FLTCTL Register (Offset = C2h) [reset = 0h]

COMPL/CEVT2 Digital filter1 Control Register.

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Table 3-3722. Instance Table

Instance Name	Physical Address
SDFM0	5026 80C2h
SDFM1	5026 90C2h

Figure 3-1904. SDFM_SDCOMP1EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-3723. SDFM_SDCOMP1EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.22.2.65 SDFM_SDCOMP1EVT2FLTCLKCTL Register

3.22.2.65.1 SDFM_SDCOMP1EVT2FLTCLKCTL Register (Offset = C4h) [reset = 0h]

COMPL/CEVT2 Digital filter1 Clock Control Register.

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Table 3-3724. Instance Table

Instance Name	Physical Address
SDFM0	5026 80C4h
SDFM1	5026 90C4h

Figure 3-1905. SDFM_SDCOMP1EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKPRESCALE							
R/W							
0h							

Table 3-3725. SDFM_SDCOMP1EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples.

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3.22.2.66 SDFM_SDCOMP1EVT1FLTCTL Register

3.22.2.66.1 SDFM_SDCOMP1EVT1FLTCTL Register (Offset = C6h) [reset = 0h]

COMPH/CEVT1 Digital filter1 Control Register.

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Table 3-3726. Instance Table

Instance Name	Physical Address
SDFM0	5026 80C6h
SDFM1	5026 90C6h

Figure 3-1906. SDFM_SDCOMP1EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-3727. SDFM_SDCOMP1EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.22.2.67 SDFM_SDCOMP1EVT1FLTCLKCTL Register

3.22.2.67.1 SDFM_SDCOMP1EVT1FLTCLKCTL Register (Offset = C8h) [reset = 0h]

COMPH/CEVT1 Digital filter1 Clock Control Register.

Return to Summary Table

Table 3-3728. Instance Table

Instance Name	Physical Address
SDFM0	5026 80C8h
SDFM1	5026 90C8h

Figure 3-1907. SDFM_SDCOMP1EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Table 3-3729. SDFM_SDCOMP1EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples.

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3.22.2.68 SDFM_SDCOMP1LOCK Register

3.22.2.68.1 SDFM_SDCOMP1LOCK Register (Offset = CEh) [reset = 0h]

SD compartor event filter1 Lock Register.

Return to Summary Table

Table 3-3730. Instance Table

Instance Name	Physical Address
SDFM0	5026 80CEh
SDFM1	5026 90CEh

Figure 3-1908. SDFM_SDCOMP1LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_4			RESERVED_3	COMP	RESERVED_2	RESERVED_1	SDCOMP1CTL
R			R	R/W1TS	R	R	R/W1TS
0h			0h	0h	0h	0h	0h

Table 3-3731. SDFM_SDCOMP1LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_4	R	0h	Reserved
4	RESERVED_3	R	0h	Reserved
3	COMP	R/W1TS	0h	Lock write-access to the SDCOMP1EVT1/2FLTTCTL and COMP1FILCLKCTL registers. 0 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED_2	R	0h	Reserved
1	RESERVED_1	R	0h	Reserved
0	SDCOMP1CTL	R/W1TS	0h	Lock write-access to the SDCOMP1CTL register. 0 SDCOMP1CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP1CTL register is locked. Only a system reset can clear this bit.

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3.22.2.69 SDFM_SDCOMP2CTL Register

3.22.2.69.1 SDFM_SDCOMP2CTL Register (Offset = D0h) [reset = 0h]

SD Comparator event filter2 Control Register.

Return to Summary Table

Table 3-3732. Instance Table

Instance Name	Physical Address
SDFM0	5026 80D0h
SDFM1	5026 90D0h

Figure 3-1909. SDFM_SDCOMP2CTL Name Register

15	14	13	12	11	10	9	8
RESERVED_10	RESERVED_9	RESERVED_8		CEVT2DIGFILTSEL		RESERVED_7	RESERVED_6
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_5	RESERVED_4	RESERVED_3		CEVT1DIGFILTSEL		RESERVED_2	RESERVED_1
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h

Table 3-3733. SDFM_SDCOMP2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_10	R	0h	Reserved
14	RESERVED_9	R	0h	Reserved
13:12	RESERVED_8	R	0h	Reserved
11:10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED_7	R	0h	Reserved
8	RESERVED_6	R	0h	Reserved
7	RESERVED_5	R	0h	Reserved
6	RESERVED_4	R	0h	Reserved
5:4	RESERVED_3	R	0h	Reserved
3:2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED_2	R	0h	Reserved
0	RESERVED_1	R	0h	Reserved

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3.22.2.70 SDFM_SDCOMP2EVT2FLTCTL Register

3.22.2.70.1 SDFM_SDCOMP2EVT2FLTCTL Register (Offset = D2h) [reset = 0h]

COMPL/CEVT2 Digital filter2 Control Register.

Return to Summary Table

Table 3-3734. Instance Table

Instance Name	Physical Address
SDFM0	5026 80D2h
SDFM1	5026 90D2h

Figure 3-1910. SDFM_SDCOMP2EVT2FLTCTL Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>FILINIT</td><td>RESERVED_2</td><td colspan="5">THRESH</td><td>SAMPWIN</td></tr>
<tr><td>R/W1TS</td><td>R</td><td colspan="5">R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">SAMPWIN</td><td colspan="4">RESERVED_1</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
</table>

Table 3-3735. SDFM_SDCOMP2EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.22.2.71 SDFM_SDCOMP2EVT2FLTCLKCTL Register

3.22.2.71.1 SDFM_SDCOMP2EVT2FLTCLKCTL Register (Offset = D4h) [reset = 0h]

COMPL/CEVT2 Digital filter2 Clock Control Register.

Return to Summary Table

Table 3-3736. Instance Table

Instance Name	Physical Address
SDFM0	5026 80D4h
SDFM1	5026 90D4h

Figure 3-1911. SDFM_SDCOMP2EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKPRESCALE							
R/W							
0h							

Table 3-3737. SDFM_SDCOMP2EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples.

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3.22.2.72 SDFM_SDCOMP2EVT1FLTCTL Register

3.22.2.72.1 SDFM_SDCOMP2EVT1FLTCTL Register (Offset = D6h) [reset = 0h]

COMPH/CEVT1 Digital filter2 Control Register.

Return to Summary Table

Table 3-3738. Instance Table

Instance Name	Physical Address
SDFM0	5026 80D6h
SDFM1	5026 90D6h

Figure 3-1912. SDFM_SDCOMP2EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-3739. SDFM_SDCOMP2EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.22.2.73 SDFM_SDCOMP2EVT1FLTCLKCTL Register

3.22.2.73.1 SDFM_SDCOMP2EVT1FLTCLKCTL Register (Offset = D8h) [reset = 0h]

COMPH/CEVT1 Digital filter2 Clock Control Register.

Return to Summary Table

Table 3-3740. Instance Table

Instance Name	Physical Address
SDFM0	5026 80D8h
SDFM1	5026 90D8h

Figure 3-1913. SDFM_SDCOMP2EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKPRESCALE							
R/W							
0h							

Table 3-3741. SDFM_SDCOMP2EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples.

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3.22.2.74 SDFM_SDCOMP2LOCK Register

3.22.2.74.1 SDFM_SDCOMP2LOCK Register (Offset = DEh) [reset = 0h]

SD compartor event filter2 Lock Register.

Return to Summary Table

Table 3-3742. Instance Table

Instance Name	Physical Address
SDFM0	5026 80DEh
SDFM1	5026 90DEh

Figure 3-1914. SDFM_SDCOMP2LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_4			RESERVED_3	COMP	RESERVED_2	RESERVED_1	SDCOMP2CTL
R			R	R/W1TS	R	R	R/W1TS
0h			0h	0h	0h	0h	0h

Table 3-3743. SDFM_SDCOMP2LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_4	R	0h	Reserved
4	RESERVED_3	R	0h	Reserved
3	COMP	R/W1TS	0h	Lock write-access to the SDCOMP2EVT1/2FLTTCTL and COMP2FILCLKCTL registers. 0 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED_2	R	0h	Reserved
1	RESERVED_1	R	0h	Reserved
0	SDCOMP2CTL	R/W1TS	0h	Lock write-access to the SDCOMP2CTL register. 0 SDCOMP2CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP2CTL register is locked. Only a system reset can clear this bit.

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3.22.2.75 SDFM_SDCOMP3CTL Register

3.22.2.75.1 SDFM_SDCOMP3CTL Register (Offset = E0h) [reset = 0h]

SD Comparator event filter3 Control Register.

Return to Summary Table

Table 3-3744. Instance Table

Instance Name	Physical Address
SDFM0	5026 80E0h
SDFM1	5026 90E0h

Figure 3-1915. SDFM_SDCOMP3CTL Name Register

15	14	13	12	11	10	9	8
RESERVED_10	RESERVED_9	RESERVED_8		CEVT2DIGFILTSEL		RESERVED_7	RESERVED_6
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_5	RESERVED_4	RESERVED_3		CEVT1DIGFILTSEL		RESERVED_2	RESERVED_1
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h

Table 3-3745. SDFM_SDCOMP3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_10	R	0h	Reserved
14	RESERVED_9	R	0h	Reserved
13:12	RESERVED_8	R	0h	Reserved
11:10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED_7	R	0h	Reserved
8	RESERVED_6	R	0h	Reserved
7	RESERVED_5	R	0h	Reserved
6	RESERVED_4	R	0h	Reserved
5:4	RESERVED_3	R	0h	Reserved
3:2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED_2	R	0h	Reserved
0	RESERVED_1	R	0h	Reserved

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3.22.2.76 SDFM_SDCOMP3EVT2FLTCTL Register

3.22.2.76.1 SDFM_SDCOMP3EVT2FLTCTL Register (Offset = E2h) [reset = 0h]

COMPL/CEVT2 Digital filter3 Control Register.

Return to Summary Table

Table 3-3746. Instance Table

Instance Name	Physical Address
SDFM0	5026 80E2h
SDFM1	5026 90E2h

Figure 3-1916. SDFM_SDCOMP3EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-3747. SDFM_SDCOMP3EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.22.2.77 SDFM_SDCOMP3EVT2FLTCLKCTL Register

3.22.2.77.1 SDFM_SDCOMP3EVT2FLTCLKCTL Register (Offset = E4h) [reset = 0h]

COMPL/CEVT2 Digital filter3 Clock Control Register.

Return to Summary Table

Table 3-3748. Instance Table

Instance Name	Physical Address
SDFM0	5026 80E4h
SDFM1	5026 90E4h

Figure 3-1917. SDFM_SDCOMP3EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	

7	6	5	4	3	2	1	0
CLKPRESCALE							
R/W							
0h							

Table 3-3749. SDFM_SDCOMP3EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples.

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3.22.2.78 SDFM_SDCOMP3EVT1FLTCTL Register

3.22.2.78.1 SDFM_SDCOMP3EVT1FLTCTL Register (Offset = E6h) [reset = 0h]

COMPH/CEVT1 Digital filter3 Control Register.

Return to Summary Table

Table 3-3750. Instance Table

Instance Name	Physical Address
SDFM0	5026 80E6h
SDFM1	5026 90E6h

Figure 3-1918. SDFM_SDCOMP3EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-3751. SDFM_SDCOMP3EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.22.2.79 SDFM_SDCOMP3EVT1FLTCLKCTL Register

3.22.2.79.1 SDFM_SDCOMP3EVT1FLTCLKCTL Register (Offset = E8h) [reset = 0h]

COMPH/CEVT1 Digital filter3 Clock Control Register.

Return to Summary Table

Table 3-3752. Instance Table

Instance Name	Physical Address
SDFM0	5026 80E8h
SDFM1	5026 90E8h

Figure 3-1919. SDFM_SDCOMP3EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKPRESCALE							
R/W							
0h							

Table 3-3753. SDFM_SDCOMP3EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples.

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3.22.2.80 SDFM_SDCOMP3LOCK Register

3.22.2.80.1 SDFM_SDCOMP3LOCK Register (Offset = EEh) [reset = 0h]

SD compartor event filter3 Lock Register.

Return to Summary Table

Table 3-3754. Instance Table

Instance Name	Physical Address
SDFM0	5026 80EEh
SDFM1	5026 90EEh

Figure 3-1920. SDFM_SDCOMP3LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							

7	6	5	4	3	2	1	0
RESERVED_4			RESERVED_3	COMP	RESERVED_2	RESERVED_1	SDCOMP3CTL
R			R	R/W1TS	R	R	R/W1TS
0h			0h	0h	0h	0h	0h

Table 3-3755. SDFM_SDCOMP3LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_4	R	0h	Reserved
4	RESERVED_3	R	0h	Reserved
3	COMP	R/W1TS	0h	Lock write-access to the SDCOMP3EVT1/2FLTTCTL and COMP3FILCLKCTL registers. 0 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED_2	R	0h	Reserved
1	RESERVED_1	R	0h	Reserved
0	SDCOMP3CTL	R/W1TS	0h	Lock write-access to the SDCOMP3CTL register. 0 SDCOMP3CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP3CTL register is locked. Only a system reset can clear this bit.

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3.22.2.81 SDFM_SDCOMP4CTL Register

3.22.2.81.1 SDFM_SDCOMP4CTL Register (Offset = F0h) [reset = 0h]

SD Comparator event filter4 Control Register.

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Table 3-3756. Instance Table

Instance Name	Physical Address
SDFM0	5026 80F0h
SDFM1	5026 90F0h

Figure 3-1921. SDFM_SDCOMP4CTL Name Register

15	14	13	12	11	10	9	8
RESERVED_10	RESERVED_9	RESERVED_8		CEVT2DIGFILTSEL		RESERVED_7	RESERVED_6
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_5	RESERVED_4	RESERVED_3		CEVT1DIGFILTSEL		RESERVED_2	RESERVED_1
R	R	R		R/W		R	R
0h	0h	0h		0h		0h	0h

Table 3-3757. SDFM_SDCOMP4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED_10	R	0h	Reserved
14	RESERVED_9	R	0h	Reserved
13:12	RESERVED_8	R	0h	Reserved
11:10	CEVT2DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED_7	R	0h	Reserved
8	RESERVED_6	R	0h	Reserved
7	RESERVED_5	R	0h	Reserved
6	RESERVED_4	R	0h	Reserved
5:4	RESERVED_3	R	0h	Reserved
3:2	CEVT1DIGFILTSEL	R/W	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED_2	R	0h	Reserved
0	RESERVED_1	R	0h	Reserved

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3.22.2.82 SDFM_SDCOMP4EVT2FLTCTL Register

3.22.2.82.1 SDFM_SDCOMP4EVT2FLTCTL Register (Offset = F2h) [reset = 0h]

COMPL/CEVT2 Digital filter4 Control Register.

Return to Summary Table

Table 3-3758. Instance Table

Instance Name	Physical Address
SDFM0	5026 80F2h
SDFM1	5026 90F2h

Figure 3-1922. SDFM_SDCOMP4EVT2FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-3759. SDFM_SDCOMP4EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8:4	SAMPWIN	R/W	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.22.2.83 SDFM_SDCOMP4EVT2FLTCLKCTL Register

3.22.2.83.1 SDFM_SDCOMP4EVT2FLTCLKCTL Register (Offset = F4h) [reset = 0h]

COMPL/CEVT2 Digital filter4 Clock Control Register.

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Table 3-3760. Instance Table

Instance Name	Physical Address
SDFM0	5026 80F4h
SDFM1	5026 90F4h

Figure 3-1923. SDFM_SDCOMP4EVT2FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKPRESCALE							
R/W							
0h							

Table 3-3761. SDFM_SDCOMP4EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	CLKPRESCALE	R/W	0h	Low filter sample clock prescale. Number of system clocks between samples.

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3.22.2.84 SDFM_SDCOMP4EVT1FLTCTL Register

3.22.2.84.1 SDFM_SDCOMP4EVT1FLTCTL Register (Offset = F6h) [reset = 0h]

COMPH/CEVT1 Digital filter4 Control Register.

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Table 3-3762. Instance Table

Instance Name	Physical Address
SDFM0	5026 80F6h
SDFM1	5026 90F6h

Figure 3-1924. SDFM_SDCOMP4EVT1FLTCTL Name Register

15	14	13	12	11	10	9	8
FILINIT	RESERVED_2	THRESH					SAMPWIN
R/W1TS	R	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SAMPWIN				RESERVED_1			
R/W				R			
0h				0h			

Table 3-3763. SDFM_SDCOMP4EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	R/W1TS	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED_2	R	0h	Reserved
13:9	THRESH	R/W	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8:4	SAMPWIN	R/W	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3:0	RESERVED_1	R	0h	Reserved

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3.22.2.85 SDFM_SDCOMP4EVT1FLTCLKCTL Register

3.22.2.85.1 SDFM_SDCOMP4EVT1FLTCLKCTL Register (Offset = F8h) [reset = 0h]

COMPH/CEVT1 Digital filter4 Clock Control Register.

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Table 3-3764. Instance Table

Instance Name	Physical Address
SDFM0	5026 80F8h
SDFM1	5026 90F8h

Figure 3-1925. SDFM_SDCOMP4EVT1FLTCLKCTL Name Register

15	14	13	12	11	10	9	8
RESERVED_1						CLKPRESCALE	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKPRESCALE							
R/W							
0h							

Table 3-3765. SDFM_SDCOMP4EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED_1	R	0h	Reserved
9:0	CLKPRESCALE	R/W	0h	High filter sample clock prescale. Number of system clocks between samples.

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3.22.2.86 SDFM_SDCOMP4LOCK Register

3.22.2.86.1 SDFM_SDCOMP4LOCK Register (Offset = FEh) [reset = 0h]

SD compartor event filter4 Lock Register.

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Table 3-3766. Instance Table

Instance Name	Physical Address
SDFM0	5026 80FEh
SDFM1	5026 90FEh

Figure 3-1926. SDFM_SDCOMP4LOCK Name Register

15	14	13	12	11	10	9	8
RESERVED_4							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_4			RESERVED_3	COMP	RESERVED_2	RESERVED_1	SDCOMP4CTL
R			R	R/W1TS	R	R	R/W1TS
0h			0h	0h	0h	0h	0h

Table 3-3767. SDFM_SDCOMP4LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED_4	R	0h	Reserved
4	RESERVED_3	R	0h	Reserved
3	COMP	R/W1TS	0h	Lock write-access to the SDCOMP4EVT1/2FLTTCTL and COMP4FILCLKCTL registers. 0 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED_2	R	0h	Reserved
1	RESERVED_1	R	0h	Reserved
0	SDCOMP4CTL	R/W1TS	0h	Lock write-access to the SDCOMP4CTL register. 0 SDCOMP4CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP4CTL register is locked. Only a system reset can clear this bit.

4 Processors and Accelerator Registers

The Processor and Accelerator module registers are described in the following sections.

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4.1 R5SS

R5SS

4.1.1 R5SS Summaries

R5SS Summaries

Table 4-1. TCMA_CORE0_ROM Registers, Base Address=0000 0000h, Length=131072

Offset	Length	Register Name	R5SS0 Physical Address
0h	32	TCMA_CORE0_ROM_START	0000 0000h
1FFFCh	32	TCMA_CORE0_ROM_END	0001 FFFCh

Table 4-2. TCMA_CORE0_RAM Registers, Base Address=0002 0000h, Length=32768

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TCMA_CORE0_RAM_START	0002 0000h	0002 0000h
7FFCh	32	TCMA_CORE0_RAM_END	0002 7FFCh	0002 7FFCh

Table 4-3. TCMA_CORE1_RAM Registers, Base Address=0002 0000h, Length=32768

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TCMA_CORE1_RAM_START	0002 0000h	0002 0000h
7FFCh	32	TCMA_CORE1_RAM_END	0002 7FFCh	0002 7FFCh

Table 4-4. TMU_0 Registers, Base Address=0006 0000h, Length=1024

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TMU_0_REVISION	0006 0000h	0006 0000h
40h	32	TMU_0_SINPUF32_R0	0006 0040h	0006 0040h
48h	32	TMU_0_SINPUF32_R1	0006 0048h	0006 0048h
50h	32	TMU_0_SINPUF32_R2	0006 0050h	0006 0050h
58h	32	TMU_0_SINPUF32_R3	0006 0058h	0006 0058h
60h	32	TMU_0_SINPUF32_R4	0006 0060h	0006 0060h
68h	32	TMU_0_SINPUF32_R5	0006 0068h	0006 0068h
70h	32	TMU_0_SINPUF32_R6	0006 0070h	0006 0070h
78h	32	TMU_0_SINPUF32_R7	0006 0078h	0006 0078h
80h	32	TMU_0_COSPUF32_R0	0006 0080h	0006 0080h
88h	32	TMU_0_COSPUF32_R1	0006 0088h	0006 0088h
90h	32	TMU_0_COSPUF32_R2	0006 0090h	0006 0090h
98h	32	TMU_0_COSPUF32_R3	0006 0098h	0006 0098h
A0h	32	TMU_0_COSPUF32_R4	0006 00A0h	0006 00A0h
A8h	32	TMU_0_COSPUF32_R5	0006 00A8h	0006 00A8h
B0h	32	TMU_0_COSPUF32_R6	0006 00B0h	0006 00B0h
B8h	32	TMU_0_COSPUF32_R7	0006 00B8h	0006 00B8h
C0h	32	TMU_0_ATANPUF32_R0	0006 00C0h	0006 00C0h
C8h	32	TMU_0_ATANPUF32_R1	0006 00C8h	0006 00C8h
D0h	32	TMU_0_ATANPUF32_R2	0006 00D0h	0006 00D0h
D8h	32	TMU_0_ATANPUF32_R3	0006 00D8h	0006 00D8h
E0h	32	TMU_0_ATANPUF32_R4	0006 00E0h	0006 00E0h
E8h	32	TMU_0_ATANPUF32_R5	0006 00E8h	0006 00E8h

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Table 4-4. TMU_0 Registers, Base Address=0006 0000h, Length=1024 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
F0h	32	TMU_0_ATANPUF32_R6	0006 00F0h	0006 00F0h
F8h	32	TMU_0_ATANPUF32_R7	0006 00F8h	0006 00F8h
140h	32	TMU_0_IEXP2F32_R0	0006 0140h	0006 0140h
148h	32	TMU_0_IEXP2F32_R1	0006 0148h	0006 0148h
150h	32	TMU_0_IEXP2F32_R2	0006 0150h	0006 0150h
158h	32	TMU_0_IEXP2F32_R3	0006 0158h	0006 0158h
160h	32	TMU_0_IEXP2F32_R4	0006 0160h	0006 0160h
168h	32	TMU_0_IEXP2F32_R5	0006 0168h	0006 0168h
170h	32	TMU_0_IEXP2F32_R6	0006 0170h	0006 0170h
178h	32	TMU_0_IEXP2F32_R7	0006 0178h	0006 0178h
180h	32	TMU_0_LOG2F32_R0	0006 0180h	0006 0180h
188h	32	TMU_0_LOG2F32_R1	0006 0188h	0006 0188h
190h	32	TMU_0_LOG2F32_R2	0006 0190h	0006 0190h
198h	32	TMU_0_LOG2F32_R3	0006 0198h	0006 0198h
1A0h	32	TMU_0_LOG2F32_R4	0006 01A0h	0006 01A0h
1A8h	32	TMU_0_LOG2F32_R5	0006 01A8h	0006 01A8h
1B0h	32	TMU_0_LOG2F32_R6	0006 01B0h	0006 01B0h
1B8h	32	TMU_0_LOG2F32_R7	0006 01B8h	0006 01B8h
1C0h	32	TMU_0_QUADF32_X_R0_R1	0006 01C0h	0006 01C0h
1C8h	32	TMU_0_QUADF32_X_R1_R2	0006 01C8h	0006 01C8h
1D0h	32	TMU_0_QUADF32_X_R2_R3	0006 01D0h	0006 01D0h
1D8h	32	TMU_0_QUADF32_X_R3_R4	0006 01D8h	0006 01D8h
1E0h	32	TMU_0_QUADF32_X_R4_R5	0006 01E0h	0006 01E0h
1E8h	32	TMU_0_QUADF32_X_R5SS0_R6	0006 01E8h	0006 01E8h
1F0h	32	TMU_0_QUADF32_X_R6_R7	0006 01F0h	0006 01F0h
280h	32	TMU_0_RESULT_R0	0006 0280h	0006 0280h
288h	32	TMU_0_RESULT_R1	0006 0288h	0006 0288h
290h	32	TMU_0_RESULT_R2	0006 0290h	0006 0290h
298h	32	TMU_0_RESULT_R3	0006 0298h	0006 0298h
2A0h	32	TMU_0_RESULT_R4	0006 02A0h	0006 02A0h
2A8h	32	TMU_0_RESULT_R5	0006 02A8h	0006 02A8h
2B0h	32	TMU_0_RESULT_R6	0006 02B0h	0006 02B0h
2B8h	32	TMU_0_RESULT_R7	0006 02B8h	0006 02B8h
2C0h	32	TMU_0_CSAVE_R0	0006 02C0h	0006 02C0h
2C8h	32	TMU_0_CSAVE_R1	0006 02C8h	0006 02C8h
2D0h	32	TMU_0_CSAVE_R2	0006 02D0h	0006 02D0h
2D8h	32	TMU_0_CSAVE_R3	0006 02D8h	0006 02D8h
2E0h	32	TMU_0_CSAVE_R4	0006 02E0h	0006 02E0h
2E8h	32	TMU_0_CSAVE_R5	0006 02E8h	0006 02E8h
2F0h	32	TMU_0_CSAVE_R6	0006 02F0h	0006 02F0h
2F8h	32	TMU_0_CSAVE_R7	0006 02F8h	0006 02F8h
300h	32	TMU_0_CSAVE_OP2	0006 0300h	0006 0300h
308h	32	TMU_0_CONTEXT_SAVE	0006 0308h	0006 0308h
310h	32	TMU_0_CONTEXT_RESTORE	0006 0310h	0006 0310h
348h	32	TMU_0_STF	0006 0348h	0006 0348h
380h	32	TMU_0_PARITY_TEST	0006 0380h	0006 0380h
390h	32	TMU_0_LCM_LOCK	0006 0390h	0006 0390h

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Table 4-4. TMU_0 Registers, Base Address=0006 0000h, Length=1024 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
3A0h	32	TMU_0_LCM_COMMIT	0006 03A0h	0006 03A0h

Table 4-5. TMU_1 Registers, Base Address=0006 0000h, Length=1024

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TMU_1_REVISION	0006 0000h	0006 0000h
40h	32	TMU_1_SINPUF32_R0	0006 0040h	0006 0040h
48h	32	TMU_1_SINPUF32_R1	0006 0048h	0006 0048h
50h	32	TMU_1_SINPUF32_R2	0006 0050h	0006 0050h
58h	32	TMU_1_SINPUF32_R3	0006 0058h	0006 0058h
60h	32	TMU_1_SINPUF32_R4	0006 0060h	0006 0060h
68h	32	TMU_1_SINPUF32_R5	0006 0068h	0006 0068h
70h	32	TMU_1_SINPUF32_R6	0006 0070h	0006 0070h
78h	32	TMU_1_SINPUF32_R7	0006 0078h	0006 0078h
80h	32	TMU_1_COSPUF32_R0	0006 0080h	0006 0080h
88h	32	TMU_1_COSPUF32_R1	0006 0088h	0006 0088h
90h	32	TMU_1_COSPUF32_R2	0006 0090h	0006 0090h
98h	32	TMU_1_COSPUF32_R3	0006 0098h	0006 0098h
A0h	32	TMU_1_COSPUF32_R4	0006 00A0h	0006 00A0h
A8h	32	TMU_1_COSPUF32_R5	0006 00A8h	0006 00A8h
B0h	32	TMU_1_COSPUF32_R6	0006 00B0h	0006 00B0h
B8h	32	TMU_1_COSPUF32_R7	0006 00B8h	0006 00B8h
C0h	32	TMU_1_ATANPUF32_R0	0006 00C0h	0006 00C0h
C8h	32	TMU_1_ATANPUF32_R1	0006 00C8h	0006 00C8h
D0h	32	TMU_1_ATANPUF32_R2	0006 00D0h	0006 00D0h
D8h	32	TMU_1_ATANPUF32_R3	0006 00D8h	0006 00D8h
E0h	32	TMU_1_ATANPUF32_R4	0006 00E0h	0006 00E0h
E8h	32	TMU_1_ATANPUF32_R5	0006 00E8h	0006 00E8h
F0h	32	TMU_1_ATANPUF32_R6	0006 00F0h	0006 00F0h
F8h	32	TMU_1_ATANPUF32_R7	0006 00F8h	0006 00F8h
140h	32	TMU_1_IEXP2F32_R0	0006 0140h	0006 0140h
148h	32	TMU_1_IEXP2F32_R1	0006 0148h	0006 0148h
150h	32	TMU_1_IEXP2F32_R2	0006 0150h	0006 0150h
158h	32	TMU_1_IEXP2F32_R3	0006 0158h	0006 0158h
160h	32	TMU_1_IEXP2F32_R4	0006 0160h	0006 0160h
168h	32	TMU_1_IEXP2F32_R5	0006 0168h	0006 0168h
170h	32	TMU_1_IEXP2F32_R6	0006 0170h	0006 0170h
178h	32	TMU_1_IEXP2F32_R7	0006 0178h	0006 0178h
180h	32	TMU_1_LOG2F32_R0	0006 0180h	0006 0180h
188h	32	TMU_1_LOG2F32_R1	0006 0188h	0006 0188h
190h	32	TMU_1_LOG2F32_R2	0006 0190h	0006 0190h
198h	32	TMU_1_LOG2F32_R3	0006 0198h	0006 0198h
1A0h	32	TMU_1_LOG2F32_R4	0006 01A0h	0006 01A0h
1A8h	32	TMU_1_LOG2F32_R5	0006 01A8h	0006 01A8h
1B0h	32	TMU_1_LOG2F32_R6	0006 01B0h	0006 01B0h
1B8h	32	TMU_1_LOG2F32_R7	0006 01B8h	0006 01B8h
1C0h	32	TMU_1_QUADF32_X_R0_R1	0006 01C0h	0006 01C0h

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Table 4-5. TMU_1 Registers, Base Address=0006 0000h, Length=1024 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
1C8h	32	TMU_1_QUADF32_X_R1_R2	0006 01C8h	0006 01C8h
1D0h	32	TMU_1_QUADF32_X_R2_R3	0006 01D0h	0006 01D0h
1D8h	32	TMU_1_QUADF32_X_R3_R4	0006 01D8h	0006 01D8h
1E0h	32	TMU_1_QUADF32_X_R4_R5	0006 01E0h	0006 01E0h
1E8h	32	TMU_1_QUADF32_X_R5SS0_R6	0006 01E8h	0006 01E8h
1F0h	32	TMU_1_QUADF32_X_R6_R7	0006 01F0h	0006 01F0h
280h	32	TMU_1_RESULT_R0	0006 0280h	0006 0280h
288h	32	TMU_1_RESULT_R1	0006 0288h	0006 0288h
290h	32	TMU_1_RESULT_R2	0006 0290h	0006 0290h
298h	32	TMU_1_RESULT_R3	0006 0298h	0006 0298h
2A0h	32	TMU_1_RESULT_R4	0006 02A0h	0006 02A0h
2A8h	32	TMU_1_RESULT_R5	0006 02A8h	0006 02A8h
2B0h	32	TMU_1_RESULT_R6	0006 02B0h	0006 02B0h
2B8h	32	TMU_1_RESULT_R7	0006 02B8h	0006 02B8h
2C0h	32	TMU_1_CSAVE_R0	0006 02C0h	0006 02C0h
2C8h	32	TMU_1_CSAVE_R1	0006 02C8h	0006 02C8h
2D0h	32	TMU_1_CSAVE_R2	0006 02D0h	0006 02D0h
2D8h	32	TMU_1_CSAVE_R3	0006 02D8h	0006 02D8h
2E0h	32	TMU_1_CSAVE_R4	0006 02E0h	0006 02E0h
2E8h	32	TMU_1_CSAVE_R5	0006 02E8h	0006 02E8h
2F0h	32	TMU_1_CSAVE_R6	0006 02F0h	0006 02F0h
2F8h	32	TMU_1_CSAVE_R7	0006 02F8h	0006 02F8h
300h	32	TMU_1_CSAVE_OP2	0006 0300h	0006 0300h
308h	32	TMU_1_CONTEXT_SAVE	0006 0308h	0006 0308h
310h	32	TMU_1_CONTEXT_RESTORE	0006 0310h	0006 0310h
348h	32	TMU_1_STF	0006 0348h	0006 0348h
380h	32	TMU_1_PARITY_TEST	0006 0380h	0006 0380h
390h	32	TMU_1_LCM_LOCK	0006 0390h	0006 0390h
3A0h	32	TMU_1_LCM_COMMIT	0006 03A0h	0006 03A0h

Table 4-6. TCMB_CORE0_RAM Registers, Base Address=0008 0000h, Length=98304

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TCMB_CORE0_RAM_START	0008 0000h	0008 0000h
17FFCh	32	TCMB_CORE0_RAM_END	0009 7FFCh	0009 7FFCh

Table 4-7. TCMB_CORE1_RAM Registers, Base Address=0008 0000h, Length=98304

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TCMB_CORE1_RAM_START	0008 0000h	0008 0000h
17FFCh	32	TCMB_CORE1_RAM_END	0009 7FFCh	0009 7FFCh

Table 4-8. VIM0 Registers, Base Address=50F0 0000h, Length=16384

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	VIM0_PID	50F0 0000h	50F0 0000h
4h	32	VIM0_INFO	50F0 0004h	50F0 0004h
8h	32	VIM0_PRIIRQ	50F0 0008h	50F0 0008h

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Table 4-8. VIM0 Registers, Base Address=50F0 0000h, Length=16384 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
Ch	32	VIM0_PRIFIQ	50F0 000Ch	50F0 000Ch
10h	32	VIM0_IRQGSTS	50F0 0010h	50F0 0010h
14h	32	VIM0_FIQGSTS	50F0 0014h	50F0 0014h
18h	32	VIM0_IRQVEC	50F0 0018h	50F0 0018h
1Ch	32	VIM0_FIQVEC	50F0 001Ch	50F0 001Ch
20h	32	VIM0_ACTIRQ	50F0 0020h	50F0 0020h
24h	32	VIM0_ACTFIQ	50F0 0024h	50F0 0024h
28h	32	VIM0_IRQPRIMSK	50F0 0028h	50F0 0028h
2Ch	32	VIM0_FIQPRIMSK	50F0 002Ch	50F0 002Ch
30h	32	VIM0_DEDVEC	50F0 0030h	50F0 0030h
400h	32	VIM0_RAW_M	50F0 0400h	50F0 0400h
404h	32	VIM0_STS_M	50F0 0404h	50F0 0404h
408h	32	VIM0_INTR_EN_SET_M	50F0 0408h	50F0 0408h
40Ch	32	VIM0_INTER_EN_CLR_M	50F0 040Ch	50F0 040Ch
410h	32	VIM0_IRQSTS_M	50F0 0410h	50F0 0410h
414h	32	VIM0_FIQSTS_M	50F0 0414h	50F0 0414h
418h	32	VIM0_INTMAP_M	50F0 0418h	50F0 0418h
41Ch	32	VIM0_INTTYPE_M	50F0 041Ch	50F0 041Ch
1000h	32	VIM0_INTPRIORITY_Q	50F0 1000h	50F0 1000h
2000h	32	VIM0_INTVECTOR_Q	50F0 2000h	50F0 2000h

Table 4-9. VIM1 Registers, Base Address=50F0 0000h, Length=16384

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	VIM1_PID	50F0 0000h	50F0 0000h
4h	32	VIM1_INFO	50F0 0004h	50F0 0004h
8h	32	VIM1_PRIIRQ	50F0 0008h	50F0 0008h
Ch	32	VIM1_PRIFIQ	50F0 000Ch	50F0 000Ch
10h	32	VIM1_IRQGSTS	50F0 0010h	50F0 0010h
14h	32	VIM1_FIQGSTS	50F0 0014h	50F0 0014h
18h	32	VIM1_IRQVEC	50F0 0018h	50F0 0018h
1Ch	32	VIM1_FIQVEC	50F0 001Ch	50F0 001Ch
20h	32	VIM1_ACTIRQ	50F0 0020h	50F0 0020h
24h	32	VIM1_ACTFIQ	50F0 0024h	50F0 0024h
28h	32	VIM1_IRQPRIMSK	50F0 0028h	50F0 0028h
2Ch	32	VIM1_FIQPRIMSK	50F0 002Ch	50F0 002Ch
30h	32	VIM1_DEDVEC	50F0 0030h	50F0 0030h
400h	32	VIM1_RAW_M	50F0 0400h	50F0 0400h
404h	32	VIM1_STS_M	50F0 0404h	50F0 0404h
408h	32	VIM1_INTR_EN_SET_M	50F0 0408h	50F0 0408h
40Ch	32	VIM1_INTER_EN_CLR_M	50F0 040Ch	50F0 040Ch
410h	32	VIM1_IRQSTS_M	50F0 0410h	50F0 0410h
414h	32	VIM1_FIQSTS_M	50F0 0414h	50F0 0414h
418h	32	VIM1_INTMAP_M	50F0 0418h	50F0 0418h
41Ch	32	VIM1_INTTYPE_M	50F0 041Ch	50F0 041Ch
1000h	32	VIM1_INTPRIORITY_Q	50F0 1000h	50F0 1000h
2000h	32	VIM1_INTVECTOR_Q	50F0 2000h	50F0 2000h

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Table 4-10. ECC_AGG_CORE0 Registers, Base Address=5300 0000h, Length=1024

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	ECC_AGG_CORE0_AGGR_REVISION	5300 0000h	5300 4000h
8h	32	ECC_AGG_CORE0_ECC_VECTOR	5300 0008h	5300 4008h
Ch	32	ECC_AGG_CORE0_MISC_STATUS	5300 000Ch	5300 400Ch
10h	32	ECC_AGG_CORE0_ECC_WRAP_REVISION	5300 0010h	5300 4010h
14h	32	ECC_AGG_CORE0_CONTROL	5300 0014h	5300 4014h
18h	32	ECC_AGG_CORE0_ERROR_CTRL1	5300 0018h	5300 4018h
1Ch	32	ECC_AGG_CORE0_ERROR_CTRL2	5300 001Ch	5300 401Ch
20h	32	ECC_AGG_CORE0_ERROR_STATUS1	5300 0020h	5300 4020h
24h	32	ECC_AGG_CORE0_ERROR_STATUS2	5300 0024h	5300 4024h
28h	32	ECC_AGG_CORE0_ERROR_STATUS3	5300 0028h	5300 4028h
3Ch	32	ECC_AGG_CORE0_SEC_EOI_REG	5300 003Ch	5300 403Ch
40h	32	ECC_AGG_CORE0_SEC_STATUS_REG0	5300 0040h	5300 4040h
80h	32	ECC_AGG_CORE0_SEC_ENABLE_SET_REG0	5300 0080h	5300 4080h
C0h	32	ECC_AGG_CORE0_SEC_ENABLE_CLR_REG0	5300 00C0h	5300 40C0h
13Ch	32	ECC_AGG_CORE0_DED_EOI_REG	5300 013Ch	5300 413Ch
140h	32	ECC_AGG_CORE0_DED_STATUS_REG0	5300 0140h	5300 4140h
180h	32	ECC_AGG_CORE0_DED_ENABLE_SET_REG0	5300 0180h	5300 4180h
1C0h	32	ECC_AGG_CORE0_DED_ENABLE_CLR_REG0	5300 01C0h	5300 41C0h
200h	32	ECC_AGG_CORE0_AGGR_ENABLE_SET	5300 0200h	5300 4200h
204h	32	ECC_AGG_CORE0_AGGR_ENABLE_CLR	5300 0204h	5300 4204h
208h	32	ECC_AGG_CORE0_AGGR_STATUS_SET	5300 0208h	5300 4208h
20Ch	32	ECC_AGG_CORE0_AGGR_STATUS_CLR	5300 020Ch	5300 420Ch

Table 4-11. ECC_AGG_CORE1 Registers, Base Address=5300 3000h, Length=1024

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	ECC_AGG_CORE1_AGGR_REVISION	5300 3000h	5300 7000h
8h	32	ECC_AGG_CORE1_ECC_VECTOR	5300 3008h	5300 7008h
Ch	32	ECC_AGG_CORE1_MISC_STATUS	5300 300Ch	5300 700Ch
10h	32	ECC_AGG_CORE1_ECC_WRAP_REVISION	5300 3010h	5300 7010h
14h	32	ECC_AGG_CORE1_CONTROL	5300 3014h	5300 7014h
18h	32	ECC_AGG_CORE1_ERROR_CTRL1	5300 3018h	5300 7018h
1Ch	32	ECC_AGG_CORE1_ERROR_CTRL2	5300 301Ch	5300 701Ch
20h	32	ECC_AGG_CORE1_ERROR_STATUS1	5300 3020h	5300 7020h
24h	32	ECC_AGG_CORE1_ERROR_STATUS2	5300 3024h	5300 7024h
28h	32	ECC_AGG_CORE1_ERROR_STATUS3	5300 3028h	5300 7028h
3Ch	32	ECC_AGG_CORE1_SEC_EOI_REG	5300 303Ch	5300 703Ch
40h	32	ECC_AGG_CORE1_SEC_STATUS_REG0	5300 3040h	5300 7040h
80h	32	ECC_AGG_CORE1_SEC_ENABLE_SET_REG0	5300 3080h	5300 7080h
C0h	32	ECC_AGG_CORE1_SEC_ENABLE_CLR_REG0	5300 30C0h	5300 70C0h
13Ch	32	ECC_AGG_CORE1_DED_EOI_REG	5300 313Ch	5300 713Ch

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Table 4-11. ECC_AGG_CORE1 Registers, Base Address=5300 3000h, Length=1024 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
140h	32	ECC_AGG_CORE1_DED_STATUS_REG0	5300 3140h	5300 7140h
180h	32	ECC_AGG_CORE1_DED_ENABLE_SET_REG0	5300 3180h	5300 7180h
1C0h	32	ECC_AGG_CORE1_DED_ENABLE_CLR_REG0	5300 31C0h	5300 71C0h
200h	32	ECC_AGG_CORE1_AGGR_ENABLE_SET	5300 3200h	5300 7200h
204h	32	ECC_AGG_CORE1_AGGR_ENABLE_CLR	5300 3204h	5300 7204h
208h	32	ECC_AGG_CORE1_AGGR_STATUS_SET	5300 3208h	5300 7208h
20Ch	32	ECC_AGG_CORE1_AGGR_STATUS_CLR	5300 320Ch	5300 720Ch

Table 4-12. TMU_ROM_CORE0 Registers, Base Address=5302 0000h, Length=8192

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TMU_ROM_CORE0_START	5302 0000h	5302 8000h
2FFCh	32	TMU_ROM_CORE0_END	5302 2FFCh	5302 AFFCh

Table 4-13. TMU_ROM_CORE1 Registers, Base Address=5302 4000h, Length=8192

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TMU_ROM_CORE1_START	5302 4000h	5302 C000h
2FFCh	32	TMU_ROM_CORE1_END	5302 6FFCh	5302 EFFCh

Table 4-14. CCMR Registers, Base Address=5321 0000h, Length=4096

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	CCMR_CCMSR1	5321 0000h	5321 1000h
4h	32	CCMR_CCMKEYR1	5321 0004h	5321 1004h
8h	32	CCMR_CCMSR2	5321 0008h	5321 1008h
Ch	32	CCMR_CCMKEYR2	5321 000Ch	5321 100Ch
10h	32	CCMR_CCMSR3	5321 0010h	5321 1010h
14h	32	CCMR_CCMKEYR3	5321 0014h	5321 1014h
18h	32	CCMR_CCMPOLCNTRL	5321 0018h	5321 1018h
2Ch	32	CCMR_CCMSR5	5321 002Ch	5321 102Ch
30h	32	CCMR_CCMKEYR5	5321 0030h	5321 1030h
34h	32	CCMR_CCMSR6	5321 0034h	5321 1034h
38h	32	CCMR_CCMKEYR6	5321 0038h	5321 1038h

Table 4-15. STC Registers, Base Address=5350 0000h, Length=512

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	STC_STCGCR0	5350 0000h	5351 0000h
4h	32	STC_STCGCR1	5350 0004h	5351 0004h
8h	32	STC_STCTPR	5350 0008h	5351 0008h
Ch	32	STC_STC_CADDR	5350 000Ch	5351 000Ch
10h	32	STC_STCCICR	5350 0010h	5351 0010h
14h	32	STC_STCGSTAT	5350 0014h	5351 0014h
18h	32	STC_STCFSTAT	5350 0018h	5351 0018h
1Ch	32	STC_STCSCSCR	5350 001Ch	5351 001Ch
20h	32	STC_STC_CADDR2	5350 0020h	5351 0020h
24h	32	STC_STC_CLKDIV	5350 0024h	5351 0024h

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Table 4-15. STC Registers, Base Address=5350 0000h, Length=512 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
28h	32	STC_STC_SEGPLR	5350 0028h	5351 0028h
2Ch	32	STC_SEG0_START_ADDR	5350 002Ch	5351 002Ch
30h	32	STC_SEG1_START_ADDR	5350 0030h	5351 0030h
34h	32	STC_SEG2_START_ADDR	5350 0034h	5351 0034h
38h	32	STC_SEG3_START_ADDR	5350 0038h	5351 0038h
3Ch	32	STC_CORE1_CURMISR_0	5350 003Ch	5351 003Ch
40h	32	STC_CORE1_CURMISR_1	5350 0040h	5351 0040h
44h	32	STC_CORE1_CURMISR_2	5350 0044h	5351 0044h
48h	32	STC_CORE1_CURMISR_3	5350 0048h	5351 0048h
4Ch	32	STC_CORE1_CURMISR_4	5350 004Ch	5351 004Ch
50h	32	STC_CORE1_CURMISR_5	5350 0050h	5351 0050h
54h	32	STC_CORE1_CURMISR_6	5350 0054h	5351 0054h
58h	32	STC_CORE1_CURMISR_7	5350 0058h	5351 0058h
5Ch	32	STC_CORE1_CURMISR_8	5350 005Ch	5351 005Ch
60h	32	STC_CORE1_CURMISR_9	5350 0060h	5351 0060h
64h	32	STC_CORE1_CURMISR_10	5350 0064h	5351 0064h
68h	32	STC_CORE1_CURMISR_11	5350 0068h	5351 0068h
6Ch	32	STC_CORE1_CURMISR_12	5350 006Ch	5351 006Ch
70h	32	STC_CORE1_CURMISR_13	5350 0070h	5351 0070h
74h	32	STC_CORE1_CURMISR_14	5350 0074h	5351 0074h
78h	32	STC_CORE1_CURMISR_15	5350 0078h	5351 0078h
7Ch	32	STC_CORE1_CURMISR_16	5350 007Ch	5351 007Ch
80h	32	STC_CORE1_CURMISR_17	5350 0080h	5351 0080h
84h	32	STC_CORE1_CURMISR_18	5350 0084h	5351 0084h
88h	32	STC_CORE1_CURMISR_19	5350 0088h	5351 0088h
8Ch	32	STC_CORE1_CURMISR_20	5350 008Ch	5351 008Ch
90h	32	STC_CORE1_CURMISR_21	5350 0090h	5351 0090h
94h	32	STC_CORE1_CURMISR_22	5350 0094h	5351 0094h
98h	32	STC_CORE1_CURMISR_23	5350 0098h	5351 0098h
9Ch	32	STC_CORE1_CURMISR_24	5350 009Ch	5351 009Ch
A0h	32	STC_CORE1_CURMISR_25	5350 00A0h	5351 00A0h
A4h	32	STC_CORE1_CURMISR_26	5350 00A4h	5351 00A4h
A8h	32	STC_CORE1_CURMISR_27	5350 00A8h	5351 00A8h
ACh	32	STC_CORE2_CURMISR_0	5350 00ACh	5351 00ACh
B0h	32	STC_CORE2_CURMISR_1	5350 00B0h	5351 00B0h
B4h	32	STC_CORE2_CURMISR_2	5350 00B4h	5351 00B4h
B8h	32	STC_CORE2_CURMISR_3	5350 00B8h	5351 00B8h
BCh	32	STC_CORE2_CURMISR_4	5350 00BCh	5351 00BCh
C0h	32	STC_CORE2_CURMISR_5	5350 00C0h	5351 00C0h
C4h	32	STC_CORE2_CURMISR_6	5350 00C4h	5351 00C4h
C8h	32	STC_CORE2_CURMISR_7	5350 00C8h	5351 00C8h
CCh	32	STC_CORE2_CURMISR_8	5350 00CCh	5351 00CCh
D0h	32	STC_CORE2_CURMISR_9	5350 00D0h	5351 00D0h
D4h	32	STC_CORE2_CURMISR_10	5350 00D4h	5351 00D4h
D8h	32	STC_CORE2_CURMISR_11	5350 00D8h	5351 00D8h
DCh	32	STC_CORE2_CURMISR_12	5350 00DCh	5351 00DCh
E0h	32	STC_CORE2_CURMISR_13	5350 00E0h	5351 00E0h

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Table 4-15. STC Registers, Base Address=5350 0000h, Length=512 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
E4h	32	STC_CORE2_CURMISR_14	5350 00E4h	5351 00E4h
E8h	32	STC_CORE2_CURMISR_15	5350 00E8h	5351 00E8h
ECh	32	STC_CORE2_CURMISR_16	5350 00ECh	5351 00ECh
F0h	32	STC_CORE2_CURMISR_17	5350 00F0h	5351 00F0h
F4h	32	STC_CORE2_CURMISR_18	5350 00F4h	5351 00F4h
F8h	32	STC_CORE2_CURMISR_19	5350 00F8h	5351 00F8h
FCh	32	STC_CORE2_CURMISR_20	5350 00FCh	5351 00FCh
100h	32	STC_CORE2_CURMISR_21	5350 0100h	5351 0100h
104h	32	STC_CORE2_CURMISR_22	5350 0104h	5351 0104h
108h	32	STC_CORE2_CURMISR_23	5350 0108h	5351 0108h
10Ch	32	STC_CORE2_CURMISR_24	5350 010Ch	5351 010Ch
110h	32	STC_CORE2_CURMISR_25	5350 0110h	5351 0110h
114h	32	STC_CORE2_CURMISR_26	5350 0114h	5351 0114h
118h	32	STC_CORE2_CURMISR_27	5350 0118h	5351 0118h

Table 4-16. ICACHE_CORE0 Registers, Base Address=7400 0000h, Length=8388608

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	ICACHE_CORE0_START	7400 0000h	7600 0000h
7FFFFCh	32	ICACHE_CORE0_END	747F FFFCh	767F FFFCh

Table 4-17. DCACHE_CORE0 Registers, Base Address=7480 0000h, Length=8388608

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	DCACHE_CORE0_START	7480 0000h	7680 0000h
7FFFFCh	32	DCACHE_CORE0_END	74FF FFFCh	76FF FFFCh

Table 4-18. ICACHE_CORE1 Registers, Base Address=7500 0000h, Length=8388608

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	ICACHE_CORE1_START	7500 0000h	7700 0000h
7FFFFCh	32	ICACHE_CORE1_END	757F FFFCh	777F FFFCh

Table 4-19. DCACHE_CORE1 Registers, Base Address=7580 0000h, Length=8388608

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	DCACHE_CORE1_START	7580 0000h	7780 0000h
7FFFFCh	32	DCACHE_CORE1_END	75FF FFFCh	77FF FFFCh

Table 4-20. TCMA_CORE0 Registers, Base Address=7800 0000h, Length=32768

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TCMA_CORE0_START	7800 0000h	7840 0000h
27FFCh	32	TCMA_CORE0_END	7802 7FFCh	7842 7FFCh

Table 4-21. TMU_EXT_CORE0 Registers, Base Address=7806 0000h, Length=1024

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TMU_EXT_CORE0_REVISION	7806 0000h	7846 0000h
40h	32	TMU_EXT_CORE0_SINPUF32_R0	7806 0040h	7846 0040h

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Table 4-21. TMU_EXT_CORE0 Registers, Base Address=7806 0000h, Length=1024 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
48h	32	TMU_EXT_CORE0_SINPUF32_R1	7806 0048h	7846 0048h
50h	32	TMU_EXT_CORE0_SINPUF32_R2	7806 0050h	7846 0050h
58h	32	TMU_EXT_CORE0_SINPUF32_R3	7806 0058h	7846 0058h
60h	32	TMU_EXT_CORE0_SINPUF32_R4	7806 0060h	7846 0060h
68h	32	TMU_EXT_CORE0_SINPUF32_R5	7806 0068h	7846 0068h
70h	32	TMU_EXT_CORE0_SINPUF32_R6	7806 0070h	7846 0070h
78h	32	TMU_EXT_CORE0_SINPUF32_R7	7806 0078h	7846 0078h
80h	32	TMU_EXT_CORE0_COSPUF32_R0	7806 0080h	7846 0080h
88h	32	TMU_EXT_CORE0_COSPUF32_R1	7806 0088h	7846 0088h
90h	32	TMU_EXT_CORE0_COSPUF32_R2	7806 0090h	7846 0090h
98h	32	TMU_EXT_CORE0_COSPUF32_R3	7806 0098h	7846 0098h
A0h	32	TMU_EXT_CORE0_COSPUF32_R4	7806 00A0h	7846 00A0h
A8h	32	TMU_EXT_CORE0_COSPUF32_R5	7806 00A8h	7846 00A8h
B0h	32	TMU_EXT_CORE0_COSPUF32_R6	7806 00B0h	7846 00B0h
B8h	32	TMU_EXT_CORE0_COSPUF32_R7	7806 00B8h	7846 00B8h
C0h	32	TMU_EXT_CORE0_ATANPUF32_R0	7806 00C0h	7846 00C0h
C8h	32	TMU_EXT_CORE0_ATANPUF32_R1	7806 00C8h	7846 00C8h
D0h	32	TMU_EXT_CORE0_ATANPUF32_R2	7806 00D0h	7846 00D0h
D8h	32	TMU_EXT_CORE0_ATANPUF32_R3	7806 00D8h	7846 00D8h
E0h	32	TMU_EXT_CORE0_ATANPUF32_R4	7806 00E0h	7846 00E0h
E8h	32	TMU_EXT_CORE0_ATANPUF32_R5	7806 00E8h	7846 00E8h
F0h	32	TMU_EXT_CORE0_ATANPUF32_R6	7806 00F0h	7846 00F0h
F8h	32	TMU_EXT_CORE0_ATANPUF32_R7	7806 00F8h	7846 00F8h
140h	32	TMU_EXT_CORE0_IEXP2F32_R0	7806 0140h	7846 0140h
148h	32	TMU_EXT_CORE0_IEXP2F32_R1	7806 0148h	7846 0148h
150h	32	TMU_EXT_CORE0_IEXP2F32_R2	7806 0150h	7846 0150h
158h	32	TMU_EXT_CORE0_IEXP2F32_R3	7806 0158h	7846 0158h
160h	32	TMU_EXT_CORE0_IEXP2F32_R4	7806 0160h	7846 0160h
168h	32	TMU_EXT_CORE0_IEXP2F32_R5	7806 0168h	7846 0168h
170h	32	TMU_EXT_CORE0_IEXP2F32_R6	7806 0170h	7846 0170h
178h	32	TMU_EXT_CORE0_IEXP2F32_R7	7806 0178h	7846 0178h
180h	32	TMU_EXT_CORE0_LOG2F32_R0	7806 0180h	7846 0180h
188h	32	TMU_EXT_CORE0_LOG2F32_R1	7806 0188h	7846 0188h
190h	32	TMU_EXT_CORE0_LOG2F32_R2	7806 0190h	7846 0190h
198h	32	TMU_EXT_CORE0_LOG2F32_R3	7806 0198h	7846 0198h
1A0h	32	TMU_EXT_CORE0_LOG2F32_R4	7806 01A0h	7846 01A0h
1A8h	32	TMU_EXT_CORE0_LOG2F32_R5	7806 01A8h	7846 01A8h
1B0h	32	TMU_EXT_CORE0_LOG2F32_R6	7806 01B0h	7846 01B0h
1B8h	32	TMU_EXT_CORE0_LOG2F32_R7	7806 01B8h	7846 01B8h
1C0h	32	TMU_EXT_CORE0_QUADF32_X_R0_R1	7806 01C0h	7846 01C0h
1C8h	32	TMU_EXT_CORE0_QUADF32_X_R1_R2	7806 01C8h	7846 01C8h
1D0h	32	TMU_EXT_CORE0_QUADF32_X_R2_R3	7806 01D0h	7846 01D0h
1D8h	32	TMU_EXT_CORE0_QUADF32_X_R3_R4	7806 01D8h	7846 01D8h
1E0h	32	TMU_EXT_CORE0_QUADF32_X_R4_R5	7806 01E0h	7846 01E0h
1E8h	32	TMU_EXT_CORE0_QUADF32_X_R5SS0_R6	7806 01E8h	7846 01E8h
1F0h	32	TMU_EXT_CORE0_QUADF32_X_R6_R7	7806 01F0h	7846 01F0h

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Table 4-21. TMU_EXT_CORE0 Registers, Base Address=7806 0000h, Length=1024 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
280h	32	TMU_EXT_CORE0_RESULT_R0	7806 0280h	7846 0280h
288h	32	TMU_EXT_CORE0_RESULT_R1	7806 0288h	7846 0288h
290h	32	TMU_EXT_CORE0_RESULT_R2	7806 0290h	7846 0290h
298h	32	TMU_EXT_CORE0_RESULT_R3	7806 0298h	7846 0298h
2A0h	32	TMU_EXT_CORE0_RESULT_R4	7806 02A0h	7846 02A0h
2A8h	32	TMU_EXT_CORE0_RESULT_R5	7806 02A8h	7846 02A8h
2B0h	32	TMU_EXT_CORE0_RESULT_R6	7806 02B0h	7846 02B0h
2B8h	32	TMU_EXT_CORE0_RESULT_R7	7806 02B8h	7846 02B8h
2C0h	32	TMU_EXT_CORE0_CSAVE_R0	7806 02C0h	7846 02C0h
2C8h	32	TMU_EXT_CORE0_CSAVE_R1	7806 02C8h	7846 02C8h
2D0h	32	TMU_EXT_CORE0_CSAVE_R2	7806 02D0h	7846 02D0h
2D8h	32	TMU_EXT_CORE0_CSAVE_R3	7806 02D8h	7846 02D8h
2E0h	32	TMU_EXT_CORE0_CSAVE_R4	7806 02E0h	7846 02E0h
2E8h	32	TMU_EXT_CORE0_CSAVE_R5	7806 02E8h	7846 02E8h
2F0h	32	TMU_EXT_CORE0_CSAVE_R6	7806 02F0h	7846 02F0h
2F8h	32	TMU_EXT_CORE0_CSAVE_R7	7806 02F8h	7846 02F8h
300h	32	TMU_EXT_CORE0_CSAVE_OP2	7806 0300h	7846 0300h
308h	32	TMU_EXT_CORE0_CONTEXT_SAVE	7806 0308h	7846 0308h
310h	32	TMU_EXT_CORE0_CONTEXT_RESTORE	7806 0310h	7846 0310h
348h	32	TMU_EXT_CORE0_STF	7806 0348h	7846 0348h
380h	32	TMU_EXT_CORE0_PARITY_TEST	7806 0380h	7846 0380h
390h	32	TMU_EXT_CORE0_LCM_LOCK	7806 0390h	7846 0390h
3A0h	32	TMU_EXT_CORE0_LCM_COMMIT	7806 03A0h	7846 03A0h

Table 4-22. TCMB_CORE0 Registers, Base Address=7810 0000h, Length=98304

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TCMB_CORE0_START	7810 0000h	7850 0000h
2FFFCh	32	TCMB_CORE0_END	7812 FFFCh	7852 FFFCh

Table 4-23. TCMA_CORE1 Registers, Base Address=7820 0000h, Length=32768

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TCMA_CORE1_START	7820 0000h	7860 0000h
7FFCh	32	TCMA_CORE1_END	7820 7FFCh	7860 7FFCh

Table 4-24. TMU_EXT_CORE1 Registers, Base Address=7826 0000h, Length=1024

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TMU_EXT_CORE1_REVISION	7826 0000h	7866 0000h
40h	32	TMU_EXT_CORE1_SINPUF32_R0	7826 0040h	7866 0040h
48h	32	TMU_EXT_CORE1_SINPUF32_R1	7826 0048h	7866 0048h
50h	32	TMU_EXT_CORE1_SINPUF32_R2	7826 0050h	7866 0050h
58h	32	TMU_EXT_CORE1_SINPUF32_R3	7826 0058h	7866 0058h
60h	32	TMU_EXT_CORE1_SINPUF32_R4	7826 0060h	7866 0060h
68h	32	TMU_EXT_CORE1_SINPUF32_R5	7826 0068h	7866 0068h
70h	32	TMU_EXT_CORE1_SINPUF32_R6	7826 0070h	7866 0070h
78h	32	TMU_EXT_CORE1_SINPUF32_R7	7826 0078h	7866 0078h

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Table 4-24. TMU_EXT_CORE1 Registers, Base Address=7826 0000h, Length=1024 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
80h	32	TMU_EXT_CORE1_COSPUF32_R0	7826 0080h	7866 0080h
88h	32	TMU_EXT_CORE1_COSPUF32_R1	7826 0088h	7866 0088h
90h	32	TMU_EXT_CORE1_COSPUF32_R2	7826 0090h	7866 0090h
98h	32	TMU_EXT_CORE1_COSPUF32_R3	7826 0098h	7866 0098h
A0h	32	TMU_EXT_CORE1_COSPUF32_R4	7826 00A0h	7866 00A0h
A8h	32	TMU_EXT_CORE1_COSPUF32_R5	7826 00A8h	7866 00A8h
B0h	32	TMU_EXT_CORE1_COSPUF32_R6	7826 00B0h	7866 00B0h
B8h	32	TMU_EXT_CORE1_COSPUF32_R7	7826 00B8h	7866 00B8h
C0h	32	TMU_EXT_CORE1_ATANPUF32_R0	7826 00C0h	7866 00C0h
C8h	32	TMU_EXT_CORE1_ATANPUF32_R1	7826 00C8h	7866 00C8h
D0h	32	TMU_EXT_CORE1_ATANPUF32_R2	7826 00D0h	7866 00D0h
D8h	32	TMU_EXT_CORE1_ATANPUF32_R3	7826 00D8h	7866 00D8h
E0h	32	TMU_EXT_CORE1_ATANPUF32_R4	7826 00E0h	7866 00E0h
E8h	32	TMU_EXT_CORE1_ATANPUF32_R5	7826 00E8h	7866 00E8h
F0h	32	TMU_EXT_CORE1_ATANPUF32_R6	7826 00F0h	7866 00F0h
F8h	32	TMU_EXT_CORE1_ATANPUF32_R7	7826 00F8h	7866 00F8h
140h	32	TMU_EXT_CORE1_IEXP2F32_R0	7826 0140h	7866 0140h
148h	32	TMU_EXT_CORE1_IEXP2F32_R1	7826 0148h	7866 0148h
150h	32	TMU_EXT_CORE1_IEXP2F32_R2	7826 0150h	7866 0150h
158h	32	TMU_EXT_CORE1_IEXP2F32_R3	7826 0158h	7866 0158h
160h	32	TMU_EXT_CORE1_IEXP2F32_R4	7826 0160h	7866 0160h
168h	32	TMU_EXT_CORE1_IEXP2F32_R5	7826 0168h	7866 0168h
170h	32	TMU_EXT_CORE1_IEXP2F32_R6	7826 0170h	7866 0170h
178h	32	TMU_EXT_CORE1_IEXP2F32_R7	7826 0178h	7866 0178h
180h	32	TMU_EXT_CORE1_LOG2F32_R0	7826 0180h	7866 0180h
188h	32	TMU_EXT_CORE1_LOG2F32_R1	7826 0188h	7866 0188h
190h	32	TMU_EXT_CORE1_LOG2F32_R2	7826 0190h	7866 0190h
198h	32	TMU_EXT_CORE1_LOG2F32_R3	7826 0198h	7866 0198h
1A0h	32	TMU_EXT_CORE1_LOG2F32_R4	7826 01A0h	7866 01A0h
1A8h	32	TMU_EXT_CORE1_LOG2F32_R5	7826 01A8h	7866 01A8h
1B0h	32	TMU_EXT_CORE1_LOG2F32_R6	7826 01B0h	7866 01B0h
1B8h	32	TMU_EXT_CORE1_LOG2F32_R7	7826 01B8h	7866 01B8h
1C0h	32	TMU_EXT_CORE1_QUADF32_X_R0_R1	7826 01C0h	7866 01C0h
1C8h	32	TMU_EXT_CORE1_QUADF32_X_R1_R2	7826 01C8h	7866 01C8h
1D0h	32	TMU_EXT_CORE1_QUADF32_X_R2_R3	7826 01D0h	7866 01D0h
1D8h	32	TMU_EXT_CORE1_QUADF32_X_R3_R4	7826 01D8h	7866 01D8h
1E0h	32	TMU_EXT_CORE1_QUADF32_X_R4_R5	7826 01E0h	7866 01E0h
1E8h	32	TMU_EXT_CORE1_QUADF32_X_R5SS0_R6	7826 01E8h	7866 01E8h
1F0h	32	TMU_EXT_CORE1_QUADF32_X_R6_R7	7826 01F0h	7866 01F0h
280h	32	TMU_EXT_CORE1_RESULT_R0	7826 0280h	7866 0280h
288h	32	TMU_EXT_CORE1_RESULT_R1	7826 0288h	7866 0288h
290h	32	TMU_EXT_CORE1_RESULT_R2	7826 0290h	7866 0290h
298h	32	TMU_EXT_CORE1_RESULT_R3	7826 0298h	7866 0298h
2A0h	32	TMU_EXT_CORE1_RESULT_R4	7826 02A0h	7866 02A0h
2A8h	32	TMU_EXT_CORE1_RESULT_R5	7826 02A8h	7866 02A8h
2B0h	32	TMU_EXT_CORE1_RESULT_R6	7826 02B0h	7866 02B0h

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Table 4-24. TMU_EXT_CORE1 Registers, Base Address=7826 0000h, Length=1024 (continued)

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
2B8h	32	TMU_EXT_CORE1_RESULT_R7	7826 02B8h	7866 02B8h
2C0h	32	TMU_EXT_CORE1_CSAVE_R0	7826 02C0h	7866 02C0h
2C8h	32	TMU_EXT_CORE1_CSAVE_R1	7826 02C8h	7866 02C8h
2D0h	32	TMU_EXT_CORE1_CSAVE_R2	7826 02D0h	7866 02D0h
2D8h	32	TMU_EXT_CORE1_CSAVE_R3	7826 02D8h	7866 02D8h
2E0h	32	TMU_EXT_CORE1_CSAVE_R4	7826 02E0h	7866 02E0h
2E8h	32	TMU_EXT_CORE1_CSAVE_R5	7826 02E8h	7866 02E8h
2F0h	32	TMU_EXT_CORE1_CSAVE_R6	7826 02F0h	7866 02F0h
2F8h	32	TMU_EXT_CORE1_CSAVE_R7	7826 02F8h	7866 02F8h
300h	32	TMU_EXT_CORE1_CSAVE_OP2	7826 0300h	7866 0300h
308h	32	TMU_EXT_CORE1_CONTEXT_SAVE	7826 0308h	7866 0308h
310h	32	TMU_EXT_CORE1_CONTEXT_RESTORE	7826 0310h	7866 0310h
348h	32	TMU_EXT_CORE1_STF	7826 0348h	7866 0348h
380h	32	TMU_EXT_CORE1_PARITY_TEST	7826 0380h	7866 0380h
390h	32	TMU_EXT_CORE1_LCM_LOCK	7826 0390h	7866 0390h
3A0h	32	TMU_EXT_CORE1_LCM_COMMIT	7826 03A0h	7866 03A0h

Table 4-25. TCMB_CORE1 Registers, Base Address=7830 0000h, Length=98304

Offset	Length	Register Name	R5SS0 Physical Address	R5SS1 Physical Address
0h	32	TCMB_CORE1_START	7830 0000h	7870 0000h
17FFCh	32	TCMB_CORE1_END	7831 7FFCh	7871 7FFCh

4.1.2 R5SS Registers

R5SS Registers

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4.1.2.1 TCMA_CORE0_ROM_START Register

4.1.2.1.1 TCMA_CORE0_ROM_START Register (Offset = 0h) [reset = 0h]

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Table 4-26. Instance Table

Instance Name	Physical Address
R5SS0	0000 0000h

Figure 4-1. TCMA_CORE0_ROM_START Name Register

31	30	29	28	27	26	25	24
ROM_START							
R							
0h							
23	22	21	20	19	18	17	16
ROM_START							
R							
0h							
15	14	13	12	11	10	9	8
ROM_START							
R							
0h							
7	6	5	4	3	2	1	0
ROM_START							
R							
0h							

Table 4-27. TCMA_CORE0_ROM_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_START	R	0h	ROM start address of master sub system tcma

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4.1.2.2 TCMA_CORE0_ROM_END Register

4.1.2.2.1 TCMA_CORE0_ROM_END Register (Offset = 1FFFCh) [reset = 0h]

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Table 4-28. Instance Table

Instance Name	Physical Address
R5SS0	0001 FFFCh

Figure 4-2. TCMA_CORE0_ROM_END Name Register

31	30	29	28	27	26	25	24
ROM_END							
R							
0h							
23	22	21	20	19	18	17	16
ROM_END							
R							
0h							
15	14	13	12	11	10	9	8
ROM_END							
R							
0h							
7	6	5	4	3	2	1	0
ROM_END							
R							
0h							

Table 4-29. TCMA_CORE0_ROM_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ROM_END	R	0h	ROM end address of master sub system tcma

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4.1.2.3 TCMA_CORE0_RAM_START Register

4.1.2.3.1 TCMA_CORE0_RAM_START Register (Offset = 0h) [reset = 0h]

Return to Summary Table

Table 4-30. Instance Table

Instance Name	Physical Address
R5SS0	0002 0000h
R5SS1	0002 0000h

Figure 4-3. TCMA_CORE0_RAM_START Name Register

31	30	29	28	27	26	25	24
RAM_START							
R/W							
0h							
23	22	21	20	19	18	17	16
RAM_START							
R/W							
0h							
15	14	13	12	11	10	9	8
RAM_START							
R/W							
0h							
7	6	5	4	3	2	1	0
RAM_START							
R/W							
0h							

Table 4-31. TCMA_CORE0_RAM_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAM_START	R/W	0h	RAM start address of master sub system tcma

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4.1.2.4 TCMA_CORE0_RAM_END Register

4.1.2.4.1 TCMA_CORE0_RAM_END Register (Offset = 7FFCh) [reset = 0h]

Return to Summary Table

Table 4-32. Instance Table

Instance Name	Physical Address
R5SS0	0002 7FFCh
R5SS1	0002 7FFCh

Figure 4-4. TCMA_CORE0_RAM_END Name Register

31	30	29	28	27	26	25	24
RAM_END							
R/W							
0h							
23	22	21	20	19	18	17	16
RAM_END							
R/W							
0h							
15	14	13	12	11	10	9	8
RAM_END							
R/W							
0h							
7	6	5	4	3	2	1	0
RAM_END							
R/W							
0h							

Table 4-33. TCMA_CORE0_RAM_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAM_END	R/W	0h	RAM end address of master sub system tcma

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4.1.2.5 TCMA_CORE1_RAM_START Register

4.1.2.5.1 TCMA_CORE1_RAM_START Register (Offset = 0h) [reset = 0h]

Return to Summary Table

Table 4-34. Instance Table

Instance Name	Physical Address
R5SS0	0002 0000h
R5SS1	0002 0000h

Figure 4-5. TCMA_CORE1_RAM_START Name Register

31	30	29	28	27	26	25	24
RAM_START							
R/W							
0h							
23	22	21	20	19	18	17	16
RAM_START							
R/W							
0h							
15	14	13	12	11	10	9	8
RAM_START							
R/W							
0h							
7	6	5	4	3	2	1	0
RAM_START							
R/W							
0h							

Table 4-35. TCMA_CORE1_RAM_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAM_START	R/W	0h	RAM start address of master sub system tcma

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4.1.2.6 TCMA_CORE1_RAM_END Register

4.1.2.6.1 TCMA_CORE1_RAM_END Register (Offset = 7FFCh) [reset = 0h]

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Table 4-36. Instance Table

Instance Name	Physical Address
R5SS0	0002 7FFCh
R5SS1	0002 7FFCh

Figure 4-6. TCMA_CORE1_RAM_END Name Register

31	30	29	28	27	26	25	24
RAM_END							
R/W							
0h							
23	22	21	20	19	18	17	16
RAM_END							
R/W							
0h							
15	14	13	12	11	10	9	8
RAM_END							
R/W							
0h							
7	6	5	4	3	2	1	0
RAM_END							
R/W							
0h							

Table 4-37. TCMA_CORE1_RAM_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAM_END	R/W	0h	RAM end address of master sub system tcma

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4.1.2.7 TMU_0_REVISION Register

4.1.2.7.1 TMU_0_REVISION Register (Offset = 0h) [reset = 40000000h]

IP revision id register.

Return to Summary Table

Table 4-38. Instance Table

Instance Name	Physical Address
R5SS0	0006 0000h
R5SS1	0006 0000h

Figure 4-7. TMU_0_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED_1		FUNC			
R		R		R			
1h		0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 4-39. TMU_0_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	This identifies the scheme revision ID register type implemented for this module
29:28	RESERVED_1	R	0h	Reserved
27:16	FUNC	R	0h	Functional Release Number Reflects software-compatability. If there is no software compatability, a unique func number is assigned; for compatible modules, the same number is maintained.
15:11	RTL	R	0h	Design Release Number Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented.
10:8	MAJOR	R	0h	Major Revision Number Represents major changes to the module [e.g. entirely new features are added/changed]. The major revision number for this module.
7:6	CUSTOM	R	0h	Custom Module Number Indicates a special version of the module. May not be supported by standard software.
5:0	MINOR	R	0h	Minor Revision Number Represents minor changes to the module [e.g. enhancements to existing features]. The minor revision number for this module.

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4.1.2.8 TMU_0_SINPUF32_R0 Register

4.1.2.8.1 TMU_0_SINPUF32_R0 Register (Offset = 40h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R0.

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Table 4-40. Instance Table

Instance Name	Physical Address
R5SS0	0006 0040h
R5SS1	0006 0040h

Figure 4-8. TMU_0_SINPUF32_R0 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R0							
R/W							
0h							

Table 4-41. TMU_0_SINPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R0	R/W	0h	

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4.1.2.9 TMU_0_SINPUF32_R1 Register

4.1.2.9.1 TMU_0_SINPUF32_R1 Register (Offset = 48h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-42. Instance Table

Instance Name	Physical Address
R5SS0	0006 0048h
R5SS1	0006 0048h

Figure 4-9. TMU_0_SINPUF32_R1 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R1							
R/W							
0h							

Table 4-43. TMU_0_SINPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R1

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4.1.2.10 TMU_0_SINPUF32_R2 Register

4.1.2.10.1 TMU_0_SINPUF32_R2 Register (Offset = 50h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-44. Instance Table

Instance Name	Physical Address
R5SS0	0006 0050h
R5SS1	0006 0050h

Figure 4-10. TMU_0_SINPUF32_R2 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R2							
R/W							
0h							

Table 4-45. TMU_0_SINPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R2

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4.1.2.11 TMU_0_SINPUF32_R3 Register

4.1.2.11.1 TMU_0_SINPUF32_R3 Register (Offset = 58h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R3.

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Table 4-46. Instance Table

Instance Name	Physical Address
R5SS0	0006 0058h
R5SS1	0006 0058h

Figure 4-11. TMU_0_SINPUF32_R3 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R3							
R/W							
0h							

Table 4-47. TMU_0_SINPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R3

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4.1.2.12 TMU_0_SINPUF32_R4 Register

4.1.2.12.1 TMU_0_SINPUF32_R4 Register (Offset = 60h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R4.

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Table 4-48. Instance Table

Instance Name	Physical Address
R5SS0	0006 0060h
R5SS1	0006 0060h

Figure 4-12. TMU_0_SINPUF32_R4 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R4							
R/W							
0h							

Table 4-49. TMU_0_SINPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R4

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4.1.2.13 TMU_0_SINPUF32_R5 Register

4.1.2.13.1 TMU_0_SINPUF32_R5 Register (Offset = 68h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R5.

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Table 4-50. Instance Table

Instance Name	Physical Address
R5SS0	0006 0068h
R5SS1	0006 0068h

Figure 4-13. TMU_0_SINPUF32_R5 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R5							
R/W							
0h							

Table 4-51. TMU_0_SINPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R5

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4.1.2.14 TMU_0_SINPUF32_R6 Register

4.1.2.14.1 TMU_0_SINPUF32_R6 Register (Offset = 70h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R6.

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Table 4-52. Instance Table

Instance Name	Physical Address
R5SS0	0006 0070h
R5SS1	0006 0070h

Figure 4-14. TMU_0_SINPUF32_R6 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R6							
R/W							
0h							

Table 4-53. TMU_0_SINPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R6

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4.1.2.15 TMU_0_SINPUF32_R7 Register

4.1.2.15.1 TMU_0_SINPUF32_R7 Register (Offset = 78h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-54. Instance Table

Instance Name	Physical Address
R5SS0	0006 0078h
R5SS1	0006 0078h

Figure 4-15. TMU_0_SINPUF32_R7 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R7							
R/W							
0h							

Table 4-55. TMU_0_SINPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R7

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4.1.2.16 TMU_0_COSPUF32_R0 Register

4.1.2.16.1 TMU_0_COSPUF32_R0 Register (Offset = 80h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-56. Instance Table

Instance Name	Physical Address
R5SS0	0006 0080h
R5SS1	0006 0080h

Figure 4-16. TMU_0_COSPUF32_R0 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R0							
R/W							
0h							

Table 4-57. TMU_0_COSPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R0

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4.1.2.17 TMU_0_COSPUF32_R1 Register

4.1.2.17.1 TMU_0_COSPUF32_R1 Register (Offset = 88h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-58. Instance Table

Instance Name	Physical Address
R5SS0	0006 0088h
R5SS1	0006 0088h

Figure 4-17. TMU_0_COSPUF32_R1 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R1							
R/W							
0h							

Table 4-59. TMU_0_COSPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R1

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4.1.2.18 TMU_0_COSPUF32_R2 Register

4.1.2.18.1 TMU_0_COSPUF32_R2 Register (Offset = 90h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-60. Instance Table

Instance Name	Physical Address
R5SS0	0006 0090h
R5SS1	0006 0090h

Figure 4-18. TMU_0_COSPUF32_R2 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R2							
R/W							
0h							

Table 4-61. TMU_0_COSPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R2

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4.1.2.19 TMU_0_COSPUF32_R3 Register

4.1.2.19.1 TMU_0_COSPUF32_R3 Register (Offset = 98h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-62. Instance Table

Instance Name	Physical Address
R5SS0	0006 0098h
R5SS1	0006 0098h

Figure 4-19. TMU_0_COSPUF32_R3 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R3							
R/W							
0h							

Table 4-63. TMU_0_COSPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R3

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4.1.2.20 TMU_0_COSPUF32_R4 Register

4.1.2.20.1 TMU_0_COSPUF32_R4 Register (Offset = A0h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-64. Instance Table

Instance Name	Physical Address
R5SS0	0006 00A0h
R5SS1	0006 00A0h

Figure 4-20. TMU_0_COSPUF32_R4 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R4							
R/W							
0h							

Table 4-65. TMU_0_COSPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R4

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4.1.2.21 TMU_0_COSPUF32_R5 Register

4.1.2.21.1 TMU_0_COSPUF32_R5 Register (Offset = A8h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R5.

Return to Summary Table

Table 4-66. Instance Table

Instance Name	Physical Address
R5SS0	0006 00A8h
R5SS1	0006 00A8h

Figure 4-21. TMU_0_COSPUF32_R5 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R5							
R/W							
0h							

Table 4-67. TMU_0_COSPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R5

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4.1.2.22 TMU_0_COSPUF32_R6 Register

4.1.2.22.1 TMU_0_COSPUF32_R6 Register (Offset = B0h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-68. Instance Table

Instance Name	Physical Address
R5SS0	0006 00B0h
R5SS1	0006 00B0h

Figure 4-22. TMU_0_COSPUF32_R6 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R6							
R/W							
0h							

Table 4-69. TMU_0_COSPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R6

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4.1.2.23 TMU_0_COSPUF32_R7 Register

4.1.2.23.1 TMU_0_COSPUF32_R7 Register (Offset = B8h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-70. Instance Table

Instance Name	Physical Address
R5SS0	0006 00B8h
R5SS1	0006 00B8h

Figure 4-23. TMU_0_COSPUF32_R7 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R7							
R/W							
0h							

Table 4-71. TMU_0_COSPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R7

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4.1.2.24 TMU_0_ATANPUF32_R0 Register

4.1.2.24.1 TMU_0_ATANPUF32_R0 Register (Offset = C0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R0.

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Table 4-72. Instance Table

Instance Name	Physical Address
R5SS0	0006 00C0h
R5SS1	0006 00C0h

Figure 4-24. TMU_0_ATANPUF32_R0 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R0							
R/W							
0h							

Table 4-73. TMU_0_ATANPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R0

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4.1.2.25 TMU_0_ATANPUF32_R1 Register

4.1.2.25.1 TMU_0_ATANPUF32_R1 Register (Offset = C8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-74. Instance Table

Instance Name	Physical Address
R5SS0	0006 00C8h
R5SS1	0006 00C8h

Figure 4-25. TMU_0_ATANPUF32_R1 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R1							
R/W							
0h							

Table 4-75. TMU_0_ATANPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R1

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4.1.2.26 TMU_0_ATANPUF32_R2 Register

4.1.2.26.1 TMU_0_ATANPUF32_R2 Register (Offset = D0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R2.

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Table 4-76. Instance Table

Instance Name	Physical Address
R5SS0	0006 00D0h
R5SS1	0006 00D0h

Figure 4-26. TMU_0_ATANPUF32_R2 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R2							
R/W							
0h							

Table 4-77. TMU_0_ATANPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R2

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4.1.2.27 TMU_0_ATANPUF32_R3 Register

4.1.2.27.1 TMU_0_ATANPUF32_R3 Register (Offset = D8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-78. Instance Table

Instance Name	Physical Address
R5SS0	0006 00D8h
R5SS1	0006 00D8h

Figure 4-27. TMU_0_ATANPUF32_R3 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R3							
R/W							
0h							

Table 4-79. TMU_0_ATANPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R3

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4.1.2.28 TMU_0_ATANPUF32_R4 Register

4.1.2.28.1 TMU_0_ATANPUF32_R4 Register (Offset = E0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R4.

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Table 4-80. Instance Table

Instance Name	Physical Address
R5SS0	0006 00E0h
R5SS1	0006 00E0h

Figure 4-28. TMU_0_ATANPUF32_R4 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R4							
R/W							
0h							

Table 4-81. TMU_0_ATANPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R4

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4.1.2.29 TMU_0_ATANPUF32_R5 Register

4.1.2.29.1 TMU_0_ATANPUF32_R5 Register (Offset = E8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R5.

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Table 4-82. Instance Table

Instance Name	Physical Address
R5SS0	0006 00E8h
R5SS1	0006 00E8h

Figure 4-29. TMU_0_ATANPUF32_R5 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R5							
R/W							
0h							

Table 4-83. TMU_0_ATANPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R5

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4.1.2.30 TMU_0_ATANPUF32_R6 Register

4.1.2.30.1 TMU_0_ATANPUF32_R6 Register (Offset = F0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R6.

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Table 4-84. Instance Table

Instance Name	Physical Address
R5SS0	0006 00F0h
R5SS1	0006 00F0h

Figure 4-30. TMU_0_ATANPUF32_R6 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R6							
R/W							
0h							

Table 4-85. TMU_0_ATANPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R6

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4.1.2.31 TMU_0_ATANPUF32_R7 Register

4.1.2.31.1 TMU_0_ATANPUF32_R7 Register (Offset = F8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-86. Instance Table

Instance Name	Physical Address
R5SS0	0006 00F8h
R5SS1	0006 00F8h

Figure 4-31. TMU_0_ATANPUF32_R7 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R7							
R/W							
0h							

Table 4-87. TMU_0_ATANPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R7

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4.1.2.32 TMU_0_IEXP2F32_R0 Register

4.1.2.32.1 TMU_0_IEXP2F32_R0 Register (Offset = 140h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-88. Instance Table

Instance Name	Physical Address
R5SS0	0006 0140h
R5SS1	0006 0140h

Figure 4-32. TMU_0_IEXP2F32_R0 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R0							
R/W							
0h							

Table 4-89. TMU_0_IEXP2F32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R0

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4.1.2.33 TMU_0_IEXP2F32_R1 Register

4.1.2.33.1 TMU_0_IEXP2F32_R1 Register (Offset = 148h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R1.

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Table 4-90. Instance Table

Instance Name	Physical Address
R5SS0	0006 0148h
R5SS1	0006 0148h

Figure 4-33. TMU_0_IEXP2F32_R1 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R1							
R/W							
0h							

Table 4-91. TMU_0_IEXP2F32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R1

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4.1.2.34 TMU_0_IEXP2F32_R2 Register

4.1.2.34.1 TMU_0_IEXP2F32_R2 Register (Offset = 150h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-92. Instance Table

Instance Name	Physical Address
R5SS0	0006 0150h
R5SS1	0006 0150h

Figure 4-34. TMU_0_IEXP2F32_R2 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R2							
R/W							
0h							

Table 4-93. TMU_0_IEXP2F32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R2

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4.1.2.35 TMU_0_IEXP2F32_R3 Register

4.1.2.35.1 TMU_0_IEXP2F32_R3 Register (Offset = 158h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-94. Instance Table

Instance Name	Physical Address
R5SS0	0006 0158h
R5SS1	0006 0158h

Figure 4-35. TMU_0_IEXP2F32_R3 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R3							
R/W							
0h							

Table 4-95. TMU_0_IEXP2F32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R3

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4.1.2.36 TMU_0_IEXP2F32_R4 Register

4.1.2.36.1 TMU_0_IEXP2F32_R4 Register (Offset = 160h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-96. Instance Table

Instance Name	Physical Address
R5SS0	0006 0160h
R5SS1	0006 0160h

Figure 4-36. TMU_0_IEXP2F32_R4 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R4							
R/W							
0h							

Table 4-97. TMU_0_IEXP2F32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R4

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4.1.2.37 TMU_0_IEXP2F32_R5 Register

4.1.2.37.1 TMU_0_IEXP2F32_R5 Register (Offset = 168h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R5.

Return to Summary Table

Table 4-98. Instance Table

Instance Name	Physical Address
R5SS0	0006 0168h
R5SS1	0006 0168h

Figure 4-37. TMU_0_IEXP2F32_R5 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R5							
R/W							
0h							

Table 4-99. TMU_0_IEXP2F32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R5

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4.1.2.38 TMU_0_IEXP2F32_R6 Register

4.1.2.38.1 TMU_0_IEXP2F32_R6 Register (Offset = 170h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-100. Instance Table

Instance Name	Physical Address
R5SS0	0006 0170h
R5SS1	0006 0170h

Figure 4-38. TMU_0_IEXP2F32_R6 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R6							
R/W							
0h							

Table 4-101. TMU_0_IEXP2F32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R6

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4.1.2.39 TMU_0_IEXP2F32_R7 Register

4.1.2.39.1 TMU_0_IEXP2F32_R7 Register (Offset = 178h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R7.

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Table 4-102. Instance Table

Instance Name	Physical Address
R5SS0	0006 0178h
R5SS1	0006 0178h

Figure 4-39. TMU_0_IEXP2F32_R7 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R7							
R/W							
0h							

Table 4-103. TMU_0_IEXP2F32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R7

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4.1.2.40 TMU_0_LOG2F32_R0 Register

4.1.2.40.1 TMU_0_LOG2F32_R0 Register (Offset = 180h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R0.

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Table 4-104. Instance Table

Instance Name	Physical Address
R5SS0	0006 0180h
R5SS1	0006 0180h

Figure 4-40. TMU_0_LOG2F32_R0 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R0							
R/W							
0h							

Table 4-105. TMU_0_LOG2F32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R0

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4.1.2.41 TMU_0_LOG2F32_R1 Register

4.1.2.41.1 TMU_0_LOG2F32_R1 Register (Offset = 188h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R1.

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Table 4-106. Instance Table

Instance Name	Physical Address
R5SS0	0006 0188h
R5SS1	0006 0188h

Figure 4-41. TMU_0_LOG2F32_R1 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R1							
R/W							
0h							

Table 4-107. TMU_0_LOG2F32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R1

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4.1.2.42 TMU_0_LOG2F32_R2 Register

4.1.2.42.1 TMU_0_LOG2F32_R2 Register (Offset = 190h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R2.

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Table 4-108. Instance Table

Instance Name	Physical Address
R5SS0	0006 0190h
R5SS1	0006 0190h

Figure 4-42. TMU_0_LOG2F32_R2 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R2							
R/W							
0h							

Table 4-109. TMU_0_LOG2F32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R2

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4.1.2.43 TMU_0_LOG2F32_R3 Register

4.1.2.43.1 TMU_0_LOG2F32_R3 Register (Offset = 198h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R3.

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Table 4-110. Instance Table

Instance Name	Physical Address
R5SS0	0006 0198h
R5SS1	0006 0198h

Figure 4-43. TMU_0_LOG2F32_R3 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R3							
R/W							
0h							

Table 4-111. TMU_0_LOG2F32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R3

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4.1.2.44 TMU_0_LOG2F32_R4 Register

4.1.2.44.1 TMU_0_LOG2F32_R4 Register (Offset = 1A0h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R4.

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Table 4-112. Instance Table

Instance Name	Physical Address
R5SS0	0006 01A0h
R5SS1	0006 01A0h

Figure 4-44. TMU_0_LOG2F32_R4 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R4							
R/W							
0h							

Table 4-113. TMU_0_LOG2F32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R4

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4.1.2.45 TMU_0_LOG2F32_R5 Register

4.1.2.45.1 TMU_0_LOG2F32_R5 Register (Offset = 1A8h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R5.

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Table 4-114. Instance Table

Instance Name	Physical Address
R5SS0	0006 01A8h
R5SS1	0006 01A8h

Figure 4-45. TMU_0_LOG2F32_R5 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R5							
R/W							
0h							

Table 4-115. TMU_0_LOG2F32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R5

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4.1.2.46 TMU_0_LOG2F32_R6 Register

4.1.2.46.1 TMU_0_LOG2F32_R6 Register (Offset = 1B0h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R6.

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Table 4-116. Instance Table

Instance Name	Physical Address
R5SS0	0006 01B0h
R5SS1	0006 01B0h

Figure 4-46. TMU_0_LOG2F32_R6 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R6							
R/W							
0h							

Table 4-117. TMU_0_LOG2F32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R6

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4.1.2.47 TMU_0_LOG2F32_R7 Register

4.1.2.47.1 TMU_0_LOG2F32_R7 Register (Offset = 1B8h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R7.

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Table 4-118. Instance Table

Instance Name	Physical Address
R5SS0	0006 01B8h
R5SS1	0006 01B8h

Figure 4-47. TMU_0_LOG2F32_R7 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R7							
R/W							
0h							

Table 4-119. TMU_0_LOG2F32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R7

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4.1.2.48 TMU_0_QUADF32_X_R0_R1 Register

4.1.2.48.1 TMU_0_QUADF32_X_R0_R1 Register (Offset = 1C0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R0 and R1.

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Table 4-120. Instance Table

Instance Name	Physical Address
R5SS0	0006 01C0h
R5SS1	0006 01C0h

Figure 4-48. TMU_0_QUADF32_X_R0_R1 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R0_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R0_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R0_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R0_R1							
R/W							
0h							

Table 4-121. TMU_0_QUADF32_X_R0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R0_R1	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R0 and R1

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4.1.2.49 TMU_0_QUADF32_X_R1_R2 Register

4.1.2.49.1 TMU_0_QUADF32_X_R1_R2 Register (Offset = 1C8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R1 and R2.

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Table 4-122. Instance Table

Instance Name	Physical Address
R5SS0	0006 01C8h
R5SS1	0006 01C8h

Figure 4-49. TMU_0_QUADF32_X_R1_R2 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R1_R2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
QUADF32_X_R1_R2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
QUADF32_X_R1_R2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QUADF32_X_R1_R2							
R/W							
0h							

Table 4-123. TMU_0_QUADF32_X_R1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R1_R2	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R1 and R2

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4.1.2.50 TMU_0_QUADF32_X_R2_R3 Register

4.1.2.50.1 TMU_0_QUADF32_X_R2_R3 Register (Offset = 1D0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R2 and R3.

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Table 4-124. Instance Table

Instance Name	Physical Address
R5SS0	0006 01D0h
R5SS1	0006 01D0h

Figure 4-50. TMU_0_QUADF32_X_R2_R3 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R2_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R2_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R2_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R2_R3							
R/W							
0h							

Table 4-125. TMU_0_QUADF32_X_R2_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R2_R3	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R2 and R3

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4.1.2.51 TMU_0_QUADF32_X_R3_R4 Register

4.1.2.51.1 TMU_0_QUADF32_X_R3_R4 Register (Offset = 1D8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R3 and R4.

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Table 4-126. Instance Table

Instance Name	Physical Address
R5SS0	0006 01D8h
R5SS1	0006 01D8h

Figure 4-51. TMU_0_QUADF32_X_R3_R4 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R3_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R3_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R3_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R3_R4							
R/W							
0h							

Table 4-127. TMU_0_QUADF32_X_R3_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R3_R4	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R3 and R4

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4.1.2.52 TMU_0_QUADF32_X_R4_R5 Register

4.1.2.52.1 TMU_0_QUADF32_X_R4_R5 Register (Offset = 1E0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R4 and R5.

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Table 4-128. Instance Table

Instance Name	Physical Address
R5SS0	0006 01E0h
R5SS1	0006 01E0h

Figure 4-52. TMU_0_QUADF32_X_R4_R5 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R4_R5							
R/W							
0h							

Table 4-129. TMU_0_QUADF32_X_R4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R4_R5	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R4 and R5

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4.1.2.53 TMU_0_QUADF32_X_R5SS0_R6 Register

4.1.2.53.1 TMU_0_QUADF32_X_R5SS0_R6 Register (Offset = 1E8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R5 and R6.

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Table 4-130. Instance Table

Instance Name	Physical Address
R5SS0	0006 01E8h
R5SS1	0006 01E8h

Figure 4-53. TMU_0_QUADF32_X_R5SS0_R6 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R5_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R5_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R5_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R5_R6							
R/W							
0h							

Table 4-131. TMU_0_QUADF32_X_R5SS0_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R5_R6	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R5 and R6

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4.1.2.54 TMU_0_QUADF32_X_R6_R7 Register

4.1.2.54.1 TMU_0_QUADF32_X_R6_R7 Register (Offset = 1F0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R6 and R7.

Return to Summary Table

Table 4-132. Instance Table

Instance Name	Physical Address
R5SS0	0006 01F0h
R5SS1	0006 01F0h

Figure 4-54. TMU_0_QUADF32_X_R6_R7 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R6_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R6_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R6_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R6_R7							
R/W							
0h							

Table 4-133. TMU_0_QUADF32_X_R6_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R6_R7	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R6 and R7

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4.1.2.55 TMU_0_RESULT_R0 Register

4.1.2.55.1 TMU_0_RESULT_R0 Register (Offset = 280h) [reset = 0h]

R0 result register.

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Table 4-134. Instance Table

Instance Name	Physical Address
R5SS0	0006 0280h
R5SS1	0006 0280h

Figure 4-55. TMU_0_RESULT_R0 Name Register

31	30	29	28	27	26	25	24
R0							
R							
0h							
23	22	21	20	19	18	17	16
R0							
R							
0h							
15	14	13	12	11	10	9	8
R0							
R							
0h							
7	6	5	4	3	2	1	0
R0							
R							
0h							

Table 4-135. TMU_0_RESULT_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R0	R	0h	R0 result register

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4.1.2.56 TMU_0_RESULT_R1 Register

4.1.2.56.1 TMU_0_RESULT_R1 Register (Offset = 288h) [reset = 0h]

R1 result register.

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Table 4-136. Instance Table

Instance Name	Physical Address
R5SS0	0006 0288h
R5SS1	0006 0288h

Figure 4-56. TMU_0_RESULT_R1 Name Register

31	30	29	28	27	26	25	24
R1							
R							
0h							
23	22	21	20	19	18	17	16
R1							
R							
0h							
15	14	13	12	11	10	9	8
R1							
R							
0h							
7	6	5	4	3	2	1	0
R1							
R							
0h							

Table 4-137. TMU_0_RESULT_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R1	R	0h	R1 result register

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4.1.2.57 TMU_0_RESULT_R2 Register

4.1.2.57.1 TMU_0_RESULT_R2 Register (Offset = 290h) [reset = 0h]

R2 result register.

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Table 4-138. Instance Table

Instance Name	Physical Address
R5SS0	0006 0290h
R5SS1	0006 0290h

Figure 4-57. TMU_0_RESULT_R2 Name Register

31	30	29	28	27	26	25	24
R2							
R							
0h							
23	22	21	20	19	18	17	16
R2							
R							
0h							
15	14	13	12	11	10	9	8
R2							
R							
0h							
7	6	5	4	3	2	1	0
R2							
R							
0h							

Table 4-139. TMU_0_RESULT_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R2	R	0h	R2 result register

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4.1.2.58 TMU_0_RESULT_R3 Register

4.1.2.58.1 TMU_0_RESULT_R3 Register (Offset = 298h) [reset = 0h]

R3 result register.

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Table 4-140. Instance Table

Instance Name	Physical Address
R5SS0	0006 0298h
R5SS1	0006 0298h

Figure 4-58. TMU_0_RESULT_R3 Name Register

31	30	29	28	27	26	25	24
R3							
R							
0h							
23	22	21	20	19	18	17	16
R3							
R							
0h							
15	14	13	12	11	10	9	8
R3							
R							
0h							
7	6	5	4	3	2	1	0
R3							
R							
0h							

Table 4-141. TMU_0_RESULT_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R3	R	0h	R3 result register

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4.1.2.59 TMU_0_RESULT_R4 Register

4.1.2.59.1 TMU_0_RESULT_R4 Register (Offset = 2A0h) [reset = 0h]

R4 result register.

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Table 4-142. Instance Table

Instance Name	Physical Address
R5SS0	0006 02A0h
R5SS1	0006 02A0h

Figure 4-59. TMU_0_RESULT_R4 Name Register

31	30	29	28	27	26	25	24
R4							
R							
0h							
23	22	21	20	19	18	17	16
R4							
R							
0h							
15	14	13	12	11	10	9	8
R4							
R							
0h							
7	6	5	4	3	2	1	0
R4							
R							
0h							

Table 4-143. TMU_0_RESULT_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R4	R	0h	R4 result register

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4.1.2.60 TMU_0_RESULT_R5 Register

4.1.2.60.1 TMU_0_RESULT_R5 Register (Offset = 2A8h) [reset = 0h]

R5 result register.

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Table 4-144. Instance Table

Instance Name	Physical Address
R5SS0	0006 02A8h
R5SS1	0006 02A8h

Figure 4-60. TMU_0_RESULT_R5 Name Register

31	30	29	28	27	26	25	24
R5							
R							
0h							
23	22	21	20	19	18	17	16
R5							
R							
0h							
15	14	13	12	11	10	9	8
R5							
R							
0h							
7	6	5	4	3	2	1	0
R5							
R							
0h							

Table 4-145. TMU_0_RESULT_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5	R	0h	R5 result register

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4.1.2.61 TMU_0_RESULT_R6 Register

4.1.2.61.1 TMU_0_RESULT_R6 Register (Offset = 2B0h) [reset = 0h]

R6 result register.

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Table 4-146. Instance Table

Instance Name	Physical Address
R5SS0	0006 02B0h
R5SS1	0006 02B0h

Figure 4-61. TMU_0_RESULT_R6 Name Register

31	30	29	28	27	26	25	24
R6							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R6							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R6							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R6							
R							
0h							

Table 4-147. TMU_0_RESULT_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R6	R	0h	R6 result register

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4.1.2.62 TMU_0_RESULT_R7 Register

4.1.2.62.1 TMU_0_RESULT_R7 Register (Offset = 2B8h) [reset = 0h]

R7 result register.

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Table 4-148. Instance Table

Instance Name	Physical Address
R5SS0	0006 02B8h
R5SS1	0006 02B8h

Figure 4-62. TMU_0_RESULT_R7 Name Register

31	30	29	28	27	26	25	24
R7							
R							
0h							
23	22	21	20	19	18	17	16
R7							
R							
0h							
15	14	13	12	11	10	9	8
R7							
R							
0h							
7	6	5	4	3	2	1	0
R7							
R							
0h							

Table 4-149. TMU_0_RESULT_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R7	R	0h	R7 result register

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4.1.2.63 TMU_0_CSAVE_R0 Register

4.1.2.63.1 TMU_0_CSAVE_R0 Register (Offset = 2C0h) [reset = 0h]

Context save of R0 result register.

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Table 4-150. Instance Table

Instance Name	Physical Address
R5SS0	0006 02C0h
R5SS1	0006 02C0h

Figure 4-63. TMU_0_CSAVE_R0 Name Register

31	30	29	28	27	26	25	24
CSAVE_R0							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R0							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R0							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R0							
R							
0h							

Table 4-151. TMU_0_CSAVE_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R0	R	0h	Context save of R0 result register

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4.1.2.64 TMU_0_CSAVE_R1 Register

4.1.2.64.1 TMU_0_CSAVE_R1 Register (Offset = 2C8h) [reset = 0h]

Context save of R1 result register.

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Table 4-152. Instance Table

Instance Name	Physical Address
R5SS0	0006 02C8h
R5SS1	0006 02C8h

Figure 4-64. TMU_0_CSAVE_R1 Name Register

31	30	29	28	27	26	25	24
CSAVE_R1							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R1							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R1							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R1							
R							
0h							

Table 4-153. TMU_0_CSAVE_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R1	R	0h	Context save of R1 result register

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4.1.2.65 TMU_0_CSAVE_R2 Register

4.1.2.65.1 TMU_0_CSAVE_R2 Register (Offset = 2D0h) [reset = 0h]

Context save of R2 result register.

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Table 4-154. Instance Table

Instance Name	Physical Address
R5SS0	0006 02D0h
R5SS1	0006 02D0h

Figure 4-65. TMU_0_CSAVE_R2 Name Register

31	30	29	28	27	26	25	24
CSAVE_R2							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R2							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R2							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R2							
R							
0h							

Table 4-155. TMU_0_CSAVE_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R2	R	0h	Context save of R2 result register

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4.1.2.66 TMU_0_CSAVE_R3 Register

4.1.2.66.1 TMU_0_CSAVE_R3 Register (Offset = 2D8h) [reset = 0h]

Context save of R3 result register.

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Table 4-156. Instance Table

Instance Name	Physical Address
R5SS0	0006 02D8h
R5SS1	0006 02D8h

Figure 4-66. TMU_0_CSAVE_R3 Name Register

31	30	29	28	27	26	25	24
CSAVE_R3							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R3							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R3							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R3							
R							
0h							

Table 4-157. TMU_0_CSAVE_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R3	R	0h	Context save of R3 result register

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4.1.2.67 TMU_0_CSAVE_R4 Register

4.1.2.67.1 TMU_0_CSAVE_R4 Register (Offset = 2E0h) [reset = 0h]

Context save of R4 result register.

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Table 4-158. Instance Table

Instance Name	Physical Address
R5SS0	0006 02E0h
R5SS1	0006 02E0h

Figure 4-67. TMU_0_CSAVE_R4 Name Register

31	30	29	28	27	26	25	24
CSAVE_R4							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R4							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R4							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R4							
R							
0h							

Table 4-159. TMU_0_CSAVE_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R4	R	0h	Context save of R4 result register

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4.1.2.68 TMU_0_CSAVE_R5 Register

4.1.2.68.1 TMU_0_CSAVE_R5 Register (Offset = 2E8h) [reset = 0h]

Context save of R5 result register.

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Table 4-160. Instance Table

Instance Name	Physical Address
R5SS0	0006 02E8h
R5SS1	0006 02E8h

Figure 4-68. TMU_0_CSAVE_R5 Name Register

31	30	29	28	27	26	25	24
CSAVE_R5							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R5							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R5							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R5							
R							
0h							

Table 4-161. TMU_0_CSAVE_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R5	R	0h	Context save of R5 result register

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4.1.2.69 TMU_0_CSAVE_R6 Register

4.1.2.69.1 TMU_0_CSAVE_R6 Register (Offset = 2F0h) [reset = 0h]

Context save of R6 result register.

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Table 4-162. Instance Table

Instance Name	Physical Address
R5SS0	0006 02F0h
R5SS1	0006 02F0h

Figure 4-69. TMU_0_CSAVE_R6 Name Register

31	30	29	28	27	26	25	24
CSAVE_R6							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R6							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R6							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R6							
R							
0h							

Table 4-163. TMU_0_CSAVE_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R6	R	0h	Context save of R6 result register

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4.1.2.70 TMU_0_CSAVE_R7 Register

4.1.2.70.1 TMU_0_CSAVE_R7 Register (Offset = 2F8h) [reset = 0h]

Context save of R7 result register.

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Table 4-164. Instance Table

Instance Name	Physical Address
R5SS0	0006 02F8h
R5SS1	0006 02F8h

Figure 4-70. TMU_0_CSAVE_R7 Name Register

31	30	29	28	27	26	25	24
CSAVE_R7							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R7							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R7							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R7							
R							
0h							

Table 4-165. TMU_0_CSAVE_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R7	R	0h	Context save of R7 result register

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4.1.2.71 TMU_0_CSAVE_OP2 Register

4.1.2.71.1 TMU_0_CSAVE_OP2 Register (Offset = 300h) [reset = 0h]

Context save of Operarand2 result register.

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Table 4-166. Instance Table

Instance Name	Physical Address
R5SS0	0006 0300h
R5SS1	0006 0300h

Figure 4-71. TMU_0_CSAVE_OP2 Name Register

31	30	29	28	27	26	25	24
CSAVE_OP2							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_OP2							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_OP2							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_OP2							
R							
0h							

Table 4-167. TMU_0_CSAVE_OP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_OP2	R	0h	Context save of operand 2 [OP2] result register

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4.1.2.72 TMU_0_CONTEXT_SAVE Register

4.1.2.72.1 TMU_0_CONTEXT_SAVE Register (Offset = 308h) [reset = 0h]

Register to initiate context save of result registers.

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Table 4-168. Instance Table

Instance Name	Physical Address
R5SS0	0006 0308h
R5SS1	0006 0308h

Figure 4-72. TMU_0_CONTEXT_SAVE Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							SAVE
R							R/W1TS
0h							0h

Table 4-169. TMU_0_CONTEXT_SAVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	SAVE	R/W1TS	0h	Writing one will initiate context save. Context save will be done only after completion all operations initiated by master before context save was issued. Results registers R0 to R3 and Operand2 will be saved. Note: Contex is saved within IP, not to external memory.

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4.1.2.73 TMU_0_CONTEXT_RESTORE Register

4.1.2.73.1 TMU_0_CONTEXT_RESTORE Register (Offset = 310h) [reset = 0h]

Register to initiate context restore of result registers.

Return to Summary Table

Table 4-170. Instance Table

Instance Name	Physical Address
R5SS0	0006 0310h
R5SS1	0006 0310h

Figure 4-73. TMU_0_CONTEXT_RESTORE Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							RESTORE
R							R/W1TS
0h							0h

Table 4-171. TMU_0_CONTEXT_RESTORE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	RESTORE	R/W1TS	0h	Writing one will initiate context restore. Results registers R0 to R3 and Operand2 will be restored.

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4.1.2.74 TMU_0_STF Register

4.1.2.74.1 TMU_0_STF Register (Offset = 348h) [reset = 0h]

TMU status Register.

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Table 4-172. Instance Table

Instance Name	Physical Address
R5SS0	0006 0348h
R5SS1	0006 0348h

Figure 4-74. TMU_0_STF Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2						LUF_WR_EN	LVF_WR_EN
R						R	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						LUF	LVF
R						R/W	R/W
0h						0h	0h

Table 4-173. TMU_0_STF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_2	R	0h	Reserved
9	LUF_WR_EN	R	0h	Always read as zero, Value is written to this bit either enables/ disables write to LVF [[br] 0:Disbles write to LUF 1:Enables write to LUF
8	LVF_WR_EN	R	0h	Always read as zero, Value is written to this bit either enables/ disables write to LVF [[br] 0:Disbles write to LVF 1:Enables write to LVF
7:2	RESERVED_1	R	0h	Reserved
1	LUF	R/W	0h	Is set to '1' when a TMU operation results in LVF. It is sticky bit, once set, it remains set until it is cleared with write. It can be written only when LUF_WR_EN Is written with '1'
0	LVF	R/W	0h	Is set to '1' when a TMU operation results in LVF. It is sticky bit, once set, it remains set until it is cleared with write. It can be written only when LVF_WR_EN Is written with '1'

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4.1.2.75 TMU_0_PARITY_TEST Register

4.1.2.75.1 TMU_0_PARITY_TEST Register (Offset = 380h) [reset = 0h]

Enabling the parity test feature.

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Table 4-174. Instance Table

Instance Name	Physical Address
R5SS0	0006 0380h
R5SS1	0006 0380h

Figure 4-75. TMU_0_PARITY_TEST Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				TESTEN			
R				R/W			
0h				0h			

Table 4-175. TMU_0_PARITY_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:4	RESERVED_1	R	0h	Reserved
3:0	TESTEN	R/W	0h	1010: Parity test feature is enabled All other values: Parity test feature is disabled Note: When the parity test feature is enabled, acutal registers are not accessible in the memory map. Instead, the parity values are accessible. Parity is computed for every byte and the correponding parity value is available at the bit-0 of every byte. Value of '1' written to the parity bit after enabling the parity test feature can be used to inject the error by inverting the stored parity value.

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4.1.2.76 TMU_0_LCM_LOCK Register

4.1.2.76.1 TMU_0_LCM_LOCK Register (Offset = 390h) [reset = 0h]

LCM lock configuration.

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Table 4-176. Instance Table

Instance Name	Physical Address
R5SS0	0006 0390h
R5SS1	0006 0390h

Figure 4-76. TMU_0_LCM_LOCK Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							PARITY_TEST
R							R/W
0h							0h

Table 4-177. TMU_0_LCM_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	PARITY_TEST	R/W	0h	0: Register configuration is not locked. [[br] 1:Register configuration is locked.

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4.1.2.77 TMU_0_LCM_COMMIT Register

4.1.2.77.1 TMU_0_LCM_COMMIT Register (Offset = 3A0h) [reset = 0h]

LCM commit configuration.

Return to Summary Table

Table 4-178. Instance Table

Instance Name	Physical Address
R5SS0	0006 03A0h
R5SS1	0006 03A0h

Figure 4-77. TMU_0_LCM_COMMIT Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							PARITY_TEST
R							R/W1TS
0h							0h

Table 4-179. TMU_0_LCM_COMMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	PARITY_TEST	R/W1TS	0h	0: Register lock configuration is not committed. [[br] 1:Register lock configuration is committed. Once configuration is committed, only reset can change the configuration.

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4.1.2.78 TMU_1_REVISION Register

4.1.2.78.1 TMU_1_REVISION Register (Offset = 0h) [reset = 40000000h]

IP revision id register.

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Table 4-180. Instance Table

Instance Name	Physical Address
R5SS0	0006 0000h
R5SS1	0006 0000h

Figure 4-78. TMU_1_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED_1		FUNC			
R		R		R			
1h		0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 4-181. TMU_1_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	This identifies the scheme revision ID register type implemented for this module
29:28	RESERVED_1	R	0h	Reserved
27:16	FUNC	R	0h	Functional Release Number Reflects software-compatability. If there is no software compatability, a unique func number is assigned; for compatible modules, the same number is maintained.
15:11	RTL	R	0h	Design Release Number Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented.
10:8	MAJOR	R	0h	Major Revision Number Represents major changes to the module [e.g. entirely new features are added/changed]. The major revision number for this module.
7:6	CUSTOM	R	0h	Custom Module Number Indicates a special version of the module. May not be supported by standard software.
5:0	MINOR	R	0h	Minor Revision Number Represents minor changes to the module [e.g. enhancements to existing features]. The minor revision number for this module.

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4.1.2.79 TMU_1_SINPUF32_R0 Register

4.1.2.79.1 TMU_1_SINPUF32_R0 Register (Offset = 40h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R0.

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Table 4-182. Instance Table

Instance Name	Physical Address
R5SS0	0006 0040h
R5SS1	0006 0040h

Figure 4-79. TMU_1_SINPUF32_R0 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R0							
R/W							
0h							

Table 4-183. TMU_1_SINPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R0

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4.1.2.80 TMU_1_SINPUF32_R1 Register

4.1.2.80.1 TMU_1_SINPUF32_R1 Register (Offset = 48h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R1.

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Table 4-184. Instance Table

Instance Name	Physical Address
R5SS0	0006 0048h
R5SS1	0006 0048h

Figure 4-80. TMU_1_SINPUF32_R1 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R1							
R/W							
0h							

Table 4-185. TMU_1_SINPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R1

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4.1.2.81 TMU_1_SINPUF32_R2 Register

4.1.2.81.1 TMU_1_SINPUF32_R2 Register (Offset = 50h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R2.

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Table 4-186. Instance Table

Instance Name	Physical Address
R5SS0	0006 0050h
R5SS1	0006 0050h

Figure 4-81. TMU_1_SINPUF32_R2 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R2							
R/W							
0h							

Table 4-187. TMU_1_SINPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R2

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4.1.2.82 TMU_1_SINPUF32_R3 Register

4.1.2.82.1 TMU_1_SINPUF32_R3 Register (Offset = 58h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R3.

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Table 4-188. Instance Table

Instance Name	Physical Address
R5SS0	0006 0058h
R5SS1	0006 0058h

Figure 4-82. TMU_1_SINPUF32_R3 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R3							
R/W							
0h							

Table 4-189. TMU_1_SINPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R3

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4.1.2.83 TMU_1_SINPUF32_R4 Register

4.1.2.83.1 TMU_1_SINPUF32_R4 Register (Offset = 60h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R4.

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Table 4-190. Instance Table

Instance Name	Physical Address
R5SS0	0006 0060h
R5SS1	0006 0060h

Figure 4-83. TMU_1_SINPUF32_R4 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R4							
R/W							
0h							

Table 4-191. TMU_1_SINPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R4

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4.1.2.84 TMU_1_SINPUF32_R5 Register

4.1.2.84.1 TMU_1_SINPUF32_R5 Register (Offset = 68h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R5.

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Table 4-192. Instance Table

Instance Name	Physical Address
R5SS0	0006 0068h
R5SS1	0006 0068h

Figure 4-84. TMU_1_SINPUF32_R5 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R5							
R/W							
0h							

Table 4-193. TMU_1_SINPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R5

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4.1.2.85 TMU_1_SINPUF32_R6 Register

4.1.2.85.1 TMU_1_SINPUF32_R6 Register (Offset = 70h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R6.

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Table 4-194. Instance Table

Instance Name	Physical Address
R5SS0	0006 0070h
R5SS1	0006 0070h

Figure 4-85. TMU_1_SINPUF32_R6 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R6							
R/W							
0h							

Table 4-195. TMU_1_SINPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R6

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4.1.2.86 TMU_1_SINPUF32_R7 Register

4.1.2.86.1 TMU_1_SINPUF32_R7 Register (Offset = 78h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R7.

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Table 4-196. Instance Table

Instance Name	Physical Address
R5SS0	0006 0078h
R5SS1	0006 0078h

Figure 4-86. TMU_1_SINPUF32_R7 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R7							
R/W							
0h							

Table 4-197. TMU_1_SINPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R7

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4.1.2.87 TMU_1_COSPUF32_R0 Register

4.1.2.87.1 TMU_1_COSPUF32_R0 Register (Offset = 80h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R0.

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Table 4-198. Instance Table

Instance Name	Physical Address
R5SS0	0006 0080h
R5SS1	0006 0080h

Figure 4-87. TMU_1_COSPUF32_R0 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R0							
R/W							
0h							

Table 4-199. TMU_1_COSPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R0

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4.1.2.88 TMU_1_COSPUF32_R1 Register

4.1.2.88.1 TMU_1_COSPUF32_R1 Register (Offset = 88h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R1.

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Table 4-200. Instance Table

Instance Name	Physical Address
R5SS0	0006 0088h
R5SS1	0006 0088h

Figure 4-88. TMU_1_COSPUF32_R1 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R1							
R/W							
0h							

Table 4-201. TMU_1_COSPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R1

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4.1.2.89 TMU_1_COSPUF32_R2 Register

4.1.2.89.1 TMU_1_COSPUF32_R2 Register (Offset = 90h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R2.

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Table 4-202. Instance Table

Instance Name	Physical Address
R5SS0	0006 0090h
R5SS1	0006 0090h

Figure 4-89. TMU_1_COSPUF32_R2 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R2							
R/W							
0h							

Table 4-203. TMU_1_COSPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R2

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4.1.2.90 TMU_1_COSPUF32_R3 Register

4.1.2.90.1 TMU_1_COSPUF32_R3 Register (Offset = 98h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-204. Instance Table

Instance Name	Physical Address
R5SS0	0006 0098h
R5SS1	0006 0098h

Figure 4-90. TMU_1_COSPUF32_R3 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R3							
R/W							
0h							

Table 4-205. TMU_1_COSPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R3

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4.1.2.91 TMU_1_COSPUF32_R4 Register

4.1.2.91.1 TMU_1_COSPUF32_R4 Register (Offset = A0h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-206. Instance Table

Instance Name	Physical Address
R5SS0	0006 00A0h
R5SS1	0006 00A0h

Figure 4-91. TMU_1_COSPUF32_R4 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R4							
R/W							
0h							

Table 4-207. TMU_1_COSPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R4

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4.1.2.92 TMU_1_COSPUF32_R5 Register

4.1.2.92.1 TMU_1_COSPUF32_R5 Register (Offset = A8h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R5.

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Table 4-208. Instance Table

Instance Name	Physical Address
R5SS0	0006 00A8h
R5SS1	0006 00A8h

Figure 4-92. TMU_1_COSPUF32_R5 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R5							
R/W							
0h							

Table 4-209. TMU_1_COSPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R5

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4.1.2.93 TMU_1_COSPUF32_R6 Register

4.1.2.93.1 TMU_1_COSPUF32_R6 Register (Offset = B0h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R6.

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Table 4-210. Instance Table

Instance Name	Physical Address
R5SS0	0006 00B0h
R5SS1	0006 00B0h

Figure 4-93. TMU_1_COSPUF32_R6 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R6							
R/W							
0h							

Table 4-211. TMU_1_COSPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R6

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4.1.2.94 TMU_1_COSPUF32_R7 Register

4.1.2.94.1 TMU_1_COSPUF32_R7 Register (Offset = B8h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R7.

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Table 4-212. Instance Table

Instance Name	Physical Address
R5SS0	0006 00B8h
R5SS1	0006 00B8h

Figure 4-94. TMU_1_COSPUF32_R7 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R7							
R/W							
0h							

Table 4-213. TMU_1_COSPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R7

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4.1.2.95 TMU_1_ATANPUF32_R0 Register

4.1.2.95.1 TMU_1_ATANPUF32_R0 Register (Offset = C0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-214. Instance Table

Instance Name	Physical Address
R5SS0	0006 00C0h
R5SS1	0006 00C0h

Figure 4-95. TMU_1_ATANPUF32_R0 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R0							
R/W							
0h							

Table 4-215. TMU_1_ATANPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R0

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4.1.2.96 TMU_1_ATANPUF32_R1 Register

4.1.2.96.1 TMU_1_ATANPUF32_R1 Register (Offset = C8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-216. Instance Table

Instance Name	Physical Address
R5SS0	0006 00C8h
R5SS1	0006 00C8h

Figure 4-96. TMU_1_ATANPUF32_R1 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R1							
R/W							
0h							

Table 4-217. TMU_1_ATANPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R1

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4.1.2.97 TMU_1_ATANPUF32_R2 Register

4.1.2.97.1 TMU_1_ATANPUF32_R2 Register (Offset = D0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-218. Instance Table

Instance Name	Physical Address
R5SS0	0006 00D0h
R5SS1	0006 00D0h

Figure 4-97. TMU_1_ATANPUF32_R2 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R2							
R/W							
0h							

Table 4-219. TMU_1_ATANPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R2

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4.1.2.98 TMU_1_ATANPUF32_R3 Register

4.1.2.98.1 TMU_1_ATANPUF32_R3 Register (Offset = D8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-220. Instance Table

Instance Name	Physical Address
R5SS0	0006 00D8h
R5SS1	0006 00D8h

Figure 4-98. TMU_1_ATANPUF32_R3 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R3							
R/W							
0h							

Table 4-221. TMU_1_ATANPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R3

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4.1.2.99 TMU_1_ATANPUF32_R4 Register

4.1.2.99.1 TMU_1_ATANPUF32_R4 Register (Offset = E0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-222. Instance Table

Instance Name	Physical Address
R5SS0	0006 00E0h
R5SS1	0006 00E0h

Figure 4-99. TMU_1_ATANPUF32_R4 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R4							
R/W							
0h							

Table 4-223. TMU_1_ATANPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R4

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4.1.2.100 TMU_1_ATANPUF32_R5 Register

4.1.2.100.1 TMU_1_ATANPUF32_R5 Register (Offset = E8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R5.

Return to Summary Table

Table 4-224. Instance Table

Instance Name	Physical Address
R5SS0	0006 00E8h
R5SS1	0006 00E8h

Figure 4-100. TMU_1_ATANPUF32_R5 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R5							
R/W							
0h							

Table 4-225. TMU_1_ATANPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R5

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4.1.2.101 TMU_1_ATANPUF32_R6 Register

4.1.2.101.1 TMU_1_ATANPUF32_R6 Register (Offset = F0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-226. Instance Table

Instance Name	Physical Address
R5SS0	0006 00F0h
R5SS1	0006 00F0h

Figure 4-101. TMU_1_ATANPUF32_R6 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R6							
R/W							
0h							

Table 4-227. TMU_1_ATANPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R6

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4.1.2.102 TMU_1_ATANPUF32_R7 Register

4.1.2.102.1 TMU_1_ATANPUF32_R7 Register (Offset = F8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-228. Instance Table

Instance Name	Physical Address
R5SS0	0006 00F8h
R5SS1	0006 00F8h

Figure 4-102. TMU_1_ATANPUF32_R7 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R7							
R/W							
0h							

Table 4-229. TMU_1_ATANPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R7

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4.1.2.103 TMU_1_IEXP2F32_R0 Register

4.1.2.103.1 TMU_1_IEXP2F32_R0 Register (Offset = 140h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-230. Instance Table

Instance Name	Physical Address
R5SS0	0006 0140h
R5SS1	0006 0140h

Figure 4-103. TMU_1_IEXP2F32_R0 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R0							
R/W							
0h							

Table 4-231. TMU_1_IEXP2F32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R0

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4.1.2.104 TMU_1_IEXP2F32_R1 Register

4.1.2.104.1 TMU_1_IEXP2F32_R1 Register (Offset = 148h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-232. Instance Table

Instance Name	Physical Address
R5SS0	0006 0148h
R5SS1	0006 0148h

Figure 4-104. TMU_1_IEXP2F32_R1 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R1							
R/W							
0h							

Table 4-233. TMU_1_IEXP2F32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R1

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4.1.2.105 TMU_1_IEXP2F32_R2 Register

4.1.2.105.1 TMU_1_IEXP2F32_R2 Register (Offset = 150h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-234. Instance Table

Instance Name	Physical Address
R5SS0	0006 0150h
R5SS1	0006 0150h

Figure 4-105. TMU_1_IEXP2F32_R2 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R2							
R/W							
0h							

Table 4-235. TMU_1_IEXP2F32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R2

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4.1.2.106 TMU_1_IEXP2F32_R3 Register

4.1.2.106.1 TMU_1_IEXP2F32_R3 Register (Offset = 158h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-236. Instance Table

Instance Name	Physical Address
R5SS0	0006 0158h
R5SS1	0006 0158h

Figure 4-106. TMU_1_IEXP2F32_R3 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R3							
R/W							
0h							

Table 4-237. TMU_1_IEXP2F32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R3

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4.1.2.107 TMU_1_IEXP2F32_R4 Register

4.1.2.107.1 TMU_1_IEXP2F32_R4 Register (Offset = 160h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-238. Instance Table

Instance Name	Physical Address
R5SS0	0006 0160h
R5SS1	0006 0160h

Figure 4-107. TMU_1_IEXP2F32_R4 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R4							
R/W							
0h							

Table 4-239. TMU_1_IEXP2F32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R4

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4.1.2.108 TMU_1_IEXP2F32_R5 Register

4.1.2.108.1 TMU_1_IEXP2F32_R5 Register (Offset = 168h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R5.

Return to Summary Table

Table 4-240. Instance Table

Instance Name	Physical Address
R5SS0	0006 0168h
R5SS1	0006 0168h

Figure 4-108. TMU_1_IEXP2F32_R5 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R5							
R/W							
0h							

Table 4-241. TMU_1_IEXP2F32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R5

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4.1.2.109 TMU_1_IEXP2F32_R6 Register

4.1.2.109.1 TMU_1_IEXP2F32_R6 Register (Offset = 170h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-242. Instance Table

Instance Name	Physical Address
R5SS0	0006 0170h
R5SS1	0006 0170h

Figure 4-109. TMU_1_IEXP2F32_R6 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R6							
R/W							
0h							

Table 4-243. TMU_1_IEXP2F32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R6

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4.1.2.110 TMU_1_IEXP2F32_R7 Register

4.1.2.110.1 TMU_1_IEXP2F32_R7 Register (Offset = 178h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-244. Instance Table

Instance Name	Physical Address
R5SS0	0006 0178h
R5SS1	0006 0178h

Figure 4-110. TMU_1_IEXP2F32_R7 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R7							
R/W							
0h							

Table 4-245. TMU_1_IEXP2F32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R7

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4.1.2.111 TMU_1_LOG2F32_R0 Register

4.1.2.111.1 TMU_1_LOG2F32_R0 Register (Offset = 180h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-246. Instance Table

Instance Name	Physical Address
R5SS0	0006 0180h
R5SS1	0006 0180h

Figure 4-111. TMU_1_LOG2F32_R0 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R0							
R/W							
0h							

Table 4-247. TMU_1_LOG2F32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R0

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4.1.2.112 TMU_1_LOG2F32_R1 Register

4.1.2.112.1 TMU_1_LOG2F32_R1 Register (Offset = 188h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-248. Instance Table

Instance Name	Physical Address
R5SS0	0006 0188h
R5SS1	0006 0188h

Figure 4-112. TMU_1_LOG2F32_R1 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R1							
R/W							
0h							

Table 4-249. TMU_1_LOG2F32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R1

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4.1.2.113 TMU_1_LOG2F32_R2 Register

4.1.2.113.1 TMU_1_LOG2F32_R2 Register (Offset = 190h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-250. Instance Table

Instance Name	Physical Address
R5SS0	0006 0190h
R5SS1	0006 0190h

Figure 4-113. TMU_1_LOG2F32_R2 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R2							
R/W							
0h							

Table 4-251. TMU_1_LOG2F32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R2

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4.1.2.114 TMU_1_LOG2F32_R3 Register

4.1.2.114.1 TMU_1_LOG2F32_R3 Register (Offset = 198h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-252. Instance Table

Instance Name	Physical Address
R5SS0	0006 0198h
R5SS1	0006 0198h

Figure 4-114. TMU_1_LOG2F32_R3 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R3							
R/W							
0h							

Table 4-253. TMU_1_LOG2F32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R3

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4.1.2.115 TMU_1_LOG2F32_R4 Register

4.1.2.115.1 TMU_1_LOG2F32_R4 Register (Offset = 1A0h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-254. Instance Table

Instance Name	Physical Address
R5SS0	0006 01A0h
R5SS1	0006 01A0h

Figure 4-115. TMU_1_LOG2F32_R4 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R4							
R/W							
0h							

Table 4-255. TMU_1_LOG2F32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R4

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4.1.2.116 TMU_1_LOG2F32_R5 Register

4.1.2.116.1 TMU_1_LOG2F32_R5 Register (Offset = 1A8h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R5.

Return to Summary Table

Table 4-256. Instance Table

Instance Name	Physical Address
R5SS0	0006 01A8h
R5SS1	0006 01A8h

Figure 4-116. TMU_1_LOG2F32_R5 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R5							
R/W							
0h							

Table 4-257. TMU_1_LOG2F32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R5

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4.1.2.117 TMU_1_LOG2F32_R6 Register

4.1.2.117.1 TMU_1_LOG2F32_R6 Register (Offset = 1B0h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-258. Instance Table

Instance Name	Physical Address
R5SS0	0006 01B0h
R5SS1	0006 01B0h

Figure 4-117. TMU_1_LOG2F32_R6 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R6							
R/W							
0h							

Table 4-259. TMU_1_LOG2F32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R6

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4.1.2.118 TMU_1_LOG2F32_R7 Register

4.1.2.118.1 TMU_1_LOG2F32_R7 Register (Offset = 1B8h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-260. Instance Table

Instance Name	Physical Address
R5SS0	0006 01B8h
R5SS1	0006 01B8h

Figure 4-118. TMU_1_LOG2F32_R7 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R7							
R/W							
0h							

Table 4-261. TMU_1_LOG2F32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R7

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4.1.2.119 TMU_1_QUADF32_X_R0_R1 Register

4.1.2.119.1 TMU_1_QUADF32_X_R0_R1 Register (Offset = 1C0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R0 and R1.

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Table 4-262. Instance Table

Instance Name	Physical Address
R5SS0	0006 01C0h
R5SS1	0006 01C0h

Figure 4-119. TMU_1_QUADF32_X_R0_R1 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R0_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R0_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R0_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R0_R1							
R/W							
0h							

Table 4-263. TMU_1_QUADF32_X_R0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R0_R1	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R0 and R1

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4.1.2.120 TMU_1_QUADF32_X_R1_R2 Register

4.1.2.120.1 TMU_1_QUADF32_X_R1_R2 Register (Offset = 1C8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R1 and R2.

Return to Summary Table

Table 4-264. Instance Table

Instance Name	Physical Address
R5SS0	0006 01C8h
R5SS1	0006 01C8h

Figure 4-120. TMU_1_QUADF32_X_R1_R2 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R1_R2							
R/W							
0h							

Table 4-265. TMU_1_QUADF32_X_R1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R1_R2	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R1 and R2

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4.1.2.121 TMU_1_QUADF32_X_R2_R3 Register

4.1.2.121.1 TMU_1_QUADF32_X_R2_R3 Register (Offset = 1D0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R2 and R3.

Return to Summary Table

Table 4-266. Instance Table

Instance Name	Physical Address
R5SS0	0006 01D0h
R5SS1	0006 01D0h

Figure 4-121. TMU_1_QUADF32_X_R2_R3 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R2_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R2_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R2_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R2_R3							
R/W							
0h							

Table 4-267. TMU_1_QUADF32_X_R2_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R2_R3	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R2 and R3

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4.1.2.122 TMU_1_QUADF32_X_R3_R4 Register

4.1.2.122.1 TMU_1_QUADF32_X_R3_R4 Register (Offset = 1D8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R3 and R4.

Return to Summary Table

Table 4-268. Instance Table

Instance Name	Physical Address
R5SS0	0006 01D8h
R5SS1	0006 01D8h

Figure 4-122. TMU_1_QUADF32_X_R3_R4 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R3_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R3_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R3_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R3_R4							
R/W							
0h							

Table 4-269. TMU_1_QUADF32_X_R3_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R3_R4	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R3 and R4

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4.1.2.123 TMU_1_QUADF32_X_R4_R5 Register

4.1.2.123.1 TMU_1_QUADF32_X_R4_R5 Register (Offset = 1E0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R4 and R5.

Return to Summary Table

Table 4-270. Instance Table

Instance Name	Physical Address
R5SS0	0006 01E0h
R5SS1	0006 01E0h

Figure 4-123. TMU_1_QUADF32_X_R4_R5 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R4_R5							
R/W							
0h							

Table 4-271. TMU_1_QUADF32_X_R4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R4_R5	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R4 and R5

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4.1.2.124 TMU_1_QUADF32_X_R5SS0_R6 Register

4.1.2.124.1 TMU_1_QUADF32_X_R5SS0_R6 Register (Offset = 1E8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R5 and R6.

Return to Summary Table

Table 4-272. Instance Table

Instance Name	Physical Address
R5SS0	0006 01E8h
R5SS1	0006 01E8h

Figure 4-124. TMU_1_QUADF32_X_R5SS0_R6 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R5_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R5_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R5_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R5_R6							
R/W							
0h							

Table 4-273. TMU_1_QUADF32_X_R5SS0_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R5_R6	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R5 and R6

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4.1.2.125 TMU_1_QUADF32_X_R6_R7 Register

4.1.2.125.1 TMU_1_QUADF32_X_R6_R7 Register (Offset = 1F0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R6 and R7.

Return to Summary Table

Table 4-274. Instance Table

Instance Name	Physical Address
R5SS0	0006 01F0h
R5SS1	0006 01F0h

Figure 4-125. TMU_1_QUADF32_X_R6_R7 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R6_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R6_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R6_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R6_R7							
R/W							
0h							

Table 4-275. TMU_1_QUADF32_X_R6_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R6_R7	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R6 and R7

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4.1.2.126 TMU_1_RESULT_R0 Register

4.1.2.126.1 TMU_1_RESULT_R0 Register (Offset = 280h) [reset = 0h]

R0 result register.

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Table 4-276. Instance Table

Instance Name	Physical Address
R5SS0	0006 0280h
R5SS1	0006 0280h

Figure 4-126. TMU_1_RESULT_R0 Name Register

31	30	29	28	27	26	25	24
R0							
R							
0h							
23	22	21	20	19	18	17	16
R0							
R							
0h							
15	14	13	12	11	10	9	8
R0							
R							
0h							
7	6	5	4	3	2	1	0
R0							
R							
0h							

Table 4-277. TMU_1_RESULT_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R0	R	0h	R0 result register

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4.1.2.127 TMU_1_RESULT_R1 Register

4.1.2.127.1 TMU_1_RESULT_R1 Register (Offset = 288h) [reset = 0h]

R1 result register.

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Table 4-278. Instance Table

Instance Name	Physical Address
R5SS0	0006 0288h
R5SS1	0006 0288h

Figure 4-127. TMU_1_RESULT_R1 Name Register

31	30	29	28	27	26	25	24
R1							
R							
0h							
23	22	21	20	19	18	17	16
R1							
R							
0h							
15	14	13	12	11	10	9	8
R1							
R							
0h							
7	6	5	4	3	2	1	0
R1							
R							
0h							

Table 4-279. TMU_1_RESULT_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R1	R	0h	R1 result register

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4.1.2.128 TMU_1_RESULT_R2 Register

4.1.2.128.1 TMU_1_RESULT_R2 Register (Offset = 290h) [reset = 0h]

R2 result register.

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Table 4-280. Instance Table

Instance Name	Physical Address
R5SS0	0006 0290h
R5SS1	0006 0290h

Figure 4-128. TMU_1_RESULT_R2 Name Register

31	30	29	28	27	26	25	24
R2							
R							
0h							
23	22	21	20	19	18	17	16
R2							
R							
0h							
15	14	13	12	11	10	9	8
R2							
R							
0h							
7	6	5	4	3	2	1	0
R2							
R							
0h							

Table 4-281. TMU_1_RESULT_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R2	R	0h	R2 result register

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4.1.2.129 TMU_1_RESULT_R3 Register

4.1.2.129.1 TMU_1_RESULT_R3 Register (Offset = 298h) [reset = 0h]

R3 result register.

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Table 4-282. Instance Table

Instance Name	Physical Address
R5SS0	0006 0298h
R5SS1	0006 0298h

Figure 4-129. TMU_1_RESULT_R3 Name Register

31	30	29	28	27	26	25	24
R3							
R							
0h							
23	22	21	20	19	18	17	16
R3							
R							
0h							
15	14	13	12	11	10	9	8
R3							
R							
0h							
7	6	5	4	3	2	1	0
R3							
R							
0h							

Table 4-283. TMU_1_RESULT_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R3	R	0h	R3 result register

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4.1.2.130 TMU_1_RESULT_R4 Register

4.1.2.130.1 TMU_1_RESULT_R4 Register (Offset = 2A0h) [reset = 0h]

R4 result register.

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Table 4-284. Instance Table

Instance Name	Physical Address
R5SS0	0006 02A0h
R5SS1	0006 02A0h

Figure 4-130. TMU_1_RESULT_R4 Name Register

31	30	29	28	27	26	25	24
R4							
R							
0h							
23	22	21	20	19	18	17	16
R4							
R							
0h							
15	14	13	12	11	10	9	8
R4							
R							
0h							
7	6	5	4	3	2	1	0
R4							
R							
0h							

Table 4-285. TMU_1_RESULT_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R4	R	0h	R4 result register

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4.1.2.131 TMU_1_RESULT_R5 Register

4.1.2.131.1 TMU_1_RESULT_R5 Register (Offset = 2A8h) [reset = 0h]

R5 result register.

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Table 4-286. Instance Table

Instance Name	Physical Address
R5SS0	0006 02A8h
R5SS1	0006 02A8h

Figure 4-131. TMU_1_RESULT_R5 Name Register

31	30	29	28	27	26	25	24
R5							
R							
0h							
23	22	21	20	19	18	17	16
R5							
R							
0h							
15	14	13	12	11	10	9	8
R5							
R							
0h							
7	6	5	4	3	2	1	0
R5							
R							
0h							

Table 4-287. TMU_1_RESULT_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5	R	0h	R5 result register

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4.1.2.132 TMU_1_RESULT_R6 Register

4.1.2.132.1 TMU_1_RESULT_R6 Register (Offset = 2B0h) [reset = 0h]

R6 result register.

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Table 4-288. Instance Table

Instance Name	Physical Address
R5SS0	0006 02B0h
R5SS1	0006 02B0h

Figure 4-132. TMU_1_RESULT_R6 Name Register

31	30	29	28	27	26	25	24
R6							
R							
0h							
23	22	21	20	19	18	17	16
R6							
R							
0h							
15	14	13	12	11	10	9	8
R6							
R							
0h							
7	6	5	4	3	2	1	0
R6							
R							
0h							

Table 4-289. TMU_1_RESULT_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R6	R	0h	R6 result register

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4.1.2.133 TMU_1_RESULT_R7 Register

4.1.2.133.1 TMU_1_RESULT_R7 Register (Offset = 2B8h) [reset = 0h]

R7 result register.

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Table 4-290. Instance Table

Instance Name	Physical Address
R5SS0	0006 02B8h
R5SS1	0006 02B8h

Figure 4-133. TMU_1_RESULT_R7 Name Register

31	30	29	28	27	26	25	24
R7							
R							
0h							
23	22	21	20	19	18	17	16
R7							
R							
0h							
15	14	13	12	11	10	9	8
R7							
R							
0h							
7	6	5	4	3	2	1	0
R7							
R							
0h							

Table 4-291. TMU_1_RESULT_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R7	R	0h	R7 result register

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4.1.2.134 TMU_1_CSAVE_R0 Register

4.1.2.134.1 TMU_1_CSAVE_R0 Register (Offset = 2C0h) [reset = 0h]

Context save of R0 result register.

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Table 4-292. Instance Table

Instance Name	Physical Address
R5SS0	0006 02C0h
R5SS1	0006 02C0h

Figure 4-134. TMU_1_CSAVE_R0 Name Register

31	30	29	28	27	26	25	24
CSAVE_R0							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R0							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R0							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R0							
R							
0h							

Table 4-293. TMU_1_CSAVE_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R0	R	0h	Context save of R0 result register

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4.1.2.135 TMU_1_CSAVE_R1 Register

4.1.2.135.1 TMU_1_CSAVE_R1 Register (Offset = 2C8h) [reset = 0h]

Context save of R1 result register.

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Table 4-294. Instance Table

Instance Name	Physical Address
R5SS0	0006 02C8h
R5SS1	0006 02C8h

Figure 4-135. TMU_1_CSAVE_R1 Name Register

31	30	29	28	27	26	25	24
CSAVE_R1							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R1							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R1							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R1							
R							
0h							

Table 4-295. TMU_1_CSAVE_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R1	R	0h	Context save of R1 result register

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4.1.2.136 TMU_1_CSAVE_R2 Register

4.1.2.136.1 TMU_1_CSAVE_R2 Register (Offset = 2D0h) [reset = 0h]

Context save of R2 result register.

Return to Summary Table

Table 4-296. Instance Table

Instance Name	Physical Address
R5SS0	0006 02D0h
R5SS1	0006 02D0h

Figure 4-136. TMU_1_CSAVE_R2 Name Register

31	30	29	28	27	26	25	24
CSAVE_R2							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R2							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R2							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R2							
R							
0h							

Table 4-297. TMU_1_CSAVE_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R2	R	0h	Context save of R2 result register

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4.1.2.137 TMU_1_CSAVE_R3 Register

4.1.2.137.1 TMU_1_CSAVE_R3 Register (Offset = 2D8h) [reset = 0h]

Context save of R3 result register.

Return to Summary Table

Table 4-298. Instance Table

Instance Name	Physical Address
R5SS0	0006 02D8h
R5SS1	0006 02D8h

Figure 4-137. TMU_1_CSAVE_R3 Name Register

31	30	29	28	27	26	25	24
CSAVE_R3							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R3							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R3							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R3							
R							
0h							

Table 4-299. TMU_1_CSAVE_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R3	R	0h	Context save of R3 result register

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4.1.2.138 TMU_1_CSAVE_R4 Register

4.1.2.138.1 TMU_1_CSAVE_R4 Register (Offset = 2E0h) [reset = 0h]

Context save of R4 result register.

Return to Summary Table

Table 4-300. Instance Table

Instance Name	Physical Address
R5SS0	0006 02E0h
R5SS1	0006 02E0h

Figure 4-138. TMU_1_CSAVE_R4 Name Register

31	30	29	28	27	26	25	24
CSAVE_R4							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R4							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R4							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R4							
R							
0h							

Table 4-301. TMU_1_CSAVE_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R4	R	0h	Context save of R4 result register

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4.1.2.139 TMU_1_CSAVE_R5 Register

4.1.2.139.1 TMU_1_CSAVE_R5 Register (Offset = 2E8h) [reset = 0h]

Context save of R5 result register.

Return to Summary Table

Table 4-302. Instance Table

Instance Name	Physical Address
R5SS0	0006 02E8h
R5SS1	0006 02E8h

Figure 4-139. TMU_1_CSAVE_R5 Name Register

31	30	29	28	27	26	25	24
CSAVE_R5							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R5							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R5							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R5							
R							
0h							

Table 4-303. TMU_1_CSAVE_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R5	R	0h	Context save of R5 result register

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4.1.2.140 TMU_1_CSAVE_R6 Register

4.1.2.140.1 TMU_1_CSAVE_R6 Register (Offset = 2F0h) [reset = 0h]

Context save of R6 result register.

Return to Summary Table

Table 4-304. Instance Table

Instance Name	Physical Address
R5SS0	0006 02F0h
R5SS1	0006 02F0h

Figure 4-140. TMU_1_CSAVE_R6 Name Register

31	30	29	28	27	26	25	24
CSAVE_R6							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R6							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R6							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R6							
R							
0h							

Table 4-305. TMU_1_CSAVE_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R6	R	0h	Context save of R6 result register

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4.1.2.141 TMU_1_CSAVE_R7 Register

4.1.2.141.1 TMU_1_CSAVE_R7 Register (Offset = 2F8h) [reset = 0h]

Context save of R7 result register.

Return to Summary Table

Table 4-306. Instance Table

Instance Name	Physical Address
R5SS0	0006 02F8h
R5SS1	0006 02F8h

Figure 4-141. TMU_1_CSAVE_R7 Name Register

31	30	29	28	27	26	25	24
CSAVE_R7							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R7							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R7							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R7							
R							
0h							

Table 4-307. TMU_1_CSAVE_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R7	R	0h	Context save of R7 result register

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4.1.2.142 TMU_1_CSAVE_OP2 Register

4.1.2.142.1 TMU_1_CSAVE_OP2 Register (Offset = 300h) [reset = 0h]

Context save of Operarand2 result register.

Return to Summary Table

Table 4-308. Instance Table

Instance Name	Physical Address
R5SS0	0006 0300h
R5SS1	0006 0300h

Figure 4-142. TMU_1_CSAVE_OP2 Name Register

31	30	29	28	27	26	25	24
CSAVE_OP2							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_OP2							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_OP2							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_OP2							
R							
0h							

Table 4-309. TMU_1_CSAVE_OP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_OP2	R	0h	Context save of operand 2 [OP2] result register

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4.1.2.143 TMU_1_CONTEXT_SAVE Register

4.1.2.143.1 TMU_1_CONTEXT_SAVE Register (Offset = 308h) [reset = 0h]

Register to initiate context save of result registers.

Return to Summary Table

Table 4-310. Instance Table

Instance Name	Physical Address
R5SS0	0006 0308h
R5SS1	0006 0308h

Figure 4-143. TMU_1_CONTEXT_SAVE Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							SAVE
R							R/W1TS
0h							0h

Table 4-311. TMU_1_CONTEXT_SAVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	SAVE	R/W1TS	0h	Writing one will initiate context save. Context save will be done only after completion all operations initiated by master before context save was issued. Results registers R0 to R3 and Operand2 will be saved. Note: Contex is saved within IP, not to external memory.

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4.1.2.144 TMU_1_CONTEXT_RESTORE Register

4.1.2.144.1 TMU_1_CONTEXT_RESTORE Register (Offset = 310h) [reset = 0h]

Register to initiate context restore of result registers.

Return to Summary Table

Table 4-312. Instance Table

Instance Name	Physical Address
R5SS0	0006 0310h
R5SS1	0006 0310h

Figure 4-144. TMU_1_CONTEXT_RESTORE Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							RESTORE
R							R/W1TS
0h							0h

Table 4-313. TMU_1_CONTEXT_RESTORE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	RESTORE	R/W1TS	0h	Writing one will initiate context restore. Results registers R0 to R3 and Operand2 will be restored.

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4.1.2.145 TMU_1_STF Register

4.1.2.145.1 TMU_1_STF Register (Offset = 348h) [reset = 0h]

TMU status Register.

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Table 4-314. Instance Table

Instance Name	Physical Address
R5SS0	0006 0348h
R5SS1	0006 0348h

Figure 4-145. TMU_1_STF Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2						LUF_WR_EN	LVF_WR_EN
R						R	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						LUF	LVF
R						R/W	R/W
0h						0h	0h

Table 4-315. TMU_1_STF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_2	R	0h	Reserved
9	LUF_WR_EN	R	0h	Always read as zero, Value is written to this bit either enables/ disables write to LVF [[br] 0:Disbles write to LUF 1:Enables write to LUF
8	LVF_WR_EN	R	0h	Always read as zero, Value is written to this bit either enables/ disables write to LVF [[br] 0:Disbles write to LVF 1:Enables write to LVF
7:2	RESERVED_1	R	0h	Reserved
1	LUF	R/W	0h	Is set to '1' when a TMU operation results in LVF. It is sticky bit, once set, it remains set until it is cleared with write. It can be written only when LUF_WR_EN Is written with '1'
0	LVF	R/W	0h	Is set to '1' when a TMU operation results in LVF. It is sticky bit, once set, it remains set until it is cleared with write. It can be written only when LVF_WR_EN Is written with '1'

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4.1.2.146 TMU_1_PARITY_TEST Register

4.1.2.146.1 TMU_1_PARITY_TEST Register (Offset = 380h) [reset = 0h]

Enabling the parity test feature.

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Table 4-316. Instance Table

Instance Name	Physical Address
R5SS0	0006 0380h
R5SS1	0006 0380h

Figure 4-146. TMU_1_PARITY_TEST Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				TESTEN			
R				R/W			
0h				0h			

Table 4-317. TMU_1_PARITY_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:4	RESERVED_1	R	0h	Reserved
3:0	TESTEN	R/W	0h	1010: Parity test feature is enabled All other values: Parity test feature is disabled Note: When the parity test feature is enabled, acutal registers are not accessible in the memory map. Instead, the parity values are accessible. Parity is computed for every byte and the correponding parity value is available at the bit-0 of every byte. Value of '1' written to the parity bit after enabling the parity test feature can be used to inject the error by inverting the stored parity value.

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4.1.2.147 TMU_1_LCM_LOCK Register

4.1.2.147.1 TMU_1_LCM_LOCK Register (Offset = 390h) [reset = 0h]

LCM lock configuration.

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Table 4-318. Instance Table

Instance Name	Physical Address
R5SS0	0006 0390h
R5SS1	0006 0390h

Figure 4-147. TMU_1_LCM_LOCK Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							PARITY_TEST
R							R/W
0h							0h

Table 4-319. TMU_1_LCM_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	PARITY_TEST	R/W	0h	0: Register configuration is not locked. [[br] 1:Register configuration is locked.

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4.1.2.148 TMU_1_LCM_COMMIT Register

4.1.2.148.1 TMU_1_LCM_COMMIT Register (Offset = 3A0h) [reset = 0h]

LCM commit configuration.

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Table 4-320. Instance Table

Instance Name	Physical Address
R5SS0	0006 03A0h
R5SS1	0006 03A0h

Figure 4-148. TMU_1_LCM_COMMIT Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							PARITY_TEST
R							R/W1TS
0h							0h

Table 4-321. TMU_1_LCM_COMMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	PARITY_TEST	R/W1TS	0h	0: Register lock configuration is not committed. [[br] 1:Register lock configuration is committed. Once configuration is committed, only reset can change the configuration.

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4.1.2.149 TCMB_CORE0_RAM_START Register

4.1.2.149.1 TCMB_CORE0_RAM_START Register (Offset = 0h) [reset = 0h]

Return to Summary Table

Table 4-322. Instance Table

Instance Name	Physical Address
R5SS0	0008 0000h
R5SS1	0008 0000h

Figure 4-149. TCMB_CORE0_RAM_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-323. TCMB_CORE0_RAM_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMB start address

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4.1.2.150 TCMB_CORE0_RAM_END Register

4.1.2.150.1 TCMB_CORE0_RAM_END Register (Offset = 17FFCh) [reset = 0h]

Return to Summary Table

Table 4-324. Instance Table

Instance Name	Physical Address
R5SS0	0009 7FFCh
R5SS1	0009 7FFCh

Figure 4-150. TCMB_CORE0_RAM_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-325. TCMB_CORE0_RAM_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMB end address

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4.1.2.151 TCMB_CORE1_RAM_START Register

4.1.2.151.1 TCMB_CORE1_RAM_START Register (Offset = 0h) [reset = 0h]

Return to Summary Table

Table 4-326. Instance Table

Instance Name	Physical Address
R5SS0	0008 0000h
R5SS1	0008 0000h

Figure 4-151. TCMB_CORE1_RAM_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-327. TCMB_CORE1_RAM_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMB start address

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4.1.2.152 TCMB_CORE1_RAM_END Register

4.1.2.152.1 TCMB_CORE1_RAM_END Register (Offset = 17FFCh) [reset = 0h]

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Table 4-328. Instance Table

Instance Name	Physical Address
R5SS0	0009 7FFCh
R5SS1	0009 7FFCh

Figure 4-152. TCMB_CORE1_RAM_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-329. TCMB_CORE1_RAM_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMB end address

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4.1.2.153 VIM0_PID Register

4.1.2.153.1 VIM0_PID Register (Offset = 0h) [reset = 60900001h]

The Revision Register contains the major and minor revisions for the module.

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Table 4-330. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0000h
R5SS1	50F0 0000h

Figure 4-153. VIM0_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		90h			
23	22	21	20	19	18	17	16
FUNC							
R							
90h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
0h					0h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 4-331. VIM0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme
29:28	BU	R	2h	Business Unit: 10 = Processors
27:16	FUNC	R	90h	Module ID
15:11	RTL	R	0h	RTL revision. Will vary depending on release.
10:8	MAJOR	R	0h	Major revision
7:6	CUSTOM	R	0h	Custom
5:0	MINOR	R	1h	Minor revision

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4.1.2.154 VIM0_INFO Register

4.1.2.154.1 VIM0_INFO Register (Offset = 4h) [reset = 100h]

The Info Register gives the configuration Inforrmation of this VIM.

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Table 4-332. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0004h
R5SS1	50F0 0004h

Figure 4-154. VIM0_INFO Name Register

31	30	29	28	27	26	25	24
RES1							
R							
0h							
23	22	21	20	19	18	17	16
RES1							
R							
0h							
15	14	13	12	11	10	9	8
RES1					INTERRUPTS		
R					R		
0h					100h		
7	6	5	4	3	2	1	0
INTERRUPTS							
R							
100h							

Table 4-333. VIM0_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RES1	R	0h	RESERVE FIELD
10:0	INTERRUPTS	R	100h	Total number of Interrupts

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4.1.2.155 VIM0_PRIIRQ Register

4.1.2.155.1 VIM0_PRIIRQ Register (Offset = 8h) [reset = 0h]

The Prioritized IRQ Register shows the number of the highest priority pending IRQ.

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Table 4-334. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0008h
R5SS1	50F0 0008h

Figure 4-155. VIM0_PRIIRQ Name Register

31	30	29	28	27	26	25	24
VALID	RES2						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES2				PRI			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES3						NUM	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM							
R							
0h							

Table 4-335. VIM0_PRIIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	Indicates that the num field is valid.
30:20	RES2	R	0h	RESERVE FIELD
19:16	PRI	R	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15:10	RES3	R	0h	RESERVE FIELD
9:0	NUM	R	0h	Number of the highest priority pending IRQ. valid only if the valid flag is set.

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4.1.2.156 VIM0_PRIFIQ Register

4.1.2.156.1 VIM0_PRIFIQ Register (Offset = Ch) [reset = 0h]

The Prioritized FIQ Register shows the number of the highest priority pending FIQ.

Return to Summary Table

Table 4-336. Instance Table

Instance Name	Physical Address
R5SS0	50F0 000Ch
R5SS1	50F0 000Ch

Figure 4-156. VIM0_PRIFIQ Name Register

31	30	29	28	27	26	25	24
VALID	RES4						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES4				PRI			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES5						NUM	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM							
R							
0h							

Table 4-337. VIM0_PRIFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	Indicates that the num field is valid.
30:20	RES4	R	0h	RESERVE FIELD
19:16	PRI	R	0h	Priority of the highest priority pending FIQ. valid only if the valid flag is set.
15:10	RES5	R	0h	RESERVE FIELD
9:0	NUM	R	0h	Number of the highest priority pending FIQ. valid only if the valid flag is set.

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4.1.2.157 VIM0_IRQGSTS Register

4.1.2.157.1 VIM0_IRQGSTS Register (Offset = 10h) [reset = 0h]

The IRQ Group Status Register indicates which groups have pending IRQ interrupts.

Return to Summary Table

Table 4-338. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0010h
R5SS1	50F0 0010h

Figure 4-157. VIM0_IRQGSTS Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 4-339. VIM0_IRQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	Indicates that the num field is valid. This field indicates that one or more interrupts in Group M are mapped to IRQ, unmasked, and pending. Bit 0 corresponds to Group 0; Bit 1 corresponds to Group 1 etc. The interrupts associated with each group are [(M*32)+31:M*32].

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4.1.2.158 VIM0_FIQGSTS Register

4.1.2.158.1 VIM0_FIQGSTS Register (Offset = 14h) [reset = 0h]

The FIQ Group Status Register indicates which groups have pending FIQ interrupts.

Return to Summary Table

Table 4-340. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0014h
R5SS1	50F0 0014h

Figure 4-158. VIM0_FIQGSTS Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 4-341. VIM0_FIQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	Indicates that the num field is valid. This field indicates that one or more interrupts in Group M are mapped to FIQ, unmasked, and pending. Bit 0 corresponds to Group 0; Bit 1 corresponds to Group 1 etc. The interrupts associated with each group are [(M*32)+31:M*32].

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4.1.2.159 VIM0_IRQVEC Register

4.1.2.159.1 VIM0_IRQVEC Register (Offset = 18h) [reset = 0h]

The IRQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind IRQ.

Return to Summary Table

Table 4-342. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0018h
R5SS1	50F0 0018h

Figure 4-159. VIM0_IRQVEC Name Register

31	30	29	28	27	26	25	24
ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR						RES21	
R/W						R	
0h						0h	

Table 4-343. VIM0_IRQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	ADDR	R/W	0h	Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized IRQ Register valid flag is true.
1:0	RES21	R	0h	RESERVE FIELD

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4.1.2.160 VIM0_FIQVEC Register

4.1.2.160.1 VIM0_FIQVEC Register (Offset = 1Ch) [reset = 0h]

The FIQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind FIQ.

Return to Summary Table

Table 4-344. Instance Table

Instance Name	Physical Address
R5SS0	50F0 001Ch
R5SS1	50F0 001Ch

Figure 4-160. VIM0_FIQVEC Name Register

31	30	29	28	27	26	25	24
ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDR						RES22	
R/W						R	
0h						0h	

Table 4-345. VIM0_FIQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	ADDR	R/W	0h	Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized FIQ Register valid flag is true.
1:0	RES22	R	0h	RESERVE FIELD

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4.1.2.161 VIM0_ACTIRQ Register

4.1.2.161.1 VIM0_ACTIRQ Register (Offset = 20h) [reset = 0h]

The Active IRQ Register shows the number of the currently active IRQ.

Return to Summary Table

Table 4-346. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0020h
R5SS1	50F0 0020h

Figure 4-161. VIM0_ACTIRQ Name Register

31	30	29	28	27	26	25	24
VALID	RES6						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
RES6				PRI			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
RES7						NUM	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
NUM							
R							
0h							

Table 4-347. VIM0_ACTIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	Indicates that the num field is valid. Set when the IRQ Vector Address Register is read and cleared whenever the IRQ Vector Address Register is written.
30:20	RES6	R	0h	RESERVE FIELD
19:16	PRI	R	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15:10	RES7	R	0h	RESERVE FIELD
9:0	NUM	R	0h	Number of the currently active IRQ. Loaded from teh Prioritized IRQ Register whenever the IRQ Vector Address is read. Valid only if the valid flag is set.

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4.1.2.162 VIM0_ACTFIQ Register

4.1.2.162.1 VIM0_ACTFIQ Register (Offset = 24h) [reset = 0h]

The Active FIQ Register shows the number of the currently active FIQ.

Return to Summary Table

Table 4-348. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0024h
R5SS1	50F0 0024h

Figure 4-162. VIM0_ACTFIQ Name Register

31	30	29	28	27	26	25	24
VALID	RES8						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES8				PRI			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES9						NUM	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM							
R							
0h							

Table 4-349. VIM0_ACTFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	Indicates that the num field is valid. Set when the FIQ Vector Address Register is read and cleared whenever the FIQ Vector Address Register is written.
30:20	RES8	R	0h	RESERVE FIELD
19:16	PRI	R	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15:10	RES9	R	0h	RESERVE FIELD
9:0	NUM	R	0h	Number of the currently active FIQ. Loaded from teh Prioritized FIQ Register whenever the FIQ Vector Address is read. Valid only if the valid flag is set.

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4.1.2.163 VIM0_IRQPRIMSK Register

4.1.2.163.1 VIM0_IRQPRIMSK Register (Offset = 28h) [reset = FFFFh]

The IRQ Priority Mask Register allows all IRQs of a particular priority to be enabled or disabled.

Return to Summary Table

Table 4-350. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0028h
R5SS1	50F0 0028h

Figure 4-163. VIM0_IRQPRIMSK Name Register

31	30	29	28	27	26	25	24
RES24							
R							
0h							
23	22	21	20	19	18	17	16
RES24							
R							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
MSK							
R/W							
FFFFh							

Table 4-351. VIM0_IRQPRIMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES24	R	0h	RESERVE FIELD
15:0	MSK	R/W	FFFFh	Each bit corresponds to the given priority. 1 - IRQs of this priority are enabled. 0 - IRQs of this priority are disabled.

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4.1.2.164 VIM0_FIQPRIMSK Register

4.1.2.164.1 VIM0_FIQPRIMSK Register (Offset = 2Ch) [reset = FFFFh]

The FIQ Priority Mask Register allows all FIQs of a particular priority to be enabled or disabled.

Return to Summary Table

Table 4-352. Instance Table

Instance Name	Physical Address
R5SS0	50F0 002Ch
R5SS1	50F0 002Ch

Figure 4-164. VIM0_FIQPRIMSK Name Register

31	30	29	28	27	26	25	24
RES24							
R							
0h							
23	22	21	20	19	18	17	16
RES24							
R							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
MSK							
R/W							
FFFFh							

Table 4-353. VIM0_FIQPRIMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES24	R	0h	RESERVE FIELD
15:0	MSK	R/W	FFFFh	Each bit corresponds to the given priority. 1 - FIQs of this priority are enabled. 0 - FIQs of this priority are disabled.

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4.1.2.165 VIM0_DEDVEC Register

4.1.2.165.1 VIM0_DEDVEC Register (Offset = 30h) [reset = 0h]

The DED Vector Address contains a default vector address for when an uncorrectable error is detected for an active IRQ or FIQ.

Return to Summary Table

Table 4-354. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0030h
R5SS1	50F0 0030h

Figure 4-165. VIM0_DEDVEC Name Register

31	30	29	28	27	26	25	24
ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR						RES23	
R/W						R	
0h						0h	

Table 4-355. VIM0_DEDVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	ADDR	R/W	0h	Upper 30 bits of the 32-bit vector address.
1:0	RES23	R	0h	RESERVE FIELD

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4.1.2.166 VIM0_RAW_M Register

4.1.2.166.1 VIM0_RAW_M Register (Offset = 400h) [reset = 0h]

Group M Interrupt Raw Status/Set Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-356. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0400h
R5SS1	50F0 0400h

Figure 4-166. VIM0_RAW_M Name Register

31	30	29	28	27	26	25	24
STS							
R/W							
0h							
23	22	21	20	19	18	17	16
STS							
R/W							
0h							
15	14	13	12	11	10	9	8
STS							
R/W							
0h							
7	6	5	4	3	2	1	0
STS							
R/W							
0h							

Table 4-357. VIM0_RAW_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R/W	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive Read 1 Active/Pending Write 0 No effect Write 1 Set to Interrupt Raw Status

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4.1.2.167 VIM0_STS_M Register

4.1.2.167.1 VIM0_STS_M Register (Offset = 404h) [reset = 0h]

Group M Interrupt Enabled Status/Clear Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h .

Return to Summary Table

Table 4-358. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0404h
R5SS1	50F0 0404h

Figure 4-167. VIM0_STS_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-359. VIM0_STS_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or Disabled Read 1 Active/Pending and Enabled Write 0 No effect Write 1 Clear Interrupt Raw Status

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4.1.2.168 VIM0_INTR_EN_SET_M Register

4.1.2.168.1 VIM0_INTR_EN_SET_M Register (Offset = 408h) [reset = 0h]

Group M Interrupt Enabled Set Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-360. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0408h
R5SS1	50F0 0408h

Figure 4-168. VIM0_INTR_EN_SET_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-361. VIM0_INTR_EN_SET_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Disabled Read 1 Enabled Write 0 No effect Write 1 Set Enable

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4.1.2.169 VIM0_INTER_EN_CLR_M Register

4.1.2.169.1 VIM0_INTER_EN_CLR_M Register (Offset = 40Ch) [reset = 0h]

Group M Interrupt Enabled Clear Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-362. Instance Table

Instance Name	Physical Address
R5SS0	50F0 040Ch
R5SS1	50F0 040Ch

Figure 4-169. VIM0_INTER_EN_CLR_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-363. VIM0_INTER_EN_CLR_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Disabled Read 1 Enabled Write 0 No effect Write 1 Clear Enable

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4.1.2.170 VIM0_IRQSTS_M Register

4.1.2.170.1 VIM0_IRQSTS_M Register (Offset = 410h) [reset = 0h]

Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-364. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0410h
R5SS1	50F0 0410h

Figure 4-170. VIM0_IRQSTS_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-365. VIM0_IRQSTS_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive, Disabled, or not an IRQ Read 1 Active/Pending, Enabled, and IRQ Write 0 No effect Write 1 Clear Interrupt Raw Status [if IRQ]

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4.1.2.171 VIM0_FIQSTS_M Register

4.1.2.171.1 VIM0_FIQSTS_M Register (Offset = 414h) [reset = 0h]

Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-366. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0414h
R5SS1	50F0 0414h

Figure 4-171. VIM0_FIQSTS_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-367. VIM0_FIQSTS_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive, Disabled, or not an FIQ Read 1 Active/Pending, Enabled, and FIQ Write 0 No effect Write 1 Clear Interrupt Raw Status [if FIQ]

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4.1.2.172 VIM0_INTMAP_M Register

4.1.2.172.1 VIM0_INTMAP_M Register (Offset = 418h) [reset = 0h]

Group M Interrupt Map Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-368. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0418h
R5SS1	50F0 0418h

Figure 4-172. VIM0_INTMAP_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-369. VIM0_INTMAP_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This field is used to indicate which interrupt the corresponding event influences [if enabled] for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt [default] 1 FIQ Interrupt

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4.1.2.173 VIM0_INTTYPE_M Register

4.1.2.173.1 VIM0_INTTYPE_M Register (Offset = 41Ch) [reset = 0h]

Group M Interrupt Type Map Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-370. Instance Table

Instance Name	Physical Address
R5SS0	50F0 041Ch
R5SS1	50F0 041Ch

Figure 4-173. VIM0_INTTYPE_M Name Register

31	30	29	28	27	26	25	24
VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL							
R/W							
0h							

Table 4-371. VIM0_INTTYPE_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R/W	0h	This field is used to indicate whether the source of an interrupt is a level [default] or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event [see 3.4 Interrupt Handling]. The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit 0 Level [default] 1 Pulse

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4.1.2.174 VIM0_INTPRIORITY_Q Register

4.1.2.174.1 VIM0_INTPRIORITY_Q Register (Offset = 1000h) [reset = Fh]

Interrupt Q Priority Register (where Q is 0 to 255)
Address formula = 50F00000h + Offset + Q x 4h.

Return to Summary Table

Table 4-372. Instance Table

Instance Name	Physical Address
R5SS0	50F0 1000h
R5SS1	50F0 1000h

Figure 4-174. VIM0_INTPRIORITY_Q Name Register

31	30	29	28	27	26	25	24
RES19							
R							
0h							
23	22	21	20	19	18	17	16
RES19							
R							
0h							
15	14	13	12	11	10	9	8
RES19							
R							
0h							
7	6	5	4	3	2	1	0
RES19				PRI			
R				R/W			
0h				Fh			

Table 4-373. VIM0_INTPRIORITY_Q Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES19	R	0h	RESERVE FIELD
3:0	PRI	R/W	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority [Default]

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4.1.2.175 VIM0_INTVECTOR_Q Register

4.1.2.175.1 VIM0_INTVECTOR_Q Register (Offset = 2000h) [reset = 0h]

Interrupt Q Vector Register (Q is 0 to 255)
Address formula = 50F00000h + Offset + Q x 4h.

Return to Summary Table

Table 4-374. Instance Table

Instance Name	Physical Address
R5SS0	50F0 2000h
R5SS1	50F0 2000h

Figure 4-175. VIM0_INTVECTOR_Q Name Register

31	30	29	28	27	26	25	24
ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDR						RES20	
R/W						R	
0h						0h	

Table 4-375. VIM0_INTVECTOR_Q Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	ADDR	R/W	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address [Base Address + 0x18] or FIQ Vector Address [Base Address + 0x1C] and the VECADDR pin when interrupt Q is the active interrupt. Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed. Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1:0	RES20	R	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

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4.1.2.176 VIM1_PID Register

4.1.2.176.1 VIM1_PID Register (Offset = 0h) [reset = 60900001h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 4-376. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0000h
R5SS1	50F0 0000h

Figure 4-176. VIM1_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		90h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
90h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 4-377. VIM1_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme
29:28	BU	R	2h	Business Unit: 10 = Processors
27:16	FUNC	R	90h	Module ID
15:11	RTL	R	0h	RTL revision. Will vary depending on release.
10:8	MAJOR	R	0h	Major revision
7:6	CUSTOM	R	0h	Custom
5:0	MINOR	R	1h	Minor revision

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4.1.2.177 VIM1_INFO Register

4.1.2.177.1 VIM1_INFO Register (Offset = 4h) [reset = 100h]

The Info Register gives the configuration Inforrmation of this VIM.

Return to Summary Table

Table 4-378. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0004h
R5SS1	50F0 0004h

Figure 4-177. VIM1_INFO Name Register

31	30	29	28	27	26	25	24
RES1							
R							
0h							
23	22	21	20	19	18	17	16
RES1							
R							
0h							
15	14	13	12	11	10	9	8
RES1					INTERRUPTS		
R					R		
0h					100h		
7	6	5	4	3	2	1	0
INTERRUPTS							
R							
100h							

Table 4-379. VIM1_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RES1	R	0h	RESERVE FIELD
10:0	INTERRUPTS	R	100h	Total number of Interrupts

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4.1.2.178 VIM1_PRIIRQ Register

4.1.2.178.1 VIM1_PRIIRQ Register (Offset = 8h) [reset = 0h]

The Prioritized IRQ Register shows the number of the highest priority pending IRQ.

Return to Summary Table

Table 4-380. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0008h
R5SS1	50F0 0008h

Figure 4-178. VIM1_PRIIRQ Name Register

31	30	29	28	27	26	25	24
VALID	RES2						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES2				PRI			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES3						NUM	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM							
R							
0h							

Table 4-381. VIM1_PRIIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	Indicates that the num field is valid.
30:20	RES2	R	0h	RESERVE FIELD
19:16	PRI	R	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15:10	RES3	R	0h	RESERVE FIELD
9:0	NUM	R	0h	Number of the highest priority pending IRQ. valid only if the valid flag is set.

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4.1.2.179 VIM1_PRIFIQ Register

4.1.2.179.1 VIM1_PRIFIQ Register (Offset = Ch) [reset = 0h]

The Prioritized FIQ Register shows the number of the highest priority pending FIQ.

Return to Summary Table

Table 4-382. Instance Table

Instance Name	Physical Address
R5SS0	50F0 000Ch
R5SS1	50F0 000Ch

Figure 4-179. VIM1_PRIFIQ Name Register

31	30	29	28	27	26	25	24
VALID	RES4						
R	R						
0h	0h						
23	22	21	20	19	18	17	16
RES4				PRI			
R				R			
0h				0h			
15	14	13	12	11	10	9	8
RES5						NUM	
R						R	
0h						0h	
7	6	5	4	3	2	1	0
NUM							
R							
0h							

Table 4-383. VIM1_PRIFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	Indicates that the num field is valid.
30:20	RES4	R	0h	RESERVE FIELD
19:16	PRI	R	0h	Priority of the highest priority pending FIQ. valid only if the valid flag is set.
15:10	RES5	R	0h	RESERVE FIELD
9:0	NUM	R	0h	Number of the highest priority pending FIQ. valid only if the valid flag is set.

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4.1.2.180 VIM1_IRQGSTS Register

4.1.2.180.1 VIM1_IRQGSTS Register (Offset = 10h) [reset = 0h]

The IRQ Group Status Register indicates which groups have pending IRQ interrupts.

Return to Summary Table

Table 4-384. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0010h
R5SS1	50F0 0010h

Figure 4-180. VIM1_IRQGSTS Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 4-385. VIM1_IRQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	Indicates that the num field is valid.

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4.1.2.181 VIM1_FIQGSTS Register

4.1.2.181.1 VIM1_FIQGSTS Register (Offset = 14h) [reset = 0h]

The FIQ Group Status Register indicates which groups have pending FIQ interrupts.

Return to Summary Table

Table 4-386. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0014h
R5SS1	50F0 0014h

Figure 4-181. VIM1_FIQGSTS Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 4-387. VIM1_FIQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	Indicates that the num field is valid.

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4.1.2.182 VIM1_IRQVEC Register

4.1.2.182.1 VIM1_IRQVEC Register (Offset = 18h) [reset = 0h]

The IRQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind IRQ.

Return to Summary Table

Table 4-388. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0018h
R5SS1	50F0 0018h

Figure 4-182. VIM1_IRQVEC Name Register

31	30	29	28	27	26	25	24
ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDR						RES21	
R/W						R	
0h						0h	

Table 4-389. VIM1_IRQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	ADDR	R/W	0h	Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized IRQ Register valid flag is true.
1:0	RES21	R	0h	RESERVE FIELD

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4.1.2.183 VIM1_FIQVEC Register

4.1.2.183.1 VIM1_FIQVEC Register (Offset = 1Ch) [reset = 0h]

The FIQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind FIQ.

Return to Summary Table

Table 4-390. Instance Table

Instance Name	Physical Address
R5SS0	50F0 001Ch
R5SS1	50F0 001Ch

Figure 4-183. VIM1_FIQVEC Name Register

31	30	29	28	27	26	25	24
ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR						RES22	
R/W						R	
0h						0h	

Table 4-391. VIM1_FIQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	ADDR	R/W	0h	Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized FIQ Register valid flag is true.
1:0	RES22	R	0h	RESERVE FIELD

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4.1.2.184 VIM1_ACTIRQ Register

4.1.2.184.1 VIM1_ACTIRQ Register (Offset = 20h) [reset = 0h]

The Active IRQ Register shows the number of the currently active IRQ.

Return to Summary Table

Table 4-392. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0020h
R5SS1	50F0 0020h

Figure 4-184. VIM1_ACTIRQ Name Register

31	30	29	28	27	26	25	24
VALID	RES6						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES6				PRI			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES7						NUM	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM							
R							
0h							

Table 4-393. VIM1_ACTIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	Indicates that the num field is valid. Set when the IRQ Vector Address Register is read and cleared whenever the IRQ Vector Address Register is written.
30:20	RES6	R	0h	RESERVE FIELD
19:16	PRI	R	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15:10	RES7	R	0h	RESERVE FIELD
9:0	NUM	R	0h	Number of the currently active IRQ. Loaded from teh Prioritized IRQ Register whenever the IRQ Vector Address is read. Valid only if the valid flag is set.

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4.1.2.185 VIM1_ACTFIQ Register

4.1.2.185.1 VIM1_ACTFIQ Register (Offset = 24h) [reset = 0h]

The Active FIQ Register shows the number of the currently active FIQ.

Return to Summary Table

Table 4-394. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0024h
R5SS1	50F0 0024h

Figure 4-185. VIM1_ACTFIQ Name Register

31	30	29	28	27	26	25	24
VALID	RES8						
R	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES8				PRI			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES9						NUM	
R						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM							
R							
0h							

Table 4-395. VIM1_ACTFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	R	0h	Indicates that the num field is valid. Set when the FIQ Vector Address Register is read and cleared whenever the FIQ Vector Address Register is written.
30:20	RES8	R	0h	RESERVE FIELD
19:16	PRI	R	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15:10	RES9	R	0h	RESERVE FIELD
9:0	NUM	R	0h	Number of the currently active FIQ. Loaded from teh Prioritized FIQ Register whenever the FIQ Vector Address is read. Valid only if the valid flag is set.

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4.1.2.186 VIM1_IRQPRIMSK Register

4.1.2.186.1 VIM1_IRQPRIMSK Register (Offset = 28h) [reset = FFFFh]

The IRQ Priority Mask Register allows all IRQs of a particular priority to be enabled or disabled.

Return to Summary Table

Table 4-396. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0028h
R5SS1	50F0 0028h

Figure 4-186. VIM1_IRQPRIMSK Name Register

31	30	29	28	27	26	25	24
RES24							
R							
0h							
23	22	21	20	19	18	17	16
RES24							
R							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
MSK							
R/W							
FFFFh							

Table 4-397. VIM1_IRQPRIMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES24	R	0h	RESERVE FIELD
15:0	MSK	R/W	FFFFh	Each bit corresponds to the given priority. 1 - IRQs of this priority are enabled. 0 - IRQs of this priority are disabled.

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4.1.2.187 VIM1_FIQPRIMSK Register

4.1.2.187.1 VIM1_FIQPRIMSK Register (Offset = 2Ch) [reset = FFFFh]

The FIQ Priority Mask Register allows all FIQs of a particular priority to be enabled or disabled.

Return to Summary Table

Table 4-398. Instance Table

Instance Name	Physical Address
R5SS0	50F0 002Ch
R5SS1	50F0 002Ch

Figure 4-187. VIM1_FIQPRIMSK Name Register

31	30	29	28	27	26	25	24
RES24							
R							
0h							
23	22	21	20	19	18	17	16
RES24							
R							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
MSK							
R/W							
FFFFh							

Table 4-399. VIM1_FIQPRIMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES24	R	0h	RESERVE FIELD
15:0	MSK	R/W	FFFFh	Each bit corresponds to the given priority. 1 - FIQs of this priority are enabled. 0 - FIQs of this priority are disabled.

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4.1.2.188 VIM1_DEDVEC Register

4.1.2.188.1 VIM1_DEDVEC Register (Offset = 30h) [reset = 0h]

The DED Vector Address contains a default vector address for when an uncorrectable error is detected for an active IRQ or FIQ.

Return to Summary Table

Table 4-400. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0030h
R5SS1	50F0 0030h

Figure 4-188. VIM1_DEDVEC Name Register

31	30	29	28	27	26	25	24
ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDR						RES23	
R/W						R	
0h						0h	

Table 4-401. VIM1_DEDVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	ADDR	R/W	0h	Upper 30 bits of the 32-bit vector address.
1:0	RES23	R	0h	RESERVE FIELD

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4.1.2.189 VIM1_RAW_M Register

4.1.2.189.1 VIM1_RAW_M Register (Offset = 400h) [reset = 0h]

Group M Interrupt Raw Status/Set Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-402. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0400h
R5SS1	50F0 0400h

Figure 4-189. VIM1_RAW_M Name Register

31	30	29	28	27	26	25	24
STS							
R/W							
0h							
23	22	21	20	19	18	17	16
STS							
R/W							
0h							
15	14	13	12	11	10	9	8
STS							
R/W							
0h							
7	6	5	4	3	2	1	0
STS							
R/W							
0h							

Table 4-403. VIM1_RAW_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R/W	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive Read 1 Active/Pending Write 0 No effect Write 1 Set to Interrupt Raw Status

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4.1.2.190 VIM1_STS_M Register

4.1.2.190.1 VIM1_STS_M Register (Offset = 404h) [reset = 0h]

Group M Interrupt Enabled Status/Clear Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h .

Return to Summary Table

Table 4-404. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0404h
R5SS1	50F0 0404h

Figure 4-190. VIM1_STS_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-405. VIM1_STS_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or Disabled Read 1 Active/Pending and Enabled Write 0 No effect Write 1 Clear Interrupt Raw Status

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4.1.2.191 VIM1_INTR_EN_SET_M Register

4.1.2.191.1 VIM1_INTR_EN_SET_M Register (Offset = 408h) [reset = 0h]

Group M Interrupt Enabled Set Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-406. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0408h
R5SS1	50F0 0408h

Figure 4-191. VIM1_INTR_EN_SET_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-407. VIM1_INTR_EN_SET_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Disabled Read 1 Enabled Write 0 No effect Write 1 Set Enable

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4.1.2.192 VIM1_INTER_EN_CLR_M Register

4.1.2.192.1 VIM1_INTER_EN_CLR_M Register (Offset = 40Ch) [reset = 0h]

Group M Interrupt Enabled Clear Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-408. Instance Table

Instance Name	Physical Address
R5SS0	50F0 040Ch
R5SS1	50F0 040Ch

Figure 4-192. VIM1_INTER_EN_CLR_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-409. VIM1_INTER_EN_CLR_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Disabled Read 1 Enabled Write 0 No effect Write 1 Clear Enable

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4.1.2.193 VIM1_IRQSTS_M Register

4.1.2.193.1 VIM1_IRQSTS_M Register (Offset = 410h) [reset = 0h]

Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-410. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0410h
R5SS1	50F0 0410h

Figure 4-193. VIM1_IRQSTS_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-411. VIM1_IRQSTS_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive, Disabled, or not an IRQ Read 1 Active/Pending, Enabled, and IRQ Write 0 No effect Write 1 Clear Interrupt Raw Status [if IRQ]

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4.1.2.194 VIM1_FIQSTS_M Register

4.1.2.194.1 VIM1_FIQSTS_M Register (Offset = 414h) [reset = 0h]

Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-412. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0414h
R5SS1	50F0 0414h

Figure 4-194. VIM1_FIQSTS_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	22	21	20	19	18	17	16
MASK							
R/W							
0h							
15	14	13	12	11	10	9	8
MASK							
R/W							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 4-413. VIM1_FIQSTS_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive, Disabled, or not an FIQ Read 1 Active/Pending, Enabled, and FIQ Write 0 No effect Write 1 Clear Interrupt Raw Status [if FIQ]

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4.1.2.195 VIM1_INTMAP_M Register

4.1.2.195.1 VIM1_INTMAP_M Register (Offset = 418h) [reset = 0h]

Group M Interrupt Map Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

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Table 4-414. Instance Table

Instance Name	Physical Address
R5SS0	50F0 0418h
R5SS1	50F0 0418h

Figure 4-195. VIM1_INTMAP_M Name Register

31	30	29	28	27	26	25	24
MASK							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MASK							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MASK							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MASK							
R/W							
0h							

Table 4-415. VIM1_INTMAP_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MASK	R/W	0h	This field is used to indicate which interrupt the corresponding event influences [if enabled] for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt [default] 1 FIQ Interrupt

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4.1.2.196 VIM1_INTTYPE_M Register

4.1.2.196.1 VIM1_INTTYPE_M Register (Offset = 41Ch) [reset = 0h]

Group M Interrupt Type Map Register (M is 0 to 7)
Address formula = 50F00000h + Offset + M x 20h.

Return to Summary Table

Table 4-416. Instance Table

Instance Name	Physical Address
R5SS0	50F0 041Ch
R5SS1	50F0 041Ch

Figure 4-196. VIM1_INTTYPE_M Name Register

31	30	29	28	27	26	25	24
VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL							
R/W							
0h							

Table 4-417. VIM1_INTTYPE_M Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R/W	0h	This field is used to indicate whether the source of an interrupt is a level [default] or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event [see 3.4 Interrupt Handling]. The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit 0 Level [default] 1 Pulse

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4.1.2.197 VIM1_INTPRIORITY_Q Register

4.1.2.197.1 VIM1_INTPRIORITY_Q Register (Offset = 1000h) [reset = Fh]

Interrupt Q Priority Register (where Q is 0 to 255)
Address formula = 50F00000h + Offset + Q x 4h.

Return to Summary Table

Table 4-418. Instance Table

Instance Name	Physical Address
R5SS0	50F0 1000h
R5SS1	50F0 1000h

Figure 4-197. VIM1_INTPRIORITY_Q Name Register

31	30	29	28	27	26	25	24
RES19							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES19							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES19							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES19				PRI			
R				R/W			
0h				Fh			

Table 4-419. VIM1_INTPRIORITY_Q Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RES19	R	0h	RESERVE FIELD
3:0	PRI	R/W	Fh	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority [Default]

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4.1.2.198 VIM1_INTVECTOR_Q Register

4.1.2.198.1 VIM1_INTVECTOR_Q Register (Offset = 2000h) [reset = 0h]

Interrupt Q Vector Register (Q is 0 to 255)
Address formula = 50F00000h + Offset + Q x 4h.

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Table 4-420. Instance Table

Instance Name	Physical Address
R5SS0	50F0 2000h
R5SS1	50F0 2000h

Figure 4-198. VIM1_INTVECTOR_Q Name Register

31	30	29	28	27	26	25	24
ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADDR						RES20	
R/W						R	
0h						0h	

Table 4-421. VIM1_INTVECTOR_Q Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	ADDR	R/W	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address [Base Address + 0x18] or FIQ Vector Address [Base Address + 0x1C] and the VECADDR pin when interrupt Q is the active interrupt. Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed. Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1:0	RES20	R	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

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4.1.2.199 ECC_AGG_CORE0_AGGR_REVISION Register

4.1.2.199.1 ECC_AGG_CORE0_AGGR_REVISION Register (Offset = 0h) [reset = 66A0C200h]

Revision parameters register. The Revision Register contains the major and minor revisions for the ECC aggregator module. It does not
support byte accesses.

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Table 4-422. Instance Table

Instance Name	Physical Address
R5SS0	5300 0000h
R5SS1	5300 4000h

Figure 4-199. ECC_AGG_CORE0_AGGR_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
18h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 4-423. ECC_AGG_CORE0_AGGR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	18h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

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4.1.2.200 ECC_AGG_CORE0_ECC_VECTOR Register

4.1.2.200.1 ECC_AGG_CORE0_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register. ECC RAM ID to select which ECC RAM to control or read status from.

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Table 4-424. Instance Table

Instance Name	Physical Address
R5SS0	5300 0008h
R5SS1	5300 4008h

Figure 4-200. ECC_AGG_CORE0_ECC_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 4-425. ECC_AGG_CORE0_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R	0h	Status to indicate if read on serial VBUS is complete
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

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4.1.2.201 ECC_AGG_CORE0_MISC_STATUS Register

4.1.2.201.1 ECC_AGG_CORE0_MISC_STATUS Register (Offset = Ch) [reset = 1Dh]

Misc Statu register. It contains misc status such as number of ECC RAMs serviced by the ECC aggregator.

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Table 4-426. Instance Table

Instance Name	Physical Address
R5SS0	5300 000Ch
R5SS1	5300 400Ch

Figure 4-201. ECC_AGG_CORE0_MISC_STATUS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">NUM_RAMS</td></tr>
<tr><td colspan="5">NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">1Dh</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">NUM_RAMS</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">1Dh</td></tr>
</table>

Table 4-427. ECC_AGG_CORE0_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Dh	Indicates the number of RAMS serviced by the ECC aggregator

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4.1.2.202 ECC_AGG_CORE0_ECC_WRAP_REVISION Register

4.1.2.202.1 ECC_AGG_CORE0_ECC_WRAP_REVISION Register (Offset = 10h) [reset = 66A40202h]

Revision parameters.

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Table 4-428. Instance Table

Instance Name	Physical Address
R5SS0	5300 0010h
R5SS1	5300 4010h

Figure 4-202. ECC_AGG_CORE0_ECC_WRAP_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A4h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		2h					

Table 4-429. ECC_AGG_CORE0_ECC_WRAP_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A4h	Module ID
15:11	REVRTL	R	0h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	2h	Minor version

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4.1.2.203 ECC_AGG_CORE0_CONTROL Register

4.1.2.203.1 ECC_AGG_CORE0_CONTROL Register (Offset = 14h) [reset = 187h]

ECC Control Register.

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Table 4-430. Instance Table

Instance Name	Physical Address
R5SS0	5300 0014h
R5SS1	5300 4014h

Figure 4-203. ECC_AGG_CORE0_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							CHECK_SVBUS_TIMEOUT
NONE							R/W
0h							1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	1h	1h	1h

Table 4-431. ECC_AGG_CORE0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CHECK_SVBUS_TIMEOUT	R/W	1h	check for svbus timeout errors
7	CHECK_PARITY	R/W	1h	check for parity errors
6	ERROR_ONCE	R/W	0h	Force Error only once
5	FORCE_N_ROW	R/W	0h	Force Error on any RAM read
4	FORCE_DED	R/W	0h	Force Double Bit Error
3	FORCE_SEC	R/W	0h	Force Single Bit Error
2	ENABLE_RMW	R/W	1h	Enable rmw
1	ECC_CHECK	R/W	1h	Enable ECC check
0	ECC_ENABLE	R/W	1h	Enable ECC

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4.1.2.204 ECC_AGG_CORE0_ERROR_CTRL1 Register

4.1.2.204.1 ECC_AGG_CORE0_ERROR_CTRL1 Register (Offset = 18h) [reset = 0h]

ECC Error Control1 Register.

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Table 4-432. Instance Table

Instance Name	Physical Address
R5SS0	5300 0018h
R5SS1	5300 4018h

Figure 4-204. ECC_AGG_CORE0_ERROR_CTRL1 Name Register

31	30	29	28	27	26	25	24
ECC_ROW							
R/W							
0h							
23	22	21	20	19	18	17	16
ECC_ROW							
R/W							
0h							
15	14	13	12	11	10	9	8
ECC_ROW							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_ROW							
R/W							
0h							

Table 4-433. ECC_AGG_CORE0_ERROR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R/W	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

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4.1.2.205 ECC_AGG_CORE0_ERROR_CTRL2 Register

4.1.2.205.1 ECC_AGG_CORE0_ERROR_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ECC Error Control2 Register.

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Table 4-434. Instance Table

Instance Name	Physical Address
R5SS0	5300 001Ch
R5SS1	5300 401Ch

Figure 4-205. ECC_AGG_CORE0_ERROR_CTRL2 Name Register

31	30	29	28	27	26	25	24
ECC_BIT2							
R/W							
0h							
23	22	21	20	19	18	17	16
ECC_BIT2							
R/W							
0h							
15	14	13	12	11	10	9	8
ECC_BIT1							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_BIT1							
R/W							
0h							

Table 4-435. ECC_AGG_CORE0_ERROR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT2	R/W	0h	Data bit that needs to be flipped if double bit error needs to be forced
15:0	ECC_BIT1	R/W	0h	Data bit that needs to be flipped when force_sec is set

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4.1.2.206 ECC_AGG_CORE0_ERROR_STATUS1 Register

4.1.2.206.1 ECC_AGG_CORE0_ERROR_STATUS1 Register (Offset = 20h) [reset = 0h]

ECC Error Status1 Register.

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Table 4-436. Instance Table

Instance Name	Physical Address
R5SS0	5300 0020h
R5SS1	5300 4020h

Figure 4-206. ECC_AGG_CORE0_ERROR_STATUS1 Name Register

31	30	29	28	27	26	25	24
ECC_BIT1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ECC_BIT1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLR_CTRL_REG_ERR	CLR_PARITY_ERR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC	
R/W1TC	R/WD		R/W1TC	R/WD		R/WD	
0h	0h		0h	0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTR_REG_ERR	PARITY_ERR		ECC_OTHER	ECC_DED		ECC_SEC	
R/W1TS	R/W1TS		R/W1TS	R/WI		R/WI	
0h	0h		0h	0h		0h	

Table 4-437. ECC_AGG_CORE0_ERROR_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT1	R	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	R/W1TC	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14:13	CLR_PARITY_ERR	R/WD	0h	Clear parity Error Status
12	CLR_ECC_OTHER	R/W1TC	0h	Clear other Error Status
11:10	CLR_ECC_DED	R/WD	0h	Clear Double Bit Error Status
9:8	CLR_ECC_SEC	R/WD	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	R/W1TS	0h	control register error pending, Level interrupt
6:5	PARITY_ERR	R/W1TS	0h	Level parity error Error Status
4	ECC_OTHER	R/W1TS	0h	Successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3:2	ECC_DED	R/WI	0h	Level Double Bit Error Status
1:0	ECC_SEC	R/WI	0h	Level Single Bit Error Status

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4.1.2.207 ECC_AGG_CORE0_ERROR_STATUS2 Register

4.1.2.207.1 ECC_AGG_CORE0_ERROR_STATUS2 Register (Offset = 24h) [reset = 0h]

ECC Error Status2 Register.

Return to Summary Table

Table 4-438. Instance Table

Instance Name	Physical Address
R5SS0	5300 0024h
R5SS1	5300 4024h

Figure 4-207. ECC_AGG_CORE0_ERROR_STATUS2 Name Register

31	30	29	28	27	26	25	24
ECC_ROW							
R							
0h							
23	22	21	20	19	18	17	16
ECC_ROW							
R							
0h							
15	14	13	12	11	10	9	8
ECC_ROW							
R							
0h							
7	6	5	4	3	2	1	0
ECC_ROW							
R							
0h							

Table 4-439. ECC_AGG_CORE0_ERROR_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R	0h	Row address where the single or double-bit error has occurred

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4.1.2.208 ECC_AGG_CORE0_ERROR_STATUS3 Register

4.1.2.208.1 ECC_AGG_CORE0_ERROR_STATUS3 Register (Offset = 28h) [reset = 0h]

ECC Error Status3 Register.

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Table 4-440. Instance Table

Instance Name	Physical Address
R5SS0	5300 0028h
R5SS1	5300 4028h

Figure 4-208. ECC_AGG_CORE0_ERROR_STATUS3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CLR_SVBUS_TIMEOUT_ERR	RESERVED
NONE						R/W1TC	NONE
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED						SVBUS_TIMEOUT_ERR	WB_PEND
NONE						R/W1TS	R
0h						0h	0h

Table 4-441. ECC_AGG_CORE0_ERROR_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CLR_SVBUS_TIMEOUT_ERR	R/W1TC	0h	Clear svbus timeout Error Status
8:2	RESERVED	NONE	0h	Reserved
1	SVBUS_TIMEOUT_ERR	R/W1TS	0h	Level svbus timeout error Error Status
0	WB_PEND	R	0h	delayed write back pending Status

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4.1.2.209 ECC_AGG_CORE0_SEC_EOI_REG Register

4.1.2.209.1 ECC_AGG_CORE0_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

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Table 4-442. Instance Table

Instance Name	Physical Address
R5SS0	5300 003Ch
R5SS1	5300 403Ch

Figure 4-209. ECC_AGG_CORE0_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 4-443. ECC_AGG_CORE0_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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4.1.2.210 ECC_AGG_CORE0_SEC_STATUS_REG0 Register

4.1.2.210.1 ECC_AGG_CORE0_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 4-444. Instance Table

Instance Name	Physical Address
R5SS0	5300 0040h
R5SS1	5300 4040h

Figure 4-210. ECC_AGG_CORE0_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_RL2_OF_RAMECC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-445. ECC_AGG_CORE0_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_RL2_OF_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_rl2_of_ramecc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend

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Table 4-445. ECC_AGG_CORE0_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

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4.1.2.211 ECC_AGG_CORE0_SEC_ENABLE_SET_REG0 Register

4.1.2.211.1 ECC_AGG_CORE0_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 4-446. Instance Table

Instance Name	Physical Address
R5SS0	5300 0080h
R5SS1	5300 4080h

Figure 4-211. ECC_AGG_CORE0_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_RL2_OF_RAMECC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-447. ECC_AGG_CORE0_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_RL2_OF_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_rl2_of_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend

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Table 4-447. ECC_AGG_CORE0_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

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4.1.2.212 ECC_AGG_CORE0_SEC_ENABLE_CLR_REG0 Register

4.1.2.212.1 ECC_AGG_CORE0_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 4-448. Instance Table

Instance Name	Physical Address
R5SS0	5300 00C0h
R5SS1	5300 40C0h

Figure 4-212. ECC_AGG_CORE0_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_RL2_OF_RAMECC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-449. ECC_AGG_CORE0_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_RL2_OF_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_rl2_of_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend

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Table 4-449. ECC_AGG_CORE0_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

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4.1.2.213 ECC_AGG_CORE0_DED_EOI_REG Register

4.1.2.213.1 ECC_AGG_CORE0_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

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Table 4-450. Instance Table

Instance Name	Physical Address
R5SS0	5300 013Ch
R5SS1	5300 413Ch

Figure 4-213. ECC_AGG_CORE0_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 4-451. ECC_AGG_CORE0_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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4.1.2.214 ECC_AGG_CORE0_DED_STATUS_REG0 Register

4.1.2.214.1 ECC_AGG_CORE0_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 4-452. Instance Table

Instance Name	Physical Address
R5SS0	5300 0140h
R5SS1	5300 4140h

Figure 4-214. ECC_AGG_CORE0_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_RL2_OF_RAMECC_PEND	CPU0_KS_VIM_RAMECC_PEND	B1TCM0_BANK1_PEND	B1TCM0_BANK0_PEND	B0TCM0_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_PEND	ATCM0_BANK1_PEND	ATCM0_BANK0_PEND	CPU0_DDATA_RAM7_PEND	CPU0_DDATA_RAM6_PEND	CPU0_DDATA_RAM5_PEND	CPU0_DDATA_RAM4_PEND	CPU0_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_PEND	CPU0_DDATA_RAM1_PEND	CPU0_DDATA_RAM0_PEND	CPU0_DDIRTY_RAM_PEND	CPU0_DTAG_RAM3_PEND	CPU0_DTAG_RAM2_PEND	CPU0_DTAG_RAM1_PEND	CPU0_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_PEND	CPU0_IDATA_BANK2_PEND	CPU0_IDATA_BANK1_PEND	CPU0_IDATA_BANK0_PEND	CPU0_ITAG_RAM3_PEND	CPU0_ITAG_RAM2_PEND	CPU0_ITAG_RAM1_PEND	CPU0_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-453. ECC_AGG_CORE0_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_RL2_OF_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_rl2_of_ramecc_pend
27	CPU0_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend

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Table 4-453. ECC_AGG_CORE0_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU0_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

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4.1.2.215 ECC_AGG_CORE0_DED_ENABLE_SET_REG0 Register

4.1.2.215.1 ECC_AGG_CORE0_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 4-454. Instance Table

Instance Name	Physical Address
R5SS0	5300 0180h
R5SS1	5300 4180h

Figure 4-215. ECC_AGG_CORE0_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_RL2_OF_RAMECC_ENABLE_SET	CPU0_KS_VIM_RAMECC_ENABLE_SET	B1TCM0_BANK1_ENABLE_SET	B1TCM0_BANK0_ENABLE_SET	B0TCM0_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_ENABLE_SET	ATCM0_BANK1_ENABLE_SET	ATCM0_BANK0_ENABLE_SET	CPU0_DDATA_RAM7_ENABLE_SET	CPU0_DDATA_RAM6_ENABLE_SET	CPU0_DDATA_RAM5_ENABLE_SET	CPU0_DDATA_RAM4_ENABLE_SET	CPU0_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_ENABLE_SET	CPU0_DDATA_RAM1_ENABLE_SET	CPU0_DDATA_RAM0_ENABLE_SET	CPU0_DDIRTY_RAM_ENABLE_SET	CPU0_DTAG_RAM3_ENABLE_SET	CPU0_DTAG_RAM2_ENABLE_SET	CPU0_DTAG_RAM1_ENABLE_SET	CPU0_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_ENABLE_SET	CPU0_IDATA_BANK2_ENABLE_SET	CPU0_IDATA_BANK1_ENABLE_SET	CPU0_IDATA_BANK0_ENABLE_SET	CPU0_ITAG_RAM3_ENABLE_SET	CPU0_ITAG_RAM2_ENABLE_SET	CPU0_ITAG_RAM1_ENABLE_SET	CPU0_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-455. ECC_AGG_CORE0_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_RL2_OF_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_rl2_of_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank1_pend

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Table 4-455. ECC_AGG_CORE0_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM0_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

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4.1.2.216 ECC_AGG_CORE0_DED_ENABLE_CLR_REG0 Register

4.1.2.216.1 ECC_AGG_CORE0_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 4-456. Instance Table

Instance Name	Physical Address
R5SS0	5300 01C0h
R5SS1	5300 41C0h

Figure 4-216. ECC_AGG_CORE0_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU0_RL2_OF_RAMECC_ENABLE_CLR	CPU0_KS_VIM_RAMECC_ENABLE_CLR	B1TCM0_BANK1_ENABLE_CLR	B1TCM0_BANK0_ENABLE_CLR	B0TCM0_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM0_BANK0_ENABLE_CLR	ATCM0_BANK1_ENABLE_CLR	ATCM0_BANK0_ENABLE_CLR	CPU0_DDATA_RAM7_ENABLE_CLR	CPU0_DDATA_RAM6_ENABLE_CLR	CPU0_DDATA_RAM5_ENABLE_CLR	CPU0_DDATA_RAM4_ENABLE_CLR	CPU0_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU0_DDATA_RAM2_ENABLE_CLR	CPU0_DDATA_RAM1_ENABLE_CLR	CPU0_DDATA_RAM0_ENABLE_CLR	CPU0_DDIRTY_RAM_ENABLE_CLR	CPU0_DTAG_RAM3_ENABLE_CLR	CPU0_DTAG_RAM2_ENABLE_CLR	CPU0_DTAG_RAM1_ENABLE_CLR	CPU0_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU0_IDATA_BANK3_ENABLE_CLR	CPU0_IDATA_BANK2_ENABLE_CLR	CPU0_IDATA_BANK1_ENABLE_CLR	CPU0_IDATA_BANK0_ENABLE_CLR	CPU0_ITAG_RAM3_ENABLE_CLR	CPU0_ITAG_RAM2_ENABLE_CLR	CPU0_ITAG_RAM1_ENABLE_CLR	CPU0_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-457. ECC_AGG_CORE0_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU0_RL2_OF_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_rl2_of_ramecc_pend
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank1_pend

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Table 4-457. ECC_AGG_CORE0_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM0_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

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4.1.2.217 ECC_AGG_CORE0_AGGR_ENABLE_SET Register

4.1.2.217.1 ECC_AGG_CORE0_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register.

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Table 4-458. Instance Table

Instance Name	Physical Address
R5SS0	5300 0200h
R5SS1	5300 4200h

Figure 4-217. ECC_AGG_CORE0_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 4-459. ECC_AGG_CORE0_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	Interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	Interrupt enable set for parity errors

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4.1.2.218 ECC_AGG_CORE0_AGGR_ENABLE_CLR Register

4.1.2.218.1 ECC_AGG_CORE0_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register.

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Table 4-460. Instance Table

Instance Name	Physical Address
R5SS0	5300 0204h
R5SS1	5300 4204h

Figure 4-218. ECC_AGG_CORE0_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 4-461. ECC_AGG_CORE0_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	Interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	Interrupt enable clear for parity errors

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4.1.2.219 ECC_AGG_CORE0_AGGR_STATUS_SET Register

4.1.2.219.1 ECC_AGG_CORE0_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register.

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Table 4-462. Instance Table

Instance Name	Physical Address
R5SS0	5300 0208h
R5SS1	5300 4208h

Figure 4-219. ECC_AGG_CORE0_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 4-463. ECC_AGG_CORE0_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	Interrupt status set for svbus timeout errors. 2-bit saturating counter of the number of timeout errors that have occurred since last cleared. 0x0: No timeout errors have occurred 0x1: 1 timeout erro has occurred 0x2: 2 timeout error has occurred 0x3: 3 or more timeout errors have occurred A write of a non-zero value to this register increments that many from the timeout fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. . If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.

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Table 4-463. ECC_AGG_CORE0_AGGR_STATUS_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PARITY	R/WI	0h	Interrupt status set for parity errors. 2-bit saturating counter of the number of parity errors that have occurred since last cleared. 0x0: No parity errors have occurred 0x1: 1 parity error has occurred 0x2: 2 parity error has occurred 0x3 3 or more parity error have occurred A write of a non-zero value to this register incrments that many from the parity fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.

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4.1.2.220 ECC_AGG_CORE0_AGGR_STATUS_CLR Register

4.1.2.220.1 ECC_AGG_CORE0_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register.

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Table 4-464. Instance Table

Instance Name	Physical Address
R5SS0	5300 020Ch
R5SS1	5300 420Ch

Figure 4-220. ECC_AGG_CORE0_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 4-465. ECC_AGG_CORE0_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	Interrupt status clear for svbus timeout errors. 0x0: No timeout errors have occurred 0x1: 1 timeout error has occurred 0x2: 2 timeout error has occurred 0x3: 3 or more timeout error have occurred A write of a non-zero value to this register decrements that many from the timeout fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will not be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.
1:0	PARITY	R/WD	0h	Interrupt status clear for parity errors. 0x0: No parity errors have occurred 0x1: 1 parity error has occurred 0x2: 2 parity error has occurred 0x3: 3 or more parity error have occurred A write of a non-zero value to this register decrements that many from the parity fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will not be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.

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4.1.2.221 ECC_AGG_CORE1_AGGR_REVISION Register

4.1.2.221.1 ECC_AGG_CORE1_AGGR_REVISION Register (Offset = 0h) [reset = 66A0C200h]

Revision parameters.

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Table 4-466. Instance Table

Instance Name	Physical Address
R5SS0	5300 3000h
R5SS1	5300 7000h

Figure 4-221. ECC_AGG_CORE1_AGGR_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
18h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 4-467. ECC_AGG_CORE1_AGGR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	18h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

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4.1.2.222 ECC_AGG_CORE1_ECC_VECTOR Register

4.1.2.222.1 ECC_AGG_CORE1_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register.

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Table 4-468. Instance Table

Instance Name	Physical Address
R5SS0	5300 3008h
R5SS1	5300 7008h

Figure 4-222. ECC_AGG_CORE1_ECC_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 4-469. ECC_AGG_CORE1_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R	0h	Status to indicate if read on serial VBUS is complete
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

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4.1.2.223 ECC_AGG_CORE1_MISC_STATUS Register

4.1.2.223.1 ECC_AGG_CORE1_MISC_STATUS Register (Offset = Ch) [reset = 1Dh]

Misc Status.

Return to Summary Table

Table 4-470. Instance Table

Instance Name	Physical Address
R5SS0	5300 300Ch
R5SS1	5300 700Ch

Figure 4-223. ECC_AGG_CORE1_MISC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1Dh		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1Dh							

Table 4-471. ECC_AGG_CORE1_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1Dh	Indicates the number of RAMS serviced by the ECC aggregator

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4.1.2.224 ECC_AGG_CORE1_ECC_WRAP_REVISION Register

4.1.2.224.1 ECC_AGG_CORE1_ECC_WRAP_REVISION Register (Offset = 10h) [reset = 66A40202h]

Revision parameters.

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Table 4-472. Instance Table

Instance Name	Physical Address
R5SS0	5300 3010h
R5SS1	5300 7010h

Figure 4-224. ECC_AGG_CORE1_ECC_WRAP_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A4h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		2h					

Table 4-473. ECC_AGG_CORE1_ECC_WRAP_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A4h	Module ID
15:11	REVRTL	R	0h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	2h	Minor version

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4.1.2.225 ECC_AGG_CORE1_CONTROL Register

4.1.2.225.1 ECC_AGG_CORE1_CONTROL Register (Offset = 14h) [reset = 187h]

ECC Control Register.

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Table 4-474. Instance Table

Instance Name	Physical Address
R5SS0	5300 3014h
R5SS1	5300 7014h

Figure 4-225. ECC_AGG_CORE1_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							CHECK_SVBUS_TIMEOUT
NONE							R/W
0h							1h
7	6	5	4	3	2	1	0
CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	1h	1h	1h

Table 4-475. ECC_AGG_CORE1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CHECK_SVBUS_TIMEOUT	R/W	1h	check for svbus timeout errors
7	CHECK_PARITY	R/W	1h	check for parity errors
6	ERROR_ONCE	R/W	0h	Force Error only once
5	FORCE_N_ROW	R/W	0h	Force Error on any RAM read
4	FORCE_DED	R/W	0h	Force Double Bit Error
3	FORCE_SEC	R/W	0h	Force Single Bit Error
2	ENABLE_RMW	R/W	1h	Enable rmw
1	ECC_CHECK	R/W	1h	Enable ECC check
0	ECC_ENABLE	R/W	1h	Enable ECC

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4.1.2.226 ECC_AGG_CORE1_ERROR_CTRL1 Register

4.1.2.226.1 ECC_AGG_CORE1_ERROR_CTRL1 Register (Offset = 18h) [reset = 0h]

ECC Error Control1 Register.

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Table 4-476. Instance Table

Instance Name	Physical Address
R5SS0	5300 3018h
R5SS1	5300 7018h

Figure 4-226. ECC_AGG_CORE1_ERROR_CTRL1 Name Register

31	30	29	28	27	26	25	24
ECC_ROW							
R/W							
0h							
23	22	21	20	19	18	17	16
ECC_ROW							
R/W							
0h							
15	14	13	12	11	10	9	8
ECC_ROW							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_ROW							
R/W							
0h							

Table 4-477. ECC_AGG_CORE1_ERROR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R/W	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

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4.1.2.227 ECC_AGG_CORE1_ERROR_CTRL2 Register

4.1.2.227.1 ECC_AGG_CORE1_ERROR_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ECC Error Control2 Register.

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Table 4-478. Instance Table

Instance Name	Physical Address
R5SS0	5300 301Ch
R5SS1	5300 701Ch

Figure 4-227. ECC_AGG_CORE1_ERROR_CTRL2 Name Register

31	30	29	28	27	26	25	24
ECC_BIT2							
R/W							
0h							
23	22	21	20	19	18	17	16
ECC_BIT2							
R/W							
0h							
15	14	13	12	11	10	9	8
ECC_BIT1							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_BIT1							
R/W							
0h							

Table 4-479. ECC_AGG_CORE1_ERROR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT2	R/W	0h	Data bit that needs to be flipped if double bit error needs to be forced
15:0	ECC_BIT1	R/W	0h	Data bit that needs to be flipped when force_sec is set

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4.1.2.228 ECC_AGG_CORE1_ERROR_STATUS1 Register

4.1.2.228.1 ECC_AGG_CORE1_ERROR_STATUS1 Register (Offset = 20h) [reset = 0h]

ECC Error Status1 Register.

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Table 4-480. Instance Table

Instance Name	Physical Address
R5SS0	5300 3020h
R5SS1	5300 7020h

Figure 4-228. ECC_AGG_CORE1_ERROR_STATUS1 Name Register

31	30	29	28	27	26	25	24
ECC_BIT1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ECC_BIT1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLR_CTRL_REG_ERR	CLR_PARITY_ERR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC	
R/W1TC	R/WD		R/W1TC	R/WD		R/WD	
0h	0h		0h	0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTR_REG_ERR	PARITY_ERR		ECC_OTHER	ECC_DED		ECC_SEC	
R/W1TS	R/W1TS		R/W1TS	R/WI		R/WI	
0h	0h		0h	0h		0h	

Table 4-481. ECC_AGG_CORE1_ERROR_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT1	R	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	R/W1TC	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14:13	CLR_PARITY_ERR	R/WD	0h	Clear parity Error Status
12	CLR_ECC_OTHER	R/W1TC	0h	Clear other Error Status
11:10	CLR_ECC_DED	R/WD	0h	Clear Double Bit Error Status
9:8	CLR_ECC_SEC	R/WD	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	R/W1TS	0h	control register error pending, Level interrupt
6:5	PARITY_ERR	R/W1TS	0h	Level parity error Error Status
4	ECC_OTHER	R/W1TS	0h	Successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3:2	ECC_DED	R/WI	0h	Level Double Bit Error Status
1:0	ECC_SEC	R/WI	0h	Level Single Bit Error Status

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4.1.2.229 ECC_AGG_CORE1_ERROR_STATUS2 Register

4.1.2.229.1 ECC_AGG_CORE1_ERROR_STATUS2 Register (Offset = 24h) [reset = 0h]

ECC Error Status2 Register.

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Table 4-482. Instance Table

Instance Name	Physical Address
R5SS0	5300 3024h
R5SS1	5300 7024h

Figure 4-229. ECC_AGG_CORE1_ERROR_STATUS2 Name Register

31	30	29	28	27	26	25	24
ECC_ROW							
R							
0h							
23	22	21	20	19	18	17	16
ECC_ROW							
R							
0h							
15	14	13	12	11	10	9	8
ECC_ROW							
R							
0h							
7	6	5	4	3	2	1	0
ECC_ROW							
R							
0h							

Table 4-483. ECC_AGG_CORE1_ERROR_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R	0h	Row address where the single or double-bit error has occurred

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4.1.2.230 ECC_AGG_CORE1_ERROR_STATUS3 Register

4.1.2.230.1 ECC_AGG_CORE1_ERROR_STATUS3 Register (Offset = 28h) [reset = 0h]

ECC Error Status3 Register.

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Table 4-484. Instance Table

Instance Name	Physical Address
R5SS0	5300 3028h
R5SS1	5300 7028h

Figure 4-230. ECC_AGG_CORE1_ERROR_STATUS3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						CLR_SVBUS_TIMEOUT_ERR	RESERVED
NONE						R/W1TC	NONE
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						SVBUS_TIMEOUT_ERR	WB_PEND
NONE						R/W1TS	R
0h						0h	0h

Table 4-485. ECC_AGG_CORE1_ERROR_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CLR_SVBUS_TIMEOUT_ERR	R/W1TC	0h	Clear svbus timeout Error Status
8:2	RESERVED	NONE	0h	Reserved
1	SVBUS_TIMEOUT_ERR	R/W1TS	0h	Level svbus timeout error Error Status
0	WB_PEND	R	0h	delayed write back pending Status

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4.1.2.231 ECC_AGG_CORE1_SEC_EOI_REG Register

4.1.2.231.1 ECC_AGG_CORE1_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

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Table 4-486. Instance Table

Instance Name	Physical Address
R5SS0	5300 303Ch
R5SS1	5300 703Ch

Figure 4-231. ECC_AGG_CORE1_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 4-487. ECC_AGG_CORE1_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register Write of 1 to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. The bit is self clearing and will be read as a zero.

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4.1.2.232 ECC_AGG_CORE1_SEC_STATUS_REG0 Register

4.1.2.232.1 ECC_AGG_CORE1_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 4-488. Instance Table

Instance Name	Physical Address
R5SS0	5300 3040h
R5SS1	5300 7040h

Figure 4-232. ECC_AGG_CORE1_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU1_RL2_OF_RAMECC_PEND	CPU1_KS_VIM_RAMECC_PEND	B1TCM1_BANK1_PEND	B1TCM1_BANK0_PEND	B0TCM1_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
B0TCM1_BANK0_PEND	ATCM1_BANK1_PEND	ATCM1_BANK0_PEND	CPU1_DDATA_RAM7_PEND	CPU1_DDATA_RAM6_PEND	CPU1_DDATA_RAM5_PEND	CPU1_DDATA_RAM4_PEND	CPU1_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
CPU1_DDATA_RAM2_PEND	CPU1_DDATA_RAM1_PEND	CPU1_DDATA_RAM0_PEND	CPU1_DDIRTY_RAM_PEND	CPU1_DTAG_RAM3_PEND	CPU1_DTAG_RAM2_PEND	CPU1_DTAG_RAM1_PEND	CPU1_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
CPU1_IDATA_BANK3_PEND	CPU1_IDATA_BANK2_PEND	CPU1_IDATA_BANK1_PEND	CPU1_IDATA_BANK0_PEND	CPU1_ITAG_RAM3_PEND	CPU1_ITAG_RAM2_PEND	CPU1_ITAG_RAM1_PEND	CPU1_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-489. ECC_AGG_CORE1_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU1_RL2_OF_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_rl2_of_ramecc_pend
27	CPU1_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm1_bank1_pend
25	B1TCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm1_bank0_pend
24	B0TCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm1_bank1_pend
23	B0TCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm1_bank0_pend
22	ATCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm1_bank1_pend
21	ATCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram5_pend

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Table 4-489. ECC_AGG_CORE1_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU1_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram0_pend

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4.1.2.233 ECC_AGG_CORE1_SEC_ENABLE_SET_REG0 Register

4.1.2.233.1 ECC_AGG_CORE1_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 4-490. Instance Table

Instance Name	Physical Address
R5SS0	5300 3080h
R5SS1	5300 7080h

Figure 4-233. ECC_AGG_CORE1_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU1_RL2_OF_RAMECC_ENABLE_SET	CPU1_KS_VIM_RAMECC_ENABLE_SET	B1TCM1_BANK1_ENABLE_SET	B1TCM1_BANK0_ENABLE_SET	B0TCM1_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM1_BANK0_ENABLE_SET	ATCM1_BANK1_ENABLE_SET	ATCM1_BANK0_ENABLE_SET	CPU1_DDATA_RAM7_ENABLE_SET	CPU1_DDATA_RAM6_ENABLE_SET	CPU1_DDATA_RAM5_ENABLE_SET	CPU1_DDATA_RAM4_ENABLE_SET	CPU1_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU1_DDATA_RAM2_ENABLE_SET	CPU1_DDATA_RAM1_ENABLE_SET	CPU1_DDATA_RAM0_ENABLE_SET	CPU1_DDIRTY_RAM_ENABLE_SET	CPU1_DTAG_RAM3_ENABLE_SET	CPU1_DTAG_RAM2_ENABLE_SET	CPU1_DTAG_RAM1_ENABLE_SET	CPU1_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU1_IDATA_BANK3_ENABLE_SET	CPU1_IDATA_BANK2_ENABLE_SET	CPU1_IDATA_BANK1_ENABLE_SET	CPU1_IDATA_BANK0_ENABLE_SET	CPU1_ITAG_RAM3_ENABLE_SET	CPU1_ITAG_RAM2_ENABLE_SET	CPU1_ITAG_RAM1_ENABLE_SET	CPU1_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-491. ECC_AGG_CORE1_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU1_RL2_OF_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_rl2_of_ramecc_pend
27	CPU1_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm1_bank1_pend

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Table 4-491. ECC_AGG_CORE1_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram0_pend

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4.1.2.234 ECC_AGG_CORE1_SEC_ENABLE_CLR_REG0 Register

4.1.2.234.1 ECC_AGG_CORE1_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 4-492. Instance Table

Instance Name	Physical Address
R5SS0	5300 30C0h
R5SS1	5300 70C0h

Figure 4-234. ECC_AGG_CORE1_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU1_RL2_OF_RAMECC_ENABLE_CLR	CPU1_KS_VIM_RAMECC_ENABLE_CLR	B1TCM1_BANK1_ENABLE_CLR	B1TCM1_BANK0_ENABLE_CLR	B0TCM1_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM1_BANK0_ENABLE_CLR	ATCM1_BANK1_ENABLE_CLR	ATCM1_BANK0_ENABLE_CLR	CPU1_DDATA_RAM7_ENABLE_CLR	CPU1_DDATA_RAM6_ENABLE_CLR	CPU1_DDATA_RAM5_ENABLE_CLR	CPU1_DDATA_RAM4_ENABLE_CLR	CPU1_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU1_DDATA_RAM2_ENABLE_CLR	CPU1_DDATA_RAM1_ENABLE_CLR	CPU1_DDATA_RAM0_ENABLE_CLR	CPU1_DDIRTY_RAM_ENABLE_CLR	CPU1_DTAG_RAM3_ENABLE_CLR	CPU1_DTAG_RAM2_ENABLE_CLR	CPU1_DTAG_RAM1_ENABLE_CLR	CPU1_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU1_IDATA_BANK3_ENABLE_CLR	CPU1_IDATA_BANK2_ENABLE_CLR	CPU1_IDATA_BANK1_ENABLE_CLR	CPU1_IDATA_BANK0_ENABLE_CLR	CPU1_ITAG_RAM3_ENABLE_CLR	CPU1_ITAG_RAM2_ENABLE_CLR	CPU1_ITAG_RAM1_ENABLE_CLR	CPU1_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-493. ECC_AGG_CORE1_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU1_RL2_OF_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_rl2_of_ramecc_pend
27	CPU1_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm1_bank1_pend

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Table 4-493. ECC_AGG_CORE1_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram0_pend

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4.1.2.235 ECC_AGG_CORE1_DED_EOI_REG Register

4.1.2.235.1 ECC_AGG_CORE1_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

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Table 4-494. Instance Table

Instance Name	Physical Address
R5SS0	5300 313Ch
R5SS1	5300 713Ch

Figure 4-235. ECC_AGG_CORE1_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 4-495. ECC_AGG_CORE1_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register Write of 1 to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. The bit is self clearing and will be read as a zero.

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4.1.2.236 ECC_AGG_CORE1_DED_STATUS_REG0 Register

4.1.2.236.1 ECC_AGG_CORE1_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 4-496. Instance Table

Instance Name	Physical Address
R5SS0	5300 3140h
R5SS1	5300 7140h

Figure 4-236. ECC_AGG_CORE1_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU1_RL2_OF_RAMECC_PEND	CPU1_KS_VIM_RAMECC_PEND	B1TCM1_BANK1_PEND	B1TCM1_BANK0_PEND	B0TCM1_BANK1_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM1_BANK0_PEND	ATCM1_BANK1_PEND	ATCM1_BANK0_PEND	CPU1_DDATA_RAM7_PEND	CPU1_DDATA_RAM6_PEND	CPU1_DDATA_RAM5_PEND	CPU1_DDATA_RAM4_PEND	CPU1_DDATA_RAM3_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU1_DDATA_RAM2_PEND	CPU1_DDATA_RAM1_PEND	CPU1_DDATA_RAM0_PEND	CPU1_DDIRTY_RAM_PEND	CPU1_DTAG_RAM3_PEND	CPU1_DTAG_RAM2_PEND	CPU1_DTAG_RAM1_PEND	CPU1_DTAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU1_IDATA_BANK3_PEND	CPU1_IDATA_BANK2_PEND	CPU1_IDATA_BANK1_PEND	CPU1_IDATA_BANK0_PEND	CPU1_ITAG_RAM3_PEND	CPU1_ITAG_RAM2_PEND	CPU1_ITAG_RAM1_PEND	CPU1_ITAG_RAM0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-497. ECC_AGG_CORE1_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU1_RL2_OF_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_rl2_of_ramecc_pend
27	CPU1_KS_VIM_RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm1_bank1_pend
25	B1TCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b1tcm1_bank0_pend
24	B0TCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm1_bank1_pend
23	B0TCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for b0tcm1_bank0_pend
22	ATCM1_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for atcm1_bank1_pend
21	ATCM1_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram5_pend

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Table 4-497. ECC_AGG_CORE1_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CPU1_DDATA_RAM4_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_PEND	R/W1TS	0h	Interrupt Pending Status for cpu1_itag_ram0_pend

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4.1.2.237 ECC_AGG_CORE1_DED_ENABLE_SET_REG0 Register

4.1.2.237.1 ECC_AGG_CORE1_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 4-498. Instance Table

Instance Name	Physical Address
R5SS0	5300 3180h
R5SS1	5300 7180h

Figure 4-237. ECC_AGG_CORE1_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU1_RL2_OF_RAMECC_ENABLE_SET	CPU1_KS_VIM_RAMECC_ENABLE_SET	B1TCM1_BANK1_ENABLE_SET	B1TCM1_BANK0_ENABLE_SET	B0TCM1_BANK1_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM1_BANK0_ENABLE_SET	ATCM1_BANK1_ENABLE_SET	ATCM1_BANK0_ENABLE_SET	CPU1_DDATA_RAM7_ENABLE_SET	CPU1_DDATA_RAM6_ENABLE_SET	CPU1_DDATA_RAM5_ENABLE_SET	CPU1_DDATA_RAM4_ENABLE_SET	CPU1_DDATA_RAM3_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU1_DDATA_RAM2_ENABLE_SET	CPU1_DDATA_RAM1_ENABLE_SET	CPU1_DDATA_RAM0_ENABLE_SET	CPU1_DDIRTY_RAM_ENABLE_SET	CPU1_DTAG_RAM3_ENABLE_SET	CPU1_DTAG_RAM2_ENABLE_SET	CPU1_DTAG_RAM1_ENABLE_SET	CPU1_DTAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU1_IDATA_BANK3_ENABLE_SET	CPU1_IDATA_BANK2_ENABLE_SET	CPU1_IDATA_BANK1_ENABLE_SET	CPU1_IDATA_BANK0_ENABLE_SET	CPU1_ITAG_RAM3_ENABLE_SET	CPU1_ITAG_RAM2_ENABLE_SET	CPU1_ITAG_RAM1_ENABLE_SET	CPU1_ITAG_RAM0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-499. ECC_AGG_CORE1_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU1_RL2_OF_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_rl2_of_ramecc_pend
27	CPU1_KS_VIM_RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm1_bank1_pend

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Table 4-499. ECC_AGG_CORE1_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM1_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for cpu1_itag_ram0_pend

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4.1.2.238 ECC_AGG_CORE1_DED_ENABLE_CLR_REG0 Register

4.1.2.238.1 ECC_AGG_CORE1_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 4-500. Instance Table

Instance Name	Physical Address
R5SS0	5300 31C0h
R5SS1	5300 71C0h

Figure 4-238. ECC_AGG_CORE1_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED			CPU1_RL2_OF_RAMECC_ENABLE_CLR	CPU1_KS_VIM_RAMECC_ENABLE_CLR	B1TCM1_BANK1_ENABLE_CLR	B1TCM1_BANK0_ENABLE_CLR	B0TCM1_BANK1_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
B0TCM1_BANK0_ENABLE_CLR	ATCM1_BANK1_ENABLE_CLR	ATCM1_BANK0_ENABLE_CLR	CPU1_DDATA_RAM7_ENABLE_CLR	CPU1_DDATA_RAM6_ENABLE_CLR	CPU1_DDATA_RAM5_ENABLE_CLR	CPU1_DDATA_RAM4_ENABLE_CLR	CPU1_DDATA_RAM3_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CPU1_DDATA_RAM2_ENABLE_CLR	CPU1_DDATA_RAM1_ENABLE_CLR	CPU1_DDATA_RAM0_ENABLE_CLR	CPU1_DDIRTY_RAM_ENABLE_CLR	CPU1_DTAG_RAM3_ENABLE_CLR	CPU1_DTAG_RAM2_ENABLE_CLR	CPU1_DTAG_RAM1_ENABLE_CLR	CPU1_DTAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CPU1_IDATA_BANK3_ENABLE_CLR	CPU1_IDATA_BANK2_ENABLE_CLR	CPU1_IDATA_BANK1_ENABLE_CLR	CPU1_IDATA_BANK0_ENABLE_CLR	CPU1_ITAG_RAM3_ENABLE_CLR	CPU1_ITAG_RAM2_ENABLE_CLR	CPU1_ITAG_RAM1_ENABLE_CLR	CPU1_ITAG_RAM0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-501. ECC_AGG_CORE1_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28	CPU1_RL2_OF_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_rl2_of_ramecc_pend
27	CPU1_KS_VIM_RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm1_bank1_pend

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Table 4-501. ECC_AGG_CORE1_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	ATCM1_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for cpu1_itag_ram0_pend

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4.1.2.239 ECC_AGG_CORE1_AGGR_ENABLE_SET Register

4.1.2.239.1 ECC_AGG_CORE1_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register.

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Table 4-502. Instance Table

Instance Name	Physical Address
R5SS0	5300 3200h
R5SS1	5300 7200h

Figure 4-239. ECC_AGG_CORE1_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 4-503. ECC_AGG_CORE1_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	Interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	Interrupt enable set for parity errors

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4.1.2.240 ECC_AGG_CORE1_AGGR_ENABLE_CLR Register

4.1.2.240.1 ECC_AGG_CORE1_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register.

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Table 4-504. Instance Table

Instance Name	Physical Address
R5SS0	5300 3204h
R5SS1	5300 7204h

Figure 4-240. ECC_AGG_CORE1_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 4-505. ECC_AGG_CORE1_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	Interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	Interrupt enable clear for parity errors

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4.1.2.241 ECC_AGG_CORE1_AGGR_STATUS_SET Register

4.1.2.241.1 ECC_AGG_CORE1_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register.

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Table 4-506. Instance Table

Instance Name	Physical Address
R5SS0	5300 3208h
R5SS1	5300 7208h

Figure 4-241. ECC_AGG_CORE1_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 4-507. ECC_AGG_CORE1_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	Interrupt status set for svbus timeout errors. 2-bit saturating counter of the number of timeout errors that have occurred since last cleared. 0x0: No timeout errors have occurred 0x1: 1 timeout erro has occurred 0x2: 2 timeout error has occurred 0x3: 3 or more timeout errors have occurred A write of a non-zero value to this register increments that many from the timeout fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. . If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.

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Table 4-507. ECC_AGG_CORE1_AGGR_STATUS_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PARITY	R/WI	0h	Interrupt status set for parity errors. 2-bit saturating counter of the number of parity errors that have occurred since last cleared. 0x0: No parity errors have occurred 0x1: 1 parity error has occurred 0x2: 2 parity error has occurred 0x3 3 or more parity error have occurred A write of a non-zero value to this register incrments that many from the parity fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.

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4.1.2.242 ECC_AGG_CORE1_AGGR_STATUS_CLR Register

4.1.2.242.1 ECC_AGG_CORE1_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register.

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Table 4-508. Instance Table

Instance Name	Physical Address
R5SS0	5300 320Ch
R5SS1	5300 720Ch

Figure 4-242. ECC_AGG_CORE1_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 4-509. ECC_AGG_CORE1_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	Interrupt status clear for svbus timeout errors. 0x0: No timeout errors have occurred 0x1: 1 timeout error has occurred 0x2: 2 timeout error has occurred 0x3: 3 or more timeout error have occurred A write of a non-zero value to this register decrements that many from the timeout fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will not be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.
1:0	PARITY	R/WD	0h	Interrupt status clear for parity errors. 0x0: No parity errors have occurred 0x1: 1 parity error has occurred 0x2: 2 parity error has occurred 0x3: 3 or more parity error have occurred A write of a non-zero value to this register decrements that many from the parity fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will not be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.

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4.1.2.243 TMU_ROM_CORE0_START Register

4.1.2.243.1 TMU_ROM_CORE0_START Register (Offset = 0h) [reset = 0h]

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Table 4-510. Instance Table

Instance Name	Physical Address
R5SS0	5302 0000h
R5SS1	5302 8000h

Figure 4-243. TMU_ROM_CORE0_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-511. TMU_ROM_CORE0_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TMU ROM start address

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4.1.2.244 TMU_ROM_CORE0_END Register

4.1.2.244.1 TMU_ROM_CORE0_END Register (Offset = 2FFCh) [reset = 0h]

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Table 4-512. Instance Table

Instance Name	Physical Address
R5SS0	5302 2FFCh
R5SS1	5302 AFFCh

Figure 4-244. TMU_ROM_CORE0_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-513. TMU_ROM_CORE0_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TMU ROM end address

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4.1.2.245 TMU_ROM_CORE1_START Register

4.1.2.245.1 TMU_ROM_CORE1_START Register (Offset = 0h) [reset = 0h]

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Table 4-514. Instance Table

Instance Name	Physical Address
R5SS0	5302 4000h
R5SS1	5302 C000h

Figure 4-245. TMU_ROM_CORE1_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-515. TMU_ROM_CORE1_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TMU ROM start address

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4.1.2.246 TMU_ROM_CORE1_END Register

4.1.2.246.1 TMU_ROM_CORE1_END Register (Offset = 2FFCh) [reset = 0h]

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Table 4-516. Instance Table

Instance Name	Physical Address
R5SS0	5302 6FFCh
R5SS1	5302 EFFCh

Figure 4-246. TMU_ROM_CORE1_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-517. TMU_ROM_CORE1_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TMU ROM end address

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4.1.2.247 CCMR_CCMSR1 Register

4.1.2.247.1 CCMR_CCMSR1 Register (Offset = 0h) [reset = 0h]

CPU Compare Status Register.

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Table 4-518. Instance Table

Instance Name	Physical Address
R5SS0	5321 0000h
R5SS1	5321 1000h

Figure 4-247. CCMR_CCMSR1 Name Register

31	30	29	28	27	26	25	24
NU2							
NU2							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU2							CMPE1
NU2							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU1							STC1
NU1							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU0						STET1	STE1
R/W						R/W	R
0h						0h	0h

Table 4-519. CCMR_CCMSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	NU2	NU2	0h	Reserved
16	CMPE1	R/W	0h	Compare Error 0 = CPU signals are identical 1= CPU signal compare mismatch Writes '1' to clear this bit
15:9	NU1	NU1	0h	Reserved
8	STC1	R/W	0h	Self Test Complete 0 = self test on-going if self test mode asserted 1 = self test is complete Writes have no effect
7:2	NU0	R/W	0h	Reserved
1	STET1	R/W	0h	Self Test Error Type 0 = self test failed during Compare Match test 1 = self test failed during Compare mismatch test Writes have no effect
0	STE1	R	0h	Self Test Error 0 = self test passed 1 = self test failed Writes have no effect

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4.1.2.248 CCMR_CCMKEYR1 Register

4.1.2.248.1 CCMR_CCMKEYR1 Register (Offset = 4h) [reset = 0h]

CPU Compare Key Register.

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Table 4-520. Instance Table

Instance Name	Physical Address
R5SS0	5321 0004h
R5SS1	5321 1004h

Figure 4-248. CCMR_CCMKEYR1 Name Register

31	30	29	28	27	26	25	24
NU3							
R/W							
0h							
23	22	21	20	19	18	17	16
NU3							
R/W							
0h							
15	14	13	12	11	10	9	8
NU3							
R/W							
0h							
7	6	5	4	3	2	1	0
NU3				MKEY1			
R/W				R/W			
0h				0h			

Table 4-521. CCMR_CCMKEYR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU3	R/W	0h	Reserved
3:0	MKEY1	R/W	0h	Mode Key 0000= lock step mode 0110= self test mode 1001= error forcing mode 1111= self test error forcing mode

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4.1.2.249 CCMR_CCMSR2 Register

4.1.2.249.1 CCMR_CCMSR2 Register (Offset = 8h) [reset = 0h]

VIM Compare Status Register.

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Table 4-522. Instance Table

Instance Name	Physical Address
R5SS0	5321 0008h
R5SS1	5321 1008h

Figure 4-249. CCMR_CCMSR2 Name Register

31	30	29	28	27	26	25	24
NU6							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU6							CMPE2
R/W							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU5							STC2
R/W							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU4						STET2	STE2
R/W						R/W	R/W
0h						0h	0h

Table 4-523. CCMR_CCMSR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	NU6	R/W	0h	Reserved
16	CMPE2	R/W	0h	Compare Error 0 = VIM signals are identical 1= VIM signal compare mismatch Writes '1' to clear this bit
15:9	NU5	R/W	0h	Reserved
8	STC2	R/W	0h	Self Test Complete 0 = self test on-going if self test mode asserted 1 = self test is complete Writes have no effect
7:2	NU4	R/W	0h	Reserved
1	STET2	R/W	0h	Self Test Error Type 0 = self test failed during Compare Match test 1 = self test failed during Compare mismatch test Writes have no effect
0	STE2	R/W	0h	Self Test Error 0 = self test passed 1 = self test failed Writes have no effect

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4.1.2.250 CCMR_CCMKEYR2 Register

4.1.2.250.1 CCMR_CCMKEYR2 Register (Offset = Ch) [reset = 0h]

VIM Compare Key Register.

Return to Summary Table

Table 4-524. Instance Table

Instance Name	Physical Address
R5SS0	5321 000Ch
R5SS1	5321 100Ch

Figure 4-250. CCMR_CCMKEYR2 Name Register

31	30	29	28	27	26	25	24
NU7							
R/W							
0h							
23	22	21	20	19	18	17	16
NU7							
R/W							
0h							
15	14	13	12	11	10	9	8
NU7							
R/W							
0h							
7	6	5	4	3	2	1	0
NU7				MKEY2			
R/W				R/W			
0h				0h			

Table 4-525. CCMR_CCMKEYR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU7	R/W	0h	Reserved
3:0	MKEY2	R/W	0h	Mode Key 0000= lock step mode 0110= self test mode 1001= error forcing mode 1111= self test error forcing mode

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4.1.2.251 CCMR_CCMSR3 Register

4.1.2.251.1 CCMR_CCMSR3 Register (Offset = 10h) [reset = 0h]

Inactivity Monitor Status Register.

Return to Summary Table

Table 4-526. Instance Table

Instance Name	Physical Address
R5SS0	5321 0010h
R5SS1	5321 1010h

Figure 4-251. CCMR_CCMSR3 Name Register

31	30	29	28	27	26	25	24
NU10							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU10							CMPE3
R/W							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU9							STC3
R/W							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU8						STET3	STE3
R/W						R/W	R
0h						0h	0h

Table 4-527. CCMR_CCMSR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	NU10	R/W	0h	Reserved
16	CMPE3	R/W	0h	Compare Error 0 = Inactivity monitor signals are identical 1= Inactivity monitor signal compare mismatch Writes '1' to clear this bit
15:9	NU9	R/W	0h	Reserved
8	STC3	R/W	0h	Self Test Complete 0 = self test on-going if self test mode asserted 1 = self test is complete Writes have no effect
7:2	NU8	R/W	0h	Reserved
1	STET3	R/W	0h	Self Test Error Type 0 = self test failed during Compare Match test 1 = self test failed during Compare mismatch test Writes have no effect
0	STE3	R	0h	Self Test Error 0 = self test passed 1 = self test failed Writes have no effect

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4.1.2.252 CCMR_CCMKEYR3 Register

4.1.2.252.1 CCMR_CCMKEYR3 Register (Offset = 14h) [reset = 0h]

Inactivity Monitor Key Register.

Return to Summary Table

Table 4-528. Instance Table

Instance Name	Physical Address
R5SS0	5321 0014h
R5SS1	5321 1014h

Figure 4-252. CCMR_CCMKEYR3 Name Register

31	30	29	28	27	26	25	24
NU11							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU11							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU11							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU11				MKEY3			
R/W				R/W			
0h				0h			

Table 4-529. CCMR_CCMKEYR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU11	R/W	0h	Reserved
3:0	MKEY3	R/W	0h	Mode Key 0000= lock step mode 0110= self test mode 1001= error forcing mode 1111= self test error forcing mode

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4.1.2.253 CCMR_CCMPOLCNTRL Register

4.1.2.253.1 CCMR_CCMPOLCNTRL Register (Offset = 18h) [reset = 0h]

CPU Compare Polarity Control Register.

Return to Summary Table

Table 4-530. Instance Table

Instance Name	Physical Address
R5SS0	5321 0018h
R5SS1	5321 1018h

Figure 4-253. CCMR_CCMPOLCNTRL Name Register

31	30	29	28	27	26	25	24
NU12							
R/W							
0h							
23	22	21	20	19	18	17	16
NU12							
R/W							
0h							
15	14	13	12	11	10	9	8
NU12							
R/W							
0h							
7	6	5	4	3	2	1	0
POL_INV							
R							
0h							

Table 4-531. CCMR_CCMPOLCNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	NU12	R/W	0h	Reserved
7:0	POL_INV	R	0h	This value is used to invert the 8 XOR of the CPU1 to create compare fail in functional active compare mode. User and privilege mode read = Returns current value of the POL INV Privilege mode write = Update the values of POL INV

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4.1.2.254 CCMR_CCMSR5 Register

4.1.2.254.1 CCMR_CCMSR5 Register (Offset = 2Ch) [reset = 0h]

TMU Compare Status Register.

Return to Summary Table

Table 4-532. Instance Table

Instance Name	Physical Address
R5SS0	5321 002Ch
R5SS1	5321 102Ch

Figure 4-254. CCMR_CCMSR5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">NU15</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="7">NU15</td><td>CMPE5</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">NU14</td><td>STC5</td></tr>
<tr><td colspan="7">R/W</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">NU13</td><td>STET5</td><td>STE5</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 4-533. CCMR_CCMSR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	NU15	R/W	0h	Reserved
16	CMPE5	R/W	0h	Compare Error 0 = Inactivity monitor signals are identical 1= Inactivity monitor signal compare mismatch Writes '1' to clear this bit
15:9	NU14	R/W	0h	Reserved
8	STC5	R/W	0h	Self Test Complete 0 = self test on-going if self test mode asserted 1 = self test is complete Writes have no effect
7:2	NU13	R/W	0h	Reserved
1	STET5	R/W	0h	Self Test Error Type 0 = self test failed during Compare Match test 1 = self test failed during Compare mismatch test Writes have no effect
0	STE5	R	0h	Self Test Error 0 = self test passed 1 = self test failed Writes have no effect

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4.1.2.255 CCMR_CCMKEYR5 Register

4.1.2.255.1 CCMR_CCMKEYR5 Register (Offset = 30h) [reset = 0h]

TMU Compare Key Register.

Return to Summary Table

Table 4-534. Instance Table

Instance Name	Physical Address
R5SS0	5321 0030h
R5SS1	5321 1030h

Figure 4-255. CCMR_CCMKEYR5 Name Register

31	30	29	28	27	26	25	24
NU16							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU16							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU16							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU16				MKEY5			
R/W				R/W			
0h				0h			

Table 4-535. CCMR_CCMKEYR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU16	R/W	0h	Reserved
3:0	MKEY5	R/W	0h	Mode Key 0000= lock step mode 0110= self test mode 1001= error forcing mode 1111= self test error forcing mode

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4.1.2.256 CCMR_CCMSR6 Register

4.1.2.256.1 CCMR_CCMSR6 Register (Offset = 34h) [reset = 0h]

RL2 Compare Status Register.

Return to Summary Table

Table 4-536. Instance Table

Instance Name	Physical Address
R5SS0	5321 0034h
R5SS1	5321 1034h

Figure 4-256. CCMR_CCMSR6 Name Register

31	30	29	28	27	26	25	24
NU19							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU19							CMPE6
R/W							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU18							STC6
R/W							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU17						STET6	STE6
R/W						R/W	R
0h						0h	0h

Table 4-537. CCMR_CCMSR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	NU19	R/W	0h	Reserved
16	CMPE6	R/W	0h	Compare Error 0 = Inactivity monitor signals are identical 1= Inactivity monitor signal compare mismatch Writes '1' to clear this bit
15:9	NU18	R/W	0h	Reserved
8	STC6	R/W	0h	Self Test Complete 0 = self test on-going if self test mode asserted 1 = self test is complete Writes have no effect
7:2	NU17	R/W	0h	Reserved
1	STET6	R/W	0h	Self Test Error Type 0 = self test failed during Compare Match test 1 = self test failed during Compare mismatch test Writes have no effect
0	STE6	R	0h	Self Test Error 0 = self test passed 1 = self test failed Writes have no effect

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4.1.2.257 CCMR_CCMKEYR6 Register

4.1.2.257.1 CCMR_CCMKEYR6 Register (Offset = 38h) [reset = 0h]

RL2 Compare Key Register.

Return to Summary Table

Table 4-538. Instance Table

Instance Name	Physical Address
R5SS0	5321 0038h
R5SS1	5321 1038h

Figure 4-257. CCMR_CCMKEYR6 Name Register

31	30	29	28	27	26	25	24
NU20							
R/W							
0h							
23	22	21	20	19	18	17	16
NU20							
R/W							
0h							
15	14	13	12	11	10	9	8
NU20							
R/W							
0h							
7	6	5	4	3	2	1	0
NU20				MKEY6			
R/W				R/W			
0h				0h			

Table 4-539. CCMR_CCMKEYR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU20	R/W	0h	Reserved
3:0	MKEY6	R/W	0h	Mode Key 0000= lock step mode 0110= self test mode 1001= error forcing mode 1111= self test error forcing mode

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4.1.2.258 STC_STCGCR0 Register

4.1.2.258.1 STC_STCGCR0 Register (Offset = 0h) [reset = 10120h]

Self test Global control Reg0. *NOT BYTE ACCESSIBLE.

Return to Summary Table

Table 4-540. Instance Table

Instance Name	Physical Address
R5SS0	5350 0000h
R5SS1	5351 0000h

Figure 4-258. STC_STCGCR0 Name Register

31	30	29	28	27	26	25	24
INTCOUNT_B16							
R/W							
1h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INTCOUNT_B16							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU0					CAP_IDLE_CYCLE		
R					R/W		
0h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SCANEN_HIGH_CAP_IDLE_CYCLE			NU1			RS_CNT_B1	
R/W			NU1			R/W	
1h			0h			0h	

Table 4-541. STC_STCGCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	INTCOUNT_B16	R/W	1h	Number of intervals of the self test run [RWP - Read, Priviledge Mode Write only] Count of intervals that need to be covered for a specific selftest run. The selftest controller sends out complete indication once it runs all of the intervals programmed in this field. INTCOUNT_B16=0 is an invalid configuration for a selftest.
15:11	NU0	R	0h	Reserved bits
10:8	CAP_IDLE_CYCLE	R/W	1h	Idle cycles before and after capture clock [RWP - Read, Priviledge Mode Write only] Idle Cycles before and after capture clock. This value is used to insert that many idle cycles in the Capture phase. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements.
7:5	SCANEN_HIGH_CAP_IDLE_CYCLE	R/W	1h	Idle cycles before and after capture clock [RWP - Read, Priviledge Mode Write only]. *NOT BYTE ACCESSIBLE Idle Cycles between scan_en going high to func_clk_en generation and scan_en going high to misr_log_en generation. This value is used to insert that many idle cycles in the shift clock [scan_en going high to func_clk_en generation] and misr_log_clk [scan_en going high to misr_log_en generation] generation. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements.
4:2	NU1	NU1	0h	Reserved bits

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Table 4-541. STC_STCGCR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RS_CNT_B1	R/W	0h	Restart/Continue or preload [RWP - Read, Priviledge Mode Write only] This bit specifies the selftest controller whether to continue the run from next interval onwards, restart from ROM address 0 or preload from a prescribed interval. This bit gets reset after the completion of selftest run. 00 = Continue NSTC run from previous interval 01 = Restart NSTC run from ROM address 0 1X = Start from segment number specified in STC_SEGPLR register

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4.1.2.259 STC_STCGCR1 Register

4.1.2.259.1 STC_STCGCR1 Register (Offset = 4h) [reset = 25h]

Self test Global control Reg1.

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Table 4-542. Instance Table

Instance Name	Physical Address
R5SS0	5350 0004h
R5SS1	5351 0004h

Figure 4-259. STC_STCGCR1 Name Register

31	30	29	28	27	26	25	24
NU2							
NU2							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU2							
NU2							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU2				SEG0_CORE_SEL			
NU2				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU3	CODEC_SPREAD_MODE	LP_SCAN_MODE	ROM_ACCESS_INV	ST_ENA_B4			
R	R/W	R/W	R/W	R/W			
0h	0h	1h	0h	5h			

Table 4-543. STC_STCGCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	NU2	NU2	0h	Reserved bits
11:8	SEG0_CORE_SEL	R/W	0h	Selects the Segment0 CORE for self test [RWP - Read, Priviledge Mode Write only] Select the Segment0 CORE for Self -Test 0001= Select CORE for selftest Other = CORE not selected.
7	NU3	R	0h	Reserved bits
6	CODEC_SPREAD_MODE	R/W	0h	Codec Spread Mode control signal [RWP - Read, Priviledge Mode Write only] This bit is used to configure the codec in spread / X-OR mode. 1 = Spread mode 0 = XOR mode
5	LP_SCAN_MODE	R/W	1h	LP scan mode [RWP - Read, Priviledge Mode Write only] This bit is used to decide the scan configuration: 1 = Operates in Low Power Scan Mode. 0 = Operates in Normal Scan Mode.
4	ROM_ACCESS_INV	R/W	0h	Rom access inversion mode [RWP - Read, Priviledge Mode Write only] - NOT SUPPORTED

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Table 4-543. STC_STCGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	ST_ENA_B4	R/W	5h	Self test enable key [RWP - Read, Priviledge Mode Write only] 1010= Self test run enabled All values other than 1010= Self test run disabled

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4.1.2.260 STC_STCTPR Register

4.1.2.260.1 STC_STCTPR Register (Offset = 8h) [reset = FFFFFFFFh]

Time out counter preload register.

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Table 4-544. Instance Table

Instance Name	Physical Address
R5SS0	5350 0008h
R5SS1	5351 0008h

Figure 4-260. STC_STCTPR Name Register

31	30	29	28	27	26	25	24
TO_PRELOAD							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
TO_PRELOAD							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
TO_PRELOAD							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
TO_PRELOAD							
R/W							
FFFFFFFFh							

Table 4-545. STC_STCTPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TO_PRELOAD	R/W	FFFFFFFFh	Self test time out preload [RWP - Read, Priviledge Mode Write only] This register contains the total number of STC clock cycles it will take before a self-test timeout error will be triggered after the initiation of the self-test run. This is a fail safe feature to avoid system hang-up situation on account of any run away self test issues. This register should be loaded with a meaningful count value for this feature to be effective. This register value [preload count value] gets loaded into the self test timeout down counter whenever a self test run is initiated [ST_ENA is enabled]. and gets disabled on completion of a self test run.

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4.1.2.261 STC_STC_CADDR Register

4.1.2.261.1 STC_STC_CADDR Register (Offset = Ch) [reset = 0h]

Current Address register for CORE1.

Return to Summary Table

Table 4-546. Instance Table

Instance Name	Physical Address
R5SS0	5350 000Ch
R5SS1	5351 000Ch

Figure 4-261. STC_STC_CADDR Name Register

31	30	29	28	27	26	25	24
ADDR							
R							
0h							
23	22	21	20	19	18	17	16
ADDR							
R							
0h							
15	14	13	12	11	10	9	8
ADDR							
R							
0h							
7	6	5	4	3	2	1	0
ADDR							
R							
0h							

Table 4-547. STC_STC_CADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR	R	0h	Current ROM Address for CORE1 This register reflects the current ROM address [for micro code load] accessed during selftest for CORE1 in of case segment0 and all the remaining segmentsn where n = 1 to 3].

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4.1.2.262 STC_STCCICR Register

4.1.2.262.1 STC_STCCICR Register (Offset = 10h) [reset = 0h]

Current Interval count register.

Return to Summary Table

Table 4-548. Instance Table

Instance Name	Physical Address
R5SS0	5350 0010h
R5SS1	5351 0010h

Figure 4-262. STC_STCCICR Name Register

31	30	29	28	27	26	25	24
CORE2_ICOUNT							
R							
0h							
23	22	21	20	19	18	17	16
CORE2_ICOUNT							
R							
0h							
15	14	13	12	11	10	9	8
CORE1_ICOUNT							
R							
0h							
7	6	5	4	3	2	1	0
CORE1_ICOUNT							
R							
0h							

Table 4-549. STC_STCCICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CORE2_ICOUNT	R	0h	Specifies the last interval number for CORE2 This specifies the Last executed Interval number for CORE2 of Segment0 if self test is being executed for secondary core as well. This field is applicable only for Segment 0.
15:0	CORE1_ICOUNT	R	0h	Specifies the last interval number for CORE1 This specifies the Last executed Interval number of a self-test run.

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4.1.2.263 STC_STCGSTAT Register

4.1.2.263.1 STC_STCGSTAT Register (Offset = 14h) [reset = 500h]

Global Status Register.

Return to Summary Table

Table 4-550. Instance Table

Instance Name	Physical Address
R5SS0	5350 0014h
R5SS1	5351 0014h

Figure 4-263. STC_STCGSTAT Name Register

31	30	29	28	27	26	25	24
NU4							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU4							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU4				ST_ACTIVE			
R				R			
0h				5h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU5						TEST_FAIL	TEST_DONE
R						R	R
0h						0h	0h

Table 4-551. STC_STCGSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	NU4	R	0h	Reserved bits
11:8	ST_ACTIVE	R	5h	Tells whether self test is currently active or not. 1010 = Self test is active Others = SelfTest is not active Once the self-test completes and ST_ENA_B4 key is cleared, this field will reflect the inactive value.
7:2	NU5	R	0h	Reserved bits
1	TEST_FAIL	R	0h	Test_fail flag [RCP - Read, Clear on Writing in Priviledge Mode] 0 = Self test run has not failed 1 = SelfTest run has failed. Write Clear.
0	TEST_DONE	R	0h	Test_done_flag [RCP - Read, Clear on Writing in Priviledge Mode] 0 = Not completed 1 = SelfTest run Completed

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4.1.2.264 STC_STCFSTAT Register

4.1.2.264.1 STC_STCFSTAT Register (Offset = 18h) [reset = 0h]

Fail Status Register.

Return to Summary Table

Table 4-552. Instance Table

Instance Name	Physical Address
R5SS0	5350 0018h
R5SS1	5351 0018h

Figure 4-264. STC_STCFSTAT Name Register

31	30	29	28	27	26	25	24
NU6							
R							
0h							
23	22	21	20	19	18	17	16
NU6							
R							
0h							
15	14	13	12	11	10	9	8
NU6							
R							
0h							
7	6	5	4	3	2	1	0
NU6			FSEG_ID		TO_ER_B1	CPU2_FAIL_B1	CPU1_FAIL_B1
R			R		R	R	R
0h			0h		0h	0h	0h

Table 4-553. STC_STCFSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	NU6	R	0h	Reserved bits
4:3	FSEG_ID	R	0h	Failed Segment ID [RCP - Read, Clear on Writing in Priviledge Mode] This field captures the Segment number for which any of the failures like TO_ER_B1, CPU1_FAIL_B1 and CPU2_FAIL_B1 occur. 00 = Failure on Segment 0 01 = Failure on Segment 1 10 = Failure on Segment 2 11 = Failure on Segment 3
2	TO_ER_B1	R	0h	Tells whether self test failed because of time out error [RCP - Read, Clear on Writing in Priviledge Mode] 0 = No time out error occurred 1 = SelfTest run failed due to a timeout error
1	CPU2_FAIL_B1	R	0h	Tells whether MISR mismatch happenned in CORE2 when in Segment0 mode [RCP - Read, Clear on Writing in Priviledge Mode] 0 = No MISR mismatch for CORE2 1 = Self test run failed due to MISR mismatch for CORE2
0	CPU1_FAIL_B1	R	0h	Tells whether MISR mismatch happenned in CORE1 [RCP - Read, Clear on Writing in Priviledge Mode] Applicable to all segments. 0 = No MISR mismatch for CORE1 1 = Self test run failed due to MISR mismatch for CORE1

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4.1.2.265 STC_STCSCSCR Register

4.1.2.265.1 STC_STCSCSCR Register (Offset = 1Ch) [reset = 5h]

Signature compare Self Check Register.

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Table 4-554. Instance Table

Instance Name	Physical Address
R5SS0	5350 001Ch
R5SS1	5351 001Ch

Figure 4-265. STC_STCSCSCR Name Register

31	30	29	28	27	26	25	24
NU7							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU7							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU7							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU7			FAULT_INS_B1	SELF_CHECK_KEY_B4			
R			R/W	R/W			
0h			0h	5h			

Table 4-555. STC_STCSCSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	NU7	R	0h	Reserved bits
4	FAULT_INS_B1	R/W	0h	Fault Insertion bit [RWP - Read, Priviledge Mode Write only] 0 = No fault insertion. 1 = Inserts fault in the logic under test which will make signature compare fail. This feature is used as diagnostic check of the STC IP.
3:0	SELF_CHECK_KEY_B4	R/W	5h	Signature compare logic self check key enable/disable [RWP - Read, Priviledge Mode Write only] 1010 = Signature compare logic Self Check is enabled All values other than 1010 = Signature compare logic Self Check is disabled

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4.1.2.266 STC_STC_CADDR2 Register

4.1.2.266.1 STC_STC_CADDR2 Register (Offset = 20h) [reset = 0h]

Current Address register for CORE2.

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Table 4-556. Instance Table

Instance Name	Physical Address
R5SS0	5350 0020h
R5SS1	5351 0020h

Figure 4-266. STC_STC_CADDR2 Name Register

31	30	29	28	27	26	25	24
ADDR							
R							
0h							
23	22	21	20	19	18	17	16
ADDR							
R							
0h							
15	14	13	12	11	10	9	8
ADDR							
R							
0h							
7	6	5	4	3	2	1	0
ADDR							
R							
0h							

Table 4-557. STC_STC_CADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR	R	0h	Current ROM Address for CORE2 This register reflects the current ROM address[for micro code load] accessed during selftest for CORE2 in of case segment0.

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4.1.2.267 STC_STC_CLKDIV Register

4.1.2.267.1 STC_STC_CLKDIV Register (Offset = 24h) [reset = 0h]

Clock Divider Register.

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Table 4-558. Instance Table

Instance Name	Physical Address
R5SS0	5350 0024h
R5SS1	5351 0024h

Figure 4-267. STC_STC_CLKDIV Name Register

31	30	29	28	27	26	25	24
NU8					CLKDIV0		
R					R/W		
0h					0h		
23	22	21	20	19	18	17	16
NU9					CLKDIV1		
R					R/W		
0h					0h		
15	14	13	12	11	10	9	8
NU10					CLKDIV2		
R					R/W		
0h					0h		
7	6	5	4	3	2	1	0
NU11					CLKDIV3		
R					R/W		
0h					0h		

Table 4-559. STC_STC_CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	NU8	R	0h	Reserved bits
26:24	CLKDIV0	R/W	0h	Clock division for Seg0 [RWP - Read, Priviledge Mode Write only] *NOT SUPPORTED X = Division ratio is X+1 for Segment 0
23:19	NU9	R	0h	Reserved bits
18:16	CLKDIV1	R/W	0h	Clock division for Seg1 [RWP - Read, Priviledge Mode Write only] *NOT SUPPORTED X = Division ratio is X+1 for Segment 1
15:11	NU10	R	0h	Reserved bits
10:8	CLKDIV2	R/W	0h	Clock division for Seg2 [RWP - Read, Priviledge Mode Write only] *NOT SUPPORTED X = Division ratio is X+1 for Segment 2
7:3	NU11	R	0h	Reserved bits
2:0	CLKDIV3	R/W	0h	Clock division for Seg3 [RWP - Read, Priviledge Mode Write only] *NOT SUPPORTED X = Division ratio is X+1 for Segment 3

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4.1.2.268 STC_STC_SEGPLR Register

4.1.2.268.1 STC_STC_SEGPLR Register (Offset = 28h) [reset = 0h]

Segment 1st interval Preload Register.

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Table 4-560. Instance Table

Instance Name	Physical Address
R5SS0	5350 0028h
R5SS1	5351 0028h

Figure 4-268. STC_STC_SEGPLR Name Register

31	30	29	28	27	26	25	24
NU12							
R							
0h							
23	22	21	20	19	18	17	16
NU12							
R							
0h							
15	14	13	12	11	10	9	8
NU12							
R							
0h							
7	6	5	4	3	2	1	0
NU12						SEGID_PLOAD	
R						R/W	
0h						0h	

Table 4-561. STC_STC_SEGPLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU12	R	0h	Reserved bits
1:0	SEGID_PLOAD	R/W	0h	Segment number for which preload is to be started [RWP - Read, Priviledge Mode Write only] This specifies the segment for which the address of its First interval will be pre-loaded into the NSTC ROM address counter. The 1st address of each segment are defined in SEGx_START_ADDR register.The address of the 1st interval of the selected segment is loaded into the NSTC ROM address counter when the RS_CNT_B1 bits of STC_GCR0 are set to 1X 00 = Preload the address of the 1st interval of segment 0. 01 = Preload the address of the 1st interval of segment 1. 10 = Preload the address of the 1st interval of segment 2. 11 = Preload the address of the 1st interval of segment 3.

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4.1.2.269 STC_SEG0_START_ADDR Register

4.1.2.269.1 STC_SEG0_START_ADDR Register (Offset = 2Ch) [reset = 0h]

ROM Start address for Segment0.

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Table 4-562. Instance Table

Instance Name	Physical Address
R5SS0	5350 002Ch
R5SS1	5351 002Ch

Figure 4-269. STC_SEG0_START_ADDR Name Register

31	30	29	28	27	26	25	24
NU13							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU13				SEG_START_ADDR			
R				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SEG_START_ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEG_START_ADDR							
R/W							
0h							

Table 4-563. STC_SEG0_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NU13	R	0h	Reserved bits
19:0	SEG_START_ADDR	R/W	0h	Segment 0 Start Address [RWP - Read, Priviledge Mode Write only] This register holds the ROM address for the start of first interval of the segment. When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register. Valid number of bits depends on RTL paramerter ADDR

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4.1.2.270 STC_SEG1_START_ADDR Register

4.1.2.270.1 STC_SEG1_START_ADDR Register (Offset = 30h) [reset = 0h]

ROM Start address for Segment1.

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Table 4-564. Instance Table

Instance Name	Physical Address
R5SS0	5350 0030h
R5SS1	5351 0030h

Figure 4-270. STC_SEG1_START_ADDR Name Register

31	30	29	28	27	26	25	24
NU14							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU14				SEG_START_ADDR			
R				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SEG_START_ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEG_START_ADDR							
R/W							
0h							

Table 4-565. STC_SEG1_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NU14	R	0h	Reserved bits
19:0	SEG_START_ADDR	R/W	0h	Segment 1 Start Address [RWP - Read, Priviledge Mode Write only] This register holds the ROM address for the start of first interval of the segment. When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register. Valid number of bits depends on RTL paramerter ADDR. This register is present only when RTL parameter NUM_SEG = 1.

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4.1.2.271 STC_SEG2_START_ADDR Register

4.1.2.271.1 STC_SEG2_START_ADDR Register (Offset = 34h) [reset = 0h]

ROM Start address for Segment2.

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Table 4-566. Instance Table

Instance Name	Physical Address
R5SS0	5350 0034h
R5SS1	5351 0034h

Figure 4-271. STC_SEG2_START_ADDR Name Register

31	30	29	28	27	26	25	24
NU15							
R							
0h							
23	22	21	20	19	18	17	16
NU15				SEG_START_ADDR			
R				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SEG_START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
SEG_START_ADDR							
R/W							
0h							

Table 4-567. STC_SEG2_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NU15	R	0h	Reserved bits
19:0	SEG_START_ADDR	R/W	0h	Segment 2 Start Address [RWP - Read, Priviledge Mode Write only] This register holds the ROM address for the start of first interval of the segment. When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register. Valid number of bits depends on RTL paramerter ADDR. This register is present only when RTL parameter NUM_SEG = 2.

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4.1.2.272 STC_SEG3_START_ADDR Register

4.1.2.272.1 STC_SEG3_START_ADDR Register (Offset = 38h) [reset = 0h]

ROM Start address for Segment3.

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Table 4-568. Instance Table

Instance Name	Physical Address
R5SS0	5350 0038h
R5SS1	5351 0038h

Figure 4-272. STC_SEG3_START_ADDR Name Register

31	30	29	28	27	26	25	24
NU16							
R							
0h							
23	22	21	20	19	18	17	16
NU16				SEG_START_ADDR			
R				R/W			
0h				0h			
15	14	13	12	11	10	9	8
SEG_START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
SEG_START_ADDR							
R/W							
0h							

Table 4-569. STC_SEG3_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NU16	R	0h	Reserved bits
19:0	SEG_START_ADDR	R/W	0h	Segment 3 Start Address [RWP - Read, Priviledge Mode Write only] This register holds the ROM address for the start of first interval of the segment. When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register. Valid number of bits depends on RTL paramerter ADDR. This register is present only when RTL parameter NUM_SEG = 3.

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4.1.2.273 STC_CORE1_CURMISR_0 Register

4.1.2.273.1 STC_CORE1_CURMISR_0 Register (Offset = 3Ch) [reset = 0h]

Holds the MISR signature for CORE1.

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Table 4-570. Instance Table

Instance Name	Physical Address
R5SS0	5350 003Ch
R5SS1	5351 003Ch

Figure 4-273. STC_CORE1_CURMISR_0 Name Register

31	30	29	28	27	26	25	24
C1MISR0							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR0							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR0							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR0							
R							
0h							

Table 4-571. STC_CORE1_CURMISR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR0	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.274 STC_CORE1_CURMISR_1 Register

4.1.2.274.1 STC_CORE1_CURMISR_1 Register (Offset = 40h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-572. Instance Table

Instance Name	Physical Address
R5SS0	5350 0040h
R5SS1	5351 0040h

Figure 4-274. STC_CORE1_CURMISR_1 Name Register

31	30	29	28	27	26	25	24
C1MISR1							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR1							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR1							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR1							
R							
0h							

Table 4-573. STC_CORE1_CURMISR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR1	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.275 STC_CORE1_CURMISR_2 Register

4.1.2.275.1 STC_CORE1_CURMISR_2 Register (Offset = 44h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-574. Instance Table

Instance Name	Physical Address
R5SS0	5350 0044h
R5SS1	5351 0044h

Figure 4-275. STC_CORE1_CURMISR_2 Name Register

31	30	29	28	27	26	25	24
C1MISR2							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR2							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR2							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR2							
R							
0h							

Table 4-575. STC_CORE1_CURMISR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR2	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.276 STC_CORE1_CURMISR_3 Register

4.1.2.276.1 STC_CORE1_CURMISR_3 Register (Offset = 48h) [reset = 0h]

Holds the MISR signature for CORE1.

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Table 4-576. Instance Table

Instance Name	Physical Address
R5SS0	5350 0048h
R5SS1	5351 0048h

Figure 4-276. STC_CORE1_CURMISR_3 Name Register

31	30	29	28	27	26	25	24
C1MISR3							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR3							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR3							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR3							
R							
0h							

Table 4-577. STC_CORE1_CURMISR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR3	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.277 STC_CORE1_CURMISR_4 Register

4.1.2.277.1 STC_CORE1_CURMISR_4 Register (Offset = 4Ch) [reset = 0h]

Holds the MISR signature for CORE1.

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Table 4-578. Instance Table

Instance Name	Physical Address
R5SS0	5350 004Ch
R5SS1	5351 004Ch

Figure 4-277. STC_CORE1_CURMISR_4 Name Register

31	30	29	28	27	26	25	24
C1MISR4							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR4							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR4							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR4							
R							
0h							

Table 4-579. STC_CORE1_CURMISR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR4	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.278 STC_CORE1_CURMISR_5 Register

4.1.2.278.1 STC_CORE1_CURMISR_5 Register (Offset = 50h) [reset = 0h]

Holds the MISR signature for CORE1.

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Table 4-580. Instance Table

Instance Name	Physical Address
R5SS0	5350 0050h
R5SS1	5351 0050h

Figure 4-278. STC_CORE1_CURMISR_5 Name Register

31	30	29	28	27	26	25	24
C1MISR5							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR5							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR5							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR5							
R							
0h							

Table 4-581. STC_CORE1_CURMISR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR5	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.279 STC_CORE1_CURMISR_6 Register

4.1.2.279.1 STC_CORE1_CURMISR_6 Register (Offset = 54h) [reset = 0h]

Holds the MISR signature for CORE1.

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Table 4-582. Instance Table

Instance Name	Physical Address
R5SS0	5350 0054h
R5SS1	5351 0054h

Figure 4-279. STC_CORE1_CURMISR_6 Name Register

31	30	29	28	27	26	25	24
C1MISR6							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR6							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR6							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR6							
R							
0h							

Table 4-583. STC_CORE1_CURMISR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR6	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.280 STC_CORE1_CURMISR_7 Register

4.1.2.280.1 STC_CORE1_CURMISR_7 Register (Offset = 58h) [reset = 0h]

Holds the MISR signature for CORE1.

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Table 4-584. Instance Table

Instance Name	Physical Address
R5SS0	5350 0058h
R5SS1	5351 0058h

Figure 4-280. STC_CORE1_CURMISR_7 Name Register

31	30	29	28	27	26	25	24
C1MISR7							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR7							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR7							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR7							
R							
0h							

Table 4-585. STC_CORE1_CURMISR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR7	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.281 STC_CORE1_CURMISR_8 Register

4.1.2.281.1 STC_CORE1_CURMISR_8 Register (Offset = 5Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-586. Instance Table

Instance Name	Physical Address
R5SS0	5350 005Ch
R5SS1	5351 005Ch

Figure 4-281. STC_CORE1_CURMISR_8 Name Register

31	30	29	28	27	26	25	24
C1MISR8							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR8							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR8							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR8							
R							
0h							

Table 4-587. STC_CORE1_CURMISR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR8	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.282 STC_CORE1_CURMISR_9 Register

4.1.2.282.1 STC_CORE1_CURMISR_9 Register (Offset = 60h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-588. Instance Table

Instance Name	Physical Address
R5SS0	5350 0060h
R5SS1	5351 0060h

Figure 4-282. STC_CORE1_CURMISR_9 Name Register

31	30	29	28	27	26	25	24
C1MISR9							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR9							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR9							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR9							
R							
0h							

Table 4-589. STC_CORE1_CURMISR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR9	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.283 STC_CORE1_CURMISR_10 Register

4.1.2.283.1 STC_CORE1_CURMISR_10 Register (Offset = 64h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-590. Instance Table

Instance Name	Physical Address
R5SS0	5350 0064h
R5SS1	5351 0064h

Figure 4-283. STC_CORE1_CURMISR_10 Name Register

31	30	29	28	27	26	25	24
C1MISR10							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR10							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR10							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR10							
R							
0h							

Table 4-591. STC_CORE1_CURMISR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR10	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.284 STC_CORE1_CURMISR_11 Register

4.1.2.284.1 STC_CORE1_CURMISR_11 Register (Offset = 68h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-592. Instance Table

Instance Name	Physical Address
R5SS0	5350 0068h
R5SS1	5351 0068h

Figure 4-284. STC_CORE1_CURMISR_11 Name Register

31	30	29	28	27	26	25	24
C1MISR11							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR11							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR11							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR11							
R							
0h							

Table 4-593. STC_CORE1_CURMISR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR11	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.285 STC_CORE1_CURMISR_12 Register

4.1.2.285.1 STC_CORE1_CURMISR_12 Register (Offset = 6Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-594. Instance Table

Instance Name	Physical Address
R5SS0	5350 006Ch
R5SS1	5351 006Ch

Figure 4-285. STC_CORE1_CURMISR_12 Name Register

31	30	29	28	27	26	25	24
C1MISR12							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR12							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR12							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR12							
R							
0h							

Table 4-595. STC_CORE1_CURMISR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR12	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.286 STC_CORE1_CURMISR_13 Register

4.1.2.286.1 STC_CORE1_CURMISR_13 Register (Offset = 70h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-596. Instance Table

Instance Name	Physical Address
R5SS0	5350 0070h
R5SS1	5351 0070h

Figure 4-286. STC_CORE1_CURMISR_13 Name Register

31	30	29	28	27	26	25	24
C1MISR13							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR13							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR13							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR13							
R							
0h							

Table 4-597. STC_CORE1_CURMISR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR13	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.287 STC_CORE1_CURMISR_14 Register

4.1.2.287.1 STC_CORE1_CURMISR_14 Register (Offset = 74h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-598. Instance Table

Instance Name	Physical Address
R5SS0	5350 0074h
R5SS1	5351 0074h

Figure 4-287. STC_CORE1_CURMISR_14 Name Register

31	30	29	28	27	26	25	24
C1MISR14							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR14							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR14							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR14							
R							
0h							

Table 4-599. STC_CORE1_CURMISR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR14	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.288 STC_CORE1_CURMISR_15 Register

4.1.2.288.1 STC_CORE1_CURMISR_15 Register (Offset = 78h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-600. Instance Table

Instance Name	Physical Address
R5SS0	5350 0078h
R5SS1	5351 0078h

Figure 4-288. STC_CORE1_CURMISR_15 Name Register

31	30	29	28	27	26	25	24
C1MISR15							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR15							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR15							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR15							
R							
0h							

Table 4-601. STC_CORE1_CURMISR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR15	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.289 STC_CORE1_CURMISR_16 Register

4.1.2.289.1 STC_CORE1_CURMISR_16 Register (Offset = 7Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-602. Instance Table

Instance Name	Physical Address
R5SS0	5350 007Ch
R5SS1	5351 007Ch

Figure 4-289. STC_CORE1_CURMISR_16 Name Register

31	30	29	28	27	26	25	24
C1MISR16							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR16							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR16							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR16							
R							
0h							

Table 4-603. STC_CORE1_CURMISR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR16	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.290 STC_CORE1_CURMISR_17 Register

4.1.2.290.1 STC_CORE1_CURMISR_17 Register (Offset = 80h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-604. Instance Table

Instance Name	Physical Address
R5SS0	5350 0080h
R5SS1	5351 0080h

Figure 4-290. STC_CORE1_CURMISR_17 Name Register

31	30	29	28	27	26	25	24
C1MISR17							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR17							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR17							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR17							
R							
0h							

Table 4-605. STC_CORE1_CURMISR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR17	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.291 STC_CORE1_CURMISR_18 Register

4.1.2.291.1 STC_CORE1_CURMISR_18 Register (Offset = 84h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-606. Instance Table

Instance Name	Physical Address
R5SS0	5350 0084h
R5SS1	5351 0084h

Figure 4-291. STC_CORE1_CURMISR_18 Name Register

31	30	29	28	27	26	25	24
C1MISR18							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR18							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR18							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR18							
R							
0h							

Table 4-607. STC_CORE1_CURMISR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR18	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.292 STC_CORE1_CURMISR_19 Register

4.1.2.292.1 STC_CORE1_CURMISR_19 Register (Offset = 88h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-608. Instance Table

Instance Name	Physical Address
R5SS0	5350 0088h
R5SS1	5351 0088h

Figure 4-292. STC_CORE1_CURMISR_19 Name Register

31	30	29	28	27	26	25	24
C1MISR19							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR19							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR19							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR19							
R							
0h							

Table 4-609. STC_CORE1_CURMISR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR19	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.293 STC_CORE1_CURMISR_20 Register

4.1.2.293.1 STC_CORE1_CURMISR_20 Register (Offset = 8Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-610. Instance Table

Instance Name	Physical Address
R5SS0	5350 008Ch
R5SS1	5351 008Ch

Figure 4-293. STC_CORE1_CURMISR_20 Name Register

31	30	29	28	27	26	25	24
C1MISR20							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR20							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR20							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR20							
R							
0h							

Table 4-611. STC_CORE1_CURMISR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR20	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.294 STC_CORE1_CURMISR_21 Register

4.1.2.294.1 STC_CORE1_CURMISR_21 Register (Offset = 90h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-612. Instance Table

Instance Name	Physical Address
R5SS0	5350 0090h
R5SS1	5351 0090h

Figure 4-294. STC_CORE1_CURMISR_21 Name Register

31	30	29	28	27	26	25	24
C1MISR21							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR21							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR21							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR21							
R							
0h							

Table 4-613. STC_CORE1_CURMISR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR21	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.295 STC_CORE1_CURMISR_22 Register

4.1.2.295.1 STC_CORE1_CURMISR_22 Register (Offset = 94h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-614. Instance Table

Instance Name	Physical Address
R5SS0	5350 0094h
R5SS1	5351 0094h

Figure 4-295. STC_CORE1_CURMISR_22 Name Register

31	30	29	28	27	26	25	24
C1MISR22							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR22							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR22							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR22							
R							
0h							

Table 4-615. STC_CORE1_CURMISR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR22	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.296 STC_CORE1_CURMISR_23 Register

4.1.2.296.1 STC_CORE1_CURMISR_23 Register (Offset = 98h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-616. Instance Table

Instance Name	Physical Address
R5SS0	5350 0098h
R5SS1	5351 0098h

Figure 4-296. STC_CORE1_CURMISR_23 Name Register

31	30	29	28	27	26	25	24
C1MISR23							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR23							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR23							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR23							
R							
0h							

Table 4-617. STC_CORE1_CURMISR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR23	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.297 STC_CORE1_CURMISR_24 Register

4.1.2.297.1 STC_CORE1_CURMISR_24 Register (Offset = 9Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-618. Instance Table

Instance Name	Physical Address
R5SS0	5350 009Ch
R5SS1	5351 009Ch

Figure 4-297. STC_CORE1_CURMISR_24 Name Register

31	30	29	28	27	26	25	24
C1MISR24							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR24							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR24							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR24							
R							
0h							

Table 4-619. STC_CORE1_CURMISR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR24	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.298 STC_CORE1_CURMISR_25 Register

4.1.2.298.1 STC_CORE1_CURMISR_25 Register (Offset = A0h) [reset = 0h]

Holds the MISR signature for CORE1.

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Table 4-620. Instance Table

Instance Name	Physical Address
R5SS0	5350 00A0h
R5SS1	5351 00A0h

Figure 4-298. STC_CORE1_CURMISR_25 Name Register

31	30	29	28	27	26	25	24
C1MISR25							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR25							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR25							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR25							
R							
0h							

Table 4-621. STC_CORE1_CURMISR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR25	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.299 STC_CORE1_CURMISR_26 Register

4.1.2.299.1 STC_CORE1_CURMISR_26 Register (Offset = A4h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-622. Instance Table

Instance Name	Physical Address
R5SS0	5350 00A4h
R5SS1	5351 00A4h

Figure 4-299. STC_CORE1_CURMISR_26 Name Register

31	30	29	28	27	26	25	24
C1MISR26							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR26							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR26							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR26							
R							
0h							

Table 4-623. STC_CORE1_CURMISR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR26	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.300 STC_CORE1_CURMISR_27 Register

4.1.2.300.1 STC_CORE1_CURMISR_27 Register (Offset = A8h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to Summary Table

Table 4-624. Instance Table

Instance Name	Physical Address
R5SS0	5350 00A8h
R5SS1	5351 00A8h

Figure 4-300. STC_CORE1_CURMISR_27 Name Register

31	30	29	28	27	26	25	24
C1MISR27							
R							
0h							
23	22	21	20	19	18	17	16
C1MISR27							
R							
0h							
15	14	13	12	11	10	9	8
C1MISR27							
R							
0h							
7	6	5	4	3	2	1	0
C1MISR27							
R							
0h							

Table 4-625. STC_CORE1_CURMISR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C1MISR27	R	0h	MISR Signature for CORE1 This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.301 STC_CORE2_CURMISR_0 Register

4.1.2.301.1 STC_CORE2_CURMISR_0 Register (Offset = ACh) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-626. Instance Table

Instance Name	Physical Address
R5SS0	5350 00ACh
R5SS1	5351 00ACh

Figure 4-301. STC_CORE2_CURMISR_0 Name Register

31	30	29	28	27	26	25	24
C2MISR0							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR0							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR0							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR0							
R							
0h							

Table 4-627. STC_CORE2_CURMISR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR0	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.302 STC_CORE2_CURMISR_1 Register

4.1.2.302.1 STC_CORE2_CURMISR_1 Register (Offset = B0h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-628. Instance Table

Instance Name	Physical Address
R5SS0	5350 00B0h
R5SS1	5351 00B0h

Figure 4-302. STC_CORE2_CURMISR_1 Name Register

31	30	29	28	27	26	25	24
C2MISR1							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR1							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR1							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR1							
R							
0h							

Table 4-629. STC_CORE2_CURMISR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR1	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.303 STC_CORE2_CURMISR_2 Register

4.1.2.303.1 STC_CORE2_CURMISR_2 Register (Offset = B4h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-630. Instance Table

Instance Name	Physical Address
R5SS0	5350 00B4h
R5SS1	5351 00B4h

Figure 4-303. STC_CORE2_CURMISR_2 Name Register

31	30	29	28	27	26	25	24
C2MISR2							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR2							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR2							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR2							
R							
0h							

Table 4-631. STC_CORE2_CURMISR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR2	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.304 STC_CORE2_CURMISR_3 Register

4.1.2.304.1 STC_CORE2_CURMISR_3 Register (Offset = B8h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-632. Instance Table

Instance Name	Physical Address
R5SS0	5350 00B8h
R5SS1	5351 00B8h

Figure 4-304. STC_CORE2_CURMISR_3 Name Register

31	30	29	28	27	26	25	24
C2MISR3							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR3							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR3							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR3							
R							
0h							

Table 4-633. STC_CORE2_CURMISR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR3	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.305 STC_CORE2_CURMISR_4 Register

4.1.2.305.1 STC_CORE2_CURMISR_4 Register (Offset = BCh) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-634. Instance Table

Instance Name	Physical Address
R5SS0	5350 00BCh
R5SS1	5351 00BCh

Figure 4-305. STC_CORE2_CURMISR_4 Name Register

31	30	29	28	27	26	25	24
C2MISR4							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR4							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR4							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR4							
R							
0h							

Table 4-635. STC_CORE2_CURMISR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR4	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.306 STC_CORE2_CURMISR_5 Register

4.1.2.306.1 STC_CORE2_CURMISR_5 Register (Offset = C0h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-636. Instance Table

Instance Name	Physical Address
R5SS0	5350 00C0h
R5SS1	5351 00C0h

Figure 4-306. STC_CORE2_CURMISR_5 Name Register

31	30	29	28	27	26	25	24
C2MISR5							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR5							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR5							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR5							
R							
0h							

Table 4-637. STC_CORE2_CURMISR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR5	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.307 STC_CORE2_CURMISR_6 Register

4.1.2.307.1 STC_CORE2_CURMISR_6 Register (Offset = C4h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-638. Instance Table

Instance Name	Physical Address
R5SS0	5350 00C4h
R5SS1	5351 00C4h

Figure 4-307. STC_CORE2_CURMISR_6 Name Register

31	30	29	28	27	26	25	24
C2MISR6							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR6							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR6							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR6							
R							
0h							

Table 4-639. STC_CORE2_CURMISR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR6	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.308 STC_CORE2_CURMISR_7 Register

4.1.2.308.1 STC_CORE2_CURMISR_7 Register (Offset = C8h) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-640. Instance Table

Instance Name	Physical Address
R5SS0	5350 00C8h
R5SS1	5351 00C8h

Figure 4-308. STC_CORE2_CURMISR_7 Name Register

31	30	29	28	27	26	25	24
C2MISR7							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR7							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR7							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR7							
R							
0h							

Table 4-641. STC_CORE2_CURMISR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR7	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.309 STC_CORE2_CURMISR_8 Register

4.1.2.309.1 STC_CORE2_CURMISR_8 Register (Offset = CCh) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-642. Instance Table

Instance Name	Physical Address
R5SS0	5350 00CCh
R5SS1	5351 00CCh

Figure 4-309. STC_CORE2_CURMISR_8 Name Register

31	30	29	28	27	26	25	24
C2MISR8							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR8							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR8							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR8							
R							
0h							

Table 4-643. STC_CORE2_CURMISR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR8	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.310 STC_CORE2_CURMISR_9 Register

4.1.2.310.1 STC_CORE2_CURMISR_9 Register (Offset = D0h) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-644. Instance Table

Instance Name	Physical Address
R5SS0	5350 00D0h
R5SS1	5351 00D0h

Figure 4-310. STC_CORE2_CURMISR_9 Name Register

31	30	29	28	27	26	25	24
C2MISR9							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR9							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR9							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR9							
R							
0h							

Table 4-645. STC_CORE2_CURMISR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR9	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.311 STC_CORE2_CURMISR_10 Register

4.1.2.311.1 STC_CORE2_CURMISR_10 Register (Offset = D4h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-646. Instance Table

Instance Name	Physical Address
R5SS0	5350 00D4h
R5SS1	5351 00D4h

Figure 4-311. STC_CORE2_CURMISR_10 Name Register

31	30	29	28	27	26	25	24
C2MISR10							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR10							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR10							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR10							
R							
0h							

Table 4-647. STC_CORE2_CURMISR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR10	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.312 STC_CORE2_CURMISR_11 Register

4.1.2.312.1 STC_CORE2_CURMISR_11 Register (Offset = D8h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-648. Instance Table

Instance Name	Physical Address
R5SS0	5350 00D8h
R5SS1	5351 00D8h

Figure 4-312. STC_CORE2_CURMISR_11 Name Register

31	30	29	28	27	26	25	24
C2MISR11							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR11							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR11							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR11							
R							
0h							

Table 4-649. STC_CORE2_CURMISR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR11	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.313 STC_CORE2_CURMISR_12 Register

4.1.2.313.1 STC_CORE2_CURMISR_12 Register (Offset = DCh) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-650. Instance Table

Instance Name	Physical Address
R5SS0	5350 00DCh
R5SS1	5351 00DCh

Figure 4-313. STC_CORE2_CURMISR_12 Name Register

31	30	29	28	27	26	25	24
C2MISR12							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR12							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR12							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR12							
R							
0h							

Table 4-651. STC_CORE2_CURMISR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR12	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.314 STC_CORE2_CURMISR_13 Register

4.1.2.314.1 STC_CORE2_CURMISR_13 Register (Offset = E0h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-652. Instance Table

Instance Name	Physical Address
R5SS0	5350 00E0h
R5SS1	5351 00E0h

Figure 4-314. STC_CORE2_CURMISR_13 Name Register

31	30	29	28	27	26	25	24
C2MISR13							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR13							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR13							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR13							
R							
0h							

Table 4-653. STC_CORE2_CURMISR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR13	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.315 STC_CORE2_CURMISR_14 Register

4.1.2.315.1 STC_CORE2_CURMISR_14 Register (Offset = E4h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-654. Instance Table

Instance Name	Physical Address
R5SS0	5350 00E4h
R5SS1	5351 00E4h

Figure 4-315. STC_CORE2_CURMISR_14 Name Register

31	30	29	28	27	26	25	24
C2MISR14							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR14							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR14							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR14							
R							
0h							

Table 4-655. STC_CORE2_CURMISR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR14	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.316 STC_CORE2_CURMISR_15 Register

4.1.2.316.1 STC_CORE2_CURMISR_15 Register (Offset = E8h) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-656. Instance Table

Instance Name	Physical Address
R5SS0	5350 00E8h
R5SS1	5351 00E8h

Figure 4-316. STC_CORE2_CURMISR_15 Name Register

31	30	29	28	27	26	25	24
C2MISR15							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR15							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR15							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR15							
R							
0h							

Table 4-657. STC_CORE2_CURMISR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR15	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.317 STC_CORE2_CURMISR_16 Register

4.1.2.317.1 STC_CORE2_CURMISR_16 Register (Offset = ECh) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-658. Instance Table

Instance Name	Physical Address
R5SS0	5350 00ECh
R5SS1	5351 00ECh

Figure 4-317. STC_CORE2_CURMISR_16 Name Register

31	30	29	28	27	26	25	24
C2MISR16							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR16							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR16							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR16							
R							
0h							

Table 4-659. STC_CORE2_CURMISR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR16	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.318 STC_CORE2_CURMISR_17 Register

4.1.2.318.1 STC_CORE2_CURMISR_17 Register (Offset = F0h) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-660. Instance Table

Instance Name	Physical Address
R5SS0	5350 00F0h
R5SS1	5351 00F0h

Figure 4-318. STC_CORE2_CURMISR_17 Name Register

31	30	29	28	27	26	25	24
C2MISR17							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR17							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR17							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR17							
R							
0h							

Table 4-661. STC_CORE2_CURMISR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR17	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.319 STC_CORE2_CURMISR_18 Register

4.1.2.319.1 STC_CORE2_CURMISR_18 Register (Offset = F4h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-662. Instance Table

Instance Name	Physical Address
R5SS0	5350 00F4h
R5SS1	5351 00F4h

Figure 4-319. STC_CORE2_CURMISR_18 Name Register

31	30	29	28	27	26	25	24
C2MISR18							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR18							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR18							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR18							
R							
0h							

Table 4-663. STC_CORE2_CURMISR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR18	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.320 STC_CORE2_CURMISR_19 Register

4.1.2.320.1 STC_CORE2_CURMISR_19 Register (Offset = F8h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-664. Instance Table

Instance Name	Physical Address
R5SS0	5350 00F8h
R5SS1	5351 00F8h

Figure 4-320. STC_CORE2_CURMISR_19 Name Register

31	30	29	28	27	26	25	24
C2MISR19							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR19							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR19							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR19							
R							
0h							

Table 4-665. STC_CORE2_CURMISR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR19	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.321 STC_CORE2_CURMISR_20 Register

4.1.2.321.1 STC_CORE2_CURMISR_20 Register (Offset = FCh) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-666. Instance Table

Instance Name	Physical Address
R5SS0	5350 00FCh
R5SS1	5351 00FCh

Figure 4-321. STC_CORE2_CURMISR_20 Name Register

31	30	29	28	27	26	25	24
C2MISR20							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR20							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR20							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR20							
R							
0h							

Table 4-667. STC_CORE2_CURMISR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR20	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.322 STC_CORE2_CURMISR_21 Register

4.1.2.322.1 STC_CORE2_CURMISR_21 Register (Offset = 100h) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-668. Instance Table

Instance Name	Physical Address
R5SS0	5350 0100h
R5SS1	5351 0100h

Figure 4-322. STC_CORE2_CURMISR_21 Name Register

31	30	29	28	27	26	25	24
C2MISR21							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR21							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR21							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR21							
R							
0h							

Table 4-669. STC_CORE2_CURMISR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR21	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.323 STC_CORE2_CURMISR_22 Register

4.1.2.323.1 STC_CORE2_CURMISR_22 Register (Offset = 104h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to Summary Table

Table 4-670. Instance Table

Instance Name	Physical Address
R5SS0	5350 0104h
R5SS1	5351 0104h

Figure 4-323. STC_CORE2_CURMISR_22 Name Register

31	30	29	28	27	26	25	24
C2MISR22							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR22							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR22							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR22							
R							
0h							

Table 4-671. STC_CORE2_CURMISR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR22	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.324 STC_CORE2_CURMISR_23 Register

4.1.2.324.1 STC_CORE2_CURMISR_23 Register (Offset = 108h) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-672. Instance Table

Instance Name	Physical Address
R5SS0	5350 0108h
R5SS1	5351 0108h

Figure 4-324. STC_CORE2_CURMISR_23 Name Register

31	30	29	28	27	26	25	24
C2MISR23							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR23							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR23							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR23							
R							
0h							

Table 4-673. STC_CORE2_CURMISR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR23	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.325 STC_CORE2_CURMISR_24 Register

4.1.2.325.1 STC_CORE2_CURMISR_24 Register (Offset = 10Ch) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-674. Instance Table

Instance Name	Physical Address
R5SS0	5350 010Ch
R5SS1	5351 010Ch

Figure 4-325. STC_CORE2_CURMISR_24 Name Register

31	30	29	28	27	26	25	24
C2MISR24							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR24							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR24							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR24							
R							
0h							

Table 4-675. STC_CORE2_CURMISR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR24	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.326 STC_CORE2_CURMISR_25 Register

4.1.2.326.1 STC_CORE2_CURMISR_25 Register (Offset = 110h) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-676. Instance Table

Instance Name	Physical Address
R5SS0	5350 0110h
R5SS1	5351 0110h

Figure 4-326. STC_CORE2_CURMISR_25 Name Register

31	30	29	28	27	26	25	24
C2MISR25							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR25							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR25							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR25							
R							
0h							

Table 4-677. STC_CORE2_CURMISR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR25	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.327 STC_CORE2_CURMISR_26 Register

4.1.2.327.1 STC_CORE2_CURMISR_26 Register (Offset = 114h) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-678. Instance Table

Instance Name	Physical Address
R5SS0	5350 0114h
R5SS1	5351 0114h

Figure 4-327. STC_CORE2_CURMISR_26 Name Register

31	30	29	28	27	26	25	24
C2MISR26							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR26							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR26							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR26							
R							
0h							

Table 4-679. STC_CORE2_CURMISR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR26	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.328 STC_CORE2_CURMISR_27 Register

4.1.2.328.1 STC_CORE2_CURMISR_27 Register (Offset = 118h) [reset = 0h]

Holds the MISR signature for CORE2.

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Table 4-680. Instance Table

Instance Name	Physical Address
R5SS0	5350 0118h
R5SS1	5351 0118h

Figure 4-328. STC_CORE2_CURMISR_27 Name Register

31	30	29	28	27	26	25	24
C2MISR27							
R							
0h							
23	22	21	20	19	18	17	16
C2MISR27							
R							
0h							
15	14	13	12	11	10	9	8
C2MISR27							
R							
0h							
7	6	5	4	3	2	1	0
C2MISR27							
R							
0h							

Table 4-681. STC_CORE2_CURMISR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	C2MISR27	R	0h	MISR Signature for CORE2 This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.1.2.329 ICACHE_CORE0_START Register

4.1.2.329.1 ICACHE_CORE0_START Register (Offset = 0h) [reset = 0h]

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Table 4-682. Instance Table

Instance Name	Physical Address
R5SS0	7400 0000h
R5SS1	7600 0000h

Figure 4-329. ICACHE_CORE0_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-683. ICACHE_CORE0_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	Memory start address

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4.1.2.330 ICACHE_CORE0_END Register

4.1.2.330.1 ICACHE_CORE0_END Register (Offset = 7FFFFCh) [reset = 0h]

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Table 4-684. Instance Table

Instance Name	Physical Address
R5SS0	747F FFFCh
R5SS1	767F FFFCh

Figure 4-330. ICACHE_CORE0_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-685. ICACHE_CORE0_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	Memory end address

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4.1.2.331 DCACHE_CORE0_START Register

4.1.2.331.1 DCACHE_CORE0_START Register (Offset = 0h) [reset = 0h]

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Table 4-686. Instance Table

Instance Name	Physical Address
R5SS0	7480 0000h
R5SS1	7680 0000h

Figure 4-331. DCACHE_CORE0_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-687. DCACHE_CORE0_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	Memory start address

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4.1.2.332 DCACHE_CORE0_END Register

4.1.2.332.1 DCACHE_CORE0_END Register (Offset = 7FFFFCh) [reset = 0h]

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Table 4-688. Instance Table

Instance Name	Physical Address
R5SS0	74FF FFFCh
R5SS1	76FF FFFCh

Figure 4-332. DCACHE_CORE0_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-689. DCACHE_CORE0_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	Memory end address

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4.1.2.333 ICACHE_CORE1_START Register

4.1.2.333.1 ICACHE_CORE1_START Register (Offset = 0h) [reset = 0h]

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Table 4-690. Instance Table

Instance Name	Physical Address
R5SS0	7500 0000h
R5SS1	7700 0000h

Figure 4-333. ICACHE_CORE1_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-691. ICACHE_CORE1_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	Memory start address

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4.1.2.334 ICACHE_CORE1_END Register

4.1.2.334.1 ICACHE_CORE1_END Register (Offset = 7FFFFCh) [reset = 0h]

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Table 4-692. Instance Table

Instance Name	Physical Address
R5SS0	757F FFFCh
R5SS1	777F FFFCh

Figure 4-334. ICACHE_CORE1_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-693. ICACHE_CORE1_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	Memory end address

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4.1.2.335 DCACHE_CORE1_START Register

4.1.2.335.1 DCACHE_CORE1_START Register (Offset = 0h) [reset = 0h]

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Table 4-694. Instance Table

Instance Name	Physical Address
R5SS0	7580 0000h
R5SS1	7780 0000h

Figure 4-335. DCACHE_CORE1_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-695. DCACHE_CORE1_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	Memory start address

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4.1.2.336 DCACHE_CORE1_END Register

4.1.2.336.1 DCACHE_CORE1_END Register (Offset = 7FFFFCh) [reset = 0h]

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Table 4-696. Instance Table

Instance Name	Physical Address
R5SS0	75FF FFFCh
R5SS1	77FF FFFCh

Figure 4-336. DCACHE_CORE1_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-697. DCACHE_CORE1_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	Memory end address

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4.1.2.337 TCMA_CORE0_START Register

4.1.2.337.1 TCMA_CORE0_START Register (Offset = 0h) [reset = 0h]

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Table 4-698. Instance Table

Instance Name	Physical Address
R5SS0	7800 0000h
R5SS1	7840 0000h

Figure 4-337. TCMA_CORE0_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-699. TCMA_CORE0_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMA start address

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4.1.2.338 TCMA_CORE0_END Register

4.1.2.338.1 TCMA_CORE0_END Register (Offset = 27FFCh) [reset = 0h]

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Table 4-700. Instance Table

Instance Name	Physical Address
R5SS0	7802 7FFCh
R5SS1	7842 7FFCh

Figure 4-338. TCMA_CORE0_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-701. TCMA_CORE0_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMA end address

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4.1.2.339 TMU_EXT_CORE0_REVISION Register

4.1.2.339.1 TMU_EXT_CORE0_REVISION Register (Offset = 0h) [reset = 40000000h]

IP revision id register.

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Table 4-702. Instance Table

Instance Name	Physical Address
R5SS0	7806 0000h
R5SS1	7846 0000h

Figure 4-339. TMU_EXT_CORE0_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED_1		FUNC			
R		R		R			
1h		0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 4-703. TMU_EXT_CORE0_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	This identifies the scheme revision ID register type implemented for this module
29:28	RESERVED_1	R	0h	Reserved
27:16	FUNC	R	0h	Functional Release Number Reflects software-compatability. If there is no software compatability, a unique func number is assigned; for compatible modules, the same number is maintained.
15:11	RTL	R	0h	Design Release Number Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented.
10:8	MAJOR	R	0h	Major Revision Number Represents major changes to the module [e.g. entirely new features are added/changed]. The major revision number for this module.
7:6	CUSTOM	R	0h	Custom Module Number Indicates a special version of the module. May not be supported by standard software.
5:0	MINOR	R	0h	Minor Revision Number Represents minor changes to the module [e.g. enhancements to existing features]. The minor revision number for this module.

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4.1.2.340 TMU_EXT_CORE0_SINPUF32_R0 Register

4.1.2.340.1 TMU_EXT_CORE0_SINPUF32_R0 Register (Offset = 40h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-704. Instance Table

Instance Name	Physical Address
R5SS0	7806 0040h
R5SS1	7846 0040h

Figure 4-340. TMU_EXT_CORE0_SINPUF32_R0 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R0							
R/W							
0h							

Table 4-705. TMU_EXT_CORE0_SINPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R0

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4.1.2.341 TMU_EXT_CORE0_SINPUF32_R1 Register

4.1.2.341.1 TMU_EXT_CORE0_SINPUF32_R1 Register (Offset = 48h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-706. Instance Table

Instance Name	Physical Address
R5SS0	7806 0048h
R5SS1	7846 0048h

Figure 4-341. TMU_EXT_CORE0_SINPUF32_R1 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R1							
R/W							
0h							

Table 4-707. TMU_EXT_CORE0_SINPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R1

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4.1.2.342 TMU_EXT_CORE0_SINPUF32_R2 Register

4.1.2.342.1 TMU_EXT_CORE0_SINPUF32_R2 Register (Offset = 50h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-708. Instance Table

Instance Name	Physical Address
R5SS0	7806 0050h
R5SS1	7846 0050h

Figure 4-342. TMU_EXT_CORE0_SINPUF32_R2 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R2							
R/W							
0h							

Table 4-709. TMU_EXT_CORE0_SINPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R2

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4.1.2.343 TMU_EXT_CORE0_SINPUF32_R3 Register

4.1.2.343.1 TMU_EXT_CORE0_SINPUF32_R3 Register (Offset = 58h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-710. Instance Table

Instance Name	Physical Address
R5SS0	7806 0058h
R5SS1	7846 0058h

Figure 4-343. TMU_EXT_CORE0_SINPUF32_R3 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R3							
R/W							
0h							

Table 4-711. TMU_EXT_CORE0_SINPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R3

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4.1.2.344 TMU_EXT_CORE0_SINPUF32_R4 Register

4.1.2.344.1 TMU_EXT_CORE0_SINPUF32_R4 Register (Offset = 60h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-712. Instance Table

Instance Name	Physical Address
R5SS0	7806 0060h
R5SS1	7846 0060h

Figure 4-344. TMU_EXT_CORE0_SINPUF32_R4 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R4							
R/W							
0h							

Table 4-713. TMU_EXT_CORE0_SINPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R4

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4.1.2.345 TMU_EXT_CORE0_SINPUF32_R5 Register

4.1.2.345.1 TMU_EXT_CORE0_SINPUF32_R5 Register (Offset = 68h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R5.

Return to Summary Table

Table 4-714. Instance Table

Instance Name	Physical Address
R5SS0	7806 0068h
R5SS1	7846 0068h

Figure 4-345. TMU_EXT_CORE0_SINPUF32_R5 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R5							
R/W							
0h							

Table 4-715. TMU_EXT_CORE0_SINPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R5

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4.1.2.346 TMU_EXT_CORE0_SINPUF32_R6 Register

4.1.2.346.1 TMU_EXT_CORE0_SINPUF32_R6 Register (Offset = 70h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-716. Instance Table

Instance Name	Physical Address
R5SS0	7806 0070h
R5SS1	7846 0070h

Figure 4-346. TMU_EXT_CORE0_SINPUF32_R6 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R6							
R/W							
0h							

Table 4-717. TMU_EXT_CORE0_SINPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R6

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4.1.2.347 TMU_EXT_CORE0_SINPUF32_R7 Register

4.1.2.347.1 TMU_EXT_CORE0_SINPUF32_R7 Register (Offset = 78h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-718. Instance Table

Instance Name	Physical Address
R5SS0	7806 0078h
R5SS1	7846 0078h

Figure 4-347. TMU_EXT_CORE0_SINPUF32_R7 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R7							
R/W							
0h							

Table 4-719. TMU_EXT_CORE0_SINPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R7

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4.1.2.348 TMU_EXT_CORE0_COSPUF32_R0 Register

4.1.2.348.1 TMU_EXT_CORE0_COSPUF32_R0 Register (Offset = 80h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-720. Instance Table

Instance Name	Physical Address
R5SS0	7806 0080h
R5SS1	7846 0080h

Figure 4-348. TMU_EXT_CORE0_COSPUF32_R0 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R0							
R/W							
0h							

Table 4-721. TMU_EXT_CORE0_COSPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R0

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4.1.2.349 TMU_EXT_CORE0_COSPUF32_R1 Register

4.1.2.349.1 TMU_EXT_CORE0_COSPUF32_R1 Register (Offset = 88h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-722. Instance Table

Instance Name	Physical Address
R5SS0	7806 0088h
R5SS1	7846 0088h

Figure 4-349. TMU_EXT_CORE0_COSPUF32_R1 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R1							
R/W							
0h							

Table 4-723. TMU_EXT_CORE0_COSPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R1

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4.1.2.350 TMU_EXT_CORE0_COSPUF32_R2 Register

4.1.2.350.1 TMU_EXT_CORE0_COSPUF32_R2 Register (Offset = 90h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-724. Instance Table

Instance Name	Physical Address
R5SS0	7806 0090h
R5SS1	7846 0090h

Figure 4-350. TMU_EXT_CORE0_COSPUF32_R2 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R2							
R/W							
0h							

Table 4-725. TMU_EXT_CORE0_COSPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R2

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4.1.2.351 TMU_EXT_CORE0_COSPUF32_R3 Register

4.1.2.351.1 TMU_EXT_CORE0_COSPUF32_R3 Register (Offset = 98h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R3.

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Table 4-726. Instance Table

Instance Name	Physical Address
R5SS0	7806 0098h
R5SS1	7846 0098h

Figure 4-351. TMU_EXT_CORE0_COSPUF32_R3 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R3							
R/W							
0h							

Table 4-727. TMU_EXT_CORE0_COSPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R3

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4.1.2.352 TMU_EXT_CORE0_COSPUF32_R4 Register

4.1.2.352.1 TMU_EXT_CORE0_COSPUF32_R4 Register (Offset = A0h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-728. Instance Table

Instance Name	Physical Address
R5SS0	7806 00A0h
R5SS1	7846 00A0h

Figure 4-352. TMU_EXT_CORE0_COSPUF32_R4 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R4							
R/W							
0h							

Table 4-729. TMU_EXT_CORE0_COSPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R4

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4.1.2.353 TMU_EXT_CORE0_COSPUF32_R5 Register

4.1.2.353.1 TMU_EXT_CORE0_COSPUF32_R5 Register (Offset = A8h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R5.

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Table 4-730. Instance Table

Instance Name	Physical Address
R5SS0	7806 00A8h
R5SS1	7846 00A8h

Figure 4-353. TMU_EXT_CORE0_COSPUF32_R5 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R5							
R/W							
0h							

Table 4-731. TMU_EXT_CORE0_COSPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R5

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4.1.2.354 TMU_EXT_CORE0_COSPUF32_R6 Register

4.1.2.354.1 TMU_EXT_CORE0_COSPUF32_R6 Register (Offset = B0h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-732. Instance Table

Instance Name	Physical Address
R5SS0	7806 00B0h
R5SS1	7846 00B0h

Figure 4-354. TMU_EXT_CORE0_COSPUF32_R6 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R6							
R/W							
0h							

Table 4-733. TMU_EXT_CORE0_COSPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R6

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4.1.2.355 TMU_EXT_CORE0_COSPUF32_R7 Register

4.1.2.355.1 TMU_EXT_CORE0_COSPUF32_R7 Register (Offset = B8h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-734. Instance Table

Instance Name	Physical Address
R5SS0	7806 00B8h
R5SS1	7846 00B8h

Figure 4-355. TMU_EXT_CORE0_COSPUF32_R7 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R7							
R/W							
0h							

Table 4-735. TMU_EXT_CORE0_COSPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R7

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4.1.2.356 TMU_EXT_CORE0_ATANPUF32_R0 Register

4.1.2.356.1 TMU_EXT_CORE0_ATANPUF32_R0 Register (Offset = C0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-736. Instance Table

Instance Name	Physical Address
R5SS0	7806 00C0h
R5SS1	7846 00C0h

Figure 4-356. TMU_EXT_CORE0_ATANPUF32_R0 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ATANPUF32_R0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ATANPUF32_R0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ATANPUF32_R0							
R/W							
0h							

Table 4-737. TMU_EXT_CORE0_ATANPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R0

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4.1.2.357 TMU_EXT_CORE0_ATANPUF32_R1 Register

4.1.2.357.1 TMU_EXT_CORE0_ATANPUF32_R1 Register (Offset = C8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-738. Instance Table

Instance Name	Physical Address
R5SS0	7806 00C8h
R5SS1	7846 00C8h

Figure 4-357. TMU_EXT_CORE0_ATANPUF32_R1 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R1							
R/W							
0h							

Table 4-739. TMU_EXT_CORE0_ATANPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R1

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4.1.2.358 TMU_EXT_CORE0_ATANPUF32_R2 Register

4.1.2.358.1 TMU_EXT_CORE0_ATANPUF32_R2 Register (Offset = D0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-740. Instance Table

Instance Name	Physical Address
R5SS0	7806 00D0h
R5SS1	7846 00D0h

Figure 4-358. TMU_EXT_CORE0_ATANPUF32_R2 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R2							
R/W							
0h							

Table 4-741. TMU_EXT_CORE0_ATANPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R2

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4.1.2.359 TMU_EXT_CORE0_ATANPUF32_R3 Register

4.1.2.359.1 TMU_EXT_CORE0_ATANPUF32_R3 Register (Offset = D8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-742. Instance Table

Instance Name	Physical Address
R5SS0	7806 00D8h
R5SS1	7846 00D8h

Figure 4-359. TMU_EXT_CORE0_ATANPUF32_R3 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R3							
R/W							
0h							

Table 4-743. TMU_EXT_CORE0_ATANPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R3

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4.1.2.360 TMU_EXT_CORE0_ATANPUF32_R4 Register

4.1.2.360.1 TMU_EXT_CORE0_ATANPUF32_R4 Register (Offset = E0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-744. Instance Table

Instance Name	Physical Address
R5SS0	7806 00E0h
R5SS1	7846 00E0h

Figure 4-360. TMU_EXT_CORE0_ATANPUF32_R4 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R4							
R/W							
0h							

Table 4-745. TMU_EXT_CORE0_ATANPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R4

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4.1.2.361 TMU_EXT_CORE0_ATANPUF32_R5 Register

4.1.2.361.1 TMU_EXT_CORE0_ATANPUF32_R5 Register (Offset = E8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R5.

Return to Summary Table

Table 4-746. Instance Table

Instance Name	Physical Address
R5SS0	7806 00E8h
R5SS1	7846 00E8h

Figure 4-361. TMU_EXT_CORE0_ATANPUF32_R5 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R5							
R/W							
0h							

Table 4-747. TMU_EXT_CORE0_ATANPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R5

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4.1.2.362 TMU_EXT_CORE0_ATANPUF32_R6 Register

4.1.2.362.1 TMU_EXT_CORE0_ATANPUF32_R6 Register (Offset = F0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-748. Instance Table

Instance Name	Physical Address
R5SS0	7806 00F0h
R5SS1	7846 00F0h

Figure 4-362. TMU_EXT_CORE0_ATANPUF32_R6 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R6							
R/W							
0h							

Table 4-749. TMU_EXT_CORE0_ATANPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R6

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4.1.2.363 TMU_EXT_CORE0_ATANPUF32_R7 Register

4.1.2.363.1 TMU_EXT_CORE0_ATANPUF32_R7 Register (Offset = F8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-750. Instance Table

Instance Name	Physical Address
R5SS0	7806 00F8h
R5SS1	7846 00F8h

Figure 4-363. TMU_EXT_CORE0_ATANPUF32_R7 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R7							
R/W							
0h							

Table 4-751. TMU_EXT_CORE0_ATANPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R7

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4.1.2.364 TMU_EXT_CORE0_IEXP2F32_R0 Register

4.1.2.364.1 TMU_EXT_CORE0_IEXP2F32_R0 Register (Offset = 140h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-752. Instance Table

Instance Name	Physical Address
R5SS0	7806 0140h
R5SS1	7846 0140h

Figure 4-364. TMU_EXT_CORE0_IEXP2F32_R0 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R0							
R/W							
0h							

Table 4-753. TMU_EXT_CORE0_IEXP2F32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R0

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4.1.2.365 TMU_EXT_CORE0_IEXP2F32_R1 Register

4.1.2.365.1 TMU_EXT_CORE0_IEXP2F32_R1 Register (Offset = 148h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-754. Instance Table

Instance Name	Physical Address
R5SS0	7806 0148h
R5SS1	7846 0148h

Figure 4-365. TMU_EXT_CORE0_IEXP2F32_R1 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R1							
R/W							
0h							

Table 4-755. TMU_EXT_CORE0_IEXP2F32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R1

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4.1.2.366 TMU_EXT_CORE0_IEXP2F32_R2 Register

4.1.2.366.1 TMU_EXT_CORE0_IEXP2F32_R2 Register (Offset = 150h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-756. Instance Table

Instance Name	Physical Address
R5SS0	7806 0150h
R5SS1	7846 0150h

Figure 4-366. TMU_EXT_CORE0_IEXP2F32_R2 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R2							
R/W							
0h							

Table 4-757. TMU_EXT_CORE0_IEXP2F32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R2

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4.1.2.367 TMU_EXT_CORE0_IEXP2F32_R3 Register

4.1.2.367.1 TMU_EXT_CORE0_IEXP2F32_R3 Register (Offset = 158h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-758. Instance Table

Instance Name	Physical Address
R5SS0	7806 0158h
R5SS1	7846 0158h

Figure 4-367. TMU_EXT_CORE0_IEXP2F32_R3 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R3							
R/W							
0h							

Table 4-759. TMU_EXT_CORE0_IEXP2F32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R3

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4.1.2.368 TMU_EXT_CORE0_IEXP2F32_R4 Register

4.1.2.368.1 TMU_EXT_CORE0_IEXP2F32_R4 Register (Offset = 160h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-760. Instance Table

Instance Name	Physical Address
R5SS0	7806 0160h
R5SS1	7846 0160h

Figure 4-368. TMU_EXT_CORE0_IEXP2F32_R4 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R4							
R/W							
0h							

Table 4-761. TMU_EXT_CORE0_IEXP2F32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R4

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4.1.2.369 TMU_EXT_CORE0_IEXP2F32_R5 Register

4.1.2.369.1 TMU_EXT_CORE0_IEXP2F32_R5 Register (Offset = 168h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R5.

Return to Summary Table

Table 4-762. Instance Table

Instance Name	Physical Address
R5SS0	7806 0168h
R5SS1	7846 0168h

Figure 4-369. TMU_EXT_CORE0_IEXP2F32_R5 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R5							
R/W							
0h							

Table 4-763. TMU_EXT_CORE0_IEXP2F32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R5

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4.1.2.370 TMU_EXT_CORE0_IEXP2F32_R6 Register

4.1.2.370.1 TMU_EXT_CORE0_IEXP2F32_R6 Register (Offset = 170h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-764. Instance Table

Instance Name	Physical Address
R5SS0	7806 0170h
R5SS1	7846 0170h

Figure 4-370. TMU_EXT_CORE0_IEXP2F32_R6 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R6							
R/W							
0h							

Table 4-765. TMU_EXT_CORE0_IEXP2F32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R6

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4.1.2.371 TMU_EXT_CORE0_IEXP2F32_R7 Register

4.1.2.371.1 TMU_EXT_CORE0_IEXP2F32_R7 Register (Offset = 178h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-766. Instance Table

Instance Name	Physical Address
R5SS0	7806 0178h
R5SS1	7846 0178h

Figure 4-371. TMU_EXT_CORE0_IEXP2F32_R7 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R7							
R/W							
0h							

Table 4-767. TMU_EXT_CORE0_IEXP2F32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R7

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4.1.2.372 TMU_EXT_CORE0_LOG2F32_R0 Register

4.1.2.372.1 TMU_EXT_CORE0_LOG2F32_R0 Register (Offset = 180h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-768. Instance Table

Instance Name	Physical Address
R5SS0	7806 0180h
R5SS1	7846 0180h

Figure 4-372. TMU_EXT_CORE0_LOG2F32_R0 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R0							
R/W							
0h							

Table 4-769. TMU_EXT_CORE0_LOG2F32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R0

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4.1.2.373 TMU_EXT_CORE0_LOG2F32_R1 Register

4.1.2.373.1 TMU_EXT_CORE0_LOG2F32_R1 Register (Offset = 188h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-770. Instance Table

Instance Name	Physical Address
R5SS0	7806 0188h
R5SS1	7846 0188h

Figure 4-373. TMU_EXT_CORE0_LOG2F32_R1 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R1							
R/W							
0h							

Table 4-771. TMU_EXT_CORE0_LOG2F32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R1

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4.1.2.374 TMU_EXT_CORE0_LOG2F32_R2 Register

4.1.2.374.1 TMU_EXT_CORE0_LOG2F32_R2 Register (Offset = 190h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-772. Instance Table

Instance Name	Physical Address
R5SS0	7806 0190h
R5SS1	7846 0190h

Figure 4-374. TMU_EXT_CORE0_LOG2F32_R2 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R2							
R/W							
0h							

Table 4-773. TMU_EXT_CORE0_LOG2F32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R2

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4.1.2.375 TMU_EXT_CORE0_LOG2F32_R3 Register

4.1.2.375.1 TMU_EXT_CORE0_LOG2F32_R3 Register (Offset = 198h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-774. Instance Table

Instance Name	Physical Address
R5SS0	7806 0198h
R5SS1	7846 0198h

Figure 4-375. TMU_EXT_CORE0_LOG2F32_R3 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R3							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LOG2F32_R3							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
LOG2F32_R3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOG2F32_R3							
R/W							
0h							

Table 4-775. TMU_EXT_CORE0_LOG2F32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R3

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4.1.2.376 TMU_EXT_CORE0_LOG2F32_R4 Register

4.1.2.376.1 TMU_EXT_CORE0_LOG2F32_R4 Register (Offset = 1A0h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-776. Instance Table

Instance Name	Physical Address
R5SS0	7806 01A0h
R5SS1	7846 01A0h

Figure 4-376. TMU_EXT_CORE0_LOG2F32_R4 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R4							
R/W							
0h							

Table 4-777. TMU_EXT_CORE0_LOG2F32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R4

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4.1.2.377 TMU_EXT_CORE0_LOG2F32_R5 Register

4.1.2.377.1 TMU_EXT_CORE0_LOG2F32_R5 Register (Offset = 1A8h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R5.

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Table 4-778. Instance Table

Instance Name	Physical Address
R5SS0	7806 01A8h
R5SS1	7846 01A8h

Figure 4-377. TMU_EXT_CORE0_LOG2F32_R5 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R5							
R/W							
0h							

Table 4-779. TMU_EXT_CORE0_LOG2F32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R5

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4.1.2.378 TMU_EXT_CORE0_LOG2F32_R6 Register

4.1.2.378.1 TMU_EXT_CORE0_LOG2F32_R6 Register (Offset = 1B0h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-780. Instance Table

Instance Name	Physical Address
R5SS0	7806 01B0h
R5SS1	7846 01B0h

Figure 4-378. TMU_EXT_CORE0_LOG2F32_R6 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R6							
R/W							
0h							

Table 4-781. TMU_EXT_CORE0_LOG2F32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R6

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4.1.2.379 TMU_EXT_CORE0_LOG2F32_R7 Register

4.1.2.379.1 TMU_EXT_CORE0_LOG2F32_R7 Register (Offset = 1B8h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R7.

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Table 4-782. Instance Table

Instance Name	Physical Address
R5SS0	7806 01B8h
R5SS1	7846 01B8h

Figure 4-379. TMU_EXT_CORE0_LOG2F32_R7 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R7							
R/W							
0h							

Table 4-783. TMU_EXT_CORE0_LOG2F32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R7

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4.1.2.380 TMU_EXT_CORE0_QUADF32_X_R0_R1 Register

4.1.2.380.1 TMU_EXT_CORE0_QUADF32_X_R0_R1 Register (Offset = 1C0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R0 and R1.

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Table 4-784. Instance Table

Instance Name	Physical Address
R5SS0	7806 01C0h
R5SS1	7846 01C0h

Figure 4-380. TMU_EXT_CORE0_QUADF32_X_R0_R1 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R0_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R0_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R0_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R0_R1							
R/W							
0h							

Table 4-785. TMU_EXT_CORE0_QUADF32_X_R0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R0_R1	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R0 and R1

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4.1.2.381 TMU_EXT_CORE0_QUADF32_X_R1_R2 Register

4.1.2.381.1 TMU_EXT_CORE0_QUADF32_X_R1_R2 Register (Offset = 1C8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R1 and R2.

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Table 4-786. Instance Table

Instance Name	Physical Address
R5SS0	7806 01C8h
R5SS1	7846 01C8h

Figure 4-381. TMU_EXT_CORE0_QUADF32_X_R1_R2 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R1_R2							
R/W							
0h							

Table 4-787. TMU_EXT_CORE0_QUADF32_X_R1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R1_R2	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R1 and R2

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4.1.2.382 TMU_EXT_CORE0_QUADF32_X_R2_R3 Register

4.1.2.382.1 TMU_EXT_CORE0_QUADF32_X_R2_R3 Register (Offset = 1D0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R2 and R3.

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Table 4-788. Instance Table

Instance Name	Physical Address
R5SS0	7806 01D0h
R5SS1	7846 01D0h

Figure 4-382. TMU_EXT_CORE0_QUADF32_X_R2_R3 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R2_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R2_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R2_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R2_R3							
R/W							
0h							

Table 4-789. TMU_EXT_CORE0_QUADF32_X_R2_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R2_R3	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R2 and R3

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4.1.2.383 TMU_EXT_CORE0_QUADF32_X_R3_R4 Register

4.1.2.383.1 TMU_EXT_CORE0_QUADF32_X_R3_R4 Register (Offset = 1D8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R3 and R4.

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Table 4-790. Instance Table

Instance Name	Physical Address
R5SS0	7806 01D8h
R5SS1	7846 01D8h

Figure 4-383. TMU_EXT_CORE0_QUADF32_X_R3_R4 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R3_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R3_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R3_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R3_R4							
R/W							
0h							

Table 4-791. TMU_EXT_CORE0_QUADF32_X_R3_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R3_R4	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R3 and R4

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4.1.2.384 TMU_EXT_CORE0_QUADF32_X_R4_R5 Register

4.1.2.384.1 TMU_EXT_CORE0_QUADF32_X_R4_R5 Register (Offset = 1E0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R4 and R5.

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Table 4-792. Instance Table

Instance Name	Physical Address
R5SS0	7806 01E0h
R5SS1	7846 01E0h

Figure 4-384. TMU_EXT_CORE0_QUADF32_X_R4_R5 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R4_R5							
R/W							
0h							

Table 4-793. TMU_EXT_CORE0_QUADF32_X_R4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R4_R5	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R4 and R5

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4.1.2.385 TMU_EXT_CORE0_QUADF32_X_R5SS0_R6 Register

4.1.2.385.1 TMU_EXT_CORE0_QUADF32_X_R5SS0_R6 Register (Offset = 1E8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R5 and R6.

Return to Summary Table

Table 4-794. Instance Table

Instance Name	Physical Address
R5SS0	7806 01E8h
R5SS1	7846 01E8h

Figure 4-385. TMU_EXT_CORE0_QUADF32_X_R5SS0_R6 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R5_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R5_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R5_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R5_R6							
R/W							
0h							

Table 4-795. TMU_EXT_CORE0_QUADF32_X_R5SS0_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R5_R6	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R5 and R6

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4.1.2.386 TMU_EXT_CORE0_QUADF32_X_R6_R7 Register

4.1.2.386.1 TMU_EXT_CORE0_QUADF32_X_R6_R7 Register (Offset = 1F0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R6 and R7.

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Table 4-796. Instance Table

Instance Name	Physical Address
R5SS0	7806 01F0h
R5SS1	7846 01F0h

Figure 4-386. TMU_EXT_CORE0_QUADF32_X_R6_R7 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R6_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R6_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R6_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R6_R7							
R/W							
0h							

Table 4-797. TMU_EXT_CORE0_QUADF32_X_R6_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R6_R7	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R6 and R7

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4.1.2.387 TMU_EXT_CORE0_RESULT_R0 Register

4.1.2.387.1 TMU_EXT_CORE0_RESULT_R0 Register (Offset = 280h) [reset = 0h]

R0 result register.

Return to Summary Table

Table 4-798. Instance Table

Instance Name	Physical Address
R5SS0	7806 0280h
R5SS1	7846 0280h

Figure 4-387. TMU_EXT_CORE0_RESULT_R0 Name Register

31	30	29	28	27	26	25	24
R0							
R							
0h							
23	22	21	20	19	18	17	16
R0							
R							
0h							
15	14	13	12	11	10	9	8
R0							
R							
0h							
7	6	5	4	3	2	1	0
R0							
R							
0h							

Table 4-799. TMU_EXT_CORE0_RESULT_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R0	R	0h	R0 result register

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4.1.2.388 TMU_EXT_CORE0_RESULT_R1 Register

4.1.2.388.1 TMU_EXT_CORE0_RESULT_R1 Register (Offset = 288h) [reset = 0h]

R1 result register.

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Table 4-800. Instance Table

Instance Name	Physical Address
R5SS0	7806 0288h
R5SS1	7846 0288h

Figure 4-388. TMU_EXT_CORE0_RESULT_R1 Name Register

31	30	29	28	27	26	25	24
R1							
R							
0h							
23	22	21	20	19	18	17	16
R1							
R							
0h							
15	14	13	12	11	10	9	8
R1							
R							
0h							
7	6	5	4	3	2	1	0
R1							
R							
0h							

Table 4-801. TMU_EXT_CORE0_RESULT_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R1	R	0h	R1 result register

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4.1.2.389 TMU_EXT_CORE0_RESULT_R2 Register

4.1.2.389.1 TMU_EXT_CORE0_RESULT_R2 Register (Offset = 290h) [reset = 0h]

R2 result register.

Return to Summary Table

Table 4-802. Instance Table

Instance Name	Physical Address
R5SS0	7806 0290h
R5SS1	7846 0290h

Figure 4-389. TMU_EXT_CORE0_RESULT_R2 Name Register

31	30	29	28	27	26	25	24
R2							
R							
0h							
23	22	21	20	19	18	17	16
R2							
R							
0h							
15	14	13	12	11	10	9	8
R2							
R							
0h							
7	6	5	4	3	2	1	0
R2							
R							
0h							

Table 4-803. TMU_EXT_CORE0_RESULT_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R2	R	0h	R2 result register

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4.1.2.390 TMU_EXT_CORE0_RESULT_R3 Register

4.1.2.390.1 TMU_EXT_CORE0_RESULT_R3 Register (Offset = 298h) [reset = 0h]

R3 result register.

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Table 4-804. Instance Table

Instance Name	Physical Address
R5SS0	7806 0298h
R5SS1	7846 0298h

Figure 4-390. TMU_EXT_CORE0_RESULT_R3 Name Register

31	30	29	28	27	26	25	24
R3							
R							
0h							
23	22	21	20	19	18	17	16
R3							
R							
0h							
15	14	13	12	11	10	9	8
R3							
R							
0h							
7	6	5	4	3	2	1	0
R3							
R							
0h							

Table 4-805. TMU_EXT_CORE0_RESULT_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R3	R	0h	R3 result register

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4.1.2.391 TMU_EXT_CORE0_RESULT_R4 Register

4.1.2.391.1 TMU_EXT_CORE0_RESULT_R4 Register (Offset = 2A0h) [reset = 0h]

R4 result register.

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Table 4-806. Instance Table

Instance Name	Physical Address
R5SS0	7806 02A0h
R5SS1	7846 02A0h

Figure 4-391. TMU_EXT_CORE0_RESULT_R4 Name Register

31	30	29	28	27	26	25	24
R4							
R							
0h							
23	22	21	20	19	18	17	16
R4							
R							
0h							
15	14	13	12	11	10	9	8
R4							
R							
0h							
7	6	5	4	3	2	1	0
R4							
R							
0h							

Table 4-807. TMU_EXT_CORE0_RESULT_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R4	R	0h	R4 result register

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4.1.2.392 TMU_EXT_CORE0_RESULT_R5 Register

4.1.2.392.1 TMU_EXT_CORE0_RESULT_R5 Register (Offset = 2A8h) [reset = 0h]

R5 result register.

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Table 4-808. Instance Table

Instance Name	Physical Address
R5SS0	7806 02A8h
R5SS1	7846 02A8h

Figure 4-392. TMU_EXT_CORE0_RESULT_R5 Name Register

31	30	29	28	27	26	25	24
R5							
R							
0h							
23	22	21	20	19	18	17	16
R5							
R							
0h							
15	14	13	12	11	10	9	8
R5							
R							
0h							
7	6	5	4	3	2	1	0
R5							
R							
0h							

Table 4-809. TMU_EXT_CORE0_RESULT_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5	R	0h	R5 result register

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4.1.2.393 TMU_EXT_CORE0_RESULT_R6 Register

4.1.2.393.1 TMU_EXT_CORE0_RESULT_R6 Register (Offset = 2B0h) [reset = 0h]

R6 result register.

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Table 4-810. Instance Table

Instance Name	Physical Address
R5SS0	7806 02B0h
R5SS1	7846 02B0h

Figure 4-393. TMU_EXT_CORE0_RESULT_R6 Name Register

31	30	29	28	27	26	25	24
R6							
R							
0h							
23	22	21	20	19	18	17	16
R6							
R							
0h							
15	14	13	12	11	10	9	8
R6							
R							
0h							
7	6	5	4	3	2	1	0
R6							
R							
0h							

Table 4-811. TMU_EXT_CORE0_RESULT_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R6	R	0h	R6 result register

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4.1.2.394 TMU_EXT_CORE0_RESULT_R7 Register

4.1.2.394.1 TMU_EXT_CORE0_RESULT_R7 Register (Offset = 2B8h) [reset = 0h]

R7 result register.

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Table 4-812. Instance Table

Instance Name	Physical Address
R5SS0	7806 02B8h
R5SS1	7846 02B8h

Figure 4-394. TMU_EXT_CORE0_RESULT_R7 Name Register

31	30	29	28	27	26	25	24
R7							
R							
0h							
23	22	21	20	19	18	17	16
R7							
R							
0h							
15	14	13	12	11	10	9	8
R7							
R							
0h							
7	6	5	4	3	2	1	0
R7							
R							
0h							

Table 4-813. TMU_EXT_CORE0_RESULT_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R7	R	0h	R7 result register

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4.1.2.395 TMU_EXT_CORE0_CSAVE_R0 Register

4.1.2.395.1 TMU_EXT_CORE0_CSAVE_R0 Register (Offset = 2C0h) [reset = 0h]

Context save of R0 result register.

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Table 4-814. Instance Table

Instance Name	Physical Address
R5SS0	7806 02C0h
R5SS1	7846 02C0h

Figure 4-395. TMU_EXT_CORE0_CSAVE_R0 Name Register

31	30	29	28	27	26	25	24
CSAVE_R0							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R0							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R0							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R0							
R							
0h							

Table 4-815. TMU_EXT_CORE0_CSAVE_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R0	R	0h	Context save of R0 result register

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4.1.2.396 TMU_EXT_CORE0_CSAVE_R1 Register

4.1.2.396.1 TMU_EXT_CORE0_CSAVE_R1 Register (Offset = 2C8h) [reset = 0h]

Context save of R1 result register.

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Table 4-816. Instance Table

Instance Name	Physical Address
R5SS0	7806 02C8h
R5SS1	7846 02C8h

Figure 4-396. TMU_EXT_CORE0_CSAVE_R1 Name Register

31	30	29	28	27	26	25	24
CSAVE_R1							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R1							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R1							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R1							
R							
0h							

Table 4-817. TMU_EXT_CORE0_CSAVE_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R1	R	0h	Context save of R1 result register

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4.1.2.397 TMU_EXT_CORE0_CSAVE_R2 Register

4.1.2.397.1 TMU_EXT_CORE0_CSAVE_R2 Register (Offset = 2D0h) [reset = 0h]

Context save of R2 result register.

Return to Summary Table

Table 4-818. Instance Table

Instance Name	Physical Address
R5SS0	7806 02D0h
R5SS1	7846 02D0h

Figure 4-397. TMU_EXT_CORE0_CSAVE_R2 Name Register

31	30	29	28	27	26	25	24
CSAVE_R2							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R2							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R2							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R2							
R							
0h							

Table 4-819. TMU_EXT_CORE0_CSAVE_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R2	R	0h	Context save of R2 result register

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4.1.2.398 TMU_EXT_CORE0_CSAVE_R3 Register

4.1.2.398.1 TMU_EXT_CORE0_CSAVE_R3 Register (Offset = 2D8h) [reset = 0h]

Context save of R3 result register.

Return to Summary Table

Table 4-820. Instance Table

Instance Name	Physical Address
R5SS0	7806 02D8h
R5SS1	7846 02D8h

Figure 4-398. TMU_EXT_CORE0_CSAVE_R3 Name Register

31	30	29	28	27	26	25	24
CSAVE_R3							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R3							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R3							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R3							
R							
0h							

Table 4-821. TMU_EXT_CORE0_CSAVE_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R3	R	0h	Context save of R3 result register

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4.1.2.399 TMU_EXT_CORE0_CSAVE_R4 Register

4.1.2.399.1 TMU_EXT_CORE0_CSAVE_R4 Register (Offset = 2E0h) [reset = 0h]

Context save of R4 result register.

Return to Summary Table

Table 4-822. Instance Table

Instance Name	Physical Address
R5SS0	7806 02E0h
R5SS1	7846 02E0h

Figure 4-399. TMU_EXT_CORE0_CSAVE_R4 Name Register

31	30	29	28	27	26	25	24
CSAVE_R4							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R4							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R4							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R4							
R							
0h							

Table 4-823. TMU_EXT_CORE0_CSAVE_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R4	R	0h	Context save of R4 result register

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4.1.2.400 TMU_EXT_CORE0_CSAVE_R5 Register

4.1.2.400.1 TMU_EXT_CORE0_CSAVE_R5 Register (Offset = 2E8h) [reset = 0h]

Context save of R5 result register.

Return to Summary Table

Table 4-824. Instance Table

Instance Name	Physical Address
R5SS0	7806 02E8h
R5SS1	7846 02E8h

Figure 4-400. TMU_EXT_CORE0_CSAVE_R5 Name Register

31	30	29	28	27	26	25	24
CSAVE_R5							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R5							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R5							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R5							
R							
0h							

Table 4-825. TMU_EXT_CORE0_CSAVE_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R5	R	0h	Context save of R5 result register

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4.1.2.401 TMU_EXT_CORE0_CSAVE_R6 Register

4.1.2.401.1 TMU_EXT_CORE0_CSAVE_R6 Register (Offset = 2F0h) [reset = 0h]

Context save of R6 result register.

Return to Summary Table

Table 4-826. Instance Table

Instance Name	Physical Address
R5SS0	7806 02F0h
R5SS1	7846 02F0h

Figure 4-401. TMU_EXT_CORE0_CSAVE_R6 Name Register

31	30	29	28	27	26	25	24
CSAVE_R6							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R6							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R6							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R6							
R							
0h							

Table 4-827. TMU_EXT_CORE0_CSAVE_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R6	R	0h	Context save of R6 result register

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4.1.2.402 TMU_EXT_CORE0_CSAVE_R7 Register

4.1.2.402.1 TMU_EXT_CORE0_CSAVE_R7 Register (Offset = 2F8h) [reset = 0h]

Context save of R7 result register.

Return to Summary Table

Table 4-828. Instance Table

Instance Name	Physical Address
R5SS0	7806 02F8h
R5SS1	7846 02F8h

Figure 4-402. TMU_EXT_CORE0_CSAVE_R7 Name Register

31	30	29	28	27	26	25	24
CSAVE_R7							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R7							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R7							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R7							
R							
0h							

Table 4-829. TMU_EXT_CORE0_CSAVE_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R7	R	0h	Context save of R7 result register

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4.1.2.403 TMU_EXT_CORE0_CSAVE_OP2 Register

4.1.2.403.1 TMU_EXT_CORE0_CSAVE_OP2 Register (Offset = 300h) [reset = 0h]

Context save of Operarand2 result register.

Return to Summary Table

Table 4-830. Instance Table

Instance Name	Physical Address
R5SS0	7806 0300h
R5SS1	7846 0300h

Figure 4-403. TMU_EXT_CORE0_CSAVE_OP2 Name Register

31	30	29	28	27	26	25	24
CSAVE_OP2							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_OP2							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_OP2							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_OP2							
R							
0h							

Table 4-831. TMU_EXT_CORE0_CSAVE_OP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_OP2	R	0h	Context save of operand 2 [OP2] result register

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4.1.2.404 TMU_EXT_CORE0_CONTEXT_SAVE Register

4.1.2.404.1 TMU_EXT_CORE0_CONTEXT_SAVE Register (Offset = 308h) [reset = 0h]

Register to initiate context save of result registers.

Return to Summary Table

Table 4-832. Instance Table

Instance Name	Physical Address
R5SS0	7806 0308h
R5SS1	7846 0308h

Figure 4-404. TMU_EXT_CORE0_CONTEXT_SAVE Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							SAVE
R							R/W1TS
0h							0h

Table 4-833. TMU_EXT_CORE0_CONTEXT_SAVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	SAVE	R/W1TS	0h	Writing one will initiate context save. Context save will be done only after completion all operations initiated by master before context save was issued. Results registers R0 to R3 and Operand2 will be saved. Note: Contex is saved within IP, not to external memory.

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4.1.2.405 TMU_EXT_CORE0_CONTEXT_RESTORE Register

4.1.2.405.1 TMU_EXT_CORE0_CONTEXT_RESTORE Register (Offset = 310h) [reset = 0h]

Register to initiate context restore of result registers.

Return to Summary Table

Table 4-834. Instance Table

Instance Name	Physical Address
R5SS0	7806 0310h
R5SS1	7846 0310h

Figure 4-405. TMU_EXT_CORE0_CONTEXT_RESTORE Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							RESTORE
R							R/W1TS
0h							0h

Table 4-835. TMU_EXT_CORE0_CONTEXT_RESTORE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	RESTORE	R/W1TS	0h	Writing one will initiate context restore. Results registers R0 to R3 and Operand2 will be restored.

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4.1.2.406 TMU_EXT_CORE0_STF Register

4.1.2.406.1 TMU_EXT_CORE0_STF Register (Offset = 348h) [reset = 0h]

TMU status Register.

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Table 4-836. Instance Table

Instance Name	Physical Address
R5SS0	7806 0348h
R5SS1	7846 0348h

Figure 4-406. TMU_EXT_CORE0_STF Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2						LUF_WR_EN	LVF_WR_EN
R						R	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						LUF	LVF
R						R/W	R/W
0h						0h	0h

Table 4-837. TMU_EXT_CORE0_STF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_2	R	0h	Reserved
9	LUF_WR_EN	R	0h	Always read as zero, Value is written to this bit either enables/ disables write to LVF [[br] 0:Disbles write to LUF 1:Enables write to LUF
8	LVF_WR_EN	R	0h	Always read as zero, Value is written to this bit either enables/ disables write to LVF [[br] 0:Disbles write to LVF 1:Enables write to LVF
7:2	RESERVED_1	R	0h	Reserved
1	LUF	R/W	0h	Is set to '1' when a TMU operation results in LVF. It is sticky bit, once set, it remains set until it is cleared with write. It can be written only when LUF_WR_EN Is written with '1'
0	LVF	R/W	0h	Is set to '1' when a TMU operation results in LVF. It is sticky bit, once set, it remains set until it is cleared with write. It can be written only when LVF_WR_EN Is written with '1'

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4.1.2.407 TMU_EXT_CORE0_PARITY_TEST Register

4.1.2.407.1 TMU_EXT_CORE0_PARITY_TEST Register (Offset = 380h) [reset = 0h]

Enabling the parity test feature.

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Table 4-838. Instance Table

Instance Name	Physical Address
R5SS0	7806 0380h
R5SS1	7846 0380h

Figure 4-407. TMU_EXT_CORE0_PARITY_TEST Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				TESTEN			
R				R/W			
0h				0h			

Table 4-839. TMU_EXT_CORE0_PARITY_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:4	RESERVED_1	R	0h	Reserved
3:0	TESTEN	R/W	0h	1010: Parity test feature is enabled All other values: Parity test feature is disabled Note: When the parity test feature is enabled, acutal registers are not accessible in the memory map. Instead, the parity values are accessible. Parity is computed for every byte and the correponding parity value is available at the bit-0 of every byte. Value of '1' written to the parity bit after enabling the parity test feature can be used to inject the error by inverting the stored parity value.

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4.1.2.408 TMU_EXT_CORE0_LCM_LOCK Register

4.1.2.408.1 TMU_EXT_CORE0_LCM_LOCK Register (Offset = 390h) [reset = 0h]

LCM lock configuration.

Return to Summary Table

Table 4-840. Instance Table

Instance Name	Physical Address
R5SS0	7806 0390h
R5SS1	7846 0390h

Figure 4-408. TMU_EXT_CORE0_LCM_LOCK Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							PARITY_TEST
R							R/W
0h							0h

Table 4-841. TMU_EXT_CORE0_LCM_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	PARITY_TEST	R/W	0h	0: Register configuration is not locked. [[br] 1:Register configuration is locked.

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4.1.2.409 TMU_EXT_CORE0_LCM_COMMIT Register

4.1.2.409.1 TMU_EXT_CORE0_LCM_COMMIT Register (Offset = 3A0h) [reset = 0h]

LCM commit configuration.

Return to Summary Table

Table 4-842. Instance Table

Instance Name	Physical Address
R5SS0	7806 03A0h
R5SS1	7846 03A0h

Figure 4-409. TMU_EXT_CORE0_LCM_COMMIT Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							PARITY_TEST
R							R/W1TS
0h							0h

Table 4-843. TMU_EXT_CORE0_LCM_COMMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	PARITY_TEST	R/W1TS	0h	0: Register lock configuration is not committed. [[br] 1:Register lock configuration is committed. Once configuration is committed, only reset can change the configuration.

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4.1.2.410 TCMB_CORE0_START Register

4.1.2.410.1 TCMB_CORE0_START Register (Offset = 0h) [reset = 0h]

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Table 4-844. Instance Table

Instance Name	Physical Address
R5SS0	7810 0000h
R5SS1	7850 0000h

Figure 4-410. TCMB_CORE0_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-845. TCMB_CORE0_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMB start address

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4.1.2.411 TCMB_CORE0_END Register

4.1.2.411.1 TCMB_CORE0_END Register (Offset = 2FFFCh) [reset = 0h]

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Table 4-846. Instance Table

Instance Name	Physical Address
R5SS0	7812 FFFCh
R5SS1	7852 FFFCh

Figure 4-411. TCMB_CORE0_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-847. TCMB_CORE0_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMB end address

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4.1.2.412 TCMA_CORE1_START Register

4.1.2.412.1 TCMA_CORE1_START Register (Offset = 0h) [reset = 0h]

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Table 4-848. Instance Table

Instance Name	Physical Address
R5SS0	7820 0000h
R5SS1	7860 0000h

Figure 4-412. TCMA_CORE1_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-849. TCMA_CORE1_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMA start address

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4.1.2.413 TCMA_CORE1_END Register

4.1.2.413.1 TCMA_CORE1_END Register (Offset = 7FFCh) [reset = 0h]

Return to Summary Table

Table 4-850. Instance Table

Instance Name	Physical Address
R5SS0	7820 7FFCh
R5SS1	7860 7FFCh

Figure 4-413. TCMA_CORE1_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-851. TCMA_CORE1_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMA end address

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4.1.2.414 TMU_EXT_CORE1_REVISION Register

4.1.2.414.1 TMU_EXT_CORE1_REVISION Register (Offset = 0h) [reset = 40000000h]

IP revision id register.

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Table 4-852. Instance Table

Instance Name	Physical Address
R5SS0	7826 0000h
R5SS1	7866 0000h

Figure 4-414. TMU_EXT_CORE1_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED_1		FUNC			
R		R		R			
1h		0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 4-853. TMU_EXT_CORE1_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	This identifies the scheme revision ID register type implemented for this module
29:28	RESERVED_1	R	0h	Reserved
27:16	FUNC	R	0h	Functional Release Number Reflects software-compatability. If there is no software compatability, a unique func number is assigned; for compatible modules, the same number is maintained.
15:11	RTL	R	0h	Design Release Number Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented.
10:8	MAJOR	R	0h	Major Revision Number Represents major changes to the module [e.g. entirely new features are added/changed]. The major revision number for this module.
7:6	CUSTOM	R	0h	Custom Module Number Indicates a special version of the module. May not be supported by standard software.
5:0	MINOR	R	0h	Minor Revision Number Represents minor changes to the module [e.g. enhancements to existing features]. The minor revision number for this module.

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4.1.2.415 TMU_EXT_CORE1_SINPUF32_R0 Register

4.1.2.415.1 TMU_EXT_CORE1_SINPUF32_R0 Register (Offset = 40h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R0.

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Table 4-854. Instance Table

Instance Name	Physical Address
R5SS0	7826 0040h
R5SS1	7866 0040h

Figure 4-415. TMU_EXT_CORE1_SINPUF32_R0 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R0							
R/W							
0h							

Table 4-855. TMU_EXT_CORE1_SINPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R0

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4.1.2.416 TMU_EXT_CORE1_SINPUF32_R1 Register

4.1.2.416.1 TMU_EXT_CORE1_SINPUF32_R1 Register (Offset = 48h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R1.

Return to Summary Table

Table 4-856. Instance Table

Instance Name	Physical Address
R5SS0	7826 0048h
R5SS1	7866 0048h

Figure 4-416. TMU_EXT_CORE1_SINPUF32_R1 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R1							
R/W							
0h							

Table 4-857. TMU_EXT_CORE1_SINPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R1

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4.1.2.417 TMU_EXT_CORE1_SINPUF32_R2 Register

4.1.2.417.1 TMU_EXT_CORE1_SINPUF32_R2 Register (Offset = 50h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-858. Instance Table

Instance Name	Physical Address
R5SS0	7826 0050h
R5SS1	7866 0050h

Figure 4-417. TMU_EXT_CORE1_SINPUF32_R2 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R2							
R/W							
0h							

Table 4-859. TMU_EXT_CORE1_SINPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R2

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4.1.2.418 TMU_EXT_CORE1_SINPUF32_R3 Register

4.1.2.418.1 TMU_EXT_CORE1_SINPUF32_R3 Register (Offset = 58h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-860. Instance Table

Instance Name	Physical Address
R5SS0	7826 0058h
R5SS1	7866 0058h

Figure 4-418. TMU_EXT_CORE1_SINPUF32_R3 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R3							
R/W							
0h							

Table 4-861. TMU_EXT_CORE1_SINPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R3

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4.1.2.419 TMU_EXT_CORE1_SINPUF32_R4 Register

4.1.2.419.1 TMU_EXT_CORE1_SINPUF32_R4 Register (Offset = 60h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-862. Instance Table

Instance Name	Physical Address
R5SS0	7826 0060h
R5SS1	7866 0060h

Figure 4-419. TMU_EXT_CORE1_SINPUF32_R4 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R4							
R/W							
0h							

Table 4-863. TMU_EXT_CORE1_SINPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R4

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4.1.2.420 TMU_EXT_CORE1_SINPUF32_R5 Register

4.1.2.420.1 TMU_EXT_CORE1_SINPUF32_R5 Register (Offset = 68h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R5.

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Table 4-864. Instance Table

Instance Name	Physical Address
R5SS0	7826 0068h
R5SS1	7866 0068h

Figure 4-420. TMU_EXT_CORE1_SINPUF32_R5 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R5							
R/W							
0h							

Table 4-865. TMU_EXT_CORE1_SINPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R5

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4.1.2.421 TMU_EXT_CORE1_SINPUF32_R6 Register

4.1.2.421.1 TMU_EXT_CORE1_SINPUF32_R6 Register (Offset = 70h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R6.

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Table 4-866. Instance Table

Instance Name	Physical Address
R5SS0	7826 0070h
R5SS1	7866 0070h

Figure 4-421. TMU_EXT_CORE1_SINPUF32_R6 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R6							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SINPUF32_R6							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SINPUF32_R6							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SINPUF32_R6							
R/W							
0h							

Table 4-867. TMU_EXT_CORE1_SINPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R6

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4.1.2.422 TMU_EXT_CORE1_SINPUF32_R7 Register

4.1.2.422.1 TMU_EXT_CORE1_SINPUF32_R7 Register (Offset = 78h) [reset = 0h]

Updates operand 1 for SINPUF32 operation. Result will be saved to R7.

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Table 4-868. Instance Table

Instance Name	Physical Address
R5SS0	7826 0078h
R5SS1	7866 0078h

Figure 4-422. TMU_EXT_CORE1_SINPUF32_R7 Name Register

31	30	29	28	27	26	25	24
SINPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
SINPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
SINPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
SINPUF32_R7							
R/W							
0h							

Table 4-869. TMU_EXT_CORE1_SINPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SINPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger SINPUF32 operation Result will be saved to R7

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4.1.2.423 TMU_EXT_CORE1_COSPUF32_R0 Register

4.1.2.423.1 TMU_EXT_CORE1_COSPUF32_R0 Register (Offset = 80h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R0.

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Table 4-870. Instance Table

Instance Name	Physical Address
R5SS0	7826 0080h
R5SS1	7866 0080h

Figure 4-423. TMU_EXT_CORE1_COSPUF32_R0 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R0							
R/W							
0h							

Table 4-871. TMU_EXT_CORE1_COSPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R0

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4.1.2.424 TMU_EXT_CORE1_COSPUF32_R1 Register

4.1.2.424.1 TMU_EXT_CORE1_COSPUF32_R1 Register (Offset = 88h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R1.

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Table 4-872. Instance Table

Instance Name	Physical Address
R5SS0	7826 0088h
R5SS1	7866 0088h

Figure 4-424. TMU_EXT_CORE1_COSPUF32_R1 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R1							
R/W							
0h							

Table 4-873. TMU_EXT_CORE1_COSPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R1

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4.1.2.425 TMU_EXT_CORE1_COSPUF32_R2 Register

4.1.2.425.1 TMU_EXT_CORE1_COSPUF32_R2 Register (Offset = 90h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R2.

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Table 4-874. Instance Table

Instance Name	Physical Address
R5SS0	7826 0090h
R5SS1	7866 0090h

Figure 4-425. TMU_EXT_CORE1_COSPUF32_R2 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R2							
R/W							
0h							

Table 4-875. TMU_EXT_CORE1_COSPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R2

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4.1.2.426 TMU_EXT_CORE1_COSPUF32_R3 Register

4.1.2.426.1 TMU_EXT_CORE1_COSPUF32_R3 Register (Offset = 98h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R3.

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Table 4-876. Instance Table

Instance Name	Physical Address
R5SS0	7826 0098h
R5SS1	7866 0098h

Figure 4-426. TMU_EXT_CORE1_COSPUF32_R3 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R3							
R/W							
0h							

Table 4-877. TMU_EXT_CORE1_COSPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R3

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4.1.2.427 TMU_EXT_CORE1_COSPUF32_R4 Register

4.1.2.427.1 TMU_EXT_CORE1_COSPUF32_R4 Register (Offset = A0h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R4.

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Table 4-878. Instance Table

Instance Name	Physical Address
R5SS0	7826 00A0h
R5SS1	7866 00A0h

Figure 4-427. TMU_EXT_CORE1_COSPUF32_R4 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R4							
R/W							
0h							

Table 4-879. TMU_EXT_CORE1_COSPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R4

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4.1.2.428 TMU_EXT_CORE1_COSPUF32_R5 Register

4.1.2.428.1 TMU_EXT_CORE1_COSPUF32_R5 Register (Offset = A8h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R5.

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Table 4-880. Instance Table

Instance Name	Physical Address
R5SS0	7826 00A8h
R5SS1	7866 00A8h

Figure 4-428. TMU_EXT_CORE1_COSPUF32_R5 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R5							
R/W							
0h							

Table 4-881. TMU_EXT_CORE1_COSPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R5

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4.1.2.429 TMU_EXT_CORE1_COSPUF32_R6 Register

4.1.2.429.1 TMU_EXT_CORE1_COSPUF32_R6 Register (Offset = B0h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R6.

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Table 4-882. Instance Table

Instance Name	Physical Address
R5SS0	7826 00B0h
R5SS1	7866 00B0h

Figure 4-429. TMU_EXT_CORE1_COSPUF32_R6 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R6							
R/W							
0h							

Table 4-883. TMU_EXT_CORE1_COSPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R6

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4.1.2.430 TMU_EXT_CORE1_COSPUF32_R7 Register

4.1.2.430.1 TMU_EXT_CORE1_COSPUF32_R7 Register (Offset = B8h) [reset = 0h]

Updates operand 1 for COSPUF32 operation. Result will be saved to R7.

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Table 4-884. Instance Table

Instance Name	Physical Address
R5SS0	7826 00B8h
R5SS1	7866 00B8h

Figure 4-430. TMU_EXT_CORE1_COSPUF32_R7 Name Register

31	30	29	28	27	26	25	24
COSPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
COSPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
COSPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
COSPUF32_R7							
R/W							
0h							

Table 4-885. TMU_EXT_CORE1_COSPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COSPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger COSPUF32 operation Result will be saved to R7

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4.1.2.431 TMU_EXT_CORE1_ATANPUF32_R0 Register

4.1.2.431.1 TMU_EXT_CORE1_ATANPUF32_R0 Register (Offset = C0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R0.

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Table 4-886. Instance Table

Instance Name	Physical Address
R5SS0	7826 00C0h
R5SS1	7866 00C0h

Figure 4-431. TMU_EXT_CORE1_ATANPUF32_R0 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R0							
R/W							
0h							

Table 4-887. TMU_EXT_CORE1_ATANPUF32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R0

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4.1.2.432 TMU_EXT_CORE1_ATANPUF32_R1 Register

4.1.2.432.1 TMU_EXT_CORE1_ATANPUF32_R1 Register (Offset = C8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R1.

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Table 4-888. Instance Table

Instance Name	Physical Address
R5SS0	7826 00C8h
R5SS1	7866 00C8h

Figure 4-432. TMU_EXT_CORE1_ATANPUF32_R1 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R1							
R/W							
0h							

Table 4-889. TMU_EXT_CORE1_ATANPUF32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R1

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4.1.2.433 TMU_EXT_CORE1_ATANPUF32_R2 Register

4.1.2.433.1 TMU_EXT_CORE1_ATANPUF32_R2 Register (Offset = D0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R2.

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Table 4-890. Instance Table

Instance Name	Physical Address
R5SS0	7826 00D0h
R5SS1	7866 00D0h

Figure 4-433. TMU_EXT_CORE1_ATANPUF32_R2 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R2							
R/W							
0h							

Table 4-891. TMU_EXT_CORE1_ATANPUF32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R2

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4.1.2.434 TMU_EXT_CORE1_ATANPUF32_R3 Register

4.1.2.434.1 TMU_EXT_CORE1_ATANPUF32_R3 Register (Offset = D8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R3.

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Table 4-892. Instance Table

Instance Name	Physical Address
R5SS0	7826 00D8h
R5SS1	7866 00D8h

Figure 4-434. TMU_EXT_CORE1_ATANPUF32_R3 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R3							
R/W							
0h							

Table 4-893. TMU_EXT_CORE1_ATANPUF32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R3

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4.1.2.435 TMU_EXT_CORE1_ATANPUF32_R4 Register

4.1.2.435.1 TMU_EXT_CORE1_ATANPUF32_R4 Register (Offset = E0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R4.

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Table 4-894. Instance Table

Instance Name	Physical Address
R5SS0	7826 00E0h
R5SS1	7866 00E0h

Figure 4-435. TMU_EXT_CORE1_ATANPUF32_R4 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R4							
R/W							
0h							

Table 4-895. TMU_EXT_CORE1_ATANPUF32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R4

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4.1.2.436 TMU_EXT_CORE1_ATANPUF32_R5 Register

4.1.2.436.1 TMU_EXT_CORE1_ATANPUF32_R5 Register (Offset = E8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R5.

Return to Summary Table

Table 4-896. Instance Table

Instance Name	Physical Address
R5SS0	7826 00E8h
R5SS1	7866 00E8h

Figure 4-436. TMU_EXT_CORE1_ATANPUF32_R5 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R5							
R/W							
0h							

Table 4-897. TMU_EXT_CORE1_ATANPUF32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R5

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4.1.2.437 TMU_EXT_CORE1_ATANPUF32_R6 Register

4.1.2.437.1 TMU_EXT_CORE1_ATANPUF32_R6 Register (Offset = F0h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R6.

Return to Summary Table

Table 4-898. Instance Table

Instance Name	Physical Address
R5SS0	7826 00F0h
R5SS1	7866 00F0h

Figure 4-437. TMU_EXT_CORE1_ATANPUF32_R6 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R6							
R/W							
0h							

Table 4-899. TMU_EXT_CORE1_ATANPUF32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R6

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4.1.2.438 TMU_EXT_CORE1_ATANPUF32_R7 Register

4.1.2.438.1 TMU_EXT_CORE1_ATANPUF32_R7 Register (Offset = F8h) [reset = 0h]

Updates operand 1 for ATANPUF32 operation. Result will be saved to R7.

Return to Summary Table

Table 4-900. Instance Table

Instance Name	Physical Address
R5SS0	7826 00F8h
R5SS1	7866 00F8h

Figure 4-438. TMU_EXT_CORE1_ATANPUF32_R7 Name Register

31	30	29	28	27	26	25	24
ATANPUF32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
ATANPUF32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
ATANPUF32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
ATANPUF32_R7							
R/W							
0h							

Table 4-901. TMU_EXT_CORE1_ATANPUF32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ATANPUF32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger ATANPUF32 operation Result will be saved to R7

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4.1.2.439 TMU_EXT_CORE1_IEXP2F32_R0 Register

4.1.2.439.1 TMU_EXT_CORE1_IEXP2F32_R0 Register (Offset = 140h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R0.

Return to Summary Table

Table 4-902. Instance Table

Instance Name	Physical Address
R5SS0	7826 0140h
R5SS1	7866 0140h

Figure 4-439. TMU_EXT_CORE1_IEXP2F32_R0 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R0							
R/W							
0h							

Table 4-903. TMU_EXT_CORE1_IEXP2F32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R0

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4.1.2.440 TMU_EXT_CORE1_IEXP2F32_R1 Register

4.1.2.440.1 TMU_EXT_CORE1_IEXP2F32_R1 Register (Offset = 148h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R1.

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Table 4-904. Instance Table

Instance Name	Physical Address
R5SS0	7826 0148h
R5SS1	7866 0148h

Figure 4-440. TMU_EXT_CORE1_IEXP2F32_R1 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R1							
R/W							
0h							

Table 4-905. TMU_EXT_CORE1_IEXP2F32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R1

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4.1.2.441 TMU_EXT_CORE1_IEXP2F32_R2 Register

4.1.2.441.1 TMU_EXT_CORE1_IEXP2F32_R2 Register (Offset = 150h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-906. Instance Table

Instance Name	Physical Address
R5SS0	7826 0150h
R5SS1	7866 0150h

Figure 4-441. TMU_EXT_CORE1_IEXP2F32_R2 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R2							
R/W							
0h							

Table 4-907. TMU_EXT_CORE1_IEXP2F32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R2

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4.1.2.442 TMU_EXT_CORE1_IEXP2F32_R3 Register

4.1.2.442.1 TMU_EXT_CORE1_IEXP2F32_R3 Register (Offset = 158h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R3.

Return to Summary Table

Table 4-908. Instance Table

Instance Name	Physical Address
R5SS0	7826 0158h
R5SS1	7866 0158h

Figure 4-442. TMU_EXT_CORE1_IEXP2F32_R3 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R3							
R/W							
0h							

Table 4-909. TMU_EXT_CORE1_IEXP2F32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R3

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4.1.2.443 TMU_EXT_CORE1_IEXP2F32_R4 Register

4.1.2.443.1 TMU_EXT_CORE1_IEXP2F32_R4 Register (Offset = 160h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R4.

Return to Summary Table

Table 4-910. Instance Table

Instance Name	Physical Address
R5SS0	7826 0160h
R5SS1	7866 0160h

Figure 4-443. TMU_EXT_CORE1_IEXP2F32_R4 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R4							
R/W							
0h							

Table 4-911. TMU_EXT_CORE1_IEXP2F32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R4

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4.1.2.444 TMU_EXT_CORE1_IEXP2F32_R5 Register

4.1.2.444.1 TMU_EXT_CORE1_IEXP2F32_R5 Register (Offset = 168h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R5.

Return to Summary Table

Table 4-912. Instance Table

Instance Name	Physical Address
R5SS0	7826 0168h
R5SS1	7866 0168h

Figure 4-444. TMU_EXT_CORE1_IEXP2F32_R5 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R5							
R/W							
0h							

Table 4-913. TMU_EXT_CORE1_IEXP2F32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R5

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4.1.2.445 TMU_EXT_CORE1_IEXP2F32_R6 Register

4.1.2.445.1 TMU_EXT_CORE1_IEXP2F32_R6 Register (Offset = 170h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R6.

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Table 4-914. Instance Table

Instance Name	Physical Address
R5SS0	7826 0170h
R5SS1	7866 0170h

Figure 4-445. TMU_EXT_CORE1_IEXP2F32_R6 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R6							
R/W							
0h							

Table 4-915. TMU_EXT_CORE1_IEXP2F32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R6

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4.1.2.446 TMU_EXT_CORE1_IEXP2F32_R7 Register

4.1.2.446.1 TMU_EXT_CORE1_IEXP2F32_R7 Register (Offset = 178h) [reset = 0h]

Updates operand 1 for IEXP2F32 operation. Result will be saved to R7.

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Table 4-916. Instance Table

Instance Name	Physical Address
R5SS0	7826 0178h
R5SS1	7866 0178h

Figure 4-446. TMU_EXT_CORE1_IEXP2F32_R7 Name Register

31	30	29	28	27	26	25	24
IEXP2F32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
IEXP2F32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
IEXP2F32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
IEXP2F32_R7							
R/W							
0h							

Table 4-917. TMU_EXT_CORE1_IEXP2F32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IEXP2F32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger IEXP2F32 operation Result will be saved to R7

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4.1.2.447 TMU_EXT_CORE1_LOG2F32_R0 Register

4.1.2.447.1 TMU_EXT_CORE1_LOG2F32_R0 Register (Offset = 180h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R0.

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Table 4-918. Instance Table

Instance Name	Physical Address
R5SS0	7826 0180h
R5SS1	7866 0180h

Figure 4-447. TMU_EXT_CORE1_LOG2F32_R0 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R0							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R0							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R0							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R0							
R/W							
0h							

Table 4-919. TMU_EXT_CORE1_LOG2F32_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R0	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R0

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4.1.2.448 TMU_EXT_CORE1_LOG2F32_R1 Register

4.1.2.448.1 TMU_EXT_CORE1_LOG2F32_R1 Register (Offset = 188h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R1.

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Table 4-920. Instance Table

Instance Name	Physical Address
R5SS0	7826 0188h
R5SS1	7866 0188h

Figure 4-448. TMU_EXT_CORE1_LOG2F32_R1 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R1							
R/W							
0h							

Table 4-921. TMU_EXT_CORE1_LOG2F32_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R1	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R1

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4.1.2.449 TMU_EXT_CORE1_LOG2F32_R2 Register

4.1.2.449.1 TMU_EXT_CORE1_LOG2F32_R2 Register (Offset = 190h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R2.

Return to Summary Table

Table 4-922. Instance Table

Instance Name	Physical Address
R5SS0	7826 0190h
R5SS1	7866 0190h

Figure 4-449. TMU_EXT_CORE1_LOG2F32_R2 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R2							
R/W							
0h							

Table 4-923. TMU_EXT_CORE1_LOG2F32_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R2	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R2

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4.1.2.450 TMU_EXT_CORE1_LOG2F32_R3 Register

4.1.2.450.1 TMU_EXT_CORE1_LOG2F32_R3 Register (Offset = 198h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R3.

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Table 4-924. Instance Table

Instance Name	Physical Address
R5SS0	7826 0198h
R5SS1	7866 0198h

Figure 4-450. TMU_EXT_CORE1_LOG2F32_R3 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R3							
R/W							
0h							

Table 4-925. TMU_EXT_CORE1_LOG2F32_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R3	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R3

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4.1.2.451 TMU_EXT_CORE1_LOG2F32_R4 Register

4.1.2.451.1 TMU_EXT_CORE1_LOG2F32_R4 Register (Offset = 1A0h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R4.

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Table 4-926. Instance Table

Instance Name	Physical Address
R5SS0	7826 01A0h
R5SS1	7866 01A0h

Figure 4-451. TMU_EXT_CORE1_LOG2F32_R4 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R4							
R/W							
0h							

Table 4-927. TMU_EXT_CORE1_LOG2F32_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R4	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R4

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4.1.2.452 TMU_EXT_CORE1_LOG2F32_R5 Register

4.1.2.452.1 TMU_EXT_CORE1_LOG2F32_R5 Register (Offset = 1A8h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R5.

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Table 4-928. Instance Table

Instance Name	Physical Address
R5SS0	7826 01A8h
R5SS1	7866 01A8h

Figure 4-452. TMU_EXT_CORE1_LOG2F32_R5 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R5							
R/W							
0h							

Table 4-929. TMU_EXT_CORE1_LOG2F32_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R5	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R5

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4.1.2.453 TMU_EXT_CORE1_LOG2F32_R6 Register

4.1.2.453.1 TMU_EXT_CORE1_LOG2F32_R6 Register (Offset = 1B0h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R6.

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Table 4-930. Instance Table

Instance Name	Physical Address
R5SS0	7826 01B0h
R5SS1	7866 01B0h

Figure 4-453. TMU_EXT_CORE1_LOG2F32_R6 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R6							
R/W							
0h							

Table 4-931. TMU_EXT_CORE1_LOG2F32_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R6	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R6

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4.1.2.454 TMU_EXT_CORE1_LOG2F32_R7 Register

4.1.2.454.1 TMU_EXT_CORE1_LOG2F32_R7 Register (Offset = 1B8h) [reset = 0h]

Updates operand 1 for LOG2F32 operation. Result will be saved to R7.

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Table 4-932. Instance Table

Instance Name	Physical Address
R5SS0	7826 01B8h
R5SS1	7866 01B8h

Figure 4-454. TMU_EXT_CORE1_LOG2F32_R7 Name Register

31	30	29	28	27	26	25	24
LOG2F32_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
LOG2F32_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
LOG2F32_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
LOG2F32_R7							
R/W							
0h							

Table 4-933. TMU_EXT_CORE1_LOG2F32_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOG2F32_R7	R/W	0h	Write to this register will update Operand 1 Update will trigger LOG2F32 operation Result will be saved to R7

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4.1.2.455 TMU_EXT_CORE1_QUADF32_X_R0_R1 Register

4.1.2.455.1 TMU_EXT_CORE1_QUADF32_X_R0_R1 Register (Offset = 1C0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R0 and R1.

Return to Summary Table

Table 4-934. Instance Table

Instance Name	Physical Address
R5SS0	7826 01C0h
R5SS1	7866 01C0h

Figure 4-455. TMU_EXT_CORE1_QUADF32_X_R0_R1 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R0_R1							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R0_R1							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R0_R1							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R0_R1							
R/W							
0h							

Table 4-935. TMU_EXT_CORE1_QUADF32_X_R0_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R0_R1	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R0 and R1

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4.1.2.456 TMU_EXT_CORE1_QUADF32_X_R1_R2 Register

4.1.2.456.1 TMU_EXT_CORE1_QUADF32_X_R1_R2 Register (Offset = 1C8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R1 and R2.

Return to Summary Table

Table 4-936. Instance Table

Instance Name	Physical Address
R5SS0	7826 01C8h
R5SS1	7866 01C8h

Figure 4-456. TMU_EXT_CORE1_QUADF32_X_R1_R2 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R1_R2							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R1_R2							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R1_R2							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R1_R2							
R/W							
0h							

Table 4-937. TMU_EXT_CORE1_QUADF32_X_R1_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R1_R2	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R1 and R2

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4.1.2.457 TMU_EXT_CORE1_QUADF32_X_R2_R3 Register

4.1.2.457.1 TMU_EXT_CORE1_QUADF32_X_R2_R3 Register (Offset = 1D0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R2 and R3.

Return to Summary Table

Table 4-938. Instance Table

Instance Name	Physical Address
R5SS0	7826 01D0h
R5SS1	7866 01D0h

Figure 4-457. TMU_EXT_CORE1_QUADF32_X_R2_R3 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R2_R3							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R2_R3							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R2_R3							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R2_R3							
R/W							
0h							

Table 4-939. TMU_EXT_CORE1_QUADF32_X_R2_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R2_R3	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R2 and R3

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4.1.2.458 TMU_EXT_CORE1_QUADF32_X_R3_R4 Register

4.1.2.458.1 TMU_EXT_CORE1_QUADF32_X_R3_R4 Register (Offset = 1D8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R3 and R4.

Return to Summary Table

Table 4-940. Instance Table

Instance Name	Physical Address
R5SS0	7826 01D8h
R5SS1	7866 01D8h

Figure 4-458. TMU_EXT_CORE1_QUADF32_X_R3_R4 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R3_R4							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R3_R4							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R3_R4							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R3_R4							
R/W							
0h							

Table 4-941. TMU_EXT_CORE1_QUADF32_X_R3_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R3_R4	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R3 and R4

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4.1.2.459 TMU_EXT_CORE1_QUADF32_X_R4_R5 Register

4.1.2.459.1 TMU_EXT_CORE1_QUADF32_X_R4_R5 Register (Offset = 1E0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R4 and R5.

Return to Summary Table

Table 4-942. Instance Table

Instance Name	Physical Address
R5SS0	7826 01E0h
R5SS1	7866 01E0h

Figure 4-459. TMU_EXT_CORE1_QUADF32_X_R4_R5 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R4_R5							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R4_R5							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R4_R5							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R4_R5							
R/W							
0h							

Table 4-943. TMU_EXT_CORE1_QUADF32_X_R4_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R4_R5	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R4 and R5

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4.1.2.460 TMU_EXT_CORE1_QUADF32_X_R5SS0_R6 Register

4.1.2.460.1 TMU_EXT_CORE1_QUADF32_X_R5SS0_R6 Register (Offset = 1E8h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R5 and R6.

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Table 4-944. Instance Table

Instance Name	Physical Address
R5SS0	7826 01E8h
R5SS1	7866 01E8h

Figure 4-460. TMU_EXT_CORE1_QUADF32_X_R5SS0_R6 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R5_R6							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R5_R6							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R5_R6							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R5_R6							
R/W							
0h							

Table 4-945. TMU_EXT_CORE1_QUADF32_X_R5SS0_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R5_R6	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R5 and R6

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4.1.2.461 TMU_EXT_CORE1_QUADF32_X_R6_R7 Register

4.1.2.461.1 TMU_EXT_CORE1_QUADF32_X_R6_R7 Register (Offset = 1F0h) [reset = 0h]

Updates operand 1 (X) for QUADF32 operation. Result will be saved to R6 and R7.

Return to Summary Table

Table 4-946. Instance Table

Instance Name	Physical Address
R5SS0	7826 01F0h
R5SS1	7866 01F0h

Figure 4-461. TMU_EXT_CORE1_QUADF32_X_R6_R7 Name Register

31	30	29	28	27	26	25	24
QUADF32_X_R6_R7							
R/W							
0h							
23	22	21	20	19	18	17	16
QUADF32_X_R6_R7							
R/W							
0h							
15	14	13	12	11	10	9	8
QUADF32_X_R6_R7							
R/W							
0h							
7	6	5	4	3	2	1	0
QUADF32_X_R6_R7							
R/W							
0h							

Table 4-947. TMU_EXT_CORE1_QUADF32_X_R6_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	QUADF32_X_R6_R7	R/W	0h	Write to this register will update Operand 1 Operand 2 must be written first by Writing to register QUADF32_Y Update will trigger QUADF32 operation Result will be saved to R6 and R7

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4.1.2.462 TMU_EXT_CORE1_RESULT_R0 Register

4.1.2.462.1 TMU_EXT_CORE1_RESULT_R0 Register (Offset = 280h) [reset = 0h]

R0 result register.

Return to Summary Table

Table 4-948. Instance Table

Instance Name	Physical Address
R5SS0	7826 0280h
R5SS1	7866 0280h

Figure 4-462. TMU_EXT_CORE1_RESULT_R0 Name Register

31	30	29	28	27	26	25	24
R0							
R							
0h							
23	22	21	20	19	18	17	16
R0							
R							
0h							
15	14	13	12	11	10	9	8
R0							
R							
0h							
7	6	5	4	3	2	1	0
R0							
R							
0h							

Table 4-949. TMU_EXT_CORE1_RESULT_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R0	R	0h	R0 result register

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4.1.2.463 TMU_EXT_CORE1_RESULT_R1 Register

4.1.2.463.1 TMU_EXT_CORE1_RESULT_R1 Register (Offset = 288h) [reset = 0h]

R1 result register.

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Table 4-950. Instance Table

Instance Name	Physical Address
R5SS0	7826 0288h
R5SS1	7866 0288h

Figure 4-463. TMU_EXT_CORE1_RESULT_R1 Name Register

31	30	29	28	27	26	25	24
R1							
R							
0h							
23	22	21	20	19	18	17	16
R1							
R							
0h							
15	14	13	12	11	10	9	8
R1							
R							
0h							
7	6	5	4	3	2	1	0
R1							
R							
0h							

Table 4-951. TMU_EXT_CORE1_RESULT_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R1	R	0h	R1 result register

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4.1.2.464 TMU_EXT_CORE1_RESULT_R2 Register

4.1.2.464.1 TMU_EXT_CORE1_RESULT_R2 Register (Offset = 290h) [reset = 0h]

R2 result register.

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Table 4-952. Instance Table

Instance Name	Physical Address
R5SS0	7826 0290h
R5SS1	7866 0290h

Figure 4-464. TMU_EXT_CORE1_RESULT_R2 Name Register

31	30	29	28	27	26	25	24
R2							
R							
0h							
23	22	21	20	19	18	17	16
R2							
R							
0h							
15	14	13	12	11	10	9	8
R2							
R							
0h							
7	6	5	4	3	2	1	0
R2							
R							
0h							

Table 4-953. TMU_EXT_CORE1_RESULT_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R2	R	0h	R2 result register

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4.1.2.465 TMU_EXT_CORE1_RESULT_R3 Register

4.1.2.465.1 TMU_EXT_CORE1_RESULT_R3 Register (Offset = 298h) [reset = 0h]

R3 result register.

Return to Summary Table

Table 4-954. Instance Table

Instance Name	Physical Address
R5SS0	7826 0298h
R5SS1	7866 0298h

Figure 4-465. TMU_EXT_CORE1_RESULT_R3 Name Register

31	30	29	28	27	26	25	24
R3							
R							
0h							
23	22	21	20	19	18	17	16
R3							
R							
0h							
15	14	13	12	11	10	9	8
R3							
R							
0h							
7	6	5	4	3	2	1	0
R3							
R							
0h							

Table 4-955. TMU_EXT_CORE1_RESULT_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R3	R	0h	R3 result register

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4.1.2.466 TMU_EXT_CORE1_RESULT_R4 Register

4.1.2.466.1 TMU_EXT_CORE1_RESULT_R4 Register (Offset = 2A0h) [reset = 0h]

R4 result register.

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Table 4-956. Instance Table

Instance Name	Physical Address
R5SS0	7826 02A0h
R5SS1	7866 02A0h

Figure 4-466. TMU_EXT_CORE1_RESULT_R4 Name Register

31	30	29	28	27	26	25	24
R4							
R							
0h							
23	22	21	20	19	18	17	16
R4							
R							
0h							
15	14	13	12	11	10	9	8
R4							
R							
0h							
7	6	5	4	3	2	1	0
R4							
R							
0h							

Table 4-957. TMU_EXT_CORE1_RESULT_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R4	R	0h	R4 result register

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4.1.2.467 TMU_EXT_CORE1_RESULT_R5 Register

4.1.2.467.1 TMU_EXT_CORE1_RESULT_R5 Register (Offset = 2A8h) [reset = 0h]

R5 result register.

Return to Summary Table

Table 4-958. Instance Table

Instance Name	Physical Address
R5SS0	7826 02A8h
R5SS1	7866 02A8h

Figure 4-467. TMU_EXT_CORE1_RESULT_R5 Name Register

31	30	29	28	27	26	25	24
R5							
R							
0h							
23	22	21	20	19	18	17	16
R5							
R							
0h							
15	14	13	12	11	10	9	8
R5							
R							
0h							
7	6	5	4	3	2	1	0
R5							
R							
0h							

Table 4-959. TMU_EXT_CORE1_RESULT_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R5	R	0h	R5 result register

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4.1.2.468 TMU_EXT_CORE1_RESULT_R6 Register

4.1.2.468.1 TMU_EXT_CORE1_RESULT_R6 Register (Offset = 2B0h) [reset = 0h]

R6 result register.

Return to Summary Table

Table 4-960. Instance Table

Instance Name	Physical Address
R5SS0	7826 02B0h
R5SS1	7866 02B0h

Figure 4-468. TMU_EXT_CORE1_RESULT_R6 Name Register

31	30	29	28	27	26	25	24
R6							
R							
0h							
23	22	21	20	19	18	17	16
R6							
R							
0h							
15	14	13	12	11	10	9	8
R6							
R							
0h							
7	6	5	4	3	2	1	0
R6							
R							
0h							

Table 4-961. TMU_EXT_CORE1_RESULT_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R6	R	0h	R6 result register

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4.1.2.469 TMU_EXT_CORE1_RESULT_R7 Register

4.1.2.469.1 TMU_EXT_CORE1_RESULT_R7 Register (Offset = 2B8h) [reset = 0h]

R7 result register.

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Table 4-962. Instance Table

Instance Name	Physical Address
R5SS0	7826 02B8h
R5SS1	7866 02B8h

Figure 4-469. TMU_EXT_CORE1_RESULT_R7 Name Register

31	30	29	28	27	26	25	24
R7							
R							
0h							
23	22	21	20	19	18	17	16
R7							
R							
0h							
15	14	13	12	11	10	9	8
R7							
R							
0h							
7	6	5	4	3	2	1	0
R7							
R							
0h							

Table 4-963. TMU_EXT_CORE1_RESULT_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R7	R	0h	R7 result register

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4.1.2.470 TMU_EXT_CORE1_CSAVE_R0 Register

4.1.2.470.1 TMU_EXT_CORE1_CSAVE_R0 Register (Offset = 2C0h) [reset = 0h]

Context save of R0 result register.

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Table 4-964. Instance Table

Instance Name	Physical Address
R5SS0	7826 02C0h
R5SS1	7866 02C0h

Figure 4-470. TMU_EXT_CORE1_CSAVE_R0 Name Register

31	30	29	28	27	26	25	24
CSAVE_R0							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R0							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R0							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R0							
R							
0h							

Table 4-965. TMU_EXT_CORE1_CSAVE_R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R0	R	0h	Context save of R0 result register

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4.1.2.471 TMU_EXT_CORE1_CSAVE_R1 Register

4.1.2.471.1 TMU_EXT_CORE1_CSAVE_R1 Register (Offset = 2C8h) [reset = 0h]

Context save of R1 result register.

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Table 4-966. Instance Table

Instance Name	Physical Address
R5SS0	7826 02C8h
R5SS1	7866 02C8h

Figure 4-471. TMU_EXT_CORE1_CSAVE_R1 Name Register

31	30	29	28	27	26	25	24
CSAVE_R1							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R1							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R1							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R1							
R							
0h							

Table 4-967. TMU_EXT_CORE1_CSAVE_R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R1	R	0h	Context save of R1 result register

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4.1.2.472 TMU_EXT_CORE1_CSAVE_R2 Register

4.1.2.472.1 TMU_EXT_CORE1_CSAVE_R2 Register (Offset = 2D0h) [reset = 0h]

Context save of R2 result register.

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Table 4-968. Instance Table

Instance Name	Physical Address
R5SS0	7826 02D0h
R5SS1	7866 02D0h

Figure 4-472. TMU_EXT_CORE1_CSAVE_R2 Name Register

31	30	29	28	27	26	25	24
CSAVE_R2							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R2							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R2							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R2							
R							
0h							

Table 4-969. TMU_EXT_CORE1_CSAVE_R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R2	R	0h	Context save of R2 result register

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4.1.2.473 TMU_EXT_CORE1_CSAVE_R3 Register

4.1.2.473.1 TMU_EXT_CORE1_CSAVE_R3 Register (Offset = 2D8h) [reset = 0h]

Context save of R3 result register.

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Table 4-970. Instance Table

Instance Name	Physical Address
R5SS0	7826 02D8h
R5SS1	7866 02D8h

Figure 4-473. TMU_EXT_CORE1_CSAVE_R3 Name Register

31	30	29	28	27	26	25	24
CSAVE_R3							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R3							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R3							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R3							
R							
0h							

Table 4-971. TMU_EXT_CORE1_CSAVE_R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R3	R	0h	Context save of R3 result register

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4.1.2.474 TMU_EXT_CORE1_CSAVE_R4 Register

4.1.2.474.1 TMU_EXT_CORE1_CSAVE_R4 Register (Offset = 2E0h) [reset = 0h]

Context save of R4 result register.

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Table 4-972. Instance Table

Instance Name	Physical Address
R5SS0	7826 02E0h
R5SS1	7866 02E0h

Figure 4-474. TMU_EXT_CORE1_CSAVE_R4 Name Register

31	30	29	28	27	26	25	24
CSAVE_R4							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R4							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R4							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R4							
R							
0h							

Table 4-973. TMU_EXT_CORE1_CSAVE_R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R4	R	0h	Context save of R4 result register

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4.1.2.475 TMU_EXT_CORE1_CSAVE_R5 Register

4.1.2.475.1 TMU_EXT_CORE1_CSAVE_R5 Register (Offset = 2E8h) [reset = 0h]

Context save of R5 result register.

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Table 4-974. Instance Table

Instance Name	Physical Address
R5SS0	7826 02E8h
R5SS1	7866 02E8h

Figure 4-475. TMU_EXT_CORE1_CSAVE_R5 Name Register

31	30	29	28	27	26	25	24
CSAVE_R5							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R5							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R5							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R5							
R							
0h							

Table 4-975. TMU_EXT_CORE1_CSAVE_R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R5	R	0h	Context save of R5 result register

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4.1.2.476 TMU_EXT_CORE1_CSAVE_R6 Register

4.1.2.476.1 TMU_EXT_CORE1_CSAVE_R6 Register (Offset = 2F0h) [reset = 0h]

Context save of R6 result register.

Return to Summary Table

Table 4-976. Instance Table

Instance Name	Physical Address
R5SS0	7826 02F0h
R5SS1	7866 02F0h

Figure 4-476. TMU_EXT_CORE1_CSAVE_R6 Name Register

31	30	29	28	27	26	25	24
CSAVE_R6							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R6							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R6							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R6							
R							
0h							

Table 4-977. TMU_EXT_CORE1_CSAVE_R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R6	R	0h	Context save of R6 result register

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4.1.2.477 TMU_EXT_CORE1_CSAVE_R7 Register

4.1.2.477.1 TMU_EXT_CORE1_CSAVE_R7 Register (Offset = 2F8h) [reset = 0h]

Context save of R7 result register.

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Table 4-978. Instance Table

Instance Name	Physical Address
R5SS0	7826 02F8h
R5SS1	7866 02F8h

Figure 4-477. TMU_EXT_CORE1_CSAVE_R7 Name Register

31	30	29	28	27	26	25	24
CSAVE_R7							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_R7							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_R7							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_R7							
R							
0h							

Table 4-979. TMU_EXT_CORE1_CSAVE_R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_R7	R	0h	Context save of R7 result register

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4.1.2.478 TMU_EXT_CORE1_CSAVE_OP2 Register

4.1.2.478.1 TMU_EXT_CORE1_CSAVE_OP2 Register (Offset = 300h) [reset = 0h]

Context save of Operarand2 result register.

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Table 4-980. Instance Table

Instance Name	Physical Address
R5SS0	7826 0300h
R5SS1	7866 0300h

Figure 4-478. TMU_EXT_CORE1_CSAVE_OP2 Name Register

31	30	29	28	27	26	25	24
CSAVE_OP2							
R							
0h							
23	22	21	20	19	18	17	16
CSAVE_OP2							
R							
0h							
15	14	13	12	11	10	9	8
CSAVE_OP2							
R							
0h							
7	6	5	4	3	2	1	0
CSAVE_OP2							
R							
0h							

Table 4-981. TMU_EXT_CORE1_CSAVE_OP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSAVE_OP2	R	0h	Context save of operand 2 [OP2] result register

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4.1.2.479 TMU_EXT_CORE1_CONTEXT_SAVE Register

4.1.2.479.1 TMU_EXT_CORE1_CONTEXT_SAVE Register (Offset = 308h) [reset = 0h]

Register to initiate context save of result registers.

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Table 4-982. Instance Table

Instance Name	Physical Address
R5SS0	7826 0308h
R5SS1	7866 0308h

Figure 4-479. TMU_EXT_CORE1_CONTEXT_SAVE Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							SAVE
R							R/W1TS
0h							0h

Table 4-983. TMU_EXT_CORE1_CONTEXT_SAVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	SAVE	R/W1TS	0h	Writing one will initiate context save. Context save will be done only after completion all operations initiated by master before context save was issued. Results registers R0 to R3 and Operand2 will be saved. Note: Contex is saved within IP, not to external memory.

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4.1.2.480 TMU_EXT_CORE1_CONTEXT_RESTORE Register

4.1.2.480.1 TMU_EXT_CORE1_CONTEXT_RESTORE Register (Offset = 310h) [reset = 0h]

Register to initiate context restore of result registers.

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Table 4-984. Instance Table

Instance Name	Physical Address
R5SS0	7826 0310h
R5SS1	7866 0310h

Figure 4-480. TMU_EXT_CORE1_CONTEXT_RESTORE Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							RESTORE
R							R/W1TS
0h							0h

Table 4-985. TMU_EXT_CORE1_CONTEXT_RESTORE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	RESTORE	R/W1TS	0h	Writing one will initiate context restore. Results registers R0 to R3 and Operand2 will be restored.

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4.1.2.481 TMU_EXT_CORE1_STF Register

4.1.2.481.1 TMU_EXT_CORE1_STF Register (Offset = 348h) [reset = 0h]

TMU status Register.

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Table 4-986. Instance Table

Instance Name	Physical Address
R5SS0	7826 0348h
R5SS1	7866 0348h

Figure 4-481. TMU_EXT_CORE1_STF Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2						LUF_WR_EN	LVF_WR_EN
R						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED_1						LUF	LVF
R						R/W	R/W
0h						0h	0h

Table 4-987. TMU_EXT_CORE1_STF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_2	R	0h	Reserved
9	LUF_WR_EN	R	0h	Always read as zero, Value is written to this bit either enables/ disables write to LVF [[br] 0:Disbles write to LUF 1:Enables write to LUF
8	LVF_WR_EN	R	0h	Always read as zero, Value is written to this bit either enables/ disables write to LVF [[br] 0:Disbles write to LVF 1:Enables write to LVF
7:2	RESERVED_1	R	0h	Reserved
1	LUF	R/W	0h	Is set to '1' when a TMU operation results in LVF. It is sticky bit, once set, it remains set until it is cleared with write. It can be written only when LUF_WR_EN Is written with '1'
0	LVF	R/W	0h	Is set to '1' when a TMU operation results in LVF. It is sticky bit, once set, it remains set until it is cleared with write. It can be written only when LVF_WR_EN Is written with '1'

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4.1.2.482 TMU_EXT_CORE1_PARITY_TEST Register

4.1.2.482.1 TMU_EXT_CORE1_PARITY_TEST Register (Offset = 380h) [reset = 0h]

Enabling the parity test feature.

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Table 4-988. Instance Table

Instance Name	Physical Address
R5SS0	7826 0380h
R5SS1	7866 0380h

Figure 4-482. TMU_EXT_CORE1_PARITY_TEST Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1				TESTEN			
R				R/W			
0h				0h			

Table 4-989. TMU_EXT_CORE1_PARITY_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:4	RESERVED_1	R	0h	Reserved
3:0	TESTEN	R/W	0h	1010: Parity test feature is enabled All other values: Parity test feature is disabled Note: When the parity test feature is enabled, acutal registers are not accessible in the memory map. Instead, the parity values are accessible. Parity is computed for every byte and the correponding parity value is available at the bit-0 of every byte. Value of '1' written to the parity bit after enabling the parity test feature can be used to inject the error by inverting the stored parity value.

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4.1.2.483 TMU_EXT_CORE1_LCM_LOCK Register

4.1.2.483.1 TMU_EXT_CORE1_LCM_LOCK Register (Offset = 390h) [reset = 0h]

LCM lock configuration.

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Table 4-990. Instance Table

Instance Name	Physical Address
R5SS0	7826 0390h
R5SS1	7866 0390h

Figure 4-483. TMU_EXT_CORE1_LCM_LOCK Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							PARITY_TEST
R							R/W
0h							0h

Table 4-991. TMU_EXT_CORE1_LCM_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	PARITY_TEST	R/W	0h	0: Register configuration is not locked. [[br] 1:Register configuration is locked.

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4.1.2.484 TMU_EXT_CORE1_LCM_COMMIT Register

4.1.2.484.1 TMU_EXT_CORE1_LCM_COMMIT Register (Offset = 3A0h) [reset = 0h]

LCM commit configuration.

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Table 4-992. Instance Table

Instance Name	Physical Address
R5SS0	7826 03A0h
R5SS1	7866 03A0h

Figure 4-484. TMU_EXT_CORE1_LCM_COMMIT Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1							PARITY_TEST
R							R/W1TS
0h							0h

Table 4-993. TMU_EXT_CORE1_LCM_COMMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_1	R	0h	Reserved
0	PARITY_TEST	R/W1TS	0h	0: Register lock configuration is not committed. [[br] 1:Register lock configuration is committed. Once configuration is committed, only reset can change the configuration.

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4.1.2.485 TCMB_CORE1_START Register

4.1.2.485.1 TCMB_CORE1_START Register (Offset = 0h) [reset = 0h]

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Table 4-994. Instance Table

Instance Name	Physical Address
R5SS0	7830 0000h
R5SS1	7870 0000h

Figure 4-485. TCMB_CORE1_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 4-995. TCMB_CORE1_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	TCMB start address

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4.1.2.486 TCMB_CORE1_END Register

4.1.2.486.1 TCMB_CORE1_END Register (Offset = 17FFCh) [reset = 0h]

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Table 4-996. Instance Table

Instance Name	Physical Address
R5SS0	7831 7FFCh
R5SS1	7871 7FFCh

Figure 4-486. TCMB_CORE1_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 4-997. TCMB_CORE1_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	TCMB end address

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4.2 ICSSM

ICSSM

4.2.1 ICSSM Summaries

ICSSM Summaries

Table 4-998. ICSSM_DRAM0_SLV_RAM Registers, Base Address=4800 0000h, Length=8192

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_DRAM0_SLV_RAM_RAM_REG_J	4800 0000h + formula

Table 4-999. ICSSM_DRAM1_SLV_RAM Registers, Base Address=4800 2000h, Length=8192

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_DRAM1_SLV_RAM_RAM_REG_J	4800 2000h + formula

Table 4-1000. RAT_SLICE0 Registers, Base Address=4800 8000h, Length=4096

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	RAT_SLICE0_PID	4800 8000h
4h	32	RAT_SLICE0_CONFIG	4800 8004h
804h	32	RAT_SLICE0_DESTINATION_ID	4800 8804h
820h	32	RAT_SLICE0_EXCEPTION_LOGGING_CONTROL	4800 8820h
824h	32	RAT_SLICE0_EXCEPTION_LOGGING_HEADER0	4800 8824h
828h	32	RAT_SLICE0_EXCEPTION_LOGGING_HEADER1	4800 8828h
82Ch	32	RAT_SLICE0_EXCEPTION_LOGGING_DATA0	4800 882Ch
830h	32	RAT_SLICE0_EXCEPTION_LOGGING_DATA1	4800 8830h
834h	32	RAT_SLICE0_EXCEPTION_LOGGING_DATA2	4800 8834h
838h	32	RAT_SLICE0_EXCEPTION_LOGGING_DATA3	4800 8838h
840h	32	RAT_SLICE0_EXCEPTION_PEND_SET	4800 8840h
844h	32	RAT_SLICE0_EXCEPTION_PEND_CLEAR	4800 8844h
848h	32	RAT_SLICE0_EXCEPTION_ENABLE_SET	4800 8848h
84Ch	32	RAT_SLICE0_EXCEPTION_ENABLE_CLEAR	4800 884Ch
850h	32	RAT_SLICE0_EOI_REG	4800 8850h
20h	32	RAT_SLICE0_REGION_CTRL_J	4800 8020h + formula
24h	32	RAT_SLICE0_REGION_BASE_J	4800 8024h + formula
28h	32	RAT_SLICE0_REGION_TRANS_L_J	4800 8028h + formula
2Ch	32	RAT_SLICE0_REGION_TRANS_U_J	4800 802Ch + formula

Table 4-1001. RAT_SLICE1 Registers, Base Address=4800 9000h, Length=4096

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	RAT_SLICE1_PID	4800 9000h
4h	32	RAT_SLICE1_CONFIG	4800 9004h
804h	32	RAT_SLICE1_DESTINATION_ID	4800 9804h
820h	32	RAT_SLICE1_EXCEPTION_LOGGING_CONTROL	4800 9820h
824h	32	RAT_SLICE1_EXCEPTION_LOGGING_HEADER0	4800 9824h
828h	32	RAT_SLICE1_EXCEPTION_LOGGING_HEADER1	4800 9828h
82Ch	32	RAT_SLICE1_EXCEPTION_LOGGING_DATA0	4800 982Ch
830h	32	RAT_SLICE1_EXCEPTION_LOGGING_DATA1	4800 9830h

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Table 4-1001. RAT_SLICE1 Registers, Base Address=4800 9000h, Length=4096 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
834h	32	RAT_SLICE1_EXCEPTION_LOGGING_DATA2	4800 9834h
838h	32	RAT_SLICE1_EXCEPTION_LOGGING_DATA3	4800 9838h
840h	32	RAT_SLICE1_EXCEPTION_PEND_SET	4800 9840h
844h	32	RAT_SLICE1_EXCEPTION_PEND_CLEAR	4800 9844h
848h	32	RAT_SLICE1_EXCEPTION_ENABLE_SET	4800 9848h
84Ch	32	RAT_SLICE1_EXCEPTION_ENABLE_CLEAR	4800 984Ch
850h	32	RAT_SLICE1_EOI_REG	4800 9850h
20h	32	RAT_SLICE1_REGION_CTRL_J	4800 9020h + formula
24h	32	RAT_SLICE1_REGION_BASE_J	4800 9024h + formula
28h	32	RAT_SLICE1_REGION_TRANS_L_J	4800 9028h + formula
2Ch	32	RAT_SLICE1_REGION_TRANS_U_J	4800 902Ch + formula

Table 4-1002. ICSSM_RAM_SLV_RAM Registers, Base Address=4801 0000h, Length=32768

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_RAM_SLV_RAM_RAM_REG_J	4801 0000h + formula

Table 4-1003. ICSSM_PR1_ICSS_INTC_INTC_SLV Registers, Base Address=4802 0000h, Length=8192

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_REVISION_REG	4802 0000h
4h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CONTROL_REG	4802 0004h
10h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_GLOBAL_ENABLE_HINT_REG	4802 0010h
1Ch	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_NEST_LEVEL_REG	4802 001Ch
20h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_SET_INDEX_REG	4802 0020h
24h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_CLR_INDEX_REG	4802 0024h
28h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_SET_INDEX_REG	4802 0028h
2Ch	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_INDEX_REG	4802 002Ch
34h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_SET_INDEX_REG	4802 0034h
38h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_CLR_INDEX_REG	4802 0038h
80h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_PRI_INTR_REG	4802 0080h
200h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG0	4802 0200h
204h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG1	4802 0204h
280h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG0	4802 0280h
284h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG1	4802 0284h
300h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG0	4802 0300h
304h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG1	4802 0304h
380h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG0	4802 0380h

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Table 4-1003. ICSSM_PR1_ICSS_INTC_INTC_SLV Registers, Base Address=4802 0000h, Length=8192 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
384h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG1	4802 0384h
400h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG0	4802 0400h
404h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG1	4802 0404h
408h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG2	4802 0408h
40Ch	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG3	4802 040Ch
410h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG4	4802 0410h
414h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG5	4802 0414h
418h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG6	4802 0418h
41Ch	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG7	4802 041Ch
420h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG8	4802 0420h
424h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG9	4802 0424h
428h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG10	4802 0428h
42Ch	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG11	4802 042Ch
430h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG12	4802 0430h
434h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG13	4802 0434h
438h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG14	4802 0438h
43Ch	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG15	4802 043Ch
800h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG0	4802 0800h
804h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG1	4802 0804h
808h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG2	4802 0808h
900h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG0	4802 0900h
904h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG1	4802 0904h
908h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG2	4802 0908h
90Ch	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG3	4802 090Ch
910h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG4	4802 0910h
914h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG5	4802 0914h
918h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG6	4802 0918h
91Ch	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG7	4802 091Ch
920h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG8	4802 0920h
924h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG9	4802 0924h
D00h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG0	4802 0D00h
D04h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG1	4802 0D04h
D80h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG0	4802 0D80h
D84h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG1	4802 0D84h
1100h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG0	4802 1100h
1104h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG1	4802 1104h
1108h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG2	4802 1108h
110Ch	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG3	4802 110Ch
1110h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG4	4802 1110h
1114h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG5	4802 1114h

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Table 4-1003. ICSSM_PR1_ICSS_INTC_INTC_SLV Registers, Base Address=4802 0000h, Length=8192 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
1118h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG6	4802 1118h
111Ch	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG7	4802 111Ch
1120h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG8	4802 1120h
1124h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG9	4802 1124h
1500h	32	ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_HINT_REG0	4802 1500h

Table 4-1004. ICSSM_PR1_PDSP0_IRAM Registers, Base Address=4802 2000h, Length=256

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_PDSP0_IRAM_CONTROL	4802 2000h
4h	32	ICSSM_PR1_PDSP0_IRAM_STATUS	4802 2004h
8h	32	ICSSM_PR1_PDSP0_IRAM_WAKEUP_ENABLE	4802 2008h
Ch	32	ICSSM_PR1_PDSP0_IRAM_CYCLE_COUNT	4802 200Ch
10h	32	ICSSM_PR1_PDSP0_IRAM_STALL_COUNT	4802 2010h
20h	32	ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_BLOCK_INDEX_0	4802 2020h
24h	32	ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_BLOCK_INDEX_1	4802 2024h
28h	32	ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_PROG_PTR_0	4802 2028h
2Ch	32	ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_PROG_PTR_1	4802 202Ch

Table 4-1005. ICSSM_PR1_PDSP0_IRAM_DEBUG Registers, Base Address=4802 2400h, Length=256

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_PDSP0_IRAM_DEBUG_IGP_J	4802 2400h + formula
80h	32	ICSSM_PR1_PDSP0_IRAM_DEBUG_ICTE_J	4802 2480h + formula

Table 4-1006. ICSSM_PR1_PDSP1_IRAM Registers, Base Address=4802 4000h, Length=256

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_PDSP1_IRAM_CONTROL	4802 4000h
4h	32	ICSSM_PR1_PDSP1_IRAM_STATUS	4802 4004h
8h	32	ICSSM_PR1_PDSP1_IRAM_WAKEUP_ENABLE	4802 4008h
Ch	32	ICSSM_PR1_PDSP1_IRAM_CYCLE_COUNT	4802 400Ch
10h	32	ICSSM_PR1_PDSP1_IRAM_STALL_COUNT	4802 4010h
20h	32	ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_BLOCK_INDEX_0	4802 4020h
24h	32	ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_BLOCK_INDEX_1	4802 4024h
28h	32	ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_PROG_PTR_0	4802 4028h
2Ch	32	ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_PROG_PTR_1	4802 402Ch

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Table 4-1007. ICSSM_PR1_PDSP1_IRAM_DEBUG Registers, Base Address=4802 4400h, Length=256

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_PDSP1_IRAM_DEBUG_IGP_J	4802 4400h + formula
80h	32	ICSSM_PR1_PDSP1_IRAM_DEBUG_ICTE_J	4802 4480h + formula

Table 4-1008. ICSSM_PR1_PROTECT_SLV Registers, Base Address=4802 4C00h, Length=256

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_PROTECT_SLV_UNLOCK_KEY	4802 4C00h
4h	32	ICSSM_PR1_PROTECT_SLV_CFG	4802 4C04h

Table 4-1009. ICSSM_PR1_CFG_SLV Registers, Base Address=4802 6000h, Length=512

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_CFG_SLV_PID_REG	4802 6000h
4h	32	ICSSM_PR1_CFG_SLV_HWDIS_REG	4802 6004h
8h	32	ICSSM_PR1_CFG_SLV_GPCFG0_REG	4802 6008h
Ch	32	ICSSM_PR1_CFG_SLV_GPCFG1_REG	4802 600Ch
10h	32	ICSSM_PR1_CFG_SLV_CGR_REG	4802 6010h
14h	32	ICSSM_PR1_CFG_SLV_GPECFG0_REG	4802 6014h
18h	32	ICSSM_PR1_CFG_SLV_GPECFG1_REG	4802 6018h
1Ch	32	ICSSM_PR1_CFG_SLV_RESET_ISO_REG	4802 601Ch
2Ch	32	ICSSM_PR1_CFG_SLV_MII_RT_REG	4802 602Ch
30h	32	ICSSM_PR1_CFG_SLV_IEPCLK_REG	4802 6030h
34h	32	ICSSM_PR1_CFG_SLV_SPP_REG	4802 6034h
38h	32	ICSSM_PR1_CFG_SLV_SPIN_CFG_REG	4802 6038h
3Ch	32	ICSSM_PR1_CFG_SLV_CORE_SYNC_REG	4802 603Ch
40h	32	ICSSM_PR1_CFG_SLV_SA_MX_REG	4802 6040h
44h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_DIV_REG	4802 6044h
48h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG0	4802 6048h
4Ch	32	ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG0	4802 604Ch
50h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG1	4802 6050h
54h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG1	4802 6054h
58h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG2	4802 6058h
5Ch	32	ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG2	4802 605Ch
60h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG3	4802 6060h
64h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG3	4802 6064h
68h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG4	4802 6068h
6Ch	32	ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG4	4802 606Ch
70h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG5	4802 6070h
74h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG5	4802 6074h
78h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG6	4802 6078h
7Ch	32	ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG6	4802 607Ch
80h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG7	4802 6080h
84h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG7	4802 6084h
88h	32	ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG8	4802 6088h
8Ch	32	ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG8	4802 608Ch
90h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_DIV_REG	4802 6090h
94h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG0	4802 6094h
98h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG0	4802 6098h

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Table 4-1009. ICSSM_PR1_CFG_SLV Registers, Base Address=4802 6000h, Length=512 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
9Ch	32	ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG1	4802 609Ch
A0h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG1	4802 60A0h
A4h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG2	4802 60A4h
A8h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG2	4802 60A8h
ACh	32	ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG3	4802 60ACh
B0h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG3	4802 60B0h
B4h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG4	4802 60B4h
B8h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG4	4802 60B8h
BCh	32	ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG5	4802 60BCh
C0h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG5	4802 60C0h
C4h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG6	4802 60C4h
C8h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG6	4802 60C8h
CCh	32	ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG7	4802 60CCh
D0h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG7	4802 60D0h
D4h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG8	4802 60D4h
D8h	32	ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG8	4802 60D8h
E0h	32	ICSSM_PR1_CFG_SLV_PRU0_ED_RX_CFG_REG	4802 60E0h
E4h	32	ICSSM_PR1_CFG_SLV_PRU0_ED_TX_CFG_REG	4802 60E4h
E8h	32	ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG0_REG	4802 60E8h
ECh	32	ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG1_REG	4802 60ECh
F0h	32	ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG0_REG	4802 60F0h
F4h	32	ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG1_REG	4802 60F4h
F8h	32	ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG0_REG	4802 60F8h
FCh	32	ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG1_REG	4802 60FCh
100h	32	ICSSM_PR1_CFG_SLV_PRU1_ED_RX_CFG_REG	4802 6100h
104h	32	ICSSM_PR1_CFG_SLV_PRU1_ED_TX_CFG_REG	4802 6104h
108h	32	ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG0_REG	4802 6108h
10Ch	32	ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG1_REG	4802 610Ch
110h	32	ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG0_REG	4802 6110h
114h	32	ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG1_REG	4802 6114h
118h	32	ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG0_REG	4802 6118h
11Ch	32	ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG1_REG	4802 611Ch
124h	32	ICSSM_PR1_CFG_SLV_RTU0_POKE_EN0_REG	4802 6124h
12Ch	32	ICSSM_PR1_CFG_SLV_RTU1_POKE_EN0_REG	4802 612Ch
130h	32	ICSSM_PR1_CFG_SLV_PWM0	4802 6130h
134h	32	ICSSM_PR1_CFG_SLV_PWM1	4802 6134h
138h	32	ICSSM_PR1_CFG_SLV_PWM2	4802 6138h
13Ch	32	ICSSM_PR1_CFG_SLV_PWM3	4802 613Ch
140h	32	ICSSM_PR1_CFG_SLV_PWM0_0	4802 6140h
144h	32	ICSSM_PR1_CFG_SLV_PWM0_1	4802 6144h
148h	32	ICSSM_PR1_CFG_SLV_PWM0_2	4802 6148h
14Ch	32	ICSSM_PR1_CFG_SLV_PWM1_0	4802 614Ch
150h	32	ICSSM_PR1_CFG_SLV_PWM1_1	4802 6150h
154h	32	ICSSM_PR1_CFG_SLV_PWM1_2	4802 6154h
158h	32	ICSSM_PR1_CFG_SLV_PWM2_0	4802 6158h
15Ch	32	ICSSM_PR1_CFG_SLV_PWM2_1	4802 615Ch
160h	32	ICSSM_PR1_CFG_SLV_PWM2_2	4802 6160h

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Table 4-1009. ICSSM_PR1_CFG_SLV Registers, Base Address=4802 6000h, Length=512 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
164h	32	ICSSM_PR1_CFG_SLV_PWM3_0	4802 6164h
168h	32	ICSSM_PR1_CFG_SLV_PWM3_1	4802 6168h
16Ch	32	ICSSM_PR1_CFG_SLV_PWM3_2	4802 616Ch
170h	32	ICSSM_PR1_CFG_SLV_SPIN_LOCK0	4802 6170h
174h	32	ICSSM_PR1_CFG_SLV_SPIN_LOCK1	4802 6174h
178h	32	ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG0	4802 6178h
17Ch	32	ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT0	4802 617Ch
180h	32	ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG1	4802 6180h
184h	32	ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT1	4802 6184h
188h	32	ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG2	4802 6188h
18Ch	32	ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT2	4802 618Ch
190h	32	ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG3	4802 6190h
194h	32	ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT3	4802 6194h

Table 4-1010. ICSSM_PR1_ICSSS_UART_UART_SLV Registers, Base Address=4802 8000h, Length=64

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_RBR	4802 8000h
4h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_IER	4802 8004h
8h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_IIR	4802 8008h
Ch	32	ICSSM_PR1_ICSSS_UART_UART_SLV_LCR	4802 800Ch
10h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_MCR	4802 8010h
14h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_LSR	4802 8014h
18h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_MSR	4802 8018h
1Ch	32	ICSSM_PR1_ICSSS_UART_UART_SLV_SCR	4802 801Ch
20h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_DLL	4802 8020h
24h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_DLH	4802 8024h
28h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_REVID1	4802 8028h
30h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_PWREMU_MGMT	4802 8030h
34h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_MDR	4802 8034h
0h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_THR	4802 8000h
8h	32	ICSSM_PR1_ICSSS_UART_UART_SLV_FCR	4802 8008h
2Ch	32	ICSSM_PR1_ICSSS_UART_UART_SLV_REVID2	4802 802Ch

Table 4-1011. ICSSM_PR1_IEP0_SLV Registers, Base Address=4802 E000h, Length=4096

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_IEP0_SLV_GLOBAL_CFG_REG	4802 E000h
4h	32	ICSSM_PR1_IEP0_SLV_GLOBAL_STATUS_REG	4802 E004h
8h	32	ICSSM_PR1_IEP0_SLV_COMPEN_REG	4802 E008h
Ch	32	ICSSM_PR1_IEP0_SLV_SLOW_COMPEN_REG	4802 E00Ch
10h	32	ICSSM_PR1_IEP0_SLV_COUNT_REG0	4802 E010h
14h	32	ICSSM_PR1_IEP0_SLV_COUNT_REG1	4802 E014h
18h	32	ICSSM_PR1_IEP0_SLV_CAP_CFG_REG	4802 E018h
1Ch	32	ICSSM_PR1_IEP0_SLV_CAP_STATUS_REG	4802 E01Ch
20h	32	ICSSM_PR1_IEP0_SLV_CAPR0_REG0	4802 E020h
24h	32	ICSSM_PR1_IEP0_SLV_CAPR0_REG1	4802 E024h

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Table 4-1011. ICSSM_PR1_IEP0_SLV Registers, Base Address=4802 E000h, Length=4096 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
28h	32	ICSSM_PR1_IEP0_SLV_CAPR1_REG0	4802 E028h
2Ch	32	ICSSM_PR1_IEP0_SLV_CAPR1_REG1	4802 E02Ch
30h	32	ICSSM_PR1_IEP0_SLV_CAPR2_REG0	4802 E030h
34h	32	ICSSM_PR1_IEP0_SLV_CAPR2_REG1	4802 E034h
38h	32	ICSSM_PR1_IEP0_SLV_CAPR3_REG0	4802 E038h
3Ch	32	ICSSM_PR1_IEP0_SLV_CAPR3_REG1	4802 E03Ch
40h	32	ICSSM_PR1_IEP0_SLV_CAPR4_REG0	4802 E040h
44h	32	ICSSM_PR1_IEP0_SLV_CAPR4_REG1	4802 E044h
48h	32	ICSSM_PR1_IEP0_SLV_CAPR5_REG0	4802 E048h
4Ch	32	ICSSM_PR1_IEP0_SLV_CAPR5_REG1	4802 E04Ch
50h	32	ICSSM_PR1_IEP0_SLV_CAPR6_REG0	4802 E050h
54h	32	ICSSM_PR1_IEP0_SLV_CAPR6_REG1	4802 E054h
58h	32	ICSSM_PR1_IEP0_SLV_CAPF6_REG0	4802 E058h
5Ch	32	ICSSM_PR1_IEP0_SLV_CAPF6_REG1	4802 E05Ch
60h	32	ICSSM_PR1_IEP0_SLV_CAPR7_REG0	4802 E060h
64h	32	ICSSM_PR1_IEP0_SLV_CAPR7_REG1	4802 E064h
68h	32	ICSSM_PR1_IEP0_SLV_CAPF7_REG0	4802 E068h
6Ch	32	ICSSM_PR1_IEP0_SLV_CAPF7_REG1	4802 E06Ch
70h	32	ICSSM_PR1_IEP0_SLV_CMP_CFG_REG	4802 E070h
74h	32	ICSSM_PR1_IEP0_SLV_CMP_STATUS_REG	4802 E074h
78h	32	ICSSM_PR1_IEP0_SLV_CMP0_REG0	4802 E078h
7Ch	32	ICSSM_PR1_IEP0_SLV_CMP0_REG1	4802 E07Ch
80h	32	ICSSM_PR1_IEP0_SLV_CMP1_REG0	4802 E080h
84h	32	ICSSM_PR1_IEP0_SLV_CMP1_REG1	4802 E084h
88h	32	ICSSM_PR1_IEP0_SLV_CMP2_REG0	4802 E088h
8Ch	32	ICSSM_PR1_IEP0_SLV_CMP2_REG1	4802 E08Ch
90h	32	ICSSM_PR1_IEP0_SLV_CMP3_REG0	4802 E090h
94h	32	ICSSM_PR1_IEP0_SLV_CMP3_REG1	4802 E094h
98h	32	ICSSM_PR1_IEP0_SLV_CMP4_REG0	4802 E098h
9Ch	32	ICSSM_PR1_IEP0_SLV_CMP4_REG1	4802 E09Ch
A0h	32	ICSSM_PR1_IEP0_SLV_CMP5_REG0	4802 E0A0h
A4h	32	ICSSM_PR1_IEP0_SLV_CMP5_REG1	4802 E0A4h
A8h	32	ICSSM_PR1_IEP0_SLV_CMP6_REG0	4802 E0A8h
ACh	32	ICSSM_PR1_IEP0_SLV_CMP6_REG1	4802 E0ACh
B0h	32	ICSSM_PR1_IEP0_SLV_CMP7_REG0	4802 E0B0h
B4h	32	ICSSM_PR1_IEP0_SLV_CMP7_REG1	4802 E0B4h
B8h	32	ICSSM_PR1_IEP0_SLV_RXIPG0_REG	4802 E0B8h
BCh	32	ICSSM_PR1_IEP0_SLV_RXIPG1_REG	4802 E0BCh
C0h	32	ICSSM_PR1_IEP0_SLV_CMP8_REG0	4802 E0C0h
C4h	32	ICSSM_PR1_IEP0_SLV_CMP8_REG1	4802 E0C4h
C8h	32	ICSSM_PR1_IEP0_SLV_CMP9_REG0	4802 E0C8h
CCh	32	ICSSM_PR1_IEP0_SLV_CMP9_REG1	4802 E0CCh
D0h	32	ICSSM_PR1_IEP0_SLV_CMP10_REG0	4802 E0D0h
D4h	32	ICSSM_PR1_IEP0_SLV_CMP10_REG1	4802 E0D4h
D8h	32	ICSSM_PR1_IEP0_SLV_CMP11_REG0	4802 E0D8h
DCh	32	ICSSM_PR1_IEP0_SLV_CMP11_REG1	4802 E0DCh
E0h	32	ICSSM_PR1_IEP0_SLV_CMP12_REG0	4802 E0E0h

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Table 4-1011. ICSSM_PR1_IEP0_SLV Registers, Base Address=4802 E000h, Length=4096 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
E4h	32	ICSSM_PR1_IEP0_SLV_CMP12_REG1	4802 E0E4h
E8h	32	ICSSM_PR1_IEP0_SLV_CMP13_REG0	4802 E0E8h
ECh	32	ICSSM_PR1_IEP0_SLV_CMP13_REG1	4802 E0ECh
F0h	32	ICSSM_PR1_IEP0_SLV_CMP14_REG0	4802 E0F0h
F4h	32	ICSSM_PR1_IEP0_SLV_CMP14_REG1	4802 E0F4h
F8h	32	ICSSM_PR1_IEP0_SLV_CMP15_REG0	4802 E0F8h
FCh	32	ICSSM_PR1_IEP0_SLV_CMP15_REG1	4802 E0FCh
100h	32	ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG0	4802 E100h
104h	32	ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG1	4802 E104h
108h	32	ICSSM_PR1_IEP0_SLV_PWM_REG	4802 E108h
10Ch	32	ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG0	4802 E10Ch
110h	32	ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG1	4802 E110h
114h	32	ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG0	4802 E114h
118h	32	ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG1	4802 E118h
11Ch	32	ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG0	4802 E11Ch
120h	32	ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG1	4802 E120h
124h	32	ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG0	4802 E124h
128h	32	ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG1	4802 E128h
12Ch	32	ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG0	4802 E12Ch
130h	32	ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG1	4802 E130h
134h	32	ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG0	4802 E134h
138h	32	ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG1	4802 E138h
13Ch	32	ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG0	4802 E13Ch
140h	32	ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG1	4802 E140h
144h	32	ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG0	4802 E144h
148h	32	ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG1	4802 E148h
14Ch	32	ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG0	4802 E14Ch
150h	32	ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG1	4802 E150h
154h	32	ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG0	4802 E154h
158h	32	ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG1	4802 E158h
180h	32	ICSSM_PR1_IEP0_SLV_SYNC_CTRL_REG	4802 E180h
184h	32	ICSSM_PR1_IEP0_SLV_SYNC_FIRST_STAT_REG	4802 E184h
188h	32	ICSSM_PR1_IEP0_SLV_SYNC0_STAT_REG	4802 E188h
18Ch	32	ICSSM_PR1_IEP0_SLV_SYNC1_STAT_REG	4802 E18Ch
190h	32	ICSSM_PR1_IEP0_SLV_SYNC_PWIDTH_REG	4802 E190h
194h	32	ICSSM_PR1_IEP0_SLV_SYNC0_PERIOD_REG	4802 E194h
198h	32	ICSSM_PR1_IEP0_SLV_SYNC1_DELAY_REG	4802 E198h
19Ch	32	ICSSM_PR1_IEP0_SLV_SYNC_START_REG	4802 E19Ch
200h	32	ICSSM_PR1_IEP0_SLV_WD_PREDIV_REG	4802 E200h
204h	32	ICSSM_PR1_IEP0_SLV_PDI_WD_TIM_REG	4802 E204h
208h	32	ICSSM_PR1_IEP0_SLV_PD_WD_TIM_REG	4802 E208h
20Ch	32	ICSSM_PR1_IEP0_SLV_WD_STATUS_REG	4802 E20Ch
210h	32	ICSSM_PR1_IEP0_SLV_WD_EXP_CNT_REG	4802 E210h
214h	32	ICSSM_PR1_IEP0_SLV_WD_CTRL_REG	4802 E214h
300h	32	ICSSM_PR1_IEP0_SLV_DIGIO_CTRL_REG	4802 E300h
304h	32	ICSSM_PR1_IEP0_SLV_DIGIO_STATUS_REG	4802 E304h
308h	32	ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_REG	4802 E308h

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Table 4-1011. ICSSM_PR1_IEP0_SLV Registers, Base Address=4802 E000h, Length=4096 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
30Ch	32	ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_RAW_REG	4802 E30Ch
310h	32	ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_REG	4802 E310h
314h	32	ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_EN_REG	4802 E314h
318h	32	ICSSM_PR1_IEP0_SLV_DIGIO_EXP_REG	4802 E318h

Table 4-1012. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV Registers, Base Address=4803 0000h, Length=256

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_TSCNT	4803 0000h
4h	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CNTPHS	4803 0004h
8h	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP1	4803 0008h
Ch	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP2	4803 000Ch
10h	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP3	4803 0010h
14h	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP4	4803 0014h
28h	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCTL2_ECCTL1	4803 0028h
2Ch	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFLG_ECEINT	4803 002Ch
30h	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCLR	4803 0030h
34h	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFRC	4803 0034h
5Ch	32	ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_REVID1	4803 005Ch

Table 4-1013. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG Registers, Base Address=4803 2000h, Length=256

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG0	4803 2000h
4h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG1	4803 2004h
10h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG0	4803 2010h
14h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG1	4803 2014h
20h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC0	4803 2020h
24h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC1	4803 2024h
30h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG0	4803 2030h
34h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG1	4803 2034h
38h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS0	4803 2038h
3Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS1	4803 203Ch
40h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS0	4803 2040h
44h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS1	4803 2044h
48h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT0	4803 2048h
4Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT1	4803 204Ch
50h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR0	4803 2050h
54h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR1	4803 2054h
60h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVEL0	4803 2060h
64h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVEL1	4803 2064h
68h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVEL0	4803 2068h
6Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVEL1	4803 206Ch

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Table 4-1014. ICSSM_PR1_MDIO_V1P7_MDIO Registers, Base Address=4803 2400h, Length=256

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_MDIO_V1P7_MDIO_MDIO_VERSION_REG	4803 2400h
4h	32	ICSSM_PR1_MDIO_V1P7_MDIO_CONTROL_REG	4803 2404h
8h	32	ICSSM_PR1_MDIO_V1P7_MDIO_ALIVE_REG	4803 2408h
Ch	32	ICSSM_PR1_MDIO_V1P7_MDIO_LINK_REG	4803 240Ch
10h	32	ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_RAW_REG	4803 2410h
14h	32	ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASKED_REG	4803 2414h
18h	32	ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_SET_REG	4803 2418h
1Ch	32	ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_CLEAR_REG	4803 241Ch
20h	32	ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_RAW_REG	4803 2420h
24h	32	ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASKED_REG	4803 2424h
28h	32	ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_SET_REG	4803 2428h
2Ch	32	ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_CLEAR_REG	4803 242Ch
30h	32	ICSSM_PR1_MDIO_V1P7_MDIO_MANUAL_IF_REG	4803 2430h
34h	32	ICSSM_PR1_MDIO_V1P7_MDIO_POLL_REG	4803 2434h
38h	32	ICSSM_PR1_MDIO_V1P7_MDIO_POLL_EN_REG	4803 2438h
3Ch	32	ICSSM_PR1_MDIO_V1P7_MDIO_CLAUS45_REG	4803 243Ch
40h	32	ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR0_REG	4803 2440h
44h	32	ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR1_REG	4803 2444h
80h	32	ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_ACCESS_REG_J	4803 2480h + formula
84h	32	ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_PHY_SEL_REG_J	4803 2484h + formula

Table 4-1015. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Registers, Base Address=4803 3000h, Length=4096

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_ICSS_G_CFG	4803 3000h
4h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_PREEMPT_CFG	4803 3004h
8h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1S_CFG	4803 3008h
Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1C_CFG	4803 300Ch
10h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_POOL_PTR_CFG	4803 3010h
14h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_TX_EARLY_EOF	4803 3014h
18h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_FRAG_CNT_CFG	4803 3018h
D00h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE0	4803 3D00h
D04h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE1	4803 3D04h
D08h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE2	4803 3D08h

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Table 4-1015. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Registers, Base Address=4803 3000h, Length=4096 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
D0Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE3	4803 3D0Ch
D10h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE4	4803 3D10h
D14h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE5	4803 3D14h
D18h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE6	4803 3D18h
D1Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE7	4803 3D1Ch
D20h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE8	4803 3D20h
D24h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE9	4803 3D24h
D28h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE10	4803 3D28h
D2Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE11	4803 3D2Ch
D30h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE12	4803 3D30h
D34h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE13	4803 3D34h
D38h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE14	4803 3D38h
D3Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE15	4803 3D3Ch
D40h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE16	4803 3D40h
D44h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE17	4803 3D44h
D48h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE18	4803 3D48h
D4Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE19	4803 3D4Ch
D50h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE20	4803 3D50h
D54h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE21	4803 3D54h
D58h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE22	4803 3D58h
D5Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE23	4803 3D5Ch
D60h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE24	4803 3D60h
D64h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE25	4803 3D64h
D68h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE26	4803 3D68h
D6Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE27	4803 3D6Ch
D70h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE28	4803 3D70h
D74h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE29	4803 3D74h

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Table 4-1015. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Registers, Base Address=4803 3000h, Length=4096 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
D78h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE30	4803 3D78h
D7Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE31	4803 3D7Ch
E00h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK0	4803 3E00h
E04h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK1	4803 3E04h
E08h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK2	4803 3E08h
E0Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK3	4803 3E0Ch
E10h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK4	4803 3E10h
E14h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK5	4803 3E14h
E18h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK6	4803 3E18h
E1Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK7	4803 3E1Ch
E20h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK8	4803 3E20h
E24h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK9	4803 3E24h
E28h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK10	4803 3E28h
E2Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK11	4803 3E2Ch
E30h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK12	4803 3E30h
E34h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK13	4803 3E34h
E38h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK14	4803 3E38h
E3Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK15	4803 3E3Ch
E40h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT0	4803 3E40h
E44h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT1	4803 3E44h
E48h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT2	4803 3E48h
E4Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT3	4803 3E4Ch
E50h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT4	4803 3E50h
E54h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT5	4803 3E54h
E58h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT6	4803 3E58h
E5Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT7	4803 3E5Ch
E60h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT8	4803 3E60h

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Table 4-1015. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G Registers, Base Address=4803 3000h, Length=4096 (continued)

Offset	Length	Register Name	ICSSM0 Physical Address
E64h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT9	4803 3E64h
E68h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT10	4803 3E68h
E6Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT11	4803 3E6Ch
E70h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT12	4803 3E70h
E74h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT13	4803 3E74h
E78h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT14	4803 3E78h
E7Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT15	4803 3E7Ch
E80h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT16	4803 3E80h
E84h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT17	4803 3E84h
E88h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT18	4803 3E88h
E8Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT19	4803 3E8Ch
E90h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT20	4803 3E90h
E94h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT21	4803 3E94h
E98h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT22	4803 3E98h
E9Ch	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT23	4803 3E9Ch
EA0h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT24	4803 3EA0h
EA4h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT25	4803 3EA4h
EA8h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT26	4803 3EA8h
EACh	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT27	4803 3EACh
EB0h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT28	4803 3EB0h
EB4h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT29	4803 3EB4h
EB8h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT30	4803 3EB8h
EBCh	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT31	4803 3EBCh
F40h	32	ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_RESET	4803 3F40h

Table 4-1016. ICSSM_PR1_PDSP0_IRAM_RAM Registers, Base Address=4803 4000h, Length=16384

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_PDSP0_IRAM_RAM_IRAM	4803 4000h

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Table 4-1017. ICSSM_PR1_PDSP1_IRAM_RAM Registers, Base Address=4803 8000h, Length=16384

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ICSSM_PR1_PDSP1_IRAM_RAM_IRAM	4803 8000h

Table 4-1018. ECC_AGGR Registers, Base Address=4810 0000h, Length=1024

Offset	Length	Register Name	ICSSM0 Physical Address
0h	32	ECC_AGGR_REV	4810 0000h
8h	32	ECC_AGGR_VECTOR	4810 0008h
Ch	32	ECC_AGGR_STAT	4810 000Ch
10h	32	ECC_AGGR_RESERVED_SVBUS_J	4810 0010h + formula
3Ch	32	ECC_AGGR_SEC_EOI_REG	4810 003Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	4810 0040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	4810 0080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	4810 00C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	4810 013Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	4810 0140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	4810 0180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	4810 01C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	4810 0200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	4810 0204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	4810 0208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	4810 020Ch

4.2.2 ICSSM Registers

ICSSM Registers

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4.2.2.1 ICSSM_DRAM0_SLV_RAM_RAM_REG_J Register

4.2.2.1.1 ICSSM_DRAM0_SLV_RAM_RAM_REG_J Register (Offset = 0h) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

Return to Summary Table

Table 4-1019. Instance Table

Instance Name	Physical Address
ICSSM0	4800 0000h + formula

Figure 4-487. ICSSM_DRAM0_SLV_RAM_RAM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 4-1020. ICSSM_DRAM0_SLV_RAM_RAM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte
23:16	BYTE2	R/W	0h	This is the UM byte
15:8	BYTE1	R/W	0h	This is the LM byte
7:0	BYTE0	R/W	0h	This is the LS byte

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4.2.2.2 ICSSM_DRAM1_SLV_RAM_RAM_REG_J Register

4.2.2.2.1 ICSSM_DRAM1_SLV_RAM_RAM_REG_J Register (Offset = 0h) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

Return to Summary Table

Table 4-1021. Instance Table

Instance Name	Physical Address
ICSSM0	4800 2000h + formula

Figure 4-488. ICSSM_DRAM1_SLV_RAM_RAM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 4-1022. ICSSM_DRAM1_SLV_RAM_RAM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte
23:16	BYTE2	R/W	0h	This is the UM byte
15:8	BYTE1	R/W	0h	This is the LM byte
7:0	BYTE0	R/W	0h	This is the LS byte

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4.2.2.3 RAT_SLICE0_PID Register

4.2.2.3.1 RAT_SLICE0_PID Register (Offset = 0h) [reset = 66803100h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 4-1023. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8000h

Figure 4-489. RAT_SLICE0_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		680h			
23	22	21	20	19	18	17	16
FUNC							
R							
680h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 4-1024. RAT_SLICE0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme
29:28	BU	R	2h	Business Unit: 10 = Processors
27:16	FUNC	R	680h	Module ID
15:11	RTL	R	6h	RTL revision. Will vary depending on release.
10:8	MAJOR	R	1h	Major revision
7:6	CUSTOM	R	0h	Custom
5:0	MINOR	R	0h	Minor revision

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4.2.2.4 RAT_SLICE0_CONFIG Register

4.2.2.4.1 RAT_SLICE0_CONFIG Register (Offset = 4h) [reset = 240106h]

The Config Register contains the configuration values for the module.

Return to Summary Table

Table 4-1025. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8004h

Figure 4-490. RAT_SLICE0_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
ADDR_WIDTH							
R							
24h							
15	14	13	12	11	10	9	8
ADDRS							
R							
1h							
7	6	5	4	3	2	1	0
REGIONS							
R							
6h							

Table 4-1026. RAT_SLICE0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	ADDR_WIDTH	R	24h	Number of address bits
15:8	ADDRS	R	1h	Number of addresses
7:0	REGIONS	R	6h	Number of regions

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4.2.2.5 RAT_SLICE0_DESTINATION_ID Register

4.2.2.5.1 RAT_SLICE0_DESTINATION_ID Register (Offset = 804h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 4-1027. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8804h

Figure 4-491. RAT_SLICE0_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 4-1028. RAT_SLICE0_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID.

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4.2.2.6 RAT_SLICE0_EXCEPTION_LOGGING_CONTROL Register

4.2.2.6.1 RAT_SLICE0_EXCEPTION_LOGGING_CONTROL Register (Offset = 820h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

Return to Summary Table

Table 4-1029. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8820h

Figure 4-492. RAT_SLICE0_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_INTR	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 4-1030. RAT_SLICE0_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

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4.2.2.7 RAT_SLICE0_EXCEPTION_LOGGING_HEADER0 Register

4.2.2.7.1 RAT_SLICE0_EXCEPTION_LOGGING_HEADER0 Register (Offset = 824h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 4-1031. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8824h

Figure 4-493. RAT_SLICE0_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 4-1032. RAT_SLICE0_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 4 = RAT.
23:8	SRC_ID	R	0h	Source ID.
7:0	DEST_ID	R	0h	Destination ID.

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4.2.2.8 RAT_SLICE0_EXCEPTION_LOGGING_HEADER1 Register

4.2.2.8.1 RAT_SLICE0_EXCEPTION_LOGGING_HEADER1 Register (Offset = 828h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

Return to Summary Table

Table 4-1033. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8828h

Figure 4-494. RAT_SLICE0_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1034. RAT_SLICE0_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group.
23:16	CODE	R	0h	Code. 1 = Boundary crossing error.
15:0	RESERVED	NONE	0h	Reserved

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4.2.2.9 RAT_SLICE0_EXCEPTION_LOGGING_DATA0 Register

4.2.2.9.1 RAT_SLICE0_EXCEPTION_LOGGING_DATA0 Register (Offset = 82Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 4-1035. Instance Table

Instance Name	Physical Address
ICSSM0	4800 882Ch

Figure 4-495. RAT_SLICE0_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 4-1036. RAT_SLICE0_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits.

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4.2.2.10 RAT_SLICE0_EXCEPTION_LOGGING_DATA1 Register

4.2.2.10.1 RAT_SLICE0_EXCEPTION_LOGGING_DATA1 Register (Offset = 830h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

Return to Summary Table

Table 4-1037. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8830h

Figure 4-496. RAT_SLICE0_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 4-1038. RAT_SLICE0_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 12 bits.

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4.2.2.11 RAT_SLICE0_EXCEPTION_LOGGING_DATA2 Register

4.2.2.11.1 RAT_SLICE0_EXCEPTION_LOGGING_DATA2 Register (Offset = 834h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

Return to Summary Table

Table 4-1039. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8834h

Figure 4-497. RAT_SLICE0_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 4-1040. RAT_SLICE0_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID.
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.
8	SECURE	R	0h	Secure.
7:0	PRIV_ID	R	0h	Priv ID.

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4.2.2.12 RAT_SLICE0_EXCEPTION_LOGGING_DATA3 Register

4.2.2.12.1 RAT_SLICE0_EXCEPTION_LOGGING_DATA3 Register (Offset = 838h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

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Table 4-1041. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8838h

Figure 4-498. RAT_SLICE0_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BYTECNT							
R							
0h							

Table 4-1042. RAT_SLICE0_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count.

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4.2.2.13 RAT_SLICE0_EXCEPTION_PEND_SET Register

4.2.2.13.1 RAT_SLICE0_EXCEPTION_PEND_SET Register (Offset = 840h) [reset = 0h]

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

Return to Summary Table

Table 4-1043. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8840h

Figure 4-499. RAT_SLICE0_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 4-1044. RAT_SLICE0_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal.

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4.2.2.14 RAT_SLICE0_EXCEPTION_PEND_CLEAR Register

4.2.2.14.1 RAT_SLICE0_EXCEPTION_PEND_CLEAR Register (Offset = 844h) [reset = 0h]

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

Return to Summary Table

Table 4-1045. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8844h

Figure 4-500. RAT_SLICE0_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 4-1046. RAT_SLICE0_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal.

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4.2.2.15 RAT_SLICE0_EXCEPTION_ENABLE_SET Register

4.2.2.15.1 RAT_SLICE0_EXCEPTION_ENABLE_SET Register (Offset = 848h) [reset = 0h]

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

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Table 4-1047. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8848h

Figure 4-501. RAT_SLICE0_EXCEPTION_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SET
NONE							R/W1TS
0h							0h

Table 4-1048. RAT_SLICE0_EXCEPTION_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_SET	R/W1TS	0h	Write a 1 to set the exception interrupt enable signal.

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4.2.2.16 RAT_SLICE0_EXCEPTION_ENABLE_CLEAR Register

4.2.2.16.1 RAT_SLICE0_EXCEPTION_ENABLE_CLEAR Register (Offset = 84Ch) [reset = 0h]

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

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Table 4-1049. Instance Table

Instance Name	Physical Address
ICSSM0	4800 884Ch

Figure 4-502. RAT_SLICE0_EXCEPTION_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 4-1050. RAT_SLICE0_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_CLR	R/W1TC	0h	Write a 1 to clear the exception interrupt enable signal.

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4.2.2.17 RAT_SLICE0_EOI_REG Register

4.2.2.17.1 RAT_SLICE0_EOI_REG Register (Offset = 850h) [reset = 0h]

EOI Register.

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Table 4-1051. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8850h

Figure 4-503. RAT_SLICE0_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 4-1052. RAT_SLICE0_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	EOI Register

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4.2.2.18 RAT_SLICE0_REGION_CTRL_J Register

4.2.2.18.1 RAT_SLICE0_REGION_CTRL_J Register (Offset = 20h) [reset = 0h]

The Control for Region a

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Table 4-1053. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8020h + formula

Figure 4-504. RAT_SLICE0_REGION_CTRL_j Name Register

31	30	29	28	27	26	25	24
EN	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		SIZE					
NONE		R/W					
0h		0h					

Table 4-1054. RAT_SLICE0_REGION_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable for the Region
30:6	RESERVED	NONE	0h	Reserved
5:0	SIZE	R/W	0h	Size of the Region in Address Bits. 0 = 1 byte, 1 = 2B, 2 = 4B, 3 = 8B, etc. up to 32 = 4GB.

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4.2.2.19 RAT_SLICE0_REGION_BASE_J Register

4.2.2.19.1 RAT_SLICE0_REGION_BASE_J Register (Offset = 24h) [reset = 0h]

The Base Address for Region a. This is the source address for matching to a region.

Return to Summary Table

Table 4-1055. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8024h + formula

Figure 4-505. RAT_SLICE0_REGION_BASE_j Name Register

31	30	29	28	27	26	25	24
BASE							
R/W							
0h							
23	22	21	20	19	18	17	16
BASE							
R/W							
0h							
15	14	13	12	11	10	9	8
BASE							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE							
R/W							
0h							

Table 4-1056. RAT_SLICE0_REGION_BASE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BASE	R/W	0h	Base Address for the Region. It must be aligned to the programmed size.

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4.2.2.20 RAT_SLICE0_REGION_TRANS_L_J Register

4.2.2.20.1 RAT_SLICE0_REGION_TRANS_L_J Register (Offset = 28h) [reset = 0h]

The Translated Lower Address Bits for Region a

Return to Summary Table

Table 4-1057. Instance Table

Instance Name	Physical Address
ICSSM0	4800 8028h + formula

Figure 4-506. RAT_SLICE0_REGION_TRANS_L_j Name Register

31	30	29	28	27	26	25	24
LOWER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOWER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOWER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOWER							
R/W							
0h							

Table 4-1058. RAT_SLICE0_REGION_TRANS_L_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOWER	R/W	0h	Translated Lower Address Bits for the Region. It must be aligned to the programmed size.

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4.2.2.21 RAT_SLICE0_REGION_TRANS_U_J Register

4.2.2.21.1 RAT_SLICE0_REGION_TRANS_U_J Register (Offset = 2Ch) [reset = 0h]

The Translated Upper Address Bits for Region a

Return to Summary Table

Table 4-1059. Instance Table

Instance Name	Physical Address
ICSSM0	4800 802Ch + formula

Figure 4-507. RAT_SLICE0_REGION_TRANS_U_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				UPPER			
NONE				R/W			
0h				0h			

Table 4-1060. RAT_SLICE0_REGION_TRANS_U_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	UPPER	R/W	0h	Translated Upper Address Bits for the Region

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4.2.2.22 RAT_SLICE1_PID Register

4.2.2.22.1 RAT_SLICE1_PID Register (Offset = 0h) [reset = 66803100h]

The Revision Register contains the major and minor revisions for the module.

Return to Summary Table

Table 4-1061. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9000h

Figure 4-508. RAT_SLICE1_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		680h			
23	22	21	20	19	18	17	16
FUNC							
R							
680h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 4-1062. RAT_SLICE1_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme
29:28	BU	R	2h	Business Unit: 10 = Processors
27:16	FUNC	R	680h	Module ID
15:11	RTL	R	6h	RTL revision. Will vary depending on release.
10:8	MAJOR	R	1h	Major revision
7:6	CUSTOM	R	0h	Custom
5:0	MINOR	R	0h	Minor revision

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4.2.2.23 RAT_SLICE1_CONFIG Register

4.2.2.23.1 RAT_SLICE1_CONFIG Register (Offset = 4h) [reset = 240106h]

The Config Register contains the configuration values for the module.

Return to Summary Table

Table 4-1063. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9004h

Figure 4-509. RAT_SLICE1_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
ADDR_WIDTH							
R							
24h							
15	14	13	12	11	10	9	8
ADDRS							
R							
1h							
7	6	5	4	3	2	1	0
REGIONS							
R							
6h							

Table 4-1064. RAT_SLICE1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	ADDR_WIDTH	R	24h	Number of address bits
15:8	ADDRS	R	1h	Number of addresses
7:0	REGIONS	R	6h	Number of regions

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4.2.2.24 RAT_SLICE1_DESTINATION_ID Register

4.2.2.24.1 RAT_SLICE1_DESTINATION_ID Register (Offset = 804h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

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Table 4-1065. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9804h

Figure 4-510. RAT_SLICE1_DESTINATION_ID Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R/W							
0h							

Table 4-1066. RAT_SLICE1_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DEST_ID	R/W	0h	The destination ID.

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4.2.2.25 RAT_SLICE1_EXCEPTION_LOGGING_CONTROL Register

4.2.2.25.1 RAT_SLICE1_EXCEPTION_LOGGING_CONTROL Register (Offset = 820h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

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Table 4-1067. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9820h

Figure 4-511. RAT_SLICE1_EXCEPTION_LOGGING_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						DISABLE_INTR	DISABLE_F
NONE						R/W	R/W
0h						0h	0h

Table 4-1068. RAT_SLICE1_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

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4.2.2.26 RAT_SLICE1_EXCEPTION_LOGGING_HEADER0 Register

4.2.2.26.1 RAT_SLICE1_EXCEPTION_LOGGING_HEADER0 Register (Offset = 824h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

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Table 4-1069. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9824h

Figure 4-512. RAT_SLICE1_EXCEPTION_LOGGING_HEADER0 Name Register

31	30	29	28	27	26	25	24
TYPE_F							
R							
0h							
23	22	21	20	19	18	17	16
SRC_ID							
R							
0h							
15	14	13	12	11	10	9	8
SRC_ID							
R							
0h							
7	6	5	4	3	2	1	0
DEST_ID							
R							
0h							

Table 4-1070. RAT_SLICE1_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TYPE_F	R	0h	Type. 4 = RAT.
23:8	SRC_ID	R	0h	Source ID.
7:0	DEST_ID	R	0h	Destination ID.

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4.2.2.27 RAT_SLICE1_EXCEPTION_LOGGING_HEADER1 Register

4.2.2.27.1 RAT_SLICE1_EXCEPTION_LOGGING_HEADER1 Register (Offset = 828h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

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Table 4-1071. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9828h

Figure 4-513. RAT_SLICE1_EXCEPTION_LOGGING_HEADER1 Name Register

31	30	29	28	27	26	25	24
GROUP							
R							
0h							
23	22	21	20	19	18	17	16
CODE							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1072. RAT_SLICE1_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	GROUP	R	0h	Group.
23:16	CODE	R	0h	Code. 1 = Boundary crossing error.
15:0	RESERVED	NONE	0h	Reserved

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4.2.2.28 RAT_SLICE1_EXCEPTION_LOGGING_DATA0 Register

4.2.2.28.1 RAT_SLICE1_EXCEPTION_LOGGING_DATA0 Register (Offset = 82Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

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Table 4-1073. Instance Table

Instance Name	Physical Address
ICSSM0	4800 982Ch

Figure 4-514. RAT_SLICE1_EXCEPTION_LOGGING_DATA0 Name Register

31	30	29	28	27	26	25	24
ADDR_L							
R							
0h							
23	22	21	20	19	18	17	16
ADDR_L							
R							
0h							
15	14	13	12	11	10	9	8
ADDR_L							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_L							
R							
0h							

Table 4-1074. RAT_SLICE1_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_L	R	0h	Address lower 32 bits.

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4.2.2.29 RAT_SLICE1_EXCEPTION_LOGGING_DATA1 Register

4.2.2.29.1 RAT_SLICE1_EXCEPTION_LOGGING_DATA1 Register (Offset = 830h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

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Table 4-1075. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9830h

Figure 4-515. RAT_SLICE1_EXCEPTION_LOGGING_DATA1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ADDR_H							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_H							
R							
0h							

Table 4-1076. RAT_SLICE1_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ADDR_H	R	0h	Address upper 12 bits.

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4.2.2.30 RAT_SLICE1_EXCEPTION_LOGGING_DATA2 Register

4.2.2.30.1 RAT_SLICE1_EXCEPTION_LOGGING_DATA2 Register (Offset = 834h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

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Table 4-1077. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9834h

Figure 4-516. RAT_SLICE1_EXCEPTION_LOGGING_DATA2 Name Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
NONE				R			
0h				0h			
23	22	21	20	19	18	17	16
ROUTEID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
PRIV_ID							
R							
0h							

Table 4-1078. RAT_SLICE1_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	ROUTEID	R	0h	Route ID.
15:14	RESERVED	NONE	0h	Reserved
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.
8	SECURE	R	0h	Secure.
7:0	PRIV_ID	R	0h	Priv ID.

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4.2.2.31 RAT_SLICE1_EXCEPTION_LOGGING_DATA3 Register

4.2.2.31.1 RAT_SLICE1_EXCEPTION_LOGGING_DATA3 Register (Offset = 838h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

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Table 4-1079. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9838h

Figure 4-517. RAT_SLICE1_EXCEPTION_LOGGING_DATA3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
BYTECNT							
R							
0h							

Table 4-1080. RAT_SLICE1_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	BYTECNT	R	0h	Byte count.

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4.2.2.32 RAT_SLICE1_EXCEPTION_PEND_SET Register

4.2.2.32.1 RAT_SLICE1_EXCEPTION_PEND_SET Register (Offset = 840h) [reset = 0h]

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

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Table 4-1081. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9840h

Figure 4-518. RAT_SLICE1_EXCEPTION_PEND_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
NONE							R/W1TS
0h							0h

Table 4-1082. RAT_SLICE1_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_SET	R/W1TS	0h	Write a 1 to set the exception pend signal.

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4.2.2.33 RAT_SLICE1_EXCEPTION_PEND_CLEAR Register

4.2.2.33.1 RAT_SLICE1_EXCEPTION_PEND_CLEAR Register (Offset = 844h) [reset = 0h]

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

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Table 4-1083. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9844h

Figure 4-519. RAT_SLICE1_EXCEPTION_PEND_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
NONE							R/W1TC
0h							0h

Table 4-1084. RAT_SLICE1_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	PEND_CLR	R/W1TC	0h	Write a 1 to clear the exception pend signal.

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4.2.2.34 RAT_SLICE1_EXCEPTION_ENABLE_SET Register

4.2.2.34.1 RAT_SLICE1_EXCEPTION_ENABLE_SET Register (Offset = 848h) [reset = 0h]

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

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Table 4-1085. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9848h

Figure 4-520. RAT_SLICE1_EXCEPTION_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SET
NONE							R/W1TS
0h							0h

Table 4-1086. RAT_SLICE1_EXCEPTION_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_SET	R/W1TS	0h	Write a 1 to set the exception interrupt enable signal.

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4.2.2.35 RAT_SLICE1_EXCEPTION_ENABLE_CLEAR Register

4.2.2.35.1 RAT_SLICE1_EXCEPTION_ENABLE_CLEAR Register (Offset = 84Ch) [reset = 0h]

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

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Table 4-1087. Instance Table

Instance Name	Physical Address
ICSSM0	4800 984Ch

Figure 4-521. RAT_SLICE1_EXCEPTION_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 4-1088. RAT_SLICE1_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_CLR	R/W1TC	0h	Write a 1 to clear the exception interrupt enable signal.

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4.2.2.36 RAT_SLICE1_EOI_REG Register

4.2.2.36.1 RAT_SLICE1_EOI_REG Register (Offset = 850h) [reset = 0h]

EOI Register.

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Table 4-1089. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9850h

Figure 4-522. RAT_SLICE1_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EOI_WR							
R/W							
0h							
7	6	5	4	3	2	1	0
EOI_WR							
R/W							
0h							

Table 4-1090. RAT_SLICE1_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	EOI_WR	R/W	0h	EOI Register

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4.2.2.37 RAT_SLICE1_REGION_CTRL_J Register

4.2.2.37.1 RAT_SLICE1_REGION_CTRL_J Register (Offset = 20h) [reset = 0h]

The Control for Region a

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Table 4-1091. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9020h + formula

Figure 4-523. RAT_SLICE1_REGION_CTRL_j Name Register

31	30	29	28	27	26	25	24
EN	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		SIZE					
NONE		R/W					
0h		0h					

Table 4-1092. RAT_SLICE1_REGION_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable for the Region
30:6	RESERVED	NONE	0h	Reserved
5:0	SIZE	R/W	0h	Size of the Region in Address Bits. 0 = 1 byte, 1 = 2B, 2 = 4B, 3 = 8B, etc. up to 32 = 4GB.

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4.2.2.38 RAT_SLICE1_REGION_BASE_J Register

4.2.2.38.1 RAT_SLICE1_REGION_BASE_J Register (Offset = 24h) [reset = 0h]

The Base Address for Region a. This is the source address for matching to a region.

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Table 4-1093. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9024h + formula

Figure 4-524. RAT_SLICE1_REGION_BASE_j Name Register

31	30	29	28	27	26	25	24
BASE							
R/W							
0h							
23	22	21	20	19	18	17	16
BASE							
R/W							
0h							
15	14	13	12	11	10	9	8
BASE							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE							
R/W							
0h							

Table 4-1094. RAT_SLICE1_REGION_BASE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BASE	R/W	0h	Base Address for the Region. It must be aligned to the programmed size.

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4.2.2.39 RAT_SLICE1_REGION_TRANS_L_J Register

4.2.2.39.1 RAT_SLICE1_REGION_TRANS_L_J Register (Offset = 28h) [reset = 0h]

The Translated Lower Address Bits for Region a

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Table 4-1095. Instance Table

Instance Name	Physical Address
ICSSM0	4800 9028h + formula

Figure 4-525. RAT_SLICE1_REGION_TRANS_L_j Name Register

31	30	29	28	27	26	25	24
LOWER							
R/W							
0h							
23	22	21	20	19	18	17	16
LOWER							
R/W							
0h							
15	14	13	12	11	10	9	8
LOWER							
R/W							
0h							
7	6	5	4	3	2	1	0
LOWER							
R/W							
0h							

Table 4-1096. RAT_SLICE1_REGION_TRANS_L_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LOWER	R/W	0h	Translated Lower Address Bits for the Region. It must be aligned to the programmed size.

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4.2.2.40 RAT_SLICE1_REGION_TRANS_U_J Register

4.2.2.40.1 RAT_SLICE1_REGION_TRANS_U_J Register (Offset = 2Ch) [reset = 0h]

The Translated Upper Address Bits for Region a

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Table 4-1097. Instance Table

Instance Name	Physical Address
ICSSM0	4800 902Ch + formula

Figure 4-526. RAT_SLICE1_REGION_TRANS_U_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				UPPER			
NONE				R/W			
0h				0h			

Table 4-1098. RAT_SLICE1_REGION_TRANS_U_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	UPPER	R/W	0h	Translated Upper Address Bits for the Region

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4.2.2.41 ICSSM_RAM_SLV_RAM_RAM_REG_J Register

4.2.2.41.1 ICSSM_RAM_SLV_RAM_RAM_REG_J Register (Offset = 0h) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

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Table 4-1099. Instance Table

Instance Name	Physical Address
ICSSM0	4801 0000h + formula

Figure 4-527. ICSSM_RAM_SLV_RAM_RAM_REG_j Name Register

31	30	29	28	27	26	25	24
BYTE3							
R/W							
0h							
23	22	21	20	19	18	17	16
BYTE2							
R/W							
0h							
15	14	13	12	11	10	9	8
BYTE1							
R/W							
0h							
7	6	5	4	3	2	1	0
BYTE0							
R/W							
0h							

Table 4-1100. ICSSM_RAM_SLV_RAM_RAM_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	BYTE3	R/W	0h	This is the MS byte
23:16	BYTE2	R/W	0h	This is the UM byte
15:8	BYTE1	R/W	0h	This is the LM byte
7:0	BYTE0	R/W	0h	This is the LS byte

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4.2.2.42 ICSSM_PR1_ICSS_INTC_INTC_SLV_REVISION_REG Register

4.2.2.42.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_REVISION_REG Register (Offset = 0h) [reset = 4E82A900h]

Revision Register

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Table 4-1101. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0000h

Figure 4-528. ICSSM_PR1_ICSS_INTC_INTC_SLV_REVISION_REG Name Register

31	30	29	28	27	26	25	24
REV_SCHEME		RESERVED		REV_MODULE			
R		NONE		R			
1h		0h		E82h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REV_MODULE							
R							
E82h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REV_RTL					REV_MAJOR		
R					R		
15h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REV_CUSTOM		REV_MINOR					
R		R					
0h		0h					

Table 4-1102. ICSSM_PR1_ICSS_INTC_INTC_SLV_REVISION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	REV_SCHEME	R	1h	Scheme
29:28	RESERVED	NONE	0h	Reserved
27:16	REV_MODULE	R	E82h	Module ID
15:11	REV_RTL	R	15h	RTL revisions
10:8	REV_MAJOR	R	1h	Major revision
7:6	REV_CUSTOM	R	0h	Custom revision
5:0	REV_MINOR	R	0h	Minor revision

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4.2.2.43 ICSSM_PR1_ICSS_INTC_INTC_SLV_CONTROL_REG Register

4.2.2.43.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CONTROL_REG Register (Offset = 4h) [reset = 0h]

Control Register

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Table 4-1103. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0004h

Figure 4-529. ICSSM_PR1_ICSS_INTC_INTC_SLV_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PRIORITY_HOLD_MODE	NEST_MODE		WAKEUP_MODE	RESERVED
NONE			R/W	R/W		R/W	NONE
0h			0h	0h		0h	0h

Table 4-1104. ICSSM_PR1_ICSS_INTC_INTC_SLV_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	PRIORITY_HOLD_MODE	R/W	0h	Priority Holding Mode
3:2	NEST_MODE	R/W	0h	Nesting Mode
1	WAKEUP_MODE	R/W	0h	Wakeup mode enable
0	RESERVED	NONE	0h	Reserved

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4.2.2.44 ICSSM_PR1_ICSS_INTC_INTC_SLV_GLOBAL_ENABLE_HINT_REG Register

4.2.2.44.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_GLOBAL_ENABLE_HINT_REG Register (Offset = 10h) [reset = 0h]

Global Host Int Enable Register

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Table 4-1105. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0010h

Figure 4-530. ICSSM_PR1_ICSS_INTC_INTC_SLV_GLOBAL_ENABLE_HINT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_HINT_ANY
NONE							R/W
0h							0h

Table 4-1106. ICSSM_PR1_ICSS_INTC_INTC_SLV_GLOBAL_ENABLE_HINT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	ENABLE_HINT_ANY	R/W	0h	Global Enable for all Host Ints

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4.2.2.45 ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_NEST_LEVEL_REG Register

4.2.2.45.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_NEST_LEVEL_REG Register (Offset = 1Ch) [reset = 100h]

Global Nesting Level Register

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Table 4-1107. Instance Table

Instance Name	Physical Address
ICSSM0	4802 001Ch

Figure 4-531. ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_NEST_LEVEL_REG Name Register

31	30	29	28	27	26	25	24
GLB_NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							GLB_NEST_LEVEL
NONE							R/W
0h							100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GLB_NEST_LEVEL							
R/W							
100h							

Table 4-1108. ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_NEST_LEVEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GLB_NEST_AUTO_OVR	W	0h	Global Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	GLB_NEST_LEVEL	R/W	100h	Global Nesting Level

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4.2.2.46 ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_SET_INDEX_REG Register

4.2.2.46.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_SET_INDEX_REG Register (Offset = 20h) [reset = 0h]

Status Set Index Register

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Table 4-1109. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0020h

Figure 4-532. ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_SET_INDEX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						STATUS_SET_INDEX	
NONE						W	
0h						0h	
7	6	5	4	3	2	1	0
STATUS_SET_INDEX							
W							
0h							

Table 4-1110. ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_SET_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	STATUS_SET_INDEX	W	0h	Status Set Index Register (write index to set status of)

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4.2.2.47 ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_CLR_INDEX_REG Register

4.2.2.47.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_CLR_INDEX_REG Register (Offset = 24h) [reset = 0h]

Status Clear Index Register

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Table 4-1111. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0024h

Figure 4-533. ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_CLR_INDEX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						STATUS_CLR_INDEX	
NONE						W	
0h						0h	
7	6	5	4	3	2	1	0
STATUS_CLR_INDEX							
W							
0h							

Table 4-1112. ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_CLR_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	STATUS_CLR_INDEX	W	0h	Status Clear Index Register (write index to clear status of)

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4.2.2.48 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_SET_INDEX_REG Register

4.2.2.48.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_SET_INDEX_REG Register (Offset = 28h) [reset = 0h]

Enable Set Index Register

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Table 4-1113. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0028h

Figure 4-534. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_SET_INDEX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						ENABLE_SET_INDEX	
NONE						W1TS	
0h						0h	
7	6	5	4	3	2	1	0
ENABLE_SET_INDEX							
W1TS							
0h							

Table 4-1114. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_SET_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	ENABLE_SET_INDEX	W1TS	0h	Enable Set Index Register (write index to set enable of)

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4.2.2.49 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_INDEX_REG Register

4.2.2.49.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_INDEX_REG Register (Offset = 2Ch) [reset = 0h]

Enable Clear Index Register

Return to Summary Table

Table 4-1115. Instance Table

Instance Name	Physical Address
ICSSM0	4802 002Ch

Figure 4-535. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_INDEX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						ENABLE_CLR_INDEX	
NONE						W1TC	
0h						0h	
7	6	5	4	3	2	1	0
ENABLE_CLR_INDEX							
W1TC							
0h							

Table 4-1116. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	ENABLE_CLR_INDEX	W1TC	0h	Enable Clear Index Register (write index to clear enable of)

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4.2.2.50 ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_SET_INDEX_REG Register

4.2.2.50.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_SET_INDEX_REG Register (Offset = 34h) [reset = 0h]

Host Int Enable Set Index Register

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Table 4-1117. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0034h

Figure 4-536. ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_SET_INDEX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						HINT_ENABLE_SET_INDEX	
NONE						W1TS	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HINT_ENABLE_SET_INDEX							
W1TS							
0h							

Table 4-1118. ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_SET_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	HINT_ENABLE_SET_INDEX	W1TS	0h	Enable set for Host Interrupts

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4.2.2.51 ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_CLR_INDEX_REG Register

4.2.2.51.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_CLR_INDEX_REG Register (Offset = 38h) [reset = 0h]

Host Int Enable Clear Index Register

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Table 4-1119. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0038h

Figure 4-537. ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_CLR_INDEX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						HINT_ENABLE_CLR_INDEX	
NONE						W1TC	
0h						0h	
7	6	5	4	3	2	1	0
HINT_ENABLE_CLR_INDEX							
W1TC							
0h							

Table 4-1120. ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_CLR_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	HINT_ENABLE_CLR_INDEX	W1TC	0h	Enable clear for Host Interrupts

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4.2.2.52 ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_PRI_INTR_REG Register

4.2.2.52.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_PRI_INTR_REG Register (Offset = 80h) [reset = 80000000h]

Global Prioritized Interrupt Register

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Table 4-1121. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0080h

Figure 4-538. ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_PRI_INTR_REG Name Register

31	30	29	28	27	26	25	24
GLB_NONE	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						GLB_PRI_INTR	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
GLB_PRI_INTR							
R							
0h							

Table 4-1122. ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_PRI_INTR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GLB_NONE	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	GLB_PRI_INTR	R	0h	Prioritized Interrupt

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4.2.2.53 ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG0 Register

4.2.2.53.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG0 Register (Offset = 200h) [reset = 0h]

Raw Status Register 0

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Table 4-1123. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0200h

Figure 4-539. ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RAW_STATUS_31	RAW_STATUS_30	RAW_STATUS_29	RAW_STATUS_28	RAW_STATUS_27	RAW_STATUS_26	RAW_STATUS_25	RAW_STATUS_24
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RAW_STATUS_23	RAW_STATUS_22	RAW_STATUS_21	RAW_STATUS_20	RAW_STATUS_19	RAW_STATUS_18	RAW_STATUS_17	RAW_STATUS_16
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAW_STATUS_15	RAW_STATUS_14	RAW_STATUS_13	RAW_STATUS_12	RAW_STATUS_11	RAW_STATUS_10	RAW_STATUS_9	RAW_STATUS_8
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAW_STATUS_7	RAW_STATUS_6	RAW_STATUS_5	RAW_STATUS_4	RAW_STATUS_3	RAW_STATUS_2	RAW_STATUS_1	RAW_STATUS_0
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1124. ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_31	W1TS	0h	Raw Status (write 1 to set) for intr_in[31]
30	RAW_STATUS_30	W1TS	0h	Raw Status (write 1 to set) for intr_in[30]
29	RAW_STATUS_29	W1TS	0h	Raw Status (write 1 to set) for intr_in[29]
28	RAW_STATUS_28	W1TS	0h	Raw Status (write 1 to set) for intr_in[28]
27	RAW_STATUS_27	W1TS	0h	Raw Status (write 1 to set) for intr_in[27]
26	RAW_STATUS_26	W1TS	0h	Raw Status (write 1 to set) for intr_in[26]
25	RAW_STATUS_25	W1TS	0h	Raw Status (write 1 to set) for intr_in[25]
24	RAW_STATUS_24	W1TS	0h	Raw Status (write 1 to set) for intr_in[24]
23	RAW_STATUS_23	W1TS	0h	Raw Status (write 1 to set) for intr_in[23]
22	RAW_STATUS_22	W1TS	0h	Raw Status (write 1 to set) for intr_in[22]
21	RAW_STATUS_21	W1TS	0h	Raw Status (write 1 to set) for intr_in[21]
20	RAW_STATUS_20	W1TS	0h	Raw Status (write 1 to set) for intr_in[20]
19	RAW_STATUS_19	W1TS	0h	Raw Status (write 1 to set) for intr_in[19]
18	RAW_STATUS_18	W1TS	0h	Raw Status (write 1 to set) for intr_in[18]
17	RAW_STATUS_17	W1TS	0h	Raw Status (write 1 to set) for intr_in[17]
16	RAW_STATUS_16	W1TS	0h	Raw Status (write 1 to set) for intr_in[16]
15	RAW_STATUS_15	W1TS	0h	Raw Status (write 1 to set) for intr_in[15]

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Table 4-1124. ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RAW_STATUS_14	W1TS	0h	Raw Status (write 1 to set) for intr_in[14]
13	RAW_STATUS_13	W1TS	0h	Raw Status (write 1 to set) for intr_in[13]
12	RAW_STATUS_12	W1TS	0h	Raw Status (write 1 to set) for intr_in[12]
11	RAW_STATUS_11	W1TS	0h	Raw Status (write 1 to set) for intr_in[11]
10	RAW_STATUS_10	W1TS	0h	Raw Status (write 1 to set) for intr_in[10]
9	RAW_STATUS_9	W1TS	0h	Raw Status (write 1 to set) for intr_in[9]
8	RAW_STATUS_8	W1TS	0h	Raw Status (write 1 to set) for intr_in[8]
7	RAW_STATUS_7	W1TS	0h	Raw Status (write 1 to set) for intr_in[7]
6	RAW_STATUS_6	W1TS	0h	Raw Status (write 1 to set) for intr_in[6]
5	RAW_STATUS_5	W1TS	0h	Raw Status (write 1 to set) for intr_in[5]
4	RAW_STATUS_4	W1TS	0h	Raw Status (write 1 to set) for intr_in[4]
3	RAW_STATUS_3	W1TS	0h	Raw Status (write 1 to set) for intr_in[3]
2	RAW_STATUS_2	W1TS	0h	Raw Status (write 1 to set) for intr_in[2]
1	RAW_STATUS_1	W1TS	0h	Raw Status (write 1 to set) for intr_in[1]
0	RAW_STATUS_0	W1TS	0h	Raw Status (write 1 to set) for intr_in[0]

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4.2.2.54 ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG1 Register

4.2.2.54.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG1 Register (Offset = 204h) [reset = 0h]

Raw Status Register 1

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Table 4-1125. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0204h

Figure 4-540. ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG1 Name Register

31	30	29	28	27	26	25	24
RAW_STATUS_63	RAW_STATUS_62	RAW_STATUS_61	RAW_STATUS_60	RAW_STATUS_59	RAW_STATUS_58	RAW_STATUS_57	RAW_STATUS_56
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RAW_STATUS_55	RAW_STATUS_54	RAW_STATUS_53	RAW_STATUS_52	RAW_STATUS_51	RAW_STATUS_50	RAW_STATUS_49	RAW_STATUS_48
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAW_STATUS_47	RAW_STATUS_46	RAW_STATUS_45	RAW_STATUS_44	RAW_STATUS_43	RAW_STATUS_42	RAW_STATUS_41	RAW_STATUS_40
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAW_STATUS_39	RAW_STATUS_38	RAW_STATUS_37	RAW_STATUS_36	RAW_STATUS_35	RAW_STATUS_34	RAW_STATUS_33	RAW_STATUS_32
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1126. ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RAW_STATUS_63	W1TS	0h	Raw Status (write 1 to set) for intr_in[63]
30	RAW_STATUS_62	W1TS	0h	Raw Status (write 1 to set) for intr_in[62]
29	RAW_STATUS_61	W1TS	0h	Raw Status (write 1 to set) for intr_in[61]
28	RAW_STATUS_60	W1TS	0h	Raw Status (write 1 to set) for intr_in[60]
27	RAW_STATUS_59	W1TS	0h	Raw Status (write 1 to set) for intr_in[59]
26	RAW_STATUS_58	W1TS	0h	Raw Status (write 1 to set) for intr_in[58]
25	RAW_STATUS_57	W1TS	0h	Raw Status (write 1 to set) for intr_in[57]
24	RAW_STATUS_56	W1TS	0h	Raw Status (write 1 to set) for intr_in[56]
23	RAW_STATUS_55	W1TS	0h	Raw Status (write 1 to set) for intr_in[55]
22	RAW_STATUS_54	W1TS	0h	Raw Status (write 1 to set) for intr_in[54]
21	RAW_STATUS_53	W1TS	0h	Raw Status (write 1 to set) for intr_in[53]
20	RAW_STATUS_52	W1TS	0h	Raw Status (write 1 to set) for intr_in[52]
19	RAW_STATUS_51	W1TS	0h	Raw Status (write 1 to set) for intr_in[51]
18	RAW_STATUS_50	W1TS	0h	Raw Status (write 1 to set) for intr_in[50]
17	RAW_STATUS_49	W1TS	0h	Raw Status (write 1 to set) for intr_in[49]
16	RAW_STATUS_48	W1TS	0h	Raw Status (write 1 to set) for intr_in[48]
15	RAW_STATUS_47	W1TS	0h	Raw Status (write 1 to set) for intr_in[47]

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Table 4-1126. ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RAW_STATUS_46	W1TS	0h	Raw Status (write 1 to set) for intr_in[46]
13	RAW_STATUS_45	W1TS	0h	Raw Status (write 1 to set) for intr_in[45]
12	RAW_STATUS_44	W1TS	0h	Raw Status (write 1 to set) for intr_in[44]
11	RAW_STATUS_43	W1TS	0h	Raw Status (write 1 to set) for intr_in[43]
10	RAW_STATUS_42	W1TS	0h	Raw Status (write 1 to set) for intr_in[42]
9	RAW_STATUS_41	W1TS	0h	Raw Status (write 1 to set) for intr_in[41]
8	RAW_STATUS_40	W1TS	0h	Raw Status (write 1 to set) for intr_in[40]
7	RAW_STATUS_39	W1TS	0h	Raw Status (write 1 to set) for intr_in[39]
6	RAW_STATUS_38	W1TS	0h	Raw Status (write 1 to set) for intr_in[38]
5	RAW_STATUS_37	W1TS	0h	Raw Status (write 1 to set) for intr_in[37]
4	RAW_STATUS_36	W1TS	0h	Raw Status (write 1 to set) for intr_in[36]
3	RAW_STATUS_35	W1TS	0h	Raw Status (write 1 to set) for intr_in[35]
2	RAW_STATUS_34	W1TS	0h	Raw Status (write 1 to set) for intr_in[34]
1	RAW_STATUS_33	W1TS	0h	Raw Status (write 1 to set) for intr_in[33]
0	RAW_STATUS_32	W1TS	0h	Raw Status (write 1 to set) for intr_in[32]

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4.2.2.55 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG0 Register

4.2.2.55.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG0 Register (Offset = 280h) [reset = 0h]

Enabled Status Register 0

Return to Summary Table

Table 4-1127. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0280h

Figure 4-541. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
ENA_STATUS_31	ENA_STATUS_30	ENA_STATUS_29	ENA_STATUS_28	ENA_STATUS_27	ENA_STATUS_26	ENA_STATUS_25	ENA_STATUS_24
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
ENA_STATUS_23	ENA_STATUS_22	ENA_STATUS_21	ENA_STATUS_20	ENA_STATUS_19	ENA_STATUS_18	ENA_STATUS_17	ENA_STATUS_16
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ENA_STATUS_15	ENA_STATUS_14	ENA_STATUS_13	ENA_STATUS_12	ENA_STATUS_11	ENA_STATUS_10	ENA_STATUS_9	ENA_STATUS_8
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ENA_STATUS_7	ENA_STATUS_6	ENA_STATUS_5	ENA_STATUS_4	ENA_STATUS_3	ENA_STATUS_2	ENA_STATUS_1	ENA_STATUS_0
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1128. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_31	W1TC	0h	Enabled Status for intr_in[31]
30	ENA_STATUS_30	W1TC	0h	Enabled Status for intr_in[30]
29	ENA_STATUS_29	W1TC	0h	Enabled Status for intr_in[29]
28	ENA_STATUS_28	W1TC	0h	Enabled Status for intr_in[28]
27	ENA_STATUS_27	W1TC	0h	Enabled Status for intr_in[27]
26	ENA_STATUS_26	W1TC	0h	Enabled Status for intr_in[26]
25	ENA_STATUS_25	W1TC	0h	Enabled Status for intr_in[25]
24	ENA_STATUS_24	W1TC	0h	Enabled Status for intr_in[24]
23	ENA_STATUS_23	W1TC	0h	Enabled Status for intr_in[23]
22	ENA_STATUS_22	W1TC	0h	Enabled Status for intr_in[22]
21	ENA_STATUS_21	W1TC	0h	Enabled Status for intr_in[21]
20	ENA_STATUS_20	W1TC	0h	Enabled Status for intr_in[20]
19	ENA_STATUS_19	W1TC	0h	Enabled Status for intr_in[19]
18	ENA_STATUS_18	W1TC	0h	Enabled Status for intr_in[18]
17	ENA_STATUS_17	W1TC	0h	Enabled Status for intr_in[17]
16	ENA_STATUS_16	W1TC	0h	Enabled Status for intr_in[16]
15	ENA_STATUS_15	W1TC	0h	Enabled Status for intr_in[15]

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Table 4-1128. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ENA_STATUS_14	W1TC	0h	Enabled Status for intr_in[14]
13	ENA_STATUS_13	W1TC	0h	Enabled Status for intr_in[13]
12	ENA_STATUS_12	W1TC	0h	Enabled Status for intr_in[12]
11	ENA_STATUS_11	W1TC	0h	Enabled Status for intr_in[11]
10	ENA_STATUS_10	W1TC	0h	Enabled Status for intr_in[10]
9	ENA_STATUS_9	W1TC	0h	Enabled Status for intr_in[9]
8	ENA_STATUS_8	W1TC	0h	Enabled Status for intr_in[8]
7	ENA_STATUS_7	W1TC	0h	Enabled Status for intr_in[7]
6	ENA_STATUS_6	W1TC	0h	Enabled Status for intr_in[6]
5	ENA_STATUS_5	W1TC	0h	Enabled Status for intr_in[5]
4	ENA_STATUS_4	W1TC	0h	Enabled Status for intr_in[4]
3	ENA_STATUS_3	W1TC	0h	Enabled Status for intr_in[3]
2	ENA_STATUS_2	W1TC	0h	Enabled Status for intr_in[2]
1	ENA_STATUS_1	W1TC	0h	Enabled Status for intr_in[1]
0	ENA_STATUS_0	W1TC	0h	Enabled Status for intr_in[0]

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4.2.2.56 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG1 Register

4.2.2.56.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG1 Register (Offset = 284h) [reset = 0h]

Enabled Status Register 1

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Table 4-1129. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0284h

Figure 4-542. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG1 Name Register

31	30	29	28	27	26	25	24
ENA_STATUS_63	ENA_STATUS_62	ENA_STATUS_61	ENA_STATUS_60	ENA_STATUS_59	ENA_STATUS_58	ENA_STATUS_57	ENA_STATUS_56
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
ENA_STATUS_55	ENA_STATUS_54	ENA_STATUS_53	ENA_STATUS_52	ENA_STATUS_51	ENA_STATUS_50	ENA_STATUS_49	ENA_STATUS_48
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ENA_STATUS_47	ENA_STATUS_46	ENA_STATUS_45	ENA_STATUS_44	ENA_STATUS_43	ENA_STATUS_42	ENA_STATUS_41	ENA_STATUS_40
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ENA_STATUS_39	ENA_STATUS_38	ENA_STATUS_37	ENA_STATUS_36	ENA_STATUS_35	ENA_STATUS_34	ENA_STATUS_33	ENA_STATUS_32
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1130. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENA_STATUS_63	W1TC	0h	Enabled Status for intr_in[63]
30	ENA_STATUS_62	W1TC	0h	Enabled Status for intr_in[62]
29	ENA_STATUS_61	W1TC	0h	Enabled Status for intr_in[61]
28	ENA_STATUS_60	W1TC	0h	Enabled Status for intr_in[60]
27	ENA_STATUS_59	W1TC	0h	Enabled Status for intr_in[59]
26	ENA_STATUS_58	W1TC	0h	Enabled Status for intr_in[58]
25	ENA_STATUS_57	W1TC	0h	Enabled Status for intr_in[57]
24	ENA_STATUS_56	W1TC	0h	Enabled Status for intr_in[56]
23	ENA_STATUS_55	W1TC	0h	Enabled Status for intr_in[55]
22	ENA_STATUS_54	W1TC	0h	Enabled Status for intr_in[54]
21	ENA_STATUS_53	W1TC	0h	Enabled Status for intr_in[53]
20	ENA_STATUS_52	W1TC	0h	Enabled Status for intr_in[52]
19	ENA_STATUS_51	W1TC	0h	Enabled Status for intr_in[51]
18	ENA_STATUS_50	W1TC	0h	Enabled Status for intr_in[50]
17	ENA_STATUS_49	W1TC	0h	Enabled Status for intr_in[49]
16	ENA_STATUS_48	W1TC	0h	Enabled Status for intr_in[48]
15	ENA_STATUS_47	W1TC	0h	Enabled Status for intr_in[47]

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Table 4-1130. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ENA_STATUS_46	W1TC	0h	Enabled Status for intr_in[46]
13	ENA_STATUS_45	W1TC	0h	Enabled Status for intr_in[45]
12	ENA_STATUS_44	W1TC	0h	Enabled Status for intr_in[44]
11	ENA_STATUS_43	W1TC	0h	Enabled Status for intr_in[43]
10	ENA_STATUS_42	W1TC	0h	Enabled Status for intr_in[42]
9	ENA_STATUS_41	W1TC	0h	Enabled Status for intr_in[41]
8	ENA_STATUS_40	W1TC	0h	Enabled Status for intr_in[40]
7	ENA_STATUS_39	W1TC	0h	Enabled Status for intr_in[39]
6	ENA_STATUS_38	W1TC	0h	Enabled Status for intr_in[38]
5	ENA_STATUS_37	W1TC	0h	Enabled Status for intr_in[37]
4	ENA_STATUS_36	W1TC	0h	Enabled Status for intr_in[36]
3	ENA_STATUS_35	W1TC	0h	Enabled Status for intr_in[35]
2	ENA_STATUS_34	W1TC	0h	Enabled Status for intr_in[34]
1	ENA_STATUS_33	W1TC	0h	Enabled Status for intr_in[33]
0	ENA_STATUS_32	W1TC	0h	Enabled Status for intr_in[32]

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4.2.2.57 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG0 Register

4.2.2.57.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG0 Register (Offset = 300h) [reset = 0h]

Enable Register 0

Return to Summary Table

Table 4-1131. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0300h

Figure 4-543. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG0 Name Register

31	30	29	28	27	26	25	24
ENABLE_31	ENABLE_30	ENABLE_29	ENABLE_28	ENABLE_27	ENABLE_26	ENABLE_25	ENABLE_24
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
ENABLE_23	ENABLE_22	ENABLE_21	ENABLE_20	ENABLE_19	ENABLE_18	ENABLE_17	ENABLE_16
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ENABLE_15	ENABLE_14	ENABLE_13	ENABLE_12	ENABLE_11	ENABLE_10	ENABLE_9	ENABLE_8
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ENABLE_7	ENABLE_6	ENABLE_5	ENABLE_4	ENABLE_3	ENABLE_2	ENABLE_1	ENABLE_0
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1132. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_31	W1TS	0h	Enable (set) for intr_in[31]
30	ENABLE_30	W1TS	0h	Enable (set) for intr_in[30]
29	ENABLE_29	W1TS	0h	Enable (set) for intr_in[29]
28	ENABLE_28	W1TS	0h	Enable (set) for intr_in[28]
27	ENABLE_27	W1TS	0h	Enable (set) for intr_in[27]
26	ENABLE_26	W1TS	0h	Enable (set) for intr_in[26]
25	ENABLE_25	W1TS	0h	Enable (set) for intr_in[25]
24	ENABLE_24	W1TS	0h	Enable (set) for intr_in[24]
23	ENABLE_23	W1TS	0h	Enable (set) for intr_in[23]
22	ENABLE_22	W1TS	0h	Enable (set) for intr_in[22]
21	ENABLE_21	W1TS	0h	Enable (set) for intr_in[21]
20	ENABLE_20	W1TS	0h	Enable (set) for intr_in[20]
19	ENABLE_19	W1TS	0h	Enable (set) for intr_in[19]
18	ENABLE_18	W1TS	0h	Enable (set) for intr_in[18]
17	ENABLE_17	W1TS	0h	Enable (set) for intr_in[17]
16	ENABLE_16	W1TS	0h	Enable (set) for intr_in[16]
15	ENABLE_15	W1TS	0h	Enable (set) for intr_in[15]
14	ENABLE_14	W1TS	0h	Enable (set) for intr_in[14]
13	ENABLE_13	W1TS	0h	Enable (set) for intr_in[13]
12	ENABLE_12	W1TS	0h	Enable (set) for intr_in[12]

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Table 4-1132. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ENABLE_11	W1TS	0h	Enable (set) for intr_in[11]
10	ENABLE_10	W1TS	0h	Enable (set) for intr_in[10]
9	ENABLE_9	W1TS	0h	Enable (set) for intr_in[9]
8	ENABLE_8	W1TS	0h	Enable (set) for intr_in[8]
7	ENABLE_7	W1TS	0h	Enable (set) for intr_in[7]
6	ENABLE_6	W1TS	0h	Enable (set) for intr_in[6]
5	ENABLE_5	W1TS	0h	Enable (set) for intr_in[5]
4	ENABLE_4	W1TS	0h	Enable (set) for intr_in[4]
3	ENABLE_3	W1TS	0h	Enable (set) for intr_in[3]
2	ENABLE_2	W1TS	0h	Enable (set) for intr_in[2]
1	ENABLE_1	W1TS	0h	Enable (set) for intr_in[1]
0	ENABLE_0	W1TS	0h	Enable (set) for intr_in[0]

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4.2.2.58 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG1 Register

4.2.2.58.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG1 Register (Offset = 304h) [reset = 0h]

Enable Register 1

Return to Summary Table

Table 4-1133. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0304h

Figure 4-544. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG1 Name Register

31	30	29	28	27	26	25	24
ENABLE_63	ENABLE_62	ENABLE_61	ENABLE_60	ENABLE_59	ENABLE_58	ENABLE_57	ENABLE_56
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
ENABLE_55	ENABLE_54	ENABLE_53	ENABLE_52	ENABLE_51	ENABLE_50	ENABLE_49	ENABLE_48
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ENABLE_47	ENABLE_46	ENABLE_45	ENABLE_44	ENABLE_43	ENABLE_42	ENABLE_41	ENABLE_40
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ENABLE_39	ENABLE_38	ENABLE_37	ENABLE_36	ENABLE_35	ENABLE_34	ENABLE_33	ENABLE_32
W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS	W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1134. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_63	W1TS	0h	Enable (set) for intr_in[63]
30	ENABLE_62	W1TS	0h	Enable (set) for intr_in[62]
29	ENABLE_61	W1TS	0h	Enable (set) for intr_in[61]
28	ENABLE_60	W1TS	0h	Enable (set) for intr_in[60]
27	ENABLE_59	W1TS	0h	Enable (set) for intr_in[59]
26	ENABLE_58	W1TS	0h	Enable (set) for intr_in[58]
25	ENABLE_57	W1TS	0h	Enable (set) for intr_in[57]
24	ENABLE_56	W1TS	0h	Enable (set) for intr_in[56]
23	ENABLE_55	W1TS	0h	Enable (set) for intr_in[55]
22	ENABLE_54	W1TS	0h	Enable (set) for intr_in[54]
21	ENABLE_53	W1TS	0h	Enable (set) for intr_in[53]
20	ENABLE_52	W1TS	0h	Enable (set) for intr_in[52]
19	ENABLE_51	W1TS	0h	Enable (set) for intr_in[51]
18	ENABLE_50	W1TS	0h	Enable (set) for intr_in[50]
17	ENABLE_49	W1TS	0h	Enable (set) for intr_in[49]
16	ENABLE_48	W1TS	0h	Enable (set) for intr_in[48]
15	ENABLE_47	W1TS	0h	Enable (set) for intr_in[47]
14	ENABLE_46	W1TS	0h	Enable (set) for intr_in[46]
13	ENABLE_45	W1TS	0h	Enable (set) for intr_in[45]
12	ENABLE_44	W1TS	0h	Enable (set) for intr_in[44]

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Table 4-1134. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ENABLE_43	W1TS	0h	Enable (set) for intr_in[43]
10	ENABLE_42	W1TS	0h	Enable (set) for intr_in[42]
9	ENABLE_41	W1TS	0h	Enable (set) for intr_in[41]
8	ENABLE_40	W1TS	0h	Enable (set) for intr_in[40]
7	ENABLE_39	W1TS	0h	Enable (set) for intr_in[39]
6	ENABLE_38	W1TS	0h	Enable (set) for intr_in[38]
5	ENABLE_37	W1TS	0h	Enable (set) for intr_in[37]
4	ENABLE_36	W1TS	0h	Enable (set) for intr_in[36]
3	ENABLE_35	W1TS	0h	Enable (set) for intr_in[35]
2	ENABLE_34	W1TS	0h	Enable (set) for intr_in[34]
1	ENABLE_33	W1TS	0h	Enable (set) for intr_in[33]
0	ENABLE_32	W1TS	0h	Enable (set) for intr_in[32]

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4.2.2.59 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG0 Register

4.2.2.59.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG0 Register (Offset = 380h) [reset = 0h]

Enable Clear Register 0

Return to Summary Table

Table 4-1135. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0380h

Figure 4-545. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
ENABLE_31_CLR	ENABLE_30_CLR	ENABLE_29_CLR	ENABLE_28_CLR	ENABLE_27_CLR	ENABLE_26_CLR	ENABLE_25_CLR	ENABLE_24_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
ENABLE_23_CLR	ENABLE_22_CLR	ENABLE_21_CLR	ENABLE_20_CLR	ENABLE_19_CLR	ENABLE_18_CLR	ENABLE_17_CLR	ENABLE_16_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ENABLE_15_CLR	ENABLE_14_CLR	ENABLE_13_CLR	ENABLE_12_CLR	ENABLE_11_CLR	ENABLE_10_CLR	ENABLE_9_CLR	ENABLE_8_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ENABLE_7_CLR	ENABLE_6_CLR	ENABLE_5_CLR	ENABLE_4_CLR	ENABLE_3_CLR	ENABLE_2_CLR	ENABLE_1_CLR	ENABLE_0_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1136. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_31_CLR	W1TC	0h	Enable clear for intr_in[31]
30	ENABLE_30_CLR	W1TC	0h	Enable clear for intr_in[30]
29	ENABLE_29_CLR	W1TC	0h	Enable clear for intr_in[29]
28	ENABLE_28_CLR	W1TC	0h	Enable clear for intr_in[28]
27	ENABLE_27_CLR	W1TC	0h	Enable clear for intr_in[27]
26	ENABLE_26_CLR	W1TC	0h	Enable clear for intr_in[26]
25	ENABLE_25_CLR	W1TC	0h	Enable clear for intr_in[25]
24	ENABLE_24_CLR	W1TC	0h	Enable clear for intr_in[24]
23	ENABLE_23_CLR	W1TC	0h	Enable clear for intr_in[23]
22	ENABLE_22_CLR	W1TC	0h	Enable clear for intr_in[22]
21	ENABLE_21_CLR	W1TC	0h	Enable clear for intr_in[21]
20	ENABLE_20_CLR	W1TC	0h	Enable clear for intr_in[20]
19	ENABLE_19_CLR	W1TC	0h	Enable clear for intr_in[19]
18	ENABLE_18_CLR	W1TC	0h	Enable clear for intr_in[18]
17	ENABLE_17_CLR	W1TC	0h	Enable clear for intr_in[17]
16	ENABLE_16_CLR	W1TC	0h	Enable clear for intr_in[16]
15	ENABLE_15_CLR	W1TC	0h	Enable clear for intr_in[15]

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Table 4-1136. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ENABLE_14_CLR	W1TC	0h	Enable clear for intr_in[14]
13	ENABLE_13_CLR	W1TC	0h	Enable clear for intr_in[13]
12	ENABLE_12_CLR	W1TC	0h	Enable clear for intr_in[12]
11	ENABLE_11_CLR	W1TC	0h	Enable clear for intr_in[11]
10	ENABLE_10_CLR	W1TC	0h	Enable clear for intr_in[10]
9	ENABLE_9_CLR	W1TC	0h	Enable clear for intr_in[9]
8	ENABLE_8_CLR	W1TC	0h	Enable clear for intr_in[8]
7	ENABLE_7_CLR	W1TC	0h	Enable clear for intr_in[7]
6	ENABLE_6_CLR	W1TC	0h	Enable clear for intr_in[6]
5	ENABLE_5_CLR	W1TC	0h	Enable clear for intr_in[5]
4	ENABLE_4_CLR	W1TC	0h	Enable clear for intr_in[4]
3	ENABLE_3_CLR	W1TC	0h	Enable clear for intr_in[3]
2	ENABLE_2_CLR	W1TC	0h	Enable clear for intr_in[2]
1	ENABLE_1_CLR	W1TC	0h	Enable clear for intr_in[1]
0	ENABLE_0_CLR	W1TC	0h	Enable clear for intr_in[0]

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4.2.2.60 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG1 Register

4.2.2.60.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG1 Register (Offset = 384h) [reset = 0h]

Enable Clear Register 1

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Table 4-1137. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0384h

Figure 4-546. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG1 Name Register

31	30	29	28	27	26	25	24
ENABLE_63_CLR	ENABLE_62_CLR	ENABLE_61_CLR	ENABLE_60_CLR	ENABLE_59_CLR	ENABLE_58_CLR	ENABLE_57_CLR	ENABLE_56_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
ENABLE_55_CLR	ENABLE_54_CLR	ENABLE_53_CLR	ENABLE_52_CLR	ENABLE_51_CLR	ENABLE_50_CLR	ENABLE_49_CLR	ENABLE_48_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ENABLE_47_CLR	ENABLE_46_CLR	ENABLE_45_CLR	ENABLE_44_CLR	ENABLE_43_CLR	ENABLE_42_CLR	ENABLE_41_CLR	ENABLE_40_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
ENABLE_39_CLR	ENABLE_38_CLR	ENABLE_37_CLR	ENABLE_36_CLR	ENABLE_35_CLR	ENABLE_34_CLR	ENABLE_33_CLR	ENABLE_32_CLR
W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC	W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1138. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_63_CLR	W1TC	0h	Enable clear for intr_in[63]
30	ENABLE_62_CLR	W1TC	0h	Enable clear for intr_in[62]
29	ENABLE_61_CLR	W1TC	0h	Enable clear for intr_in[61]
28	ENABLE_60_CLR	W1TC	0h	Enable clear for intr_in[60]
27	ENABLE_59_CLR	W1TC	0h	Enable clear for intr_in[59]
26	ENABLE_58_CLR	W1TC	0h	Enable clear for intr_in[58]
25	ENABLE_57_CLR	W1TC	0h	Enable clear for intr_in[57]
24	ENABLE_56_CLR	W1TC	0h	Enable clear for intr_in[56]
23	ENABLE_55_CLR	W1TC	0h	Enable clear for intr_in[55]
22	ENABLE_54_CLR	W1TC	0h	Enable clear for intr_in[54]
21	ENABLE_53_CLR	W1TC	0h	Enable clear for intr_in[53]
20	ENABLE_52_CLR	W1TC	0h	Enable clear for intr_in[52]
19	ENABLE_51_CLR	W1TC	0h	Enable clear for intr_in[51]
18	ENABLE_50_CLR	W1TC	0h	Enable clear for intr_in[50]
17	ENABLE_49_CLR	W1TC	0h	Enable clear for intr_in[49]
16	ENABLE_48_CLR	W1TC	0h	Enable clear for intr_in[48]
15	ENABLE_47_CLR	W1TC	0h	Enable clear for intr_in[47]

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Table 4-1138. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ENABLE_46_CLR	W1TC	0h	Enable clear for intr_in[46]
13	ENABLE_45_CLR	W1TC	0h	Enable clear for intr_in[45]
12	ENABLE_44_CLR	W1TC	0h	Enable clear for intr_in[44]
11	ENABLE_43_CLR	W1TC	0h	Enable clear for intr_in[43]
10	ENABLE_42_CLR	W1TC	0h	Enable clear for intr_in[42]
9	ENABLE_41_CLR	W1TC	0h	Enable clear for intr_in[41]
8	ENABLE_40_CLR	W1TC	0h	Enable clear for intr_in[40]
7	ENABLE_39_CLR	W1TC	0h	Enable clear for intr_in[39]
6	ENABLE_38_CLR	W1TC	0h	Enable clear for intr_in[38]
5	ENABLE_37_CLR	W1TC	0h	Enable clear for intr_in[37]
4	ENABLE_36_CLR	W1TC	0h	Enable clear for intr_in[36]
3	ENABLE_35_CLR	W1TC	0h	Enable clear for intr_in[35]
2	ENABLE_34_CLR	W1TC	0h	Enable clear for intr_in[34]
1	ENABLE_33_CLR	W1TC	0h	Enable clear for intr_in[33]
0	ENABLE_32_CLR	W1TC	0h	Enable clear for intr_in[32]

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4.2.2.61 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG0 Register

4.2.2.61.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG0 Register (Offset = 400h) [reset = 0h]

Interrupt Channel Map Register for 0 to 0+3

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Table 4-1139. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0400h

Figure 4-547. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_3			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_0			
NONE				W			
0h				0h			

Table 4-1140. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_3	R/W	0h	Interrupt Channel Map for intr_in[3]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_2	R/W	0h	Interrupt Channel Map for intr_in[2]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_1	R/W	0h	Interrupt Channel Map for intr_in[1]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_0	W	0h	Interrupt Channel Map for intr_in[0]

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4.2.2.62 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG1 Register

4.2.2.62.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG1 Register (Offset = 404h) [reset = 0h]

Interrupt Channel Map Register for 4 to 4+3

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Table 4-1141. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0404h

Figure 4-548. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_7			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_6			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_5			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_4			
NONE				R/W			
0h				0h			

Table 4-1142. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_7	R/W	0h	Interrupt Channel Map for intr_in[7]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_6	R/W	0h	Interrupt Channel Map for intr_in[6]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_5	R/W	0h	Interrupt Channel Map for intr_in[5]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_4	R/W	0h	Interrupt Channel Map for intr_in[4]

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4.2.2.63 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG2 Register

4.2.2.63.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG2 Register (Offset = 408h) [reset = 0h]

Interrupt Channel Map Register for 8 to 8+3

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Table 4-1143. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0408h

Figure 4-549. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_11			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_10			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_9			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_8			
NONE				R/W			
0h				0h			

Table 4-1144. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_11	R/W	0h	Interrupt Channel Map for intr_in[11]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_10	R/W	0h	Interrupt Channel Map for intr_in[10]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_9	R/W	0h	Interrupt Channel Map for intr_in[9]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_8	R/W	0h	Interrupt Channel Map for intr_in[8]

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4.2.2.64 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG3 Register

4.2.2.64.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG3 Register (Offset = 40Ch) [reset = 0h]

Interrupt Channel Map Register for 12 to 12+3

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Table 4-1145. Instance Table

Instance Name	Physical Address
ICSSM0	4802 040Ch

Figure 4-550. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_15			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_14			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_13			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_12			
NONE				R/W			
0h				0h			

Table 4-1146. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_15	R/W	0h	Interrupt Channel Map for intr_in[15]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_14	R/W	0h	Interrupt Channel Map for intr_in[14]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_13	R/W	0h	Interrupt Channel Map for intr_in[13]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_12	R/W	0h	Interrupt Channel Map for intr_in[12]

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4.2.2.65 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG4 Register

4.2.2.65.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG4 Register (Offset = 410h) [reset = 0h]

Interrupt Channel Map Register for 16 to 16+3

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Table 4-1147. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0410h

Figure 4-551. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_19			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_18			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_17			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_16			
NONE				R/W			
0h				0h			

Table 4-1148. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_19	R/W	0h	Interrupt Channel Map for intr_in[19]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_18	R/W	0h	Interrupt Channel Map for intr_in[18]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_17	R/W	0h	Interrupt Channel Map for intr_in[17]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_16	R/W	0h	Interrupt Channel Map for intr_in[16]

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4.2.2.66 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG5 Register

4.2.2.66.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG5 Register (Offset = 414h) [reset = 0h]

Interrupt Channel Map Register for 20 to 20+3

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Table 4-1149. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0414h

Figure 4-552. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_23			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_22			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_21			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_20			
NONE				R/W			
0h				0h			

Table 4-1150. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_23	R/W	0h	Interrupt Channel Map for intr_in[23]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_22	R/W	0h	Interrupt Channel Map for intr_in[22]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_21	R/W	0h	Interrupt Channel Map for intr_in[21]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_20	R/W	0h	Interrupt Channel Map for intr_in[20]

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4.2.2.67 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG6 Register

4.2.2.67.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG6 Register (Offset = 418h) [reset = 0h]

Interrupt Channel Map Register for 24 to 24+3

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Table 4-1151. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0418h

Figure 4-553. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_27			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_26			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_25			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_24			
NONE				R/W			
0h				0h			

Table 4-1152. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_27	R/W	0h	Interrupt Channel Map for intr_in[27]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_26	R/W	0h	Interrupt Channel Map for intr_in[26]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_25	R/W	0h	Interrupt Channel Map for intr_in[25]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_24	R/W	0h	Interrupt Channel Map for intr_in[24]

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4.2.2.68 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG7 Register

4.2.2.68.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG7 Register (Offset = 41Ch) [reset = 0h]

Interrupt Channel Map Register for 28 to 28+3

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Table 4-1153. Instance Table

Instance Name	Physical Address
ICSSM0	4802 041Ch

Figure 4-554. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_31			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_30			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_29			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_28			
NONE				R/W			
0h				0h			

Table 4-1154. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_31	R/W	0h	Interrupt Channel Map for intr_in[31]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_30	R/W	0h	Interrupt Channel Map for intr_in[30]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_29	R/W	0h	Interrupt Channel Map for intr_in[29]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_28	R/W	0h	Interrupt Channel Map for intr_in[28]

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4.2.2.69 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG8 Register

4.2.2.69.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG8 Register (Offset = 420h) [reset = 0h]

Interrupt Channel Map Register for 32 to 32+3

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Table 4-1155. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0420h

Figure 4-555. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_35			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_34			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_33			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_32			
NONE				R/W			
0h				0h			

Table 4-1156. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_35	R/W	0h	Interrupt Channel Map for intr_in[35]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_34	R/W	0h	Interrupt Channel Map for intr_in[34]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_33	R/W	0h	Interrupt Channel Map for intr_in[33]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_32	R/W	0h	Interrupt Channel Map for intr_in[32]

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4.2.2.70 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG9 Register

4.2.2.70.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG9 Register (Offset = 424h) [reset = 0h]

Interrupt Channel Map Register for 36 to 36+3

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Table 4-1157. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0424h

Figure 4-556. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG9 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_39			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_38			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_37			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_36			
NONE				R/W			
0h				0h			

Table 4-1158. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_39	R/W	0h	Interrupt Channel Map for intr_in[39]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_38	R/W	0h	Interrupt Channel Map for intr_in[38]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_37	R/W	0h	Interrupt Channel Map for intr_in[37]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_36	R/W	0h	Interrupt Channel Map for intr_in[36]

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4.2.2.71 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG10 Register

4.2.2.71.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG10 Register (Offset = 428h) [reset = 0h]

Interrupt Channel Map Register for 40 to 40+3

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Table 4-1159. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0428h

Figure 4-557. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG10 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_43			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_42			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_41			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_40			
NONE				R/W			
0h				0h			

Table 4-1160. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_43	R/W	0h	Interrupt Channel Map for intr_in[43]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_42	R/W	0h	Interrupt Channel Map for intr_in[42]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_41	R/W	0h	Interrupt Channel Map for intr_in[41]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_40	R/W	0h	Interrupt Channel Map for intr_in[40]

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4.2.2.72 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG11 Register

4.2.2.72.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG11 Register (Offset = 42Ch) [reset = 0h]

Interrupt Channel Map Register for 44 to 44+3

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Table 4-1161. Instance Table

Instance Name	Physical Address
ICSSM0	4802 042Ch

Figure 4-558. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG11 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_47			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_46			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_45			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_44			
NONE				R/W			
0h				0h			

Table 4-1162. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_47	R/W	0h	Interrupt Channel Map for intr_in[47]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_46	R/W	0h	Interrupt Channel Map for intr_in[46]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_45	R/W	0h	Interrupt Channel Map for intr_in[45]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_44	R/W	0h	Interrupt Channel Map for intr_in[44]

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4.2.2.73 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG12 Register

4.2.2.73.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG12 Register (Offset = 430h) [reset = 0h]

Interrupt Channel Map Register for 48 to 48+3

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Table 4-1163. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0430h

Figure 4-559. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG12 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_51			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_50			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_49			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_48			
NONE				R/W			
0h				0h			

Table 4-1164. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_51	R/W	0h	Interrupt Channel Map for intr_in[51]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_50	R/W	0h	Interrupt Channel Map for intr_in[50]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_49	R/W	0h	Interrupt Channel Map for intr_in[49]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_48	R/W	0h	Interrupt Channel Map for intr_in[48]

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4.2.2.74 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG13 Register

4.2.2.74.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG13 Register (Offset = 434h) [reset = 0h]

Interrupt Channel Map Register for 52 to 52+3

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Table 4-1165. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0434h

Figure 4-560. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG13 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_55			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_54			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_53			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_52			
NONE				R/W			
0h				0h			

Table 4-1166. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_55	R/W	0h	Interrupt Channel Map for intr_in[55]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_54	R/W	0h	Interrupt Channel Map for intr_in[54]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_53	R/W	0h	Interrupt Channel Map for intr_in[53]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_52	R/W	0h	Interrupt Channel Map for intr_in[52]

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4.2.2.75 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG14 Register

4.2.2.75.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG14 Register (Offset = 438h) [reset = 0h]

Interrupt Channel Map Register for 56 to 56+3

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Table 4-1167. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0438h

Figure 4-561. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG14 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_59			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_58			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_57			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_56			
NONE				R/W			
0h				0h			

Table 4-1168. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_59	R/W	0h	Interrupt Channel Map for intr_in[59]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_58	R/W	0h	Interrupt Channel Map for intr_in[58]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_57	R/W	0h	Interrupt Channel Map for intr_in[57]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_56	R/W	0h	Interrupt Channel Map for intr_in[56]

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4.2.2.76 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG15 Register

4.2.2.76.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG15 Register (Offset = 43Ch) [reset = 0h]

Interrupt Channel Map Register for 60 to 60+3

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Table 4-1169. Instance Table

Instance Name	Physical Address
ICSSM0	4802 043Ch

Figure 4-562. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG15 Name Register

31	30	29	28	27	26	25	24
RESERVED				CH_MAP_63			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				CH_MAP_62			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				CH_MAP_61			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CH_MAP_60			
NONE				R/W			
0h				0h			

Table 4-1170. ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	CH_MAP_63	R/W	0h	Interrupt Channel Map for intr_in[63]
23:20	RESERVED	NONE	0h	Reserved
19:16	CH_MAP_62	R/W	0h	Interrupt Channel Map for intr_in[62]
15:12	RESERVED	NONE	0h	Reserved
11:8	CH_MAP_61	R/W	0h	Interrupt Channel Map for intr_in[61]
7:4	RESERVED	NONE	0h	Reserved
3:0	CH_MAP_60	R/W	0h	Interrupt Channel Map for intr_in[60]

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4.2.2.77 ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG0 Register

4.2.2.77.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG0 Register (Offset = 800h) [reset = 0h]

Host Interrupt Map Register for 0 to 0+3

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Table 4-1171. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0800h

Figure 4-563. ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED				HINT_MAP_3			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_2			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				HINT_MAP_1			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_0			
NONE				R/W			
0h				0h			

Table 4-1172. ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	HINT_MAP_3	R/W	0h	Host Interrupt Map for Channel 3
23:20	RESERVED	NONE	0h	Reserved
19:16	HINT_MAP_2	R/W	0h	Host Interrupt Map for Channel 2
15:12	RESERVED	NONE	0h	Reserved
11:8	HINT_MAP_1	R/W	0h	Host Interrupt Map for Channel 1
7:4	RESERVED	NONE	0h	Reserved
3:0	HINT_MAP_0	R/W	0h	Host Interrupt Map for Channel 0

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4.2.2.78 ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG1 Register

4.2.2.78.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG1 Register (Offset = 804h) [reset = 0h]

Host Interrupt Map Register for 4 to 4+3

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Table 4-1173. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0804h

Figure 4-564. ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED				HINT_MAP_7			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_6			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED				HINT_MAP_5			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_4			
NONE				R/W			
0h				0h			

Table 4-1174. ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:24	HINT_MAP_7	R/W	0h	Host Interrupt Map for Channel 7
23:20	RESERVED	NONE	0h	Reserved
19:16	HINT_MAP_6	R/W	0h	Host Interrupt Map for Channel 6
15:12	RESERVED	NONE	0h	Reserved
11:8	HINT_MAP_5	R/W	0h	Host Interrupt Map for Channel 5
7:4	RESERVED	NONE	0h	Reserved
3:0	HINT_MAP_4	R/W	0h	Host Interrupt Map for Channel 4

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4.2.2.79 ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG2 Register

4.2.2.79.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG2 Register (Offset = 808h) [reset = 0h]

Host Interrupt Map Register for 8 to 8+3

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Table 4-1175. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0808h

Figure 4-565. ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				HINT_MAP_9			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_8			
NONE				R/W			
0h				0h			

Table 4-1176. ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	HINT_MAP_9	R/W	0h	Host Interrupt Map for Channel 9
7:4	RESERVED	NONE	0h	Reserved
3:0	HINT_MAP_8	R/W	0h	Host Interrupt Map for Channel 8

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4.2.2.80 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG0 Register

4.2.2.80.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG0 Register (Offset = 900h) [reset = 80000000h]

Host Int 0 Prioritized Interrupt Register

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Table 4-1177. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0900h

Figure 4-566. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG0 Name Register

31	30	29	28	27	26	25	24
NONE_HINT_0	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_0	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_0							
R							
0h							

Table 4-1178. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_0	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	PRI_HINT_0	R	0h	Host Int 0 Prioritized Interrupt

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4.2.2.81 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG1 Register

4.2.2.81.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG1 Register (Offset = 904h) [reset = 80000000h]

Host Int 1 Prioritized Interrupt Register

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Table 4-1179. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0904h

Figure 4-567. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG1 Name Register

31	30	29	28	27	26	25	24
NONE_HINT_1	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_1	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_1							
R							
0h							

Table 4-1180. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_1	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	PRI_HINT_1	R	0h	Host Int 1 Prioritized Interrupt

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4.2.2.82 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG2 Register

4.2.2.82.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG2 Register (Offset = 908h) [reset = 80000000h]

Host Int 2 Prioritized Interrupt Register

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Table 4-1181. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0908h

Figure 4-568. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG2 Name Register

31	30	29	28	27	26	25	24
NONE_HINT_2	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_2	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_2							
R							
0h							

Table 4-1182. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_2	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	PRI_HINT_2	R	0h	Host Int 2 Prioritized Interrupt

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4.2.2.83 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG3 Register

4.2.2.83.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG3 Register (Offset = 90Ch) [reset = 80000000h]

Host Int 3 Prioritized Interrupt Register

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Table 4-1183. Instance Table

Instance Name	Physical Address
ICSSM0	4802 090Ch

Figure 4-569. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG3 Name Register

31	30	29	28	27	26	25	24
NONE_HINT_3	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_3	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
PRI_HINT_3							
R							
0h							

Table 4-1184. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_3	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	PRI_HINT_3	R	0h	Host Int 3 Prioritized Interrupt

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4.2.2.84 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG4 Register

4.2.2.84.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG4 Register (Offset = 910h) [reset = 80000000h]

Host Int 4 Prioritized Interrupt Register

Return to Summary Table

Table 4-1185. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0910h

Figure 4-570. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG4 Name Register

31	30	29	28	27	26	25	24
NONE_HINT_4	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_4	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_4							
R							
0h							

Table 4-1186. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_4	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	PRI_HINT_4	R	0h	Host Int 4 Prioritized Interrupt

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4.2.2.85 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG5 Register

4.2.2.85.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG5 Register (Offset = 914h) [reset = 80000000h]

Host Int 5 Prioritized Interrupt Register

Return to Summary Table

Table 4-1187. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0914h

Figure 4-571. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG5 Name Register

31	30	29	28	27	26	25	24
NONE_HINT_5	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_5	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_5							
R							
0h							

Table 4-1188. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_5	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	PRI_HINT_5	R	0h	Host Int 5 Prioritized Interrupt

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4.2.2.86 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG6 Register

4.2.2.86.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG6 Register (Offset = 918h) [reset = 80000000h]

Host Int 6 Prioritized Interrupt Register

Return to Summary Table

Table 4-1189. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0918h

Figure 4-572. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG6 Name Register

31	30	29	28	27	26	25	24
NONE_HINT_6	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_6	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_6							
R							
0h							

Table 4-1190. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_6	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	PRI_HINT_6	R	0h	Host Int 6 Prioritized Interrupt

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4.2.2.87 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG7 Register

4.2.2.87.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG7 Register (Offset = 91Ch) [reset = 80000000h]

Host Int 7 Prioritized Interrupt Register

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Table 4-1191. Instance Table

Instance Name	Physical Address
ICSSM0	4802 091Ch

Figure 4-573. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG7 Name Register

31	30	29	28	27	26	25	24
NONE_HINT_7	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_7	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_7							
R							
0h							

Table 4-1192. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_7	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	PRI_HINT_7	R	0h	Host Int 7 Prioritized Interrupt

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4.2.2.88 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG8 Register

4.2.2.88.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG8 Register (Offset = 920h) [reset = 80000000h]

Host Int 8 Prioritized Interrupt Register

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Table 4-1193. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0920h

Figure 4-574. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG8 Name Register

31	30	29	28	27	26	25	24
NONE_HINT_8	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT_8	
NONE						R	
0h						0h	
7	6	5	4	3	2	1	0
PRI_HINT_8							
R							
0h							

Table 4-1194. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_8	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	PRI_HINT_8	R	0h	Host Int 8 Prioritized Interrupt

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4.2.2.89 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG9 Register

4.2.2.89.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG9 Register (Offset = 924h) [reset = 80000000h]

Host Int 9 Prioritized Interrupt Register

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Table 4-1195. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0924h

Figure 4-575. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG9 Name Register

31	30	29	28	27	26	25	24
NONE_HINT_9	RESERVED						
R	NONE						
1h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PRI_HINT_9	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_HINT_9							
R							
0h							

Table 4-1196. ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT_9	R	1h	No interrupt pending flag
30:10	RESERVED	NONE	0h	Reserved
9:0	PRI_HINT_9	R	0h	Host Int 9 Prioritized Interrupt

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4.2.2.90 ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG0 Register

4.2.2.90.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG0 Register (Offset = D00h) [reset = FFFFFFFFh]

Polarity Register 0

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Table 4-1197. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0D00h

Figure 4-576. ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG0 Name Register

31	30	29	28	27	26	25	24
POLARITY_31	POLARITY_30	POLARITY_29	POLARITY_28	POLARITY_27	POLARITY_26	POLARITY_25	POLARITY_24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h
23	22	21	20	19	18	17	16
POLARITY_23	POLARITY_22	POLARITY_21	POLARITY_20	POLARITY_19	POLARITY_18	POLARITY_17	POLARITY_16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h
15	14	13	12	11	10	9	8
POLARITY_15	POLARITY_14	POLARITY_13	POLARITY_12	POLARITY_11	POLARITY_10	POLARITY_9	POLARITY_8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
POLARITY_7	POLARITY_6	POLARITY_5	POLARITY_4	POLARITY_3	POLARITY_2	POLARITY_1	POLARITY_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h

Table 4-1198. ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_31	R/W	1h	Polarity for intr_in[31] 0=low
30	POLARITY_30	R/W	1h	Polarity for intr_in[30] 0=low
29	POLARITY_29	R/W	1h	Polarity for intr_in[29] 0=low
28	POLARITY_28	R/W	1h	Polarity for intr_in[28] 0=low
27	POLARITY_27	R/W	1h	Polarity for intr_in[27] 0=low
26	POLARITY_26	R/W	1h	Polarity for intr_in[26] 0=low
25	POLARITY_25	R/W	1h	Polarity for intr_in[25] 0=low
24	POLARITY_24	R/W	1h	Polarity for intr_in[24] 0=low
23	POLARITY_23	R/W	1h	Polarity for intr_in[23] 0=low
22	POLARITY_22	R/W	1h	Polarity for intr_in[22] 0=low
21	POLARITY_21	R/W	1h	Polarity for intr_in[21] 0=low
20	POLARITY_20	R/W	1h	Polarity for intr_in[20] 0=low
19	POLARITY_19	R/W	1h	Polarity for intr_in[19] 0=low
18	POLARITY_18	R/W	1h	Polarity for intr_in[18] 0=low
17	POLARITY_17	R/W	1h	Polarity for intr_in[17] 0=low
16	POLARITY_16	R/W	1h	Polarity for intr_in[16] 0=low
15	POLARITY_15	R/W	1h	Polarity for intr_in[15] 0=low
14	POLARITY_14	R/W	1h	Polarity for intr_in[14] 0=low
13	POLARITY_13	R/W	1h	Polarity for intr_in[13] 0=low

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Table 4-1198. ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	POLARITY_12	R/W	1h	Polarity for intr_in[12] 0=low
11	POLARITY_11	R/W	1h	Polarity for intr_in[11] 0=low
10	POLARITY_10	R/W	1h	Polarity for intr_in[10] 0=low
9	POLARITY_9	R/W	1h	Polarity for intr_in[9] 0=low
8	POLARITY_8	R/W	1h	Polarity for intr_in[8] 0=low
7	POLARITY_7	R/W	1h	Polarity for intr_in[7] 0=low
6	POLARITY_6	R/W	1h	Polarity for intr_in[6] 0=low
5	POLARITY_5	R/W	1h	Polarity for intr_in[5] 0=low
4	POLARITY_4	R/W	1h	Polarity for intr_in[4] 0=low
3	POLARITY_3	R/W	1h	Polarity for intr_in[3] 0=low
2	POLARITY_2	R/W	1h	Polarity for intr_in[2] 0=low
1	POLARITY_1	R/W	1h	Polarity for intr_in[1] 0=low
0	POLARITY_0	R/W	1h	Polarity for intr_in[0] 0=low

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4.2.2.91 ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG1 Register

4.2.2.91.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG1 Register (Offset = D04h) [reset = FFFFFFFFh]

Polarity Register 1

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Table 4-1199. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0D04h

Figure 4-577. ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG1 Name Register

31	30	29	28	27	26	25	24
POLARITY_63	POLARITY_62	POLARITY_61	POLARITY_60	POLARITY_59	POLARITY_58	POLARITY_57	POLARITY_56
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h
23	22	21	20	19	18	17	16
POLARITY_55	POLARITY_54	POLARITY_53	POLARITY_52	POLARITY_51	POLARITY_50	POLARITY_49	POLARITY_48
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h
15	14	13	12	11	10	9	8
POLARITY_47	POLARITY_46	POLARITY_45	POLARITY_44	POLARITY_43	POLARITY_42	POLARITY_41	POLARITY_40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h
7	6	5	4	3	2	1	0
POLARITY_39	POLARITY_38	POLARITY_37	POLARITY_36	POLARITY_35	POLARITY_34	POLARITY_33	POLARITY_32
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h

Table 4-1200. ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLARITY_63	R/W	1h	Polarity for intr_in[63] 0=low
30	POLARITY_62	R/W	1h	Polarity for intr_in[62] 0=low
29	POLARITY_61	R/W	1h	Polarity for intr_in[61] 0=low
28	POLARITY_60	R/W	1h	Polarity for intr_in[60] 0=low
27	POLARITY_59	R/W	1h	Polarity for intr_in[59] 0=low
26	POLARITY_58	R/W	1h	Polarity for intr_in[58] 0=low
25	POLARITY_57	R/W	1h	Polarity for intr_in[57] 0=low
24	POLARITY_56	R/W	1h	Polarity for intr_in[56] 0=low
23	POLARITY_55	R/W	1h	Polarity for intr_in[55] 0=low
22	POLARITY_54	R/W	1h	Polarity for intr_in[54] 0=low
21	POLARITY_53	R/W	1h	Polarity for intr_in[53] 0=low
20	POLARITY_52	R/W	1h	Polarity for intr_in[52] 0=low
19	POLARITY_51	R/W	1h	Polarity for intr_in[51] 0=low
18	POLARITY_50	R/W	1h	Polarity for intr_in[50] 0=low
17	POLARITY_49	R/W	1h	Polarity for intr_in[49] 0=low
16	POLARITY_48	R/W	1h	Polarity for intr_in[48] 0=low
15	POLARITY_47	R/W	1h	Polarity for intr_in[47] 0=low
14	POLARITY_46	R/W	1h	Polarity for intr_in[46] 0=low
13	POLARITY_45	R/W	1h	Polarity for intr_in[45] 0=low

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Table 4-1200. ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	POLARITY_44	R/W	1h	Polarity for intr_in[44] 0=low
11	POLARITY_43	R/W	1h	Polarity for intr_in[43] 0=low
10	POLARITY_42	R/W	1h	Polarity for intr_in[42] 0=low
9	POLARITY_41	R/W	1h	Polarity for intr_in[41] 0=low
8	POLARITY_40	R/W	1h	Polarity for intr_in[40] 0=low
7	POLARITY_39	R/W	1h	Polarity for intr_in[39] 0=low
6	POLARITY_38	R/W	1h	Polarity for intr_in[38] 0=low
5	POLARITY_37	R/W	1h	Polarity for intr_in[37] 0=low
4	POLARITY_36	R/W	1h	Polarity for intr_in[36] 0=low
3	POLARITY_35	R/W	1h	Polarity for intr_in[35] 0=low
2	POLARITY_34	R/W	1h	Polarity for intr_in[34] 0=low
1	POLARITY_33	R/W	1h	Polarity for intr_in[33] 0=low
0	POLARITY_32	R/W	1h	Polarity for intr_in[32] 0=low

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4.2.2.92 ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG0 Register

4.2.2.92.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG0 Register (Offset = D80h) [reset = 0h]

Type Register 0

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Table 4-1201. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0D80h

Figure 4-578. ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG0 Name Register

31	30	29	28	27	26	25	24
TYPE_31	TYPE_30	TYPE_29	TYPE_28	TYPE_27	TYPE_26	TYPE_25	TYPE_24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
TYPE_23	TYPE_22	TYPE_21	TYPE_20	TYPE_19	TYPE_18	TYPE_17	TYPE_16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TYPE_15	TYPE_14	TYPE_13	TYPE_12	TYPE_11	TYPE_10	TYPE_9	TYPE_8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TYPE_7	TYPE_6	TYPE_5	TYPE_4	TYPE_3	TYPE_2	TYPE_1	TYPE_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1202. ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_31	R/W	0h	Type for intr_in[31] 0=level
30	TYPE_30	R/W	0h	Type for intr_in[30] 0=level
29	TYPE_29	R/W	0h	Type for intr_in[29] 0=level
28	TYPE_28	R/W	0h	Type for intr_in[28] 0=level
27	TYPE_27	R/W	0h	Type for intr_in[27] 0=level
26	TYPE_26	R/W	0h	Type for intr_in[26] 0=level
25	TYPE_25	R/W	0h	Type for intr_in[25] 0=level
24	TYPE_24	R/W	0h	Type for intr_in[24] 0=level
23	TYPE_23	R/W	0h	Type for intr_in[23] 0=level
22	TYPE_22	R/W	0h	Type for intr_in[22] 0=level
21	TYPE_21	R/W	0h	Type for intr_in[21] 0=level
20	TYPE_20	R/W	0h	Type for intr_in[20] 0=level
19	TYPE_19	R/W	0h	Type for intr_in[19] 0=level
18	TYPE_18	R/W	0h	Type for intr_in[18] 0=level
17	TYPE_17	R/W	0h	Type for intr_in[17] 0=level
16	TYPE_16	R/W	0h	Type for intr_in[16] 0=level
15	TYPE_15	R/W	0h	Type for intr_in[15] 0=level
14	TYPE_14	R/W	0h	Type for intr_in[14] 0=level
13	TYPE_13	R/W	0h	Type for intr_in[13] 0=level
12	TYPE_12	R/W	0h	Type for intr_in[12] 0=level

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Table 4-1202. ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TYPE_11	R/W	0h	Type for intr_in[11] 0=level
10	TYPE_10	R/W	0h	Type for intr_in[10] 0=level
9	TYPE_9	R/W	0h	Type for intr_in[9] 0=level
8	TYPE_8	R/W	0h	Type for intr_in[8] 0=level
7	TYPE_7	R/W	0h	Type for intr_in[7] 0=level
6	TYPE_6	R/W	0h	Type for intr_in[6] 0=level
5	TYPE_5	R/W	0h	Type for intr_in[5] 0=level
4	TYPE_4	R/W	0h	Type for intr_in[4] 0=level
3	TYPE_3	R/W	0h	Type for intr_in[3] 0=level
2	TYPE_2	R/W	0h	Type for intr_in[2] 0=level
1	TYPE_1	R/W	0h	Type for intr_in[1] 0=level
0	TYPE_0	R/W	0h	Type for intr_in[0] 0=level

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4.2.2.93 ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG1 Register

4.2.2.93.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG1 Register (Offset = D84h) [reset = 0h]

Type Register 1

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Table 4-1203. Instance Table

Instance Name	Physical Address
ICSSM0	4802 0D84h

Figure 4-579. ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG1 Name Register

31	30	29	28	27	26	25	24
TYPE_63	TYPE_62	TYPE_61	TYPE_60	TYPE_59	TYPE_58	TYPE_57	TYPE_56
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
TYPE_55	TYPE_54	TYPE_53	TYPE_52	TYPE_51	TYPE_50	TYPE_49	TYPE_48
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TYPE_47	TYPE_46	TYPE_45	TYPE_44	TYPE_43	TYPE_42	TYPE_41	TYPE_40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TYPE_39	TYPE_38	TYPE_37	TYPE_36	TYPE_35	TYPE_34	TYPE_33	TYPE_32
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1204. ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TYPE_63	R/W	0h	Type for intr_in[63] 0=level
30	TYPE_62	R/W	0h	Type for intr_in[62] 0=level
29	TYPE_61	R/W	0h	Type for intr_in[61] 0=level
28	TYPE_60	R/W	0h	Type for intr_in[60] 0=level
27	TYPE_59	R/W	0h	Type for intr_in[59] 0=level
26	TYPE_58	R/W	0h	Type for intr_in[58] 0=level
25	TYPE_57	R/W	0h	Type for intr_in[57] 0=level
24	TYPE_56	R/W	0h	Type for intr_in[56] 0=level
23	TYPE_55	R/W	0h	Type for intr_in[55] 0=level
22	TYPE_54	R/W	0h	Type for intr_in[54] 0=level
21	TYPE_53	R/W	0h	Type for intr_in[53] 0=level
20	TYPE_52	R/W	0h	Type for intr_in[52] 0=level
19	TYPE_51	R/W	0h	Type for intr_in[51] 0=level
18	TYPE_50	R/W	0h	Type for intr_in[50] 0=level
17	TYPE_49	R/W	0h	Type for intr_in[49] 0=level
16	TYPE_48	R/W	0h	Type for intr_in[48] 0=level
15	TYPE_47	R/W	0h	Type for intr_in[47] 0=level
14	TYPE_46	R/W	0h	Type for intr_in[46] 0=level
13	TYPE_45	R/W	0h	Type for intr_in[45] 0=level
12	TYPE_44	R/W	0h	Type for intr_in[44] 0=level

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Table 4-1204. ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TYPE_43	R/W	0h	Type for intr_in[43] 0=level
10	TYPE_42	R/W	0h	Type for intr_in[42] 0=level
9	TYPE_41	R/W	0h	Type for intr_in[41] 0=level
8	TYPE_40	R/W	0h	Type for intr_in[40] 0=level
7	TYPE_39	R/W	0h	Type for intr_in[39] 0=level
6	TYPE_38	R/W	0h	Type for intr_in[38] 0=level
5	TYPE_37	R/W	0h	Type for intr_in[37] 0=level
4	TYPE_36	R/W	0h	Type for intr_in[36] 0=level
3	TYPE_35	R/W	0h	Type for intr_in[35] 0=level
2	TYPE_34	R/W	0h	Type for intr_in[34] 0=level
1	TYPE_33	R/W	0h	Type for intr_in[33] 0=level
0	TYPE_32	R/W	0h	Type for intr_in[32] 0=level

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4.2.2.94 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG0 Register

4.2.2.94.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG0 Register (Offset = 1100h) [reset = 100h]

Host Int 0 Nesting Level Register

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Table 4-1205. Instance Table

Instance Name	Physical Address
ICSSM0	4802 1100h

Figure 4-580. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG0 Name Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_0
NONE							R/W
0h							100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_0							
R/W							
100h							

Table 4-1206. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	0h	Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	NEST_HINT_0	R/W	100h	Host Int 0 Nesting Level

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4.2.2.95 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG1 Register

4.2.2.95.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG1 Register (Offset = 1104h) [reset = 100h]

Host Int 1 Nesting Level Register

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Table 4-1207. Instance Table

Instance Name	Physical Address
ICSSM0	4802 1104h

Figure 4-581. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG1 Name Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT_1
NONE							R/W
0h							100h
7	6	5	4	3	2	1	0
NEST_HINT_1							
R/W							
100h							

Table 4-1208. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	0h	Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	NEST_HINT_1	R/W	100h	Host Int 1 Nesting Level

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4.2.2.96 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG2 Register

4.2.2.96.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG2 Register (Offset = 1108h) [reset = 100h]

Host Int 2 Nesting Level Register

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Table 4-1209. Instance Table

Instance Name	Physical Address
ICSSM0	4802 1108h

Figure 4-582. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG2 Name Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_2
NONE							R/W
0h							100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_2							
R/W							
100h							

Table 4-1210. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	0h	Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	NEST_HINT_2	R/W	100h	Host Int 2 Nesting Level

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4.2.2.97 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG3 Register

4.2.2.97.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG3 Register (Offset = 110Ch) [reset = 100h]

Host Int 3 Nesting Level Register

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Table 4-1211. Instance Table

Instance Name	Physical Address
ICSSM0	4802 110Ch

Figure 4-583. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG3 Name Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_3
NONE							R/W
0h							100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_3							
R/W							
100h							

Table 4-1212. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	0h	Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	NEST_HINT_3	R/W	100h	Host Int 3 Nesting Level

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4.2.2.98 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG4 Register

4.2.2.98.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG4 Register (Offset = 1110h) [reset = 100h]

Host Int 4 Nesting Level Register

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Table 4-1213. Instance Table

Instance Name	Physical Address
ICSSM0	4802 1110h

Figure 4-584. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG4 Name Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_4
NONE							R/W
0h							100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_4							
R/W							
100h							

Table 4-1214. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	0h	Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	NEST_HINT_4	R/W	100h	Host Int 4 Nesting Level

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4.2.2.99 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG5 Register

4.2.2.99.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG5 Register (Offset = 1114h) [reset = 100h]

Host Int 5 Nesting Level Register

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Table 4-1215. Instance Table

Instance Name	Physical Address
ICSSM0	4802 1114h

Figure 4-585. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG5 Name Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_5
NONE							R/W
0h							100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_5							
R/W							
100h							

Table 4-1216. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	0h	Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	NEST_HINT_5	R/W	100h	Host Int 5 Nesting Level

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4.2.2.100 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG6 Register

4.2.2.100.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG6 Register (Offset = 1118h) [reset = 100h]

Host Int 6 Nesting Level Register

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Table 4-1217. Instance Table

Instance Name	Physical Address
ICSSM0	4802 1118h

Figure 4-586. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG6 Name Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_6
NONE							R/W
0h							100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_6							
R/W							
100h							

Table 4-1218. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	0h	Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	NEST_HINT_6	R/W	100h	Host Int 6 Nesting Level

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4.2.2.101 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG7 Register

4.2.2.101.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG7 Register (Offset = 111Ch) [reset = 100h]

Host Int 7 Nesting Level Register

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Table 4-1219. Instance Table

Instance Name	Physical Address
ICSSM0	4802 111Ch

Figure 4-587. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG7 Name Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_7
NONE							R/W
0h							100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_7							
R/W							
100h							

Table 4-1220. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	0h	Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	NEST_HINT_7	R/W	100h	Host Int 7 Nesting Level

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4.2.2.102 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG8 Register

4.2.2.102.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG8 Register (Offset = 1120h) [reset = 100h]

Host Int 8 Nesting Level Register

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Table 4-1221. Instance Table

Instance Name	Physical Address
ICSSM0	4802 1120h

Figure 4-588. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG8 Name Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_8
NONE							R/W
0h							100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_8							
R/W							
100h							

Table 4-1222. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	0h	Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	NEST_HINT_8	R/W	100h	Host Int 8 Nesting Level

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4.2.2.103 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG9 Register

4.2.2.103.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG9 Register (Offset = 1124h) [reset = 100h]

Host Int 9 Nesting Level Register

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Table 4-1223. Instance Table

Instance Name	Physical Address
ICSSM0	4802 1124h

Figure 4-589. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG9 Name Register

31	30	29	28	27	26	25	24
NEST_AUTO_OVR	RESERVED						
W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							NEST_HINT_9
NONE							R/W
0h							100h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NEST_HINT_9							
R/W							
100h							

Table 4-1224. ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NEST_AUTO_OVR	W	0h	Nesting Level Override Automatic
30:9	RESERVED	NONE	0h	Reserved
8:0	NEST_HINT_9	R/W	100h	Host Int 9 Nesting Level

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4.2.2.104 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_HINT_REG0 Register

4.2.2.104.1 ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_HINT_REG0 Register (Offset = 1500h) [reset = 0h]

Host Int Enable Register 0

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Table 4-1225. Instance Table

Instance Name	Physical Address
ICSSM0	4802 1500h

Figure 4-590. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_HINT_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						ENABLE_HINT_9	ENABLE_HINT_8
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ENABLE_HINT_7	ENABLE_HINT_6	ENABLE_HINT_5	ENABLE_HINT_4	ENABLE_HINT_3	ENABLE_HINT_2	ENABLE_HINT_1	ENABLE_HINT_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1226. ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_HINT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	ENABLE_HINT_9	R/W	0h	Enable for Host Int 9
8	ENABLE_HINT_8	R/W	0h	Enable for Host Int 8
7	ENABLE_HINT_7	R/W	0h	Enable for Host Int 7
6	ENABLE_HINT_6	R/W	0h	Enable for Host Int 6
5	ENABLE_HINT_5	R/W	0h	Enable for Host Int 5
4	ENABLE_HINT_4	R/W	0h	Enable for Host Int 4
3	ENABLE_HINT_3	R/W	0h	Enable for Host Int 3
2	ENABLE_HINT_2	R/W	0h	Enable for Host Int 2
1	ENABLE_HINT_1	R/W	0h	Enable for Host Int 1
0	ENABLE_HINT_0	R/W	0h	Enable for Host Int 0

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4.2.2.105 ICSSM_PR1_PDSP0_IRAM_CONTROL Register

4.2.2.105.1 ICSSM_PR1_PDSP0_IRAM_CONTROL Register (Offset = 0h) [reset = 1h]

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Table 4-1227. Instance Table

Instance Name	Physical Address
ICSSM0	4802 2000h

Figure 4-591. ICSSM_PR1_PDSP0_IRAM_CONTROL Name Register

31	30	29	28	27	26	25	24
PCOUNTER_RST_VAL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PCOUNTER_RST_VAL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PDSP_STATE	BIG_ENDIAN	RESERVED					SINGLE_STEP
R	R	NONE					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			RESTART	COUNTER_ENABLE	PDSP_SLEEPING	PDSP_ENABLE	SOFT_RST_N
NONE			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	1h

Table 4-1228. ICSSM_PR1_PDSP0_IRAM_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PCOUNTER_RST_VAL	R/W	0h	Program counter reset value
15	PDSP_STATE	R	0h	PDSP run state: 0=PDSP is halted, 1=PDSP is running
14	BIG_ENDIAN	R	0h	Big-endian input state
13:9	RESERVED	NONE	0h	Reserved
8	SINGLE_STEP	R/W	0h	Single step enable: 0=PDSP will free run when enabled, 1=PDSP will execute a single instruction and then the pdsp_enable bit will be cleared
7:5	RESERVED	NONE	0h	Reserved
4	RESTART	R/W	0h	Causes PDSP to stop current operation gracefully and return to the PC reset value
3	COUNTER_ENABLE	R/W	0h	PDSP cycle counter enable: 0=Counters not enabled, 1=Counters enabled
2	PDSP_SLEEPING	R/W	0h	PDSP sleep indicator: 0=PDSP is not asleep, 1=PDSP us asleep
1	PDSP_ENABLE	R/W	0h	PDSP enable: 0=PDSP is disabled, 1=PDSP is enabled
0	SOFT_RST_N	R	1h	Soft reset. When this bit is cleared, the PDSP will be reset. This bit is set back to 1 on the next cycle after it has been cleared.

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4.2.2.106 ICSSM_PR1_PDSP0_IRAM_STATUS Register

4.2.2.106.1 ICSSM_PR1_PDSP0_IRAM_STATUS Register (Offset = 4h) [reset = 0h]

STATUS

Return to Summary Table

Table 4-1229. Instance Table

Instance Name	Physical Address
ICSSM0	4802 2004h

Figure 4-592. ICSSM_PR1_PDSP0_IRAM_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PCOUNTER							
R							
0h							
7	6	5	4	3	2	1	0
PCOUNTER							
R							
0h							

Table 4-1230. ICSSM_PR1_PDSP0_IRAM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PCOUNTER	R	0h	Current PDSP program counter

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4.2.2.107 ICSSM_PR1_PDSP0_IRAM_WAKEUP_ENABLE Register

4.2.2.107.1 ICSSM_PR1_PDSP0_IRAM_WAKEUP_ENABLE Register (Offset = 8h) [reset = 0h]

WAKEUP_ENABLE

Return to Summary Table

Table 4-1231. Instance Table

Instance Name	Physical Address
ICSSM0	4802 2008h

Figure 4-593. ICSSM_PR1_PDSP0_IRAM_WAKEUP_ENABLE Name Register

31	30	29	28	27	26	25	24
BITWISE_ENABLES							
R/W							
0h							
23	22	21	20	19	18	17	16
BITWISE_ENABLES							
R/W							
0h							
15	14	13	12	11	10	9	8
BITWISE_ENABLES							
R/W							
0h							
7	6	5	4	3	2	1	0
BITWISE_ENABLES							
R/W							
0h							

Table 4-1232. ICSSM_PR1_PDSP0_IRAM_WAKEUP_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BITWISE_ENABLES	R/W	0h	Wakeup enables

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4.2.2.108 ICSSM_PR1_PDSP0_IRAM_CYCLE_COUNT Register

4.2.2.108.1 ICSSM_PR1_PDSP0_IRAM_CYCLE_COUNT Register (Offset = Ch) [reset = 0h]

CYCLE_COUNT

Return to Summary Table

Table 4-1233. Instance Table

Instance Name	Physical Address
ICSSM0	4802 200Ch

Figure 4-594. ICSSM_PR1_PDSP0_IRAM_CYCLE_COUNT Name Register

31	30	29	28	27	26	25	24
CYCLECOUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CYCLECOUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CYCLECOUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CYCLECOUNT							
R/W							
0h							

Table 4-1234. ICSSM_PR1_PDSP0_IRAM_CYCLE_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CYCLECOUNT	R/W	0h	This value is incremented by 1 for every clock cycle during which the PDSP is enabled and the counter is enabled.

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4.2.2.109 ICSSM_PR1_PDSP0_IRAM_STALL_COUNT Register

4.2.2.109.1 ICSSM_PR1_PDSP0_IRAM_STALL_COUNT Register (Offset = 10h) [reset = 0h]

STALL_COUNT

Return to Summary Table

Table 4-1235. Instance Table

Instance Name	Physical Address
ICSSM0	4802 2010h

Figure 4-595. ICSSM_PR1_PDSP0_IRAM_STALL_COUNT Name Register

31	30	29	28	27	26	25	24
STALLCOUNT							
R							
0h							
23	22	21	20	19	18	17	16
STALLCOUNT							
R							
0h							
15	14	13	12	11	10	9	8
STALLCOUNT							
R							
0h							
7	6	5	4	3	2	1	0
STALLCOUNT							
R							
0h							

Table 4-1236. ICSSM_PR1_PDSP0_IRAM_STALL_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STALLCOUNT	R	0h	This value is incremented by 1 for every clock cycle during which the PDSP is enabled, the counter is enabled, and the PDSP was unable to fetch a new instruction for any reason.

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4.2.2.110 ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_BLOCK_INDEX_0 Register

4.2.2.110.1 ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_BLOCK_INDEX_0 Register (Offset = 20h) [reset = 0h]

CONSTANT_TABLE_BLOCK_INDEX_0

Return to Summary Table

Table 4-1237. Instance Table

Instance Name	Physical Address
ICSSM0	4802 2020h

Figure 4-596. ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_BLOCK_INDEX_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
C25_BLK_INDEX							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
C24_BLK_INDEX							
R/W							
0h							

Table 4-1238. ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_BLOCK_INDEX_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	C25_BLK_INDEX	R/W	0h	PDSP constant entry 25 block index
15:8	RESERVED	NONE	0h	Reserved
7:0	C24_BLK_INDEX	R/W	0h	PDSP constant entry 24 block index

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4.2.2.111 ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_BLOCK_INDEX_1 Register

4.2.2.111.1 ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_BLOCK_INDEX_1 Register (Offset = 24h) [reset = 0h]

CONSTANT_TABLE_BLOCK_INDEX_1

Return to Summary Table

Table 4-1239. Instance Table

Instance Name	Physical Address
ICSSM0	4802 2024h

Figure 4-597. ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_BLOCK_INDEX_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
C27_BLK_INDEX							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C26_BLK_INDEX							
R/W							
0h							

Table 4-1240. ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_BLOCK_INDEX_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	C27_BLK_INDEX	R/W	0h	PDSP constant entry 27 block index
15:8	RESERVED	NONE	0h	Reserved
7:0	C26_BLK_INDEX	R/W	0h	PDSP constant entry 26 block index

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4.2.2.112 ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_PROG_PTR_0 Register

4.2.2.112.1 ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_PROG_PTR_0 Register (Offset = 28h) [reset = 0h]

CONSTANT_TABLE_PROG_PTR_0

Return to Summary Table

Table 4-1241. Instance Table

Instance Name	Physical Address
ICSSM0	4802 2028h

Figure 4-598. ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_PROG_PTR_0 Name Register

31	30	29	28	27	26	25	24
C29_POINTER							
R/W							
0h							
23	22	21	20	19	18	17	16
C29_POINTER							
R/W							
0h							
15	14	13	12	11	10	9	8
C28_POINTER							
R/W							
0h							
7	6	5	4	3	2	1	0
C28_POINTER							
R/W							
0h							

Table 4-1242. ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_PROG_PTR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	C29_POINTER	R/W	0h	PDSP constant entry 29 pointer
15:0	C28_POINTER	R/W	0h	PDSP constant entry 28 pointer

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4.2.2.113 ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_PROG_PTR_1 Register

4.2.2.113.1 ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_PROG_PTR_1 Register (Offset = 2Ch) [reset = 0h]

CONSTANT_TABLE_PROG_PTR_1

Return to Summary Table

Table 4-1243. Instance Table

Instance Name	Physical Address
ICSSM0	4802 202Ch

Figure 4-599. ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_PROG_PTR_1 Name Register

31	30	29	28	27	26	25	24
C31_POINTER							
R/W							
0h							
23	22	21	20	19	18	17	16
C31_POINTER							
R/W							
0h							
15	14	13	12	11	10	9	8
C30_POINTER							
R/W							
0h							
7	6	5	4	3	2	1	0
C30_POINTER							
R/W							
0h							

Table 4-1244. ICSSM_PR1_PDSP0_IRAM_CONSTANT_TABLE_PROG_PTR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	C31_POINTER	R/W	0h	PDSP constant entry 31 pointer
15:0	C30_POINTER	R/W	0h	PDSP constant entry 30 pointer

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4.2.2.114 ICSSM_PR1_PDSP0_IRAM_DEBUG_IGP_J Register

4.2.2.114.1 ICSSM_PR1_PDSP0_IRAM_DEBUG_IGP_J Register (Offset = 0h) [reset = 0h]

PDSP Internal General Purpose Register.

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Table 4-1245. Instance Table

Instance Name	Physical Address
ICSSM0	4802 2400h + formula

Figure 4-600. ICSSM_PR1_PDSP0_IRAM_DEBUG_IGP_j Name Register

31	30	29	28	27	26	25	24
REGN							
R/W							
0h							
23	22	21	20	19	18	17	16
REGN							
R/W							
0h							
15	14	13	12	11	10	9	8
REGN							
R/W							
0h							
7	6	5	4	3	2	1	0
REGN							
R/W							
0h							

Table 4-1246. ICSSM_PR1_PDSP0_IRAM_DEBUG_IGP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REGN	R/W	0h	PDSP Internal GP Register N

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4.2.2.115 ICSSM_PR1_PDSP0_IRAM_DEBUG_ICTE_J Register

4.2.2.115.1 ICSSM_PR1_PDSP0_IRAM_DEBUG_ICTE_J Register (Offset = 80h) [reset = 0h]

PDSP Internal Contants Table Entry Register.

Return to Summary Table

Table 4-1247. Instance Table

Instance Name	Physical Address
ICSSM0	4802 2480h + formula

Figure 4-601. ICSSM_PR1_PDSP0_IRAM_DEBUG_ICTE_j Name Register

31	30	29	28	27	26	25	24
CT_ENTRYN							
R							
0h							
23	22	21	20	19	18	17	16
CT_ENTRYN							
R							
0h							
15	14	13	12	11	10	9	8
CT_ENTRYN							
R							
0h							
7	6	5	4	3	2	1	0
CT_ENTRYN							
R							
0h							

Table 4-1248. ICSSM_PR1_PDSP0_IRAM_DEBUG_ICTE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CT_ENTRYN	R	0h	PDSP Internal Constants Table Entry N

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4.2.2.116 ICSSM_PR1_PDSP1_IRAM_CONTROL Register

4.2.2.116.1 ICSSM_PR1_PDSP1_IRAM_CONTROL Register (Offset = 0h) [reset = 1h]

CONTROL

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Table 4-1249. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4000h

Figure 4-602. ICSSM_PR1_PDSP1_IRAM_CONTROL Name Register

31	30	29	28	27	26	25	24
PCOUNTER_RST_VAL							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PCOUNTER_RST_VAL							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PDSP_STATE	BIG_ENDIAN	RESERVED					SINGLE_STEP
R	R	NONE					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			RESTART	COUNTER_ENABLE	PDSP_SLEEPING	PDSP_ENABLE	SOFT_RST_N
NONE			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	1h

Table 4-1250. ICSSM_PR1_PDSP1_IRAM_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PCOUNTER_RST_VAL	R/W	0h	Program counter reset value
15	PDSP_STATE	R	0h	PDSP run state: 0=PDSP is halted, 1=PDSP is running
14	BIG_ENDIAN	R	0h	Big-endian input state
13:9	RESERVED	NONE	0h	Reserved
8	SINGLE_STEP	R/W	0h	Single step enable: 0=PDSP will free run when enabled, 1=PDSP will execute a single instruction and then the pdsp_enable bit will be cleared
7:5	RESERVED	NONE	0h	Reserved
4	RESTART	R/W	0h	Causes PDSP to stop current operation gracefully and return to the PC reset value
3	COUNTER_ENABLE	R/W	0h	PDSP cycle counter enable: 0=Counters not enabled, 1=Counters enabled
2	PDSP_SLEEPING	R/W	0h	PDSP sleep indicator: 0=PDSP is not asleep, 1=PDSP us asleep
1	PDSP_ENABLE	R/W	0h	PDSP enable: 0=PDSP is disabled, 1=PDSP is enabled
0	SOFT_RST_N	R	1h	Soft reset. When this bit is cleared, the PDSP will be reset. This bit is set back to 1 on the next cycle after it has been cleared.

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4.2.2.117 ICSSM_PR1_PDSP1_IRAM_STATUS Register

4.2.2.117.1 ICSSM_PR1_PDSP1_IRAM_STATUS Register (Offset = 4h) [reset = 0h]

STATUS

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Table 4-1251. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4004h

Figure 4-603. ICSSM_PR1_PDSP1_IRAM_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PCOUNTER							
R							
0h							
7	6	5	4	3	2	1	0
PCOUNTER							
R							
0h							

Table 4-1252. ICSSM_PR1_PDSP1_IRAM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PCOUNTER	R	0h	Current PDSP program counter

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4.2.2.118 ICSSM_PR1_PDSP1_IRAM_WAKEUP_ENABLE Register

4.2.2.118.1 ICSSM_PR1_PDSP1_IRAM_WAKEUP_ENABLE Register (Offset = 8h) [reset = 0h]

WAKEUP_ENABLE

Return to Summary Table

Table 4-1253. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4008h

Figure 4-604. ICSSM_PR1_PDSP1_IRAM_WAKEUP_ENABLE Name Register

31	30	29	28	27	26	25	24
BITWISE_ENABLES							
R/W							
0h							
23	22	21	20	19	18	17	16
BITWISE_ENABLES							
R/W							
0h							
15	14	13	12	11	10	9	8
BITWISE_ENABLES							
R/W							
0h							
7	6	5	4	3	2	1	0
BITWISE_ENABLES							
R/W							
0h							

Table 4-1254. ICSSM_PR1_PDSP1_IRAM_WAKEUP_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BITWISE_ENABLES	R/W	0h	Wakeup enables

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4.2.2.119 ICSSM_PR1_PDSP1_IRAM_CYCLE_COUNT Register

4.2.2.119.1 ICSSM_PR1_PDSP1_IRAM_CYCLE_COUNT Register (Offset = Ch) [reset = 0h]

CYCLE_COUNT

Return to Summary Table

Table 4-1255. Instance Table

Instance Name	Physical Address
ICSSM0	4802 400Ch

Figure 4-605. ICSSM_PR1_PDSP1_IRAM_CYCLE_COUNT Name Register

31	30	29	28	27	26	25	24
CYCLECOUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
CYCLECOUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
CYCLECOUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CYCLECOUNT							
R/W							
0h							

Table 4-1256. ICSSM_PR1_PDSP1_IRAM_CYCLE_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CYCLECOUNT	R/W	0h	This value is incremented by 1 for every clock cycle during which the PDSP is enabled and the counter is enabled.

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4.2.2.120 ICSSM_PR1_PDSP1_IRAM_STALL_COUNT Register

4.2.2.120.1 ICSSM_PR1_PDSP1_IRAM_STALL_COUNT Register (Offset = 10h) [reset = 0h]

STALL_COUNT

Return to Summary Table

Table 4-1257. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4010h

Figure 4-606. ICSSM_PR1_PDSP1_IRAM_STALL_COUNT Name Register

31	30	29	28	27	26	25	24
STALLCOUNT							
R							
0h							
23	22	21	20	19	18	17	16
STALLCOUNT							
R							
0h							
15	14	13	12	11	10	9	8
STALLCOUNT							
R							
0h							
7	6	5	4	3	2	1	0
STALLCOUNT							
R							
0h							

Table 4-1258. ICSSM_PR1_PDSP1_IRAM_STALL_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STALLCOUNT	R	0h	This value is incremented by 1 for every clock cycle during which the PDSP is enabled, the counter is enabled, and the PDSP was unable to fetch a new instruction for any reason.

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4.2.2.121 ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_BLOCK_INDEX_0 Register

4.2.2.121.1 ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_BLOCK_INDEX_0 Register (Offset = 20h) [reset = 0h]

CONSTANT_TABLE_BLOCK_INDEX_0

Return to Summary Table

Table 4-1259. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4020h

Figure 4-607. ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_BLOCK_INDEX_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
C25_BLK_INDEX							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
C24_BLK_INDEX							
R/W							
0h							

Table 4-1260. ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_BLOCK_INDEX_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	C25_BLK_INDEX	R/W	0h	PDSP constant entry 25 block index
15:8	RESERVED	NONE	0h	Reserved
7:0	C24_BLK_INDEX	R/W	0h	PDSP constant entry 24 block index

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4.2.2.122 ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_BLOCK_INDEX_1 Register

4.2.2.122.1 ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_BLOCK_INDEX_1 Register (Offset = 24h) [reset = 0h]

CONSTANT_TABLE_BLOCK_INDEX_1

Return to Summary Table

Table 4-1261. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4024h

Figure 4-608. ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_BLOCK_INDEX_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
C27_BLK_INDEX							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C26_BLK_INDEX							
R/W							
0h							

Table 4-1262. ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_BLOCK_INDEX_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	C27_BLK_INDEX	R/W	0h	PDSP constant entry 27 block index
15:8	RESERVED	NONE	0h	Reserved
7:0	C26_BLK_INDEX	R/W	0h	PDSP constant entry 26 block index

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4.2.2.123 ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_PROG_PTR_0 Register

4.2.2.123.1 ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_PROG_PTR_0 Register (Offset = 28h) [reset = 0h]

CONSTANT_TABLE_PROG_PTR_0

Return to Summary Table

Table 4-1263. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4028h

Figure 4-609. ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_PROG_PTR_0 Name Register

31	30	29	28	27	26	25	24
C29_POINTER							
R/W							
0h							
23	22	21	20	19	18	17	16
C29_POINTER							
R/W							
0h							
15	14	13	12	11	10	9	8
C28_POINTER							
R/W							
0h							
7	6	5	4	3	2	1	0
C28_POINTER							
R/W							
0h							

Table 4-1264. ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_PROG_PTR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	C29_POINTER	R/W	0h	PDSP constant entry 29 pointer
15:0	C28_POINTER	R/W	0h	PDSP constant entry 28 pointer

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4.2.2.124 ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_PROG_PTR_1 Register

4.2.2.124.1 ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_PROG_PTR_1 Register (Offset = 2Ch) [reset = 0h]

CONSTANT_TABLE_PROG_PTR_1

Return to Summary Table

Table 4-1265. Instance Table

Instance Name	Physical Address
ICSSM0	4802 402Ch

Figure 4-610. ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_PROG_PTR_1 Name Register

31	30	29	28	27	26	25	24
C31_POINTER							
R/W							
0h							
23	22	21	20	19	18	17	16
C31_POINTER							
R/W							
0h							
15	14	13	12	11	10	9	8
C30_POINTER							
R/W							
0h							
7	6	5	4	3	2	1	0
C30_POINTER							
R/W							
0h							

Table 4-1266. ICSSM_PR1_PDSP1_IRAM_CONSTANT_TABLE_PROG_PTR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	C31_POINTER	R/W	0h	PDSP constant entry 31 pointer
15:0	C30_POINTER	R/W	0h	PDSP constant entry 30 pointer

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4.2.2.125 ICSSM_PR1_PDSP1_IRAM_DEBUG_IGP_J Register

4.2.2.125.1 ICSSM_PR1_PDSP1_IRAM_DEBUG_IGP_J Register (Offset = 0h) [reset = 0h]

PDSP Internal General Purpose Register.

Return to Summary Table

Table 4-1267. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4400h + formula

Figure 4-611. ICSSM_PR1_PDSP1_IRAM_DEBUG_IGP_j Name Register

31	30	29	28	27	26	25	24
REGN							
R/W							
0h							
23	22	21	20	19	18	17	16
REGN							
R/W							
0h							
15	14	13	12	11	10	9	8
REGN							
R/W							
0h							
7	6	5	4	3	2	1	0
REGN							
R/W							
0h							

Table 4-1268. ICSSM_PR1_PDSP1_IRAM_DEBUG_IGP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REGN	R/W	0h	PDSP Internal GP Register N

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4.2.2.126 ICSSM_PR1_PDSP1_IRAM_DEBUG_ICTE_J Register

4.2.2.126.1 ICSSM_PR1_PDSP1_IRAM_DEBUG_ICTE_J Register (Offset = 80h) [reset = 0h]

PDSP Internal Contants Table Entry Register.

Return to Summary Table

Table 4-1269. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4480h + formula

Figure 4-612. ICSSM_PR1_PDSP1_IRAM_DEBUG_ICTE_j Name Register

31	30	29	28	27	26	25	24
CT_ENTRYN							
R							
0h							
23	22	21	20	19	18	17	16
CT_ENTRYN							
R							
0h							
15	14	13	12	11	10	9	8
CT_ENTRYN							
R							
0h							
7	6	5	4	3	2	1	0
CT_ENTRYN							
R							
0h							

Table 4-1270. ICSSM_PR1_PDSP1_IRAM_DEBUG_ICTE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CT_ENTRYN	R	0h	PDSP Internal Constants Table Entry N

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4.2.2.127 ICSSM_PR1_PROTECT_SLV_UNLOCK_KEY Register

4.2.2.127.1 ICSSM_PR1_PROTECT_SLV_UNLOCK_KEY Register (Offset = 0h) [reset = 0h]

LOCK KEY

Return to Summary Table

Table 4-1271. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4C00h

Figure 4-613. ICSSM_PR1_PROTECT_SLV_UNLOCK_KEY Name Register

31	30	29	28	27	26	25	24
UNLOCK_KEY							
R/W							
0h							
23	22	21	20	19	18	17	16
UNLOCK_KEY							
R/W							
0h							
15	14	13	12	11	10	9	8
UNLOCK_KEY							
R/W							
0h							
7	6	5	4	3	2	1	0
UNLOCK_KEY							
R/W							
0h							

Table 4-1272. ICSSM_PR1_PROTECT_SLV_UNLOCK_KEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UNLOCK_KEY	R/W	0h	UnLock Key Pattern 0x83E7_0B13 to UnLock 0x0000_0000 to Lock Must unlock to update MMRs

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4.2.2.128 ICSSM_PR1_PROTECT_SLV_CFG Register

4.2.2.128.1 ICSSM_PR1_PROTECT_SLV_CFG Register (Offset = 4h) [reset = 0h]

Config.

Return to Summary Table

Table 4-1273. Instance Table

Instance Name	Physical Address
ICSSM0	4802 4C04h

Figure 4-614. ICSSM_PR1_PROTECT_SLV_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	PRU1_DMEM1_LOCK_EN	PRU0_DMEM0_LOCK_EN	ICSS_CFG_WP_EN	RTU1_PRU_WP_EN	RTU0_PRU_WP_EN	PRU1_WP_EN	PRU0_WP_EN
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1274. ICSSM_PR1_PROTECT_SLV_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	PRU1_DMEM1_LOCK_EN	R/W	0h	Write Protect DMEM1 0:disable 1:enable When enabled only PRU1 can write to DMEM1
5	PRU0_DMEM0_LOCK_EN	R/W	0h	Write Protect DMEM0 0:disable 1:enable When enabled only PRU0 can write to DMEM0
4	ICSS_CFG_WP_EN	R/W	0h	Write Protect ICSS_CFG 0:disable 1:enable
3	RTU1_PRU_WP_EN	R/W	0h	Write Protect RTU1_PRU access Debug IMEM 0:disable 1:enable
2	RTU0_PRU_WP_EN	R/W	0h	Write Protect RTU0_PRU access Debug IMEM 0:disable 1:enable
1	PRU1_WP_EN	R/W	0h	Write Protect PRU1 access Debug IMEM 0:disable 1:enable
0	PRU0_WP_EN	R/W	0h	Write Protect PRU0 access Debug IMEM 0:disable 1:enable

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4.2.2.129 ICSSM_PR1_CFG_SLV_PID_REG Register

4.2.2.129.1 ICSSM_PR1_CFG_SLV_PID_REG Register (Offset = 0h) [reset = 6B080203h]

PID Register

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Table 4-1275. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6000h

Figure 4-615. ICSSM_PR1_CFG_SLV_PID_REG Name Register

31	30	29	28	27	26	25	24
ICSS_IDVER							
R							
6B080203h							
23	22	21	20	19	18	17	16
ICSS_IDVER							
R							
6B080203h							
15	14	13	12	11	10	9	8
ICSS_IDVER							
R							
6B080203h							
7	6	5	4	3	2	1	0
ICSS_IDVER							
R							
6B080203h							

Table 4-1276. ICSSM_PR1_CFG_SLV_PID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ICSS_IDVER	R	6B080203h	Module ID field

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4.2.2.130 ICSSM_PR1_CFG_SLV_HWDIS_REG Register

4.2.2.130.1 ICSSM_PR1_CFG_SLV_HWDIS_REG Register (Offset = 4h) [reset = 0h]

HW DIS Register

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Table 4-1277. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6004h

Figure 4-616. ICSSM_PR1_CFG_SLV_HWDIS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
HWDIS							
R							
0h							

Table 4-1278. ICSSM_PR1_CFG_SLV_HWDIS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	HWDIS	R	0h	HW Disable Observation

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4.2.2.131 ICSSM_PR1_CFG_SLV_GPCFG0_REG Register

4.2.2.131.1 ICSSM_PR1_CFG_SLV_GPCFG0_REG Register (Offset = 8h) [reset = 0h]

gpcfg0 Register

Return to Summary Table

Table 4-1279. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6008h

Figure 4-617. ICSSM_PR1_CFG_SLV_GPCFG0_REG Name Register

31	30	29	28	27	26	25	24
RESERVED		PR1_PRU0_GP_MUX_SEL				PRU0_GPO_SH1_SEL	PRU0_GPO_DIV1
NONE		R/W				R	R/W
0h		0h				0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_GPO_DIV1				PRU0_GPO_DIV0			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_GPO_DIV0	PRU0_GPO_MODE	PRU0_GPI_SB	PRU0_GPI_DIV1				
R/W	R/W	R/W1TC	R/W				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_GPI_DIV0					PRU0_GPI_CLK_MODE	PRU0_GPI_MODE	
R/W					R/W	R/W	
0h					0h	0h	

Table 4-1280. ICSSM_PR1_CFG_SLV_GPCFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:26	PR1_PRU0_GP_MUX_SEL	R/W	0h	
25	PRU0_GPO_SH1_SEL	R	0h	
24:20	PRU0_GPO_DIV1	R/W	0h	
19:15	PRU0_GPO_DIV0	R/W	0h	
14	PRU0_GPO_MODE	R/W	0h	
13	PRU0_GPI_SB	R/W1TC	0h	
12:8	PRU0_GPI_DIV1	R/W	0h	
7:3	PRU0_GPI_DIV0	R/W	0h	
2	PRU0_GPI_CLK_MODE	R/W	0h	
1:0	PRU0_GPI_MODE	R/W	0h	

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4.2.2.132 ICSSM_PR1_CFG_SLV_GPCFG1_REG Register

4.2.2.132.1 ICSSM_PR1_CFG_SLV_GPCFG1_REG Register (Offset = Ch) [reset = 0h]

gpcfg1 Register

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Table 4-1281. Instance Table

Instance Name	Physical Address
ICSSM0	4802 600Ch

Figure 4-618. ICSSM_PR1_CFG_SLV_GPCFG1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED		PR1_PRU1_GP_MUX_SEL				PRU1_GPO_SH1_SEL	PRU1_GPO_DIV1
NONE		R/W				R	R/W
0h		0h				0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_GPO_DIV1				PRU1_GPO_DIV0			
R/W				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_GPO_DIV0	PRU1_GPO_MODE	PRU1_GPI_SB	PRU1_GPI_DIV1				
R/W	R/W	R/W1TC	R/W				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_GPI_DIV0					PRU1_GPI_CLK_MODE	PRU1_GPI_MODE	
R/W					R/W	R/W	
0h					0h	0h	

Table 4-1282. ICSSM_PR1_CFG_SLV_GPCFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:26	PR1_PRU1_GP_MUX_SEL	R/W	0h	
25	PRU1_GPO_SH1_SEL	R	0h	
24:20	PRU1_GPO_DIV1	R/W	0h	
19:15	PRU1_GPO_DIV0	R/W	0h	
14	PRU1_GPO_MODE	R/W	0h	
13	PRU1_GPI_SB	R/W1TC	0h	
12:8	PRU1_GPI_DIV1	R/W	0h	
7:3	PRU1_GPI_DIV0	R/W	0h	
2	PRU1_GPI_CLK_MODE	R/W	0h	
1:0	PRU1_GPI_MODE	R/W	0h	

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4.2.2.133 ICSSM_PR1_CFG_SLV_CGR_REG Register

4.2.2.133.1 ICSSM_PR1_CFG_SLV_CGR_REG Register (Offset = 10h) [reset = A0324900h]

cgr Register

Return to Summary Table

Table 4-1283. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6010h

Figure 4-619. ICSSM_PR1_CFG_SLV_CGR_REG Name Register

31	30	29	28	27	26	25	24
ICSS_STOP_ACK	ICSS_STOP_REQ	ICSS_PWR_IDLE	RESERVED				
R/W	R	R/W	NONE				
1h	0h	1h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		BOTTOM_HALF_CLK_GATE_EN	TOP_HALF_CLK_GATE_EN	AUTO_SLICE1_CLK_GATE_EN	AUTO_SLICE0_CLK_GATE_EN	IEP_CLK_EN	IEP_CLK_STOP_ACK
NONE		R/W	R/W	R/W	R/W	R/W	R
0h		1h	1h	0h	0h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IEP_CLK_STOP_REQ	ECAP_CLK_EN	ECAP_CLK_STOP_ACK	ECAP_CLK_STOP_REQ	UART_CLK_EN	UART_CLK_STOP_ACK	UART_CLK_STOP_REQ	INTC_CLK_EN
R/W	R/W	R	R/W	R/W	R	R/W	R/W
0h	1h	0h	0h	1h	0h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTC_CLK_STOP_ACK	INTC_CLK_STOP_REQ	RESERVED					
R	R/W	NONE					
0h	0h	0h					

Table 4-1284. ICSSM_PR1_CFG_SLV_CGR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ICSS_STOP_ACK	R/W	1h	
30	ICSS_STOP_REQ	R	0h	
29	ICSS_PWR_IDLE	R/W	1h	
28:22	RESERVED	NONE	0h	Reserved
21	BOTTOM_HALF_CLK_GATE_EN	R/W	1h	
20	TOP_HALF_CLK_GATE_EN	R/W	1h	
19	AUTO_SLICE1_CLK_GATE_EN	R/W	0h	
18	AUTO_SLICE0_CLK_GATE_EN	R/W	0h	
17	IEP_CLK_EN	R/W	1h	
16	IEP_CLK_STOP_ACK	R	0h	
15	IEP_CLK_STOP_REQ	R/W	0h	
14	ECAP_CLK_EN	R/W	1h	
13	ECAP_CLK_STOP_ACK	R	0h	

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Table 4-1284. ICSSM_PR1_CFG_SLV_CGR_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	ECAP_CLK_STOP_REQ	R/W	0h	
11	UART_CLK_EN	R/W	1h	
10	UART_CLK_STOP_ACK	R	0h	
9	UART_CLK_STOP_REQ	R/W	0h	
8	INTC_CLK_EN	R/W	1h	
7	INTC_CLK_STOP_ACK	R	0h	
6	INTC_CLK_STOP_REQ	R/W	0h	
5:0	RESERVED	NONE	0h	Reserved

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4.2.2.134 ICSSM_PR1_CFG_SLV_GPECFG0_REG Register

4.2.2.134.1 ICSSM_PR1_CFG_SLV_GPECFG0_REG Register (Offset = 14h) [reset = 23h]

gpecfg0 Register

Return to Summary Table

Table 4-1285. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6014h

Figure 4-620. ICSSM_PR1_CFG_SLV_GPECFG0_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						PRU0_GPO_SHIFT_CLK_DONE	PRU0_GPO_SHIFT_CLK_HIGH
NONE						R/W1C	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
PRU0_GPO_SHIFT_CNT							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED	PRU0_GPO_SHIFT_GP_EN	PRU0_GPO_SHIFT_CLK_FREE	PRU0_GPO_SHIFT_SWAP	RESERVED		PRU0_GPI_SHIFT_EN	PRU0_GPI_SB_P
NONE	R/W	R/W	R/W	NONE		R/W	R/W
0h	0h	1h	0h	0h		1h	1h

Table 4-1286. ICSSM_PR1_CFG_SLV_GPECFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	PRU0_GPO_SHIFT_CLK_DONE	R/W1C	0h	
16	PRU0_GPO_SHIFT_CLK_HIGH	R/W	0h	
15:8	PRU0_GPO_SHIFT_CNT	R/W	0h	
7	RESERVED	NONE	0h	Reserved
6	PRU0_GPO_SHIFT_GP_EN	R/W	0h	
5	PRU0_GPO_SHIFT_CLK_FREE	R/W	1h	
4	PRU0_GPO_SHIFT_SWAP	R/W	0h	
3:2	RESERVED	NONE	0h	Reserved
1	PRU0_GPI_SHIFT_EN	R/W	1h	
0	PRU0_GPI_SB_P	R/W	1h	

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4.2.2.135 ICSSM_PR1_CFG_SLV_GPECFG1_REG Register

4.2.2.135.1 ICSSM_PR1_CFG_SLV_GPECFG1_REG Register (Offset = 18h) [reset = 23h]

gpecfg1 Register

Return to Summary Table

Table 4-1287. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6018h

Figure 4-621. ICSSM_PR1_CFG_SLV_GPECFG1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED						PRU1_GPO_SHIFT_CLK_DONE	PRU1_GPO_SHIFT_CLK_HIGH
NONE						R/W1C	R/W
0h						0h	0h

15	14	13	12	11	10	9	8
PRU1_GPO_SHIFT_CNT							
R/W							
0h							

7	6	5	4	3	2	1	0
RESERVED	PRU1_GPO_SHIFT_GP_EN	PRU1_GPO_SHIFT_CLK_FREE	PRU1_GPO_SHIFT_SWAP	RESERVED		PRU1_GPI_SHIFT_EN	PRU1_GPI_SB_P
NONE	R/W	R/W	R/W	NONE		R/W	R/W
0h	0h	1h	0h	0h		1h	1h

Table 4-1288. ICSSM_PR1_CFG_SLV_GPECFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	PRU1_GPO_SHIFT_CLK_DONE	R/W1C	0h	
16	PRU1_GPO_SHIFT_CLK_HIGH	R/W	0h	
15:8	PRU1_GPO_SHIFT_CNT	R/W	0h	
7	RESERVED	NONE	0h	Reserved
6	PRU1_GPO_SHIFT_GP_EN	R/W	0h	
5	PRU1_GPO_SHIFT_CLK_FREE	R/W	1h	
4	PRU1_GPO_SHIFT_SWAP	R/W	0h	
3:2	RESERVED	NONE	0h	Reserved
1	PRU1_GPI_SHIFT_EN	R/W	1h	
0	PRU1_GPI_SB_P	R/W	1h	

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4.2.2.136 ICSSM_PR1_CFG_SLV_RESET_ISO_REG Register

4.2.2.136.1 ICSSM_PR1_CFG_SLV_RESET_ISO_REG Register (Offset = 1Ch) [reset = 0h]

Reset ISO Register

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Table 4-1289. Instance Table

Instance Name	Physical Address
ICSSM0	4802 601Ch

Figure 4-622. ICSSM_PR1_CFG_SLV_RESET_ISO_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RESET_ISO_EDGE	RESET_ISO_ACK	RESET_ISO_REQ
NONE					W	W	R/W1C
0h					0h	0h	0h

Table 4-1290. ICSSM_PR1_CFG_SLV_RESET_ISO_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	RESET_ISO_EDGE	W	0h	
1	RESET_ISO_ACK	W	0h	
0	RESET_ISO_REQ	R/W1C	0h	

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4.2.2.137 ICSSM_PR1_CFG_SLV_MII_RT_REG Register

4.2.2.137.1 ICSSM_PR1_CFG_SLV_MII_RT_REG Register (Offset = 2Ch) [reset = 1h]

mii_rt Register

Return to Summary Table

Table 4-1291. Instance Table

Instance Name	Physical Address
ICSSM0	4802 602Ch

Figure 4-623. ICSSM_PR1_CFG_SLV_MII_RT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							MII_RT_EVENT_EN
NONE							R/W
0h							1h

Table 4-1292. ICSSM_PR1_CFG_SLV_MII_RT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	MII_RT_EVENT_EN	R/W	1h	

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4.2.2.138 ICSSM_PR1_CFG_SLV_IEPCLK_REG Register

4.2.2.138.1 ICSSM_PR1_CFG_SLV_IEPCLK_REG Register (Offset = 30h) [reset = 0h]

iepclk Register

Return to Summary Table

Table 4-1293. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6030h

Figure 4-624. ICSSM_PR1_CFG_SLV_IEPCLK_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						IEP1_SLV_EN	IEP_OCP_CLK_EN
NONE						R/W	R/W
0h						0h	0h

Table 4-1294. ICSSM_PR1_CFG_SLV_IEPCLK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	IEP1_SLV_EN	R/W	0h	
0	IEP_OCP_CLK_EN	R/W	0h	

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4.2.2.139 ICSSM_PR1_CFG_SLV_SPP_REG Register

4.2.2.139.1 ICSSM_PR1_CFG_SLV_SPP_REG Register (Offset = 34h) [reset = 0h]

spp Register

Return to Summary Table

Table 4-1295. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6034h

Figure 4-625. ICSSM_PR1_CFG_SLV_SPP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RTU_XFR_SHIFT_EN	XFR_BYTE_SHIFT_EN	XFR_SHIFT_EN	PRU1_PAD_HP_EN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 4-1296. ICSSM_PR1_CFG_SLV_SPP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RTU_XFR_SHIFT_EN	R/W	0h	
2	XFR_BYTE_SHIFT_EN	R/W	0h	
1	XFR_SHIFT_EN	R/W	0h	
0	PRU1_PAD_HP_EN	R/W	0h	

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4.2.2.140 ICSSM_PR1_CFG_SLV_SPIN_CFG_REG Register

4.2.2.140.1 ICSSM_PR1_CFG_SLV_SPIN_CFG_REG Register (Offset = 38h) [reset = 0h]

Spin Lock CFG Register

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Table 4-1297. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6038h

Figure 4-626. ICSSM_PR1_CFG_SLV_SPIN_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SPIN_CLOCK_TX_PRU_EN
NONE							R/W
0h							0h

Table 4-1298. ICSSM_PR1_CFG_SLV_SPIN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SPIN_CLOCK_TX_PRU_EN	R/W	0h	

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4.2.2.141 ICSSM_PR1_CFG_SLV_CORE_SYNC_REG Register

4.2.2.141.1 ICSSM_PR1_CFG_SLV_CORE_SYNC_REG Register (Offset = 3Ch) [reset = 0h]

Core Sync Register

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Table 4-1299. Instance Table

Instance Name	Physical Address
ICSSM0	4802 603Ch

Figure 4-627. ICSSM_PR1_CFG_SLV_CORE_SYNC_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CORE_VBUSP_SYNC_EN
NONE							R/W
0h							0h

Table 4-1300. ICSSM_PR1_CFG_SLV_CORE_SYNC_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CORE_VBUSP_SYNC_EN	R/W	0h	

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4.2.2.142 ICSSM_PR1_CFG_SLV_SA_MX_REG Register

4.2.2.142.1 ICSSM_PR1_CFG_SLV_SA_MX_REG Register (Offset = 40h) [reset = 0h]

sa_mx Register

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Table 4-1301. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6040h

Figure 4-628. ICSSM_PR1_CFG_SLV_SA_MX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PWM_EFC_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED				PWM3_REMAP_EN		PWM0_REMAP_EN	
NONE				R/W		R/W	
0h				0h		0h	
7	6	5	4	3	2	1	0
SA_MUX_SEL							
R/W							
0h							

Table 4-1302. ICSSM_PR1_CFG_SLV_SA_MX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PWM_EFC_EN	R/W	0h	
15:12	RESERVED	NONE	0h	Reserved
11:10	PWM3_REMAP_EN	R/W	0h	
9:8	PWM0_REMAP_EN	R/W	0h	
7:0	SA_MUX_SEL	R/W	0h	

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4.2.2.143 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_DIV_REG Register

4.2.2.143.1 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_DIV_REG Register (Offset = 44h) [reset = 0h]

SD Register

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Table 4-1303. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6044h

Figure 4-629. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_DIV_REG Name Register

31	30	29	28	27	26	25	24
PRU0_SD_MAN_REC_CLK_PERIOD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PRU0_SD_MAN_CLK_CAL_DONE
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_SD_MAN_STATUS	PRU0_SD_CH_SEL				PRU0_SD_MAN_NV_DATA_EN	PRU0_SD_MAN_EN	PRU0_SD_SHARE_EN
R	R/W				R/W	R/W	R/W
0h	0h				0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 4-1304. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_DIV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRU0_SD_MAN_REC_CLK_PERIOD	R	0h	
23:17	RESERVED	NONE	0h	Reserved
16	PRU0_SD_MAN_CLK_CAL_DONE	R	0h	
15	PRU0_SD_MAN_STATUS	R	0h	
14:11	PRU0_SD_CH_SEL	R/W	0h	
10	PRU0_SD_MAN_NV_DATA_EN	R/W	0h	
9	PRU0_SD_MAN_EN	R/W	0h	
8	PRU0_SD_SHARE_EN	R/W	0h	
7:0	RESERVED	NONE	0h	Reserved

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4.2.2.144 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG0 Register

4.2.2.144.1 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG0 Register (Offset = 48h) [reset = 0h]

SD Register

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Table 4-1305. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6048h

Figure 4-630. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>PRU0_FD_ZERO_MAX_0</td><td colspan="5">PRU0_FD_ZERO_MAX_LIMIT_0</td><td>PRU0_FD_ZERO_MIN_0</td></tr>
<tr><td>NONE</td><td>R/W1C</td><td colspan="5">R/W</td><td>R/W1C</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU0_FD_ZERO_MIN_LIMIT_0</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">PRU0_SD_ACC_SEL0</td><td>RESERVED</td><td>PRU0_SD_CLK_INV0</td><td colspan="2">PRU0_SD_CLK_SEL0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R/W</td><td>NONE</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
</table>

Table 4-1306. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU0_FD_ZERO_MAX_0	R/W1C	0h	
21:17	PRU0_FD_ZERO_MAX_LIMIT_0	R/W	0h	
16	PRU0_FD_ZERO_MIN_0	R/W1C	0h	
15:11	PRU0_FD_ZERO_MIN_LIMIT_0	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU0_SD_ACC_SEL0	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU0_SD_CLK_INV0	R/W	0h	
1:0	PRU0_SD_CLK_SEL0	R/W	0h	

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4.2.2.145 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG0 Register

4.2.2.145.1 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG0 Register (Offset = 4Ch) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1307. Instance Table

Instance Name	Physical Address
ICSSM0	4802 604Ch

Figure 4-631. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_FD_EN_0	PRU0_FD_ONE_MAX_0	PRU0_FD_ONE_MAX_LIMIT_0					PRU0_FD_ONE_MIN_0
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ONE_MIN_LIMIT_0					PRU0_FD_WINDOW_SIZE_0		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_SD_SAMPLE_SIZE0							
R/W							
0h							

Table 4-1308. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU0_FD_EN_0	R/W	0h	
22	PRU0_FD_ONE_MAX_0	R/W1C	0h	
21:17	PRU0_FD_ONE_MAX_LIMIT_0	R/W	0h	
16	PRU0_FD_ONE_MIN_0	R/W1C	0h	
15:11	PRU0_FD_ONE_MIN_LIMIT_0	R/W	0h	
10:8	PRU0_FD_WINDOW_SIZE_0	R/W	0h	
7:0	PRU0_SD_SAMPLE_SIZE0	R/W	0h	

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4.2.2.146 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG1 Register

4.2.2.146.1 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG1 Register (Offset = 50h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1309. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6050h

Figure 4-632. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>PRU0_FD_ZERO_MAX_1</td><td colspan="5">PRU0_FD_ZERO_MAX_LIMIT_1</td><td>PRU0_FD_ZERO_MIN_1</td></tr>
<tr><td>NONE</td><td>R/W1C</td><td colspan="5">R/W</td><td>R/W1C</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU0_FD_ZERO_MIN_LIMIT_1</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">PRU0_SD_ACC_SEL1</td><td>RESERVED</td><td>PRU0_SD_CLK_INV1</td><td colspan="2">PRU0_SD_CLK_SEL1</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R/W</td><td>NONE</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
</table>

Table 4-1310. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU0_FD_ZERO_MAX_1	R/W1C	0h	
21:17	PRU0_FD_ZERO_MAX_LIMIT_1	R/W	0h	
16	PRU0_FD_ZERO_MIN_1	R/W1C	0h	
15:11	PRU0_FD_ZERO_MIN_LIMIT_1	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU0_SD_ACC_SEL1	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU0_SD_CLK_INV1	R/W	0h	
1:0	PRU0_SD_CLK_SEL1	R/W	0h	

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4.2.2.147 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG1 Register

4.2.2.147.1 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG1 Register (Offset = 54h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1311. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6054h

Figure 4-633. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRU0_FD_EN_1	PRU0_FD_ONE_MAX_1	PRU0_FD_ONE_MAX_LIMIT_1					PRU0_FD_ONE_MIN_1
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h

15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_1					PRU0_FD_WINDOW_SIZE_1		
R/W					R/W		
0h					0h		

7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE1							
R/W							
0h							

Table 4-1312. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU0_FD_EN_1	R/W	0h	
22	PRU0_FD_ONE_MAX_1	R/W1C	0h	
21:17	PRU0_FD_ONE_MAX_LIMIT_1	R/W	0h	
16	PRU0_FD_ONE_MIN_1	R/W1C	0h	
15:11	PRU0_FD_ONE_MIN_LIMIT_1	R/W	0h	
10:8	PRU0_FD_WINDOW_SIZE_1	R/W	0h	
7:0	PRU0_SD_SAMPLE_SIZE1	R/W	0h	

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4.2.2.148 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG2 Register

4.2.2.148.1 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG2 Register (Offset = 58h) [reset = 0h]

SD Register

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Table 4-1313. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6058h

Figure 4-634. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_2	PRU0_FD_ZERO_MAX_LIMIT_2					PRU0_FD_ZERO_MIN_2
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_2					RESERVED		
R/W					NONE		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL2		RESERVED	PRU0_SD_CLK_INV2	PRU0_SD_CLK_SEL2	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1314. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU0_FD_ZERO_MAX_2	R/W1C	0h	
21:17	PRU0_FD_ZERO_MAX_LIMIT_2	R/W	0h	
16	PRU0_FD_ZERO_MIN_2	R/W1C	0h	
15:11	PRU0_FD_ZERO_MIN_LIMIT_2	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU0_SD_ACC_SEL2	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU0_SD_CLK_INV2	R/W	0h	
1:0	PRU0_SD_CLK_SEL2	R/W	0h	

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4.2.2.149 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG2 Register

4.2.2.149.1 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG2 Register (Offset = 5Ch) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1315. Instance Table

Instance Name	Physical Address
ICSSM0	4802 605Ch

Figure 4-635. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_FD_EN_2	PRU0_FD_ONE_MAX_2	PRU0_FD_ONE_MAX_LIMIT_2					PRU0_FD_ONE_MIN_2
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ONE_MIN_LIMIT_2					PRU0_FD_WINDOW_SIZE_2		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_SD_SAMPLE_SIZE2							
R/W							
0h							

Table 4-1316. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU0_FD_EN_2	R/W	0h	
22	PRU0_FD_ONE_MAX_2	R/W1C	0h	
21:17	PRU0_FD_ONE_MAX_LIMIT_2	R/W	0h	
16	PRU0_FD_ONE_MIN_2	R/W1C	0h	
15:11	PRU0_FD_ONE_MIN_LIMIT_2	R/W	0h	
10:8	PRU0_FD_WINDOW_SIZE_2	R/W	0h	
7:0	PRU0_SD_SAMPLE_SIZE2	R/W	0h	

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4.2.2.150 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG3 Register

4.2.2.150.1 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG3 Register (Offset = 60h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1317. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6060h

Figure 4-636. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_3	PRU0_FD_ZERO_MAX_LIMIT_3					PRU0_FD_ZERO_MIN_3
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_3					RESERVED		
R/W					NONE		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL3		RESERVED	PRU0_SD_CLK_INV3	PRU0_SD_CLK_SEL3	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1318. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU0_FD_ZERO_MAX_3	R/W1C	0h	
21:17	PRU0_FD_ZERO_MAX_LIMIT_3	R/W	0h	
16	PRU0_FD_ZERO_MIN_3	R/W1C	0h	
15:11	PRU0_FD_ZERO_MIN_LIMIT_3	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU0_SD_ACC_SEL3	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU0_SD_CLK_INV3	R/W	0h	
1:0	PRU0_SD_CLK_SEL3	R/W	0h	

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4.2.2.151 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG3 Register

4.2.2.151.1 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG3 Register (Offset = 64h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1319. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6064h

Figure 4-637. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
PRU0_FD_EN_3	PRU0_FD_ONE_MAX_3	PRU0_FD_ONE_MAX_LIMIT_3					PRU0_FD_ONE_MIN_3
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h

15	14	13	12	11	10	9	8
PRU0_FD_ONE_MIN_LIMIT_3					PRU0_FD_WINDOW_SIZE_3		
R/W					R/W		
0h					0h		

7	6	5	4	3	2	1	0
PRU0_SD_SAMPLE_SIZE3							
R/W							
0h							

Table 4-1320. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU0_FD_EN_3	R/W	0h	
22	PRU0_FD_ONE_MAX_3	R/W1C	0h	
21:17	PRU0_FD_ONE_MAX_LIMIT_3	R/W	0h	
16	PRU0_FD_ONE_MIN_3	R/W1C	0h	
15:11	PRU0_FD_ONE_MIN_LIMIT_3	R/W	0h	
10:8	PRU0_FD_WINDOW_SIZE_3	R/W	0h	
7:0	PRU0_SD_SAMPLE_SIZE3	R/W	0h	

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4.2.2.152 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG4 Register

4.2.2.152.1 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG4 Register (Offset = 68h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1321. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6068h

Figure 4-638. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRU0_FD_ZERO_MAX_4	PRU0_FD_ZERO_MAX_LIMIT_4					PRU0_FD_ZERO_MIN_4
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ZERO_MIN_LIMIT_4					RESERVED		
R/W					NONE		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PRU0_SD_ACC_SEL4		RESERVED	PRU0_SD_CLK_INV4	PRU0_SD_CLK_SEL4	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1322. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU0_FD_ZERO_MAX_4	R/W1C	0h	
21:17	PRU0_FD_ZERO_MAX_LIMIT_4	R/W	0h	
16	PRU0_FD_ZERO_MIN_4	R/W1C	0h	
15:11	PRU0_FD_ZERO_MIN_LIMIT_4	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU0_SD_ACC_SEL4	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU0_SD_CLK_INV4	R/W	0h	
1:0	PRU0_SD_CLK_SEL4	R/W	0h	

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4.2.2.153 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG4 Register

4.2.2.153.1 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG4 Register (Offset = 6Ch) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1323. Instance Table

Instance Name	Physical Address
ICSSM0	4802 606Ch

Figure 4-639. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_FD_EN_4	PRU0_FD_ONE_MAX_4	PRU0_FD_ONE_MAX_LIMIT_4					PRU0_FD_ONE_MIN_4
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ONE_MIN_LIMIT_4					PRU0_FD_WINDOW_SIZE_4		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_SD_SAMPLE_SIZE4							
R/W							
0h							

Table 4-1324. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU0_FD_EN_4	R/W	0h	
22	PRU0_FD_ONE_MAX_4	R/W1C	0h	
21:17	PRU0_FD_ONE_MAX_LIMIT_4	R/W	0h	
16	PRU0_FD_ONE_MIN_4	R/W1C	0h	
15:11	PRU0_FD_ONE_MIN_LIMIT_4	R/W	0h	
10:8	PRU0_FD_WINDOW_SIZE_4	R/W	0h	
7:0	PRU0_SD_SAMPLE_SIZE4	R/W	0h	

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4.2.2.154 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG5 Register

4.2.2.154.1 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG5 Register (Offset = 70h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1325. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6070h

Figure 4-640. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRU0_FD_ZERO_MAX_5	PRU0_FD_ZERO_MAX_LIMIT_5					PRU0_FD_ZERO_MIN_5
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ZERO_MIN_LIMIT_5					RESERVED		
R/W					NONE		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PRU0_SD_ACC_SEL5		RESERVED	PRU0_SD_CLK_INV5	PRU0_SD_CLK_SEL5	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1326. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU0_FD_ZERO_MAX_5	R/W1C	0h	
21:17	PRU0_FD_ZERO_MAX_LIMIT_5	R/W	0h	
16	PRU0_FD_ZERO_MIN_5	R/W1C	0h	
15:11	PRU0_FD_ZERO_MIN_LIMIT_5	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU0_SD_ACC_SEL5	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU0_SD_CLK_INV5	R/W	0h	
1:0	PRU0_SD_CLK_SEL5	R/W	0h	

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4.2.2.155 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG5 Register

4.2.2.155.1 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG5 Register (Offset = 74h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1327. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6074h

Figure 4-641. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG5 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PRU0_FD_EN_5</td><td>PRU0_FD_ONE_MAX_5</td><td colspan="5">PRU0_FD_ONE_MAX_LIMIT_5</td><td>PRU0_FD_ONE_MIN_5</td></tr>
<tr><td>R/W</td><td>R/W1C</td><td colspan="5">R/W</td><td>R/W1C</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU0_FD_ONE_MIN_LIMIT_5</td><td colspan="3">PRU0_FD_WINDOW_SIZE_5</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRU0_SD_SAMPLE_SIZE5</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 4-1328. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU0_FD_EN_5	R/W	0h	
22	PRU0_FD_ONE_MAX_5	R/W1C	0h	
21:17	PRU0_FD_ONE_MAX_LIMIT_5	R/W	0h	
16	PRU0_FD_ONE_MIN_5	R/W1C	0h	
15:11	PRU0_FD_ONE_MIN_LIMIT_5	R/W	0h	
10:8	PRU0_FD_WINDOW_SIZE_5	R/W	0h	
7:0	PRU0_SD_SAMPLE_SIZE5	R/W	0h	

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4.2.2.156 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG6 Register

4.2.2.156.1 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG6 Register (Offset = 78h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1329. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6078h

Figure 4-642. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_6	PRU0_FD_ZERO_MAX_LIMIT_6					PRU0_FD_ZERO_MIN_6
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h

15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_6					RESERVED		
R/W					NONE		
0h					0h		

7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL6		RESERVED	PRU0_SD_CLK_INV6	PRU0_SD_CLK_SEL6	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1330. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU0_FD_ZERO_MAX_6	R/W1C	0h	
21:17	PRU0_FD_ZERO_MAX_LIMIT_6	R/W	0h	
16	PRU0_FD_ZERO_MIN_6	R/W1C	0h	
15:11	PRU0_FD_ZERO_MIN_LIMIT_6	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU0_SD_ACC_SEL6	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU0_SD_CLK_INV6	R/W	0h	
1:0	PRU0_SD_CLK_SEL6	R/W	0h	

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4.2.2.157 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG6 Register

4.2.2.157.1 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG6 Register (Offset = 7Ch) [reset = 0h]

SD Register

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Table 4-1331. Instance Table

Instance Name	Physical Address
ICSSM0	4802 607Ch

Figure 4-643. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_FD_EN_6	PRU0_FD_ONE_MAX_6	PRU0_FD_ONE_MAX_LIMIT_6					PRU0_FD_ONE_MIN_6
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ONE_MIN_LIMIT_6					PRU0_FD_WINDOW_SIZE_6		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_SD_SAMPLE_SIZE6							
R/W							
0h							

Table 4-1332. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU0_FD_EN_6	R/W	0h	
22	PRU0_FD_ONE_MAX_6	R/W1C	0h	
21:17	PRU0_FD_ONE_MAX_LIMIT_6	R/W	0h	
16	PRU0_FD_ONE_MIN_6	R/W1C	0h	
15:11	PRU0_FD_ONE_MIN_LIMIT_6	R/W	0h	
10:8	PRU0_FD_WINDOW_SIZE_6	R/W	0h	
7:0	PRU0_SD_SAMPLE_SIZE6	R/W	0h	

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4.2.2.158 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG7 Register

4.2.2.158.1 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG7 Register (Offset = 80h) [reset = 0h]

SD Register

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Table 4-1333. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6080h

Figure 4-644. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	PRU0_FD_ZERO_MAX_7	PRU0_FD_ZERO_MAX_LIMIT_7					PRU0_FD_ZERO_MIN_7
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h

15	14	13	12	11	10	9	8
PRU0_FD_ZERO_MIN_LIMIT_7					RESERVED		
R/W					NONE		
0h					0h		

7	6	5	4	3	2	1	0
RESERVED		PRU0_SD_ACC_SEL7		RESERVED	PRU0_SD_CLK_INV7	PRU0_SD_CLK_SEL7	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1334. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU0_FD_ZERO_MAX_7	R/W1C	0h	
21:17	PRU0_FD_ZERO_MAX_LIMIT_7	R/W	0h	
16	PRU0_FD_ZERO_MIN_7	R/W1C	0h	
15:11	PRU0_FD_ZERO_MIN_LIMIT_7	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU0_SD_ACC_SEL7	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU0_SD_CLK_INV7	R/W	0h	
1:0	PRU0_SD_CLK_SEL7	R/W	0h	

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4.2.2.159 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG7 Register

4.2.2.159.1 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG7 Register (Offset = 84h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1335. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6084h

Figure 4-645. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_FD_EN_7	PRU0_FD_ONE_MAX_7	PRU0_FD_ONE_MAX_LIMIT_7					PRU0_FD_ONE_MIN_7
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ONE_MIN_LIMIT_7					PRU0_FD_WINDOW_SIZE_7		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_SD_SAMPLE_SIZE7							
R/W							
0h							

Table 4-1336. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU0_FD_EN_7	R/W	0h	
22	PRU0_FD_ONE_MAX_7	R/W1C	0h	
21:17	PRU0_FD_ONE_MAX_LIMIT_7	R/W	0h	
16	PRU0_FD_ONE_MIN_7	R/W1C	0h	
15:11	PRU0_FD_ONE_MIN_LIMIT_7	R/W	0h	
10:8	PRU0_FD_WINDOW_SIZE_7	R/W	0h	
7:0	PRU0_SD_SAMPLE_SIZE7	R/W	0h	

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4.2.2.160 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG8 Register

4.2.2.160.1 ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG8 Register (Offset = 88h) [reset = 0h]

SD Register

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Table 4-1337. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6088h

Figure 4-646. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRU0_FD_ZERO_MAX_8	PRU0_FD_ZERO_MAX_LIMIT_8					PRU0_FD_ZERO_MIN_8
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ZERO_MIN_LIMIT_8					RESERVED		
R/W					NONE		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PRU0_SD_ACC_SEL8		RESERVED	PRU0_SD_CLK_INV8	PRU0_SD_CLK_SEL8	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1338. ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU0_FD_ZERO_MAX_8	R/W1C	0h	
21:17	PRU0_FD_ZERO_MAX_LIMIT_8	R/W	0h	
16	PRU0_FD_ZERO_MIN_8	R/W1C	0h	
15:11	PRU0_FD_ZERO_MIN_LIMIT_8	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU0_SD_ACC_SEL8	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU0_SD_CLK_INV8	R/W	0h	
1:0	PRU0_SD_CLK_SEL8	R/W	0h	

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4.2.2.161 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG8 Register

4.2.2.161.1 ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG8 Register (Offset = 8Ch) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1339. Instance Table

Instance Name	Physical Address
ICSSM0	4802 608Ch

Figure 4-647. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_FD_EN_8	PRU0_FD_ONE_MAX_8	PRU0_FD_ONE_MAX_LIMIT_8					PRU0_FD_ONE_MIN_8
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_FD_ONE_MIN_LIMIT_8					PRU0_FD_WINDOW_SIZE_8		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_SD_SAMPLE_SIZE8							
R/W							
0h							

Table 4-1340. ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU0_FD_EN_8	R/W	0h	
22	PRU0_FD_ONE_MAX_8	R/W1C	0h	
21:17	PRU0_FD_ONE_MAX_LIMIT_8	R/W	0h	
16	PRU0_FD_ONE_MIN_8	R/W1C	0h	
15:11	PRU0_FD_ONE_MIN_LIMIT_8	R/W	0h	
10:8	PRU0_FD_WINDOW_SIZE_8	R/W	0h	
7:0	PRU0_SD_SAMPLE_SIZE8	R/W	0h	

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4.2.2.162 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_DIV_REG Register

4.2.2.162.1 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_DIV_REG Register (Offset = 90h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1341. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6090h

Figure 4-648. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_DIV_REG Name Register

31	30	29	28	27	26	25	24
PRU1_SD_MAN_REC_CLK_PERIOD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PRU1_SD_MAN_CLK_CAL_DONE
NONE							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_SD_MAN_STATUS	PRU1_SD_CH_SEL				PRU1_SD_MAN_NV_DATA_EN	PRU1_SD_MAN_EN	PRU1_SD_SHARE_EN
R	R/W				R/W	R/W	R/W
0h	0h				0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 4-1342. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_DIV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRU1_SD_MAN_REC_CLK_PERIOD	R	0h	
23:17	RESERVED	NONE	0h	Reserved
16	PRU1_SD_MAN_CLK_CAL_DONE	R	0h	
15	PRU1_SD_MAN_STATUS	R	0h	
14:11	PRU1_SD_CH_SEL	R/W	0h	
10	PRU1_SD_MAN_NV_DATA_EN	R/W	0h	
9	PRU1_SD_MAN_EN	R/W	0h	
8	PRU1_SD_SHARE_EN	R/W	0h	
7:0	RESERVED	NONE	0h	Reserved

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4.2.2.163 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG0 Register

4.2.2.163.1 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG0 Register (Offset = 94h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1343. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6094h

Figure 4-649. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG0 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>PRU1_FD_ZERO_MAX_0</td><td colspan="5">PRU1_FD_ZERO_MAX_LIMIT_0</td><td>PRU1_FD_ZERO_MIN_0</td></tr>
<tr><td>NONE</td><td>R/W1C</td><td colspan="5">R/W</td><td>R/W1C</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU1_FD_ZERO_MIN_LIMIT_0</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">PRU1_SD_ACC_SEL0</td><td>RESERVED</td><td>PRU1_SD_CLK_INV0</td><td colspan="2">PRU1_SD_CLK_SEL0</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R/W</td><td>NONE</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
</table>

Table 4-1344. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU1_FD_ZERO_MAX_0	R/W1C	0h	
21:17	PRU1_FD_ZERO_MAX_LIMIT_0	R/W	0h	
16	PRU1_FD_ZERO_MIN_0	R/W1C	0h	
15:11	PRU1_FD_ZERO_MIN_LIMIT_0	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU1_SD_ACC_SEL0	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU1_SD_CLK_INV0	R/W	0h	
1:0	PRU1_SD_CLK_SEL0	R/W	0h	

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4.2.2.164 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG0 Register

4.2.2.164.1 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG0 Register (Offset = 98h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1345. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6098h

Figure 4-650. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRU1_FD_EN_0	PRU1_FD_ONE_MAX_0	PRU1_FD_ONE_MAX_LIMIT_0					PRU1_FD_ONE_MIN_0
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_0					PRU1_FD_WINDOW_SIZE_0		
R/W					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE0							
R/W							
0h							

Table 4-1346. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU1_FD_EN_0	R/W	0h	
22	PRU1_FD_ONE_MAX_0	R/W1C	0h	
21:17	PRU1_FD_ONE_MAX_LIMIT_0	R/W	0h	
16	PRU1_FD_ONE_MIN_0	R/W1C	0h	
15:11	PRU1_FD_ONE_MIN_LIMIT_0	R/W	0h	
10:8	PRU1_FD_WINDOW_SIZE_0	R/W	0h	
7:0	PRU1_SD_SAMPLE_SIZE0	R/W	0h	

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4.2.2.165 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG1 Register

4.2.2.165.1 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG1 Register (Offset = 9Ch) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1347. Instance Table

Instance Name	Physical Address
ICSSM0	4802 609Ch

Figure 4-651. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_1	PRU1_FD_ZERO_MAX_LIMIT_1					PRU1_FD_ZERO_MIN_1
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h

15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_1					RESERVED		
R/W					NONE		
0h					0h		

7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL1		RESERVED	PRU1_SD_CLK_INV1	PRU1_SD_CLK_SEL1	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1348. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU1_FD_ZERO_MAX_1	R/W1C	0h	
21:17	PRU1_FD_ZERO_MAX_LIMIT_1	R/W	0h	
16	PRU1_FD_ZERO_MIN_1	R/W1C	0h	
15:11	PRU1_FD_ZERO_MIN_LIMIT_1	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU1_SD_ACC_SEL1	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU1_SD_CLK_INV1	R/W	0h	
1:0	PRU1_SD_CLK_SEL1	R/W	0h	

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4.2.2.166 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG1 Register

4.2.2.166.1 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG1 Register (Offset = A0h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1349. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60A0h

Figure 4-652. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG1 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PRU1_FD_EN_1</td><td>PRU1_FD_ONE_MAX_1</td><td colspan="5">PRU1_FD_ONE_MAX_LIMIT_1</td><td>PRU1_FD_ONE_MIN_1</td></tr>
<tr><td>R/W</td><td>R/W1C</td><td colspan="5">R/W</td><td>R/W1C</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU1_FD_ONE_MIN_LIMIT_1</td><td colspan="3">PRU1_FD_WINDOW_SIZE_1</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRU1_SD_SAMPLE_SIZE1</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 4-1350. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU1_FD_EN_1	R/W	0h	
22	PRU1_FD_ONE_MAX_1	R/W1C	0h	
21:17	PRU1_FD_ONE_MAX_LIMIT_1	R/W	0h	
16	PRU1_FD_ONE_MIN_1	R/W1C	0h	
15:11	PRU1_FD_ONE_MIN_LIMIT_1	R/W	0h	
10:8	PRU1_FD_WINDOW_SIZE_1	R/W	0h	
7:0	PRU1_SD_SAMPLE_SIZE1	R/W	0h	

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4.2.2.167 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG2 Register

4.2.2.167.1 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG2 Register (Offset = A4h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1351. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60A4h

Figure 4-653. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG2 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>RESERVED</td><td>PRU1_FD_ZERO_MAX_2</td><td colspan="5">PRU1_FD_ZERO_MAX_LIMIT_2</td><td>PRU1_FD_ZERO_MIN_2</td></tr>
<tr><td>NONE</td><td>R/W1C</td><td colspan="5">R/W</td><td>R/W1C</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU1_FD_ZERO_MIN_LIMIT_2</td><td colspan="3">RESERVED</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">NONE</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">PRU1_SD_ACC_SEL2</td><td>RESERVED</td><td>PRU1_SD_CLK_INV2</td><td colspan="2">PRU1_SD_CLK_SEL2</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R/W</td><td>NONE</td><td>R/W</td><td colspan="2">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td></tr>
</table>

Table 4-1352. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU1_FD_ZERO_MAX_2	R/W1C	0h	
21:17	PRU1_FD_ZERO_MAX_LIMIT_2	R/W	0h	
16	PRU1_FD_ZERO_MIN_2	R/W1C	0h	
15:11	PRU1_FD_ZERO_MIN_LIMIT_2	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU1_SD_ACC_SEL2	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU1_SD_CLK_INV2	R/W	0h	
1:0	PRU1_SD_CLK_SEL2	R/W	0h	

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4.2.2.168 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG2 Register

4.2.2.168.1 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG2 Register (Offset = A8h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1353. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60A8h

Figure 4-654. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_FD_EN_2	PRU1_FD_ONE_MAX_2	PRU1_FD_ONE_MAX_LIMIT_2					PRU1_FD_ONE_MIN_2
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_FD_ONE_MIN_LIMIT_2					PRU1_FD_WINDOW_SIZE_2		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_SD_SAMPLE_SIZE2							
R/W							
0h							

Table 4-1354. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU1_FD_EN_2	R/W	0h	
22	PRU1_FD_ONE_MAX_2	R/W1C	0h	
21:17	PRU1_FD_ONE_MAX_LIMIT_2	R/W	0h	
16	PRU1_FD_ONE_MIN_2	R/W1C	0h	
15:11	PRU1_FD_ONE_MIN_LIMIT_2	R/W	0h	
10:8	PRU1_FD_WINDOW_SIZE_2	R/W	0h	
7:0	PRU1_SD_SAMPLE_SIZE2	R/W	0h	

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4.2.2.169 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG3 Register

4.2.2.169.1 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG3 Register (Offset = ACh) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1355. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60ACh

Figure 4-655. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_3	PRU1_FD_ZERO_MAX_LIMIT_3					PRU1_FD_ZERO_MIN_3
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_3					RESERVED		
R/W					NONE		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL3		RESERVED	PRU1_SD_CLK_INV3	PRU1_SD_CLK_SEL3	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1356. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU1_FD_ZERO_MAX_3	R/W1C	0h	
21:17	PRU1_FD_ZERO_MAX_LIMIT_3	R/W	0h	
16	PRU1_FD_ZERO_MIN_3	R/W1C	0h	
15:11	PRU1_FD_ZERO_MIN_LIMIT_3	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU1_SD_ACC_SEL3	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU1_SD_CLK_INV3	R/W	0h	
1:0	PRU1_SD_CLK_SEL3	R/W	0h	

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4.2.2.170 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG3 Register

4.2.2.170.1 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG3 Register (Offset = B0h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1357. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60B0h

Figure 4-656. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_FD_EN_3	PRU1_FD_ONE_MAX_3	PRU1_FD_ONE_MAX_LIMIT_3					PRU1_FD_ONE_MIN_3
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_FD_ONE_MIN_LIMIT_3					PRU1_FD_WINDOW_SIZE_3		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_SD_SAMPLE_SIZE3							
R/W							
0h							

Table 4-1358. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU1_FD_EN_3	R/W	0h	
22	PRU1_FD_ONE_MAX_3	R/W1C	0h	
21:17	PRU1_FD_ONE_MAX_LIMIT_3	R/W	0h	
16	PRU1_FD_ONE_MIN_3	R/W1C	0h	
15:11	PRU1_FD_ONE_MIN_LIMIT_3	R/W	0h	
10:8	PRU1_FD_WINDOW_SIZE_3	R/W	0h	
7:0	PRU1_SD_SAMPLE_SIZE3	R/W	0h	

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4.2.2.171 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG4 Register

4.2.2.171.1 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG4 Register (Offset = B4h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1359. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60B4h

Figure 4-657. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRU1_FD_ZERO_MAX_4	PRU1_FD_ZERO_MAX_LIMIT_4					PRU1_FD_ZERO_MIN_4
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_FD_ZERO_MIN_LIMIT_4					RESERVED		
R/W					NONE		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PRU1_SD_ACC_SEL4		RESERVED	PRU1_SD_CLK_INV4	PRU1_SD_CLK_SEL4	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1360. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU1_FD_ZERO_MAX_4	R/W1C	0h	
21:17	PRU1_FD_ZERO_MAX_LIMIT_4	R/W	0h	
16	PRU1_FD_ZERO_MIN_4	R/W1C	0h	
15:11	PRU1_FD_ZERO_MIN_LIMIT_4	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU1_SD_ACC_SEL4	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU1_SD_CLK_INV4	R/W	0h	
1:0	PRU1_SD_CLK_SEL4	R/W	0h	

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4.2.2.172 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG4 Register

4.2.2.172.1 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG4 Register (Offset = B8h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1361. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60B8h

Figure 4-658. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG4 Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>PRU1_FD_EN_4</td><td>PRU1_FD_ONE_MAX_4</td><td colspan="5">PRU1_FD_ONE_MAX_LIMIT_4</td><td>PRU1_FD_ONE_MIN_4</td></tr>
<tr><td>R/W</td><td>R/W1C</td><td colspan="5">R/W</td><td>R/W1C</td></tr>
<tr><td>0h</td><td>0h</td><td colspan="5">0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">PRU1_FD_ONE_MIN_LIMIT_4</td><td colspan="3">PRU1_FD_WINDOW_SIZE_4</td></tr>
<tr><td colspan="5">R/W</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PRU1_SD_SAMPLE_SIZE4</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 4-1362. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU1_FD_EN_4	R/W	0h	
22	PRU1_FD_ONE_MAX_4	R/W1C	0h	
21:17	PRU1_FD_ONE_MAX_LIMIT_4	R/W	0h	
16	PRU1_FD_ONE_MIN_4	R/W1C	0h	
15:11	PRU1_FD_ONE_MIN_LIMIT_4	R/W	0h	
10:8	PRU1_FD_WINDOW_SIZE_4	R/W	0h	
7:0	PRU1_SD_SAMPLE_SIZE4	R/W	0h	

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4.2.2.173 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG5 Register

4.2.2.173.1 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG5 Register (Offset = BCh) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1363. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60BCh

Figure 4-659. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRU1_FD_ZERO_MAX_5	PRU1_FD_ZERO_MAX_LIMIT_5					PRU1_FD_ZERO_MIN_5
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_FD_ZERO_MIN_LIMIT_5					RESERVED		
R/W					NONE		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PRU1_SD_ACC_SEL5		RESERVED	PRU1_SD_CLK_INV5	PRU1_SD_CLK_SEL5	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1364. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU1_FD_ZERO_MAX_5	R/W1C	0h	
21:17	PRU1_FD_ZERO_MAX_LIMIT_5	R/W	0h	
16	PRU1_FD_ZERO_MIN_5	R/W1C	0h	
15:11	PRU1_FD_ZERO_MIN_LIMIT_5	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU1_SD_ACC_SEL5	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU1_SD_CLK_INV5	R/W	0h	
1:0	PRU1_SD_CLK_SEL5	R/W	0h	

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4.2.2.174 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG5 Register

4.2.2.174.1 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG5 Register (Offset = C0h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1365. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60C0h

Figure 4-660. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRU1_FD_EN_5	PRU1_FD_ONE_MAX_5	PRU1_FD_ONE_MAX_LIMIT_5					PRU1_FD_ONE_MIN_5
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_5					PRU1_FD_WINDOW_SIZE_5		
R/W					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE5							
R/W							
0h							

Table 4-1366. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU1_FD_EN_5	R/W	0h	
22	PRU1_FD_ONE_MAX_5	R/W1C	0h	
21:17	PRU1_FD_ONE_MAX_LIMIT_5	R/W	0h	
16	PRU1_FD_ONE_MIN_5	R/W1C	0h	
15:11	PRU1_FD_ONE_MIN_LIMIT_5	R/W	0h	
10:8	PRU1_FD_WINDOW_SIZE_5	R/W	0h	
7:0	PRU1_SD_SAMPLE_SIZE5	R/W	0h	

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4.2.2.175 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG6 Register

4.2.2.175.1 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG6 Register (Offset = C4h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1367. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60C4h

Figure 4-661. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_6	PRU1_FD_ZERO_MAX_LIMIT_6					PRU1_FD_ZERO_MIN_6
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h

15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_6					RESERVED		
R/W					NONE		
0h					0h		

7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL6		RESERVED	PRU1_SD_CLK_INV6	PRU1_SD_CLK_SEL6	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1368. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU1_FD_ZERO_MAX_6	R/W1C	0h	
21:17	PRU1_FD_ZERO_MAX_LIMIT_6	R/W	0h	
16	PRU1_FD_ZERO_MIN_6	R/W1C	0h	
15:11	PRU1_FD_ZERO_MIN_LIMIT_6	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU1_SD_ACC_SEL6	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU1_SD_CLK_INV6	R/W	0h	
1:0	PRU1_SD_CLK_SEL6	R/W	0h	

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4.2.2.176 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG6 Register

4.2.2.176.1 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG6 Register (Offset = C8h) [reset = 0h]

SD Register

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Table 4-1369. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60C8h

Figure 4-662. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_FD_EN_6	PRU1_FD_ONE_MAX_6	PRU1_FD_ONE_MAX_LIMIT_6					PRU1_FD_ONE_MIN_6
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_FD_ONE_MIN_LIMIT_6					PRU1_FD_WINDOW_SIZE_6		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_SD_SAMPLE_SIZE6							
R/W							
0h							

Table 4-1370. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU1_FD_EN_6	R/W	0h	
22	PRU1_FD_ONE_MAX_6	R/W1C	0h	
21:17	PRU1_FD_ONE_MAX_LIMIT_6	R/W	0h	
16	PRU1_FD_ONE_MIN_6	R/W1C	0h	
15:11	PRU1_FD_ONE_MIN_LIMIT_6	R/W	0h	
10:8	PRU1_FD_WINDOW_SIZE_6	R/W	0h	
7:0	PRU1_SD_SAMPLE_SIZE6	R/W	0h	

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4.2.2.177 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG7 Register

4.2.2.177.1 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG7 Register (Offset = CCh) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1371. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60CCh

Figure 4-663. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	PRU1_FD_ZERO_MAX_7	PRU1_FD_ZERO_MAX_LIMIT_7					PRU1_FD_ZERO_MIN_7
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	14	13	12	11	10	9	8
PRU1_FD_ZERO_MIN_LIMIT_7					RESERVED		
R/W					NONE		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED		PRU1_SD_ACC_SEL7		RESERVED	PRU1_SD_CLK_INV7	PRU1_SD_CLK_SEL7	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1372. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU1_FD_ZERO_MAX_7	R/W1C	0h	
21:17	PRU1_FD_ZERO_MAX_LIMIT_7	R/W	0h	
16	PRU1_FD_ZERO_MIN_7	R/W1C	0h	
15:11	PRU1_FD_ZERO_MIN_LIMIT_7	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU1_SD_ACC_SEL7	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU1_SD_CLK_INV7	R/W	0h	
1:0	PRU1_SD_CLK_SEL7	R/W	0h	

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4.2.2.178 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG7 Register

4.2.2.178.1 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG7 Register (Offset = D0h) [reset = 0h]

SD Register

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Table 4-1373. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60D0h

Figure 4-664. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_FD_EN_7	PRU1_FD_ONE_MAX_7	PRU1_FD_ONE_MAX_LIMIT_7					PRU1_FD_ONE_MIN_7
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_FD_ONE_MIN_LIMIT_7					PRU1_FD_WINDOW_SIZE_7		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_SD_SAMPLE_SIZE7							
R/W							
0h							

Table 4-1374. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU1_FD_EN_7	R/W	0h	
22	PRU1_FD_ONE_MAX_7	R/W1C	0h	
21:17	PRU1_FD_ONE_MAX_LIMIT_7	R/W	0h	
16	PRU1_FD_ONE_MIN_7	R/W1C	0h	
15:11	PRU1_FD_ONE_MIN_LIMIT_7	R/W	0h	
10:8	PRU1_FD_WINDOW_SIZE_7	R/W	0h	
7:0	PRU1_SD_SAMPLE_SIZE7	R/W	0h	

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4.2.2.179 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG8 Register

4.2.2.179.1 ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG8 Register (Offset = D4h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1375. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60D4h

Figure 4-665. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRU1_FD_ZERO_MAX_8	PRU1_FD_ZERO_MAX_LIMIT_8					PRU1_FD_ZERO_MIN_8
NONE	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_FD_ZERO_MIN_LIMIT_8					RESERVED		
R/W					NONE		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		PRU1_SD_ACC_SEL8		RESERVED	PRU1_SD_CLK_INV8	PRU1_SD_CLK_SEL8	
NONE		R/W		NONE	R/W	R/W	
0h		0h		0h	0h	0h	

Table 4-1376. ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22	PRU1_FD_ZERO_MAX_8	R/W1C	0h	
21:17	PRU1_FD_ZERO_MAX_LIMIT_8	R/W	0h	
16	PRU1_FD_ZERO_MIN_8	R/W1C	0h	
15:11	PRU1_FD_ZERO_MIN_LIMIT_8	R/W	0h	
10:6	RESERVED	NONE	0h	Reserved
5:4	PRU1_SD_ACC_SEL8	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	PRU1_SD_CLK_INV8	R/W	0h	
1:0	PRU1_SD_CLK_SEL8	R/W	0h	

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4.2.2.180 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG8 Register

4.2.2.180.1 ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG8 Register (Offset = D8h) [reset = 0h]

SD Register

Return to Summary Table

Table 4-1377. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60D8h

Figure 4-666. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
PRU1_FD_EN_8	PRU1_FD_ONE_MAX_8	PRU1_FD_ONE_MAX_LIMIT_8					PRU1_FD_ONE_MIN_8
R/W	R/W1C	R/W					R/W1C
0h	0h	0h					0h
15	14	13	12	11	10	9	8
PRU1_FD_ONE_MIN_LIMIT_8					PRU1_FD_WINDOW_SIZE_8		
R/W					R/W		
0h					0h		
7	6	5	4	3	2	1	0
PRU1_SD_SAMPLE_SIZE8							
R/W							
0h							

Table 4-1378. ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23	PRU1_FD_EN_8	R/W	0h	
22	PRU1_FD_ONE_MAX_8	R/W1C	0h	
21:17	PRU1_FD_ONE_MAX_LIMIT_8	R/W	0h	
16	PRU1_FD_ONE_MIN_8	R/W1C	0h	
15:11	PRU1_FD_ONE_MIN_LIMIT_8	R/W	0h	
10:8	PRU1_FD_WINDOW_SIZE_8	R/W	0h	
7:0	PRU1_SD_SAMPLE_SIZE8	R/W	0h	

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4.2.2.181 ICSSM_PR1_CFG_SLV_PRU0_ED_RX_CFG_REG Register

4.2.2.181.1 ICSSM_PR1_CFG_SLV_PRU0_ED_RX_CFG_REG Register (Offset = E0h) [reset = Fh]

ED Register

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Table 4-1379. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60E0h

Figure 4-667. ICSSM_PR1_CFG_SLV_PRU0_ED_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24
PRU0_ED_RX_DIV_FACTOR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_ED_RX_DIV_FACTOR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_ED_RX_DIV_FACTOR_FRAC	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRU0_ED_RX_CLK_SEL	PRU0_ED_RX_SB_POL	PRU0_ED_RX_SAMPLE_SIZE		
NONE			R/W	R/W	R/W		
0h			0h	1h	7h		

Table 4-1380. ICSSM_PR1_CFG_SLV_PRU0_ED_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PRU0_ED_RX_DIV_FACTOR	R/W	0h	
15	PRU0_ED_RX_DIV_FACTOR_FRAC	R/W	0h	
14:5	RESERVED	NONE	0h	Reserved
4	PRU0_ED_RX_CLK_SEL	R/W	0h	
3	PRU0_ED_RX_SB_POL	R/W	1h	
2:0	PRU0_ED_RX_SAMPLE_SIZE	R/W	7h	

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4.2.2.182 ICSSM_PR1_CFG_SLV_PRU0_ED_TX_CFG_REG Register

4.2.2.182.1 ICSSM_PR1_CFG_SLV_PRU0_ED_TX_CFG_REG Register (Offset = E4h) [reset = 700h]

Register

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Table 4-1381. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60E4h

Figure 4-668. ICSSM_PR1_CFG_SLV_PRU0_ED_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_DIV_FACTOR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_ED_TX_DIV_FACTOR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_ED_TX_DIV_FACTOR_FRAC	RESERVED			PRU0_ENDAT_SHARE_EN	PRU0_ENDAT2_CLK_SYNC	PRU0_ENDAT1_CLK_SYNC	PRU0_ENDAT0_CLK_SYNC
R/W	NONE			R/W	R	R	R
0h	0h			0h	1h	1h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_ED_BUSY_2	PRU0_ED_BUSY_1	PRU0_ED_BUSY_0	PRU0_ED_TX_CLK_SEL	RESERVED			
R	R	R	R/W	NONE			
0h	0h	0h	0h	0h			

Table 4-1382. ICSSM_PR1_CFG_SLV_PRU0_ED_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PRU0_ED_TX_DIV_FACTOR	R/W	0h	
15	PRU0_ED_TX_DIV_FACTOR_FRAC	R/W	0h	
14:12	RESERVED	NONE	0h	Reserved
11	PRU0_ENDAT_SHARE_EN	R/W	0h	
10	PRU0_ENDAT2_CLK_SYNC	R	1h	
9	PRU0_ENDAT1_CLK_SYNC	R	1h	
8	PRU0_ENDAT0_CLK_SYNC	R	1h	
7	PRU0_ED_BUSY_2	R	0h	
6	PRU0_ED_BUSY_1	R	0h	
5	PRU0_ED_BUSY_0	R	0h	
4	PRU0_ED_TX_CLK_SEL	R/W	0h	
3:0	RESERVED	NONE	0h	Reserved

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4.2.2.183 ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG0_REG Register

4.2.2.183.1 ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG0_REG Register (Offset = E8h) [reset = 0h]

ED Register

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Table 4-1383. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60E8h

Figure 4-669. ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG0_REG Name Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_FIFO_SWAP_BITS0	PRU0_ED_SW_CLK_OUT0	PRU0_ED_CLK_OUT_OVR_EN0	PRU0_ED_RX_SNOOP0	PRU0_ED_RX_FRAME_SIZE0			
R/W	R/W	R/W	R	R/W			
0h	0h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_ED_RX_FRAME_SIZE0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_ED_TX_FRAME_SIZE0					PRU0_ED_TX_WDLY0		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_ED_TX_WDLY0							
R/W							
0h							

Table 4-1384. ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU0_ED_TX_FIFO_SWAP_BITS0	R/W	0h	
30	PRU0_ED_SW_CLK_OUT0	R/W	0h	
29	PRU0_ED_CLK_OUT_OVR_EN0	R/W	0h	
28	PRU0_ED_RX_SNOOP0	R	0h	
27:16	PRU0_ED_RX_FRAME_SIZE0	R/W	0h	
15:11	PRU0_ED_TX_FRAME_SIZE0	R/W	0h	
10:0	PRU0_ED_TX_WDLY0	R/W	0h	

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4.2.2.184 ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG1_REG Register

4.2.2.184.1 ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG1_REG Register (Offset = ECh) [reset = 0h]

ED Register

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Table 4-1385. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60ECh

Figure 4-670. ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG1_REG Name Register

31	30	29	28	27	26	25	24
PRU0_ED_RX_EN_COUNTER0							
R/W							
0h							
23	22	21	20	19	18	17	16
PRU0_ED_RX_EN_COUNTER0							
R/W							
0h							
15	14	13	12	11	10	9	8
PRU0_ED_TST_DELAY_COUNTER0							
R/W							
0h							
7	6	5	4	3	2	1	0
PRU0_ED_TST_DELAY_COUNTER0							
R/W							
0h							

Table 4-1386. ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PRU0_ED_RX_EN_COUNTER0	R/W	0h	
15:0	PRU0_ED_TST_DELAY_COUNTER0	R/W	0h	

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4.2.2.185 ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG0_REG Register

4.2.2.185.1 ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG0_REG Register (Offset = F0h) [reset = 0h]

ED Register

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Table 4-1387. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60F0h

Figure 4-671. ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG0_REG Name Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_FIFO_SWAP_BITS1	PRU0_ED_SW_CLK_OUT1	PRU0_ED_CLK_OUT_OVR_EN1	PRU0_ED_RX_SNOOP1	PRU0_ED_RX_FRAME_SIZE1			
R/W	R/W	R/W	R	R/W			
0h	0h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_ED_RX_FRAME_SIZE1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_ED_TX_FRAME_SIZE1					PRU0_ED_TX_WDLY1		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_ED_TX_WDLY1							
R/W							
0h							

Table 4-1388. ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU0_ED_TX_FIFO_SWAP_BITS1	R/W	0h	
30	PRU0_ED_SW_CLK_OUT1	R/W	0h	
29	PRU0_ED_CLK_OUT_OVR_EN1	R/W	0h	
28	PRU0_ED_RX_SNOOP1	R	0h	
27:16	PRU0_ED_RX_FRAME_SIZE1	R/W	0h	
15:11	PRU0_ED_TX_FRAME_SIZE1	R/W	0h	
10:0	PRU0_ED_TX_WDLY1	R/W	0h	

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4.2.2.186 ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG1_REG Register

4.2.2.186.1 ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG1_REG Register (Offset = F4h) [reset = 0h]

ED Register

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Table 4-1389. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60F4h

Figure 4-672. ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG1_REG Name Register

31	30	29	28	27	26	25	24
PRU0_ED_RX_EN_COUNTER1							
R/W							
0h							
23	22	21	20	19	18	17	16
PRU0_ED_RX_EN_COUNTER1							
R/W							
0h							
15	14	13	12	11	10	9	8
PRU0_ED_TST_DELAY_COUNTER1							
R/W							
0h							
7	6	5	4	3	2	1	0
PRU0_ED_TST_DELAY_COUNTER1							
R/W							
0h							

Table 4-1390. ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PRU0_ED_RX_EN_COUNTER1	R/W	0h	
15:0	PRU0_ED_TST_DELAY_COUNTER1	R/W	0h	

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4.2.2.187 ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG0_REG Register

4.2.2.187.1 ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG0_REG Register (Offset = F8h) [reset = 0h]

ED Register

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Table 4-1391. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60F8h

Figure 4-673. ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG0_REG Name Register

31	30	29	28	27	26	25	24
PRU0_ED_TX_FIFO_SWAP_BITS2	PRU0_ED_SW_CLK_OUT2	PRU0_ED_CLK_OUT_OVR_EN2	PRU0_ED_RX_SNOOP2	PRU0_ED_RX_FRAME_SIZE2			
R/W	R/W	R/W	R	R/W			
0h	0h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_ED_RX_FRAME_SIZE2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_ED_TX_FRAME_SIZE2					PRU0_ED_TX_WDLY2		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_ED_TX_WDLY2							
R/W							
0h							

Table 4-1392. ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU0_ED_TX_FIFO_SWAP_BITS2	R/W	0h	
30	PRU0_ED_SW_CLK_OUT2	R/W	0h	
29	PRU0_ED_CLK_OUT_OVR_EN2	R/W	0h	
28	PRU0_ED_RX_SNOOP2	R	0h	
27:16	PRU0_ED_RX_FRAME_SIZE2	R/W	0h	
15:11	PRU0_ED_TX_FRAME_SIZE2	R/W	0h	
10:0	PRU0_ED_TX_WDLY2	R/W	0h	

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4.2.2.188 ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG1_REG Register

4.2.2.188.1 ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG1_REG Register (Offset = FCh) [reset = 0h]

ED Register

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Table 4-1393. Instance Table

Instance Name	Physical Address
ICSSM0	4802 60FCh

Figure 4-674. ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG1_REG Name Register

31	30	29	28	27	26	25	24
PRU0_ED_RX_EN_COUNTER2							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU0_ED_RX_EN_COUNTER2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU0_ED_TST_DELAY_COUNTER2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU0_ED_TST_DELAY_COUNTER2							
R/W							
0h							

Table 4-1394. ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PRU0_ED_RX_EN_COUNTER2	R/W	0h	
15:0	PRU0_ED_TST_DELAY_COUNTER2	R/W	0h	

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4.2.2.189 ICSSM_PR1_CFG_SLV_PRU1_ED_RX_CFG_REG Register

4.2.2.189.1 ICSSM_PR1_CFG_SLV_PRU1_ED_RX_CFG_REG Register (Offset = 100h) [reset = Fh]

ED Register

Return to Summary Table

Table 4-1395. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6100h

Figure 4-675. ICSSM_PR1_CFG_SLV_PRU1_ED_RX_CFG_REG Name Register

31	30	29	28	27	26	25	24
PRU1_ED_RX_DIV_FACTOR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_ED_RX_DIV_FACTOR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_ED_RX_DIV_FACTOR_FRAC	RESERVED						
R/W	NONE						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRU1_ED_RX_CLK_SEL	PRU1_ED_RX_SB_POL	PRU1_ED_RX_SAMPLE_SIZE		
NONE			R/W	R/W	R/W		
0h			0h	1h	7h		

Table 4-1396. ICSSM_PR1_CFG_SLV_PRU1_ED_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PRU1_ED_RX_DIV_FACTOR	R/W	0h	
15	PRU1_ED_RX_DIV_FACTOR_FRAC	R/W	0h	
14:5	RESERVED	NONE	0h	Reserved
4	PRU1_ED_RX_CLK_SEL	R/W	0h	
3	PRU1_ED_RX_SB_POL	R/W	1h	
2:0	PRU1_ED_RX_SAMPLE_SIZE	R/W	7h	

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4.2.2.190 ICSSM_PR1_CFG_SLV_PRU1_ED_TX_CFG_REG Register

4.2.2.190.1 ICSSM_PR1_CFG_SLV_PRU1_ED_TX_CFG_REG Register (Offset = 104h) [reset = 700h]

ED Register

Return to Summary Table

Table 4-1397. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6104h

Figure 4-676. ICSSM_PR1_CFG_SLV_PRU1_ED_TX_CFG_REG Name Register

31	30	29	28	27	26	25	24
PRU1_ED_TX_DIV_FACTOR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_ED_TX_DIV_FACTOR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_ED_TX_DIV_FACTOR_FRAC	RESERVED			PRU1_ENDAT_SHARE_EN	PRU1_ENDAT2_CLK_SYNC	PRU1_ENDAT1_CLK_SYNC	PRU1_ENDAT0_CLK_SYNC
R/W	NONE			R/W	R	R	R
0h	0h			0h	1h	1h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_ED_BUSY_2	PRU1_ED_BUSY_1	PRU1_ED_BUSY_0	PRU1_ED_TX_CLK_SEL	RESERVED			
R	R	R	R/W	NONE			
0h	0h	0h	0h	0h			

Table 4-1398. ICSSM_PR1_CFG_SLV_PRU1_ED_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PRU1_ED_TX_DIV_FACTOR	R/W	0h	
15	PRU1_ED_TX_DIV_FACTOR_FRAC	R/W	0h	
14:12	RESERVED	NONE	0h	Reserved
11	PRU1_ENDAT_SHARE_EN	R/W	0h	
10	PRU1_ENDAT2_CLK_SYNC	R	1h	
9	PRU1_ENDAT1_CLK_SYNC	R	1h	
8	PRU1_ENDAT0_CLK_SYNC	R	1h	
7	PRU1_ED_BUSY_2	R	0h	
6	PRU1_ED_BUSY_1	R	0h	
5	PRU1_ED_BUSY_0	R	0h	
4	PRU1_ED_TX_CLK_SEL	R/W	0h	
3:0	RESERVED	NONE	0h	Reserved

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4.2.2.191 ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG0_REG Register

4.2.2.191.1 ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG0_REG Register (Offset = 108h) [reset = 0h]

ED Register

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Table 4-1399. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6108h

Figure 4-677. ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG0_REG Name Register

31	30	29	28	27	26	25	24
PRU1_ED_TX_FIFO_SWAP_BITS0	PRU1_ED_SW_CLK_OUT0	PRU1_ED_CLK_OUT_OVR_EN0	PRU1_ED_RX_SNOOP0	PRU1_ED_RX_FRAME_SIZE0			
R/W	R/W	R/W	R	R/W			
0h	0h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_ED_RX_FRAME_SIZE0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_ED_TX_FRAME_SIZE0					PRU1_ED_TX_WDLY0		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_ED_TX_WDLY0							
R/W							
0h							

Table 4-1400. ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU1_ED_TX_FIFO_SWAP_BITS0	R/W	0h	
30	PRU1_ED_SW_CLK_OUT0	R/W	0h	
29	PRU1_ED_CLK_OUT_OVR_EN0	R/W	0h	
28	PRU1_ED_RX_SNOOP0	R	0h	
27:16	PRU1_ED_RX_FRAME_SIZE0	R/W	0h	
15:11	PRU1_ED_TX_FRAME_SIZE0	R/W	0h	
10:0	PRU1_ED_TX_WDLY0	R/W	0h	

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4.2.2.192 ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG1_REG Register

4.2.2.192.1 ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG1_REG Register (Offset = 10Ch) [reset = 0h]

ED Register

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Table 4-1401. Instance Table

Instance Name	Physical Address
ICSSM0	4802 610Ch

Figure 4-678. ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG1_REG Name Register

31	30	29	28	27	26	25	24
PRU1_ED_RX_EN_COUNTER0							
R/W							
0h							
23	22	21	20	19	18	17	16
PRU1_ED_RX_EN_COUNTER0							
R/W							
0h							
15	14	13	12	11	10	9	8
PRU1_ED_TST_DELAY_COUNTER0							
R/W							
0h							
7	6	5	4	3	2	1	0
PRU1_ED_TST_DELAY_COUNTER0							
R/W							
0h							

Table 4-1402. ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PRU1_ED_RX_EN_COUNTER0	R/W	0h	
15:0	PRU1_ED_TST_DELAY_COUNTER0	R/W	0h	

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4.2.2.193 ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG0_REG Register

4.2.2.193.1 ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG0_REG Register (Offset = 110h) [reset = 0h]

ED Register

Return to Summary Table

Table 4-1403. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6110h

Figure 4-679. ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG0_REG Name Register

31	30	29	28	27	26	25	24
PRU1_ED_TX_FIFO_SWAP_BITS1	PRU1_ED_SW_CLK_OUT1	PRU1_ED_CLK_OUT_OVR_EN1	PRU1_ED_RX_SNOOP1	PRU1_ED_RX_FRAME_SIZE1			
R/W	R/W	R/W	R	R/W			
0h	0h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_ED_RX_FRAME_SIZE1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_ED_TX_FRAME_SIZE1					PRU1_ED_TX_WDLY1		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_ED_TX_WDLY1							
R/W							
0h							

Table 4-1404. ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU1_ED_TX_FIFO_SWAP_BITS1	R/W	0h	
30	PRU1_ED_SW_CLK_OUT1	R/W	0h	
29	PRU1_ED_CLK_OUT_OVR_EN1	R/W	0h	
28	PRU1_ED_RX_SNOOP1	R	0h	
27:16	PRU1_ED_RX_FRAME_SIZE1	R/W	0h	
15:11	PRU1_ED_TX_FRAME_SIZE1	R/W	0h	
10:0	PRU1_ED_TX_WDLY1	R/W	0h	

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4.2.2.194 ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG1_REG Register

4.2.2.194.1 ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG1_REG Register (Offset = 114h) [reset = 0h]

ED Register

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Table 4-1405. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6114h

Figure 4-680. ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG1_REG Name Register

31	30	29	28	27	26	25	24
PRU1_ED_RX_EN_COUNTER1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_ED_RX_EN_COUNTER1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_ED_TST_DELAY_COUNTER1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_ED_TST_DELAY_COUNTER1							
R/W							
0h							

Table 4-1406. ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PRU1_ED_RX_EN_COUNTER1	R/W	0h	
15:0	PRU1_ED_TST_DELAY_COUNTER1	R/W	0h	

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4.2.2.195 ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG0_REG Register

4.2.2.195.1 ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG0_REG Register (Offset = 118h) [reset = 0h]

ED Register

Return to Summary Table

Table 4-1407. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6118h

Figure 4-681. ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG0_REG Name Register

31	30	29	28	27	26	25	24
PRU1_ED_TX_FIFO_SWAP_BITS2	PRU1_ED_SW_CLK_OUT2	PRU1_ED_CLK_OUT_OVR_EN2	PRU1_ED_RX_SNOOP2	PRU1_ED_RX_FRAME_SIZE2			
R/W	R/W	R/W	R	R/W			
0h	0h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRU1_ED_RX_FRAME_SIZE2							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRU1_ED_TX_FRAME_SIZE2					PRU1_ED_TX_WDLY2		
R/W					R/W		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRU1_ED_TX_WDLY2							
R/W							
0h							

Table 4-1408. ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRU1_ED_TX_FIFO_SWAP_BITS2	R/W	0h	
30	PRU1_ED_SW_CLK_OUT2	R/W	0h	
29	PRU1_ED_CLK_OUT_OVR_EN2	R/W	0h	
28	PRU1_ED_RX_SNOOP2	R	0h	
27:16	PRU1_ED_RX_FRAME_SIZE2	R/W	0h	
15:11	PRU1_ED_TX_FRAME_SIZE2	R/W	0h	
10:0	PRU1_ED_TX_WDLY2	R/W	0h	

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4.2.2.196 ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG1_REG Register

4.2.2.196.1 ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG1_REG Register (Offset = 11Ch) [reset = 0h]

ED Register

Return to Summary Table

Table 4-1409. Instance Table

Instance Name	Physical Address
ICSSM0	4802 611Ch

Figure 4-682. ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG1_REG Name Register

31	30	29	28	27	26	25	24
PRU1_ED_RX_EN_COUNTER2							
R/W							
0h							
23	22	21	20	19	18	17	16
PRU1_ED_RX_EN_COUNTER2							
R/W							
0h							
15	14	13	12	11	10	9	8
PRU1_ED_TST_DELAY_COUNTER2							
R/W							
0h							
7	6	5	4	3	2	1	0
PRU1_ED_TST_DELAY_COUNTER2							
R/W							
0h							

Table 4-1410. ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PRU1_ED_RX_EN_COUNTER2	R/W	0h	
15:0	PRU1_ED_TST_DELAY_COUNTER2	R/W	0h	

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4.2.2.197 ICSSM_PR1_CFG_SLV_RTU0_POKE_EN0_REG Register

4.2.2.197.1 ICSSM_PR1_CFG_SLV_RTU0_POKE_EN0_REG Register (Offset = 124h) [reset = 0h]

RTU PRU Poke Enable

Return to Summary Table

Table 4-1411. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6124h

Figure 4-683. ICSSM_PR1_CFG_SLV_RTU0_POKE_EN0_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1412. ICSSM_PR1_CFG_SLV_RTU0_POKE_EN0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.198 ICSSM_PR1_CFG_SLV_RTU1_POKE_EN0_REG Register

4.2.2.198.1 ICSSM_PR1_CFG_SLV_RTU1_POKE_EN0_REG Register (Offset = 12Ch) [reset = 0h]

RTU PRU Poke Enable

Return to Summary Table

Table 4-1413. Instance Table

Instance Name	Physical Address
ICSSM0	4802 612Ch

Figure 4-684. ICSSM_PR1_CFG_SLV_RTU1_POKE_EN0_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1414. ICSSM_PR1_CFG_SLV_RTU1_POKE_EN0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.199 ICSSM_PR1_CFG_SLV_PWM0 Register

4.2.2.199.1 ICSSM_PR1_CFG_SLV_PWM0 Register (Offset = 130h) [reset = 0h]

PWM0 Safety Config

Return to Summary Table

Table 4-1415. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6130h

Figure 4-685. ICSSM_PR1_CFG_SLV_PWM0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1416. ICSSM_PR1_CFG_SLV_PWM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.200 ICSSM_PR1_CFG_SLV_PWM1 Register

4.2.2.200.1 ICSSM_PR1_CFG_SLV_PWM1 Register (Offset = 134h) [reset = 0h]

PWM1 Safety Config

Return to Summary Table

Table 4-1417. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6134h

Figure 4-686. ICSSM_PR1_CFG_SLV_PWM1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1418. ICSSM_PR1_CFG_SLV_PWM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.201 ICSSM_PR1_CFG_SLV_PWM2 Register

4.2.2.201.1 ICSSM_PR1_CFG_SLV_PWM2 Register (Offset = 138h) [reset = 0h]

PWM2 Safety Config

Return to Summary Table

Table 4-1419. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6138h

Figure 4-687. ICSSM_PR1_CFG_SLV_PWM2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1420. ICSSM_PR1_CFG_SLV_PWM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.202 ICSSM_PR1_CFG_SLV_PWM3 Register

4.2.2.202.1 ICSSM_PR1_CFG_SLV_PWM3 Register (Offset = 13Ch) [reset = 0h]

PWM3 Safety Config

Return to Summary Table

Table 4-1421. Instance Table

Instance Name	Physical Address
ICSSM0	4802 613Ch

Figure 4-688. ICSSM_PR1_CFG_SLV_PWM3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1422. ICSSM_PR1_CFG_SLV_PWM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.203 ICSSM_PR1_CFG_SLV_PWM0_0 Register

4.2.2.203.1 ICSSM_PR1_CFG_SLV_PWM0_0 Register (Offset = 140h) [reset = 0h]

PWM0 State Config0

Return to Summary Table

Table 4-1423. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6140h

Figure 4-689. ICSSM_PR1_CFG_SLV_PWM0_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1424. ICSSM_PR1_CFG_SLV_PWM0_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.204 ICSSM_PR1_CFG_SLV_PWM0_1 Register

4.2.2.204.1 ICSSM_PR1_CFG_SLV_PWM0_1 Register (Offset = 144h) [reset = 0h]

PWM0 State Config1

Return to Summary Table

Table 4-1425. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6144h

Figure 4-690. ICSSM_PR1_CFG_SLV_PWM0_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1426. ICSSM_PR1_CFG_SLV_PWM0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.205 ICSSM_PR1_CFG_SLV_PWM0_2 Register

4.2.2.205.1 ICSSM_PR1_CFG_SLV_PWM0_2 Register (Offset = 148h) [reset = 0h]

PWM0 State Config2

Return to Summary Table

Table 4-1427. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6148h

Figure 4-691. ICSSM_PR1_CFG_SLV_PWM0_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1428. ICSSM_PR1_CFG_SLV_PWM0_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.206 ICSSM_PR1_CFG_SLV_PWM1_0 Register

4.2.2.206.1 ICSSM_PR1_CFG_SLV_PWM1_0 Register (Offset = 14Ch) [reset = 0h]

PWM1 State Config0

Return to Summary Table

Table 4-1429. Instance Table

Instance Name	Physical Address
ICSSM0	4802 614Ch

Figure 4-692. ICSSM_PR1_CFG_SLV_PWM1_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1430. ICSSM_PR1_CFG_SLV_PWM1_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.207 ICSSM_PR1_CFG_SLV_PWM1_1 Register

4.2.2.207.1 ICSSM_PR1_CFG_SLV_PWM1_1 Register (Offset = 150h) [reset = 0h]

PWM1 State Config1

Return to Summary Table

Table 4-1431. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6150h

Figure 4-693. ICSSM_PR1_CFG_SLV_PWM1_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1432. ICSSM_PR1_CFG_SLV_PWM1_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.208 ICSSM_PR1_CFG_SLV_PWM1_2 Register

4.2.2.208.1 ICSSM_PR1_CFG_SLV_PWM1_2 Register (Offset = 154h) [reset = 0h]

PWM1 State Config2

Return to Summary Table

Table 4-1433. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6154h

Figure 4-694. ICSSM_PR1_CFG_SLV_PWM1_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1434. ICSSM_PR1_CFG_SLV_PWM1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.209 ICSSM_PR1_CFG_SLV_PWM2_0 Register

4.2.2.209.1 ICSSM_PR1_CFG_SLV_PWM2_0 Register (Offset = 158h) [reset = 0h]

PWM2 State Config0

Return to Summary Table

Table 4-1435. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6158h

Figure 4-695. ICSSM_PR1_CFG_SLV_PWM2_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1436. ICSSM_PR1_CFG_SLV_PWM2_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.210 ICSSM_PR1_CFG_SLV_PWM2_1 Register

4.2.2.210.1 ICSSM_PR1_CFG_SLV_PWM2_1 Register (Offset = 15Ch) [reset = 0h]

PWM2 State Config1

Return to Summary Table

Table 4-1437. Instance Table

Instance Name	Physical Address
ICSSM0	4802 615Ch

Figure 4-696. ICSSM_PR1_CFG_SLV_PWM2_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1438. ICSSM_PR1_CFG_SLV_PWM2_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.211 ICSSM_PR1_CFG_SLV_PWM2_2 Register

4.2.2.211.1 ICSSM_PR1_CFG_SLV_PWM2_2 Register (Offset = 160h) [reset = 0h]

PWM2 State Config2

Return to Summary Table

Table 4-1439. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6160h

Figure 4-697. ICSSM_PR1_CFG_SLV_PWM2_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1440. ICSSM_PR1_CFG_SLV_PWM2_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.212 ICSSM_PR1_CFG_SLV_PWM3_0 Register

4.2.2.212.1 ICSSM_PR1_CFG_SLV_PWM3_0 Register (Offset = 164h) [reset = 0h]

PWM3 State Config0

Return to Summary Table

Table 4-1441. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6164h

Figure 4-698. ICSSM_PR1_CFG_SLV_PWM3_0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1442. ICSSM_PR1_CFG_SLV_PWM3_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.213 ICSSM_PR1_CFG_SLV_PWM3_1 Register

4.2.2.213.1 ICSSM_PR1_CFG_SLV_PWM3_1 Register (Offset = 168h) [reset = 0h]

PWM3 State Config1

Return to Summary Table

Table 4-1443. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6168h

Figure 4-699. ICSSM_PR1_CFG_SLV_PWM3_1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1444. ICSSM_PR1_CFG_SLV_PWM3_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.214 ICSSM_PR1_CFG_SLV_PWM3_2 Register

4.2.2.214.1 ICSSM_PR1_CFG_SLV_PWM3_2 Register (Offset = 16Ch) [reset = 0h]

PWM3 State Config2

Return to Summary Table

Table 4-1445. Instance Table

Instance Name	Physical Address
ICSSM0	4802 616Ch

Figure 4-700. ICSSM_PR1_CFG_SLV_PWM3_2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1446. ICSSM_PR1_CFG_SLV_PWM3_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.215 ICSSM_PR1_CFG_SLV_SPIN_LOCK0 Register

4.2.2.215.1 ICSSM_PR1_CFG_SLV_SPIN_LOCK0 Register (Offset = 170h) [reset = 0h]

Spin Lock

Return to Summary Table

Table 4-1447. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6170h

Figure 4-701. ICSSM_PR1_CFG_SLV_SPIN_LOCK0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1448. ICSSM_PR1_CFG_SLV_SPIN_LOCK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.216 ICSSM_PR1_CFG_SLV_SPIN_LOCK1 Register

4.2.2.216.1 ICSSM_PR1_CFG_SLV_SPIN_LOCK1 Register (Offset = 174h) [reset = 0h]

Spin Lock

Return to Summary Table

Table 4-1449. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6174h

Figure 4-702. ICSSM_PR1_CFG_SLV_SPIN_LOCK1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1450. ICSSM_PR1_CFG_SLV_SPIN_LOCK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.217 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG0 Register

4.2.2.217.1 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG0 Register (Offset = 178h) [reset = 0h]

PA STATS PDSP0 Vector

Return to Summary Table

Table 4-1451. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6178h

Figure 4-703. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1452. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.218 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT0 Register

4.2.2.218.1 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT0 Register (Offset = 17Ch) [reset = 0h]

PA STATS PDSP0 Status

Return to Summary Table

Table 4-1453. Instance Table

Instance Name	Physical Address
ICSSM0	4802 617Ch

Figure 4-704. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1454. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.219 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG1 Register

4.2.2.219.1 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG1 Register (Offset = 180h) [reset = 0h]

PA STATS PDSP1 Vector

Return to Summary Table

Table 4-1455. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6180h

Figure 4-705. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1456. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.220 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT1 Register

4.2.2.220.1 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT1 Register (Offset = 184h) [reset = 0h]

PA STATS PDSP1 Status

Return to Summary Table

Table 4-1457. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6184h

Figure 4-706. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1458. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.221 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG2 Register

4.2.2.221.1 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG2 Register (Offset = 188h) [reset = 0h]

PA STATS PDSP2 Vector

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Table 4-1459. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6188h

Figure 4-707. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1460. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.222 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT2 Register

4.2.2.222.1 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT2 Register (Offset = 18Ch) [reset = 0h]

PA STATS PDSP2 Status

Return to Summary Table

Table 4-1461. Instance Table

Instance Name	Physical Address
ICSSM0	4802 618Ch

Figure 4-708. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1462. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.223 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG3 Register

4.2.2.223.1 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG3 Register (Offset = 190h) [reset = 0h]

PA STATS PDSP3 Vector

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Table 4-1463. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6190h

Figure 4-709. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1464. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.224 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT3 Register

4.2.2.224.1 ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT3 Register (Offset = 194h) [reset = 0h]

PA STATS PDSP3 Status

Return to Summary Table

Table 4-1465. Instance Table

Instance Name	Physical Address
ICSSM0	4802 6194h

Figure 4-710. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1466. ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.225 ICSSM_PR1_ICSSS_UART_UART_SLV_RBR Register

4.2.2.225.1 ICSSM_PR1_ICSSS_UART_UART_SLV_RBR Register (Offset = 0h) [reset = 0h]

Receiver Buffer Register (read only)
The UART receiver section consists of a receiver shift register (RSR) and a receiver buffer register (RBR). When the UART is in the FIFO mode, RBR is a 16-byte FIFO. Timing is supplied by the 16x receiver clock or 13x receiver clock by programming OSM_SEL bit field of MDR register. Receiver section control is a function of the line control register (LCR).
RSR receives serial data from the UARTn_RXD pin. Then RSR concatenates the data and moves it into RBR (or the receiver FIFO). In the non-FIFO mode, when a character is placed in RBR and the receiver data-ready interrupt is enabled (DR = 1 in IER), an interrupt is generated. This interrupt is cleared when the character is read from RBR. In the FIFO mode, the interrupt is generated when the FIFO is filled to the trigger level selected in the FIFO control register (FCR), and it is cleared when the FIFO contents drop below the trigger level.

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Table 4-1467. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8000h

Figure 4-711. ICSSM_PR1_ICSSS_UART_UART_SLV_RBR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">RESERVED</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">DATA</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 4-1468. ICSSM_PR1_ICSSS_UART_UART_SLV_RBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:8	RESERVED	W	0h	Reserved
7:0	DATA	R	0h	Received Data

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4.2.2.226 ICSSM_PR1_ICSSS_UART_UART_SLV_IER Register

4.2.2.226.1 ICSSM_PR1_ICSSS_UART_UART_SLV_IER Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) is used to individually enable or disable each type of interrupt request that can be generated by the UART. Each interrupt request that is enabled in IER is forwarded to the CPU.

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Table 4-1469. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8004h

Figure 4-712. ICSSM_PR1_ICSSS_UART_UART_SLV_IER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EDSSI	ELSI	ETBEI	ERBI
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 4-1470. ICSSM_PR1_ICSSS_UART_UART_SLV_IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	EDSSI	R/W	0h	Enable for Modem Status Interrupt
2	ELSI	R/W	0h	Enable for Receiver Line Status Interrupt 0h Receiver line status interrupt is disabled. 1h Received line status is enabled
1	ETBEI	R/W	0h	Enable for Transmitter Holding Register Empty Interrupt 0h Transmitter holding register empty interrupt is disabled. 1h Transmitter holding register empty interrupt is enabled.
0	ERBI	R/W	0h	Enable for Receiver Data Available Interrupt 0h Receiver data available interrupt and character timeout indication interrupt is disabled. 1h Receiver data available interrupt and character timeout indication interrupt is enabled.

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4.2.2.227 ICSSM_PR1_ICSSS_UART_UART_SLV_IIR Register

4.2.2.227.1 ICSSM_PR1_ICSSS_UART_UART_SLV_IIR Register (Offset = 8h) [reset = 1h]

The interrupt identification register (IIR) is a read-only register at the same address as the FIFO control register (FCR), which is a write-only register. When an interrupt is generated and enabled in the interrupt enable register (IER), IIR indicates that an interrupt is pending in the IPEND bit and encodes the type of interrupt in the INTID bits. Reading IIR clears any THR empty (THRE) interrupts that are pending.

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Table 4-1471. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8008h

Figure 4-713. ICSSM_PR1_ICSSS_UART_UART_SLV_IIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		RESERVED		RESERVED	RESERVED	RESERVED	RESERVED
W		NONE		W	W	W	W
0h		0h		0h	0h	0h	0h
7	6	5	4	3	2	1	0
FIFOEN		RESERVED		INTID			IPEND
R		NONE		R			R
0h		0h		0h			1h

Table 4-1472. ICSSM_PR1_ICSSS_UART_UART_SLV_IIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:14	RESERVED	W	0h	Reserved
13:12	RESERVED	NONE	0h	Reserved
11	RESERVED	W	0h	Reserved
10	RESERVED	W	0h	Reserved
9	RESERVED	W	0h	Reserved
8	RESERVED	W	0h	Reserved
7:6	FIFOEN	R	0h	FIFOs enabled 0h Non-FIFO mode 1h-2h Reserved 3h FIFOs are enabled. FIFOEN bit in the FIFO control register (FCR) is set to 1.
5:4	RESERVED	NONE	0h	Reserved

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Table 4-1472. ICSSM_PR1_ICSSS_UART_UART_SLV_IIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:1	INTID	R	0h	Interrupt Type 0h Reserved 1h Transmitter holding register empty (priority 3) 2h Receiver data available (priority 2) 3h Receiver line status (priority 1, highest) 4h-5h Reserved 6h Character timeout indication (priority 2) 7h Reserved
0	IPEND	R	1h	Interrupt pending. When any UART interrupt is generated and is enabled in IER, IPEND is forced to 0. IPEND remains 0 until all pending interrupts are cleared or until a hardware reset occurs. If no interrupts are enabled, IPEND is never forced to 0. 0h Interrupts pending 1h No interrupts pending

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4.2.2.228 ICSSM_PR1_ICSSS_UART_UART_SLV_LCR Register

4.2.2.228.1 ICSSM_PR1_ICSSS_UART_UART_SLV_LCR Register (Offset = Ch) [reset = 0h]

Line Control Register (LCR)
The system programmer controls the format of the asynchronous data communication exchange by using LCR. In addition, the programmer can retrieve, inspect, and modify the content of LCR; this eliminates the need for separate storage of the line characteristics in system memory.

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Table 4-1473. Instance Table

Instance Name	Physical Address
ICSSM0	4802 800Ch

Figure 4-714. ICSSM_PR1_ICSSS_UART_UART_SLV_LCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLAB	BC	SP	EPS	PEN	STB	WLS1	WLS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1474. ICSSM_PR1_ICSSS_UART_UART_SLV_LCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	DLAB	R/W	0h	Divisor latch access bit. The divisor latch registers (DLL and DLH) can be accessed at dedicated addresses or at addresses shared by RBR, THR, and IER. Using the shared addresses requires toggling DLAB to change which registers are selected. If you use the dedicated addresses, you can keep DLAB = 0. 0 Allows access to the receiver buffer register (RBR), the transmitter holding register (THR), and the interrupt enable register (IER) selected. At the address shared by RBR, THR, and DLL, the CPU can read from RBR and write to THR. At the address shared by IER and DLH, the CPU can read from and write to IER. 1 Allows access to the divisor latches of the baud generator during a read or write operation (DLL and DLH). At the address shared by RBR, THR, and DLL, the CPU can read from and write to DLL. At the address shared by IER and DLH, the CPU can read from and write to DLH.

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Table 4-1474. ICSSM_PR1_ICSSS_UART_UART_SLV_LCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BC	R/W	0h	Break Control 0 Break condition is disabled 1 Break condition is transmitted to the receiving UART. A break condition is a condition where the UARTn_TXD signal is forced to the spacing (cleared) state.
5	SP	R/W	0h	Stick parity. The SP bit works in conjunction with the EPS and PEN bits. 0 Stick parity is disabled 1 Stick parity is enabled -When odd parity is selected (EPS = 0), the PARITY bit is transmitted and checked as set. -When even parity is selected (EPS = 1), the PARITY bit is transmitted and checked as cleared.
4	EPS	R/W	0h	Even parity select. Selects the parity when parity is enabled (PEN = 1). The EPS bit works in conjunction with the SP and PEN bits. 0 Odd parity is selected (an odd number of logic 1s is transmitted or checked in the data and PARITY bits). 1 Even parity is selected (an even number of logic 1s is transmitted or checked in the data and PARITY bits).
3	PEN	R/W	0h	Parity enable. The PEN bit works in conjunction with the SP and EPS bits. 0 No PARITY bit is transmitted or checked. 1 Parity bit is generated in transmitted data and is checked in received data between the last data word bit and the first STOP bit.
2	STB	R/W	0h	Number of STOP bits generated. STB specifies 1, 1.5, or 2 STOP bits in each transmitted character. When STB = 1, the WLS bit determines the number of STOP bits. The receiver clocks only the first STOP bit, regardless of the number of STOP bits selected. 0 1 STOP bit is generated. 1 WLS bit determines the number of STOP bits: -When WLS = 0, 1.5 STOP bits are generated. -When WLS = 1h, 2h, or 3h, 2 STOP bits are generated.
1	WLS1	R/W	0h	Word Length Select Bit 1
0	WLS	R/W	0h	Word length select. Number of bits in each transmitted or received serial character. When STB = 1, the WLS bit determines the number of STOP bits. 0 5 bits 1 6 bits 2 7 bits 3 8 bits

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4.2.2.229 ICSSM_PR1_ICSSS_UART_UART_SLV_MCR Register

4.2.2.229.1 ICSSM_PR1_ICSSS_UART_UART_SLV_MCR Register (Offset = 10h) [reset = 0h]

Modem Control Register (MCR)
The modem control register provides the ability to enable/disable the autoflow functions, and enable/disable the loopback function for diagnostic purposes.

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Table 4-1475. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8010h

Figure 4-715. ICSSM_PR1_ICSSS_UART_UART_SLV_MCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		AFE	LOOP	OUT2	OUT1	RTS	RESERVED
NONE		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 4-1476. ICSSM_PR1_ICSSS_UART_UART_SLV_MCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	AFE	R/W	0h	Autoflow control enable. Autoflow control allows the UARTn_RTS and UARTn_CTS signals to provide handshaking between UARTs during data transfer. When AFE = 1, the RTS bit determines the autoflow control enabled. Note that all UARTs do not support this feature, see your device-specific data manual for supported features. If this feature is not available, this bit is reserved and should be cleared to 0. 0 Autoflow control is disabled. 1 Autoflow control is enabled: -When RTS = 0, UARTnCTS is only enabled -When RTS = 1, UARTn_RTS and UARTn_CTS are enabled
4	LOOP	R/W	0h	Loop back mode enable. LOOP is used for the diagnostic testing using the loop back feature. 0 Loop back mode is disabled. 1 Loop back mode is enabled. When LOOP is set, the following occur: -The UARTn_TXD signal is set high. -The UARTn_RXD pin is disconnected -The output of the transmitter shift register (TSR) is lopped back in to the receiver shift register (RSR) input.
3	OUT2	R/W	0h	Out2 Bit
2	OUT1	R/W	0h	Out1 Bit

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Table 4-1476. ICSSM_PR1_ICSSS_UART_UART_SLV_MCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RTS	R/W	0h	RTS control. When AFE = 1, the RTS bit determines the autoflow control enabled. Note that all UARTs do not support this feature, see your device-specific data manual for supported features. If this feature is not available, this bit is reserved and should be cleared to 0. 0 `UARTn_RTS is disabled, UARTn_CTS is only enabled.` 1 `UARTn_RTS and UARTn_CTS are enabled.`
0	RESERVED	R/W	0h	Reserved

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4.2.2.230 ICSSM_PR1_ICSSS_UART_UART_SLV_LSR Register

4.2.2.230.1 ICSSM_PR1_ICSSS_UART_UART_SLV_LSR Register (Offset = 14h) [reset = 60h]

Line Status Register (LSR)
LSR provides information to the CPU concerning the status of data transfers. LSR is intended for read operations only; do not write to this register. Bits 1 through 4 record the error conditions that produce a receiver line status interrupt.

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Table 4-1477. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8014h

Figure 4-716. ICSSM_PR1_ICSSS_UART_UART_SLV_LSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RXFIFOE	TEMT	THRE	BI	FE	PE	OE	DR
R	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 4-1478. ICSSM_PR1_ICSSS_UART_UART_SLV_LSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	RXFIFOE	R	0h	Receiver FIFO error. In non-FIFO mode: 0 = There has been no error, or RXFIFOE was cleared because the CPU read the erroneous character from the receiver buffer register (RBR). 1 = There is a parity error, framing error, or break indicator in the receiver buffer register (RBR). In FIFO mode: 0 = There has been no error, or RXFIFOE was cleared because the CPU read the erroneous character from the receiver FIFO and there are no more errors in the receiver FIFO. 1 = At least one parity error, framing error, or break indicator in the receiver FIFO.

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Table 4-1478. ICSSM_PR1_ICSSS_UART_UART_SLV_LSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TEMT	R	1h	Transmitter empty (TEMT) indicator. In non-FIFO mode: 0 = Either the transmitter holding register (THR) or the transmitter shift register (TSR) contains a data character. 1 = Both the transmitter holding register (THR) and the transmitter shift register (TSR) are empty. In FIFO mode: 0 = Either the transmitter FIFO or the transmitter shift register (TSR) contains a data character. 1 = Both the transmitter FIFO and the transmitter shift register (TSR) are empty.
5	THRE	R	1h	Transmitter holding register empty (THRE) indicator. If the THRE bit is set and the corresponding interrupt enable bit is set (ETBEI = 1 in IER), an interrupt request is generated. In non-FIFO mode: 0 = Transmitter holding register (THR) is not empty. THR has been loaded by the CPU. 1 = Transmitter holding register (THR) is empty (ready to accept a new character). The content of THR has been transferred to the transmitter shift register (TSR). In FIFO mode: 0 = Transmitter FIFO is not empty. At least one character has been written to the transmitter FIFO. You can write to the transmitter FIFO if it is not full. 1 = Transmitter FIFO is empty. The last character in the FIFO has been transferred to the transmitter shift register (TSR).
4	BI	R	0h	Break indicator. The BI bit is set whenever the receive data input (UARTn_RXD) was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the START, data, PARITY, and STOP bits. If the BI bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. In non-FIFO mode: 0 = No break has been detected, or the BI bit was cleared because the CPU read the erroneous character from the receiver buffer register (RBR). 1 = A break has been detected with the character in the receiver buffer register (RBR). In FIFO mode: 0 = No break has been detected, or the BI bit was cleared because the CPU read the erroneous character from the receiver FIFO and the next character to be read from the FIFO has no break indicator. 1 = A break has been detected with the character at the top of the receiver FIFO.
3	FE	R	0h	Framing error (FE) indicator. A framing error occurs when the received character does not have a valid STOP bit. In response to a framing error, the UART sets the FE bit and waits until the signal on the RX pin goes high. Once the RX signal goes high, the receiver is ready to detect a new START bit and receive new data. If the FE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. In non-FIFO mode: 0 = No framing error has been detected, or the FE bit was cleared because the CPU read the erroneous data from the receiver buffer register (RBR). 1 = A framing error has been detected with the character in the receiver buffer register (RBR). In FIFO mode: 0 = No framing error has been detected, or the FE bit was cleared because the CPU read the erroneous data from the receiver FIFO and the next character to be read from the FIFO has no framing error. 1 = A framing error has been detected with the character at the top of the receiver FIFO.

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Table 4-1478. ICSSM_PR1_ICSSS_UART_UART_SLV_LSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PE	R	0h	Parity error (PE) indicator. A parity error occurs when the parity of the received character does not match the parity selected with the EPS bit in the line control register (LCR). If the PE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. In non-FIFO mode: 0 = No parity error has been detected, or the PE bit was cleared because the CPU read the erroneous data from the receiver buffer register (RBR). 1 = A parity error has been detected with the character in the receiver buffer register (RBR). In FIFO mode: 0 = No parity error has been detected, or the PE bit was cleared because the CPU read the erroneous data from the receiver FIFO and the next character to be read from the FIFO has no parity error. 1 = A parity error has been detected with the character at the top of the receiver FIFO.
1	OE	R	0h	Overrun error (OE) indicator. An overrun error in the non-FIFO mode is different from an overrun error in the FIFO mode. If the OE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. In non-FIFO mode: 0 = No overrun error has been detected, or the OE bit was cleared because the CPU read the content of the line status register (LSR). 1 = Overrun error has been detected. Before the character in the receiver buffer register (RBR) could be read, it was overwritten by the next character arriving in RBR. In FIFO mode: 0 = No overrun error has been detected, or the OE bit was cleared because the CPU read the content of the line status register (LSR). 1 = Overrun error has been detected. If data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The new character overwrites the character in the shift register, but it is not transferred to the FIFO.
0	DR	R	0h	Data-ready (DR) indicator for the receiver. If the DR bit is set and the corresponding interrupt enable bit is set (ERBI = 1 in IER), an interrupt request is generated. In non-FIFO mode: 0 = Data is not ready, or the DR bit was cleared because the character was read from the receiver buffer register (RBR). 1 = Data is ready. A complete incoming character has been received and transferred into the receiver buffer register (RBR). In FIFO mode: 0 = Data is not ready, or the DR bit was cleared because all of the characters in the receiver FIFO have been read. 1 = Data is ready. There is at least one unread character in the receiver FIFO. If the FIFO is empty, the DR bit is set as soon as a complete incoming character has been received and transferred into the FIFO. The DR bit remains set until the FIFO is empty again.

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4.2.2.231 ICSSM_PR1_ICSSS_UART_UART_SLV_MSR Register

4.2.2.231.1 ICSSM_PR1_ICSSS_UART_UART_SLV_MSR Register (Offset = 18h) [reset = 0h]

Modem Status Register (MSR)
MSR provides information to the CPU concerning the status of modem control signals. MSR is intended for read operations only; do not write to this register.

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Table 4-1479. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8018h

Figure 4-717. ICSSM_PR1_ICSSS_UART_UART_SLV_MSR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CD	RI	DSR	CTS	DCD	TERI	DDSR	DCTS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1480. ICSSM_PR1_ICSSS_UART_UART_SLV_MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	CD	R	0h	Complement of the Carrier Detect input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 3 (OUT2).
6	RI	R	0h	Complement of the Ring Indicator input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 2 (OUT1).
5	DSR	R	0h	Complement of the Data Set Ready input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 0 (DTR).
4	CTS	R	0h	Complement of the Clear To Send input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 1 (RTS).
3	DCD	R	0h	Change in DCD indicator bit. DCD indicates that the DCD input has changed state since the last time it was read by the CPU. When DCD is set and the modem status interrupt is enabled, a modem status interrupt is generated.
2	TERI	R	0h	Trailing edge of RI (TERI) indicator bit. TERI indicates that the RI input has changed from a low to a high. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated.

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Table 4-1480. ICSSM_PR1_ICSSS_UART_UART_SLV_MSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DDSR	R	0h	Change in DSR indicator bit. DDSR indicates that the DSR input has changed state since the last time it was read by the CPU. When DDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated.
0	DCTS	R	0h	Change in CTS indicator bit. DCTS indicates that the CTS input has changed state since the last time it was read by the CPU. When DCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled, no interrupt is generated.

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4.2.2.232 ICSSM_PR1_ICSSS_UART_UART_SLV_SCR Register

4.2.2.232.1 ICSSM_PR1_ICSSS_UART_UART_SLV_SCR Register (Offset = 1Ch) [reset = 0h]

Scratch Pad Register (SCR)
SCR is intended for programmer's use as a scratch pad. It temporarily holds the programmer's data without affecting UART operation.

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Table 4-1481. Instance Table

Instance Name	Physical Address
ICSSM0	4802 801Ch

Figure 4-718. ICSSM_PR1_ICSSS_UART_UART_SLV_SCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 4-1482. ICSSM_PR1_ICSSS_UART_UART_SLV_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATA	R/W	0h	Scratch Register Bits These bits are intended for the programmer's use as a scratch pad in the sense that it temporarily holds the programmer's data without affecting any other UART operation.

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4.2.2.233 ICSSM_PR1_ICSSS_UART_UART_SLV_DLL Register

4.2.2.233.1 ICSSM_PR1_ICSSS_UART_UART_SLV_DLL Register (Offset = 20h) [reset = 0h]

Divisor LSB Latch.

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Table 4-1483. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8020h

Figure 4-719. ICSSM_PR1_ICSSS_UART_UART_SLV_DLL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DLL							
R/W							
0h							

Table 4-1484. ICSSM_PR1_ICSSS_UART_UART_SLV_DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DLL	R/W	0h	The 8 least-significant bits (LSBs) of the 16-bit divisor for generation of the baud clock in the baud rate generator.

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4.2.2.234 ICSSM_PR1_ICSSS_UART_UART_SLV_DLH Register

4.2.2.234.1 ICSSM_PR1_ICSSS_UART_UART_SLV_DLH Register (Offset = 24h) [reset = 0h]

Divisor MSB Latch.

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Table 4-1485. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8024h

Figure 4-720. ICSSM_PR1_ICSSS_UART_UART_SLV_DLH Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DLH							
R/W							
0h							

Table 4-1486. ICSSM_PR1_ICSSS_UART_UART_SLV_DLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DLH	R/W	0h	The 8 most-significant bits (MSBs) of the 16-bit divisor for generation of the baud clock in the baud rate generator.

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4.2.2.235 ICSSM_PR1_ICSSS_UART_UART_SLV_REVID1 Register

4.2.2.235.1 ICSSM_PR1_ICSSS_UART_UART_SLV_REVID1 Register (Offset = 28h) [reset = 44141102h]

Revision Identification Register 1

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Table 4-1487. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8028h

Figure 4-721. ICSSM_PR1_ICSSS_UART_UART_SLV_REVID1 Name Register

31	30	29	28	27	26	25	24
REVID1							
R							
11020002h							
23	22	21	20	19	18	17	16
REVID1							
R							
11020002h							
15	14	13	12	11	10	9	8
REVID1							
R							
11020002h							
7	6	5	4	3	2	1	0
REVID1							
R							
11020002h							

Table 4-1488. ICSSM_PR1_ICSSS_UART_UART_SLV_REVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REVID1	R	11020002h	Peripheral Identification Number

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4.2.2.236 ICSSM_PR1_ICSSS_UART_UART_SLV_PWREMU_MGMT Register

4.2.2.236.1 ICSSM_PR1_ICSSS_UART_UART_SLV_PWREMU_MGMT Register (Offset = 30h) [reset = 2h]

UART PowerManagement and Emulation Register.

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Table 4-1489. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8030h

Figure 4-722. ICSSM_PR1_ICSSS_UART_UART_SLV_PWREMU_MGMT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	UTRST	URRST	RESERVED				
R/W	R/W	R/W	NONE				
0h	0h	0h	0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						RESERVED	FREE
NONE						R	R/W
0h						1h	0h

Table 4-1490. ICSSM_PR1_ICSSS_UART_UART_SLV_PWREMU_MGMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	RESERVED	R/W	0h	Reserved
14	UTRST	R/W	0h	UART transmitter reset. Resets and enables the transmitter. 0 Transmitter is disabled and in reset state. 1 Transmitter is enabled.
13	URRST	R/W	0h	UART receiver reset. Resets and enables the receiver. 0 Receiver is disabled and in reset state. 1 Receiver is enabled.
12:2	RESERVED	NONE	0h	Reserved
1	RESERVED	R	1h	Reserved
0	FREE	R/W	0h	Free-running enable mode bit. This bit determines the emulation mode functionality of the UART. When halted, the UART can handle register read/write requests, but does not generate any transmission/ reception, interrupts or events. 0 If a transmission is not in progress, the UART halts immediately. If a transmission is in progress, the UART halts after completion of the one-word transmission. 1 Free-running mode is enabled; UART continues to run normally.

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4.2.2.237 ICSSM_PR1_ICSSS_UART_UART_SLV_MDR Register

4.2.2.237.1 ICSSM_PR1_ICSSS_UART_UART_SLV_MDR Register (Offset = 34h) [reset = 0h]

UART Mode Definition Register.

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Table 4-1491. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8034h

Figure 4-723. ICSSM_PR1_ICSSS_UART_UART_SLV_MDR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							OSM_SEL
NONE							R/W
0h							0h

Table 4-1492. ICSSM_PR1_ICSSS_UART_UART_SLV_MDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	OSM_SEL	R/W	0h	Over-Sampling Mode Select 0 16x over-sampling 1 13x over-sampling

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4.2.2.238 ICSSM_PR1_ICSSS_UART_UART_SLV_THR Register

4.2.2.238.1 ICSSM_PR1_ICSSS_UART_UART_SLV_THR Register (Offset = 0h) [reset = 0h]

The transmitter holding register (THR) (write only)
The UART transmitter section consists of a transmitter hold register (THR) and a transmitter shift register (TSR). When the UART is in the FIFO mode, THR is a 16-byte FIFO. Transmitter section control is a function of the line control register (LCR).
THR receives data from the internal data bus and when TSR is idle, the UART moves the data from THR to TSR. The UART serializes the data in TSR and transmits the data on the TX pin. In the non-FIFO mode, if THR is empty and the THR empty (THRE) interrupt is enabled (ETBEI = 1 in IER), an interrupt is generated. This interrupt is cleared when a character is loaded into THR or the interrupt identification register (IIR) is read. In the FIFO mode, the interrupt is generated when the transmitter FIFO is empty, and it is cleared when at least one byte is loaded into the FIFO or IIR is read.

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Table 4-1493. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8000h

Figure 4-724. ICSSM_PR1_ICSSS_UART_UART_SLV_THR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DATA							
W							
0h							

Table 4-1494. ICSSM_PR1_ICSSS_UART_UART_SLV_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DATA	W	0h	Data to transmit

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4.2.2.239 ICSSM_PR1_ICSSS_UART_UART_SLV_FCR Register

4.2.2.239.1 ICSSM_PR1_ICSSS_UART_UART_SLV_FCR Register (Offset = 8h) [reset = 0h]

FIFO Control Register (write only)
The FIFO control register (FCR) is a write-only register at the same address as the interrupt identification register (IIR), which is a read-only register.

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Table 4-1495. Instance Table

Instance Name	Physical Address
ICSSM0	4802 8008h

Figure 4-725. ICSSM_PR1_ICSSS_UART_UART_SLV_FCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RXFITL		RESERVED		DMAMODE1	TXCLR	RXCLR	FIFOEN
W		NONE		W	W	W	W
0h		0h		1h	0h	0h	0h

Table 4-1496. ICSSM_PR1_ICSSS_UART_UART_SLV_FCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	RXFITL	W	0h	Receiver FIFO trigger level. RXFIFTL sets the trigger level for the receiver FIFO. When the trigger level is reached, a receiver data-ready interrupt is generated (if the interrupt request is enabled). Once the FIFO drops below the trigger level, the interrupt is cleared. 0h 1 byte 1h 4 bytes 2h 8 bytes 3h 14 bytes
5:4	RESERVED	NONE	0h	Reserved
3	DMAMODE1	W	1h	DMA MODE1 enable if FIFOs are enabled. Always write 1 to DMAMODE1. After a hardware reset, change DMAMODE1 from 0 to 1. DMAMODE1 = 1 is a requirement for proper communication between the UART and the EDMA controller. 0h DMA MODE 1 is disabled 1h DMA MODE 1 is enabled
2	TXCLR	W	0h	Transmitter FIFO clear. Write a 1 to TXCLR to clear the bit. 0h No effect 1h Clears transmitter FIFO and resets the transmitter FIFO counter. The shift register is not cleared.

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Table 4-1496. ICSSM_PR1_ICSSS_UART_UART_SLV_FCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RXCLR	W	0h	Receiver FIFO clear. Write a 1 to RXCLR to clear the bit. 0h No effect 1h Clears receiver FIFO and resets the receiver FIFO counter. The shift register is not cleared.
0	FIFOEN	W	0h	Transmitter and receiver FIFOs mode enable. FIFOEN must be set before other FCR bits are written to or the FCR bits are not programmed. Clearing this bit clears the FIFO counters. 0h Non-FIFO mode. The transmitter and receiver FIFOs are disabled, and the FIFO pointers are cleared. 1h FIFO mode. The transmitter and receiver FIFOs are enabled.

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4.2.2.240 ICSSM_PR1_ICSSS_UART_UART_SLV_REVID2 Register

4.2.2.240.1 ICSSM_PR1_ICSSS_UART_UART_SLV_REVID2 Register (Offset = 2Ch) [reset = 0h]

Revision Identification Register 2

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Table 4-1497. Instance Table

Instance Name	Physical Address
ICSSM0	4802 802Ch

Figure 4-726. ICSSM_PR1_ICSSS_UART_UART_SLV_REVID2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REVID2							
R							
0h							

Table 4-1498. ICSSM_PR1_ICSSS_UART_UART_SLV_REVID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	REVID2	R	0h	Peripheral Identification Number

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4.2.2.241 ICSSM_PR1_IEP0_SLV_GLOBAL_CFG_REG Register

4.2.2.241.1 ICSSM_PR1_IEP0_SLV_GLOBAL_CFG_REG Register (Offset = 0h) [reset = 550h]

Global Cfg

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Table 4-1499. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E000h

Figure 4-727. ICSSM_PR1_IEP0_SLV_GLOBAL_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				CMP_INC			
NONE				R/W			
0h				5h			
15	14	13	12	11	10	9	8
CMP_INC							
R/W							
5h							
7	6	5	4	3	2	1	0
DEFAULT_INC				RESERVED			CNT_ENABLE
R/W				NONE			R/W
5h				0h			0h

Table 4-1500. ICSSM_PR1_IEP0_SLV_GLOBAL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:8	CMP_INC	R/W	5h	
7:4	DEFAULT_INC	R/W	5h	
3:1	RESERVED	NONE	0h	Reserved
0	CNT_ENABLE	R/W	0h	

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4.2.2.242 ICSSM_PR1_IEP0_SLV_GLOBAL_STATUS_REG Register

4.2.2.242.1 ICSSM_PR1_IEP0_SLV_GLOBAL_STATUS_REG Register (Offset = 4h) [reset = 0h]

Status

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Table 4-1501. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E004h

Figure 4-728. ICSSM_PR1_IEP0_SLV_GLOBAL_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CNT_OVF
NONE							R/W1TC
0h							0h

Table 4-1502. ICSSM_PR1_IEP0_SLV_GLOBAL_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CNT_OVF	R/W1TC	0h	

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4.2.2.243 ICSSM_PR1_IEP0_SLV_COMPEN_REG Register

4.2.2.243.1 ICSSM_PR1_IEP0_SLV_COMPEN_REG Register (Offset = 8h) [reset = 0h]

Compensation

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Table 4-1503. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E008h

Figure 4-729. ICSSM_PR1_IEP0_SLV_COMPEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	COMPEN_CNT						
NONE	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COMPEN_CNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMPEN_CNT							
R/W							
0h							

Table 4-1504. ICSSM_PR1_IEP0_SLV_COMPEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:0	COMPEN_CNT	R/W	0h	

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4.2.2.244 ICSSM_PR1_IEP0_SLV_SLOW_COMPEN_REG Register

4.2.2.244.1 ICSSM_PR1_IEP0_SLV_SLOW_COMPEN_REG Register (Offset = Ch) [reset = 0h]

Slow Compensation

Return to Summary Table

Table 4-1505. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E00Ch

Figure 4-730. ICSSM_PR1_IEP0_SLV_SLOW_COMPEN_REG Name Register

31	30	29	28	27	26	25	24
SLOW_COMPEN_CNT							
R/W							
0h							
23	22	21	20	19	18	17	16
SLOW_COMPEN_CNT							
R/W							
0h							
15	14	13	12	11	10	9	8
SLOW_COMPEN_CNT							
R/W							
0h							
7	6	5	4	3	2	1	0
SLOW_COMPEN_CNT							
R/W							
0h							

Table 4-1506. ICSSM_PR1_IEP0_SLV_SLOW_COMPEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SLOW_COMPEN_CNT	R/W	0h	

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4.2.2.245 ICSSM_PR1_IEP0_SLV_COUNT_REG0 Register

4.2.2.245.1 ICSSM_PR1_IEP0_SLV_COUNT_REG0 Register (Offset = 10h) [reset = 0h]

Low Counter

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Table 4-1507. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E010h

Figure 4-731. ICSSM_PR1_IEP0_SLV_COUNT_REG0 Name Register

31	30	29	28	27	26	25	24
COUNT_LO							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT_LO							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT_LO							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT_LO							
R/W							
0h							

Table 4-1508. ICSSM_PR1_IEP0_SLV_COUNT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT_LO	R/W	0h	

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4.2.2.246 ICSSM_PR1_IEP0_SLV_COUNT_REG1 Register

4.2.2.246.1 ICSSM_PR1_IEP0_SLV_COUNT_REG1 Register (Offset = 14h) [reset = 0h]

High Counter

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Table 4-1509. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E014h

Figure 4-732. ICSSM_PR1_IEP0_SLV_COUNT_REG1 Name Register

31	30	29	28	27	26	25	24
COUNT_HI							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT_HI							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT_HI							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT_HI							
R/W							
0h							

Table 4-1510. ICSSM_PR1_IEP0_SLV_COUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT_HI	R/W	0h	

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4.2.2.247 ICSSM_PR1_IEP0_SLV_CAP_CFG_REG Register

4.2.2.247.1 ICSSM_PR1_IEP0_SLV_CAP_CFG_REG Register (Offset = 18h) [reset = 1FC00h]

Capture Cfg

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Table 4-1511. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E018h

Figure 4-733. ICSSM_PR1_IEP0_SLV_CAP_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
EXT_CAP_EN						CAP_ASYNC_EN	
R/W						R/W	
0h						7Fh	
15	14	13	12	11	10	9	8
CAP_ASYNC_EN						CAP_EN	
R/W						R/W	
7Fh						0h	
7	6	5	4	3	2	1	0
CAP_EN							
R/W							
0h							

Table 4-1512. ICSSM_PR1_IEP0_SLV_CAP_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:18	EXT_CAP_EN	R/W	0h	
17:10	CAP_ASYNC_EN	R/W	7Fh	
9:0	CAP_EN	R/W	0h	

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4.2.2.248 ICSSM_PR1_IEP0_SLV_CAP_STATUS_REG Register

4.2.2.248.1 ICSSM_PR1_IEP0_SLV_CAP_STATUS_REG Register (Offset = 1Ch) [reset = 0h]

Capture Status Cfg

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Table 4-1513. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E01Ch

Figure 4-734. ICSSM_PR1_IEP0_SLV_CAP_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CAP_RAW							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					CAP_VALID		
NONE					R		
0h					0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAP_VALID							
R							
0h							

Table 4-1514. ICSSM_PR1_IEP0_SLV_CAP_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	CAP_RAW	R	0h	
15:11	RESERVED	NONE	0h	Reserved
10:0	CAP_VALID	R	0h	

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4.2.2.249 ICSSM_PR1_IEP0_SLV_CAPR0_REG0 Register

4.2.2.249.1 ICSSM_PR1_IEP0_SLV_CAPR0_REG0 Register (Offset = 20h) [reset = 0h]

Capture Rise00

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Table 4-1515. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E020h

Figure 4-735. ICSSM_PR1_IEP0_SLV_CAPR0_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR0_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR0_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR0_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR0_0							
R							
0h							

Table 4-1516. ICSSM_PR1_IEP0_SLV_CAPR0_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR0_0	R	0h	

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4.2.2.250 ICSSM_PR1_IEP0_SLV_CAPR0_REG1 Register

4.2.2.250.1 ICSSM_PR1_IEP0_SLV_CAPR0_REG1 Register (Offset = 24h) [reset = 0h]

Capture Rise10

Return to Summary Table

Table 4-1517. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E024h

Figure 4-736. ICSSM_PR1_IEP0_SLV_CAPR0_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR0_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR0_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR0_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR0_1							
R							
0h							

Table 4-1518. ICSSM_PR1_IEP0_SLV_CAPR0_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR0_1	R	0h	

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4.2.2.251 ICSSM_PR1_IEP0_SLV_CAPR1_REG0 Register

4.2.2.251.1 ICSSM_PR1_IEP0_SLV_CAPR1_REG0 Register (Offset = 28h) [reset = 0h]

Capture Rise01

Return to Summary Table

Table 4-1519. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E028h

Figure 4-737. ICSSM_PR1_IEP0_SLV_CAPR1_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR1_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR1_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR1_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR1_0							
R							
0h							

Table 4-1520. ICSSM_PR1_IEP0_SLV_CAPR1_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR1_0	R	0h	

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4.2.2.252 ICSSM_PR1_IEP0_SLV_CAPR1_REG1 Register

4.2.2.252.1 ICSSM_PR1_IEP0_SLV_CAPR1_REG1 Register (Offset = 2Ch) [reset = 0h]

Capture Rise11

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Table 4-1521. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E02Ch

Figure 4-738. ICSSM_PR1_IEP0_SLV_CAPR1_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR1_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR1_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR1_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR1_1							
R							
0h							

Table 4-1522. ICSSM_PR1_IEP0_SLV_CAPR1_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR1_1	R	0h	

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4.2.2.253 ICSSM_PR1_IEP0_SLV_CAPR2_REG0 Register

4.2.2.253.1 ICSSM_PR1_IEP0_SLV_CAPR2_REG0 Register (Offset = 30h) [reset = 0h]

Capture Rise02

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Table 4-1523. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E030h

Figure 4-739. ICSSM_PR1_IEP0_SLV_CAPR2_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR2_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR2_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR2_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR2_0							
R							
0h							

Table 4-1524. ICSSM_PR1_IEP0_SLV_CAPR2_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR2_0	R	0h	

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4.2.2.254 ICSSM_PR1_IEP0_SLV_CAPR2_REG1 Register

4.2.2.254.1 ICSSM_PR1_IEP0_SLV_CAPR2_REG1 Register (Offset = 34h) [reset = 0h]

Capture Rise12

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Table 4-1525. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E034h

Figure 4-740. ICSSM_PR1_IEP0_SLV_CAPR2_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR2_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR2_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR2_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR2_1							
R							
0h							

Table 4-1526. ICSSM_PR1_IEP0_SLV_CAPR2_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR2_1	R	0h	

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4.2.2.255 ICSSM_PR1_IEP0_SLV_CAPR3_REG0 Register

4.2.2.255.1 ICSSM_PR1_IEP0_SLV_CAPR3_REG0 Register (Offset = 38h) [reset = 0h]

Capture Rise03

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Table 4-1527. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E038h

Figure 4-741. ICSSM_PR1_IEP0_SLV_CAPR3_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR3_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR3_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR3_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR3_0							
R							
0h							

Table 4-1528. ICSSM_PR1_IEP0_SLV_CAPR3_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR3_0	R	0h	

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4.2.2.256 ICSSM_PR1_IEP0_SLV_CAPR3_REG1 Register

4.2.2.256.1 ICSSM_PR1_IEP0_SLV_CAPR3_REG1 Register (Offset = 3Ch) [reset = 0h]

Capture Rise13

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Table 4-1529. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E03Ch

Figure 4-742. ICSSM_PR1_IEP0_SLV_CAPR3_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR3_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR3_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR3_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR3_1							
R							
0h							

Table 4-1530. ICSSM_PR1_IEP0_SLV_CAPR3_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR3_1	R	0h	

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4.2.2.257 ICSSM_PR1_IEP0_SLV_CAPR4_REG0 Register

4.2.2.257.1 ICSSM_PR1_IEP0_SLV_CAPR4_REG0 Register (Offset = 40h) [reset = 0h]

Capture Rise04

Return to Summary Table

Table 4-1531. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E040h

Figure 4-743. ICSSM_PR1_IEP0_SLV_CAPR4_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR4_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR4_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR4_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR4_0							
R							
0h							

Table 4-1532. ICSSM_PR1_IEP0_SLV_CAPR4_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR4_0	R	0h	

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4.2.2.258 ICSSM_PR1_IEP0_SLV_CAPR4_REG1 Register

4.2.2.258.1 ICSSM_PR1_IEP0_SLV_CAPR4_REG1 Register (Offset = 44h) [reset = 0h]

Capture Rise14

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Table 4-1533. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E044h

Figure 4-744. ICSSM_PR1_IEP0_SLV_CAPR4_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR4_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR4_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR4_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR4_1							
R							
0h							

Table 4-1534. ICSSM_PR1_IEP0_SLV_CAPR4_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR4_1	R	0h	

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4.2.2.259 ICSSM_PR1_IEP0_SLV_CAPR5_REG0 Register

4.2.2.259.1 ICSSM_PR1_IEP0_SLV_CAPR5_REG0 Register (Offset = 48h) [reset = 0h]

Capture Rise05

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Table 4-1535. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E048h

Figure 4-745. ICSSM_PR1_IEP0_SLV_CAPR5_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR5_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR5_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR5_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR5_0							
R							
0h							

Table 4-1536. ICSSM_PR1_IEP0_SLV_CAPR5_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR5_0	R	0h	

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4.2.2.260 ICSSM_PR1_IEP0_SLV_CAPR5_REG1 Register

4.2.2.260.1 ICSSM_PR1_IEP0_SLV_CAPR5_REG1 Register (Offset = 4Ch) [reset = 0h]

Capture Rise15

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Table 4-1537. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E04Ch

Figure 4-746. ICSSM_PR1_IEP0_SLV_CAPR5_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR5_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR5_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR5_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR5_1							
R							
0h							

Table 4-1538. ICSSM_PR1_IEP0_SLV_CAPR5_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR5_1	R	0h	

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4.2.2.261 ICSSM_PR1_IEP0_SLV_CAPR6_REG0 Register

4.2.2.261.1 ICSSM_PR1_IEP0_SLV_CAPR6_REG0 Register (Offset = 50h) [reset = 0h]

Capture Rise06

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Table 4-1539. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E050h

Figure 4-747. ICSSM_PR1_IEP0_SLV_CAPR6_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR6_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR6_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR6_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR6_0							
R							
0h							

Table 4-1540. ICSSM_PR1_IEP0_SLV_CAPR6_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR6_0	R	0h	

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4.2.2.262 ICSSM_PR1_IEP0_SLV_CAPR6_REG1 Register

4.2.2.262.1 ICSSM_PR1_IEP0_SLV_CAPR6_REG1 Register (Offset = 54h) [reset = 0h]

Capture Rise16

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Table 4-1541. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E054h

Figure 4-748. ICSSM_PR1_IEP0_SLV_CAPR6_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR6_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CAPR6_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CAPR6_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAPR6_1							
R							
0h							

Table 4-1542. ICSSM_PR1_IEP0_SLV_CAPR6_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR6_1	R	0h	

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4.2.2.263 ICSSM_PR1_IEP0_SLV_CAPF6_REG0 Register

4.2.2.263.1 ICSSM_PR1_IEP0_SLV_CAPF6_REG0 Register (Offset = 58h) [reset = 0h]

Capture Fall06

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Table 4-1543. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E058h

Figure 4-749. ICSSM_PR1_IEP0_SLV_CAPF6_REG0 Name Register

31	30	29	28	27	26	25	24
CAPF6_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPF6_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPF6_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPF6_0							
R							
0h							

Table 4-1544. ICSSM_PR1_IEP0_SLV_CAPF6_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPF6_0	R	0h	

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4.2.2.264 ICSSM_PR1_IEP0_SLV_CAPF6_REG1 Register

4.2.2.264.1 ICSSM_PR1_IEP0_SLV_CAPF6_REG1 Register (Offset = 5Ch) [reset = 0h]

Capture Fall16

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Table 4-1545. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E05Ch

Figure 4-750. ICSSM_PR1_IEP0_SLV_CAPF6_REG1 Name Register

31	30	29	28	27	26	25	24
CAPF6_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPF6_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPF6_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPF6_1							
R							
0h							

Table 4-1546. ICSSM_PR1_IEP0_SLV_CAPF6_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPF6_1	R	0h	

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4.2.2.265 ICSSM_PR1_IEP0_SLV_CAPR7_REG0 Register

4.2.2.265.1 ICSSM_PR1_IEP0_SLV_CAPR7_REG0 Register (Offset = 60h) [reset = 0h]

Capture Rise07

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Table 4-1547. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E060h

Figure 4-751. ICSSM_PR1_IEP0_SLV_CAPR7_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR7_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR7_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR7_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR7_0							
R							
0h							

Table 4-1548. ICSSM_PR1_IEP0_SLV_CAPR7_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR7_0	R	0h	

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4.2.2.266 ICSSM_PR1_IEP0_SLV_CAPR7_REG1 Register

4.2.2.266.1 ICSSM_PR1_IEP0_SLV_CAPR7_REG1 Register (Offset = 64h) [reset = 0h]

Capture Rise17

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Table 4-1549. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E064h

Figure 4-752. ICSSM_PR1_IEP0_SLV_CAPR7_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR7_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR7_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR7_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR7_1							
R							
0h							

Table 4-1550. ICSSM_PR1_IEP0_SLV_CAPR7_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR7_1	R	0h	

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4.2.2.267 ICSSM_PR1_IEP0_SLV_CAPF7_REG0 Register

4.2.2.267.1 ICSSM_PR1_IEP0_SLV_CAPF7_REG0 Register (Offset = 68h) [reset = 0h]

Capture Fall07

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Table 4-1551. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E068h

Figure 4-753. ICSSM_PR1_IEP0_SLV_CAPF7_REG0 Name Register

31	30	29	28	27	26	25	24
CAPF7_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPF7_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPF7_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPF7_0							
R							
0h							

Table 4-1552. ICSSM_PR1_IEP0_SLV_CAPF7_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPF7_0	R	0h	

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4.2.2.268 ICSSM_PR1_IEP0_SLV_CAPF7_REG1 Register

4.2.2.268.1 ICSSM_PR1_IEP0_SLV_CAPF7_REG1 Register (Offset = 6Ch) [reset = 0h]

Capture Fall17

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Table 4-1553. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E06Ch

Figure 4-754. ICSSM_PR1_IEP0_SLV_CAPF7_REG1 Name Register

31	30	29	28	27	26	25	24
CAPF7_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPF7_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPF7_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPF7_1							
R							
0h							

Table 4-1554. ICSSM_PR1_IEP0_SLV_CAPF7_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPF7_1	R	0h	

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4.2.2.269 ICSSM_PR1_IEP0_SLV_CMP_CFG_REG Register

4.2.2.269.1 ICSSM_PR1_IEP0_SLV_CMP_CFG_REG Register (Offset = 70h) [reset = 0h]

Capture Cfg

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Table 4-1555. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E070h

Figure 4-755. ICSSM_PR1_IEP0_SLV_CMP_CFG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						SHADOW_EN	CMP_EN
NONE						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
CMP_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP_EN							CMP0_RST_CNT_EN
R/W							R/W
0h							0h

Table 4-1556. ICSSM_PR1_IEP0_SLV_CMP_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	SHADOW_EN	R/W	0h	
16:1	CMP_EN	R/W	0h	
0	CMP0_RST_CNT_EN	R/W	0h	

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4.2.2.270 ICSSM_PR1_IEP0_SLV_CMP_STATUS_REG Register

4.2.2.270.1 ICSSM_PR1_IEP0_SLV_CMP_STATUS_REG Register (Offset = 74h) [reset = 0h]

Capture Status

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Table 4-1557. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E074h

Figure 4-756. ICSSM_PR1_IEP0_SLV_CMP_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CMP_STATUS							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CMP_STATUS							
R/W1TC							
0h							

Table 4-1558. ICSSM_PR1_IEP0_SLV_CMP_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CMP_STATUS	R/W1TC	0h	

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4.2.2.271 ICSSM_PR1_IEP0_SLV_CMP0_REG0 Register

4.2.2.271.1 ICSSM_PR1_IEP0_SLV_CMP0_REG0 Register (Offset = 78h) [reset = 0h]

Compare00

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Table 4-1559. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E078h

Figure 4-757. ICSSM_PR1_IEP0_SLV_CMP0_REG0 Name Register

31	30	29	28	27	26	25	24
CMP0_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP0_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP0_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP0_0							
R/W							
0h							

Table 4-1560. ICSSM_PR1_IEP0_SLV_CMP0_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP0_0	R/W	0h	

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4.2.2.272 ICSSM_PR1_IEP0_SLV_CMP0_REG1 Register

4.2.2.272.1 ICSSM_PR1_IEP0_SLV_CMP0_REG1 Register (Offset = 7Ch) [reset = 0h]

Compare10

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Table 4-1561. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E07Ch

Figure 4-758. ICSSM_PR1_IEP0_SLV_CMP0_REG1 Name Register

31	30	29	28	27	26	25	24
CMP0_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP0_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP0_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP0_1							
R/W							
0h							

Table 4-1562. ICSSM_PR1_IEP0_SLV_CMP0_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP0_1	R/W	0h	

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4.2.2.273 ICSSM_PR1_IEP0_SLV_CMP1_REG0 Register

4.2.2.273.1 ICSSM_PR1_IEP0_SLV_CMP1_REG0 Register (Offset = 80h) [reset = 0h]

Compare01

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Table 4-1563. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E080h

Figure 4-759. ICSSM_PR1_IEP0_SLV_CMP1_REG0 Name Register

31	30	29	28	27	26	25	24
CMP1_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP1_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP1_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP1_0							
R/W							
0h							

Table 4-1564. ICSSM_PR1_IEP0_SLV_CMP1_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP1_0	R/W	0h	

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4.2.2.274 ICSSM_PR1_IEP0_SLV_CMP1_REG1 Register

4.2.2.274.1 ICSSM_PR1_IEP0_SLV_CMP1_REG1 Register (Offset = 84h) [reset = 0h]

Compare11

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Table 4-1565. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E084h

Figure 4-760. ICSSM_PR1_IEP0_SLV_CMP1_REG1 Name Register

31	30	29	28	27	26	25	24
CMP1_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP1_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP1_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP1_1							
R/W							
0h							

Table 4-1566. ICSSM_PR1_IEP0_SLV_CMP1_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP1_1	R/W	0h	

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4.2.2.275 ICSSM_PR1_IEP0_SLV_CMP2_REG0 Register

4.2.2.275.1 ICSSM_PR1_IEP0_SLV_CMP2_REG0 Register (Offset = 88h) [reset = 0h]

Compare02

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Table 4-1567. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E088h

Figure 4-761. ICSSM_PR1_IEP0_SLV_CMP2_REG0 Name Register

31	30	29	28	27	26	25	24
CMP2_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP2_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP2_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP2_0							
R/W							
0h							

Table 4-1568. ICSSM_PR1_IEP0_SLV_CMP2_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP2_0	R/W	0h	

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4.2.2.276 ICSSM_PR1_IEP0_SLV_CMP2_REG1 Register

4.2.2.276.1 ICSSM_PR1_IEP0_SLV_CMP2_REG1 Register (Offset = 8Ch) [reset = 0h]

Compare12

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Table 4-1569. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E08Ch

Figure 4-762. ICSSM_PR1_IEP0_SLV_CMP2_REG1 Name Register

31	30	29	28	27	26	25	24
CMP2_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP2_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP2_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP2_1							
R/W							
0h							

Table 4-1570. ICSSM_PR1_IEP0_SLV_CMP2_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP2_1	R/W	0h	

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4.2.2.277 ICSSM_PR1_IEP0_SLV_CMP3_REG0 Register

4.2.2.277.1 ICSSM_PR1_IEP0_SLV_CMP3_REG0 Register (Offset = 90h) [reset = 0h]

Compare03

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Table 4-1571. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E090h

Figure 4-763. ICSSM_PR1_IEP0_SLV_CMP3_REG0 Name Register

31	30	29	28	27	26	25	24
CMP3_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP3_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP3_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP3_0							
R/W							
0h							

Table 4-1572. ICSSM_PR1_IEP0_SLV_CMP3_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP3_0	R/W	0h	

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4.2.2.278 ICSSM_PR1_IEP0_SLV_CMP3_REG1 Register

4.2.2.278.1 ICSSM_PR1_IEP0_SLV_CMP3_REG1 Register (Offset = 94h) [reset = 0h]

Compare13

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Table 4-1573. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E094h

Figure 4-764. ICSSM_PR1_IEP0_SLV_CMP3_REG1 Name Register

31	30	29	28	27	26	25	24
CMP3_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP3_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP3_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP3_1							
R/W							
0h							

Table 4-1574. ICSSM_PR1_IEP0_SLV_CMP3_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP3_1	R/W	0h	

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4.2.2.279 ICSSM_PR1_IEP0_SLV_CMP4_REG0 Register

4.2.2.279.1 ICSSM_PR1_IEP0_SLV_CMP4_REG0 Register (Offset = 98h) [reset = 0h]

Compare04

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Table 4-1575. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E098h

Figure 4-765. ICSSM_PR1_IEP0_SLV_CMP4_REG0 Name Register

31	30	29	28	27	26	25	24
CMP4_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP4_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP4_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP4_0							
R/W							
0h							

Table 4-1576. ICSSM_PR1_IEP0_SLV_CMP4_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP4_0	R/W	0h	

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4.2.2.280 ICSSM_PR1_IEP0_SLV_CMP4_REG1 Register

4.2.2.280.1 ICSSM_PR1_IEP0_SLV_CMP4_REG1 Register (Offset = 9Ch) [reset = 0h]

Compare14

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Table 4-1577. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E09Ch

Figure 4-766. ICSSM_PR1_IEP0_SLV_CMP4_REG1 Name Register

31	30	29	28	27	26	25	24
CMP4_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP4_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP4_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP4_1							
R/W							
0h							

Table 4-1578. ICSSM_PR1_IEP0_SLV_CMP4_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP4_1	R/W	0h	

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4.2.2.281 ICSSM_PR1_IEP0_SLV_CMP5_REG0 Register

4.2.2.281.1 ICSSM_PR1_IEP0_SLV_CMP5_REG0 Register (Offset = A0h) [reset = 0h]

Compare05

Return to Summary Table

Table 4-1579. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0A0h

Figure 4-767. ICSSM_PR1_IEP0_SLV_CMP5_REG0 Name Register

31	30	29	28	27	26	25	24
CMP5_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP5_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP5_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP5_0							
R/W							
0h							

Table 4-1580. ICSSM_PR1_IEP0_SLV_CMP5_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP5_0	R/W	0h	

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4.2.2.282 ICSSM_PR1_IEP0_SLV_CMP5_REG1 Register

4.2.2.282.1 ICSSM_PR1_IEP0_SLV_CMP5_REG1 Register (Offset = A4h) [reset = 0h]

Compare15

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Table 4-1581. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0A4h

Figure 4-768. ICSSM_PR1_IEP0_SLV_CMP5_REG1 Name Register

31	30	29	28	27	26	25	24
CMP5_1							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CMP5_1							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CMP5_1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMP5_1							
R/W							
0h							

Table 4-1582. ICSSM_PR1_IEP0_SLV_CMP5_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP5_1	R/W	0h	

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4.2.2.283 ICSSM_PR1_IEP0_SLV_CMP6_REG0 Register

4.2.2.283.1 ICSSM_PR1_IEP0_SLV_CMP6_REG0 Register (Offset = A8h) [reset = 0h]

Compare06

Return to Summary Table

Table 4-1583. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0A8h

Figure 4-769. ICSSM_PR1_IEP0_SLV_CMP6_REG0 Name Register

31	30	29	28	27	26	25	24
CMP6_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP6_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP6_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP6_0							
R/W							
0h							

Table 4-1584. ICSSM_PR1_IEP0_SLV_CMP6_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP6_0	R/W	0h	

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4.2.2.284 ICSSM_PR1_IEP0_SLV_CMP6_REG1 Register

4.2.2.284.1 ICSSM_PR1_IEP0_SLV_CMP6_REG1 Register (Offset = ACh) [reset = 0h]

Compare16

Return to Summary Table

Table 4-1585. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0ACh

Figure 4-770. ICSSM_PR1_IEP0_SLV_CMP6_REG1 Name Register

31	30	29	28	27	26	25	24
CMP6_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP6_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP6_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP6_1							
R/W							
0h							

Table 4-1586. ICSSM_PR1_IEP0_SLV_CMP6_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP6_1	R/W	0h	

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4.2.2.285 ICSSM_PR1_IEP0_SLV_CMP7_REG0 Register

4.2.2.285.1 ICSSM_PR1_IEP0_SLV_CMP7_REG0 Register (Offset = B0h) [reset = 0h]

Compare07

Return to Summary Table

Table 4-1587. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0B0h

Figure 4-771. ICSSM_PR1_IEP0_SLV_CMP7_REG0 Name Register

31	30	29	28	27	26	25	24
CMP7_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP7_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP7_0							
R/W							
0h							

Table 4-1588. ICSSM_PR1_IEP0_SLV_CMP7_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP7_0	R/W	0h	

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4.2.2.286 ICSSM_PR1_IEP0_SLV_CMP7_REG1 Register

4.2.2.286.1 ICSSM_PR1_IEP0_SLV_CMP7_REG1 Register (Offset = B4h) [reset = 0h]

Compare17

Return to Summary Table

Table 4-1589. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0B4h

Figure 4-772. ICSSM_PR1_IEP0_SLV_CMP7_REG1 Name Register

31	30	29	28	27	26	25	24
CMP7_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP7_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP7_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP7_1							
R/W							
0h							

Table 4-1590. ICSSM_PR1_IEP0_SLV_CMP7_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP7_1	R/W	0h	

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4.2.2.287 ICSSM_PR1_IEP0_SLV_RXIPG0_REG Register

4.2.2.287.1 ICSSM_PR1_IEP0_SLV_RXIPG0_REG Register (Offset = B8h) [reset = FFFF0000h]

RXIPG0

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Table 4-1591. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0B8h

Figure 4-773. ICSSM_PR1_IEP0_SLV_RXIPG0_REG Name Register

31	30	29	28	27	26	25	24
RX_MIN_IPG0							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
RX_MIN_IPG0							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
RX_IPG0							
R							
0h							
7	6	5	4	3	2	1	0
RX_IPG0							
R							
0h							

Table 4-1592. ICSSM_PR1_IEP0_SLV_RXIPG0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RX_MIN_IPG0	R/W	FFFFh	
15:0	RX_IPG0	R	0h	

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4.2.2.288 ICSSM_PR1_IEP0_SLV_RXIPG1_REG Register

4.2.2.288.1 ICSSM_PR1_IEP0_SLV_RXIPG1_REG Register (Offset = BCh) [reset = FFFF0000h]

RXIPG1

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Table 4-1593. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0BCh

Figure 4-774. ICSSM_PR1_IEP0_SLV_RXIPG1_REG Name Register

31	30	29	28	27	26	25	24
RX_MIN_IPG1							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
RX_MIN_IPG1							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
RX_IPG1							
R							
0h							
7	6	5	4	3	2	1	0
RX_IPG1							
R							
0h							

Table 4-1594. ICSSM_PR1_IEP0_SLV_RXIPG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RX_MIN_IPG1	R/W	FFFFh	
15:0	RX_IPG1	R	0h	

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4.2.2.289 ICSSM_PR1_IEP0_SLV_CMP8_REG0 Register

4.2.2.289.1 ICSSM_PR1_IEP0_SLV_CMP8_REG0 Register (Offset = C0h) [reset = 0h]

Compare08

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Table 4-1595. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0C0h

Figure 4-775. ICSSM_PR1_IEP0_SLV_CMP8_REG0 Name Register

31	30	29	28	27	26	25	24
CMP8_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP8_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP8_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP8_0							
R/W							
0h							

Table 4-1596. ICSSM_PR1_IEP0_SLV_CMP8_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP8_0	R/W	0h	

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4.2.2.290 ICSSM_PR1_IEP0_SLV_CMP8_REG1 Register

4.2.2.290.1 ICSSM_PR1_IEP0_SLV_CMP8_REG1 Register (Offset = C4h) [reset = 0h]

Compare18

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Table 4-1597. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0C4h

Figure 4-776. ICSSM_PR1_IEP0_SLV_CMP8_REG1 Name Register

31	30	29	28	27	26	25	24
CMP8_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP8_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP8_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP8_1							
R/W							
0h							

Table 4-1598. ICSSM_PR1_IEP0_SLV_CMP8_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP8_1	R/W	0h	

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4.2.2.291 ICSSM_PR1_IEP0_SLV_CMP9_REG0 Register

4.2.2.291.1 ICSSM_PR1_IEP0_SLV_CMP9_REG0 Register (Offset = C8h) [reset = 0h]

Compare09

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Table 4-1599. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0C8h

Figure 4-777. ICSSM_PR1_IEP0_SLV_CMP9_REG0 Name Register

31	30	29	28	27	26	25	24
CMP9_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP9_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP9_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP9_0							
R/W							
0h							

Table 4-1600. ICSSM_PR1_IEP0_SLV_CMP9_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP9_0	R/W	0h	

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4.2.2.292 ICSSM_PR1_IEP0_SLV_CMP9_REG1 Register

4.2.2.292.1 ICSSM_PR1_IEP0_SLV_CMP9_REG1 Register (Offset = CCh) [reset = 0h]

Compare19

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Table 4-1601. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0CCh

Figure 4-778. ICSSM_PR1_IEP0_SLV_CMP9_REG1 Name Register

31	30	29	28	27	26	25	24
CMP9_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP9_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP9_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP9_1							
R/W							
0h							

Table 4-1602. ICSSM_PR1_IEP0_SLV_CMP9_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP9_1	R/W	0h	

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4.2.2.293 ICSSM_PR1_IEP0_SLV_CMP10_REG0 Register

4.2.2.293.1 ICSSM_PR1_IEP0_SLV_CMP10_REG0 Register (Offset = D0h) [reset = 0h]

Compare010

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Table 4-1603. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0D0h

Figure 4-779. ICSSM_PR1_IEP0_SLV_CMP10_REG0 Name Register

31	30	29	28	27	26	25	24
CMP10_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP10_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP10_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP10_0							
R/W							
0h							

Table 4-1604. ICSSM_PR1_IEP0_SLV_CMP10_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP10_0	R/W	0h	

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4.2.2.294 ICSSM_PR1_IEP0_SLV_CMP10_REG1 Register

4.2.2.294.1 ICSSM_PR1_IEP0_SLV_CMP10_REG1 Register (Offset = D4h) [reset = 0h]

Compare110

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Table 4-1605. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0D4h

Figure 4-780. ICSSM_PR1_IEP0_SLV_CMP10_REG1 Name Register

31	30	29	28	27	26	25	24
CMP10_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP10_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP10_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP10_1							
R/W							
0h							

Table 4-1606. ICSSM_PR1_IEP0_SLV_CMP10_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP10_1	R/W	0h	

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4.2.2.295 ICSSM_PR1_IEP0_SLV_CMP11_REG0 Register

4.2.2.295.1 ICSSM_PR1_IEP0_SLV_CMP11_REG0 Register (Offset = D8h) [reset = 0h]

Compare011

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Table 4-1607. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0D8h

Figure 4-781. ICSSM_PR1_IEP0_SLV_CMP11_REG0 Name Register

31	30	29	28	27	26	25	24
CMP11_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP11_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP11_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP11_0							
R/W							
0h							

Table 4-1608. ICSSM_PR1_IEP0_SLV_CMP11_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP11_0	R/W	0h	

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4.2.2.296 ICSSM_PR1_IEP0_SLV_CMP11_REG1 Register

4.2.2.296.1 ICSSM_PR1_IEP0_SLV_CMP11_REG1 Register (Offset = DCh) [reset = 0h]

Compare111

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Table 4-1609. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0DCh

Figure 4-782. ICSSM_PR1_IEP0_SLV_CMP11_REG1 Name Register

31	30	29	28	27	26	25	24
CMP11_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP11_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP11_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP11_1							
R/W							
0h							

Table 4-1610. ICSSM_PR1_IEP0_SLV_CMP11_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP11_1	R/W	0h	

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4.2.2.297 ICSSM_PR1_IEP0_SLV_CMP12_REG0 Register

4.2.2.297.1 ICSSM_PR1_IEP0_SLV_CMP12_REG0 Register (Offset = E0h) [reset = 0h]

Compare012

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Table 4-1611. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0E0h

Figure 4-783. ICSSM_PR1_IEP0_SLV_CMP12_REG0 Name Register

31	30	29	28	27	26	25	24
CMP12_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP12_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP12_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP12_0							
R/W							
0h							

Table 4-1612. ICSSM_PR1_IEP0_SLV_CMP12_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP12_0	R/W	0h	

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4.2.2.298 ICSSM_PR1_IEP0_SLV_CMP12_REG1 Register

4.2.2.298.1 ICSSM_PR1_IEP0_SLV_CMP12_REG1 Register (Offset = E4h) [reset = 0h]

Compare112

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Table 4-1613. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0E4h

Figure 4-784. ICSSM_PR1_IEP0_SLV_CMP12_REG1 Name Register

31	30	29	28	27	26	25	24
CMP12_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP12_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP12_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP12_1							
R/W							
0h							

Table 4-1614. ICSSM_PR1_IEP0_SLV_CMP12_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP12_1	R/W	0h	

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4.2.2.299 ICSSM_PR1_IEP0_SLV_CMP13_REG0 Register

4.2.2.299.1 ICSSM_PR1_IEP0_SLV_CMP13_REG0 Register (Offset = E8h) [reset = 0h]

Compare013

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Table 4-1615. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0E8h

Figure 4-785. ICSSM_PR1_IEP0_SLV_CMP13_REG0 Name Register

31	30	29	28	27	26	25	24
CMP13_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP13_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP13_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP13_0							
R/W							
0h							

Table 4-1616. ICSSM_PR1_IEP0_SLV_CMP13_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP13_0	R/W	0h	

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4.2.2.300 ICSSM_PR1_IEP0_SLV_CMP13_REG1 Register

4.2.2.300.1 ICSSM_PR1_IEP0_SLV_CMP13_REG1 Register (Offset = ECh) [reset = 0h]

Compare113

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Table 4-1617. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0ECh

Figure 4-786. ICSSM_PR1_IEP0_SLV_CMP13_REG1 Name Register

31	30	29	28	27	26	25	24
CMP13_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP13_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP13_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP13_1							
R/W							
0h							

Table 4-1618. ICSSM_PR1_IEP0_SLV_CMP13_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP13_1	R/W	0h	

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4.2.2.301 ICSSM_PR1_IEP0_SLV_CMP14_REG0 Register

4.2.2.301.1 ICSSM_PR1_IEP0_SLV_CMP14_REG0 Register (Offset = F0h) [reset = 0h]

Compare014

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Table 4-1619. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0F0h

Figure 4-787. ICSSM_PR1_IEP0_SLV_CMP14_REG0 Name Register

31	30	29	28	27	26	25	24
CMP14_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP14_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP14_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP14_0							
R/W							
0h							

Table 4-1620. ICSSM_PR1_IEP0_SLV_CMP14_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP14_0	R/W	0h	

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4.2.2.302 ICSSM_PR1_IEP0_SLV_CMP14_REG1 Register

4.2.2.302.1 ICSSM_PR1_IEP0_SLV_CMP14_REG1 Register (Offset = F4h) [reset = 0h]

Compare114

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Table 4-1621. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0F4h

Figure 4-788. ICSSM_PR1_IEP0_SLV_CMP14_REG1 Name Register

31	30	29	28	27	26	25	24
CMP14_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP14_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP14_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP14_1							
R/W							
0h							

Table 4-1622. ICSSM_PR1_IEP0_SLV_CMP14_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP14_1	R/W	0h	

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4.2.2.303 ICSSM_PR1_IEP0_SLV_CMP15_REG0 Register

4.2.2.303.1 ICSSM_PR1_IEP0_SLV_CMP15_REG0 Register (Offset = F8h) [reset = 0h]

Compare015

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Table 4-1623. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0F8h

Figure 4-789. ICSSM_PR1_IEP0_SLV_CMP15_REG0 Name Register

31	30	29	28	27	26	25	24
CMP15_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP15_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP15_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP15_0							
R/W							
0h							

Table 4-1624. ICSSM_PR1_IEP0_SLV_CMP15_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP15_0	R/W	0h	

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4.2.2.304 ICSSM_PR1_IEP0_SLV_CMP15_REG1 Register

4.2.2.304.1 ICSSM_PR1_IEP0_SLV_CMP15_REG1 Register (Offset = FCh) [reset = 0h]

Compare115

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Table 4-1625. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E0FCh

Figure 4-790. ICSSM_PR1_IEP0_SLV_CMP15_REG1 Name Register

31	30	29	28	27	26	25	24
CMP15_1							
R/W							
0h							
23	22	21	20	19	18	17	16
CMP15_1							
R/W							
0h							
15	14	13	12	11	10	9	8
CMP15_1							
R/W							
0h							
7	6	5	4	3	2	1	0
CMP15_1							
R/W							
0h							

Table 4-1626. ICSSM_PR1_IEP0_SLV_CMP15_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CMP15_1	R/W	0h	

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4.2.2.305 ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG0 Register

4.2.2.305.1 ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG0 Register (Offset = 100h) [reset = 0h]

Low Counter Reset Value

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Table 4-1627. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E100h

Figure 4-791. ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG0 Name Register

31	30	29	28	27	26	25	24
RESET_VAL_0							
R/W							
0h							
23	22	21	20	19	18	17	16
RESET_VAL_0							
R/W							
0h							
15	14	13	12	11	10	9	8
RESET_VAL_0							
R/W							
0h							
7	6	5	4	3	2	1	0
RESET_VAL_0							
R/W							
0h							

Table 4-1628. ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESET_VAL_0	R/W	0h	

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4.2.2.306 ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG1 Register

4.2.2.306.1 ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG1 Register (Offset = 104h) [reset = 0h]

Low Counter Reset Value

Return to Summary Table

Table 4-1629. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E104h

Figure 4-792. ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG1 Name Register

31	30	29	28	27	26	25	24
RESET_VAL_1							
R/W							
0h							
23	22	21	20	19	18	17	16
RESET_VAL_1							
R/W							
0h							
15	14	13	12	11	10	9	8
RESET_VAL_1							
R/W							
0h							
7	6	5	4	3	2	1	0
RESET_VAL_1							
R/W							
0h							

Table 4-1630. ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESET_VAL_1	R/W	0h	

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4.2.2.307 ICSSM_PR1_IEP0_SLV_PWM_REG Register

4.2.2.307.1 ICSSM_PR1_IEP0_SLV_PWM_REG Register (Offset = 108h) [reset = 0h]

PWM

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Table 4-1631. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E108h

Figure 4-793. ICSSM_PR1_IEP0_SLV_PWM_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				PWM3_HIT	PWM3_RST_CNT_EN	PWM0_HIT	PWM0_RST_CNT_EN
NONE				R/W1TC	R/W	R/W1TC	R/W
0h				0h	0h	0h	0h

Table 4-1632. ICSSM_PR1_IEP0_SLV_PWM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	PWM3_HIT	R/W1TC	0h	
2	PWM3_RST_CNT_EN	R/W	0h	
1	PWM0_HIT	R/W1TC	0h	
0	PWM0_RST_CNT_EN	R/W	0h	

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4.2.2.308 ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG0 Register

4.2.2.308.1 ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG0 Register (Offset = 10Ch) [reset = 0h]

Capture Big Indian Rise00

Return to Summary Table

Table 4-1633. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E10Ch

Figure 4-794. ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR0_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR0_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR0_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR0_0							
R							
0h							

Table 4-1634. ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR0_0	R	0h	

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4.2.2.309 ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG1 Register

4.2.2.309.1 ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG1 Register (Offset = 110h) [reset = 0h]

Capture Big Indian Rise10

Return to Summary Table

Table 4-1635. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E110h

Figure 4-795. ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR0_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR0_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR0_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR0_1							
R							
0h							

Table 4-1636. ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR0_1	R	0h	

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4.2.2.310 ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG0 Register

4.2.2.310.1 ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG0 Register (Offset = 114h) [reset = 0h]

Capture Big Indian Rise01

Return to Summary Table

Table 4-1637. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E114h

Figure 4-796. ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR1_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR1_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR1_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR1_0							
R							
0h							

Table 4-1638. ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR1_0	R	0h	

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4.2.2.311 ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG1 Register

4.2.2.311.1 ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG1 Register (Offset = 118h) [reset = 0h]

Capture Big Indian Rise11

Return to Summary Table

Table 4-1639. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E118h

Figure 4-797. ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR1_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR1_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR1_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR1_1							
R							
0h							

Table 4-1640. ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR1_1	R	0h	

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4.2.2.312 ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG0 Register

4.2.2.312.1 ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG0 Register (Offset = 11Ch) [reset = 0h]

Capture Big Indian Rise02

Return to Summary Table

Table 4-1641. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E11Ch

Figure 4-798. ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR2_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR2_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR2_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR2_0							
R							
0h							

Table 4-1642. ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR2_0	R	0h	

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4.2.2.313 ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG1 Register

4.2.2.313.1 ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG1 Register (Offset = 120h) [reset = 0h]

Capture Big Indian Rise12

Return to Summary Table

Table 4-1643. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E120h

Figure 4-799. ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR2_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR2_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR2_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR2_1							
R							
0h							

Table 4-1644. ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR2_1	R	0h	

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4.2.2.314 ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG0 Register

4.2.2.314.1 ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG0 Register (Offset = 124h) [reset = 0h]

Capture Big Indian Rise03

Return to Summary Table

Table 4-1645. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E124h

Figure 4-800. ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR3_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR3_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR3_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR3_0							
R							
0h							

Table 4-1646. ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR3_0	R	0h	

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4.2.2.315 ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG1 Register

4.2.2.315.1 ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG1 Register (Offset = 128h) [reset = 0h]

Capture Big Indian Rise13

Return to Summary Table

Table 4-1647. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E128h

Figure 4-801. ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR3_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR3_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR3_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR3_1							
R							
0h							

Table 4-1648. ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR3_1	R	0h	

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4.2.2.316 ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG0 Register

4.2.2.316.1 ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG0 Register (Offset = 12Ch) [reset = 0h]

Capture Big Indian Rise04

Return to Summary Table

Table 4-1649. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E12Ch

Figure 4-802. ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR4_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR4_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR4_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR4_0							
R							
0h							

Table 4-1650. ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR4_0	R	0h	

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4.2.2.317 ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG1 Register

4.2.2.317.1 ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG1 Register (Offset = 130h) [reset = 0h]

Capture Big Indian Rise14

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Table 4-1651. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E130h

Figure 4-803. ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR4_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR4_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR4_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR4_1							
R							
0h							

Table 4-1652. ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR4_1	R	0h	

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4.2.2.318 ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG0 Register

4.2.2.318.1 ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG0 Register (Offset = 134h) [reset = 0h]

Capture Big Indian Rise05

Return to Summary Table

Table 4-1653. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E134h

Figure 4-804. ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR5_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR5_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR5_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR5_0							
R							
0h							

Table 4-1654. ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR5_0	R	0h	

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4.2.2.319 ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG1 Register

4.2.2.319.1 ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG1 Register (Offset = 138h) [reset = 0h]

Capture Big Indian Rise15

Return to Summary Table

Table 4-1655. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E138h

Figure 4-805. ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR5_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR5_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR5_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR5_1							
R							
0h							

Table 4-1656. ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR5_1	R	0h	

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4.2.2.320 ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG0 Register

4.2.2.320.1 ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG0 Register (Offset = 13Ch) [reset = 0h]

Capture Big Indian Rise06

Return to Summary Table

Table 4-1657. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E13Ch

Figure 4-806. ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR6_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR6_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR6_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR6_0							
R							
0h							

Table 4-1658. ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR6_0	R	0h	

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4.2.2.321 ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG1 Register

4.2.2.321.1 ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG1 Register (Offset = 140h) [reset = 0h]

Capture Big Indian Rise16

Return to Summary Table

Table 4-1659. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E140h

Figure 4-807. ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR6_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR6_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR6_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR6_1							
R							
0h							

Table 4-1660. ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR6_1	R	0h	

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4.2.2.322 ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG0 Register

4.2.2.322.1 ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG0 Register (Offset = 144h) [reset = 0h]

Capture Big Indian Fall06

Return to Summary Table

Table 4-1661. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E144h

Figure 4-808. ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG0 Name Register

31	30	29	28	27	26	25	24
CAPF6_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPF6_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPF6_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPF6_0							
R							
0h							

Table 4-1662. ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPF6_0	R	0h	

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4.2.2.323 ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG1 Register

4.2.2.323.1 ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG1 Register (Offset = 148h) [reset = 0h]

Capture Big Indian Fall16

Return to Summary Table

Table 4-1663. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E148h

Figure 4-809. ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG1 Name Register

31	30	29	28	27	26	25	24
CAPF6_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPF6_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPF6_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPF6_1							
R							
0h							

Table 4-1664. ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPF6_1	R	0h	

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4.2.2.324 ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG0 Register

4.2.2.324.1 ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG0 Register (Offset = 14Ch) [reset = 0h]

Capture Big Indian Rise07

Return to Summary Table

Table 4-1665. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E14Ch

Figure 4-810. ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG0 Name Register

31	30	29	28	27	26	25	24
CAPR7_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPR7_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPR7_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPR7_0							
R							
0h							

Table 4-1666. ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR7_0	R	0h	

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4.2.2.325 ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG1 Register

4.2.2.325.1 ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG1 Register (Offset = 150h) [reset = 0h]

Capture Big Indian Rise17

Return to Summary Table

Table 4-1667. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E150h

Figure 4-811. ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG1 Name Register

31	30	29	28	27	26	25	24
CAPR7_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPR7_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPR7_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPR7_1							
R							
0h							

Table 4-1668. ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPR7_1	R	0h	

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4.2.2.326 ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG0 Register

4.2.2.326.1 ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG0 Register (Offset = 154h) [reset = 0h]

Capture Big Indian Fall07

Return to Summary Table

Table 4-1669. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E154h

Figure 4-812. ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG0 Name Register

31	30	29	28	27	26	25	24
CAPF7_0							
R							
0h							
23	22	21	20	19	18	17	16
CAPF7_0							
R							
0h							
15	14	13	12	11	10	9	8
CAPF7_0							
R							
0h							
7	6	5	4	3	2	1	0
CAPF7_0							
R							
0h							

Table 4-1670. ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPF7_0	R	0h	

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4.2.2.327 ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG1 Register

4.2.2.327.1 ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG1 Register (Offset = 158h) [reset = 0h]

Capture Big Indian Fall17

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Table 4-1671. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E158h

Figure 4-813. ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG1 Name Register

31	30	29	28	27	26	25	24
CAPF7_1							
R							
0h							
23	22	21	20	19	18	17	16
CAPF7_1							
R							
0h							
15	14	13	12	11	10	9	8
CAPF7_1							
R							
0h							
7	6	5	4	3	2	1	0
CAPF7_1							
R							
0h							

Table 4-1672. ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAPF7_1	R	0h	

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4.2.2.328 ICSSM_PR1_IEP0_SLV_SYNC_CTRL_REG Register

4.2.2.328.1 ICSSM_PR1_IEP0_SLV_SYNC_CTRL_REG Register (Offset = 180h) [reset = 0h]

Sync Ctrl

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Table 4-1673. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E180h

Figure 4-814. ICSSM_PR1_IEP0_SLV_SYNC_CTRL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					SYNC1_OUT_NV_EN	SYNC0_OUT_NV_EN	SYNC1_IND_EN
NONE					R/W	R/W	R/W
0h					0h	0h	0h
7	6	5	4	3	2	1	0
SYNC1_CYCLIC_EN	SYNC1_ACK_EN	SYNC0_CYCLIC_EN	SYNC0_ACK_EN	RESERVED	SYNC1_EN	SYNC0_EN	SYNC_EN
R/W	R/W	R/W	R/W	NONE	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1674. ICSSM_PR1_IEP0_SLV_SYNC_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	SYNC1_OUT_NV_EN	R/W	0h	
9	SYNC0_OUT_NV_EN	R/W	0h	
8	SYNC1_IND_EN	R/W	0h	
7	SYNC1_CYCLIC_EN	R/W	0h	
6	SYNC1_ACK_EN	R/W	0h	
5	SYNC0_CYCLIC_EN	R/W	0h	
4	SYNC0_ACK_EN	R/W	0h	
3	RESERVED	NONE	0h	Reserved
2	SYNC1_EN	R/W	0h	
1	SYNC0_EN	R/W	0h	
0	SYNC_EN	R/W	0h	

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4.2.2.329 ICSSM_PR1_IEP0_SLV_SYNC_FIRST_STAT_REG Register

4.2.2.329.1 ICSSM_PR1_IEP0_SLV_SYNC_FIRST_STAT_REG Register (Offset = 184h) [reset = 0h]

Sync Ctrl

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Table 4-1675. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E184h

Figure 4-815. ICSSM_PR1_IEP0_SLV_SYNC_FIRST_STAT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						FIRST_SYNC1	FIRST_SYNC0
NONE						R	R
0h						0h	0h

Table 4-1676. ICSSM_PR1_IEP0_SLV_SYNC_FIRST_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	FIRST_SYNC1	R	0h	
0	FIRST_SYNC0	R	0h	

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4.2.2.330 ICSSM_PR1_IEP0_SLV_SYNC0_STAT_REG Register

4.2.2.330.1 ICSSM_PR1_IEP0_SLV_SYNC0_STAT_REG Register (Offset = 188h) [reset = 0h]

Sync Ctrl

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Table 4-1677. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E188h

Figure 4-816. ICSSM_PR1_IEP0_SLV_SYNC0_STAT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SYNC0_PEND
NONE							R
0h							0h

Table 4-1678. ICSSM_PR1_IEP0_SLV_SYNC0_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SYNC0_PEND	R	0h	

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4.2.2.331 ICSSM_PR1_IEP0_SLV_SYNC1_STAT_REG Register

4.2.2.331.1 ICSSM_PR1_IEP0_SLV_SYNC1_STAT_REG Register (Offset = 18Ch) [reset = 0h]

Sync Ctrl

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Table 4-1679. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E18Ch

Figure 4-817. ICSSM_PR1_IEP0_SLV_SYNC1_STAT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SYNC1_PEND
NONE							R
0h							0h

Table 4-1680. ICSSM_PR1_IEP0_SLV_SYNC1_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SYNC1_PEND	R	0h	

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4.2.2.332 ICSSM_PR1_IEP0_SLV_SYNC_PWIDTH_REG Register

4.2.2.332.1 ICSSM_PR1_IEP0_SLV_SYNC_PWIDTH_REG Register (Offset = 190h) [reset = 0h]

Sync Ctrl

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Table 4-1681. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E190h

Figure 4-818. ICSSM_PR1_IEP0_SLV_SYNC_PWIDTH_REG Name Register

31	30	29	28	27	26	25	24
SYNC_HPW							
R/W							
0h							
23	22	21	20	19	18	17	16
SYNC_HPW							
R/W							
0h							
15	14	13	12	11	10	9	8
SYNC_HPW							
R/W							
0h							
7	6	5	4	3	2	1	0
SYNC_HPW							
R/W							
0h							

Table 4-1682. ICSSM_PR1_IEP0_SLV_SYNC_PWIDTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNC_HPW	R/W	0h	

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4.2.2.333 ICSSM_PR1_IEP0_SLV_SYNC0_PERIOD_REG Register

4.2.2.333.1 ICSSM_PR1_IEP0_SLV_SYNC0_PERIOD_REG Register (Offset = 194h) [reset = 1h]

Sync Ctrl

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Table 4-1683. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E194h

Figure 4-819. ICSSM_PR1_IEP0_SLV_SYNC0_PERIOD_REG Name Register

31	30	29	28	27	26	25	24
SYNC0_PERIOD							
R/W							
1h							
23	22	21	20	19	18	17	16
SYNC0_PERIOD							
R/W							
1h							
15	14	13	12	11	10	9	8
SYNC0_PERIOD							
R/W							
1h							
7	6	5	4	3	2	1	0
SYNC0_PERIOD							
R/W							
1h							

Table 4-1684. ICSSM_PR1_IEP0_SLV_SYNC0_PERIOD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNC0_PERIOD	R/W	1h	

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4.2.2.334 ICSSM_PR1_IEP0_SLV_SYNC1_DELAY_REG Register

4.2.2.334.1 ICSSM_PR1_IEP0_SLV_SYNC1_DELAY_REG Register (Offset = 198h) [reset = 0h]

Sync Ctrl

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Table 4-1685. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E198h

Figure 4-820. ICSSM_PR1_IEP0_SLV_SYNC1_DELAY_REG Name Register

31	30	29	28	27	26	25	24
SYNC1_DELAY							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SYNC1_DELAY							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SYNC1_DELAY							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYNC1_DELAY							
R/W							
0h							

Table 4-1686. ICSSM_PR1_IEP0_SLV_SYNC1_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNC1_DELAY	R/W	0h	

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4.2.2.335 ICSSM_PR1_IEP0_SLV_SYNC_START_REG Register

4.2.2.335.1 ICSSM_PR1_IEP0_SLV_SYNC_START_REG Register (Offset = 19Ch) [reset = 0h]

Sync Ctrl

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Table 4-1687. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E19Ch

Figure 4-821. ICSSM_PR1_IEP0_SLV_SYNC_START_REG Name Register

31	30	29	28	27	26	25	24
SYNC_START							
R/W							
0h							
23	22	21	20	19	18	17	16
SYNC_START							
R/W							
0h							
15	14	13	12	11	10	9	8
SYNC_START							
R/W							
0h							
7	6	5	4	3	2	1	0
SYNC_START							
R/W							
0h							

Table 4-1688. ICSSM_PR1_IEP0_SLV_SYNC_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNC_START	R/W	0h	

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4.2.2.336 ICSSM_PR1_IEP0_SLV_WD_PREDIV_REG Register

4.2.2.336.1 ICSSM_PR1_IEP0_SLV_WD_PREDIV_REG Register (Offset = 200h) [reset = 4E20h]

WD

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Table 4-1689. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E200h

Figure 4-822. ICSSM_PR1_IEP0_SLV_WD_PREDIV_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PRE_DIV							
R/W							
4E20h							
7	6	5	4	3	2	1	0
PRE_DIV							
R/W							
4E20h							

Table 4-1690. ICSSM_PR1_IEP0_SLV_WD_PREDIV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PRE_DIV	R/W	4E20h	

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4.2.2.337 ICSSM_PR1_IEP0_SLV_PDI_WD_TIM_REG Register

4.2.2.337.1 ICSSM_PR1_IEP0_SLV_PDI_WD_TIM_REG Register (Offset = 204h) [reset = 3E8h]

WD

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Table 4-1691. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E204h

Figure 4-823. ICSSM_PR1_IEP0_SLV_PDI_WD_TIM_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PDI_WD_TIME							
R/W							
3E8h							
7	6	5	4	3	2	1	0
PDI_WD_TIME							
R/W							
3E8h							

Table 4-1692. ICSSM_PR1_IEP0_SLV_PDI_WD_TIM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PDI_WD_TIME	R/W	3E8h	

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4.2.2.338 ICSSM_PR1_IEP0_SLV_PD_WD_TIM_REG Register

4.2.2.338.1 ICSSM_PR1_IEP0_SLV_PD_WD_TIM_REG Register (Offset = 208h) [reset = 3E8h]

WD

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Table 4-1693. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E208h

Figure 4-824. ICSSM_PR1_IEP0_SLV_PD_WD_TIM_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PD_WD_TIME							
R/W							
3E8h							
7	6	5	4	3	2	1	0
PD_WD_TIME							
R/W							
3E8h							

Table 4-1694. ICSSM_PR1_IEP0_SLV_PD_WD_TIM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	PD_WD_TIME	R/W	3E8h	

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4.2.2.339 ICSSM_PR1_IEP0_SLV_WD_STATUS_REG Register

4.2.2.339.1 ICSSM_PR1_IEP0_SLV_WD_STATUS_REG Register (Offset = 20Ch) [reset = 10001h]

WD

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Table 4-1695. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E20Ch

Figure 4-825. ICSSM_PR1_IEP0_SLV_WD_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							PDI_WD_STAT
NONE							R
0h							1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							PD_WD_STAT
NONE							R
0h							1h

Table 4-1696. ICSSM_PR1_IEP0_SLV_WD_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PDI_WD_STAT	R	1h	
15:1	RESERVED	NONE	0h	Reserved
0	PD_WD_STAT	R	1h	

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4.2.2.340 ICSSM_PR1_IEP0_SLV_WD_EXP_CNT_REG Register

4.2.2.340.1 ICSSM_PR1_IEP0_SLV_WD_EXP_CNT_REG Register (Offset = 210h) [reset = 0h]

WD

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Table 4-1697. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E210h

Figure 4-826. ICSSM_PR1_IEP0_SLV_WD_EXP_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PD_EXP_CNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PDI_EXP_CNT							
R/W							
0h							

Table 4-1698. ICSSM_PR1_IEP0_SLV_WD_EXP_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	PD_EXP_CNT	R/W	0h	
7:0	PDI_EXP_CNT	R/W	0h	

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4.2.2.341 ICSSM_PR1_IEP0_SLV_WD_CTRL_REG Register

4.2.2.341.1 ICSSM_PR1_IEP0_SLV_WD_CTRL_REG Register (Offset = 214h) [reset = 0h]

WD

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Table 4-1699. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E214h

Figure 4-827. ICSSM_PR1_IEP0_SLV_WD_CTRL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							PDI_WD_EN
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							PD_WD_EN
NONE							R/W
0h							0h

Table 4-1700. ICSSM_PR1_IEP0_SLV_WD_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	PDI_WD_EN	R/W	0h	
15:1	RESERVED	NONE	0h	Reserved
0	PD_WD_EN	R/W	0h	

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4.2.2.342 ICSSM_PR1_IEP0_SLV_DIGIO_CTRL_REG Register

4.2.2.342.1 ICSSM_PR1_IEP0_SLV_DIGIO_CTRL_REG Register (Offset = 300h) [reset = 4h]

DIGIO

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Table 4-1701. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E300h

Figure 4-828. ICSSM_PR1_IEP0_SLV_DIGIO_CTRL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUT_MODE		IN_MODE		WD_MODE	BIDI_MODE	OUTVALID_MODE	OUTVALID_POL
R/W		R/W		R/W	R	R/W	R
0h		0h		0h	1h	0h	0h

Table 4-1702. ICSSM_PR1_IEP0_SLV_DIGIO_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	OUT_MODE	R/W	0h	
5:4	IN_MODE	R/W	0h	
3	WD_MODE	R/W	0h	
2	BIDI_MODE	R	1h	
1	OUTVALID_MODE	R/W	0h	
0	OUTVALID_POL	R	0h	

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4.2.2.343 ICSSM_PR1_IEP0_SLV_DIGIO_STATUS_REG Register

4.2.2.343.1 ICSSM_PR1_IEP0_SLV_DIGIO_STATUS_REG Register (Offset = 304h) [reset = 0h]

DIGIO

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Table 4-1703. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E304h

Figure 4-829. ICSSM_PR1_IEP0_SLV_DIGIO_STATUS_REG Name Register

31	30	29	28	27	26	25	24
DIGIO_STAT							
R							
0h							
23	22	21	20	19	18	17	16
DIGIO_STAT							
R							
0h							
15	14	13	12	11	10	9	8
DIGIO_STAT							
R							
0h							
7	6	5	4	3	2	1	0
DIGIO_STAT							
R							
0h							

Table 4-1704. ICSSM_PR1_IEP0_SLV_DIGIO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DIGIO_STAT	R	0h	

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4.2.2.344 ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_REG Register

4.2.2.344.1 ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_REG Register (Offset = 308h) [reset = 0h]

DIGIO

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Table 4-1705. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E308h

Figure 4-830. ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_REG Name Register

31	30	29	28	27	26	25	24
DATA_IN							
R							
0h							
23	22	21	20	19	18	17	16
DATA_IN							
R							
0h							
15	14	13	12	11	10	9	8
DATA_IN							
R							
0h							
7	6	5	4	3	2	1	0
DATA_IN							
R							
0h							

Table 4-1706. ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_IN	R	0h	

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4.2.2.345 ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_RAW_REG Register

4.2.2.345.1 ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_RAW_REG Register (Offset = 30Ch) [reset = 0h]

DIGIO

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Table 4-1707. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E30Ch

Figure 4-831. ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_RAW_REG Name Register

31	30	29	28	27	26	25	24
DATA_IN_RAW							
R							
0h							
23	22	21	20	19	18	17	16
DATA_IN_RAW							
R							
0h							
15	14	13	12	11	10	9	8
DATA_IN_RAW							
R							
0h							
7	6	5	4	3	2	1	0
DATA_IN_RAW							
R							
0h							

Table 4-1708. ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_IN_RAW	R	0h	

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4.2.2.346 ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_REG Register

4.2.2.346.1 ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_REG Register (Offset = 310h) [reset = 0h]

DIGIO

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Table 4-1709. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E310h

Figure 4-832. ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_REG Name Register

31	30	29	28	27	26	25	24
DATA_OUT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DATA_OUT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA_OUT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA_OUT							
R/W							
0h							

Table 4-1710. ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_OUT	R/W	0h	

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4.2.2.347 ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_EN_REG Register

4.2.2.347.1 ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_EN_REG Register (Offset = 314h) [reset = 0h]

DIGIO

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Table 4-1711. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E314h

Figure 4-833. ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_EN_REG Name Register

31	30	29	28	27	26	25	24
DATA_OUT_EN							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_OUT_EN							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_OUT_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_OUT_EN							
R/W							
0h							

Table 4-1712. ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_OUT_EN	R/W	0h	

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4.2.2.348 ICSSM_PR1_IEP0_SLV_DIGIO_EXP_REG Register

4.2.2.348.1 ICSSM_PR1_IEP0_SLV_DIGIO_EXP_REG Register (Offset = 318h) [reset = 20h]

DIGIO

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Table 4-1713. Instance Table

Instance Name	Physical Address
ICSSM0	4802 E318h

Figure 4-834. ICSSM_PR1_IEP0_SLV_DIGIO_EXP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		EOF_SEL	SOF_SEL	SOF_DLY			
NONE		R/W	R/W	R/W			
0h		0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OUTVALID_DLY				RESERVED	SW_OUTVALID	OUTVALID_OVR_EN	SW_DATA_OUT_UP
R/W				NONE	R/W	R/W	R/W
2h				0h	0h	0h	0h

Table 4-1714. ICSSM_PR1_IEP0_SLV_DIGIO_EXP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13	EOF_SEL	R/W	0h	
12	SOF_SEL	R/W	0h	
11:8	SOF_DLY	R/W	0h	
7:4	OUTVALID_DLY	R/W	2h	
3	RESERVED	NONE	0h	Reserved
2	SW_OUTVALID	R/W	0h	
1	OUTVALID_OVR_EN	R/W	0h	
0	SW_DATA_OUT_UP	R/W	0h	

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4.2.2.349 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_TSCNT Register

4.2.2.349.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_TSCNT Register (Offset = 0h) [reset = 0h]

TIME STAMP COUNTER REGISTER.

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Table 4-1715. Instance Table

Instance Name	Physical Address
ICSSM0	4803 0000h

Figure 4-835. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_TSCNT Name Register

31	30	29	28	27	26	25	24
TSCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
TSCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
TSCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
TSCNT							
R/W							
0h							

Table 4-1716. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_TSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TSCNT	R/W	0h	ACTIVE 32 BIT COUNTER REGISTER WHICH IS USED AS THE CAPTURE TIME-BASE

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4.2.2.350 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CNTPHS Register

4.2.2.350.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CNTPHS Register (Offset = 4h) [reset = 0h]

COUNTER PHASE CONTROL REGISTER.

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Table 4-1717. Instance Table

Instance Name	Physical Address
ICSSM0	4803 0004h

Figure 4-836. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CNTPHS Name Register

31	30	29	28	27	26	25	24
CNTPHS							
R/W							
0h							
23	22	21	20	19	18	17	16
CNTPHS							
R/W							
0h							
15	14	13	12	11	10	9	8
CNTPHS							
R/W							
0h							
7	6	5	4	3	2	1	0
CNTPHS							
R/W							
0h							

Table 4-1718. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CNTPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CNTPHS	R/W	0h	COUNTER PHASE VALUE REGISTER THAT CAN BE PROGRAMMED FOR PHASE LAG/LEAD THIS REGISTER SHADOWS TSCNT AND IS LOADED INTO TSCNT UPON EITHER A SYNCI EVENT OR S/W FORCE VIA A CONTROL BITUSED TO ACHIEVE PHASE CONTROL SYNC WITH RESPECT TO OTHER ECAP AND EPWM TIME-BASES

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4.2.2.351 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP1 Register

4.2.2.351.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP1 Register (Offset = 8h) [reset = 0h]

CAPTURE-1 REGISTER.

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Table 4-1719. Instance Table

Instance Name	Physical Address
ICSSM0	4803 0008h

Figure 4-837. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP1 Name Register

31	30	29	28	27	26	25	24
CAP1							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP1							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP1							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP1							
R/W							
0h							

Table 4-1720. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP1	R/W	0h	THIS REGISTER CAN BE LOADED [WRITTEN] BY :TIME-STAMP [IE COUNTER VALUE] DURING A CAPTURE EVENTS/W MAY BE USEFUL FOR TEST PURPOSES / INITIALISATIONAPRD SHADOW REGISTER [IE CAP3] WHEN USED IN APWM MODE

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4.2.2.352 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP2 Register

4.2.2.352.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP2 Register (Offset = Ch) [reset = 0h]

CAPTURE-2 REGISTER.

Return to Summary Table

Table 4-1721. Instance Table

Instance Name	Physical Address
ICSSM0	4803 000Ch

Figure 4-838. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP2 Name Register

31	30	29	28	27	26	25	24
CAP2							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP2							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP2							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP2							
R/W							
0h							

Table 4-1722. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP2	R/W	0h	THIS REGISTER CAN BE LOADED [WRITTEN] BY :TIME-STAMP [IE COUNTER VALUE] DURING A CAPTURE EVENTS/W MAY BE USEFUL FOR TEST PURPOSESACMP SHADOW REGISTER [IE CAP4] WHEN USED IN APWM MODE

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4.2.2.353 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP3 Register

4.2.2.353.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP3 Register (Offset = 10h) [reset = 0h]

CAPTURE-3 REGISTER.

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Table 4-1723. Instance Table

Instance Name	Physical Address
ICSSM0	4803 0010h

Figure 4-839. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP3 Name Register

31	30	29	28	27	26	25	24
CAP3							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP3							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP3							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP3							
R/W							
0h							

Table 4-1724. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP3	R/W	0h	IN CMP MODE THIS IS A TIME-STAMP CAPTURE REGISTERIN APMW MODE THIS IS THE PERIOD SHADOW [APER] REGISTER USER UPDATES THE PWM PERIOD VALUE VIA THIS REGISTER IN THIS MODE CAP3 [APRD] SHADOWS CAP1

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4.2.2.354 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP4 Register

4.2.2.354.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP4 Register (Offset = 14h) [reset = 0h]

CAPTURE-4 REGISTER.

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Table 4-1725. Instance Table

Instance Name	Physical Address
ICSSM0	4803 0014h

Figure 4-840. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP4 Name Register

31	30	29	28	27	26	25	24
CAP4							
R/W							
0h							
23	22	21	20	19	18	17	16
CAP4							
R/W							
0h							
15	14	13	12	11	10	9	8
CAP4							
R/W							
0h							
7	6	5	4	3	2	1	0
CAP4							
R/W							
0h							

Table 4-1726. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAP4	R/W	0h	IN CMP MODE THIS IS A TIME-STAMP CAPTURE REGISTERIN APMW MODE THIS IS THE COMPARE SHADOW [ACMP] REGISTER USER UPDATES THE PWM COMPARE VALUE VIA THIS REGISTER IN THIS MODE CAP4 [ACMP] SHADOWS CAP2

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4.2.2.355 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCTL2_ECCTL1 Register

4.2.2.355.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCTL2_ECCTL1 Register (Offset = 28h) [reset = 60000h]

ECAP CONTROL REGISTER 1

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Table 4-1727. Instance Table

Instance Name	Physical Address
ICSSM0	4803 0028h

Figure 4-841. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCTL2_ECCTL1 Name Register

31	30	29	28	27	26	25	24
FILTER					APWMPOL	CAP_APWM	SWSYNC
R					R/W	R/W	R/W
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SYNCO_SEL		SYNCI_EN	TSCNTSTP	REARM_RESET	STOPVALUE		CONT_ONESHT
R/W		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	3h		0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FREE	SOFT	EVTFLTPS					CAPLDEN
R/W	R/W	R/W					R/W
0h	0h	0h					0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1728. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCTL2_ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	FILTER	R	0h	
26	APWMPOL	R/W	0h	APWM OUTPUT POLARITY SELECT:0OUTPUT IS ACTIVE HIGH [IE COMPARE VALUE DEFINES HIGH TIME]1OUTPUT IS ACTIVE LOW [IE COMPARE VALUE DEFINES LOW TIME]NOTE: THIS IS APPLICABLE ONLY IN APWM OPERATING MODE
25	CAP_APWM	R/W	0h	CAP/APWM OPERATING MODE SELECT:0ECAP MODULE OPERATES IN CAPTURE MODETHIS MODE FORCES THE FOLLOWING CONFIGURATION:1] INHIBITS TSCNT RESETS VIA PRD_EQ EVENT2] INHIBITS SHADOW LOADS ON CAP1 &
24	SWSYNC	R/W	0h	SOFTWARE FORCED COUNTER [TSCNT] SYNCING:0WRITING A ZERO HAS NO EFFECT WILL ALWAYS RETURN A ZERO1WRITING A ONE WILL FORCE A TSCNT SHADOW LOAD OF CURRENT ECAP MODULE AND ANY ECAP MODULES DOWN-STREAM PROVIDING THE SYNCO_SEL BITS ARE 0,0 AFTER WRITING A ONE THIS BIT RETURNS TO A ZERONOTE: THIS PROVIDES A CONVENIENT S/W METHOD TO SYNCHRONIZE SOME OR ALL ECAP TIMEBASES IN APWM MODE THE SYNCING CAN ALSO BE DONE VIA THE PRD_EQ EVENT

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Table 4-1728. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCTL2_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	SYNCO_SEL	R/W	0h	SYNC-OUT SELECT:0,0SELECT SYNC-IN EVENT TO BE THE SYNC-OUT SIGNAL [PASS THROUGH]0,1SELECT PRD_EQ EVENT TO BE THE SYNC-OUT SIGNAL1,0DISABLE SYNC OUT SIGNAL1,1DISABLE SYNC OUT SIGNALNOTE: SELECTION PRD_EQ IS MEANINGFUL ONLY IN APWM MODE, HOWEVER CAN STILL BE CHOSEN IN CAP MODE IF USER BELIEVES IT TO BE USEFUL
21	SYNCI_EN	R/W	0h	COUNTER [TSCNT] SYNC-IN SELECT MODE:0DISABLE SYNC-IN OPTION1ENABLE COUNTER [TSCNT] TO BE LOADED FROM CNTPHS REGISTER UPON EITHER A SYNCI SIGNAL OR A S/W FORCE EVENT
20	TSCNTSTP	R/W	0h	COUNTER STOP [FREEZE] CONTROL:0COUNTER STOPPED1COUNTER FREE RUNNING
19	REARM_RESET	R/W	0h	ONE-SHOT RE-ARMING, IE WAIT FOR STOP TRIGGER:WRITING A ONE ARMS THE ONE-SHOT SEQUENCE, IE:1] RESETS THE MOD4 COUNTER TO ZERO2] UN-FREEZES THE MOD4 COUNTER3] ENABLES CAPTURE REGISTER LOADSWRITING A ZERO HAS NO EFFECT ALWAYS RETURNS A 0NOTE: THE RE-ARM FUNCTION IS VALID IN ONESHT OR CONTINOUS MODE
18:17	STOPVALUE	R/W	3h	STOP VALUE FOR ONE-SHOT MODE:THIS IS THE NUMBER [BETWEEN 1-4] OF CAPTURES ALLOWED TO OCCUR BEFORE THE CAP[1-4] REGISTERS ARE FROZEN, IECAPTURE SEQUENCE IS STOPPED0,0STOP AFTER CAPTURE EVENT 10,1STOP AFTER CAPTURE EVENT 21,0STOP AFTER CAPTURE EVENT 31,1STOP AFTER CAPTURE EVENT 4NOTES: [1] STOPVALUE IS COMPARED TO MOD4 COUNTER, WHEN EQUAL, 2 ACTIONS OCCUR:1] MOD4 COUNTER IS STOPPED [FROZEN]2] CAPTURE REGISTER LOADS ARE INHIBITED[2] IN ONE SHOT MODE, FURTHER INTERRUPT EVENTS ARE BLOCKED UNTIL WE RE-ARM, ONCE THE NUMBER OF EVENTS CAPTURED HAS BEEN REACHED
16	CONT_ONESHT	R/W	0h	CONTINUOUS OR ONESHOT MODE CONTROL:[APPLICABLE ONLY IN CAPTURE MODE]0OPERATE IN CONTINUOUS MODE1OPERATE IN ONE-SHOT MODE
15	FREE	R/W	0h	EMULATION CONTROL0,0 TSCNT COUNTER STOPS IMMEDIATELY ON EMULATION SUSPEND0,1 TSCNT COUNTER RUNS UNTIL = 01,X TSCNT COUNTER IS UNAFFECTED BY EMULATION SUSPEND [RUN FREE]
14	SOFT	R/W	0h	EMULATION CONTROL0,0 TSCNT COUNTER STOPS IMMEDIATELY ON EMULATION SUSPEND0,1 TSCNT COUNTER RUNS UNTIL = 01,X TSCNT COUNTER IS UNAFFECTED BY EMULATION SUSPEND [RUN FREE]
13:9	EVTFLTPS	R/W	0h	EVENT FILTER PRESCALE SELECT:0,0,0,0,0DIVIDE BY 1 [IE NO PRESCALE, BY-PASS THE PRESCALER]0,0,0,0,1DIVIDE BY 20,0,0,1,0DIVIDE BY 40,0,0,1,1DIVIDE BY 60,0,1,0,0DIVIDE BY 80,0,1,0,1DIVIDE BY 10 1,1,1,1,0DIVIDE BY 601,1,1,1,1DIVIDE BY 62
8	CAPLDEN	R/W	0h	ENABLE LOADING OF CAP1-4 REGISTERS ON A CAPTURE EVENT:0DISABLE CAP1-4 REGISTER LOADS AT CAPTURE EVENT TIME1ENABLE CAP1-4 REGISTER LOADS AT CAPTURE EVENT TIME
7	CTRRST4	R/W	0h	COUNTER RESET ON CAPTURE EVENT 4:0DO NOT RESET COUNTER ON CAPTURE EVENT 4 [ABSOLUTE TIME STAMP]1RESET COUNTER AFTER EVENT 4 TIME-STAMP HAS BEEN CAPTURED[USED IN DIFFERENCE MODE OPERATION]
6	CAP4POL	R/W	0h	CAPTURE EVENT 4 POLARITY SELECT:0CAPTURE EVENT 4 TRIGGERED ON A RISING EDGE [FE]1CAPTURE EVENT 4 TRIGGERED ON A FALLING EDGE [FE]

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Table 4-1728. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCTL2_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CTRRST3	R/W	0h	COUNTER RESET ON CAPTURE EVENT 3:0DO NOT RESET COUNTER ON CAPTURE EVENT 3 [ABSOLUTE TIME STAMP]1RESET COUNTER AFTER EVENT 3 TIME-STAMP HAS BEEN CAPTURED[USED IN DIFFERENCE MODE OPERATION]
4	CAP3POL	R/W	0h	CAPTURE EVENT 3 POLARITY SELECT:0CAPTURE EVENT 3 TRIGGERED ON A RISING EDGE [FE]1CAPTURE EVENT 3 TRIGGERED ON A FALLING EDGE [FE]
3	CTRRST2	R/W	0h	COUNTER RESET ON CAPTURE EVENT 2:0DO NOT RESET COUNTER ON CAPTURE EVENT 2 [ABSOLUTE TIME STAMP]1RESET COUNTER AFTER EVENT 2 TIME-STAMP HAS BEEN CAPTURED[USED IN DIFFERENCE MODE OPERATION]
2	CAP2POL	R/W	0h	CAPTURE EVENT 2 POLARITY SELECT:0CAPTURE EVENT 2 TRIGGERED ON A RISING EDGE [FE]1CAPTURE EVENT 2 TRIGGERED ON A FALLING EDGE [FE]
1	CTRRST1	R/W	0h	COUNTER RESET ON CAPTURE EVENT 1:0DO NOT RESET COUNTER ON CAPTURE EVENT 1 [ABSOLUTE TIME STAMP]1RESET COUNTER AFTER EVENT 1 TIME-STAMP HAS BEEN CAPTURED[USED IN DIFFERENCE MODE OPERATION]
0	CAP1POL	R/W	0h	CAPTURE EVENT 1 POLARITY SELECT:0CAPTURE EVENT 1 TRIGGERED ON A RISING EDGE [FE]1CAPTURE EVENT 1 TRIGGERED ON A FALLING EDGE [FE]

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4.2.2.356 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFLG_ECEINT Register

4.2.2.356.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFLG_ECEINT Register (Offset = 2Ch) [reset = 0h]

ECAP INTERRUPT ENABLE REGISTER.

Return to Summary Table

Table 4-1729. Instance Table

Instance Name	Physical Address
ICSSM0	4803 002Ch

Figure 4-842. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFLG_ECEINT Name Register

31	30	29	28	27	26	25	24
FLAG_RESV0							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FLAG_CMPEQ	FLAG_PRDEQ	FLAG_CNTOVF	FLAG_CEVT4	FLAG_CEVT3	FLAG_CEVT2	FLAG_CEVT1	FLAG_INT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EN__RESV1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EN_CMPEQ	EN_PRDEQ	EN_CNTOVF	EN_CEVT4	EN_CEVT3	EN_CEVT2	EN_CEVT1	EN_RESV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1730. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFLG_ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	FLAG_RESV0	R	0h	
23	FLAG_CMPEQ	R	0h	COMPARE EQUAL STATUS FLAG: READING A 1 ON THIS BIT INDICATES THE COUNTER [TSCNT] REACHED THE COMPARE REGISTER VALUE [ACMP]READING A 0 INDICATES NO EVENT OCCURREDNOTE: THIS FLAG IS ONLY ACTIVE IN APWM MODE
22	FLAG_PRDEQ	R	0h	PERIOD EQUAL STATUS FLAG: READING A 1 ON THIS BIT INDICATES THE COUNTER [TSCNT] REACHED THE PERIOD REGISTER VALUE [APER] AND WAS RESETREADING A 0 INDICATES NO EVENT OCCURREDNOTES: THIS FLAG IS ONLY ACTIVE IN APWM MODE
21	FLAG_CNTOVF	R	0h	COUNTER OVERFLOW STATUS FLAG: READING A 1 ON THIS BIT INDICATES THE COUNTER [TSCNT] HAS MADE THE TRANSITION FROM FFFFFFFF 00000000READING A 0 INDICATES NO EVENT OCCURREDNOTE: THIS FLAG IS ACTIVE IN CAP &
20	FLAG_CEVT4	R	0h	CAPTURE EVENT 4 STATUS FLAG: READING A 1 ON THIS BIT INDICATES THE FOURTH EVENT OCCURRED AT ECAPX PINREADING A 0 INDICATES NO EVENT OCCURREDNOTE: THIS FLAG IS ONLY ACTIVE IN CAP MODE
19	FLAG_CEVT3	R	0h	CAPTURE EVENT 3 STATUS FLAG: READING A 1 ON THIS BIT INDICATES THE THIRD EVENT OCCURRED AT ECAPX PINREADING A 0 INDICATES NO EVENT OCCURREDNOTE: THIS FLAG IS ONLY ACTIVE IN CAP MODE

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Table 4-1730. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFLG_ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	FLAG_CEVT2	R	0h	CAPTURE EVENT 2 STATUS FLAG: READING A 1 ON THIS BIT INDICATES THE SECOND EVENT OCCURRED AT ECAPX PINREADING A 0 INDICATES NO EVENT OCCURREDNOTE: THIS FLAG IS ONLY ACTIVE IN CAP MODE
17	FLAG_CEVT1	R	0h	CAPTURE EVENT 1 STATUS FLAG: READING A 1 ON THIS BIT INDICATES THE FIRST EVENT OCCURRED AT ECAPX PINREADING A 0 INDICATES NO EVENT OCCURREDNOTE: THIS FLAG IS ONLY ACTIVE IN CAP MODE
16	FLAG_INT	R	0h	GLOBAL INTERRUPT STATUS FLAG: READING A 1 ON THIS BIT INDICATES THAT AN INTERRUPT WAS GENERATED FROM ONE OF THE FOLLOWING EVENTSREADING A 0 INDICATES NO INTERRUPT GENERATED
15:8	EN__RESV1	R	0h	
7	EN_CMPEQ	R/W	0h	COMPARE EQUAL INTERRUPT ENABLE: 0DISABLED COMPARE EQUAL AS AN INTERRUPT SOURCE1ENABLE COMPARE EQUAL AS AN INTERRUPT SOURCE
6	EN_PRDEQ	R/W	0h	PERIOD EQUAL INTERRUPT ENABLE: 0DISABLED PERIOD EQUAL AS AN INTERRUPT SOURCE1ENABLE PERIOD EQUAL AS AN INTERRUPT SOURCE
5	EN_CNTOVF	R/W	0h	COUNTER OVERFLOW INTERRUPT ENABLE: 0DISABLED COUNTER OVERFLOW AS AN INTERRUPT SOURCE1ENABLE COUNTER OVERFLOW AS AN INTERRUPT SOURCE
4	EN_CEVT4	R/W	0h	CAPTURE EVENT 4 INTERRUPT ENABLE: 0DISABLED CAPTURE EVENT 1 AS AN INTERRUPT SOURCE1ENABLE CAPTURE EVENT 1 AS AN INTERRUPT SOURCE
3	EN_CEVT3	R/W	0h	CAPTURE EVENT 3 INTERRUPT ENABLE: 0DISABLED CAPTURE EVENT 1 AS AN INTERRUPT SOURCE1ENABLE CAPTURE EVENT 1 AS AN INTERRUPT SOURCE
2	EN_CEVT2	R/W	0h	CAPTURE EVENT 2 INTERRUPT ENABLE: 0DISABLED CAPTURE EVENT 1 AS AN INTERRUPT SOURCE1ENABLE CAPTURE EVENT 1 AS AN INTERRUPT SOURCE
1	EN_CEVT1	R/W	0h	CAPTURE EVENT 1 INTERRUPT ENABLE: 0DISABLED CAPTURE EVENT 1 AS AN INTERRUPT SOURCE1ENABLE CAPTURE EVENT 1 AS AN INTERRUPT SOURCE
0	EN_RESV0	R	0h	

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4.2.2.357 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCLR Register

4.2.2.357.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCLR Register (Offset = 30h) [reset = 0h]

ECAP INTERRUPT CLEAR REGISTER.

Return to Summary Table

Table 4-1731. Instance Table

Instance Name	Physical Address
ICSSM0	4803 0030h

Figure 4-843. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
_RESV0							
R							
0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1732. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	_RESV0	R	0h	
7	CMPEQ	R/W	0h	COMPARE EQUAL STATUS FLAG: WRITING A 1 WILL CLEAR THE CMPEQ FLAG CONDITIONWRITING A 0 WILL HAVE NO EFFECTALWAYS READS BACK A 0
6	PRDEQ	R/W	0h	PERIOD EQUAL STATUS FLAG: WRITING A 1 WILL CLEAR THE PRDEQ FLAG CONDITIONWRITING A 0 WILL HAVE NO EFFECTALWAYS READS BACK A 0
5	CNTOVF	R/W	0h	COUNTER OVERFLOW STATUS FLAG: WRITING A 1 WILL CLEAR THE CNTOVF FLAG CONDITIONWRITING A 0 WILL HAVE NO EFFECTALWAYS READS BACK A 0
4	CEVT4	R/W	0h	CAPTURE EVENT 4 STATUS FLAG: WRITING A 1 WILL CLEAR THE CEVT3 FLAG CONDITIONWRITING A 0 WILL HAVE NO EFFECTALWAYS READS BACK A 0
3	CEVT3	R/W	0h	CAPTURE EVENT 3 STATUS FLAG: WRITING A 1 WILL CLEAR THE CEVT3 FLAG CONDITIONWRITING A 0 WILL HAVE NO EFFECTALWAYS READS BACK A 0
2	CEVT2	R/W	0h	CAPTURE EVENT 2 STATUS FLAG: WRITING A 1 WILL CLEAR THE CEVT2 FLAG CONDITIONWRITING A 0 WILL HAVE NO EFFECTALWAYS READS BACK A 0
1	CEVT1	R/W	0h	CAPTURE EVENT 1 STATUS FLAG: WRITING A 1 WILL CLEAR THE CEVT1 FLAG CONDITIONWRITING A 0 WILL HAVE NO EFFECTALWAYS READS BACK A 0

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Table 4-1732. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	R/W	0h	GLOBAL INTERRUPT CLEAR FLAG: WRITING A 1 WILL CLEAR THE INT FLAG AND ENABLE FURTHER INTERRUPTS TO BE GENERATED IF ANY OF THE EVENT FLAGS ARE SET TO 1WRITING A 0 WILL HAVE NO EFFECTALWAYS READS BACK A 0

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4.2.2.358 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFRC Register

4.2.2.358.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFRC Register (Offset = 34h) [reset = 0h]

ECAP INTERRUPT FORCING REGISTER.

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Table 4-1733. Instance Table

Instance Name	Physical Address
ICSSM0	4803 0034h

Figure 4-844. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFRC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
_RESV1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	_RESV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1734. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	_RESV1	R	0h	
7	CMPEQ	R/W	0h	FORCE COMPARE EQUAL: WRITING A 1 TO THIS BIT WILL SET THE CMPEQ FLAG BITWRITING OF 0 WILL BE IGNORED ALWAYS READS BACK A 0
6	PRDEQ	R/W	0h	FORCE PERIOD EQUAL: WRITING A 1 TO THIS BIT WILL SET THE PRDEQ FLAG BITWRITING OF 0 WILL BE IGNORED ALWAYS READS BACK A 0
5	CNTOVF	R/W	0h	FORCE COUNTER OVERFLOW: WRITING A 1 TO THIS BIT WILL SET THE CNTOVF FLAG BITWRITING OF 0 WILL BE IGNORED ALWAYS READS BACK A 0
4	CEVT4	R/W	0h	FORCE CAPTURE EVENT 4:WRITING A 1 TO THIS BIT WILL SET THE CEVT4 FLAG BITWRITING OF 0 WILL BE IGNORED ALWAYS READS BACK A 0
3	CEVT3	R/W	0h	FORCE CAPTURE EVENT 3:WRITING A 1 TO THIS BIT WILL SET THE CEVT3 FLAG BITWRITING OF 0 WILL BE IGNORED ALWAYS READS BACK A 0
2	CEVT2	R/W	0h	FORCE CAPTURE EVENT 2:WRITING A 1 TO THIS BIT WILL SET THE CEVT2 FLAG BITWRITING OF 0 WILL BE IGNORED ALWAYS READS BACK A 0
1	CEVT1	R/W	0h	FORCE CAPTURE EVENT 1:WRITING A 1 TO THIS BIT WILL SET THE CEVT1 FLAG BITWRITING OF 0 WILL BE IGNORED ALWAYS READS BACK A 0

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Table 4-1734. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	_RESV0	R	0h	

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4.2.2.359 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_REVID1 Register

4.2.2.359.1 ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_REVID1 Register (Offset = 5Ch) [reset = 44D22100h]

Revision Identification Register 1

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Table 4-1735. Instance Table

Instance Name	Physical Address
ICSSM0	4803 005Ch

Figure 4-845. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_REVID1 Name Register

31	30	29	28	27	26	25	24
REVID							
R							
44D22100h							
23	22	21	20	19	18	17	16
REVID							
R							
44D22100h							
15	14	13	12	11	10	9	8
REVID							
R							
44D22100h							
7	6	5	4	3	2	1	0
REVID							
R							
44D22100h							

Table 4-1736. ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_REVID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REVID	R	44D22100h	

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4.2.2.360 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG0 Register

4.2.2.360.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG0 Register (Offset = 0h) [reset = 0h]

MIIRXCFG0Register.

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Table 4-1737. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2000h

Figure 4-846. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						RX_EOF_SCLR_DIS0	RX_ERR_RAW0
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_SFD_RAW0	RX_AUTO_FWD_PRE0	RX_BYTE_SWAP0	RX_L2_EN0	RX_MUX_SEL0	RX_CUT_PREAMBLE0	RX_DATA_RDY_MODE_DIS0	RX_ENABLE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-1738. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	RX_EOF_SCLR_DIS0	R/W	0h	
8	RX_ERR_RAW0	R/W	0h	
7	RX_SFD_RAW0	R/W	0h	
6	RX_AUTO_FWD_PRE0	R/W	0h	
5	RX_BYTE_SWAP0	R/W	0h	
4	RX_L2_EN0	R/W	0h	
3	RX_MUX_SEL0	R/W	0h	
2	RX_CUT_PREAMBLE0	R/W	0h	
1	RX_DATA_RDY_MODE_DIS0	R/W	0h	
0	RX_ENABLE0	R/W	0h	

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4.2.2.361 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG1 Register

4.2.2.361.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG1 Register (Offset = 4h) [reset = 8h]

MIIRXCFG1Register.

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Table 4-1739. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2004h

Figure 4-847. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						RX_EOF_SCLR_DIS1	RX_ERR_RAW1
NONE						R/W	R/W
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_SFD_RAW1	RX_AUTO_FWD_PRE1	RX_BYTE_SWAP1	RX_L2_EN1	RX_MUX_SEL1	RX_CUT_PREAMBLE1	RX_DATA_RDY_MODE_DIS1	RX_ENABLE1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	1h	0h	0h	0h

Table 4-1740. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	RX_EOF_SCLR_DIS1	R/W	0h	
8	RX_ERR_RAW1	R/W	0h	
7	RX_SFD_RAW1	R/W	0h	
6	RX_AUTO_FWD_PRE1	R/W	0h	
5	RX_BYTE_SWAP1	R/W	0h	
4	RX_L2_EN1	R/W	0h	
3	RX_MUX_SEL1	R/W	1h	
2	RX_CUT_PREAMBLE1	R/W	0h	
1	RX_DATA_RDY_MODE_DIS1	R/W	0h	
0	RX_ENABLE1	R/W	0h	

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4.2.2.362 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG0 Register

4.2.2.362.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG0 Register (Offset = 10h) [reset = 400100h]

MIITXCFG0Register.

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Table 4-1741. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2010h

Figure 4-848. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG0 Name Register

31	30	29	28	27	26	25	24
RESERVED	TX_CLK_DELAY0			RESERVED		TX_START_DELAY0	
NONE	R/W			NONE		R/W	
0h	0h			0h		40h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_START_DELAY0							
R/W							
40h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TX_IPG_WIRE_CLK_EN0	TX_32_MODE_EN0	PRE_TX_AUTO_ESC_ERR0	PRE_TX_AUTO_SEQUENCE0	TX_MUX_SEL0
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TX_BYTE_SWAP0	TX_EN_MODE0	TX_AUTO_PREAMBLE0	TX_ENABLE0
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 4-1742. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	TX_CLK_DELAY0	R/W	0h	
27:26	RESERVED	NONE	0h	Reserved
25:16	TX_START_DELAY0	R/W	40h	
15:13	RESERVED	NONE	0h	Reserved
12	TX_IPG_WIRE_CLK_EN0	R/W	0h	
11	TX_32_MODE_EN0	R/W	0h	
10	PRE_TX_AUTO_ESC_ERR0	R/W	0h	
9	PRE_TX_AUTO_SEQUENCE0	R/W	0h	
8	TX_MUX_SEL0	R/W	1h	
7:4	RESERVED	NONE	0h	Reserved
3	TX_BYTE_SWAP0	R/W	0h	
2	TX_EN_MODE0	R/W	0h	
1	TX_AUTO_PREAMBLE0	R/W	0h	
0	TX_ENABLE0	R/W	0h	

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4.2.2.363 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG1 Register

4.2.2.363.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG1 Register (Offset = 14h) [reset = 400000h]

MIITXCFG1Register.

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Table 4-1743. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2014h

Figure 4-849. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG1 Name Register

31	30	29	28	27	26	25	24
RESERVED	TX_CLK_DELAY1			RESERVED		TX_START_DELAY1	
NONE	R/W			NONE		R/W	
0h	0h			0h		40h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_START_DELAY1							
R/W							
40h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			TX_IPG_WIRE_CLK_EN1	TX_32_MODE_EN1	PRE_TX_AUTO_ESC_ERR1	PRE_TX_AUTO_SEQUENCE1	TX_MUX_SEL1
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TX_BYTE_SWAP1	TX_EN_MODE1	TX_AUTO_PREAMBLE1	TX_ENABLE1
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 4-1744. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	TX_CLK_DELAY1	R/W	0h	
27:26	RESERVED	NONE	0h	Reserved
25:16	TX_START_DELAY1	R/W	40h	
15:13	RESERVED	NONE	0h	Reserved
12	TX_IPG_WIRE_CLK_EN1	R/W	0h	
11	TX_32_MODE_EN1	R/W	0h	
10	PRE_TX_AUTO_ESC_ERR1	R/W	0h	
9	PRE_TX_AUTO_SEQUENCE1	R/W	0h	
8	TX_MUX_SEL1	R/W	0h	
7:4	RESERVED	NONE	0h	Reserved
3	TX_BYTE_SWAP1	R/W	0h	
2	TX_EN_MODE1	R/W	0h	
1	TX_AUTO_PREAMBLE1	R/W	0h	
0	TX_ENABLE1	R/W	0h	

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4.2.2.364 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC0 Register

4.2.2.364.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC0 Register (Offset = 20h) [reset = 0h]

MIITXCRC0Register.

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Table 4-1745. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2020h

Figure 4-850. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC0 Name Register

31	30	29	28	27	26	25	24
TX_CRC0							
R							
0h							
23	22	21	20	19	18	17	16
TX_CRC0							
R							
0h							
15	14	13	12	11	10	9	8
TX_CRC0							
R							
0h							
7	6	5	4	3	2	1	0
TX_CRC0							
R							
0h							

Table 4-1746. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TX_CRC0	R	0h	Transmit CRC for last packet

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4.2.2.365 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC1 Register

4.2.2.365.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC1 Register (Offset = 24h) [reset = 0h]

MIITXCRC1Register.

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Table 4-1747. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2024h

Figure 4-851. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC1 Name Register

31	30	29	28	27	26	25	24
TX_CRC1							
R							
0h							
23	22	21	20	19	18	17	16
TX_CRC1							
R							
0h							
15	14	13	12	11	10	9	8
TX_CRC1							
R							
0h							
7	6	5	4	3	2	1	0
TX_CRC1							
R							
0h							

Table 4-1748. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TX_CRC1	R	0h	Transmit CRC for last packet

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4.2.2.366 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG0 Register

4.2.2.366.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG0 Register (Offset = 30h) [reset = 28h]

MIITXIPG0Register.

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Table 4-1749. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2030h

Figure 4-852. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_IPG0							
R/W							
28h							
7	6	5	4	3	2	1	0
TX_IPG0							
R/W							
28h							

Table 4-1750. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_IPG0	R/W	28h	Transmit IPG

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4.2.2.367 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG1 Register

4.2.2.367.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG1 Register (Offset = 34h) [reset = 28h]

MIITXIPG1Register.

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Table 4-1751. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2034h

Figure 4-853. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_IPG1							
R/W							
28h							
7	6	5	4	3	2	1	0
TX_IPG1							
R/W							
28h							

Table 4-1752. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_IPG1	R/W	28h	Transmit IPG

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4.2.2.368 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS0 Register

4.2.2.368.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS0 Register (Offset = 38h) [reset = 0h]

MIIPortStatus0Register.

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Table 4-1753. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2038h

Figure 4-854. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SYNC_PORT0_CRS	SYNC_PORT0_COL
NONE						R	R
0h						0h	0h

Table 4-1754. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SYNC_PORT0_CRS	R	0h	Sync_port0_crs
0	SYNC_PORT0_COL	R	0h	Sync_port0_col

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4.2.2.369 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS1 Register

4.2.2.369.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS1 Register (Offset = 3Ch) [reset = 0h]

MIIPortStatus1Register.

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Table 4-1755. Instance Table

Instance Name	Physical Address
ICSSM0	4803 203Ch

Figure 4-855. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SYNC_PORT1_CRS	SYNC_PORT1_COL
NONE						R	R
0h						0h	0h

Table 4-1756. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SYNC_PORT1_CRS	R	0h	Sync_port1_crs
0	SYNC_PORT1_COL	R	0h	Sync_port1_col

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4.2.2.370 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS0 Register

4.2.2.370.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS0 Register (Offset = 40h) [reset = 5F1003Fh]

MIIRXFRMS0Register.

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Table 4-1757. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2040h

Figure 4-856. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS0 Name Register

31	30	29	28	27	26	25	24
RX_MAX_FRM0							
R/W							
5F1h							
23	22	21	20	19	18	17	16
RX_MAX_FRM0							
R/W							
5F1h							
15	14	13	12	11	10	9	8
RX_MIN_FRM0							
R/W							
3Fh							
7	6	5	4	3	2	1	0
RX_MIN_FRM0							
R/W							
3Fh							

Table 4-1758. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RX_MAX_FRM0	R/W	5F1h	Rx_max_frm0
15:0	RX_MIN_FRM0	R/W	3Fh	Rx_min_frm0

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4.2.2.371 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS1 Register

4.2.2.371.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS1 Register (Offset = 44h) [reset = 5F1003Fh]

MIIRXFRMS1Register.

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Table 4-1759. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2044h

Figure 4-857. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS1 Name Register

31	30	29	28	27	26	25	24
RX_MAX_FRM1							
R/W							
5F1h							
23	22	21	20	19	18	17	16
RX_MAX_FRM1							
R/W							
5F1h							
15	14	13	12	11	10	9	8
RX_MIN_FRM1							
R/W							
3Fh							
7	6	5	4	3	2	1	0
RX_MIN_FRM1							
R/W							
3Fh							

Table 4-1760. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RX_MAX_FRM1	R/W	5F1h	Rx_max_frm1
15:0	RX_MIN_FRM1	R/W	3Fh	Rx_min_frm1

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4.2.2.372 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT0 Register

4.2.2.372.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT0 Register (Offset = 48h) [reset = E1h]

MIIRXPCNT0Register.

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Table 4-1761. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2048h

Figure 4-858. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							RX_MAX_PCNT0
NONE							R/W
0h							Eh
7	6	5	4	3	2	1	0
RX_MAX_PCNT0				RX_MIN_PCNT0			
R/W				R/W			
Eh				1h			

Table 4-1762. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:4	RX_MAX_PCNT0	R/W	Eh	Rx_max_pcnt0
3:0	RX_MIN_PCNT0	R/W	1h	Rx_min_pcnt0

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4.2.2.373 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT1 Register

4.2.2.373.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT1 Register (Offset = 4Ch) [reset = E1h]

MIIRXPCNT1Register.

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Table 4-1763. Instance Table

Instance Name	Physical Address
ICSSM0	4803 204Ch

Figure 4-859. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							RX_MAX_PCNT1
NONE							R/W
0h							Eh
7	6	5	4	3	2	1	0
RX_MAX_PCNT1				RX_MIN_PCNT1			
R/W				R/W			
Eh				1h			

Table 4-1764. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8:4	RX_MAX_PCNT1	R/W	Eh	Rx_max_pcnt1
3:0	RX_MIN_PCNT1	R/W	1h	Rx_min_pcnt1

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4.2.2.374 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR0 Register

4.2.2.374.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR0 Register (Offset = 50h) [reset = 0h]

MIIRXERR0Register.

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Table 4-1765. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2050h

Figure 4-860. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				RX_MAX_FRM_ERR0	RX_MIN_FRM_ERR0	RX_MAX_PCNT_ERR0	RX_MIN_PCNT_ERR0
NONE				R/W1C	R/W1C	R/W1C	R/W1C
0h				0h	0h	0h	0h

Table 4-1766. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RX_MAX_FRM_ERR0	R/W1C	0h	Rx_max_frm_err0
2	RX_MIN_FRM_ERR0	R/W1C	0h	Rx_min_frm_err0
1	RX_MAX_PCNT_ERR0	R/W1C	0h	Rx_max_pcnt_err0
0	RX_MIN_PCNT_ERR0	R/W1C	0h	Rx_min_pcnt_err0

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4.2.2.375 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR1 Register

4.2.2.375.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR1 Register (Offset = 54h) [reset = 0h]

MIIRXERR1Register.

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Table 4-1767. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2054h

Figure 4-861. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RX_MAX_FRM_ERR1	RX_MIN_FRM_ERR1	RX_MAX_PCNT_ERR1	RX_MIN_PCNT_ERR1
NONE				R/W1C	R/W1C	R/W1C	R/W1C
0h				0h	0h	0h	0h

Table 4-1768. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	RX_MAX_FRM_ERR1	R/W1C	0h	Rx_max_frm_err1
2	RX_MIN_FRM_ERR1	R/W1C	0h	Rx_min_frm_err1
1	RX_MAX_PCNT_ERR1	R/W1C	0h	Rx_max_pcnt_err1
0	RX_MIN_PCNT_ERR1	R/W1C	0h	Rx_min_pcnt_err1

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4.2.2.376 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVEL0 Register

4.2.2.376.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVEL0 Register (Offset = 60h) [reset = 0h]

MIIRXFIFOLEVEL0Register.

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Table 4-1769. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2060h

Figure 4-862. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVEL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_LEVEL0							
R							
0h							

Table 4-1770. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_FIFO_LEVEL0	R	0h	Rx_fifo_level0

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4.2.2.377 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVEL1 Register

4.2.2.377.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVEL1 Register (Offset = 64h) [reset = 0h]

MIIRXFIFOLEVEL1Register.

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Table 4-1771. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2064h

Figure 4-863. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVEL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_LEVEL1							
R							
0h							

Table 4-1772. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	RX_FIFO_LEVEL1	R	0h	Rx_fifo_level1

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4.2.2.378 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVEL0 Register

4.2.2.378.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVEL0 Register (Offset = 68h) [reset = 0h]

MIIRXFIFOLEVEL0Register.

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Table 4-1773. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2068h

Figure 4-864. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVEL0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_FIFO_LEVEL0							
R							
0h							

Table 4-1774. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_FIFO_LEVEL0	R	0h	tx_fifo_level0

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4.2.2.379 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVEL1 Register

4.2.2.379.1 ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVEL1 Register (Offset = 6Ch) [reset = 0h]

MIIRXFIFOLEVEL1Register.

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Table 4-1775. Instance Table

Instance Name	Physical Address
ICSSM0	4803 206Ch

Figure 4-865. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVEL1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TX_FIFO_LEVEL1							
R							
0h							

Table 4-1776. ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TX_FIFO_LEVEL1	R	0h	tx_fifo_level1

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4.2.2.380 ICSSM_PR1_MDIO_V1P7_MDIO_MDIO_VERSION_REG Register

4.2.2.380.1 ICSSM_PR1_MDIO_V1P7_MDIO_MDIO_VERSION_REG Register (Offset = 0h) [reset = 70107h]

version_reg.

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Table 4-1777. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2400h

Figure 4-866. ICSSM_PR1_MDIO_V1P7_MDIO_MDIO_VERSION_REG Name Register

31	30	29	28	27	26	25	24
MODID							
R							
7h							
23	22	21	20	19	18	17	16
MODID							
R							
7h							
15	14	13	12	11	10	9	8
REVMAJ							
R							
1h							
7	6	5	4	3	2	1	0
REVMINOR							
R							
7h							

Table 4-1778. ICSSM_PR1_MDIO_V1P7_MDIO_MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	7h	Module ID
15:8	REVMAJ	R	1h	Major revision value
7:0	REVMINOR	R	7h	Minor revision value

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4.2.2.381 ICSSM_PR1_MDIO_V1P7_MDIO_CONTROL_REG Register

4.2.2.381.1 ICSSM_PR1_MDIO_V1P7_MDIO_CONTROL_REG Register (Offset = 4h) [reset = 810000FFh]

control_reg.

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Table 4-1779. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2404h

Figure 4-867. ICSSM_PR1_MDIO_V1P7_MDIO_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R	R/W	NONE	R				
1h	0h	0h	1h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
NONE			R/W	R/W1TC	R/W	R/W	NONE
0h			0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKDIV							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKDIV							
R/W							
FFh							

Table 4-1780. ICSSM_PR1_MDIO_V1P7_MDIO_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine idle
30	ENABLE	R/W	0h	Enable control
29	RESERVED	NONE	0h	Reserved
28:24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel
23:21	RESERVED	NONE	0h	Reserved
20	PREAMBLE	R/W	0h	Preamble disable
19	FAULT	R/W1TC	0h	Fault indicator
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable
16	RESERVED	NONE	0h	Reserved
15:0	CLKDIV	R/W	FFh	Clock divider

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4.2.2.382 ICSSM_PR1_MDIO_V1P7_MDIO_ALIVE_REG Register

4.2.2.382.1 ICSSM_PR1_MDIO_V1P7_MDIO_ALIVE_REG Register (Offset = 8h) [reset = 0h]

Alive_reg.

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Table 4-1781. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2408h

Figure 4-868. ICSSM_PR1_MDIO_V1P7_MDIO_ALIVE_REG Name Register

31	30	29	28	27	26	25	24
ALIVE							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
ALIVE							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
ALIVE							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
ALIVE							
R/W1TC							
0h							

Table 4-1782. ICSSM_PR1_MDIO_V1P7_MDIO_ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ALIVE	R/W1TC	0h	MDIO alive

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4.2.2.383 ICSSM_PR1_MDIO_V1P7_MDIO_LINK_REG Register

4.2.2.383.1 ICSSM_PR1_MDIO_V1P7_MDIO_LINK_REG Register (Offset = Ch) [reset = 0h]

Link_reg.

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Table 4-1783. Instance Table

Instance Name	Physical Address
ICSSM0	4803 240Ch

Figure 4-869. ICSSM_PR1_MDIO_V1P7_MDIO_LINK_REG Name Register

31	30	29	28	27	26	25	24
LINK							
R							
0h							
23	22	21	20	19	18	17	16
LINK							
R							
0h							
15	14	13	12	11	10	9	8
LINK							
R							
0h							
7	6	5	4	3	2	1	0
LINK							
R							
0h							

Table 4-1784. ICSSM_PR1_MDIO_V1P7_MDIO_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LINK	R	0h	MDIO link state

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4.2.2.384 ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_RAW_REG Register

4.2.2.384.1 ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_RAW_REG Register (Offset = 10h) [reset = 0h]

Link_int_raw_reg.

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Table 4-1785. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2410h

Figure 4-870. ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTRAW	
NONE						R/W1TC	
0h						0h	

Table 4-1786. ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	LINKINTRAW	R/W1TC	0h	MDIO link change event raw value

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4.2.2.385 ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASKED_REG Register

4.2.2.385.1 ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASKED_REG Register (Offset = 14h) [reset = 0h]

Link_int_masked_reg.

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Table 4-1787. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2414h

Figure 4-871. ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTMASKED	
NONE						R/W1TC	
0h						0h	

Table 4-1788. ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	LINKINTMASKED	R/W1TC	0h	MDIO link change interrupt masked value

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4.2.2.386 ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_SET_REG Register

4.2.2.386.1 ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_SET_REG Register (Offset = 18h) [reset = 0h]

Link_int_mask_set_reg.

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Table 4-1789. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2418h

Figure 4-872. ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK SET
NONE							R/W1TS
0h							0h

Table 4-1790. ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINKINTMASKSET	R/W1TS	0h	MDIO link interrupt mask set

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4.2.2.387 ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_CLEAR_REG Register

4.2.2.387.1 ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = 1Ch) [reset = 0h]

Link_int_mask_clear_reg.

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Table 4-1791. Instance Table

Instance Name	Physical Address
ICSSM0	4803 241Ch

Figure 4-873. ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK CLR
NONE							R/W1TC
0h							0h

Table 4-1792. ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINKINTMASKCLR	R/W1TC	0h	MDIO link interrupt mask clear

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4.2.2.388 ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_RAW_REG Register

4.2.2.388.1 ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_RAW_REG Register (Offset = 20h) [reset = 0h]

user_int_raw_reg.

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Table 4-1793. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2420h

Figure 4-874. ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTRAW	
NONE						R/W1TC	
0h						0h	

Table 4-1794. ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTRAW	R/W1TC	0h	User interrupt raw

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4.2.2.389 ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASKED_REG Register

4.2.2.389.1 ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASKED_REG Register (Offset = 24h) [reset = 0h]

user_int_masked_reg.

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Table 4-1795. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2424h

Figure 4-875. ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKED	
NONE						R/W1TC	
0h						0h	

Table 4-1796. ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKED	R/W1TC	0h	User interrupt masked

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4.2.2.390 ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_SET_REG Register

4.2.2.390.1 ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_SET_REG Register (Offset = 28h) [reset = 0h]

user_int_mask_set_reg.

Return to Summary Table

Table 4-1797. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2428h

Figure 4-876. ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKSET	
NONE						R/W1TS	
0h						0h	

Table 4-1798. ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKSET	R/W1TS	0h	MDIO user interrupt mask set

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4.2.2.391 ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_CLEAR_REG Register

4.2.2.391.1 ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = 2Ch) [reset = 0h]

user_int_mask_clear_reg.

Return to Summary Table

Table 4-1799. Instance Table

Instance Name	Physical Address
ICSSM0	4803 242Ch

Figure 4-877. ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKCLR	
NONE						R/W1TC	
0h						0h	

Table 4-1800. ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKCLR	R/W1TC	0h	MDIO user interrupt mask clear

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4.2.2.392 ICSSM_PR1_MDIO_V1P7_MDIO_MANUAL_IF_REG Register

4.2.2.392.1 ICSSM_PR1_MDIO_V1P7_MDIO_MANUAL_IF_REG Register (Offset = 30h) [reset = 0h]

manual_if_reg.

Return to Summary Table

Table 4-1801. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2430h

Figure 4-878. ICSSM_PR1_MDIO_V1P7_MDIO_MANUAL_IF_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					MDIO_MDCLK_O	MDIO_OE	MDIO_PIN
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 4-1802. ICSSM_PR1_MDIO_V1P7_MDIO_MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output
1	MDIO_OE	R/W	0h	MDIO Output Enable
0	MDIO_PIN	R/W	0h	MDIO Pin

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4.2.2.393 ICSSM_PR1_MDIO_V1P7_MDIO_POLL_REG Register

4.2.2.393.1 ICSSM_PR1_MDIO_V1P7_MDIO_POLL_REG Register (Offset = 34h) [reset = 0h]

poll_reg.

Return to Summary Table

Table 4-1803. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2434h

Figure 4-879. ICSSM_PR1_MDIO_V1P7_MDIO_POLL_REG Name Register

31	30	29	28	27	26	25	24
MANUALMODE	STATECHANGEMODE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPG							
R/W							
0h							

Table 4-1804. ICSSM_PR1_MDIO_V1P7_MDIO_POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	MDIO Manual Mode
30	STATECHANGEMODE	R/W	0h	MDIO State Change Mode
29:8	RESERVED	NONE	0h	Reserved
7:0	IPG	R/W	0h	MDIO IPG

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4.2.2.394 ICSSM_PR1_MDIO_V1P7_MDIO_POLL_EN_REG Register

4.2.2.394.1 ICSSM_PR1_MDIO_V1P7_MDIO_POLL_EN_REG Register (Offset = 38h) [reset = FFFFFFFFh]

poll_en_reg.

Return to Summary Table

Table 4-1805. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2438h

Figure 4-880. ICSSM_PR1_MDIO_V1P7_MDIO_POLL_EN_REG Name Register

31	30	29	28	27	26	25	24
POLL_EN							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
POLL_EN							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
POLL_EN							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
POLL_EN							
R/W							
FFFFFFFFh							

Table 4-1806. ICSSM_PR1_MDIO_V1P7_MDIO_POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POLL_EN	R/W	FFFFFFFFh	MDIO Poll Enable

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4.2.2.395 ICSSM_PR1_MDIO_V1P7_MDIO_CLAUS45_REG Register

4.2.2.395.1 ICSSM_PR1_MDIO_V1P7_MDIO_CLAUS45_REG Register (Offset = 3Ch) [reset = 0h]

clause 45_reg

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Table 4-1807. Instance Table

Instance Name	Physical Address
ICSSM0	4803 243Ch

Figure 4-881. ICSSM_PR1_MDIO_V1P7_MDIO_CLAUS45_REG Name Register

31	30	29	28	27	26	25	24
CLAUSE45							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAUSE45							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAUSE45							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAUSE45							
R/W							
0h							

Table 4-1808. ICSSM_PR1_MDIO_V1P7_MDIO_CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAUSE45	R/W	0h	MDIO Clause 45

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4.2.2.396 ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR0_REG Register

4.2.2.396.1 ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR0_REG Register (Offset = 40h) [reset = 0h]

MDIO USER Address 0

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Table 4-1809. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2440h

Figure 4-882. ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR0_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
USER_ADDR0							
R/W							
0h							
7	6	5	4	3	2	1	0
USER_ADDR0							
R/W							
0h							

Table 4-1810. ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	USER_ADDR0	R/W	0h	MDIO USER Address 0

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4.2.2.397 ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR1_REG Register

4.2.2.397.1 ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR1_REG Register (Offset = 44h) [reset = 0h]

MDIO USER Address 1

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Table 4-1811. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2444h

Figure 4-883. ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
USER_ADDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
USER_ADDR1							
R/W							
0h							

Table 4-1812. ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	USER_ADDR1	R/W	0h	MDIO USER Address 1

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4.2.2.398 ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_ACCESS_REG_J Register

4.2.2.398.1 ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_ACCESS_REG_J Register (Offset = 80h) [reset = 0h]

user_access_reg

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Table 4-1813. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2480h + formula

Figure 4-884. ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_ACCESS_REG_j Name Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W1TS	R/W	R/W	NONE			R/W	
0h	0h	0h	0h			0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REGADR			PHYADR				
R/W			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 4-1814. ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_ACCESS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W1TS	0h	Go
30	WRITE	R/W	0h	Write
29	ACK	R/W	0h	Acknowledge
28:26	RESERVED	NONE	0h	Reserved
25:21	REGADR	R/W	0h	Register address
20:16	PHYADR	R/W	0h	PHY address
15:0	DATA	R/W	0h	User data

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4.2.2.399 ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_PHY_SEL_REG_J Register

4.2.2.399.1 ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_PHY_SEL_REG_J Register (Offset = 84h) [reset = 0h]

user_phy_sel_reg

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Table 4-1815. Instance Table

Instance Name	Physical Address
ICSSM0	4803 2484h + formula

Figure 4-885. ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W	R/W	NONE	R/W				
0h	0h	0h	0h				

Table 4-1816. ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LINKSEL	R/W	0h	Link status determination select
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable
5	RESERVED	NONE	0h	Reserved
4:0	PHYADR_MON	R/W	0h	PHY address whose link status is monitored

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4.2.2.400 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_ICSS_G_CFG Register

4.2.2.400.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_ICSS_G_CFG Register (Offset = 0h) [reset = 1h]

ICSS_G Ethernet Cfg.

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Table 4-1817. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3000h

Figure 4-886. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_ICSS_G_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					RX_SFD_TX_SOF_EN	RESERVED	
NONE					R/W	NONE	
0h					0h	0h	
7	6	5	4	3	2	1	0
RESERVED	MII1_MODE		MII0_MODE		RX_L2_G_EN	TX_L2_EN	TX_L1_EN
NONE	R/W		R/W		R/W	R/W	R/W
0h	0h		0h		0h	0h	1h

Table 4-1818. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_ICSS_G_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10	RX_SFD_TX_SOF_EN	R/W	0h	Enable the remaping of tx_sof to rx_sfd if auto fwd is enable
9:7	RESERVED	NONE	0h	Reserved
6:5	MII1_MODE	R/W	0h	MII1 MODE 0:MII 1:RGMII 2:SGMII
4:3	MII0_MODE	R/W	0h	MII0 MODE 0:MII 1:RGMII 2:SGMII
2	RX_L2_G_EN	R/W	0h	Enable the RX L2 G features of filter frags of size TBD and backpressure RX L2 0:Disabled 1:Enabled
1	TX_L2_EN	R/W	0h	Enable the TX L2 Fifo 0:Disabled 1:Enabled
0	TX_L1_EN	R/W	1h	Enable the TX L1 Fifo 0:Disabled 1:Enabled

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4.2.2.401 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_PREEMPT_CFG Register

4.2.2.401.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_PREEMPT_CFG Register (Offset = 4h) [reset = 1907D500h]

Preemption_Cfg

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Table 4-1819. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3004h

Figure 4-887. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_PREEMPT_CFG Name Register

31	30	29	28	27	26	25	24
SMD_R							
R/W							
19h							
23	22	21	20	19	18	17	16
SMD_V							
R/W							
7h							
15	14	13	12	11	10	9	8
EXP_SMD							
R/W							
D5h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1820. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_PREEMPT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SMD_R	R/W	19h	Response frame TAG
23:16	SMD_V	R/W	7h	Verification frame TAG
15:8	EXP_SMD	R/W	D5h	None preemptable frame start, or express frame
7:0	RESERVED	NONE	0h	Reserved

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4.2.2.402 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1S_CFG Register

4.2.2.402.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1S_CFG Register (Offset = 8h) [reset = B37F4CE6h]

SMDType1SPreemptableFrameStartCfg

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Table 4-1821. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3008h

Figure 4-888. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1S_CFG Name Register

31	30	29	28	27	26	25	24
SMDT1S_3							
R/W							
B3h							
23	22	21	20	19	18	17	16
SMDT1S_2							
R/W							
7Fh							
15	14	13	12	11	10	9	8
SMDT1S_1							
R/W							
4Ch							
7	6	5	4	3	2	1	0
SMDT1S_0							
R/W							
E6h							

Table 4-1822. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1S_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SMDT1S_3	R/W	B3h	SMDT1S3 pattern
23:16	SMDT1S_2	R/W	7Fh	SMDT1S2 pattern
15:8	SMDT1S_1	R/W	4Ch	SMDT1S1 pattern
7:0	SMDT1S_0	R/W	E6h	SMDT1S0 pattern

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4.2.2.403 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1C_CFG Register

4.2.2.403.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1C_CFG Register (Offset = Ch) [reset = 2A9E5261h]

SMDType1CNoneInitialFragCfg

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Table 4-1823. Instance Table

Instance Name	Physical Address
ICSSM0	4803 300Ch

Figure 4-889. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1C_CFG Name Register

31	30	29	28	27	26	25	24
SMDT1C_3							
R/W							
2Ah							
23	22	21	20	19	18	17	16
SMDT1C_2							
R/W							
9Eh							
15	14	13	12	11	10	9	8
SMDT1C_1							
R/W							
52h							
7	6	5	4	3	2	1	0
SMDT1C_0							
R/W							
61h							

Table 4-1824. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1C_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SMDT1C_3	R/W	2Ah	SMDT1C3 pattern
23:16	SMDT1C_2	R/W	9Eh	SMDT1C2 pattern
15:8	SMDT1C_1	R/W	52h	SMDT1C1 pattern
7:0	SMDT1C_0	R/W	61h	SMDT1C0 pattern

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4.2.2.404 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_POOL_PTR_CFG Register

4.2.2.404.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_POOL_PTR_CFG Register (Offset = 10h) [reset = 800h]

PoolPtrCfg

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Table 4-1825. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3010h

Figure 4-890. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_POOL_PTR_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAX_PKT_SIZE							
R/W							
800h							
7	6	5	4	3	2	1	0
MAX_PKT_SIZE							
R/W							
800h							

Table 4-1826. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_POOL_PTR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	MAX_PKT_SIZE	R/W	800h	Max Pkt Size, used in pool ptr logic for wrap around

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4.2.2.405 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_TX_EARLY_EOF Register

4.2.2.405.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_TX_EARLY_EOF Register (Offset = 14h) [reset = 0h]

TX Early EOF Enable Reserved

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Table 4-1827. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3014h

Figure 4-891. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_TX_EARLY_EOF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 4-1828. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_TX_EARLY_EOF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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4.2.2.406 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_FRAG_CNT_CFG Register

4.2.2.406.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_FRAG_CNT_CFG Register (Offset = 18h) [reset = B37F4CE6h]

FragCntCfg

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Table 4-1829. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3018h

Figure 4-892. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_FRAG_CNT_CFG Name Register

31	30	29	28	27	26	25	24
FRAG_CNT_3							
R/W							
B3h							
23	22	21	20	19	18	17	16
FRAG_CNT_2							
R/W							
7Fh							
15	14	13	12	11	10	9	8
FRAG_CNT_1							
R/W							
4Ch							
7	6	5	4	3	2	1	0
FRAG_CNT_0							
R/W							
E6h							

Table 4-1830. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_FRAG_CNT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	FRAG_CNT_3	R/W	B3h	FRAG Cnt3 pattern
23:16	FRAG_CNT_2	R/W	7Fh	FRAG Cnt2 pattern
15:8	FRAG_CNT_1	R/W	4Ch	FRAG Cnt1 pattern
7:0	FRAG_CNT_0	R/W	E6h	FRAG Cnt0 pattern

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4.2.2.407 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE0 Register

4.2.2.407.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE0 Register (Offset = D00h) [reset = 0h]

Queue0

Return to Summary Table

Table 4-1831. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D00h

Figure 4-893. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR0							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR0							
R/W							
0h							

Table 4-1832. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR0	R/W	0h	Queue 0

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4.2.2.408 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE1 Register

4.2.2.408.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE1 Register (Offset = D04h) [reset = 0h]

Queue1

Return to Summary Table

Table 4-1833. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D04h

Figure 4-894. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR1							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR1							
R/W							
0h							

Table 4-1834. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR1	R/W	0h	Queue 1

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4.2.2.409 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE2 Register

4.2.2.409.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE2 Register (Offset = D08h) [reset = 0h]

Queue2

Return to Summary Table

Table 4-1835. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D08h

Figure 4-895. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR2							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR2							
R/W							
0h							

Table 4-1836. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR2	R/W	0h	Queue 2

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4.2.2.410 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE3 Register

4.2.2.410.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE3 Register (Offset = D0Ch) [reset = 0h]

Queue3

Return to Summary Table

Table 4-1837. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D0Ch

Figure 4-896. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR3							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR3							
R/W							
0h							

Table 4-1838. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR3	R/W	0h	Queue 3

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4.2.2.411 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE4 Register

4.2.2.411.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE4 Register (Offset = D10h) [reset = 0h]

Queue4

Return to Summary Table

Table 4-1839. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D10h

Figure 4-897. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR4							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR4							
R/W							
0h							

Table 4-1840. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR4	R/W	0h	Queue 4

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4.2.2.412 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE5 Register

4.2.2.412.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE5 Register (Offset = D14h) [reset = 0h]

Queue5

Return to Summary Table

Table 4-1841. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D14h

Figure 4-898. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR5							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR5							
R/W							
0h							

Table 4-1842. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR5	R/W	0h	Queue 5

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4.2.2.413 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE6 Register

4.2.2.413.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE6 Register (Offset = D18h) [reset = 0h]

Queue6

Return to Summary Table

Table 4-1843. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D18h

Figure 4-899. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR6							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR6							
R/W							
0h							

Table 4-1844. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR6	R/W	0h	Queue 6

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4.2.2.414 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE7 Register

4.2.2.414.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE7 Register (Offset = D1Ch) [reset = 0h]

Queue7

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Table 4-1845. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D1Ch

Figure 4-900. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR7							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR7							
R/W							
0h							

Table 4-1846. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR7	R/W	0h	Queue 7

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4.2.2.415 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE8 Register

4.2.2.415.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE8 Register (Offset = D20h) [reset = 0h]

Queue8

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Table 4-1847. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D20h

Figure 4-901. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR8							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR8							
R/W							
0h							

Table 4-1848. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR8	R/W	0h	Queue 8

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4.2.2.416 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE9 Register

4.2.2.416.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE9 Register (Offset = D24h) [reset = 0h]

Queue9

Return to Summary Table

Table 4-1849. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D24h

Figure 4-902. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR9							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR9							
R/W							
0h							

Table 4-1850. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR9	R/W	0h	Queue 9

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4.2.2.417 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE10 Register

4.2.2.417.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE10 Register (Offset = D28h) [reset = 0h]

Queue10

Return to Summary Table

Table 4-1851. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D28h

Figure 4-903. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR10							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR10							
R/W							
0h							

Table 4-1852. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR10	R/W	0h	Queue 10

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4.2.2.418 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE11 Register

4.2.2.418.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE11 Register (Offset = D2Ch) [reset = 0h]

Queue11

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Table 4-1853. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D2Ch

Figure 4-904. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR11							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR11							
R/W							
0h							

Table 4-1854. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR11	R/W	0h	Queue 11

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4.2.2.419 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE12 Register

4.2.2.419.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE12 Register (Offset = D30h) [reset = 0h]

Queue12

Return to Summary Table

Table 4-1855. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D30h

Figure 4-905. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR12							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR12							
R/W							
0h							

Table 4-1856. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR12	R/W	0h	Queue 12

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4.2.2.420 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE13 Register

4.2.2.420.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE13 Register (Offset = D34h) [reset = 0h]

Queue13

Return to Summary Table

Table 4-1857. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D34h

Figure 4-906. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR13							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR13							
R/W							
0h							

Table 4-1858. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR13	R/W	0h	Queue 13

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4.2.2.421 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE14 Register

4.2.2.421.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE14 Register (Offset = D38h) [reset = 0h]

Queue14

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Table 4-1859. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D38h

Figure 4-907. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR14							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR14							
R/W							
0h							

Table 4-1860. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR14	R/W	0h	Queue 14

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4.2.2.422 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE15 Register

4.2.2.422.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE15 Register (Offset = D3Ch) [reset = 0h]

Queue15

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Table 4-1861. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D3Ch

Figure 4-908. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR15							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR15							
R/W							
0h							

Table 4-1862. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR15	R/W	0h	Queue 15

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4.2.2.423 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE16 Register

4.2.2.423.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE16 Register (Offset = D40h) [reset = 0h]

Queue16

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Table 4-1863. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D40h

Figure 4-909. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR16							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR16							
R/W							
0h							

Table 4-1864. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR16	R/W	0h	Queue 16

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4.2.2.424 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE17 Register

4.2.2.424.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE17 Register (Offset = D44h) [reset = 0h]

Queue17

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Table 4-1865. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D44h

Figure 4-910. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR17							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR17							
R/W							
0h							

Table 4-1866. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR17	R/W	0h	Queue 17

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4.2.2.425 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE18 Register

4.2.2.425.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE18 Register (Offset = D48h) [reset = 0h]

Queue18

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Table 4-1867. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D48h

Figure 4-911. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR18							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR18							
R/W							
0h							

Table 4-1868. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR18	R/W	0h	Queue 18

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4.2.2.426 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE19 Register

4.2.2.426.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE19 Register (Offset = D4Ch) [reset = 0h]

Queue19

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Table 4-1869. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D4Ch

Figure 4-912. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR19							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR19							
R/W							
0h							

Table 4-1870. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR19	R/W	0h	Queue 19

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4.2.2.427 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE20 Register

4.2.2.427.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE20 Register (Offset = D50h) [reset = 0h]

Queue20

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Table 4-1871. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D50h

Figure 4-913. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR20							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR20							
R/W							
0h							

Table 4-1872. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR20	R/W	0h	Queue 20

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4.2.2.428 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE21 Register

4.2.2.428.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE21 Register (Offset = D54h) [reset = 0h]

Queue21

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Table 4-1873. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D54h

Figure 4-914. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR21							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR21							
R/W							
0h							

Table 4-1874. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR21	R/W	0h	Queue 21

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4.2.2.429 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE22 Register

4.2.2.429.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE22 Register (Offset = D58h) [reset = 0h]

Queue22

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Table 4-1875. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D58h

Figure 4-915. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR22							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR22							
R/W							
0h							

Table 4-1876. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR22	R/W	0h	Queue 22

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4.2.2.430 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE23 Register

4.2.2.430.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE23 Register (Offset = D5Ch) [reset = 0h]

Queue23

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Table 4-1877. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D5Ch

Figure 4-916. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR23							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR23							
R/W							
0h							

Table 4-1878. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR23	R/W	0h	Queue 23

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4.2.2.431 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE24 Register

4.2.2.431.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE24 Register (Offset = D60h) [reset = 0h]

Queue24

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Table 4-1879. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D60h

Figure 4-917. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR24							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR24							
R/W							
0h							

Table 4-1880. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR24	R/W	0h	Queue 24

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4.2.2.432 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE25 Register

4.2.2.432.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE25 Register (Offset = D64h) [reset = 0h]

Queue25

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Table 4-1881. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D64h

Figure 4-918. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR25							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR25							
R/W							
0h							

Table 4-1882. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR25	R/W	0h	Queue 25

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4.2.2.433 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE26 Register

4.2.2.433.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE26 Register (Offset = D68h) [reset = 0h]

Queue26

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Table 4-1883. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D68h

Figure 4-919. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR26							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR26							
R/W							
0h							

Table 4-1884. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR26	R/W	0h	Queue 26

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4.2.2.434 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE27 Register

4.2.2.434.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE27 Register (Offset = D6Ch) [reset = 0h]

Queue27

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Table 4-1885. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D6Ch

Figure 4-920. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR27							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR27							
R/W							
0h							

Table 4-1886. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR27	R/W	0h	Queue 27

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4.2.2.435 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE28 Register

4.2.2.435.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE28 Register (Offset = D70h) [reset = 0h]

Queue28

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Table 4-1887. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D70h

Figure 4-921. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR28							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR28							
R/W							
0h							

Table 4-1888. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR28	R/W	0h	Queue 28

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4.2.2.436 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE29 Register

4.2.2.436.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE29 Register (Offset = D74h) [reset = 0h]

Queue29

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Table 4-1889. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D74h

Figure 4-922. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR29							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR29							
R/W							
0h							

Table 4-1890. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR29	R/W	0h	Queue 29

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4.2.2.437 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE30 Register

4.2.2.437.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE30 Register (Offset = D78h) [reset = 0h]

Queue30

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Table 4-1891. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D78h

Figure 4-923. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR30							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR30							
R/W							
0h							

Table 4-1892. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR30	R/W	0h	Queue 30

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4.2.2.438 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE31 Register

4.2.2.438.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE31 Register (Offset = D7Ch) [reset = 0h]

Queue31

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Table 4-1893. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3D7Ch

Figure 4-924. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PTR31							
R/W							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PTR31							
R/W							
0h							

Table 4-1894. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PTR31	R/W	0h	Queue 31

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4.2.2.439 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK0 Register

4.2.2.439.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK0 Register (Offset = E00h) [reset = 0h]

QueuePeek0

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Table 4-1895. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E00h

Figure 4-925. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR0							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR0							
R							
0h							

Table 4-1896. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR0	R	0h	Queue 0 Peek portal

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4.2.2.440 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK1 Register

4.2.2.440.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK1 Register (Offset = E04h) [reset = 0h]

QueuePeek1

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Table 4-1897. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E04h

Figure 4-926. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR1							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR1							
R							
0h							

Table 4-1898. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR1	R	0h	Queue 1 Peek portal

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4.2.2.441 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK2 Register

4.2.2.441.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK2 Register (Offset = E08h) [reset = 0h]

QueuePeek2

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Table 4-1899. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E08h

Figure 4-927. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR2							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR2							
R							
0h							

Table 4-1900. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR2	R	0h	Queue 2 Peek portal

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4.2.2.442 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK3 Register

4.2.2.442.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK3 Register (Offset = E0Ch) [reset = 0h]

QueuePeek3

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Table 4-1901. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E0Ch

Figure 4-928. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR3							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR3							
R							
0h							

Table 4-1902. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR3	R	0h	Queue 3 Peek portal

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4.2.2.443 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK4 Register

4.2.2.443.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK4 Register (Offset = E10h) [reset = 0h]

QueuePeek4

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Table 4-1903. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E10h

Figure 4-929. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR4							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR4							
R							
0h							

Table 4-1904. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR4	R	0h	Queue 4 Peek portal

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4.2.2.444 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK5 Register

4.2.2.444.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK5 Register (Offset = E14h) [reset = 0h]

QueuePeek5

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Table 4-1905. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E14h

Figure 4-930. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR5							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR5							
R							
0h							

Table 4-1906. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR5	R	0h	Queue 5 Peek portal

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4.2.2.445 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK6 Register

4.2.2.445.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK6 Register (Offset = E18h) [reset = 0h]

QueuePeek6

Return to Summary Table

Table 4-1907. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E18h

Figure 4-931. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR6							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR6							
R							
0h							

Table 4-1908. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR6	R	0h	Queue 6 Peek portal

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4.2.2.446 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK7 Register

4.2.2.446.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK7 Register (Offset = E1Ch) [reset = 0h]

QueuePeek7

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Table 4-1909. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E1Ch

Figure 4-932. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR7							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR7							
R							
0h							

Table 4-1910. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR7	R	0h	Queue 7 Peek portal

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4.2.2.447 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK8 Register

4.2.2.447.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK8 Register (Offset = E20h) [reset = 0h]

QueuePeek8

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Table 4-1911. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E20h

Figure 4-933. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR8							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR8							
R							
0h							

Table 4-1912. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR8	R	0h	Queue 8 Peek portal

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4.2.2.448 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK9 Register

4.2.2.448.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK9 Register (Offset = E24h) [reset = 0h]

QueuePeek9

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Table 4-1913. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E24h

Figure 4-934. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR9							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR9							
R							
0h							

Table 4-1914. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR9	R	0h	Queue 9 Peek portal

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4.2.2.449 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK10 Register

4.2.2.449.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK10 Register (Offset = E28h) [reset = 0h]

QueuePeek10

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Table 4-1915. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E28h

Figure 4-935. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR10							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR10							
R							
0h							

Table 4-1916. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR10	R	0h	Queue 10 Peek portal

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4.2.2.450 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK11 Register

4.2.2.450.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK11 Register (Offset = E2Ch) [reset = 0h]

QueuePeek11

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Table 4-1917. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E2Ch

Figure 4-936. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR11							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR11							
R							
0h							

Table 4-1918. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR11	R	0h	Queue 11 Peek portal

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4.2.2.451 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK12 Register

4.2.2.451.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK12 Register (Offset = E30h) [reset = 0h]

QueuePeek12

Return to Summary Table

Table 4-1919. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E30h

Figure 4-937. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR12							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR12							
R							
0h							

Table 4-1920. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR12	R	0h	Queue 12 Peek portal

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4.2.2.452 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK13 Register

4.2.2.452.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK13 Register (Offset = E34h) [reset = 0h]

QueuePeek13

Return to Summary Table

Table 4-1921. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E34h

Figure 4-938. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR13							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR13							
R							
0h							

Table 4-1922. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR13	R	0h	Queue 13 Peek portal

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4.2.2.453 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK14 Register

4.2.2.453.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK14 Register (Offset = E38h) [reset = 0h]

QueuePeek14

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Table 4-1923. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E38h

Figure 4-939. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR14							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR14							
R							
0h							

Table 4-1924. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR14	R	0h	Queue 14 Peek portal

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4.2.2.454 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK15 Register

4.2.2.454.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK15 Register (Offset = E3Ch) [reset = 0h]

QueuePeek15

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Table 4-1925. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E3Ch

Figure 4-940. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_H_PEEK_PTR15							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_H_PEEK_PTR15							
R							
0h							

Table 4-1926. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_PEEK15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_H_PEEK_PTR15	R	0h	Queue 15 Peek portal

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4.2.2.455 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT0 Register

4.2.2.455.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT0 Register (Offset = E40h) [reset = 0h]

QueueCnt0

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Table 4-1927. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E40h

Figure 4-941. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_0							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_0							
R							
0h							

Table 4-1928. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_0	R	0h	Queue Entry Count0

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4.2.2.456 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT1 Register

4.2.2.456.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT1 Register (Offset = E44h) [reset = 0h]

QueueCnt1

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Table 4-1929. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E44h

Figure 4-942. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_1							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_1							
R							
0h							

Table 4-1930. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_1	R	0h	Queue Entry Count1

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4.2.2.457 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT2 Register

4.2.2.457.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT2 Register (Offset = E48h) [reset = 0h]

QueueCnt2

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Table 4-1931. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E48h

Figure 4-943. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_2							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_2							
R							
0h							

Table 4-1932. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_2	R	0h	Queue Entry Count2

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4.2.2.458 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT3 Register

4.2.2.458.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT3 Register (Offset = E4Ch) [reset = 0h]

QueueCnt3

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Table 4-1933. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E4Ch

Figure 4-944. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_3							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_3							
R							
0h							

Table 4-1934. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_3	R	0h	Queue Entry Count3

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4.2.2.459 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT4 Register

4.2.2.459.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT4 Register (Offset = E50h) [reset = 0h]

QueueCnt4

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Table 4-1935. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E50h

Figure 4-945. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_4							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_4							
R							
0h							

Table 4-1936. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_4	R	0h	Queue Entry Count4

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4.2.2.460 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT5 Register

4.2.2.460.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT5 Register (Offset = E54h) [reset = 0h]

QueueCnt5

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Table 4-1937. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E54h

Figure 4-946. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_5							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_5							
R							
0h							

Table 4-1938. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_5	R	0h	Queue Entry Count5

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4.2.2.461 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT6 Register

4.2.2.461.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT6 Register (Offset = E58h) [reset = 0h]

QueueCnt6

Return to Summary Table

Table 4-1939. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E58h

Figure 4-947. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_6							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_6							
R							
0h							

Table 4-1940. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_6	R	0h	Queue Entry Count6

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4.2.2.462 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT7 Register

4.2.2.462.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT7 Register (Offset = E5Ch) [reset = 0h]

QueueCnt7

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Table 4-1941. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E5Ch

Figure 4-948. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT7 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_7							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_7							
R							
0h							

Table 4-1942. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_7	R	0h	Queue Entry Count7

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4.2.2.463 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT8 Register

4.2.2.463.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT8 Register (Offset = E60h) [reset = 0h]

QueueCnt8

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Table 4-1943. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E60h

Figure 4-949. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_8							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_8							
R							
0h							

Table 4-1944. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_8	R	0h	Queue Entry Count8

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4.2.2.464 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT9 Register

4.2.2.464.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT9 Register (Offset = E64h) [reset = 0h]

QueueCnt9

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Table 4-1945. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E64h

Figure 4-950. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT9 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_9							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_9							
R							
0h							

Table 4-1946. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_9	R	0h	Queue Entry Count9

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4.2.2.465 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT10 Register

4.2.2.465.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT10 Register (Offset = E68h) [reset = 0h]

QueueCnt10

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Table 4-1947. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E68h

Figure 4-951. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT10 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_10							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_10							
R							
0h							

Table 4-1948. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_10	R	0h	Queue Entry Count10

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4.2.2.466 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT11 Register

4.2.2.466.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT11 Register (Offset = E6Ch) [reset = 0h]

QueueCnt11

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Table 4-1949. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E6Ch

Figure 4-952. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT11 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_11							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_11							
R							
0h							

Table 4-1950. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_11	R	0h	Queue Entry Count11

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4.2.2.467 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT12 Register

4.2.2.467.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT12 Register (Offset = E70h) [reset = 0h]

QueueCnt12

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Table 4-1951. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E70h

Figure 4-953. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT12 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_12							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_12							
R							
0h							

Table 4-1952. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_12	R	0h	Queue Entry Count12

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4.2.2.468 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT13 Register

4.2.2.468.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT13 Register (Offset = E74h) [reset = 0h]

QueueCnt13

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Table 4-1953. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E74h

Figure 4-954. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT13 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_13							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_13							
R							
0h							

Table 4-1954. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_13	R	0h	Queue Entry Count13

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4.2.2.469 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT14 Register

4.2.2.469.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT14 Register (Offset = E78h) [reset = 0h]

QueueCnt14

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Table 4-1955. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E78h

Figure 4-955. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT14 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_14							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_14							
R							
0h							

Table 4-1956. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_14	R	0h	Queue Entry Count14

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4.2.2.470 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT15 Register

4.2.2.470.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT15 Register (Offset = E7Ch) [reset = 0h]

QueueCnt15

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Table 4-1957. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E7Ch

Figure 4-956. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT15 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_15							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_15							
R							
0h							

Table 4-1958. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_15	R	0h	Queue Entry Count15

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4.2.2.471 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT16 Register

4.2.2.471.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT16 Register (Offset = E80h) [reset = 0h]

QueueCnt16

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Table 4-1959. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E80h

Figure 4-957. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT16 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_16							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_16							
R							
0h							

Table 4-1960. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_16	R	0h	Queue Entry Count16

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4.2.2.472 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT17 Register

4.2.2.472.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT17 Register (Offset = E84h) [reset = 0h]

QueueCnt17

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Table 4-1961. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E84h

Figure 4-958. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT17 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_17							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_17							
R							
0h							

Table 4-1962. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_17	R	0h	Queue Entry Count17

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4.2.2.473 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT18 Register

4.2.2.473.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT18 Register (Offset = E88h) [reset = 0h]

QueueCnt18

Return to Summary Table

Table 4-1963. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E88h

Figure 4-959. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT18 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_18							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_18							
R							
0h							

Table 4-1964. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_18	R	0h	Queue Entry Count18

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4.2.2.474 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT19 Register

4.2.2.474.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT19 Register (Offset = E8Ch) [reset = 0h]

QueueCnt19

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Table 4-1965. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E8Ch

Figure 4-960. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT19 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_19							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_19							
R							
0h							

Table 4-1966. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_19	R	0h	Queue Entry Count19

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4.2.2.475 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT20 Register

4.2.2.475.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT20 Register (Offset = E90h) [reset = 0h]

QueueCnt20

Return to Summary Table

Table 4-1967. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E90h

Figure 4-961. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT20 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_20							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_20							
R							
0h							

Table 4-1968. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_20	R	0h	Queue Entry Count20

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4.2.2.476 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT21 Register

4.2.2.476.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT21 Register (Offset = E94h) [reset = 0h]

QueueCnt21

Return to Summary Table

Table 4-1969. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E94h

Figure 4-962. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT21 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_21							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_21							
R							
0h							

Table 4-1970. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_21	R	0h	Queue Entry Count21

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4.2.2.477 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT22 Register

4.2.2.477.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT22 Register (Offset = E98h) [reset = 0h]

QueueCnt22

Return to Summary Table

Table 4-1971. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E98h

Figure 4-963. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT22 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_22							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_22							
R							
0h							

Table 4-1972. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_22	R	0h	Queue Entry Count22

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4.2.2.478 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT23 Register

4.2.2.478.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT23 Register (Offset = E9Ch) [reset = 0h]

QueueCnt23

Return to Summary Table

Table 4-1973. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3E9Ch

Figure 4-964. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT23 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_23							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_23							
R							
0h							

Table 4-1974. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_23	R	0h	Queue Entry Count23

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4.2.2.479 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT24 Register

4.2.2.479.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT24 Register (Offset = EA0h) [reset = 0h]

QueueCnt24

Return to Summary Table

Table 4-1975. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3EA0h

Figure 4-965. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT24 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_24							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_24							
R							
0h							

Table 4-1976. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_24	R	0h	Queue Entry Count24

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4.2.2.480 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT25 Register

4.2.2.480.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT25 Register (Offset = EA4h) [reset = 0h]

QueueCnt25

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Table 4-1977. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3EA4h

Figure 4-966. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT25 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_25							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_25							
R							
0h							

Table 4-1978. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_25	R	0h	Queue Entry Count25

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4.2.2.481 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT26 Register

4.2.2.481.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT26 Register (Offset = EA8h) [reset = 0h]

QueueCnt26

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Table 4-1979. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3EA8h

Figure 4-967. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT26 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_26							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_26							
R							
0h							

Table 4-1980. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_26	R	0h	Queue Entry Count26

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4.2.2.482 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT27 Register

4.2.2.482.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT27 Register (Offset = EACh) [reset = 0h]

QueueCnt27

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Table 4-1981. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3EACh

Figure 4-968. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT27 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_27							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_27							
R							
0h							

Table 4-1982. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_27	R	0h	Queue Entry Count27

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4.2.2.483 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT28 Register

4.2.2.483.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT28 Register (Offset = EB0h) [reset = 0h]

QueueCnt28

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Table 4-1983. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3EB0h

Figure 4-969. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT28 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_28							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_28							
R							
0h							

Table 4-1984. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_28	R	0h	Queue Entry Count28

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4.2.2.484 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT29 Register

4.2.2.484.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT29 Register (Offset = EB4h) [reset = 0h]

QueueCnt29

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Table 4-1985. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3EB4h

Figure 4-970. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT29 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_29							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_29							
R							
0h							

Table 4-1986. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_29	R	0h	Queue Entry Count29

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4.2.2.485 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT30 Register

4.2.2.485.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT30 Register (Offset = EB8h) [reset = 0h]

QueueCnt30

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Table 4-1987. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3EB8h

Figure 4-971. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT30 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_30							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_30							
R							
0h							

Table 4-1988. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_30	R	0h	Queue Entry Count30

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4.2.2.486 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT31 Register

4.2.2.486.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT31 Register (Offset = EBCh) [reset = 0h]

QueueCnt31

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Table 4-1989. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3EBCh

Figure 4-972. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT31 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
QUEUE_CNT_ENTRIES_31							
R							
0h							
7	6	5	4	3	2	1	0
QUEUE_CNT_ENTRIES_31							
R							
0h							

Table 4-1990. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_CNT31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	QUEUE_CNT_ENTRIES_31	R	0h	Queue Entry Count31

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4.2.2.487 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_RESET Register

4.2.2.487.1 ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_RESET Register (Offset = F40h) [reset = 0h]

QueueReset32

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Table 4-1991. Instance Table

Instance Name	Physical Address
ICSSM0	4803 3F40h

Figure 4-973. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_RESET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		RESET_QUEUE_ID					
NONE		R/W					
0h		0h					

Table 4-1992. ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	RESET_QUEUE_ID	R/W	0h	Reset Queue ID

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4.2.2.488 ICSSM_PR1_PDSP0_IRAM_RAM_IRAM Register

4.2.2.488.1 ICSSM_PR1_PDSP0_IRAM_RAM_IRAM Register (Offset = 0h) [reset = 0h]

PDSP instruction RAM.

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Table 4-1993. Instance Table

Instance Name	Physical Address
ICSSM0	4803 4000h

Figure 4-974. ICSSM_PR1_PDSP0_IRAM_RAM_IRAM Name Register

31	30	29	28	27	26	25	24
VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 4-1994. ICSSM_PR1_PDSP0_IRAM_RAM_IRAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE	R/W	0h	PDSP IRAM

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4.2.2.489 ICSSM_PR1_PDSP1_IRAM_RAM_IRAM Register

4.2.2.489.1 ICSSM_PR1_PDSP1_IRAM_RAM_IRAM Register (Offset = 0h) [reset = 0h]

PDSP instruction RAM.

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Table 4-1995. Instance Table

Instance Name	Physical Address
ICSSM0	4803 8000h

Figure 4-975. ICSSM_PR1_PDSP1_IRAM_RAM_IRAM Name Register

31	30	29	28	27	26	25	24
VALUE							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE							
R/W							
0h							

Table 4-1996. ICSSM_PR1_PDSP1_IRAM_RAM_IRAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE	R/W	0h	PDSP IRAM

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4.2.2.490 ECC_AGGR_REV Register

4.2.2.490.1 ECC_AGGR_REV Register (Offset = 0h) [reset = 66A0EA00h]

Revision parameters.

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Table 4-1997. Instance Table

Instance Name	Physical Address
ICSSM0	4810 0000h

Figure 4-976. ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
1Dh					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 4-1998. ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	1Dh	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

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4.2.2.491 ECC_AGGR_VECTOR Register

4.2.2.491.1 ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register.

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Table 4-1999. Instance Table

Instance Name	Physical Address
ICSSM0	4810 0008h

Figure 4-977. ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 4-2000. ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

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4.2.2.492 ECC_AGGR_STAT Register

4.2.2.492.1 ECC_AGGR_STAT Register (Offset = Ch) [reset = 5h]

Misc Status.

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Table 4-2001. Instance Table

Instance Name	Physical Address
ICSSM0	4810 000Ch

Figure 4-978. ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					5h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
5h							

Table 4-2002. ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	5h	Indicates the number of RAMS serviced by the ECC aggregator

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4.2.2.493 ECC_AGGR_RESERVED_SVBUS_J Register

4.2.2.493.1 ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 4-2003. Instance Table

Instance Name	Physical Address
ICSSM0	4810 0010h + formula

Figure 4-979. ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 4-2004. ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

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4.2.2.494 ECC_AGGR_SEC_EOI_REG Register

4.2.2.494.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

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Table 4-2005. Instance Table

Instance Name	Physical Address
ICSSM0	4810 003Ch

Figure 4-980. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 4-2006. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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4.2.2.495 ECC_AGGR_SEC_STATUS_REG0 Register

4.2.2.495.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 4-2007. Instance Table

Instance Name	Physical Address
ICSSM0	4810 0040h

Figure 4-981. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PR1_RAM_PEND	PR1_PDSP1_IRAM_PEND	PR1_PDSP0_IRAM_PEND	PR1_DRAM1_PEND	PR1_DRAM0_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 4-2008. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	PR1_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for pr1_ram_pend
3	PR1_PDSP1_IRAM_PEND	R/W1TS	0h	Interrupt Pending Status for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_PEND	R/W1TS	0h	Interrupt Pending Status for pr1_pdsp0_iram_pend
1	PR1_DRAM1_PEND	R/W1TS	0h	Interrupt Pending Status for pr1_dram1_pend
0	PR1_DRAM0_PEND	R/W1TS	0h	Interrupt Pending Status for pr1_dram0_pend

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4.2.2.496 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

4.2.2.496.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 4-2009. Instance Table

Instance Name	Physical Address
ICSSM0	4810 0080h

Figure 4-982. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PR1_RAM_ENABLE_SET	PR1_PDSP1_IRAM_ENABLE_SET	PR1_PDSP0_IRAM_ENABLE_SET	PR1_DRAM1_ENABLE_SET	PR1_DRAM0_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 4-2010. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	PR1_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pr1_dram1_pend
0	PR1_DRAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pr1_dram0_pend

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4.2.2.497 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

4.2.2.497.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 4-2011. Instance Table

Instance Name	Physical Address
ICSSM0	4810 00C0h

Figure 4-983. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PR1_RAM_ENABLE_CLR	PR1_PDSP1_IRAM_ENABLE_CLR	PR1_PDSP0_IRAM_ENABLE_CLR	PR1_DRAM1_ENABLE_CLR	PR1_DRAM0_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 4-2012. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	PR1_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pr1_dram1_pend
0	PR1_DRAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pr1_dram0_pend

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4.2.2.498 ECC_AGGR_DED_EOI_REG Register

4.2.2.498.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

Return to Summary Table

Table 4-2013. Instance Table

Instance Name	Physical Address
ICSSM0	4810 013Ch

Figure 4-984. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 4-2014. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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4.2.2.499 ECC_AGGR_DED_STATUS_REG0 Register

4.2.2.499.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 4-2015. Instance Table

Instance Name	Physical Address
ICSSM0	4810 0140h

Figure 4-985. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PR1_RAM_PEND	PR1_PDSP1_IRAM_PEND	PR1_PDSP0_IRAM_PEND	PR1_DRAM1_PEND	PR1_DRAM0_PEND
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 4-2016. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	PR1_RAM_PEND	R/W1TS	0h	Interrupt Pending Status for pr1_ram_pend
3	PR1_PDSP1_IRAM_PEND	R/W1TS	0h	Interrupt Pending Status for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_PEND	R/W1TS	0h	Interrupt Pending Status for pr1_pdsp0_iram_pend
1	PR1_DRAM1_PEND	R/W1TS	0h	Interrupt Pending Status for pr1_dram1_pend
0	PR1_DRAM0_PEND	R/W1TS	0h	Interrupt Pending Status for pr1_dram0_pend

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4.2.2.500 ECC_AGGR_DED_ENABLE_SET_REG0 Register

4.2.2.500.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 4-2017. Instance Table

Instance Name	Physical Address
ICSSM0	4810 0180h

Figure 4-986. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PR1_RAM_ENABLE_SET	PR1_PDSP1_IRAM_ENABLE_SET	PR1_PDSP0_IRAM_ENABLE_SET	PR1_DRAM1_ENABLE_SET	PR1_DRAM0_ENABLE_SET
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 4-2018. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	PR1_RAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pr1_dram1_pend
0	PR1_DRAM0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for pr1_dram0_pend

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4.2.2.501 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

4.2.2.501.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 4-2019. Instance Table

Instance Name	Physical Address
ICSSM0	4810 01C0h

Figure 4-987. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			PR1_RAM_ENABLE_CLR	PR1_PDSP1_IRAM_ENABLE_CLR	PR1_PDSP0_IRAM_ENABLE_CLR	PR1_DRAM1_ENABLE_CLR	PR1_DRAM0_ENABLE_CLR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 4-2020. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	PR1_RAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pr1_ram_pend
3	PR1_PDSP1_IRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pr1_pdsp1_iram_pend
2	PR1_PDSP0_IRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pr1_pdsp0_iram_pend
1	PR1_DRAM1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pr1_dram1_pend
0	PR1_DRAM0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for pr1_dram0_pend

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4.2.2.502 ECC_AGGR_AGGR_ENABLE_SET Register

4.2.2.502.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register.

Return to Summary Table

Table 4-2021. Instance Table

Instance Name	Physical Address
ICSSM0	4810 0200h

Figure 4-988. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 4-2022. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	Interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	Interrupt enable set for parity errors

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4.2.2.503 ECC_AGGR_AGGR_ENABLE_CLR Register

4.2.2.503.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register.

Return to Summary Table

Table 4-2023. Instance Table

Instance Name	Physical Address
ICSSM0	4810 0204h

Figure 4-989. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 4-2024. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	Interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	Interrupt enable clear for parity errors

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4.2.2.504 ECC_AGGR_AGGR_STATUS_SET Register

4.2.2.504.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register.

Return to Summary Table

Table 4-2025. Instance Table

Instance Name	Physical Address
ICSSM0	4810 0208h

Figure 4-990. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 4-2026. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	Interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	Interrupt status set for parity errors

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4.2.2.505 ECC_AGGR_AGGR_STATUS_CLR Register

4.2.2.505.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register.

Return to Summary Table

Table 4-2027. Instance Table

Instance Name	Physical Address
ICSSM0	4810 020Ch

Figure 4-991. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 4-2028. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	Interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	Interrupt status clear for parity errors

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4.3 ICSSM_XBAR_INTR

ICSSM_XBAR_INTR

4.3.1 ICSSM_XBAR_INTR Summaries

ICSSM_XBAR_INTR Summaries

Table 4-2029. ICSSM_XBAR_INTR Registers, Base Address=52E0 3000h, Length=256

Offset	Length	Register Name	ICSSM_XBAR_INTR Physical Address
0h	32	ICSSM_XBAR_INTR_PID	52E0 3000h
4h	32	ICSSM_XBAR_INTR_MUXCNTL_J	52E0 3004h + formula

4.3.2 ICSSM_XBAR_INTR Registers

ICSSM_XBAR_INTR Registers

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4.3.2.1 ICSSM_XBAR_INTR_PID Register

4.3.2.1.1 ICSSM_XBAR_INTR_PID Register (Offset = 0h) [reset = 66948100h]

Identification register.

Return to Summary Table

Table 4-2030. Instance Table

Instance Name	Physical Address
ICSSM_XBAR_INTR	52E0 3000h

Figure 4-992. ICSSM_XBAR_INTR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
694h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTLVER					MAJREV		
R					R		
10h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINREV					
R		R					
0h		0h					

Table 4-2031. ICSSM_XBAR_INTR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	FUNCTION	R	694h	function
15:11	RTLVER	R	10h	Rtl version
10:8	MAJREV	R	1h	major version
7:6	CUSTOM	R	0h	custom id
5:0	MINREV	R	0h	minor version

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4.3.2.2 ICSSM_XBAR_INTR_MUXCNTL_J Register

4.3.2.2.1 ICSSM_XBAR_INTR_MUXCNTL_J Register (Offset = 4h) [reset = 0h]

Interrupt mux control register.

Return to Summary Table

Table 4-2032. Instance Table

Instance Name	Physical Address
ICSSM_XBAR_INTR	52E0 3004h + formula

Figure 4-993. ICSSM_XBAR_INTR_MUXCNTL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							INT_ENABLE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MUX_CNTL						
NONE	R/W						
0h	0h						

Table 4-2033. ICSSM_XBAR_INTR_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	Interrupt *j* Output Enable.
15:7	RESERVED	NONE	0h	Reserved
6:0	MUX_CNTL	R/W	0h	Mux Control for Interrupt *j*.

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4.4 EDMA

EDMA

4.4.1 EDMA Summaries

EDMA Summaries

Table 4-2034. TPCC Registers, Base Address=52A0 0000h, Length=32768

Offset	Length	Register Name	EDMA0 Physical Address
0h	32	TPCC_PID	52A0 0000h
4h	32	TPCC_CCCFG	52A0 0004h
100h	32	TPCC_DCHMAPN	52A0 0100h
200h	32	TPCC_QCHMAPN	52A0 0200h
240h	32	TPCC_DMAQNUMN	52A0 0240h
260h	32	TPCC_QDMAQNUM	52A0 0260h
280h	32	TPCC_QUETCMAP	52A0 0280h
284h	32	TPCC_QUEPRI	52A0 0284h
300h	32	TPCC_EMR	52A0 0300h
304h	32	TPCC_EMRH	52A0 0304h
308h	32	TPCC_EMCR	52A0 0308h
30Ch	32	TPCC_EMCRH	52A0 030Ch
310h	32	TPCC_QEMR	52A0 0310h
314h	32	TPCC_QEMCR	52A0 0314h
318h	32	TPCC_CCERR	52A0 0318h
31Ch	32	TPCC_CCERRCLR	52A0 031Ch
320h	32	TPCC_EEVAL	52A0 0320h
340h	32	TPCC_DRAEM	52A0 0340h
344h	32	TPCC_DRAEHM	52A0 0344h
380h	32	TPCC_QRAEN	52A0 0380h
400h	32	TPCC_QNE0	52A0 0400h
404h	32	TPCC_QNE1	52A0 0404h
408h	32	TPCC_QNE2	52A0 0408h
40Ch	32	TPCC_QNE3	52A0 040Ch
410h	32	TPCC_QNE4	52A0 0410h
414h	32	TPCC_QNE5	52A0 0414h
418h	32	TPCC_QNE6	52A0 0418h
41Ch	32	TPCC_QNE7	52A0 041Ch
420h	32	TPCC_QNE8	52A0 0420h
424h	32	TPCC_QNE9	52A0 0424h
428h	32	TPCC_QNE10	52A0 0428h
42Ch	32	TPCC_QNE11	52A0 042Ch
430h	32	TPCC_QNE12	52A0 0430h
434h	32	TPCC_QNE13	52A0 0434h
438h	32	TPCC_QNE14	52A0 0438h
43Ch	32	TPCC_QNE15	52A0 043Ch
600h	32	TPCC_QSTATN	52A0 0600h
620h	32	TPCC_QWMTHRA	52A0 0620h
640h	32	TPCC_CCSTAT	52A0 0640h
700h	32	TPCC_AETCTL	52A0 0700h

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Table 4-2034. TPCC Registers, Base Address=52A0 0000h, Length=32768 (continued)

Offset	Length	Register Name	EDMA0 Physical Address
704h	32	TPCC_AETSTAT	52A0 0704h
708h	32	TPCC_AETCMD	52A0 0708h
1000h	32	TPCC_ER	52A0 1000h
1004h	32	TPCC_ERH	52A0 1004h
1008h	32	TPCC_ECR	52A0 1008h
100Ch	32	TPCC_ECRH	52A0 100Ch
1010h	32	TPCC_ESR	52A0 1010h
1014h	32	TPCC_ESRH	52A0 1014h
1018h	32	TPCC_CER	52A0 1018h
101Ch	32	TPCC_CERH	52A0 101Ch
1020h	32	TPCC_EER	52A0 1020h
1024h	32	TPCC_EERH	52A0 1024h
1028h	32	TPCC_EECR	52A0 1028h
102Ch	32	TPCC_EECRH	52A0 102Ch
1030h	32	TPCC_EESR	52A0 1030h
1034h	32	TPCC_EESRH	52A0 1034h
1038h	32	TPCC_SER	52A0 1038h
103Ch	32	TPCC_SERH	52A0 103Ch
1040h	32	TPCC_SECR	52A0 1040h
1044h	32	TPCC_SECRH	52A0 1044h
1050h	32	TPCC_IER	52A0 1050h
1054h	32	TPCC_IERH	52A0 1054h
1058h	32	TPCC_IECR	52A0 1058h
105Ch	32	TPCC_IECRH	52A0 105Ch
1060h	32	TPCC_IESR	52A0 1060h
1064h	32	TPCC_IESRH	52A0 1064h
1068h	32	TPCC_IPR	52A0 1068h
106Ch	32	TPCC_IPRH	52A0 106Ch
1070h	32	TPCC_ICR	52A0 1070h
1074h	32	TPCC_ICRH	52A0 1074h
1078h	32	TPCC_IEVAL	52A0 1078h
1080h	32	TPCC_QER	52A0 1080h
1084h	32	TPCC_QEER	52A0 1084h
1088h	32	TPCC_QEECR	52A0 1088h
108Ch	32	TPCC_QEESR	52A0 108Ch
1090h	32	TPCC_QSER	52A0 1090h
1094h	32	TPCC_QSECR	52A0 1094h
2000h	32	TPCC_ER_RN	52A0 2000h
2004h	32	TPCC_ERH_RN	52A0 2004h
2008h	32	TPCC_ECR_RN	52A0 2008h
200Ch	32	TPCC_ECRH_RN	52A0 200Ch
2010h	32	TPCC_ESR_RN	52A0 2010h
2014h	32	TPCC_ESRH_RN	52A0 2014h
2018h	32	TPCC_CER_RN	52A0 2018h
201Ch	32	TPCC_CERH_RN	52A0 201Ch
2020h	32	TPCC_EER_RN	52A0 2020h
2024h	32	TPCC_EERH_RN	52A0 2024h

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Table 4-2034. TPCC Registers, Base Address=52A0 0000h, Length=32768 (continued)

Offset	Length	Register Name	EDMA0 Physical Address
2028h	32	TPCC_EECR_RN	52A0 2028h
202Ch	32	TPCC_EECRH_RN	52A0 202Ch
2030h	32	TPCC_EESR_RN	52A0 2030h
2034h	32	TPCC_EESRH_RN	52A0 2034h
2038h	32	TPCC_SER_RN	52A0 2038h
203Ch	32	TPCC_SERH_RN	52A0 203Ch
2040h	32	TPCC_SECR_RN	52A0 2040h
2044h	32	TPCC_SECRH_RN	52A0 2044h
2050h	32	TPCC_IER_RN	52A0 2050h
2054h	32	TPCC_IERH_RN	52A0 2054h
2058h	32	TPCC_IECR_RN	52A0 2058h
205Ch	32	TPCC_IECRH_RN	52A0 205Ch
2060h	32	TPCC_IESR_RN	52A0 2060h
2064h	32	TPCC_IESRH_RN	52A0 2064h
2068h	32	TPCC_IPR_RN	52A0 2068h
206Ch	32	TPCC_IPRH_RN	52A0 206Ch
2070h	32	TPCC_ICR_RN	52A0 2070h
2074h	32	TPCC_ICRH_RN	52A0 2074h
2078h	32	TPCC_IEVAL_RN	52A0 2078h
2080h	32	TPCC_QER_RN	52A0 2080h
2084h	32	TPCC_QEER_RN	52A0 2084h
2088h	32	TPCC_QEECR_RN	52A0 2088h
208Ch	32	TPCC_QEESR_RN	52A0 208Ch
2090h	32	TPCC_QSER_RN	52A0 2090h
2094h	32	TPCC_QSECR_RN	52A0 2094h
4000h	32	TPCC_OPT	52A0 4000h
4004h	32	TPCC_SRC	52A0 4004h
4008h	32	TPCC_ABCNT	52A0 4008h
400Ch	32	TPCC_DST	52A0 400Ch
4010h	32	TPCC_BIDX	52A0 4010h
4014h	32	TPCC_LNK	52A0 4014h
4018h	32	TPCC_CIDX	52A0 4018h
401Ch	32	TPCC_CCNT	52A0 401Ch

Table 4-2035. TPTC Registers, Base Address=52A4 0000h, Length=4096

Offset	Length	Register Name	EDMA0 Physical Address	EDMA1 Physical Address
0h	32	TPTC_PID	52A4 0000h	52A6 0000h
4h	32	TPTC_TCCFG	52A4 0004h	52A6 0004h
100h	32	TPTC_TCSTAT	52A4 0100h	52A6 0100h
104h	32	TPTC_INTSTAT	52A4 0104h	52A6 0104h
108h	32	TPTC_INTEN	52A4 0108h	52A6 0108h
10Ch	32	TPTC_INTCLR	52A4 010Ch	52A6 010Ch
110h	32	TPTC_INTCMD	52A4 0110h	52A6 0110h
120h	32	TPTC_ERRSTAT	52A4 0120h	52A6 0120h
124h	32	TPTC_ERREN	52A4 0124h	52A6 0124h
128h	32	TPTC_ERRCLR	52A4 0128h	52A6 0128h

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Table 4-2035. TPTC Registers, Base Address=52A4 0000h, Length=4096 (continued)

Offset	Length	Register Name	EDMA0 Physical Address	EDMA1 Physical Address
12Ch	32	TPTC_ERRDET	52A4 012Ch	52A6 012Ch
130h	32	TPTC_ERRCMD	52A4 0130h	52A6 0130h
140h	32	TPTC_RDRATE	52A4 0140h	52A6 0140h
200h	32	TPTC_POPT	52A4 0200h	52A6 0200h
204h	32	TPTC_PSRC	52A4 0204h	52A6 0204h
208h	32	TPTC_PCNT	52A4 0208h	52A6 0208h
20Ch	32	TPTC_PDST	52A4 020Ch	52A6 020Ch
210h	32	TPTC_PBIDX	52A4 0210h	52A6 0210h
214h	32	TPTC_PMPPRXY	52A4 0214h	52A6 0214h
240h	32	TPTC_SAOPT	52A4 0240h	52A6 0240h
244h	32	TPTC_SASRC	52A4 0244h	52A6 0244h
248h	32	TPTC_SACNT	52A4 0248h	52A6 0248h
24Ch	32	TPTC_SADST	52A4 024Ch	52A6 024Ch
250h	32	TPTC_SABIDX	52A4 0250h	52A6 0250h
254h	32	TPTC_SAMPPRXY	52A4 0254h	52A6 0254h
258h	32	TPTC_SACNTRLD	52A4 0258h	52A6 0258h
25Ch	32	TPTC_SASRCBREF	52A4 025Ch	52A6 025Ch
260h	32	TPTC_SADSTBREF	52A4 0260h	52A6 0260h
264h	32	TPTC_SABCNT	52A4 0264h	52A6 0264h
280h	32	TPTC_DFCNTRLD	52A4 0280h	52A6 0280h
284h	32	TPTC_DFSRCBREF	52A4 0284h	52A6 0284h
300h	32	TPTC_DFOPT0	52A4 0300h	52A6 0300h
304h	32	TPTC_DFSRC0	52A4 0304h	52A6 0304h
308h	32	TPTC_DFACNT0	52A4 0308h	52A6 0308h
30Ch	32	TPTC_DFDST0	52A4 030Ch	52A6 030Ch
310h	32	TPTC_DFBIDX0	52A4 0310h	52A6 0310h
314h	32	TPTC_DFMPPRXY0	52A4 0314h	52A6 0314h
318h	32	TPTC_DFBCNT0	52A4 0318h	52A6 0318h
340h	32	TPTC_DFOPT1	52A4 0340h	52A6 0340h
344h	32	TPTC_DFSRC1	52A4 0344h	52A6 0344h
348h	32	TPTC_DFACNT1	52A4 0348h	52A6 0348h
34Ch	32	TPTC_DFDST1	52A4 034Ch	52A6 034Ch
350h	32	TPTC_DFBIDX1	52A4 0350h	52A6 0350h
354h	32	TPTC_DFMPPRXY1	52A4 0354h	52A6 0354h
358h	32	TPTC_DFBCNT1	52A4 0358h	52A6 0358h

4.4.2 EDMA Registers

EDMA Registers

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4.4.2.1 TPCC_PID Register

4.4.2.1.1 TPCC_PID Register (Offset = 0h) [reset = 4001AB00h]

Peripheral ID Register

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Table 4-2036. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0000h

Figure 4-994. TPCC_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RES1		FUNC			
R		R		R			
1h		0h		1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
15h					3h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 4-2037. TPCC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1.
29:28	RES1	R	0h	RESERVE FIELD
27:16	FUNC	R	1h	Function indicates a software compatible module family.
15:11	RTL	R	15h	RTL Version
10:8	MAJOR	R	3h	Major Revision
7:6	CUSTOM	R	0h	Custom revision field: Not used on this version of EDMA.
5:0	MINOR	R	0h	Minor Revision

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4.4.2.2 TPCC_CCCFG Register

4.4.2.2.1 TPCC_CCCFG Register (Offset = 4h) [reset = 3314445h]

CC Configuration Register

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Table 4-2038. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0004h

Figure 4-995. TPCC_CCCFG Name Register

31	30	29	28	27	26	25	24
RES2						MPEXIST	CHMAPEXIST
R						R	R
0h						1h	1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES3		NUMREGN		RES4	NUMTC		
R		R		R	R		
0h		3h		0h	1h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES5	NUMPAENTRY			RES6	NUMINTCH		
R	R			R	R		
0h	4h			0h	4h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES7	NUMQDMACH			RES8	NUMDMACH		
R	R			R	R		
0h	4h			0h	5h		

Table 4-2039. TPCC_CCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RES2	R	0h	RESERVE FIELD
25	MPEXIST	R	1h	Memory Protection Existence MPEXIST = 0 : No memory protection. MPEXIST = 1 : Memory Protection logic included.
24	CHMAPEXIST	R	1h	Channel Mapping Existence CHMAPEXIST = 0 : No Channel mapping. CHMAPEXIST = 1 : Channel mapping logic included.
23:22	RES3	R	0h	RESERVE FIELD
21:20	NUMREGN	R	3h	Number of MP and Shadow regions
19	RES4	R	0h	RESERVE FIELD
18:16	NUMTC	R	1h	Number of Queues/Number of TCs
15	RES5	R	0h	RESERVE FIELD
14:12	NUMPAENTRY	R	4h	Number of PaRAM entries
11	RES6	R	0h	RESERVE FIELD
10:8	NUMINTCH	R	4h	Number of Interrupt Channels
7	RES7	R	0h	RESERVE FIELD
6:4	NUMQDMACH	R	4h	Number of QDMA Channels
3	RES8	R	0h	RESERVE FIELD
2:0	NUMDMACH	R	5h	Number of DMA Channels

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4.4.2.3 TPCC_DCHMAPN Register

4.4.2.3.1 TPCC_DCHMAPN Register (Offset = 100h) [reset = 0h]

DMA Channel N mapping to PaRAM.

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Table 4-2040. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0100h

Figure 4-996. TPCC_DCHMAPN Name Register

31	30	29	28	27	26	25	24
RES10							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES10							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES10		PAENTRY					
R		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PAENTRY			RES100				
R/W			R				
0h			0h				

Table 4-2041. TPCC_DCHMAPN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RES10	R	0h	RESERVE FIELD
13:5	PAENTRY	R/W	0h	PAENTRY points to the PaRAM Entry number for DMA Channel N
4:0	RES100	R	0h	RESERVE FIELD

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4.4.2.4 TPCC_QCHMAPN Register

4.4.2.4.1 TPCC_QCHMAPN Register (Offset = 200h) [reset = 0h]

QDMA Channel N Mapping Register

Return to Summary Table

Table 4-2042. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0200h

Figure 4-997. TPCC_QCHMAPN Name Register

31	30	29	28	27	26	25	24
RES10							
R							
0h							
23	22	21	20	19	18	17	16
RES10							
R							
0h							
15	14	13	12	11	10	9	8
RES10		PAENTRY					
R		R/W					
0h		0h					
7	6	5	4	3	2	1	0
PAENTRY			TRWORD			RESERVED	
R/W			R/W			NONE	
0h			0h			0h	

Table 4-2043. TPCC_QCHMAPN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RES10	R	0h	RESERVE FIELD
13:5	PAENTRY	R/W	0h	PaRAM Entry number for QDMA Channel N.
4:2	TRWORD	R/W	0h	TRWORD points to the specific trigger word of the PaRAM Entry defined by PAENTRY. A write to the trigger word results in a QDMA Event being recognized.
1:0	RESERVED	NONE	0h	Reserved

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4.4.2.5 TPCC_DMAQNUMN Register

4.4.2.5.1 TPCC_DMAQNUMN Register (Offset = 240h) [reset = 0h]

DMA Queue Number Register n Contains the Event queue number to be used for the corresponding DMA Channel.

Return to Summary Table

Table 4-2044. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0240h

Figure 4-998. TPCC_DMAQNUMN Name Register

31	30	29	28	27	26	25	24
RES11	E7			RES12	E6		
R	R/W			R	R/W		
0h	0h			0h	0h		
23	22	21	20	19	18	17	16
RES13	E5			RES14	E4		
R	R/W			R	R/W		
0h	0h			0h	0h		
15	14	13	12	11	10	9	8
RES15	E3			RES16	E2		
R	R/W			R	R/W		
0h	0h			0h	0h		
7	6	5	4	3	2	1	0
RES17	E1			RES18	E0		
R	R/W			R	R/W		
0h	0h			0h	0h		

Table 4-2045. TPCC_DMAQNUMN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES11	R	0h	RESERVE FIELD
30:28	E7	R/W	0h	DMA Queue Number for event #7
27	RES12	R	0h	RESERVE FIELD
26:24	E6	R/W	0h	DMA Queue Number for event #6
23	RES13	R	0h	RESERVE FIELD
22:20	E5	R/W	0h	DMA Queue Number for event #5
19	RES14	R	0h	RESERVE FIELD
18:16	E4	R/W	0h	DMA Queue Number for event #4
15	RES15	R	0h	RESERVE FIELD
14:12	E3	R/W	0h	DMA Queue Number for event #3
11	RES16	R	0h	RESERVE FIELD
10:8	E2	R/W	0h	DMA Queue Number for event #2
7	RES17	R	0h	RESERVE FIELD
6:4	E1	R/W	0h	DMA Queue Number for event #1
3	RES18	R	0h	RESERVE FIELD
2:0	E0	R/W	0h	DMA Queue Number for event #0

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4.4.2.6 TPCC_QDMAQNUM Register

4.4.2.6.1 TPCC_QDMAQNUM Register (Offset = 260h) [reset = 0h]

QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.

Return to Summary Table

Table 4-2046. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0260h

Figure 4-999. TPCC_QDMAQNUM Name Register

31	30	29	28	27	26	25	24
RES19	E7			RES20	E6		
R	R/W			R	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES21	E5			RES22	E4		
R	R/W			R	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES23	E3			RES24	E2		
R	R/W			R	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES25	E1			RES26	E0		
R	R/W			R	R/W		
0h	0h			0h	0h		

Table 4-2047. TPCC_QDMAQNUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES19	R	0h	RESERVE FIELD
30:28	E7	R/W	0h	QDMA Queue Number for event #7
27	RES20	R	0h	RESERVE FIELD
26:24	E6	R/W	0h	QDMA Queue Number for event #6
23	RES21	R	0h	RESERVE FIELD
22:20	E5	R/W	0h	QDMA Queue Number for event #5
19	RES22	R	0h	RESERVE FIELD
18:16	E4	R/W	0h	QDMA Queue Number for event #4
15	RES23	R	0h	RESERVE FIELD
14:12	E3	R/W	0h	QDMA Queue Number for event #3
11	RES24	R	0h	RESERVE FIELD
10:8	E2	R/W	0h	QDMA Queue Number for event #2
7	RES25	R	0h	RESERVE FIELD
6:4	E1	R/W	0h	QDMA Queue Number for event #1
3	RES26	R	0h	RESERVE FIELD
2:0	E0	R/W	0h	QDMA Queue Number for event #0

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4.4.2.7 TPCC_QUETCMAP Register

4.4.2.7.1 TPCC_QUETCMAP Register (Offset = 280h) [reset = 10h]

Queue to TC Mapping

Return to Summary Table

Table 4-2048. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0280h

Figure 4-1000. TPCC_QUETCMAP Name Register

31	30	29	28	27	26	25	24
RES27							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES27							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES27							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES27	TCNUMQ1			RES28	TCNUMQ0		
R	R/W			R	R/W		
0h	1h			0h	0h		

Table 4-2049. TPCC_QUETCMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RES27	R	0h	RESERVE FIELD
6:4	TCNUMQ1	R/W	1h	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to.
3	RES28	R	0h	RESERVE FIELD
2:0	TCNUMQ0	R/W	0h	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to.

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4.4.2.8 TPCC_QUEPRI Register

4.4.2.8.1 TPCC_QUEPRI Register (Offset = 284h) [reset = 0h]

Queue Priority

Return to Summary Table

Table 4-2050. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0284h

Figure 4-1001. TPCC_QUEPRI Name Register

31	30	29	28	27	26	25	24
RES29							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES29							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES29							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES29	PRIQ1			RES30	PRIQ0		
R	R/W			R	R/W		
0h	0h			0h	0h		

Table 4-2051. TPCC_QUEPRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RES29	R	0h	RESERVE FIELD
6:4	PRIQ1	R/W	0h	Priority Level for Queue 1 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands.
3	RES30	R	0h	RESERVE FIELD
2:0	PRIQ0	R/W	0h	Priority Level for Queue 0 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands.

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4.4.2.9 TPCC_EMR Register

4.4.2.9.1 TPCC_EMR Register (Offset = 300h) [reset = 0h]

Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Return to Summary Table

Table 4-2052. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0300h

Figure 4-1002. TPCC_EMR Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2053. TPCC_EMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event Missed #31
30	E30	R	0h	Event Missed #30
29	E29	R	0h	Event Missed #29
28	E28	R	0h	Event Missed #28
27	E27	R	0h	Event Missed #27
26	E26	R	0h	Event Missed #26
25	E25	R	0h	Event Missed #25
24	E24	R	0h	Event Missed #24
23	E23	R	0h	Event Missed #23
22	E22	R	0h	Event Missed #22
21	E21	R	0h	Event Missed #21
20	E20	R	0h	Event Missed #20
19	E19	R	0h	Event Missed #19
18	E18	R	0h	Event Missed #18
17	E17	R	0h	Event Missed #17
16	E16	R	0h	Event Missed #16
15	E15	R	0h	Event Missed #15

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Table 4-2053. TPCC_EMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	E14	R	0h	Event Missed #14
13	E13	R	0h	Event Missed #13
12	E12	R	0h	Event Missed #12
11	E11	R	0h	Event Missed #11
10	E10	R	0h	Event Missed #10
9	E9	R	0h	Event Missed #9
8	E8	R	0h	Event Missed #8
7	E7	R	0h	Event Missed #7
6	E6	R	0h	Event Missed #6
5	E5	R	0h	Event Missed #5
4	E4	R	0h	Event Missed #4
3	E3	R	0h	Event Missed #3
2	E2	R	0h	Event Missed #2
1	E1	R	0h	Event Missed #1
0	E0	R	0h	Event Missed #0

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4.4.2.10 TPCC_EMRH Register

4.4.2.10.1 TPCC_EMRH Register (Offset = 304h) [reset = 0h]

Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Return to Summary Table

Table 4-2054. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0304h

Figure 4-1003. TPCC_EMRH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2055. TPCC_EMRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event Missed #63
30	E62	R	0h	Event Missed #62
29	E61	R	0h	Event Missed #61
28	E60	R	0h	Event Missed #60
27	E59	R	0h	Event Missed #59
26	E58	R	0h	Event Missed #58
25	E57	R	0h	Event Missed #57
24	E56	R	0h	Event Missed #56
23	E55	R	0h	Event Missed #55
22	E54	R	0h	Event Missed #54
21	E53	R	0h	Event Missed #53
20	E52	R	0h	Event Missed #52
19	E51	R	0h	Event Missed #51
18	E50	R	0h	Event Missed #50
17	E49	R	0h	Event Missed #49
16	E48	R	0h	Event Missed #48
15	E47	R	0h	Event Missed #47

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Table 4-2055. TPCC_EMRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	E46	R	0h	Event Missed #46
13	E45	R	0h	Event Missed #45
12	E44	R	0h	Event Missed #44
11	E43	R	0h	Event Missed #43
10	E42	R	0h	Event Missed #42
9	E41	R	0h	Event Missed #41
8	E40	R	0h	Event Missed #40
7	E39	R	0h	Event Missed #39
6	E38	R	0h	Event Missed #38
5	E37	R	0h	Event Missed #37
4	E36	R	0h	Event Missed #36
3	E35	R	0h	Event Missed #35
2	E34	R	0h	Event Missed #34
1	E33	R	0h	Event Missed #33
0	E32	R	0h	Event Missed #32

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4.4.2.11 TPCC_EMCR Register

4.4.2.11.1 TPCC_EMCR Register (Offset = 308h) [reset = 0h]

Event Missed Clear Register: CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

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Table 4-2056. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0308h

Figure 4-1004. TPCC_EMCR Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2057. TPCC_EMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event Missed Clear #31
30	E30	W	0h	Event Missed Clear #30
29	E29	W	0h	Event Missed Clear #29
28	E28	W	0h	Event Missed Clear #28
27	E27	W	0h	Event Missed Clear #27
26	E26	W	0h	Event Missed Clear #26
25	E25	W	0h	Event Missed Clear #25
24	E24	W	0h	Event Missed Clear #24
23	E23	W	0h	Event Missed Clear #23
22	E22	W	0h	Event Missed Clear #22
21	E21	W	0h	Event Missed Clear #21
20	E20	W	0h	Event Missed Clear #20
19	E19	W	0h	Event Missed Clear #19
18	E18	W	0h	Event Missed Clear #18
17	E17	W	0h	Event Missed Clear #17
16	E16	W	0h	Event Missed Clear #16
15	E15	W	0h	Event Missed Clear #15
14	E14	W	0h	Event Missed Clear #14
13	E13	W	0h	Event Missed Clear #13

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Table 4-2057. TPCC_EMCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event Missed Clear #12
11	E11	W	0h	Event Missed Clear #11
10	E10	W	0h	Event Missed Clear #10
9	E9	W	0h	Event Missed Clear #9
8	E8	W	0h	Event Missed Clear #8
7	E7	W	0h	Event Missed Clear #7
6	E6	W	0h	Event Missed Clear #6
5	E5	W	0h	Event Missed Clear #5
4	E4	W	0h	Event Missed Clear #4
3	E3	W	0h	Event Missed Clear #3
2	E2	W	0h	Event Missed Clear #2
1	E1	W	0h	Event Missed Clear #1
0	E0	W	0h	Event Missed Clear #0

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4.4.2.12 TPCC_EMCRH Register

4.4.2.12.1 TPCC_EMCRH Register (Offset = 30Ch) [reset = 0h]

Event Missed Clear Register (High Part): CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

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Table 4-2058. Instance Table

Instance Name	Physical Address
EDMA0	52A0 030Ch

Figure 4-1005. TPCC_EMCRH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2059. TPCC_EMCRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event Missed Clear #63
30	E62	W	0h	Event Missed Clear #62
29	E61	W	0h	Event Missed Clear #61
28	E60	W	0h	Event Missed Clear #60
27	E59	W	0h	Event Missed Clear #59
26	E58	W	0h	Event Missed Clear #58
25	E57	W	0h	Event Missed Clear #57
24	E56	W	0h	Event Missed Clear #56
23	E55	W	0h	Event Missed Clear #55
22	E54	W	0h	Event Missed Clear #54
21	E53	W	0h	Event Missed Clear #53
20	E52	W	0h	Event Missed Clear #52
19	E51	W	0h	Event Missed Clear #51
18	E50	W	0h	Event Missed Clear #50
17	E49	W	0h	Event Missed Clear #49
16	E48	W	0h	Event Missed Clear #48
15	E47	W	0h	Event Missed Clear #47
14	E46	W	0h	Event Missed Clear #46

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Table 4-2059. TPCC_EMCRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	E45	W	0h	Event Missed Clear #45
12	E44	W	0h	Event Missed Clear #44
11	E43	W	0h	Event Missed Clear #43
10	E42	W	0h	Event Missed Clear #42
9	E41	W	0h	Event Missed Clear #41
8	E40	W	0h	Event Missed Clear #40
7	E39	W	0h	Event Missed Clear #39
6	E38	W	0h	Event Missed Clear #38
5	E37	W	0h	Event Missed Clear #37
4	E36	W	0h	Event Missed Clear #36
3	E35	W	0h	Event Missed Clear #35
2	E34	W	0h	Event Missed Clear #34
1	E33	W	0h	Event Missed Clear #33
0	E32	W	0h	Event Missed Clear #32

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4.4.2.13 TPCC_QEMR Register

4.4.2.13.1 TPCC_QEMR Register (Offset = 310h) [reset = 0h]

QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced.. If any bit in the QEMR register is set (and all errors (including EMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

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Table 4-2060. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0310h

Figure 4-1006. TPCC_QEMR Name Register

31	30	29	28	27	26	25	24
RES31							
R							
0h							
23	22	21	20	19	18	17	16
RES31							
R							
0h							
15	14	13	12	11	10	9	8
RES31							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2061. TPCC_QEMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES31	R	0h	RESERVE FIELD
7	E7	R	0h	Event Missed #7
6	E6	R	0h	Event Missed #6
5	E5	R	0h	Event Missed #5
4	E4	R	0h	Event Missed #4
3	E3	R	0h	Event Missed #3
2	E2	R	0h	Event Missed #2
1	E1	R	0h	Event Missed #1
0	E0	R	0h	Event Missed #0

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4.4.2.14 TPCC_QEMCR Register

4.4.2.14.1 TPCC_QEMCR Register (Offset = 314h) [reset = 0h]

QDMA Event Missed Clear Register: CPU write of '1' to the QEMCR.En bit causes the QEMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

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Table 4-2062. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0314h

Figure 4-1007. TPCC_QEMCR Name Register

31	30	29	28	27	26	25	24
RES32							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES32							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES32							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2063. TPCC_QEMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES32	R	0h	RESERVE FIELD
7	E7	W	0h	Event Missed Clear #7
6	E6	W	0h	Event Missed Clear #6
5	E5	W	0h	Event Missed Clear #5
4	E4	W	0h	Event Missed Clear #4
3	E3	W	0h	Event Missed Clear #3
2	E2	W	0h	Event Missed Clear #2
1	E1	W	0h	Event Missed Clear #1
0	E0	W	0h	Event Missed Clear #0

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4.4.2.15 TPCC_CCERR Register

4.4.2.15.1 TPCC_CCERR Register (Offset = 318h) [reset = 0h]

CC Error Register

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Table 4-2064. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0318h

Figure 4-1008. TPCC_CCERR Name Register

31	30	29	28	27	26	25	24
RES33							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES33							TCERR
R							R
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES34							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QTHRXCD7	QTHRXCD6	QTHRXCD5	QTHRXCD4	QTHRXCD3	QTHRXCD2	QTHRXCD1	QTHRXCD0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2065. TPCC_CCERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RES33	R	0h	RESERVE FIELD
16	TCERR	R	0h	Transfer Completion Code Error: TCCERR = 0 : Total number of allowed TCCs outstanding has not been reached. TCCERR = 1 : Total number of allowed TCCs has been reached. TCCERR can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors were previously clear] then an error will be signaled with TPCC error interrupt.
15:8	RES34	R	0h	RESERVE FIELD
7	QTHRXCD7	R	0h	Queue Threshold Error for Q7: QTHRXCD7 = 0 : Watermark/threshold has not been exceeded. QTHRXCD7 = 1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD7 can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt.
6	QTHRXCD6	R	0h	Queue Threshold Error for Q6: QTHRXCD6 = 0 : Watermark/threshold has not been exceeded. QTHRXCD6 = 1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD6 can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt.

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Table 4-2065. TPCC_CCERR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	QTHRXCD5	R	0h	Queue Threshold Error for Q5: QTHRXCD5 = 0 : Watermark/threshold has not been exceeded. QTHRXCD5 = 1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD5 can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt.
4	QTHRXCD4	R	0h	Queue Threshold Error for Q4: QTHRXCD4 = 0 : Watermark/threshold has not been exceeded. QTHRXCD4 = 1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD4 can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt.
3	QTHRXCD3	R	0h	Queue Threshold Error for Q3: QTHRXCD3 = 0 : Watermark/threshold has not been exceeded. QTHRXCD3 = 1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD3 can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt.
2	QTHRXCD2	R	0h	Queue Threshold Error for Q2: QTHRXCD2 = 0 : Watermark/threshold has not been exceeded. QTHRXCD2 = 1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD2 can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt.
1	QTHRXCD1	R	0h	Queue Threshold Error for Q1: QTHRXCD1 = 0 : Watermark/threshold has not been exceeded. QTHRXCD1 = 1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD1 can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt.
0	QTHRXCD0	R	0h	Queue Threshold Error for Q0: QTHRXCD0 = 0 : Watermark/threshold has not been exceeded. QTHRXCD0 = 1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD0 can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt.

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4.4.2.16 TPCC_CCERRCLR Register

4.4.2.16.1 TPCC_CCERRCLR Register (Offset = 31Ch) [reset = 0h]

CC Error Clear Register

Return to Summary Table

Table 4-2066. Instance Table

Instance Name	Physical Address
EDMA0	52A0 031Ch

Figure 4-1009. TPCC_CCERRCLR Name Register

31	30	29	28	27	26	25	24
RES35							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES35							TCERR
R							W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES36							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
QTHRXCD7	QTHRXCD6	QTHRXCD5	QTHRXCD4	QTHRXCD3	QTHRXCD2	QTHRXCD1	QTHRXCD0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2067. TPCC_CCERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RES35	R	0h	RESERVE FIELD
16	TCERR	W	0h	Clear Error for CCERR.TCERR: Write of '1' clears the value of CCERR bit N. Writes of '0' have no affect.
15:8	RES36	R	0h	RESERVE FIELD
7	QTHRXCD7	W	0h	Clear error for CCERR.QTHRXCD7: Write of '1' clears the values of QSTAT7.WM QSTAT7.THRXCD CCERR.QTHRXCD7 Writes of '0' have no affect.
6	QTHRXCD6	W	0h	Clear error for CCERR.QTHRXCD6: Write of '1' clears the values of QSTAT6.WM QSTAT6.THRXCD CCERR.QTHRXCD6 Writes of '0' have no affect.
5	QTHRXCD5	W	0h	Clear error for CCERR.QTHRXCD5: Write of '1' clears the values of QSTAT5.WM QSTAT5.THRXCD CCERR.QTHRXCD5 Writes of '0' have no affect.
4	QTHRXCD4	W	0h	Clear error for CCERR.QTHRXCD4: Write of '1' clears the values of QSTAT4.WM QSTAT4.THRXCD CCERR.QTHRXCD4 Writes of '0' have no affect.
3	QTHRXCD3	W	0h	Clear error for CCERR.QTHRXCD3: Write of '1' clears the values of QSTAT3.WM QSTAT3.THRXCD CCERR.QTHRXCD3 Writes of '0' have no affect.
2	QTHRXCD2	W	0h	Clear error for CCERR.QTHRXCD2: Write of '1' clears the values of QSTAT2.WM QSTAT2.THRXCD CCERR.QTHRXCD2 Writes of '0' have no affect.

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Table 4-2067. TPCC_CCERRCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	QTHRXCD1	W	0h	Clear error for CCERR.QTHRXCD1: Write of '1' clears the values of QSTAT1.WM QSTAT1.THRXCD CCERR.QTHRXCD1 Writes of '0' have no affect.
0	QTHRXCD0	W	0h	Clear error for CCERR.QTHRXCD0: Write of '1' clears the values of QSTAT0.WM QSTAT0.THRXCD CCERR.QTHRXCD0 Writes of '0' have no affect.

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4.4.2.17 TPCC_EEVAL Register

4.4.2.17.1 TPCC_EEVAL Register (Offset = 320h) [reset = 0h]

Error Eval Register

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Table 4-2068. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0320h

Figure 4-1010. TPCC_EEVAL Name Register

31	30	29	28	27	26	25	24
RES37							
R							
0h							
23	22	21	20	19	18	17	16
RES37							
R							
0h							
15	14	13	12	11	10	9	8
RES37							
R							
0h							
7	6	5	4	3	2	1	0
RES37						SET	EVAL
R						W	W
0h						0h	0h

Table 4-2069. TPCC_EEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES37	R	0h	RESERVE FIELD
1	SET	W	0h	Error Interrupt Set: CPU write of '1' to the SET bit causes the TPCC error interrupt to be pulsed regardless of state of EMR/EMRH QEMR or CCERR. CPU write of '0' has no effect.
0	EVAL	W	0h	Error Interrupt Evaluate: CPU write of '1' to the EVAL bit causes the TPCC error interrupt to be pulsed if any errors have not been cleared in the EMR/EMRH QEMR or CCERR registers. CPU write of '0' has no effect.

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4.4.2.18 TPCC_DRAEM Register

4.4.2.18.1 TPCC_DRAEM Register (Offset = 340h) [reset = 0h]

DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

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Table 4-2070. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0340h

Figure 4-1011. TPCC_DRAEM Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2071. TPCC_DRAEM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R/W	0h	DMA Region Access enable for Region M bit #31
30	E30	R/W	0h	DMA Region Access enable for Region M bit #30
29	E29	R/W	0h	DMA Region Access enable for Region M bit #29
28	E28	R/W	0h	DMA Region Access enable for Region M bit #28
27	E27	R/W	0h	DMA Region Access enable for Region M bit #27
26	E26	R/W	0h	DMA Region Access enable for Region M bit #26
25	E25	R/W	0h	DMA Region Access enable for Region M bit #25
24	E24	R/W	0h	DMA Region Access enable for Region M bit #24
23	E23	R/W	0h	DMA Region Access enable for Region M bit #23
22	E22	R/W	0h	DMA Region Access enable for Region M bit #22
21	E21	R/W	0h	DMA Region Access enable for Region M bit #21
20	E20	R/W	0h	DMA Region Access enable for Region M bit #20
19	E19	R/W	0h	DMA Region Access enable for Region M bit #19
18	E18	R/W	0h	DMA Region Access enable for Region M bit #18
17	E17	R/W	0h	DMA Region Access enable for Region M bit #17

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Table 4-2071. TPCC_DRAEM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	E16	R/W	0h	DMA Region Access enable for Region M bit #16
15	E15	R/W	0h	DMA Region Access enable for Region M bit #15
14	E14	R/W	0h	DMA Region Access enable for Region M bit #14
13	E13	R/W	0h	DMA Region Access enable for Region M bit #13
12	E12	R/W	0h	DMA Region Access enable for Region M bit #12
11	E11	R/W	0h	DMA Region Access enable for Region M bit #11
10	E10	R/W	0h	DMA Region Access enable for Region M bit #10
9	E9	R/W	0h	DMA Region Access enable for Region M bit #9
8	E8	R/W	0h	DMA Region Access enable for Region M bit #8
7	E7	R/W	0h	DMA Region Access enable for Region M bit #7
6	E6	R/W	0h	DMA Region Access enable for Region M bit #6
5	E5	R/W	0h	DMA Region Access enable for Region M bit #5
4	E4	R/W	0h	DMA Region Access enable for Region M bit #4
3	E3	R/W	0h	DMA Region Access enable for Region M bit #3
2	E2	R/W	0h	DMA Region Access enable for Region M bit #2
1	E1	R/W	0h	DMA Region Access enable for Region M bit #1
0	E0	R/W	0h	DMA Region Access enable for Region M bit #0

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4.4.2.19 TPCC_DRAEHM Register

4.4.2.19.1 TPCC_DRAEHM Register (Offset = 344h) [reset = 0h]

DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

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Table 4-2072. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0344h

Figure 4-1012. TPCC_DRAEHM Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2073. TPCC_DRAEHM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R/W	0h	DMA Region Access enable for Region M bit #63
30	E62	R/W	0h	DMA Region Access enable for Region M bit #62
29	E61	R/W	0h	DMA Region Access enable for Region M bit #61
28	E60	R/W	0h	DMA Region Access enable for Region M bit #60
27	E59	R/W	0h	DMA Region Access enable for Region M bit #59
26	E58	R/W	0h	DMA Region Access enable for Region M bit #58
25	E57	R/W	0h	DMA Region Access enable for Region M bit #57
24	E56	R/W	0h	DMA Region Access enable for Region M bit #56
23	E55	R/W	0h	DMA Region Access enable for Region M bit #55
22	E54	R/W	0h	DMA Region Access enable for Region M bit #54
21	E53	R/W	0h	DMA Region Access enable for Region M bit #53

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Table 4-2073. TPCC_DRAEHM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	E52	R/W	0h	DMA Region Access enable for Region M bit #52
19	E51	R/W	0h	DMA Region Access enable for Region M bit #51
18	E50	R/W	0h	DMA Region Access enable for Region M bit #50
17	E49	R/W	0h	DMA Region Access enable for Region M bit #49
16	E48	R/W	0h	DMA Region Access enable for Region M bit #48
15	E47	R/W	0h	DMA Region Access enable for Region M bit #47
14	E46	R/W	0h	DMA Region Access enable for Region M bit #46
13	E45	R/W	0h	DMA Region Access enable for Region M bit #45
12	E44	R/W	0h	DMA Region Access enable for Region M bit #44
11	E43	R/W	0h	DMA Region Access enable for Region M bit #43
10	E42	R/W	0h	DMA Region Access enable for Region M bit #42
9	E41	R/W	0h	DMA Region Access enable for Region M bit #41
8	E40	R/W	0h	DMA Region Access enable for Region M bit #40
7	E39	R/W	0h	DMA Region Access enable for Region M bit #39
6	E38	R/W	0h	DMA Region Access enable for Region M bit #38
5	E37	R/W	0h	DMA Region Access enable for Region M bit #37
4	E36	R/W	0h	DMA Region Access enable for Region M bit #36
3	E35	R/W	0h	DMA Region Access enable for Region M bit #35
2	E34	R/W	0h	DMA Region Access enable for Region M bit #34
1	E33	R/W	0h	DMA Region Access enable for Region M bit #33
0	E32	R/W	0h	DMA Region Access enable for Region M bit #32

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4.4.2.20 TPCC_QRAEN Register

4.4.2.20.1 TPCC_QRAEN Register (Offset = 380h) [reset = 0h]

QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region n interrupt.

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Table 4-2074. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0380h

Figure 4-1013. TPCC_QRAEN Name Register

31	30	29	28	27	26	25	24
RES38							
R							
0h							
23	22	21	20	19	18	17	16
RES38							
R							
0h							
15	14	13	12	11	10	9	8
RES38							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2075. TPCC_QRAEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES38	R	0h	RESERVE FIELD
7	E7	R/W	0h	QDMA Region Access enable for Region M bit #7
6	E6	R/W	0h	QDMA Region Access enable for Region M bit #6
5	E5	R/W	0h	QDMA Region Access enable for Region M bit #5
4	E4	R/W	0h	QDMA Region Access enable for Region M bit #4
3	E3	R/W	0h	QDMA Region Access enable for Region M bit #3
2	E2	R/W	0h	QDMA Region Access enable for Region M bit #2
1	E1	R/W	0h	QDMA Region Access enable for Region M bit #1
0	E0	R/W	0h	QDMA Region Access enable for Region M bit #0

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4.4.2.21 TPCC_QNE0 Register

4.4.2.21.1 TPCC_QNE0 Register (Offset = 400h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 0

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Table 4-2076. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0400h

Figure 4-1014. TPCC_QNE0 Name Register

31	30	29	28	27	26	25	24
RES39							
R							
0h							
23	22	21	20	19	18	17	16
RES39							
R							
0h							
15	14	13	12	11	10	9	8
RES39							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2077. TPCC_QNE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES39	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.22 TPCC_QNE1 Register

4.4.2.22.1 TPCC_QNE1 Register (Offset = 404h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 1

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Table 4-2078. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0404h

Figure 4-1015. TPCC_QNE1 Name Register

31	30	29	28	27	26	25	24
RES40							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES40							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES40							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2079. TPCC_QNE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES40	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.23 TPCC_QNE2 Register

4.4.2.23.1 TPCC_QNE2 Register (Offset = 408h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 2

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Table 4-2080. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0408h

Figure 4-1016. TPCC_QNE2 Name Register

31	30	29	28	27	26	25	24
RES41							
R							
0h							
23	22	21	20	19	18	17	16
RES41							
R							
0h							
15	14	13	12	11	10	9	8
RES41							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2081. TPCC_QNE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES41	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.24 TPCC_QNE3 Register

4.4.2.24.1 TPCC_QNE3 Register (Offset = 40Ch) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 3

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Table 4-2082. Instance Table

Instance Name	Physical Address
EDMA0	52A0 040Ch

Figure 4-1017. TPCC_QNE3 Name Register

31	30	29	28	27	26	25	24
RES42							
R							
0h							
23	22	21	20	19	18	17	16
RES42							
R							
0h							
15	14	13	12	11	10	9	8
RES42							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2083. TPCC_QNE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES42	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.25 TPCC_QNE4 Register

4.4.2.25.1 TPCC_QNE4 Register (Offset = 410h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 4

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Table 4-2084. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0410h

Figure 4-1018. TPCC_QNE4 Name Register

31	30	29	28	27	26	25	24
RES43							
R							
0h							
23	22	21	20	19	18	17	16
RES43							
R							
0h							
15	14	13	12	11	10	9	8
RES43							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2085. TPCC_QNE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES43	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.26 TPCC_QNE5 Register

4.4.2.26.1 TPCC_QNE5 Register (Offset = 414h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 5

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Table 4-2086. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0414h

Figure 4-1019. TPCC_QNE5 Name Register

31	30	29	28	27	26	25	24
RES44							
R							
0h							
23	22	21	20	19	18	17	16
RES44							
R							
0h							
15	14	13	12	11	10	9	8
RES44							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2087. TPCC_QNE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES44	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.27 TPCC_QNE6 Register

4.4.2.27.1 TPCC_QNE6 Register (Offset = 418h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 6

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Table 4-2088. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0418h

Figure 4-1020. TPCC_QNE6 Name Register

31	30	29	28	27	26	25	24
RES45							
R							
0h							
23	22	21	20	19	18	17	16
RES45							
R							
0h							
15	14	13	12	11	10	9	8
RES45							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2089. TPCC_QNE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES45	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.28 TPCC_QNE7 Register

4.4.2.28.1 TPCC_QNE7 Register (Offset = 41Ch) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 7

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Table 4-2090. Instance Table

Instance Name	Physical Address
EDMA0	52A0 041Ch

Figure 4-1021. TPCC_QNE7 Name Register

31	30	29	28	27	26	25	24
RES46							
R							
0h							
23	22	21	20	19	18	17	16
RES46							
R							
0h							
15	14	13	12	11	10	9	8
RES46							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2091. TPCC_QNE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES46	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.29 TPCC_QNE8 Register

4.4.2.29.1 TPCC_QNE8 Register (Offset = 420h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 8

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Table 4-2092. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0420h

Figure 4-1022. TPCC_QNE8 Name Register

31	30	29	28	27	26	25	24
RES47							
R							
0h							
23	22	21	20	19	18	17	16
RES47							
R							
0h							
15	14	13	12	11	10	9	8
RES47							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2093. TPCC_QNE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES47	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.30 TPCC_QNE9 Register

4.4.2.30.1 TPCC_QNE9 Register (Offset = 424h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 9

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Table 4-2094. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0424h

Figure 4-1023. TPCC_QNE9 Name Register

31	30	29	28	27	26	25	24
RES48							
R							
0h							
23	22	21	20	19	18	17	16
RES48							
R							
0h							
15	14	13	12	11	10	9	8
RES48							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2095. TPCC_QNE9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES48	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.31 TPCC_QNE10 Register

4.4.2.31.1 TPCC_QNE10 Register (Offset = 428h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 0

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Table 4-2096. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0428h

Figure 4-1024. TPCC_QNE10 Name Register

31	30	29	28	27	26	25	24
RES49							
R							
0h							
23	22	21	20	19	18	17	16
RES49							
R							
0h							
15	14	13	12	11	10	9	8
RES49							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2097. TPCC_QNE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES49	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.32 TPCC_QNE11 Register

4.4.2.32.1 TPCC_QNE11 Register (Offset = 42Ch) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 11

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Table 4-2098. Instance Table

Instance Name	Physical Address
EDMA0	52A0 042Ch

Figure 4-1025. TPCC_QNE11 Name Register

31	30	29	28	27	26	25	24
RES50							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES50							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES50							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2099. TPCC_QNE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES50	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.33 TPCC_QNE12 Register

4.4.2.33.1 TPCC_QNE12 Register (Offset = 430h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 12

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Table 4-2100. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0430h

Figure 4-1026. TPCC_QNE12 Name Register

31	30	29	28	27	26	25	24
RES51							
R							
0h							
23	22	21	20	19	18	17	16
RES51							
R							
0h							
15	14	13	12	11	10	9	8
RES51							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2101. TPCC_QNE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES51	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.34 TPCC_QNE13 Register

4.4.2.34.1 TPCC_QNE13 Register (Offset = 434h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 13

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Table 4-2102. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0434h

Figure 4-1027. TPCC_QNE13 Name Register

31	30	29	28	27	26	25	24
RES52							
R							
0h							
23	22	21	20	19	18	17	16
RES52							
R							
0h							
15	14	13	12	11	10	9	8
RES52							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2103. TPCC_QNE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES52	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.35 TPCC_QNE14 Register

4.4.2.35.1 TPCC_QNE14 Register (Offset = 438h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 14

Return to Summary Table

Table 4-2104. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0438h

Figure 4-1028. TPCC_QNE14 Name Register

31	30	29	28	27	26	25	24
RES53							
R							
0h							
23	22	21	20	19	18	17	16
RES53							
R							
0h							
15	14	13	12	11	10	9	8
RES53							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2105. TPCC_QNE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES53	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.36 TPCC_QNE15 Register

4.4.2.36.1 TPCC_QNE15 Register (Offset = 43Ch) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 15

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Table 4-2106. Instance Table

Instance Name	Physical Address
EDMA0	52A0 043Ch

Figure 4-1029. TPCC_QNE15 Name Register

31	30	29	28	27	26	25	24
RES54							
R							
0h							
23	22	21	20	19	18	17	16
RES54							
R							
0h							
15	14	13	12	11	10	9	8
RES54							
R							
0h							
7	6	5	4	3	2	1	0
ETYPE		ENUM					
R		R					
0h		0h					

Table 4-2107. TPCC_QNE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES54	R	0h	RESERVE FIELD
7:6	ETYPE	R	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5:0	ENUM	R	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7].

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4.4.2.37 TPCC_QSTATN Register

4.4.2.37.1 TPCC_QSTATN Register (Offset = 600h) [reset = 0h]

QSTATn Register Set

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Table 4-2108. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0600h

Figure 4-1030. TPCC_QSTATN Name Register

31	30	29	28	27	26	25	24
RES55							THRXCD
R							R
0h							0h
23	22	21	20	19	18	17	16
RES56			WM				
R			R				
0h			0h				
15	14	13	12	11	10	9	8
RES57			NUMVAL				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
RES58				STRTPTR			
R				R			
0h				0h			

Table 4-2109. TPCC_QSTATN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RES55	R	0h	RESERVE FIELD
24	THRXCD	R	0h	Threshold Exceeded: THRXCD = 0 : Threshold specified by QWMTHR[A B].Qn has not been exceeded. THRXCD = 1 : Threshold specified by QWMTHR[A B].Qn has been exceeded. QSTATn.THRXCD is cleared via CCERR.WMCLRn bit.
23:21	RES56	R	0h	RESERVE FIELD
20:16	WM	R	0h	Watermark for Maximum Queue Usage: Watermark tracks the most entries that have been in QueueN since reset or since the last time that the watermark [WM] was cleared. QSTATn.WM is cleared via CCERR.WMCLRn bit. Legal values = 0x0 [empty] to 0x10 [full]
15:13	RES57	R	0h	RESERVE FIELD
12:8	NUMVAL	R	0h	Number of Valid Entries in QueueN: Represents the total number of entries residing in the Queue Manager FIFO at a given instant. Always enabled. Legal values = 0x0 [empty] to 0x10 [full]
7:4	RES58	R	0h	RESERVE FIELD
3:0	STRTPTR	R	0h	Start Pointer: Represents the offset to the head entry of QueueN in units of entries. Always enabled. Legal values = 0x0 [0th entry] to 0xF [15th entry]

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4.4.2.38 TPCC_QWMTHRA Register

4.4.2.38.1 TPCC_QWMTHRA Register (Offset = 620h) [reset = 1010h]

Queue Threshold A for Q[3:0]: CCERR.QTHRXCDn and QSTATn.THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via QSTATn.NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.

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Table 4-2110. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0620h

Figure 4-1031. TPCC_QWMTHRA Name Register

31	30	29	28	27	26	25	24
RES59							
R							
0h							
23	22	21	20	19	18	17	16
RES59							
R							
0h							
15	14	13	12	11	10	9	8
RES59			Q1				
R			R/W				
0h			10h				
7	6	5	4	3	2	1	0
RES60			Q0				
R			R/W				
0h			10h				

Table 4-2111. TPCC_QWMTHRA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RES59	R	0h	RESERVE FIELD
12:8	Q1	R/W	10h	Queue Threshold for Q1 value
7:5	RES60	R	0h	RESERVE FIELD
4:0	Q0	R/W	10h	Queue Threshold for Q0 value

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4.4.2.39 TPCC_CCSTAT Register

4.4.2.39.1 TPCC_CCSTAT Register (Offset = 640h) [reset = 0h]

CC Status Register

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Table 4-2112. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0640h

Figure 4-1032. TPCC_CCSTAT Name Register

31	30	29	28	27	26	25	24
RES61							
R							
0h							
23	22	21	20	19	18	17	16
QUEACTV7	QUEACTV6	QUEACTV5	QUEACTV4	QUEACTV3	QUEACTV2	QUEACTV1	QUEACTV0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RES62		COMPACTV					
R		R					
0h		0h					
7	6	5	4	3	2	1	0
RES63			ACTV	RES64	TRACTV	QEVTACTV	EVTACTV
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h

Table 4-2113. TPCC_CCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RES61	R	0h	RESERVE FIELD
23	QUEACTV7	R	0h	Queue 7 Active QUEACTV7 = 0 : No Evts are queued in Q7. QUEACTV7 = 1 : At least one TR is queued in Q7.
22	QUEACTV6	R	0h	Queue 6 Active QUEACTV6 = 0 : No Evts are queued in Q6. QUEACTV6 = 1 : At least one TR is queued in Q6.
21	QUEACTV5	R	0h	Queue 5 Active QUEACTV5 = 0 : No Evts are queued in Q5. QUEACTV5 = 1 : At least one TR is queued in Q5.
20	QUEACTV4	R	0h	Queue 4 Active QUEACTV4 = 0 : No Evts are queued in Q4. QUEACTV4 = 1 : At least one TR is queued in Q4.
19	QUEACTV3	R	0h	Queue 3 Active QUEACTV3 = 0 : No Evts are queued in Q3. QUEACTV3 = 1 : At least one TR is queued in Q3.
18	QUEACTV2	R	0h	Queue 2 Active QUEACTV2 = 0 : No Evts are queued in Q2. QUEACTV2 = 1 : At least one TR is queued in Q2.
17	QUEACTV1	R	0h	Queue 1 Active QUEACTV1 = 0 : No Evts are queued in Q1. QUEACTV1 = 1 : At least one TR is queued in Q1.
16	QUEACTV0	R	0h	Queue 0 Active QUEACTV0 = 0 : No Evts are queued in Q0. QUEACTV0 = 1 : At least one TR is queued in Q0.

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Table 4-2113. TPCC_CCSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	RES62	R	0h	RESERVE FIELD
13:8	COMPACTV	R	0h	Completion Request Active: Counter that tracks the total number of completion requests submitted to the TC. The counter increments when a TR is submitted with TCINTEN or TCCHEN set to '1'. The counter decrements for every valid completion code received from any of the external TCs. The CC will not service new TRs if COMPACTV count is already at the limit. COMPACTV = 0 : No completion requests outstanding. COMPACTV = 1:Total of '1' completion request outstanding. ... COMPACTV = 63 : Total of 63 completion requests are outstanding. No additional TRs will be submitted until count is less than 63.
7:5	RES63	R	0h	RESERVE FIELD
4	ACTV	R	0h	Channel Controller Active: Channel Controller Active is a logical-OR of each of the ACTV signals. The ACTV bit must remain high through the life of a TR. ACTV = 0 : Channel is idle. ACTV = 1 : Channel is busy.
3	RES64	R	0h	RESERVE FIELD
2	TRACTV	R	0h	Transfer Request Active: TRACTV = 0 : Transfer Request processing/submission logic is inactive. TRACTV = 1 : Transfer Request processing/submission logic is active.
1	QEVTACTV	R	0h	QDMA Event Active: QEVTACTV = 0 : No enabled QDMA Events are active within the CC. QEVTACTV = 1 : At least one enabled DMA Event [ER & EER ESR CER] is active within the CC.
0	EVTACTV	R	0h	DMA Event Active: EVTACTV = 0 : No enabled DMA Events are active within the CC. EVTACTV = 1 : At least one enabled DMA Event [ER & EER ESR CER] is active within the CC.

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4.4.2.40 TPCC_AETCTL Register

4.4.2.40.1 TPCC_AETCTL Register (Offset = 700h) [reset = 0h]

Advanced Event Trigger Control

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Table 4-2114. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0700h

Figure 4-1033. TPCC_AETCTL Name Register

31	30	29	28	27	26	25	24
EN	RES65						
R/W	R						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES65							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES65		ENDINT					
R		R/W					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES66	TYPE	STRTEVT					
R	R/W	R/W					
0h	0h	0h					

Table 4-2115. TPCC_AETCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	AET Enable: EN = 0 : AET event generation is disabled. EN = 1 : AET event generation is enabled.
30:14	RES65	R	0h	RESERVE FIELD
13:8	ENDINT	R/W	0h	AET End Interrupt: Dictates the completion interrupt number that will force the tpcc_aet signal to be deasserted [low]
7	RES66	R	0h	RESERVE FIELD
6	TYPE	R/W	0h	AET Event Type: TYPE = 0 : Event specified by STARTEVT applies to DMA Events [set by ER ESR or CER] TYPE = 1 : Event specified by STARTEVT applies to QDMA Events
5:0	STRTEVT	R/W	0h	AET Start Event: Dictates the Event Number that will force the tpcc_aet signal to be asserted [high]

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4.4.2.41 TPCC_AETSTAT Register

4.4.2.41.1 TPCC_AETSTAT Register (Offset = 704h) [reset = 0h]

Advanced Event Trigger Stat

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Table 4-2116. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0704h

Figure 4-1034. TPCC_AETSTAT Name Register

31	30	29	28	27	26	25	24
RES67							
R							
0h							
23	22	21	20	19	18	17	16
RES67							
R							
0h							
15	14	13	12	11	10	9	8
RES67							
R							
0h							
7	6	5	4	3	2	1	0
RES67							STAT
R							R
0h							0h

Table 4-2117. TPCC_AETSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES67	R	0h	RESERVE FIELD
0	STAT	R	0h	AET Status: AETSTAT = 0 : tpcc_aet is currently low. AETSTAT = 1 : tpcc_aet is currently high.

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4.4.2.42 TPCC_AETCMD Register

4.4.2.42.1 TPCC_AETCMD Register (Offset = 708h) [reset = 0h]

AET Command

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Table 4-2118. Instance Table

Instance Name	Physical Address
EDMA0	52A0 0708h

Figure 4-1035. TPCC_AETCMD Name Register

31	30	29	28	27	26	25	24
RES68							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES68							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES68							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES68							CLR
R							W
0h							0h

Table 4-2119. TPCC_AETCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RES68	R	0h	RESERVE FIELD
0	CLR	W	0h	AET Clear command: CPU write of '1' to the CLR bit causes the tpcc_aet output signal and AETSTAT.STAT register to be cleared. CPU write of '0' has no effect..

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4.4.2.43 TPCC_ER Register

4.4.2.43.1 TPCC_ER Register (Offset = 1000h) [reset = 0h]

Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

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Table 4-2120. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1000h

Figure 4-1036. TPCC_ER Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2121. TPCC_ER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31
30	E30	R	0h	Event #30
29	E29	R	0h	Event #29
28	E28	R	0h	Event #28
27	E27	R	0h	Event #27
26	E26	R	0h	Event #26
25	E25	R	0h	Event #25
24	E24	R	0h	Event #24
23	E23	R	0h	Event #23
22	E22	R	0h	Event #22
21	E21	R	0h	Event #21
20	E20	R	0h	Event #20
19	E19	R	0h	Event #19
18	E18	R	0h	Event #18

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Table 4-2121. TPCC_ER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	E17	R	0h	Event #17
16	E16	R	0h	Event #16
15	E15	R	0h	Event #15
14	E14	R	0h	Event #14
13	E13	R	0h	Event #13
12	E12	R	0h	Event #12
11	E11	R	0h	Event #11
10	E10	R	0h	Event #10
9	E9	R	0h	Event #9
8	E8	R	0h	Event #8
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.44 TPCC_ERH Register

4.4.2.44.1 TPCC_ERH Register (Offset = 1004h) [reset = 0h]

Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

Return to Summary Table

Table 4-2122. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1004h

Figure 4-1037. TPCC_ERH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2123. TPCC_ERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63
30	E62	R	0h	Event #62
29	E61	R	0h	Event #61
28	E60	R	0h	Event #60
27	E59	R	0h	Event #59
26	E58	R	0h	Event #58
25	E57	R	0h	Event #57
24	E56	R	0h	Event #56
23	E55	R	0h	Event #55
22	E54	R	0h	Event #54
21	E53	R	0h	Event #53
20	E52	R	0h	Event #52
19	E51	R	0h	Event #51
18	E50	R	0h	Event #50

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Table 4-2123. TPCC_ERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	E49	R	0h	Event #49
16	E48	R	0h	Event #48
15	E47	R	0h	Event #47
14	E46	R	0h	Event #46
13	E45	R	0h	Event #45
12	E44	R	0h	Event #44
11	E43	R	0h	Event #43
10	E42	R	0h	Event #42
9	E41	R	0h	Event #41
8	E40	R	0h	Event #40
7	E39	R	0h	Event #39
6	E38	R	0h	Event #38
5	E37	R	0h	Event #37
4	E36	R	0h	Event #36
3	E35	R	0h	Event #35
2	E34	R	0h	Event #34
1	E33	R	0h	Event #33
0	E32	R	0h	Event #32

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4.4.2.45 TPCC_ECR Register

4.4.2.45.1 TPCC_ECR Register (Offset = 1008h) [reset = 0h]

Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

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Table 4-2124. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1008h

Figure 4-1038. TPCC_ECR Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2125. TPCC_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31
30	E30	W	0h	Event #30
29	E29	W	0h	Event #29
28	E28	W	0h	Event #28
27	E27	W	0h	Event #27
26	E26	W	0h	Event #26
25	E25	W	0h	Event #25
24	E24	W	0h	Event #24
23	E23	W	0h	Event #23
22	E22	W	0h	Event #22
21	E21	W	0h	Event #21
20	E20	W	0h	Event #20
19	E19	W	0h	Event #19
18	E18	W	0h	Event #18
17	E17	W	0h	Event #17
16	E16	W	0h	Event #16
15	E15	W	0h	Event #15
14	E14	W	0h	Event #14
13	E13	W	0h	Event #13

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Table 4-2125. TPCC_ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event #12
11	E11	W	0h	Event #11
10	E10	W	0h	Event #10
9	E9	W	0h	Event #9
8	E8	W	0h	Event #8
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.46 TPCC_ECRH Register

4.4.2.46.1 TPCC_ECRH Register (Offset = 100Ch) [reset = 0h]

Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

Return to Summary Table

Table 4-2126. Instance Table

Instance Name	Physical Address
EDMA0	52A0 100Ch

Figure 4-1039. TPCC_ECRH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2127. TPCC_ECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63
30	E62	W	0h	Event #62
29	E61	W	0h	Event #61
28	E60	W	0h	Event #60
27	E59	W	0h	Event #59
26	E58	W	0h	Event #58
25	E57	W	0h	Event #57
24	E56	W	0h	Event #56
23	E55	W	0h	Event #55
22	E54	W	0h	Event #54
21	E53	W	0h	Event #53
20	E52	W	0h	Event #52
19	E51	W	0h	Event #51
18	E50	W	0h	Event #50
17	E49	W	0h	Event #49
16	E48	W	0h	Event #48
15	E47	W	0h	Event #47
14	E46	W	0h	Event #46
13	E45	W	0h	Event #45

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Table 4-2127. TPCC_ECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	W	0h	Event #44
11	E43	W	0h	Event #43
10	E42	W	0h	Event #42
9	E41	W	0h	Event #41
8	E40	W	0h	Event #40
7	E39	W	0h	Event #39
6	E38	W	0h	Event #38
5	E37	W	0h	Event #37
4	E36	W	0h	Event #36
3	E35	W	0h	Event #35
2	E34	W	0h	Event #34
1	E33	W	0h	Event #33
0	E32	W	0h	Event #32

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4.4.2.47 TPCC_ESR Register

4.4.2.47.1 TPCC_ESR Register (Offset = 1010h) [reset = 0h]

Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

Return to Summary Table

Table 4-2128. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1010h

Figure 4-1040. TPCC_ESR Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2129. TPCC_ESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31
30	E30	W	0h	Event #30
29	E29	W	0h	Event #29
28	E28	W	0h	Event #28
27	E27	W	0h	Event #27
26	E26	W	0h	Event #26
25	E25	W	0h	Event #25
24	E24	W	0h	Event #24
23	E23	W	0h	Event #23
22	E22	W	0h	Event #22
21	E21	W	0h	Event #21
20	E20	W	0h	Event #20
19	E19	W	0h	Event #19
18	E18	W	0h	Event #18
17	E17	W	0h	Event #17
16	E16	W	0h	Event #16
15	E15	W	0h	Event #15
14	E14	W	0h	Event #14
13	E13	W	0h	Event #13

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Table 4-2129. TPCC_ESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event #12
11	E11	W	0h	Event #11
10	E10	W	0h	Event #10
9	E9	W	0h	Event #9
8	E8	W	0h	Event #8
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.48 TPCC_ESRH Register

4.4.2.48.1 TPCC_ESRH Register (Offset = 1014h) [reset = 0h]

Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Return to Summary Table

Table 4-2130. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1014h

Figure 4-1041. TPCC_ESRH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2131. TPCC_ESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63
30	E62	W	0h	Event #62
29	E61	W	0h	Event #61
28	E60	W	0h	Event #60
27	E59	W	0h	Event #59
26	E58	W	0h	Event #58
25	E57	W	0h	Event #57
24	E56	W	0h	Event #56
23	E55	W	0h	Event #55
22	E54	W	0h	Event #54
21	E53	W	0h	Event #53
20	E52	W	0h	Event #52
19	E51	W	0h	Event #51
18	E50	W	0h	Event #50
17	E49	W	0h	Event #49
16	E48	W	0h	Event #48
15	E47	W	0h	Event #47
14	E46	W	0h	Event #46
13	E45	W	0h	Event #45

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Table 4-2131. TPCC_ESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	W	0h	Event #44
11	E43	W	0h	Event #43
10	E42	W	0h	Event #42
9	E41	W	0h	Event #41
8	E40	W	0h	Event #40
7	E39	W	0h	Event #39
6	E38	W	0h	Event #38
5	E37	W	0h	Event #37
4	E36	W	0h	Event #36
3	E35	W	0h	Event #35
2	E34	W	0h	Event #34
1	E33	W	0h	Event #33
0	E32	W	0h	Event #32

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4.4.2.49 TPCC_CER Register

4.4.2.49.1 TPCC_CER Register (Offset = 1018h) [reset = 0h]

Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

Return to Summary Table

Table 4-2132. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1018h

Figure 4-1042. TPCC_CER Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2133. TPCC_CER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31
30	E30	R	0h	Event #30
29	E29	R	0h	Event #29
28	E28	R	0h	Event #28
27	E27	R	0h	Event #27
26	E26	R	0h	Event #26
25	E25	R	0h	Event #25
24	E24	R	0h	Event #24
23	E23	R	0h	Event #23
22	E22	R	0h	Event #22
21	E21	R	0h	Event #21
20	E20	R	0h	Event #20
19	E19	R	0h	Event #19
18	E18	R	0h	Event #18
17	E17	R	0h	Event #17

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Table 4-2133. TPCC_CER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	E16	R	0h	Event #16
15	E15	R	0h	Event #15
14	E14	R	0h	Event #14
13	E13	R	0h	Event #13
12	E12	R	0h	Event #12
11	E11	R	0h	Event #11
10	E10	R	0h	Event #10
9	E9	R	0h	Event #9
8	E8	R	0h	Event #8
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.50 TPCC_CERH Register

4.4.2.50.1 TPCC_CERH Register (Offset = 101Ch) [reset = 0h]

Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

Return to Summary Table

Table 4-2134. Instance Table

Instance Name	Physical Address
EDMA0	52A0 101Ch

Figure 4-1043. TPCC_CERH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2135. TPCC_CERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63
30	E62	R	0h	Event #62
29	E61	R	0h	Event #61
28	E60	R	0h	Event #60
27	E59	R	0h	Event #59
26	E58	R	0h	Event #58
25	E57	R	0h	Event #57
24	E56	R	0h	Event #56
23	E55	R	0h	Event #55
22	E54	R	0h	Event #54
21	E53	R	0h	Event #53
20	E52	R	0h	Event #52
19	E51	R	0h	Event #51
18	E50	R	0h	Event #50

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Table 4-2135. TPCC_CERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	E49	R	0h	Event #49
16	E48	R	0h	Event #48
15	E47	R	0h	Event #47
14	E46	R	0h	Event #46
13	E45	R	0h	Event #45
12	E44	R	0h	Event #44
11	E43	R	0h	Event #43
10	E42	R	0h	Event #42
9	E41	R	0h	Event #41
8	E40	R	0h	Event #40
7	E39	R	0h	Event #39
6	E38	R	0h	Event #38
5	E37	R	0h	Event #37
4	E36	R	0h	Event #36
3	E35	R	0h	Event #35
2	E34	R	0h	Event #34
1	E33	R	0h	Event #33
0	E32	R	0h	Event #32

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4.4.2.51 TPCC_EER Register

4.4.2.51.1 TPCC_EER Register (Offset = 1020h) [reset = 0h]

Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Return to Summary Table

Table 4-2136. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1020h

Figure 4-1044. TPCC_EER Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2137. TPCC_EER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31
30	E30	R	0h	Event #30
29	E29	R	0h	Event #29
28	E28	R	0h	Event #28
27	E27	R	0h	Event #27
26	E26	R	0h	Event #26
25	E25	R	0h	Event #25
24	E24	R	0h	Event #24
23	E23	R	0h	Event #23
22	E22	R	0h	Event #22
21	E21	R	0h	Event #21
20	E20	R	0h	Event #20
19	E19	R	0h	Event #19
18	E18	R	0h	Event #18

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Table 4-2137. TPCC_EER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	E17	R	0h	Event #17
16	E16	R	0h	Event #16
15	E15	R	0h	Event #15
14	E14	R	0h	Event #14
13	E13	R	0h	Event #13
12	E12	R	0h	Event #12
11	E11	R	0h	Event #11
10	E10	R	0h	Event #10
9	E9	R	0h	Event #9
8	E8	R	0h	Event #8
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.52 TPCC_EERH Register

4.4.2.52.1 TPCC_EERH Register (Offset = 1024h) [reset = 0h]

Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

Return to Summary Table

Table 4-2138. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1024h

Figure 4-1045. TPCC_EERH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2139. TPCC_EERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63
30	E62	R	0h	Event #62
29	E61	R	0h	Event #61
28	E60	R	0h	Event #60
27	E59	R	0h	Event #59
26	E58	R	0h	Event #58
25	E57	R	0h	Event #57
24	E56	R	0h	Event #56
23	E55	R	0h	Event #55
22	E54	R	0h	Event #54
21	E53	R	0h	Event #53
20	E52	R	0h	Event #52
19	E51	R	0h	Event #51
18	E50	R	0h	Event #50

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Table 4-2139. TPCC_EERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	E49	R	0h	Event #49
16	E48	R	0h	Event #48
15	E47	R	0h	Event #47
14	E46	R	0h	Event #46
13	E45	R	0h	Event #45
12	E44	R	0h	Event #44
11	E43	R	0h	Event #43
10	E42	R	0h	Event #42
9	E41	R	0h	Event #41
8	E40	R	0h	Event #40
7	E39	R	0h	Event #39
6	E38	R	0h	Event #38
5	E37	R	0h	Event #37
4	E36	R	0h	Event #36
3	E35	R	0h	Event #35
2	E34	R	0h	Event #34
1	E33	R	0h	Event #33
0	E32	R	0h	Event #32

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4.4.2.53 TPCC_EECR Register

4.4.2.53.1 TPCC_EECR Register (Offset = 1028h) [reset = 0h]

Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

Return to Summary Table

Table 4-2140. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1028h

Figure 4-1046. TPCC_EECR Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2141. TPCC_EECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31
30	E30	W	0h	Event #30
29	E29	W	0h	Event #29
28	E28	W	0h	Event #28
27	E27	W	0h	Event #27
26	E26	W	0h	Event #26
25	E25	W	0h	Event #25
24	E24	W	0h	Event #24
23	E23	W	0h	Event #23
22	E22	W	0h	Event #22
21	E21	W	0h	Event #21
20	E20	W	0h	Event #20
19	E19	W	0h	Event #19
18	E18	W	0h	Event #18
17	E17	W	0h	Event #17
16	E16	W	0h	Event #16
15	E15	W	0h	Event #15
14	E14	W	0h	Event #14
13	E13	W	0h	Event #13

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Table 4-2141. TPCC_EECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event #12
11	E11	W	0h	Event #11
10	E10	W	0h	Event #10
9	E9	W	0h	Event #9
8	E8	W	0h	Event #8
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.54 TPCC_EECRH Register

4.4.2.54.1 TPCC_EECRH Register (Offset = 102Ch) [reset = 0h]

Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

Return to Summary Table

Table 4-2142. Instance Table

Instance Name	Physical Address
EDMA0	52A0 102Ch

Figure 4-1047. TPCC_EECRH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2143. TPCC_EECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63
30	E62	W	0h	Event #62
29	E61	W	0h	Event #61
28	E60	W	0h	Event #60
27	E59	W	0h	Event #59
26	E58	W	0h	Event #58
25	E57	W	0h	Event #57
24	E56	W	0h	Event #56
23	E55	W	0h	Event #55
22	E54	W	0h	Event #54
21	E53	W	0h	Event #53
20	E52	W	0h	Event #52
19	E51	W	0h	Event #51
18	E50	W	0h	Event #50
17	E49	W	0h	Event #49
16	E48	W	0h	Event #48
15	E47	W	0h	Event #47
14	E46	W	0h	Event #46
13	E45	W	0h	Event #45

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Table 4-2143. TPCC_EECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	W	0h	Event #44
11	E43	W	0h	Event #43
10	E42	W	0h	Event #42
9	E41	W	0h	Event #41
8	E40	W	0h	Event #40
7	E39	W	0h	Event #39
6	E38	W	0h	Event #38
5	E37	W	0h	Event #37
4	E36	W	0h	Event #36
3	E35	W	0h	Event #35
2	E34	W	0h	Event #34
1	E33	W	0h	Event #33
0	E32	W	0h	Event #32

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4.4.2.55 TPCC_EESR Register

4.4.2.55.1 TPCC_EESR Register (Offset = 1030h) [reset = 0h]

Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Return to Summary Table

Table 4-2144. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1030h

Figure 4-1048. TPCC_EESR Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2145. TPCC_EESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31
30	E30	W	0h	Event #30
29	E29	W	0h	Event #29
28	E28	W	0h	Event #28
27	E27	W	0h	Event #27
26	E26	W	0h	Event #26
25	E25	W	0h	Event #25
24	E24	W	0h	Event #24
23	E23	W	0h	Event #23
22	E22	W	0h	Event #22
21	E21	W	0h	Event #21
20	E20	W	0h	Event #20
19	E19	W	0h	Event #19
18	E18	W	0h	Event #18
17	E17	W	0h	Event #17
16	E16	W	0h	Event #16
15	E15	W	0h	Event #15
14	E14	W	0h	Event #14
13	E13	W	0h	Event #13

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Table 4-2145. TPCC_EESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event #12
11	E11	W	0h	Event #11
10	E10	W	0h	Event #10
9	E9	W	0h	Event #9
8	E8	W	0h	Event #8
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.56 TPCC_EESRH Register

4.4.2.56.1 TPCC_EESRH Register (Offset = 1034h) [reset = 0h]

Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

Return to Summary Table

Table 4-2146. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1034h

Figure 4-1049. TPCC_EESRH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2147. TPCC_EESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63
30	E62	W	0h	Event #62
29	E61	W	0h	Event #61
28	E60	W	0h	Event #60
27	E59	W	0h	Event #59
26	E58	W	0h	Event #58
25	E57	W	0h	Event #57
24	E56	W	0h	Event #56
23	E55	W	0h	Event #55
22	E54	W	0h	Event #54
21	E53	W	0h	Event #53
20	E52	W	0h	Event #52
19	E51	W	0h	Event #51
18	E50	W	0h	Event #50
17	E49	W	0h	Event #49
16	E48	W	0h	Event #48
15	E47	W	0h	Event #47
14	E46	W	0h	Event #46
13	E45	W	0h	Event #45

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Table 4-2147. TPCC_EESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	W	0h	Event #44
11	E43	W	0h	Event #43
10	E42	W	0h	Event #42
9	E41	W	0h	Event #41
8	E40	W	0h	Event #40
7	E39	W	0h	Event #39
6	E38	W	0h	Event #38
5	E37	W	0h	Event #37
4	E36	W	0h	Event #36
3	E35	W	0h	Event #35
2	E34	W	0h	Event #34
1	E33	W	0h	Event #33
0	E32	W	0h	Event #32

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4.4.2.57 TPCC_SER Register

4.4.2.57.1 TPCC_SER Register (Offset = 1038h) [reset = 0h]

Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Return to Summary Table

Table 4-2148. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1038h

Figure 4-1050. TPCC_SER Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2149. TPCC_SER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31
30	E30	R	0h	Event #30
29	E29	R	0h	Event #29
28	E28	R	0h	Event #28
27	E27	R	0h	Event #27
26	E26	R	0h	Event #26
25	E25	R	0h	Event #25
24	E24	R	0h	Event #24
23	E23	R	0h	Event #23
22	E22	R	0h	Event #22
21	E21	R	0h	Event #21
20	E20	R	0h	Event #20
19	E19	R	0h	Event #19
18	E18	R	0h	Event #18
17	E17	R	0h	Event #17
16	E16	R	0h	Event #16
15	E15	R	0h	Event #15
14	E14	R	0h	Event #14

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Table 4-2149. TPCC_SER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	E13	R	0h	Event #13
12	E12	R	0h	Event #12
11	E11	R	0h	Event #11
10	E10	R	0h	Event #10
9	E9	R	0h	Event #9
8	E8	R	0h	Event #8
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.58 TPCC_SERH Register

4.4.2.58.1 TPCC_SERH Register (Offset = 103Ch) [reset = 0h]

Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Return to Summary Table

Table 4-2150. Instance Table

Instance Name	Physical Address
EDMA0	52A0 103Ch

Figure 4-1051. TPCC_SERH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2151. TPCC_SERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63
30	E62	R	0h	Event #62
29	E61	R	0h	Event #61
28	E60	R	0h	Event #60
27	E59	R	0h	Event #59
26	E58	R	0h	Event #58
25	E57	R	0h	Event #57
24	E56	R	0h	Event #56
23	E55	R	0h	Event #55
22	E54	R	0h	Event #54
21	E53	R	0h	Event #53
20	E52	R	0h	Event #52
19	E51	R	0h	Event #51
18	E50	R	0h	Event #50
17	E49	R	0h	Event #49
16	E48	R	0h	Event #48
15	E47	R	0h	Event #47
14	E46	R	0h	Event #46

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Table 4-2151. TPCC_SERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	E45	R	0h	Event #45
12	E44	R	0h	Event #44
11	E43	R	0h	Event #43
10	E42	R	0h	Event #42
9	E41	R	0h	Event #41
8	E40	R	0h	Event #40
7	E39	R	0h	Event #39
6	E38	R	0h	Event #38
5	E37	R	0h	Event #37
4	E36	R	0h	Event #36
3	E35	R	0h	Event #35
2	E34	R	0h	Event #34
1	E33	R	0h	Event #33
0	E32	R	0h	Event #32

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4.4.2.59 TPCC_SECR Register

4.4.2.59.1 TPCC_SECR Register (Offset = 1040h) [reset = 0h]

Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

Return to Summary Table

Table 4-2152. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1040h

Figure 4-1052. TPCC_SECR Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2153. TPCC_SECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31
30	E30	W	0h	Event #30
29	E29	W	0h	Event #29
28	E28	W	0h	Event #28
27	E27	W	0h	Event #27
26	E26	W	0h	Event #26
25	E25	W	0h	Event #25
24	E24	W	0h	Event #24
23	E23	W	0h	Event #23
22	E22	W	0h	Event #22
21	E21	W	0h	Event #21
20	E20	W	0h	Event #20
19	E19	W	0h	Event #19
18	E18	W	0h	Event #18
17	E17	W	0h	Event #17
16	E16	W	0h	Event #16
15	E15	W	0h	Event #15
14	E14	W	0h	Event #14
13	E13	W	0h	Event #13

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Table 4-2153. TPCC_SECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event #12
11	E11	W	0h	Event #11
10	E10	W	0h	Event #10
9	E9	W	0h	Event #9
8	E8	W	0h	Event #8
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.60 TPCC_SECRH Register

4.4.2.60.1 TPCC_SECRH Register (Offset = 1044h) [reset = 0h]

Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

Return to Summary Table

Table 4-2154. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1044h

Figure 4-1053. TPCC_SECRH Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2155. TPCC_SECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63
30	E62	W	0h	Event #62
29	E61	W	0h	Event #61
28	E60	W	0h	Event #60
27	E59	W	0h	Event #59
26	E58	W	0h	Event #58
25	E57	W	0h	Event #57
24	E56	W	0h	Event #56
23	E55	W	0h	Event #55
22	E54	W	0h	Event #54
21	E53	W	0h	Event #53
20	E52	W	0h	Event #52
19	E51	W	0h	Event #51
18	E50	W	0h	Event #50
17	E49	W	0h	Event #49
16	E48	W	0h	Event #48
15	E47	W	0h	Event #47
14	E46	W	0h	Event #46
13	E45	W	0h	Event #45

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Table 4-2155. TPCC_SECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	W	0h	Event #44
11	E43	W	0h	Event #43
10	E42	W	0h	Event #42
9	E41	W	0h	Event #41
8	E40	W	0h	Event #40
7	E39	W	0h	Event #39
6	E38	W	0h	Event #38
5	E37	W	0h	Event #37
4	E36	W	0h	Event #36
3	E35	W	0h	Event #35
2	E34	W	0h	Event #34
1	E33	W	0h	Event #33
0	E32	W	0h	Event #32

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4.4.2.61 TPCC_IER Register

4.4.2.61.1 TPCC_IER Register (Offset = 1050h) [reset = 0h]

Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

Return to Summary Table

Table 4-2156. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1050h

Figure 4-1054. TPCC_IER Name Register

31	30	29	28	27	26	25	24
I31	I30	I29	I28	I27	I26	I25	I24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I23	I22	I21	I20	I19	I18	I17	I16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I15	I14	I13	I12	I11	I10	I9	I8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2157. TPCC_IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	R	0h	Interrupt associated with TCC #31
30	I30	R	0h	Interrupt associated with TCC #30
29	I29	R	0h	Interrupt associated with TCC #29
28	I28	R	0h	Interrupt associated with TCC #28
27	I27	R	0h	Interrupt associated with TCC #27
26	I26	R	0h	Interrupt associated with TCC #26
25	I25	R	0h	Interrupt associated with TCC #25
24	I24	R	0h	Interrupt associated with TCC #24
23	I23	R	0h	Interrupt associated with TCC #23
22	I22	R	0h	Interrupt associated with TCC #22
21	I21	R	0h	Interrupt associated with TCC #21
20	I20	R	0h	Interrupt associated with TCC #20
19	I19	R	0h	Interrupt associated with TCC #19
18	I18	R	0h	Interrupt associated with TCC #18
17	I17	R	0h	Interrupt associated with TCC #17
16	I16	R	0h	Interrupt associated with TCC #16
15	I15	R	0h	Interrupt associated with TCC #15
14	I14	R	0h	Interrupt associated with TCC #14

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Table 4-2157. TPCC_IER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	I13	R	0h	Interrupt associated with TCC #13
12	I12	R	0h	Interrupt associated with TCC #12
11	I11	R	0h	Interrupt associated with TCC #11
10	I10	R	0h	Interrupt associated with TCC #10
9	I9	R	0h	Interrupt associated with TCC #9
8	I8	R	0h	Interrupt associated with TCC #8
7	I7	R	0h	Interrupt associated with TCC #7
6	I6	R	0h	Interrupt associated with TCC #6
5	I5	R	0h	Interrupt associated with TCC #5
4	I4	R	0h	Interrupt associated with TCC #4
3	I3	R	0h	Interrupt associated with TCC #3
2	I2	R	0h	Interrupt associated with TCC #2
1	I1	R	0h	Interrupt associated with TCC #1
0	I0	R	0h	Interrupt associated with TCC #0

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4.4.2.62 TPCC_IERH Register

4.4.2.62.1 TPCC_IERH Register (Offset = 1054h) [reset = 0h]

Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

Return to Summary Table

Table 4-2158. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1054h

Figure 4-1055. TPCC_IERH Name Register

31	30	29	28	27	26	25	24
I63	I62	I61	I60	I59	I58	I57	I56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I55	I54	I53	I52	I51	I50	I49	I48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I47	I46	I45	I44	I43	I42	I41	I40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I39	I38	I37	I36	I35	I34	I33	I32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2159. TPCC_IERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	R	0h	Interrupt associated with TCC #63
30	I62	R	0h	Interrupt associated with TCC #62
29	I61	R	0h	Interrupt associated with TCC #61
28	I60	R	0h	Interrupt associated with TCC #60
27	I59	R	0h	Interrupt associated with TCC #59
26	I58	R	0h	Interrupt associated with TCC #58
25	I57	R	0h	Interrupt associated with TCC #57
24	I56	R	0h	Interrupt associated with TCC #56
23	I55	R	0h	Interrupt associated with TCC #55
22	I54	R	0h	Interrupt associated with TCC #54
21	I53	R	0h	Interrupt associated with TCC #53
20	I52	R	0h	Interrupt associated with TCC #52
19	I51	R	0h	Interrupt associated with TCC #51
18	I50	R	0h	Interrupt associated with TCC #50
17	I49	R	0h	Interrupt associated with TCC #49
16	I48	R	0h	Interrupt associated with TCC #48
15	I47	R	0h	Interrupt associated with TCC #47
14	I46	R	0h	Interrupt associated with TCC #46

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Table 4-2159. TPCC_IERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	I45	R	0h	Interrupt associated with TCC #45
12	I44	R	0h	Interrupt associated with TCC #44
11	I43	R	0h	Interrupt associated with TCC #43
10	I42	R	0h	Interrupt associated with TCC #42
9	I41	R	0h	Interrupt associated with TCC #41
8	I40	R	0h	Interrupt associated with TCC #40
7	I39	R	0h	Interrupt associated with TCC #39
6	I38	R	0h	Interrupt associated with TCC #38
5	I37	R	0h	Interrupt associated with TCC #37
4	I36	R	0h	Interrupt associated with TCC #36
3	I35	R	0h	Interrupt associated with TCC #35
2	I34	R	0h	Interrupt associated with TCC #34
1	I33	R	0h	Interrupt associated with TCC #33
0	I32	R	0h	Interrupt associated with TCC #32

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4.4.2.63 TPCC_IECR Register

4.4.2.63.1 TPCC_IECR Register (Offset = 1058h) [reset = 0h]

Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

Return to Summary Table

Table 4-2160. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1058h

Figure 4-1056. TPCC_IECR Name Register

31	30	29	28	27	26	25	24
I31	I30	I29	I28	I27	I26	I25	I24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I15	I14	I13	I12	I11	I10	I9	I8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2161. TPCC_IECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31
30	I30	W	0h	Interrupt associated with TCC #30
29	I29	W	0h	Interrupt associated with TCC #29
28	I28	W	0h	Interrupt associated with TCC #28
27	I27	W	0h	Interrupt associated with TCC #27
26	I26	W	0h	Interrupt associated with TCC #26
25	I25	W	0h	Interrupt associated with TCC #25
24	I24	W	0h	Interrupt associated with TCC #24
23	I23	W	0h	Interrupt associated with TCC #23
22	I22	W	0h	Interrupt associated with TCC #22
21	I21	W	0h	Interrupt associated with TCC #21
20	I20	W	0h	Interrupt associated with TCC #20
19	I19	W	0h	Interrupt associated with TCC #19
18	I18	W	0h	Interrupt associated with TCC #18
17	I17	W	0h	Interrupt associated with TCC #17
16	I16	W	0h	Interrupt associated with TCC #16
15	I15	W	0h	Interrupt associated with TCC #15
14	I14	W	0h	Interrupt associated with TCC #14
13	I13	W	0h	Interrupt associated with TCC #13

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Table 4-2161. TPCC_IECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I12	W	0h	Interrupt associated with TCC #12
11	I11	W	0h	Interrupt associated with TCC #11
10	I10	W	0h	Interrupt associated with TCC #10
9	I9	W	0h	Interrupt associated with TCC #9
8	I8	W	0h	Interrupt associated with TCC #8
7	I7	W	0h	Interrupt associated with TCC #7
6	I6	W	0h	Interrupt associated with TCC #6
5	I5	W	0h	Interrupt associated with TCC #5
4	I4	W	0h	Interrupt associated with TCC #4
3	I3	W	0h	Interrupt associated with TCC #3
2	I2	W	0h	Interrupt associated with TCC #2
1	I1	W	0h	Interrupt associated with TCC #1
0	I0	W	0h	Interrupt associated with TCC #0

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4.4.2.64 TPCC_IECRH Register

4.4.2.64.1 TPCC_IECRH Register (Offset = 105Ch) [reset = 0h]

Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Return to Summary Table

Table 4-2162. Instance Table

Instance Name	Physical Address
EDMA0	52A0 105Ch

Figure 4-1057. TPCC_IECRH Name Register

31	30	29	28	27	26	25	24
I63	I62	I61	I60	I59	I58	I57	I56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I47	I46	I45	I44	I43	I42	I41	I40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2163. TPCC_IECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63
30	I62	W	0h	Interrupt associated with TCC #62
29	I61	W	0h	Interrupt associated with TCC #61
28	I60	W	0h	Interrupt associated with TCC #60
27	I59	W	0h	Interrupt associated with TCC #59
26	I58	W	0h	Interrupt associated with TCC #58
25	I57	W	0h	Interrupt associated with TCC #57
24	I56	W	0h	Interrupt associated with TCC #56
23	I55	W	0h	Interrupt associated with TCC #55
22	I54	W	0h	Interrupt associated with TCC #54
21	I53	W	0h	Interrupt associated with TCC #53
20	I52	W	0h	Interrupt associated with TCC #52
19	I51	W	0h	Interrupt associated with TCC #51
18	I50	W	0h	Interrupt associated with TCC #50
17	I49	W	0h	Interrupt associated with TCC #49
16	I48	W	0h	Interrupt associated with TCC #48
15	I47	W	0h	Interrupt associated with TCC #47
14	I46	W	0h	Interrupt associated with TCC #46
13	I45	W	0h	Interrupt associated with TCC #45

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Table 4-2163. TPCC_IECRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I44	W	0h	Interrupt associated with TCC #44
11	I43	W	0h	Interrupt associated with TCC #43
10	I42	W	0h	Interrupt associated with TCC #42
9	I41	W	0h	Interrupt associated with TCC #41
8	I40	W	0h	Interrupt associated with TCC #40
7	I39	W	0h	Interrupt associated with TCC #39
6	I38	W	0h	Interrupt associated with TCC #38
5	I37	W	0h	Interrupt associated with TCC #37
4	I36	W	0h	Interrupt associated with TCC #36
3	I35	W	0h	Interrupt associated with TCC #35
2	I34	W	0h	Interrupt associated with TCC #34
1	I33	W	0h	Interrupt associated with TCC #33
0	I32	W	0h	Interrupt associated with TCC #32

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4.4.2.65 TPCC_IESR Register

4.4.2.65.1 TPCC_IESR Register (Offset = 1060h) [reset = 0h]

Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Return to Summary Table

Table 4-2164. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1060h

Figure 4-1058. TPCC_IESR Name Register

31	30	29	28	27	26	25	24
I31	I30	I29	I28	I27	I26	I25	I24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I15	I14	I13	I12	I11	I10	I9	I8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2165. TPCC_IESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31
30	I30	W	0h	Interrupt associated with TCC #30
29	I29	W	0h	Interrupt associated with TCC #29
28	I28	W	0h	Interrupt associated with TCC #28
27	I27	W	0h	Interrupt associated with TCC #27
26	I26	W	0h	Interrupt associated with TCC #26
25	I25	W	0h	Interrupt associated with TCC #25
24	I24	W	0h	Interrupt associated with TCC #24
23	I23	W	0h	Interrupt associated with TCC #23
22	I22	W	0h	Interrupt associated with TCC #22
21	I21	W	0h	Interrupt associated with TCC #21
20	I20	W	0h	Interrupt associated with TCC #20
19	I19	W	0h	Interrupt associated with TCC #19
18	I18	W	0h	Interrupt associated with TCC #18
17	I17	W	0h	Interrupt associated with TCC #17
16	I16	W	0h	Interrupt associated with TCC #16
15	I15	W	0h	Interrupt associated with TCC #15
14	I14	W	0h	Interrupt associated with TCC #14
13	I13	W	0h	Interrupt associated with TCC #13

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Table 4-2165. TPCC_IESR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I12	W	0h	Interrupt associated with TCC #12
11	I11	W	0h	Interrupt associated with TCC #11
10	I10	W	0h	Interrupt associated with TCC #10
9	I9	W	0h	Interrupt associated with TCC #9
8	I8	W	0h	Interrupt associated with TCC #8
7	I7	W	0h	Interrupt associated with TCC #7
6	I6	W	0h	Interrupt associated with TCC #6
5	I5	W	0h	Interrupt associated with TCC #5
4	I4	W	0h	Interrupt associated with TCC #4
3	I3	W	0h	Interrupt associated with TCC #3
2	I2	W	0h	Interrupt associated with TCC #2
1	I1	W	0h	Interrupt associated with TCC #1
0	I0	W	0h	Interrupt associated with TCC #0

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4.4.2.66 TPCC_IESRH Register

4.4.2.66.1 TPCC_IESRH Register (Offset = 1064h) [reset = 0h]

Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

Return to Summary Table

Table 4-2166. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1064h

Figure 4-1059. TPCC_IESRH Name Register

31	30	29	28	27	26	25	24
I63	I62	I61	I60	I59	I58	I57	I56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I47	I46	I45	I44	I43	I42	I41	I40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2167. TPCC_IESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63
30	I62	W	0h	Interrupt associated with TCC #62
29	I61	W	0h	Interrupt associated with TCC #61
28	I60	W	0h	Interrupt associated with TCC #60
27	I59	W	0h	Interrupt associated with TCC #59
26	I58	W	0h	Interrupt associated with TCC #58
25	I57	W	0h	Interrupt associated with TCC #57
24	I56	W	0h	Interrupt associated with TCC #56
23	I55	W	0h	Interrupt associated with TCC #55
22	I54	W	0h	Interrupt associated with TCC #54
21	I53	W	0h	Interrupt associated with TCC #53
20	I52	W	0h	Interrupt associated with TCC #52
19	I51	W	0h	Interrupt associated with TCC #51
18	I50	W	0h	Interrupt associated with TCC #50
17	I49	W	0h	Interrupt associated with TCC #49
16	I48	W	0h	Interrupt associated with TCC #48
15	I47	W	0h	Interrupt associated with TCC #47
14	I46	W	0h	Interrupt associated with TCC #46
13	I45	W	0h	Interrupt associated with TCC #45

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Table 4-2167. TPCC_IESRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I44	W	0h	Interrupt associated with TCC #44
11	I43	W	0h	Interrupt associated with TCC #43
10	I42	W	0h	Interrupt associated with TCC #42
9	I41	W	0h	Interrupt associated with TCC #41
8	I40	W	0h	Interrupt associated with TCC #40
7	I39	W	0h	Interrupt associated with TCC #39
6	I38	W	0h	Interrupt associated with TCC #38
5	I37	W	0h	Interrupt associated with TCC #37
4	I36	W	0h	Interrupt associated with TCC #36
3	I35	W	0h	Interrupt associated with TCC #35
2	I34	W	0h	Interrupt associated with TCC #34
1	I33	W	0h	Interrupt associated with TCC #33
0	I32	W	0h	Interrupt associated with TCC #32

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4.4.2.67 TPCC_IPR Register

4.4.2.67.1 TPCC_IPR Register (Offset = 1068h) [reset = 0h]

Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

Return to Summary Table

Table 4-2168. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1068h

Figure 4-1060. TPCC_IPR Name Register

31	30	29	28	27	26	25	24
I31	I30	I29	I28	I27	I26	I25	I24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I23	I22	I21	I20	I19	I18	I17	I16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I15	I14	I13	I12	I11	I10	I9	I8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2169. TPCC_IPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	R	0h	Interrupt associated with TCC #31
30	I30	R	0h	Interrupt associated with TCC #30
29	I29	R	0h	Interrupt associated with TCC #29
28	I28	R	0h	Interrupt associated with TCC #28
27	I27	R	0h	Interrupt associated with TCC #27
26	I26	R	0h	Interrupt associated with TCC #26
25	I25	R	0h	Interrupt associated with TCC #25
24	I24	R	0h	Interrupt associated with TCC #24
23	I23	R	0h	Interrupt associated with TCC #23
22	I22	R	0h	Interrupt associated with TCC #22
21	I21	R	0h	Interrupt associated with TCC #21
20	I20	R	0h	Interrupt associated with TCC #20
19	I19	R	0h	Interrupt associated with TCC #19
18	I18	R	0h	Interrupt associated with TCC #18
17	I17	R	0h	Interrupt associated with TCC #17
16	I16	R	0h	Interrupt associated with TCC #16
15	I15	R	0h	Interrupt associated with TCC #15
14	I14	R	0h	Interrupt associated with TCC #14
13	I13	R	0h	Interrupt associated with TCC #13

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Table 4-2169. TPCC_IPR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I12	R	0h	Interrupt associated with TCC #12
11	I11	R	0h	Interrupt associated with TCC #11
10	I10	R	0h	Interrupt associated with TCC #10
9	I9	R	0h	Interrupt associated with TCC #9
8	I8	R	0h	Interrupt associated with TCC #8
7	I7	R	0h	Interrupt associated with TCC #7
6	I6	R	0h	Interrupt associated with TCC #6
5	I5	R	0h	Interrupt associated with TCC #5
4	I4	R	0h	Interrupt associated with TCC #4
3	I3	R	0h	Interrupt associated with TCC #3
2	I2	R	0h	Interrupt associated with TCC #2
1	I1	R	0h	Interrupt associated with TCC #1
0	I0	R	0h	Interrupt associated with TCC #0

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4.4.2.68 TPCC_IPRH Register

4.4.2.68.1 TPCC_IPRH Register (Offset = 106Ch) [reset = 0h]

Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

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Table 4-2170. Instance Table

Instance Name	Physical Address
EDMA0	52A0 106Ch

Figure 4-1061. TPCC_IPRH Name Register

31	30	29	28	27	26	25	24
I63	I62	I61	I60	I59	I58	I57	I56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I55	I54	I53	I52	I51	I50	I49	I48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I47	I46	I45	I44	I43	I42	I41	I40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I39	I38	I37	I36	I35	I34	I33	I32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2171. TPCC_IPRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	R	0h	Interrupt associated with TCC #63
30	I62	R	0h	Interrupt associated with TCC #62
29	I61	R	0h	Interrupt associated with TCC #61
28	I60	R	0h	Interrupt associated with TCC #60
27	I59	R	0h	Interrupt associated with TCC #59
26	I58	R	0h	Interrupt associated with TCC #58
25	I57	R	0h	Interrupt associated with TCC #57
24	I56	R	0h	Interrupt associated with TCC #56
23	I55	R	0h	Interrupt associated with TCC #55
22	I54	R	0h	Interrupt associated with TCC #54
21	I53	R	0h	Interrupt associated with TCC #53
20	I52	R	0h	Interrupt associated with TCC #52
19	I51	R	0h	Interrupt associated with TCC #51
18	I50	R	0h	Interrupt associated with TCC #50
17	I49	R	0h	Interrupt associated with TCC #49
16	I48	R	0h	Interrupt associated with TCC #48
15	I47	R	0h	Interrupt associated with TCC #47
14	I46	R	0h	Interrupt associated with TCC #46
13	I45	R	0h	Interrupt associated with TCC #45

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Table 4-2171. TPCC_IPRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I44	R	0h	Interrupt associated with TCC #44
11	I43	R	0h	Interrupt associated with TCC #43
10	I42	R	0h	Interrupt associated with TCC #42
9	I41	R	0h	Interrupt associated with TCC #41
8	I40	R	0h	Interrupt associated with TCC #40
7	I39	R	0h	Interrupt associated with TCC #39
6	I38	R	0h	Interrupt associated with TCC #38
5	I37	R	0h	Interrupt associated with TCC #37
4	I36	R	0h	Interrupt associated with TCC #36
3	I35	R	0h	Interrupt associated with TCC #35
2	I34	R	0h	Interrupt associated with TCC #34
1	I33	R	0h	Interrupt associated with TCC #33
0	I32	R	0h	Interrupt associated with TCC #32

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4.4.2.69 TPCC_ICR Register

4.4.2.69.1 TPCC_ICR Register (Offset = 1070h) [reset = 0h]

Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

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Table 4-2172. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1070h

Figure 4-1062. TPCC_ICR Name Register

31	30	29	28	27	26	25	24
I31	I30	I29	I28	I27	I26	I25	I24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I15	I14	I13	I12	I11	I10	I9	I8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2173. TPCC_ICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31
30	I30	W	0h	Interrupt associated with TCC #30
29	I29	W	0h	Interrupt associated with TCC #29
28	I28	W	0h	Interrupt associated with TCC #28
27	I27	W	0h	Interrupt associated with TCC #27
26	I26	W	0h	Interrupt associated with TCC #26
25	I25	W	0h	Interrupt associated with TCC #25
24	I24	W	0h	Interrupt associated with TCC #24
23	I23	W	0h	Interrupt associated with TCC #23
22	I22	W	0h	Interrupt associated with TCC #22
21	I21	W	0h	Interrupt associated with TCC #21
20	I20	W	0h	Interrupt associated with TCC #20
19	I19	W	0h	Interrupt associated with TCC #19
18	I18	W	0h	Interrupt associated with TCC #18
17	I17	W	0h	Interrupt associated with TCC #17
16	I16	W	0h	Interrupt associated with TCC #16
15	I15	W	0h	Interrupt associated with TCC #15
14	I14	W	0h	Interrupt associated with TCC #14
13	I13	W	0h	Interrupt associated with TCC #13

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Table 4-2173. TPCC_ICR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I12	W	0h	Interrupt associated with TCC #12
11	I11	W	0h	Interrupt associated with TCC #11
10	I10	W	0h	Interrupt associated with TCC #10
9	I9	W	0h	Interrupt associated with TCC #9
8	I8	W	0h	Interrupt associated with TCC #8
7	I7	W	0h	Interrupt associated with TCC #7
6	I6	W	0h	Interrupt associated with TCC #6
5	I5	W	0h	Interrupt associated with TCC #5
4	I4	W	0h	Interrupt associated with TCC #4
3	I3	W	0h	Interrupt associated with TCC #3
2	I2	W	0h	Interrupt associated with TCC #2
1	I1	W	0h	Interrupt associated with TCC #1
0	I0	W	0h	Interrupt associated with TCC #0

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4.4.2.70 TPCC_ICRH Register

4.4.2.70.1 TPCC_ICRH Register (Offset = 1074h) [reset = 0h]

Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

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Table 4-2174. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1074h

Figure 4-1063. TPCC_ICRH Name Register

31	30	29	28	27	26	25	24
I63	I62	I61	I60	I59	I58	I57	I56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I47	I46	I45	I44	I43	I42	I41	I40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2175. TPCC_ICRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63
30	I62	W	0h	Interrupt associated with TCC #62
29	I61	W	0h	Interrupt associated with TCC #61
28	I60	W	0h	Interrupt associated with TCC #60
27	I59	W	0h	Interrupt associated with TCC #59
26	I58	W	0h	Interrupt associated with TCC #58
25	I57	W	0h	Interrupt associated with TCC #57
24	I56	W	0h	Interrupt associated with TCC #56
23	I55	W	0h	Interrupt associated with TCC #55
22	I54	W	0h	Interrupt associated with TCC #54
21	I53	W	0h	Interrupt associated with TCC #53
20	I52	W	0h	Interrupt associated with TCC #52
19	I51	W	0h	Interrupt associated with TCC #51
18	I50	W	0h	Interrupt associated with TCC #50
17	I49	W	0h	Interrupt associated with TCC #49
16	I48	W	0h	Interrupt associated with TCC #48
15	I47	W	0h	Interrupt associated with TCC #47
14	I46	W	0h	Interrupt associated with TCC #46
13	I45	W	0h	Interrupt associated with TCC #45

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Table 4-2175. TPCC_ICRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I44	W	0h	Interrupt associated with TCC #44
11	I43	W	0h	Interrupt associated with TCC #43
10	I42	W	0h	Interrupt associated with TCC #42
9	I41	W	0h	Interrupt associated with TCC #41
8	I40	W	0h	Interrupt associated with TCC #40
7	I39	W	0h	Interrupt associated with TCC #39
6	I38	W	0h	Interrupt associated with TCC #38
5	I37	W	0h	Interrupt associated with TCC #37
4	I36	W	0h	Interrupt associated with TCC #36
3	I35	W	0h	Interrupt associated with TCC #35
2	I34	W	0h	Interrupt associated with TCC #34
1	I33	W	0h	Interrupt associated with TCC #33
0	I32	W	0h	Interrupt associated with TCC #32

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4.4.2.71 TPCC_IEVAL Register

4.4.2.71.1 TPCC_IEVAL Register (Offset = 1078h) [reset = 0h]

Interrupt Eval Register

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Table 4-2176. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1078h

Figure 4-1064. TPCC_IEVAL Name Register

31	30	29	28	27	26	25	24
RES69							
R							
0h							
23	22	21	20	19	18	17	16
RES69							
R							
0h							
15	14	13	12	11	10	9	8
RES69							
R							
0h							
7	6	5	4	3	2	1	0
RES69						SET	EVAL
R						W	W
0h						0h	0h

Table 4-2177. TPCC_IEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES69	R	0h	RESERVE FIELD
1	SET	W	0h	Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable [IERn] and status [IPRn]. CPU write of '0' has no effect.
0	EVAL	W	0h	Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts [IERn] are still pending [IPRn]. CPU write of '0' has no effect..

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4.4.2.72 TPCC_QER Register

4.4.2.72.1 TPCC_QER Register (Offset = 1080h) [reset = 0h]

QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

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Table 4-2178. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1080h

Figure 4-1065. TPCC_QER Name Register

31	30	29	28	27	26	25	24
RES70							
R							
0h							
23	22	21	20	19	18	17	16
RES70							
R							
0h							
15	14	13	12	11	10	9	8
RES70							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2179. TPCC_QER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES70	R	0h	RESERVE FIELD
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.73 TPCC_QEER Register

4.4.2.73.1 TPCC_QEER Register (Offset = 1084h) [reset = 0h]

QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

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Table 4-2180. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1084h

Figure 4-1066. TPCC_QEER Name Register

31	30	29	28	27	26	25	24
RES71							
R							
0h							
23	22	21	20	19	18	17	16
RES71							
R							
0h							
15	14	13	12	11	10	9	8
RES71							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2181. TPCC_QEER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES71	R	0h	RESERVE FIELD
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.74 TPCC_QEECR Register

4.4.2.74.1 TPCC_QEECR Register (Offset = 1088h) [reset = 0h]

QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

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Table 4-2182. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1088h

Figure 4-1067. TPCC_QEECR Name Register

31	30	29	28	27	26	25	24
RES72							
R							
0h							
23	22	21	20	19	18	17	16
RES72							
R							
0h							
15	14	13	12	11	10	9	8
RES72							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2183. TPCC_QEECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES72	R	0h	RESERVE FIELD
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.75 TPCC_QEESR Register

4.4.2.75.1 TPCC_QEESR Register (Offset = 108Ch) [reset = 0h]

QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

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Table 4-2184. Instance Table

Instance Name	Physical Address
EDMA0	52A0 108Ch

Figure 4-1068. TPCC_QEESR Name Register

31	30	29	28	27	26	25	24
RES73							
R							
0h							
23	22	21	20	19	18	17	16
RES73							
R							
0h							
15	14	13	12	11	10	9	8
RES73							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2185. TPCC_QEESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES73	R	0h	RESERVE FIELD
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.76 TPCC_QSER Register

4.4.2.76.1 TPCC_QSER Register (Offset = 1090h) [reset = 0h]

QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

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Table 4-2186. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1090h

Figure 4-1069. TPCC_QSER Name Register

31	30	29	28	27	26	25	24
RES74							
R							
0h							
23	22	21	20	19	18	17	16
RES74							
R							
0h							
15	14	13	12	11	10	9	8
RES74							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2187. TPCC_QSER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES74	R	0h	RESERVE FIELD
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.77 TPCC_QSECR Register

4.4.2.77.1 TPCC_QSECR Register (Offset = 1094h) [reset = 0h]

QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

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Table 4-2188. Instance Table

Instance Name	Physical Address
EDMA0	52A0 1094h

Figure 4-1070. TPCC_QSECR Name Register

31	30	29	28	27	26	25	24
RES75							
R							
0h							
23	22	21	20	19	18	17	16
RES75							
R							
0h							
15	14	13	12	11	10	9	8
RES75							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2189. TPCC_QSECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES75	R	0h	RESERVE FIELD
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.78 TPCC_ER_RN Register

4.4.2.78.1 TPCC_ER_RN Register (Offset = 2000h) [reset = 0h]

Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

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Table 4-2190. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2000h

Figure 4-1071. TPCC_ER_RN Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2191. TPCC_ER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31
30	E30	R	0h	Event #30
29	E29	R	0h	Event #29
28	E28	R	0h	Event #28
27	E27	R	0h	Event #27
26	E26	R	0h	Event #26
25	E25	R	0h	Event #25
24	E24	R	0h	Event #24
23	E23	R	0h	Event #23
22	E22	R	0h	Event #22
21	E21	R	0h	Event #21
20	E20	R	0h	Event #20
19	E19	R	0h	Event #19
18	E18	R	0h	Event #18

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Table 4-2191. TPCC_ER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	E17	R	0h	Event #17
16	E16	R	0h	Event #16
15	E15	R	0h	Event #15
14	E14	R	0h	Event #14
13	E13	R	0h	Event #13
12	E12	R	0h	Event #12
11	E11	R	0h	Event #11
10	E10	R	0h	Event #10
9	E9	R	0h	Event #9
8	E8	R	0h	Event #8
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.79 TPCC_ERH_RN Register

4.4.2.79.1 TPCC_ERH_RN Register (Offset = 2004h) [reset = 0h]

Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

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Table 4-2192. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2004h

Figure 4-1072. TPCC_ERH_RN Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2193. TPCC_ERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63
30	E62	R	0h	Event #62
29	E61	R	0h	Event #61
28	E60	R	0h	Event #60
27	E59	R	0h	Event #59
26	E58	R	0h	Event #58
25	E57	R	0h	Event #57
24	E56	R	0h	Event #56
23	E55	R	0h	Event #55
22	E54	R	0h	Event #54
21	E53	R	0h	Event #53
20	E52	R	0h	Event #52
19	E51	R	0h	Event #51
18	E50	R	0h	Event #50

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Table 4-2193. TPCC_ERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	E49	R	0h	Event #49
16	E48	R	0h	Event #48
15	E47	R	0h	Event #47
14	E46	R	0h	Event #46
13	E45	R	0h	Event #45
12	E44	R	0h	Event #44
11	E43	R	0h	Event #43
10	E42	R	0h	Event #42
9	E41	R	0h	Event #41
8	E40	R	0h	Event #40
7	E39	R	0h	Event #39
6	E38	R	0h	Event #38
5	E37	R	0h	Event #37
4	E36	R	0h	Event #36
3	E35	R	0h	Event #35
2	E34	R	0h	Event #34
1	E33	R	0h	Event #33
0	E32	R	0h	Event #32

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4.4.2.80 TPCC_ECR_RN Register

4.4.2.80.1 TPCC_ECR_RN Register (Offset = 2008h) [reset = 0h]

Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

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Table 4-2194. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2008h

Figure 4-1073. TPCC_ECR_RN Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2195. TPCC_ECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31
30	E30	W	0h	Event #30
29	E29	W	0h	Event #29
28	E28	W	0h	Event #28
27	E27	W	0h	Event #27
26	E26	W	0h	Event #26
25	E25	W	0h	Event #25
24	E24	W	0h	Event #24
23	E23	W	0h	Event #23
22	E22	W	0h	Event #22
21	E21	W	0h	Event #21
20	E20	W	0h	Event #20
19	E19	W	0h	Event #19
18	E18	W	0h	Event #18
17	E17	W	0h	Event #17
16	E16	W	0h	Event #16
15	E15	W	0h	Event #15
14	E14	W	0h	Event #14
13	E13	W	0h	Event #13

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Table 4-2195. TPCC_ECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event #12
11	E11	W	0h	Event #11
10	E10	W	0h	Event #10
9	E9	W	0h	Event #9
8	E8	W	0h	Event #8
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.81 TPCC_ECRH_RN Register

4.4.2.81.1 TPCC_ECRH_RN Register (Offset = 200Ch) [reset = 0h]

Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

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Table 4-2196. Instance Table

Instance Name	Physical Address
EDMA0	52A0 200Ch

Figure 4-1074. TPCC_ECRH_RN Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2197. TPCC_ECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63
30	E62	W	0h	Event #62
29	E61	W	0h	Event #61
28	E60	W	0h	Event #60
27	E59	W	0h	Event #59
26	E58	W	0h	Event #58
25	E57	W	0h	Event #57
24	E56	W	0h	Event #56
23	E55	W	0h	Event #55
22	E54	W	0h	Event #54
21	E53	W	0h	Event #53
20	E52	W	0h	Event #52
19	E51	W	0h	Event #51
18	E50	W	0h	Event #50
17	E49	W	0h	Event #49
16	E48	W	0h	Event #48
15	E47	W	0h	Event #47
14	E46	W	0h	Event #46
13	E45	W	0h	Event #45

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Table 4-2197. TPCC_ECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	W	0h	Event #44
11	E43	W	0h	Event #43
10	E42	W	0h	Event #42
9	E41	W	0h	Event #41
8	E40	W	0h	Event #40
7	E39	W	0h	Event #39
6	E38	W	0h	Event #38
5	E37	W	0h	Event #37
4	E36	W	0h	Event #36
3	E35	W	0h	Event #35
2	E34	W	0h	Event #34
1	E33	W	0h	Event #33
0	E32	W	0h	Event #32

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4.4.2.82 TPCC_ESR_RN Register

4.4.2.82.1 TPCC_ESR_RN Register (Offset = 2010h) [reset = 0h]

Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

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Table 4-2198. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2010h

Figure 4-1075. TPCC_ESR_RN Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2199. TPCC_ESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31
30	E30	W	0h	Event #30
29	E29	W	0h	Event #29
28	E28	W	0h	Event #28
27	E27	W	0h	Event #27
26	E26	W	0h	Event #26
25	E25	W	0h	Event #25
24	E24	W	0h	Event #24
23	E23	W	0h	Event #23
22	E22	W	0h	Event #22
21	E21	W	0h	Event #21
20	E20	W	0h	Event #20
19	E19	W	0h	Event #19
18	E18	W	0h	Event #18
17	E17	W	0h	Event #17
16	E16	W	0h	Event #16
15	E15	W	0h	Event #15
14	E14	W	0h	Event #14
13	E13	W	0h	Event #13

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Table 4-2199. TPCC_ESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event #12
11	E11	W	0h	Event #11
10	E10	W	0h	Event #10
9	E9	W	0h	Event #9
8	E8	W	0h	Event #8
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.83 TPCC_ESRH_RN Register

4.4.2.83.1 TPCC_ESRH_RN Register (Offset = 2014h) [reset = 0h]

Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

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Table 4-2200. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2014h

Figure 4-1076. TPCC_ESRH_RN Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2201. TPCC_ESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63
30	E62	W	0h	Event #62
29	E61	W	0h	Event #61
28	E60	W	0h	Event #60
27	E59	W	0h	Event #59
26	E58	W	0h	Event #58
25	E57	W	0h	Event #57
24	E56	W	0h	Event #56
23	E55	W	0h	Event #55
22	E54	W	0h	Event #54
21	E53	W	0h	Event #53
20	E52	W	0h	Event #52
19	E51	W	0h	Event #51
18	E50	W	0h	Event #50
17	E49	W	0h	Event #49
16	E48	W	0h	Event #48
15	E47	W	0h	Event #47
14	E46	W	0h	Event #46
13	E45	W	0h	Event #45

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Table 4-2201. TPCC_ESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	W	0h	Event #44
11	E43	W	0h	Event #43
10	E42	W	0h	Event #42
9	E41	W	0h	Event #41
8	E40	W	0h	Event #40
7	E39	W	0h	Event #39
6	E38	W	0h	Event #38
5	E37	W	0h	Event #37
4	E36	W	0h	Event #36
3	E35	W	0h	Event #35
2	E34	W	0h	Event #34
1	E33	W	0h	Event #33
0	E32	W	0h	Event #32

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4.4.2.84 TPCC_CER_RN Register

4.4.2.84.1 TPCC_CER_RN Register (Offset = 2018h) [reset = 0h]

Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

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Table 4-2202. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2018h

Figure 4-1077. TPCC_CER_RN Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2203. TPCC_CER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31
30	E30	R	0h	Event #30
29	E29	R	0h	Event #29
28	E28	R	0h	Event #28
27	E27	R	0h	Event #27
26	E26	R	0h	Event #26
25	E25	R	0h	Event #25
24	E24	R	0h	Event #24
23	E23	R	0h	Event #23
22	E22	R	0h	Event #22
21	E21	R	0h	Event #21
20	E20	R	0h	Event #20
19	E19	R	0h	Event #19
18	E18	R	0h	Event #18
17	E17	R	0h	Event #17

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Table 4-2203. TPCC_CER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	E16	R	0h	Event #16
15	E15	R	0h	Event #15
14	E14	R	0h	Event #14
13	E13	R	0h	Event #13
12	E12	R	0h	Event #12
11	E11	R	0h	Event #11
10	E10	R	0h	Event #10
9	E9	R	0h	Event #9
8	E8	R	0h	Event #8
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.85 TPCC_CERH_RN Register

4.4.2.85.1 TPCC_CERH_RN Register (Offset = 201Ch) [reset = 0h]

Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

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Table 4-2204. Instance Table

Instance Name	Physical Address
EDMA0	52A0 201Ch

Figure 4-1078. TPCC_CERH_RN Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2205. TPCC_CERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63
30	E62	R	0h	Event #62
29	E61	R	0h	Event #61
28	E60	R	0h	Event #60
27	E59	R	0h	Event #59
26	E58	R	0h	Event #58
25	E57	R	0h	Event #57
24	E56	R	0h	Event #56
23	E55	R	0h	Event #55
22	E54	R	0h	Event #54
21	E53	R	0h	Event #53
20	E52	R	0h	Event #52
19	E51	R	0h	Event #51
18	E50	R	0h	Event #50

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Table 4-2205. TPCC_CERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	E49	R	0h	Event #49
16	E48	R	0h	Event #48
15	E47	R	0h	Event #47
14	E46	R	0h	Event #46
13	E45	R	0h	Event #45
12	E44	R	0h	Event #44
11	E43	R	0h	Event #43
10	E42	R	0h	Event #42
9	E41	R	0h	Event #41
8	E40	R	0h	Event #40
7	E39	R	0h	Event #39
6	E38	R	0h	Event #38
5	E37	R	0h	Event #37
4	E36	R	0h	Event #36
3	E35	R	0h	Event #35
2	E34	R	0h	Event #34
1	E33	R	0h	Event #33
0	E32	R	0h	Event #32

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4.4.2.86 TPCC_EER_RN Register

4.4.2.86.1 TPCC_EER_RN Register (Offset = 2020h) [reset = 0h]

Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

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Table 4-2206. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2020h

Figure 4-1079. TPCC_EER_RN Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2207. TPCC_EER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31
30	E30	R	0h	Event #30
29	E29	R	0h	Event #29
28	E28	R	0h	Event #28
27	E27	R	0h	Event #27
26	E26	R	0h	Event #26
25	E25	R	0h	Event #25
24	E24	R	0h	Event #24
23	E23	R	0h	Event #23
22	E22	R	0h	Event #22
21	E21	R	0h	Event #21
20	E20	R	0h	Event #20
19	E19	R	0h	Event #19
18	E18	R	0h	Event #18

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Table 4-2207. TPCC_EER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	E17	R	0h	Event #17
16	E16	R	0h	Event #16
15	E15	R	0h	Event #15
14	E14	R	0h	Event #14
13	E13	R	0h	Event #13
12	E12	R	0h	Event #12
11	E11	R	0h	Event #11
10	E10	R	0h	Event #10
9	E9	R	0h	Event #9
8	E8	R	0h	Event #8
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.87 TPCC_EERH_RN Register

4.4.2.87.1 TPCC_EERH_RN Register (Offset = 2024h) [reset = 0h]

Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

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Table 4-2208. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2024h

Figure 4-1080. TPCC_EERH_RN Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2209. TPCC_EERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63
30	E62	R	0h	Event #62
29	E61	R	0h	Event #61
28	E60	R	0h	Event #60
27	E59	R	0h	Event #59
26	E58	R	0h	Event #58
25	E57	R	0h	Event #57
24	E56	R	0h	Event #56
23	E55	R	0h	Event #55
22	E54	R	0h	Event #54
21	E53	R	0h	Event #53
20	E52	R	0h	Event #52
19	E51	R	0h	Event #51
18	E50	R	0h	Event #50

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Table 4-2209. TPCC_EERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	E49	R	0h	Event #49
16	E48	R	0h	Event #48
15	E47	R	0h	Event #47
14	E46	R	0h	Event #46
13	E45	R	0h	Event #45
12	E44	R	0h	Event #44
11	E43	R	0h	Event #43
10	E42	R	0h	Event #42
9	E41	R	0h	Event #41
8	E40	R	0h	Event #40
7	E39	R	0h	Event #39
6	E38	R	0h	Event #38
5	E37	R	0h	Event #37
4	E36	R	0h	Event #36
3	E35	R	0h	Event #35
2	E34	R	0h	Event #34
1	E33	R	0h	Event #33
0	E32	R	0h	Event #32

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4.4.2.88 TPCC_EECR_RN Register

4.4.2.88.1 TPCC_EECR_RN Register (Offset = 2028h) [reset = 0h]

Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

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Table 4-2210. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2028h

Figure 4-1081. TPCC_EECR_RN Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2211. TPCC_EECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31
30	E30	W	0h	Event #30
29	E29	W	0h	Event #29
28	E28	W	0h	Event #28
27	E27	W	0h	Event #27
26	E26	W	0h	Event #26
25	E25	W	0h	Event #25
24	E24	W	0h	Event #24
23	E23	W	0h	Event #23
22	E22	W	0h	Event #22
21	E21	W	0h	Event #21
20	E20	W	0h	Event #20
19	E19	W	0h	Event #19
18	E18	W	0h	Event #18
17	E17	W	0h	Event #17
16	E16	W	0h	Event #16
15	E15	W	0h	Event #15
14	E14	W	0h	Event #14
13	E13	W	0h	Event #13

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Table 4-2211. TPCC_EECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event #12
11	E11	W	0h	Event #11
10	E10	W	0h	Event #10
9	E9	W	0h	Event #9
8	E8	W	0h	Event #8
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.89 TPCC_EECRH_RN Register

4.4.2.89.1 TPCC_EECRH_RN Register (Offset = 202Ch) [reset = 0h]

Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

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Table 4-2212. Instance Table

Instance Name	Physical Address
EDMA0	52A0 202Ch

Figure 4-1082. TPCC_EECRH_RN Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2213. TPCC_EECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63
30	E62	W	0h	Event #62
29	E61	W	0h	Event #61
28	E60	W	0h	Event #60
27	E59	W	0h	Event #59
26	E58	W	0h	Event #58
25	E57	W	0h	Event #57
24	E56	W	0h	Event #56
23	E55	W	0h	Event #55
22	E54	W	0h	Event #54
21	E53	W	0h	Event #53
20	E52	W	0h	Event #52
19	E51	W	0h	Event #51
18	E50	W	0h	Event #50
17	E49	W	0h	Event #49
16	E48	W	0h	Event #48
15	E47	W	0h	Event #47
14	E46	W	0h	Event #46
13	E45	W	0h	Event #45

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Table 4-2213. TPCC_EECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	W	0h	Event #44
11	E43	W	0h	Event #43
10	E42	W	0h	Event #42
9	E41	W	0h	Event #41
8	E40	W	0h	Event #40
7	E39	W	0h	Event #39
6	E38	W	0h	Event #38
5	E37	W	0h	Event #37
4	E36	W	0h	Event #36
3	E35	W	0h	Event #35
2	E34	W	0h	Event #34
1	E33	W	0h	Event #33
0	E32	W	0h	Event #32

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4.4.2.90 TPCC_EESR_RN Register

4.4.2.90.1 TPCC_EESR_RN Register (Offset = 2030h) [reset = 0h]

Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

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Table 4-2214. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2030h

Figure 4-1083. TPCC_EESR_RN Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2215. TPCC_EESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31
30	E30	W	0h	Event #30
29	E29	W	0h	Event #29
28	E28	W	0h	Event #28
27	E27	W	0h	Event #27
26	E26	W	0h	Event #26
25	E25	W	0h	Event #25
24	E24	W	0h	Event #24
23	E23	W	0h	Event #23
22	E22	W	0h	Event #22
21	E21	W	0h	Event #21
20	E20	W	0h	Event #20
19	E19	W	0h	Event #19
18	E18	W	0h	Event #18
17	E17	W	0h	Event #17
16	E16	W	0h	Event #16
15	E15	W	0h	Event #15
14	E14	W	0h	Event #14
13	E13	W	0h	Event #13

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Table 4-2215. TPCC_EESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event #12
11	E11	W	0h	Event #11
10	E10	W	0h	Event #10
9	E9	W	0h	Event #9
8	E8	W	0h	Event #8
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.91 TPCC_EESRH_RN Register

4.4.2.91.1 TPCC_EESRH_RN Register (Offset = 2034h) [reset = 0h]

Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

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Table 4-2216. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2034h

Figure 4-1084. TPCC_EESRH_RN Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2217. TPCC_EESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63
30	E62	W	0h	Event #62
29	E61	W	0h	Event #61
28	E60	W	0h	Event #60
27	E59	W	0h	Event #59
26	E58	W	0h	Event #58
25	E57	W	0h	Event #57
24	E56	W	0h	Event #56
23	E55	W	0h	Event #55
22	E54	W	0h	Event #54
21	E53	W	0h	Event #53
20	E52	W	0h	Event #52
19	E51	W	0h	Event #51
18	E50	W	0h	Event #50
17	E49	W	0h	Event #49
16	E48	W	0h	Event #48
15	E47	W	0h	Event #47
14	E46	W	0h	Event #46
13	E45	W	0h	Event #45

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Table 4-2217. TPCC_EESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	W	0h	Event #44
11	E43	W	0h	Event #43
10	E42	W	0h	Event #42
9	E41	W	0h	Event #41
8	E40	W	0h	Event #40
7	E39	W	0h	Event #39
6	E38	W	0h	Event #38
5	E37	W	0h	Event #37
4	E36	W	0h	Event #36
3	E35	W	0h	Event #35
2	E34	W	0h	Event #34
1	E33	W	0h	Event #33
0	E32	W	0h	Event #32

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4.4.2.92 TPCC_SER_RN Register

4.4.2.92.1 TPCC_SER_RN Register (Offset = 2038h) [reset = 0h]

Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

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Table 4-2218. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2038h

Figure 4-1085. TPCC_SER_RN Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2219. TPCC_SER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	R	0h	Event #31
30	E30	R	0h	Event #30
29	E29	R	0h	Event #29
28	E28	R	0h	Event #28
27	E27	R	0h	Event #27
26	E26	R	0h	Event #26
25	E25	R	0h	Event #25
24	E24	R	0h	Event #24
23	E23	R	0h	Event #23
22	E22	R	0h	Event #22
21	E21	R	0h	Event #21
20	E20	R	0h	Event #20
19	E19	R	0h	Event #19
18	E18	R	0h	Event #18
17	E17	R	0h	Event #17
16	E16	R	0h	Event #16
15	E15	R	0h	Event #15
14	E14	R	0h	Event #14

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Table 4-2219. TPCC_SER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	E13	R	0h	Event #13
12	E12	R	0h	Event #12
11	E11	R	0h	Event #11
10	E10	R	0h	Event #10
9	E9	R	0h	Event #9
8	E8	R	0h	Event #8
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.93 TPCC_SERH_RN Register

4.4.2.93.1 TPCC_SERH_RN Register (Offset = 203Ch) [reset = 0h]

Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

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Table 4-2220. Instance Table

Instance Name	Physical Address
EDMA0	52A0 203Ch

Figure 4-1086. TPCC_SERH_RN Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2221. TPCC_SERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	R	0h	Event #63
30	E62	R	0h	Event #62
29	E61	R	0h	Event #61
28	E60	R	0h	Event #60
27	E59	R	0h	Event #59
26	E58	R	0h	Event #58
25	E57	R	0h	Event #57
24	E56	R	0h	Event #56
23	E55	R	0h	Event #55
22	E54	R	0h	Event #54
21	E53	R	0h	Event #53
20	E52	R	0h	Event #52
19	E51	R	0h	Event #51
18	E50	R	0h	Event #50
17	E49	R	0h	Event #49
16	E48	R	0h	Event #48
15	E47	R	0h	Event #47
14	E46	R	0h	Event #46

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Table 4-2221. TPCC_SERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	E45	R	0h	Event #45
12	E44	R	0h	Event #44
11	E43	R	0h	Event #43
10	E42	R	0h	Event #42
9	E41	R	0h	Event #41
8	E40	R	0h	Event #40
7	E39	R	0h	Event #39
6	E38	R	0h	Event #38
5	E37	R	0h	Event #37
4	E36	R	0h	Event #36
3	E35	R	0h	Event #35
2	E34	R	0h	Event #34
1	E33	R	0h	Event #33
0	E32	R	0h	Event #32

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4.4.2.94 TPCC_SECR_RN Register

4.4.2.94.1 TPCC_SECR_RN Register (Offset = 2040h) [reset = 0h]

Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

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Table 4-2222. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2040h

Figure 4-1087. TPCC_SECR_RN Name Register

31	30	29	28	27	26	25	24
E31	E30	E29	E28	E27	E26	E25	E24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E15	E14	E13	E12	E11	E10	E9	E8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2223. TPCC_SECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	W	0h	Event #31
30	E30	W	0h	Event #30
29	E29	W	0h	Event #29
28	E28	W	0h	Event #28
27	E27	W	0h	Event #27
26	E26	W	0h	Event #26
25	E25	W	0h	Event #25
24	E24	W	0h	Event #24
23	E23	W	0h	Event #23
22	E22	W	0h	Event #22
21	E21	W	0h	Event #21
20	E20	W	0h	Event #20
19	E19	W	0h	Event #19
18	E18	W	0h	Event #18
17	E17	W	0h	Event #17
16	E16	W	0h	Event #16
15	E15	W	0h	Event #15
14	E14	W	0h	Event #14
13	E13	W	0h	Event #13

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Table 4-2223. TPCC_SECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E12	W	0h	Event #12
11	E11	W	0h	Event #11
10	E10	W	0h	Event #10
9	E9	W	0h	Event #9
8	E8	W	0h	Event #8
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.95 TPCC_SECRH_RN Register

4.4.2.95.1 TPCC_SECRH_RN Register (Offset = 2044h) [reset = 0h]

Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

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Table 4-2224. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2044h

Figure 4-1088. TPCC_SECRH_RN Name Register

31	30	29	28	27	26	25	24
E63	E62	E61	E60	E59	E58	E57	E56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
E55	E54	E53	E52	E51	E50	E49	E48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
E47	E46	E45	E44	E43	E42	E41	E40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
E39	E38	E37	E36	E35	E34	E33	E32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2225. TPCC_SECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	W	0h	Event #63
30	E62	W	0h	Event #62
29	E61	W	0h	Event #61
28	E60	W	0h	Event #60
27	E59	W	0h	Event #59
26	E58	W	0h	Event #58
25	E57	W	0h	Event #57
24	E56	W	0h	Event #56
23	E55	W	0h	Event #55
22	E54	W	0h	Event #54
21	E53	W	0h	Event #53
20	E52	W	0h	Event #52
19	E51	W	0h	Event #51
18	E50	W	0h	Event #50
17	E49	W	0h	Event #49
16	E48	W	0h	Event #48
15	E47	W	0h	Event #47
14	E46	W	0h	Event #46
13	E45	W	0h	Event #45

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Table 4-2225. TPCC_SECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	E44	W	0h	Event #44
11	E43	W	0h	Event #43
10	E42	W	0h	Event #42
9	E41	W	0h	Event #41
8	E40	W	0h	Event #40
7	E39	W	0h	Event #39
6	E38	W	0h	Event #38
5	E37	W	0h	Event #37
4	E36	W	0h	Event #36
3	E35	W	0h	Event #35
2	E34	W	0h	Event #34
1	E33	W	0h	Event #33
0	E32	W	0h	Event #32

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4.4.2.96 TPCC_IER_RN Register

4.4.2.96.1 TPCC_IER_RN Register (Offset = 2050h) [reset = 0h]

Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

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Table 4-2226. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2050h

Figure 4-1089. TPCC_IER_RN Name Register

31	30	29	28	27	26	25	24
I31	I30	I29	I28	I27	I26	I25	I24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I23	I22	I21	I20	I19	I18	I17	I16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I15	I14	I13	I12	I11	I10	I9	I8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2227. TPCC_IER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	R	0h	Interrupt associated with TCC #31
30	I30	R	0h	Interrupt associated with TCC #30
29	I29	R	0h	Interrupt associated with TCC #29
28	I28	R	0h	Interrupt associated with TCC #28
27	I27	R	0h	Interrupt associated with TCC #27
26	I26	R	0h	Interrupt associated with TCC #26
25	I25	R	0h	Interrupt associated with TCC #25
24	I24	R	0h	Interrupt associated with TCC #24
23	I23	R	0h	Interrupt associated with TCC #23
22	I22	R	0h	Interrupt associated with TCC #22
21	I21	R	0h	Interrupt associated with TCC #21
20	I20	R	0h	Interrupt associated with TCC #20
19	I19	R	0h	Interrupt associated with TCC #19
18	I18	R	0h	Interrupt associated with TCC #18
17	I17	R	0h	Interrupt associated with TCC #17
16	I16	R	0h	Interrupt associated with TCC #16
15	I15	R	0h	Interrupt associated with TCC #15
14	I14	R	0h	Interrupt associated with TCC #14

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Table 4-2227. TPCC_IER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	I13	R	0h	Interrupt associated with TCC #13
12	I12	R	0h	Interrupt associated with TCC #12
11	I11	R	0h	Interrupt associated with TCC #11
10	I10	R	0h	Interrupt associated with TCC #10
9	I9	R	0h	Interrupt associated with TCC #9
8	I8	R	0h	Interrupt associated with TCC #8
7	I7	R	0h	Interrupt associated with TCC #7
6	I6	R	0h	Interrupt associated with TCC #6
5	I5	R	0h	Interrupt associated with TCC #5
4	I4	R	0h	Interrupt associated with TCC #4
3	I3	R	0h	Interrupt associated with TCC #3
2	I2	R	0h	Interrupt associated with TCC #2
1	I1	R	0h	Interrupt associated with TCC #1
0	I0	R	0h	Interrupt associated with TCC #0

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4.4.2.97 TPCC_IERH_RN Register

4.4.2.97.1 TPCC_IERH_RN Register (Offset = 2054h) [reset = 0h]

Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

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Table 4-2228. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2054h

Figure 4-1090. TPCC_IERH_RN Name Register

31	30	29	28	27	26	25	24
I63	I62	I61	I60	I59	I58	I57	I56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I55	I54	I53	I52	I51	I50	I49	I48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I47	I46	I45	I44	I43	I42	I41	I40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I39	I38	I37	I36	I35	I34	I33	I32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2229. TPCC_IERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	R	0h	Interrupt associated with TCC #63
30	I62	R	0h	Interrupt associated with TCC #62
29	I61	R	0h	Interrupt associated with TCC #61
28	I60	R	0h	Interrupt associated with TCC #60
27	I59	R	0h	Interrupt associated with TCC #59
26	I58	R	0h	Interrupt associated with TCC #58
25	I57	R	0h	Interrupt associated with TCC #57
24	I56	R	0h	Interrupt associated with TCC #56
23	I55	R	0h	Interrupt associated with TCC #55
22	I54	R	0h	Interrupt associated with TCC #54
21	I53	R	0h	Interrupt associated with TCC #53
20	I52	R	0h	Interrupt associated with TCC #52
19	I51	R	0h	Interrupt associated with TCC #51
18	I50	R	0h	Interrupt associated with TCC #50
17	I49	R	0h	Interrupt associated with TCC #49
16	I48	R	0h	Interrupt associated with TCC #48
15	I47	R	0h	Interrupt associated with TCC #47
14	I46	R	0h	Interrupt associated with TCC #46

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Table 4-2229. TPCC_IERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	I45	R	0h	Interrupt associated with TCC #45
12	I44	R	0h	Interrupt associated with TCC #44
11	I43	R	0h	Interrupt associated with TCC #43
10	I42	R	0h	Interrupt associated with TCC #42
9	I41	R	0h	Interrupt associated with TCC #41
8	I40	R	0h	Interrupt associated with TCC #40
7	I39	R	0h	Interrupt associated with TCC #39
6	I38	R	0h	Interrupt associated with TCC #38
5	I37	R	0h	Interrupt associated with TCC #37
4	I36	R	0h	Interrupt associated with TCC #36
3	I35	R	0h	Interrupt associated with TCC #35
2	I34	R	0h	Interrupt associated with TCC #34
1	I33	R	0h	Interrupt associated with TCC #33
0	I32	R	0h	Interrupt associated with TCC #32

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4.4.2.98 TPCC_IECR_RN Register

4.4.2.98.1 TPCC_IECR_RN Register (Offset = 2058h) [reset = 0h]

Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

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Table 4-2230. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2058h

Figure 4-1091. TPCC_IECR_RN Name Register

31	30	29	28	27	26	25	24
I31	I30	I29	I28	I27	I26	I25	I24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I15	I14	I13	I12	I11	I10	I9	I8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2231. TPCC_IECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31
30	I30	W	0h	Interrupt associated with TCC #30
29	I29	W	0h	Interrupt associated with TCC #29
28	I28	W	0h	Interrupt associated with TCC #28
27	I27	W	0h	Interrupt associated with TCC #27
26	I26	W	0h	Interrupt associated with TCC #26
25	I25	W	0h	Interrupt associated with TCC #25
24	I24	W	0h	Interrupt associated with TCC #24
23	I23	W	0h	Interrupt associated with TCC #23
22	I22	W	0h	Interrupt associated with TCC #22
21	I21	W	0h	Interrupt associated with TCC #21
20	I20	W	0h	Interrupt associated with TCC #20
19	I19	W	0h	Interrupt associated with TCC #19
18	I18	W	0h	Interrupt associated with TCC #18
17	I17	W	0h	Interrupt associated with TCC #17
16	I16	W	0h	Interrupt associated with TCC #16
15	I15	W	0h	Interrupt associated with TCC #15
14	I14	W	0h	Interrupt associated with TCC #14
13	I13	W	0h	Interrupt associated with TCC #13

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Table 4-2231. TPCC_IECR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I12	W	0h	Interrupt associated with TCC #12
11	I11	W	0h	Interrupt associated with TCC #11
10	I10	W	0h	Interrupt associated with TCC #10
9	I9	W	0h	Interrupt associated with TCC #9
8	I8	W	0h	Interrupt associated with TCC #8
7	I7	W	0h	Interrupt associated with TCC #7
6	I6	W	0h	Interrupt associated with TCC #6
5	I5	W	0h	Interrupt associated with TCC #5
4	I4	W	0h	Interrupt associated with TCC #4
3	I3	W	0h	Interrupt associated with TCC #3
2	I2	W	0h	Interrupt associated with TCC #2
1	I1	W	0h	Interrupt associated with TCC #1
0	I0	W	0h	Interrupt associated with TCC #0

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4.4.2.99 TPCC_IECRH_RN Register

4.4.2.99.1 TPCC_IECRH_RN Register (Offset = 205Ch) [reset = 0h]

Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Return to Summary Table

Table 4-2232. Instance Table

Instance Name	Physical Address
EDMA0	52A0 205Ch

Figure 4-1092. TPCC_IECRH_RN Name Register

31	30	29	28	27	26	25	24
I63	I62	I61	I60	I59	I58	I57	I56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I47	I46	I45	I44	I43	I42	I41	I40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2233. TPCC_IECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63
30	I62	W	0h	Interrupt associated with TCC #62
29	I61	W	0h	Interrupt associated with TCC #61
28	I60	W	0h	Interrupt associated with TCC #60
27	I59	W	0h	Interrupt associated with TCC #59
26	I58	W	0h	Interrupt associated with TCC #58
25	I57	W	0h	Interrupt associated with TCC #57
24	I56	W	0h	Interrupt associated with TCC #56
23	I55	W	0h	Interrupt associated with TCC #55
22	I54	W	0h	Interrupt associated with TCC #54
21	I53	W	0h	Interrupt associated with TCC #53
20	I52	W	0h	Interrupt associated with TCC #52
19	I51	W	0h	Interrupt associated with TCC #51
18	I50	W	0h	Interrupt associated with TCC #50
17	I49	W	0h	Interrupt associated with TCC #49
16	I48	W	0h	Interrupt associated with TCC #48
15	I47	W	0h	Interrupt associated with TCC #47
14	I46	W	0h	Interrupt associated with TCC #46
13	I45	W	0h	Interrupt associated with TCC #45

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Table 4-2233. TPCC_IECRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I44	W	0h	Interrupt associated with TCC #44
11	I43	W	0h	Interrupt associated with TCC #43
10	I42	W	0h	Interrupt associated with TCC #42
9	I41	W	0h	Interrupt associated with TCC #41
8	I40	W	0h	Interrupt associated with TCC #40
7	I39	W	0h	Interrupt associated with TCC #39
6	I38	W	0h	Interrupt associated with TCC #38
5	I37	W	0h	Interrupt associated with TCC #37
4	I36	W	0h	Interrupt associated with TCC #36
3	I35	W	0h	Interrupt associated with TCC #35
2	I34	W	0h	Interrupt associated with TCC #34
1	I33	W	0h	Interrupt associated with TCC #33
0	I32	W	0h	Interrupt associated with TCC #32

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4.4.2.100 TPCC_IESR_RN Register

4.4.2.100.1 TPCC_IESR_RN Register (Offset = 2060h) [reset = 0h]

Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Return to Summary Table

Table 4-2234. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2060h

Figure 4-1093. TPCC_IESR_RN Name Register

31	30	29	28	27	26	25	24
I31	I30	I29	I28	I27	I26	I25	I24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I15	I14	I13	I12	I11	I10	I9	I8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2235. TPCC_IESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31
30	I30	W	0h	Interrupt associated with TCC #30
29	I29	W	0h	Interrupt associated with TCC #29
28	I28	W	0h	Interrupt associated with TCC #28
27	I27	W	0h	Interrupt associated with TCC #27
26	I26	W	0h	Interrupt associated with TCC #26
25	I25	W	0h	Interrupt associated with TCC #25
24	I24	W	0h	Interrupt associated with TCC #24
23	I23	W	0h	Interrupt associated with TCC #23
22	I22	W	0h	Interrupt associated with TCC #22
21	I21	W	0h	Interrupt associated with TCC #21
20	I20	W	0h	Interrupt associated with TCC #20
19	I19	W	0h	Interrupt associated with TCC #19
18	I18	W	0h	Interrupt associated with TCC #18
17	I17	W	0h	Interrupt associated with TCC #17
16	I16	W	0h	Interrupt associated with TCC #16
15	I15	W	0h	Interrupt associated with TCC #15
14	I14	W	0h	Interrupt associated with TCC #14
13	I13	W	0h	Interrupt associated with TCC #13

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Table 4-2235. TPCC_IESR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I12	W	0h	Interrupt associated with TCC #12
11	I11	W	0h	Interrupt associated with TCC #11
10	I10	W	0h	Interrupt associated with TCC #10
9	I9	W	0h	Interrupt associated with TCC #9
8	I8	W	0h	Interrupt associated with TCC #8
7	I7	W	0h	Interrupt associated with TCC #7
6	I6	W	0h	Interrupt associated with TCC #6
5	I5	W	0h	Interrupt associated with TCC #5
4	I4	W	0h	Interrupt associated with TCC #4
3	I3	W	0h	Interrupt associated with TCC #3
2	I2	W	0h	Interrupt associated with TCC #2
1	I1	W	0h	Interrupt associated with TCC #1
0	I0	W	0h	Interrupt associated with TCC #0

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4.4.2.101 TPCC_IESRH_RN Register

4.4.2.101.1 TPCC_IESRH_RN Register (Offset = 2064h) [reset = 0h]

Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

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Table 4-2236. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2064h

Figure 4-1094. TPCC_IESRH_RN Name Register

31	30	29	28	27	26	25	24
I63	I62	I61	I60	I59	I58	I57	I56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I47	I46	I45	I44	I43	I42	I41	I40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2237. TPCC_IESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63
30	I62	W	0h	Interrupt associated with TCC #62
29	I61	W	0h	Interrupt associated with TCC #61
28	I60	W	0h	Interrupt associated with TCC #60
27	I59	W	0h	Interrupt associated with TCC #59
26	I58	W	0h	Interrupt associated with TCC #58
25	I57	W	0h	Interrupt associated with TCC #57
24	I56	W	0h	Interrupt associated with TCC #56
23	I55	W	0h	Interrupt associated with TCC #55
22	I54	W	0h	Interrupt associated with TCC #54
21	I53	W	0h	Interrupt associated with TCC #53
20	I52	W	0h	Interrupt associated with TCC #52
19	I51	W	0h	Interrupt associated with TCC #51
18	I50	W	0h	Interrupt associated with TCC #50
17	I49	W	0h	Interrupt associated with TCC #49
16	I48	W	0h	Interrupt associated with TCC #48
15	I47	W	0h	Interrupt associated with TCC #47
14	I46	W	0h	Interrupt associated with TCC #46
13	I45	W	0h	Interrupt associated with TCC #45

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Table 4-2237. TPCC_IESRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I44	W	0h	Interrupt associated with TCC #44
11	I43	W	0h	Interrupt associated with TCC #43
10	I42	W	0h	Interrupt associated with TCC #42
9	I41	W	0h	Interrupt associated with TCC #41
8	I40	W	0h	Interrupt associated with TCC #40
7	I39	W	0h	Interrupt associated with TCC #39
6	I38	W	0h	Interrupt associated with TCC #38
5	I37	W	0h	Interrupt associated with TCC #37
4	I36	W	0h	Interrupt associated with TCC #36
3	I35	W	0h	Interrupt associated with TCC #35
2	I34	W	0h	Interrupt associated with TCC #34
1	I33	W	0h	Interrupt associated with TCC #33
0	I32	W	0h	Interrupt associated with TCC #32

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4.4.2.102 TPCC_IPR_RN Register

4.4.2.102.1 TPCC_IPR_RN Register (Offset = 2068h) [reset = 0h]

Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

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Table 4-2238. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2068h

Figure 4-1095. TPCC_IPR_RN Name Register

31	30	29	28	27	26	25	24
I31	I30	I29	I28	I27	I26	I25	I24
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I23	I22	I21	I20	I19	I18	I17	I16
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I15	I14	I13	I12	I11	I10	I9	I8
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2239. TPCC_IPR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	R	0h	Interrupt associated with TCC #31
30	I30	R	0h	Interrupt associated with TCC #30
29	I29	R	0h	Interrupt associated with TCC #29
28	I28	R	0h	Interrupt associated with TCC #28
27	I27	R	0h	Interrupt associated with TCC #27
26	I26	R	0h	Interrupt associated with TCC #26
25	I25	R	0h	Interrupt associated with TCC #25
24	I24	R	0h	Interrupt associated with TCC #24
23	I23	R	0h	Interrupt associated with TCC #23
22	I22	R	0h	Interrupt associated with TCC #22
21	I21	R	0h	Interrupt associated with TCC #21
20	I20	R	0h	Interrupt associated with TCC #20
19	I19	R	0h	Interrupt associated with TCC #19
18	I18	R	0h	Interrupt associated with TCC #18
17	I17	R	0h	Interrupt associated with TCC #17
16	I16	R	0h	Interrupt associated with TCC #16
15	I15	R	0h	Interrupt associated with TCC #15
14	I14	R	0h	Interrupt associated with TCC #14
13	I13	R	0h	Interrupt associated with TCC #13

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Table 4-2239. TPCC_IPR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I12	R	0h	Interrupt associated with TCC #12
11	I11	R	0h	Interrupt associated with TCC #11
10	I10	R	0h	Interrupt associated with TCC #10
9	I9	R	0h	Interrupt associated with TCC #9
8	I8	R	0h	Interrupt associated with TCC #8
7	I7	R	0h	Interrupt associated with TCC #7
6	I6	R	0h	Interrupt associated with TCC #6
5	I5	R	0h	Interrupt associated with TCC #5
4	I4	R	0h	Interrupt associated with TCC #4
3	I3	R	0h	Interrupt associated with TCC #3
2	I2	R	0h	Interrupt associated with TCC #2
1	I1	R	0h	Interrupt associated with TCC #1
0	I0	R	0h	Interrupt associated with TCC #0

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4.4.2.103 TPCC_IPRH_RN Register

4.4.2.103.1 TPCC_IPRH_RN Register (Offset = 206Ch) [reset = 0h]

Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

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Table 4-2240. Instance Table

Instance Name	Physical Address
EDMA0	52A0 206Ch

Figure 4-1096. TPCC_IPRH_RN Name Register

31	30	29	28	27	26	25	24
I63	I62	I61	I60	I59	I58	I57	I56
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I55	I54	I53	I52	I51	I50	I49	I48
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I47	I46	I45	I44	I43	I42	I41	I40
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I39	I38	I37	I36	I35	I34	I33	I32
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2241. TPCC_IPRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	R	0h	Interrupt associated with TCC #63
30	I62	R	0h	Interrupt associated with TCC #62
29	I61	R	0h	Interrupt associated with TCC #61
28	I60	R	0h	Interrupt associated with TCC #60
27	I59	R	0h	Interrupt associated with TCC #59
26	I58	R	0h	Interrupt associated with TCC #58
25	I57	R	0h	Interrupt associated with TCC #57
24	I56	R	0h	Interrupt associated with TCC #56
23	I55	R	0h	Interrupt associated with TCC #55
22	I54	R	0h	Interrupt associated with TCC #54
21	I53	R	0h	Interrupt associated with TCC #53
20	I52	R	0h	Interrupt associated with TCC #52
19	I51	R	0h	Interrupt associated with TCC #51
18	I50	R	0h	Interrupt associated with TCC #50
17	I49	R	0h	Interrupt associated with TCC #49
16	I48	R	0h	Interrupt associated with TCC #48
15	I47	R	0h	Interrupt associated with TCC #47
14	I46	R	0h	Interrupt associated with TCC #46
13	I45	R	0h	Interrupt associated with TCC #45

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Table 4-2241. TPCC_IPRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I44	R	0h	Interrupt associated with TCC #44
11	I43	R	0h	Interrupt associated with TCC #43
10	I42	R	0h	Interrupt associated with TCC #42
9	I41	R	0h	Interrupt associated with TCC #41
8	I40	R	0h	Interrupt associated with TCC #40
7	I39	R	0h	Interrupt associated with TCC #39
6	I38	R	0h	Interrupt associated with TCC #38
5	I37	R	0h	Interrupt associated with TCC #37
4	I36	R	0h	Interrupt associated with TCC #36
3	I35	R	0h	Interrupt associated with TCC #35
2	I34	R	0h	Interrupt associated with TCC #34
1	I33	R	0h	Interrupt associated with TCC #33
0	I32	R	0h	Interrupt associated with TCC #32

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4.4.2.104 TPCC_ICR_RN Register

4.4.2.104.1 TPCC_ICR_RN Register (Offset = 2070h) [reset = 0h]

Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

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Table 4-2242. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2070h

Figure 4-1097. TPCC_ICR_RN Name Register

31	30	29	28	27	26	25	24
I31	I30	I29	I28	I27	I26	I25	I24
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I23	I22	I21	I20	I19	I18	I17	I16
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I15	I14	I13	I12	I11	I10	I9	I8
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2243. TPCC_ICR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	W	0h	Interrupt associated with TCC #31
30	I30	W	0h	Interrupt associated with TCC #30
29	I29	W	0h	Interrupt associated with TCC #29
28	I28	W	0h	Interrupt associated with TCC #28
27	I27	W	0h	Interrupt associated with TCC #27
26	I26	W	0h	Interrupt associated with TCC #26
25	I25	W	0h	Interrupt associated with TCC #25
24	I24	W	0h	Interrupt associated with TCC #24
23	I23	W	0h	Interrupt associated with TCC #23
22	I22	W	0h	Interrupt associated with TCC #22
21	I21	W	0h	Interrupt associated with TCC #21
20	I20	W	0h	Interrupt associated with TCC #20
19	I19	W	0h	Interrupt associated with TCC #19
18	I18	W	0h	Interrupt associated with TCC #18
17	I17	W	0h	Interrupt associated with TCC #17
16	I16	W	0h	Interrupt associated with TCC #16
15	I15	W	0h	Interrupt associated with TCC #15
14	I14	W	0h	Interrupt associated with TCC #14
13	I13	W	0h	Interrupt associated with TCC #13

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Table 4-2243. TPCC_ICR_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I12	W	0h	Interrupt associated with TCC #12
11	I11	W	0h	Interrupt associated with TCC #11
10	I10	W	0h	Interrupt associated with TCC #10
9	I9	W	0h	Interrupt associated with TCC #9
8	I8	W	0h	Interrupt associated with TCC #8
7	I7	W	0h	Interrupt associated with TCC #7
6	I6	W	0h	Interrupt associated with TCC #6
5	I5	W	0h	Interrupt associated with TCC #5
4	I4	W	0h	Interrupt associated with TCC #4
3	I3	W	0h	Interrupt associated with TCC #3
2	I2	W	0h	Interrupt associated with TCC #2
1	I1	W	0h	Interrupt associated with TCC #1
0	I0	W	0h	Interrupt associated with TCC #0

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4.4.2.105 TPCC_ICRH_RN Register

4.4.2.105.1 TPCC_ICRH_RN Register (Offset = 2074h) [reset = 0h]

Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

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Table 4-2244. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2074h

Figure 4-1098. TPCC_ICRH_RN Name Register

31	30	29	28	27	26	25	24
I63	I62	I61	I60	I59	I58	I57	I56
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
I55	I54	I53	I52	I51	I50	I49	I48
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
I47	I46	I45	I44	I43	I42	I41	I40
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
I39	I38	I37	I36	I35	I34	I33	I32
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2245. TPCC_ICRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	W	0h	Interrupt associated with TCC #63
30	I62	W	0h	Interrupt associated with TCC #62
29	I61	W	0h	Interrupt associated with TCC #61
28	I60	W	0h	Interrupt associated with TCC #60
27	I59	W	0h	Interrupt associated with TCC #59
26	I58	W	0h	Interrupt associated with TCC #58
25	I57	W	0h	Interrupt associated with TCC #57
24	I56	W	0h	Interrupt associated with TCC #56
23	I55	W	0h	Interrupt associated with TCC #55
22	I54	W	0h	Interrupt associated with TCC #54
21	I53	W	0h	Interrupt associated with TCC #53
20	I52	W	0h	Interrupt associated with TCC #52
19	I51	W	0h	Interrupt associated with TCC #51
18	I50	W	0h	Interrupt associated with TCC #50
17	I49	W	0h	Interrupt associated with TCC #49
16	I48	W	0h	Interrupt associated with TCC #48
15	I47	W	0h	Interrupt associated with TCC #47
14	I46	W	0h	Interrupt associated with TCC #46
13	I45	W	0h	Interrupt associated with TCC #45

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Table 4-2245. TPCC_ICRH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I44	W	0h	Interrupt associated with TCC #44
11	I43	W	0h	Interrupt associated with TCC #43
10	I42	W	0h	Interrupt associated with TCC #42
9	I41	W	0h	Interrupt associated with TCC #41
8	I40	W	0h	Interrupt associated with TCC #40
7	I39	W	0h	Interrupt associated with TCC #39
6	I38	W	0h	Interrupt associated with TCC #38
5	I37	W	0h	Interrupt associated with TCC #37
4	I36	W	0h	Interrupt associated with TCC #36
3	I35	W	0h	Interrupt associated with TCC #35
2	I34	W	0h	Interrupt associated with TCC #34
1	I33	W	0h	Interrupt associated with TCC #33
0	I32	W	0h	Interrupt associated with TCC #32

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4.4.2.106 TPCC_IEVAL_RN Register

4.4.2.106.1 TPCC_IEVAL_RN Register (Offset = 2078h) [reset = 0h]

Interrupt Eval Register

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Table 4-2246. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2078h

Figure 4-1099. TPCC_IEVAL_RN Name Register

31	30	29	28	27	26	25	24
RES76							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RES76							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RES76							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES76						SET	EVAL
R						W	W
0h						0h	0h

Table 4-2247. TPCC_IEVAL_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RES76	R	0h	RESERVE FIELD
1	SET	W	0h	Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable [IERn] and status [IPRn]. CPU write of '0' has no effect.
0	EVAL	W	0h	Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts [IERn] are still pending [IPRn]. CPU write of '0' has no effect..

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4.4.2.107 TPCC_QER_RN Register

4.4.2.107.1 TPCC_QER_RN Register (Offset = 2080h) [reset = 0h]

QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

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Table 4-2248. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2080h

Figure 4-1100. TPCC_QER_RN Name Register

31	30	29	28	27	26	25	24
RES77							
R							
0h							
23	22	21	20	19	18	17	16
RES77							
R							
0h							
15	14	13	12	11	10	9	8
RES77							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2249. TPCC_QER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES77	R	0h	RESERVE FIELD
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.108 TPCC_QEER_RN Register

4.4.2.108.1 TPCC_QEER_RN Register (Offset = 2084h) [reset = 0h]

QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

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Table 4-2250. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2084h

Figure 4-1101. TPCC_QEER_RN Name Register

31	30	29	28	27	26	25	24
RES78							
R							
0h							
23	22	21	20	19	18	17	16
RES78							
R							
0h							
15	14	13	12	11	10	9	8
RES78							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2251. TPCC_QEER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES78	R	0h	RESERVE FIELD
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.109 TPCC_QEECR_RN Register

4.4.2.109.1 TPCC_QEECR_RN Register (Offset = 2088h) [reset = 0h]

QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

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Table 4-2252. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2088h

Figure 4-1102. TPCC_QEECR_RN Name Register

31	30	29	28	27	26	25	24
RES79							
R							
0h							
23	22	21	20	19	18	17	16
RES79							
R							
0h							
15	14	13	12	11	10	9	8
RES79							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2253. TPCC_QEECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES79	R	0h	RESERVE FIELD
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.110 TPCC_QEESR_RN Register

4.4.2.110.1 TPCC_QEESR_RN Register (Offset = 208Ch) [reset = 0h]

QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

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Table 4-2254. Instance Table

Instance Name	Physical Address
EDMA0	52A0 208Ch

Figure 4-1103. TPCC_QEESR_RN Name Register

31	30	29	28	27	26	25	24
RES80							
R							
0h							
23	22	21	20	19	18	17	16
RES80							
R							
0h							
15	14	13	12	11	10	9	8
RES80							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2255. TPCC_QEESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES80	R	0h	RESERVE FIELD
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.111 TPCC_QSER_RN Register

4.4.2.111.1 TPCC_QSER_RN Register (Offset = 2090h) [reset = 0h]

QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

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Table 4-2256. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2090h

Figure 4-1104. TPCC_QSER_RN Name Register

31	30	29	28	27	26	25	24
RES81							
R							
0h							
23	22	21	20	19	18	17	16
RES81							
R							
0h							
15	14	13	12	11	10	9	8
RES81							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2257. TPCC_QSER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES81	R	0h	RESERVE FIELD
7	E7	R	0h	Event #7
6	E6	R	0h	Event #6
5	E5	R	0h	Event #5
4	E4	R	0h	Event #4
3	E3	R	0h	Event #3
2	E2	R	0h	Event #2
1	E1	R	0h	Event #1
0	E0	R	0h	Event #0

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4.4.2.112 TPCC_QSECR_RN Register

4.4.2.112.1 TPCC_QSECR_RN Register (Offset = 2094h) [reset = 0h]

QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

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Table 4-2258. Instance Table

Instance Name	Physical Address
EDMA0	52A0 2094h

Figure 4-1105. TPCC_QSECR_RN Name Register

31	30	29	28	27	26	25	24
RES82							
R							
0h							
23	22	21	20	19	18	17	16
RES82							
R							
0h							
15	14	13	12	11	10	9	8
RES82							
R							
0h							
7	6	5	4	3	2	1	0
E7	E6	E5	E4	E3	E2	E1	E0
W	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h

Table 4-2259. TPCC_QSECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RES82	R	0h	RESERVE FIELD
7	E7	W	0h	Event #7
6	E6	W	0h	Event #6
5	E5	W	0h	Event #5
4	E4	W	0h	Event #4
3	E3	W	0h	Event #3
2	E2	W	0h	Event #2
1	E1	W	0h	Event #1
0	E0	W	0h	Event #0

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4.4.2.113 TPCC_OPT Register

4.4.2.113.1 TPCC_OPT Register (Offset = 4000h) [reset = 0h]

Options Parameter

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Table 4-2260. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4000h

Figure 4-1106. TPCC_OPT Name Register

31	30	29	28	27	26	25	24
PRIV	RES83			PRIVID			
R	R			R			
0h	0h			0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ITCCHEN	TCCHEN	ITCINTEN	TCINTEN	WIMODE	RES84	TCC	
R/W	R/W	R/W	R/W	R/W	R	R/W	
0h	0h	0h	0h	0h	0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TCC				TCCMODE	FWID		
R/W				R/W	R/W		
0h				0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RES85				STATIC	SYNCDIM	DAM	SAM
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 4-2261. TPCC_OPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRIV	R	0h	Privilege level: privilege level [supervisor vs. user] for the host/cpu/dma that programmed this PaRAM Entry. Value is set with the vbus priv value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus. PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege
30:28	RES83	R	0h	RESERVE FIELD
27:24	PRIVID	R	0h	Privilege ID: Privilege ID for the external host/cpu/dma that programmed this PaRAM Entry. This value is set with the vbus privid value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus.
23	ITCCHEN	R/W	0h	Intermediate transfer completion chaining enable: 0: Intermediate transfer complete chaining is disabled. 1: Intermediate transfer complete chaining is enabled.
22	TCCHEN	R/W	0h	Transfer complete chaining enable: 0:Transfer complete chaining is disabled. 1:Transfer complete chaining is enabled.
21	ITCINTEN	R/W	0h	Intermediate transfer completion interrupt enable: 0: Intermediate transfer complete interrupt is disabled. 1: Intermediate transfer complete interrupt is enabled [corresponding IER[TCC] bit must be set to 1 to generate interrupt]
20	TCINTEN	R/W	0h	Transfer complete interrupt enable: 0:Transfer complete interrupt is disabled. 1:Transfer complete interrupt is enabled [corresponding IER[TCC] bit must be set to 1 to generate interrupt]

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Table 4-2261. TPCC_OPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	WIMODE	R/W	0h	Backward compatibility mode: 0:Normal operation 1 : WI Backwards Compatibility mode forces BCNT to be adjusted by '1' upon TR submission [0 means 1 1 means 2 ...] and forces ACNT to be treated as a word-count [left shifted by 2 by hardware to create byte cnt for TR submission]
18	RES84	R	0h	RESERVE FIELD
17:12	TCC	R/W	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER [bit CER[TCC]] for chaining or in IER [bit IER[TCC]] for interrupts.
11	TCCMODE	R/W	0h	Transfer complete code mode: Indicates the point at which a transfer is considered completed. Applies to both chaining and interrupt. 0:Normal Completion A transfer is considered completed after the transfer parameters are returned to the CC from the TC [which was returned from the peripheral]. 1:Early Completion A transfer is considered completed after the CC submits a TR to the TC. CC generates completion code internally .
10:8	FWID	R/W	0h	FIFO width: Applies if either SAM or DAM is set to FIFO mode. Pass-thru to TC.
7:4	RES85	R	0h	RESERVE FIELD
3	STATIC	R/W	0h	Static Entry: 0:Entry is updated as normal 1:Entry is static Count and Address updates are not updated after TRP is submitted. Linking is not performed.
2	SYNCDIM	R/W	0h	Transfer Synchronization Dimension: 0:A-Sync Each event triggers the transfer of ACNT elements. 1:AB-Sync Each event triggers the transfer of BCNT arrays of ACNT elements
1	DAM	R/W	0h	Destination Address Mode: Destination Address Mode within an array. Pass-thru to TC. 0:INCR Dst addressing within an array increments. Dst is not a FIFO. 1:FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	R/W	0h	Source Address Mode: Source Address Mode within an array. Pass-thru to TC. 0:INCR Src addressing within an array increments. Source is not a FIFO. 1:FIFO Src addressing within an array wraps around upon reaching FIFO width.

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4.4.2.114 TPCC_SRC Register

4.4.2.114.1 TPCC_SRC Register (Offset = 4004h) [reset = 0h]

Source Address

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Table 4-2262. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4004h

Figure 4-1107. TPCC_SRC Name Register

31	30	29	28	27	26	25	24
SRC							
R/W							
0h							
23	22	21	20	19	18	17	16
SRC							
R/W							
0h							
15	14	13	12	11	10	9	8
SRC							
R/W							
0h							
7	6	5	4	3	2	1	0
SRC							
R/W							
0h							

Table 4-2263. TPCC_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SRC	R/W	0h	Source Address: The 32-bit source address parameters specify the starting byte address of the source . If SAM is set to FIFO mode then the user should program the Source address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true.

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4.4.2.115 TPCC_ABCNT Register

4.4.2.115.1 TPCC_ABCNT Register (Offset = 4008h) [reset = 0h]

A and B byte count

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Table 4-2264. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4008h

Figure 4-1108. TPCC_ABCNT Name Register

31	30	29	28	27	26	25	24
BCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
ACNT							
R/W							
0h							
7	6	5	4	3	2	1	0
ACNT							
R/W							
0h							

Table 4-2265. TPCC_ABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	BCNT	R/W	0h	BCNT : Count for 2nd Dimension: BCNT is a 16-bit unsigned value that specifies the number of arrays of length ACNT. For normal operation valid values for BCNT can be anywhere between 1 and 65535. Therefore the maximum number of arrays in a frame is 65535 [64K-1 arrays]. BCNT=1 means 1 array in the frame and BCNT=0 means 0 arrays in the frame. In normal mode a BCNT of '0' is considered as either a Null or Dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the programmed BCNT value will be incremented by '1' before submission to TC. I.e. 0 means 1 1 means 2 2 means 3 ...

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Table 4-2265. TPCC_ABCNT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	ACNT	R/W	0h	ACNT : number of bytes in 1st dimension: ACNT represents the number of bytes within the first dimension of a transfer. ACNT is a 16-bit unsigned value with valid values between 0 and 65535. Therefore the maximum number of bytes in an array is 65535 bytes [64K-1 bytes]. ACNT must be greater than or equal to '1' for a TR to be submitted to TC. An ACNT of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the ACNT field represents a word count. The CC must internally multiply by 4 to translate the word count to a byte count prior to submission to the TC. The 2 MSBs of the 16-bit ACNT are reserved and should always be written as 'b00 by the user. If user writes a value other than 0 it will still be treated as 0 since the multiply-by-4 operation [to translate between a word count and a byte count] will drop the 2 msbits. For dummy and null transfer definition the ACNT definition will disregard the 2 msbits. I.e. a programmed ACNT value of 0x8000 in WI-mode will be treated as 0 byte transfer resulting in null or dummy operation dependent on the state of BCNT and CCNT.

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4.4.2.116 TPCC_DST Register

4.4.2.116.1 TPCC_DST Register (Offset = 400Ch) [reset = 0h]

Destination Address

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Table 4-2266. Instance Table

Instance Name	Physical Address
EDMA0	52A0 400Ch

Figure 4-1109. TPCC_DST Name Register

31	30	29	28	27	26	25	24
DST							
R/W							
0h							
23	22	21	20	19	18	17	16
DST							
R/W							
0h							
15	14	13	12	11	10	9	8
DST							
R/W							
0h							
7	6	5	4	3	2	1	0
DST							
R/W							
0h							

Table 4-2267. TPCC_DST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DST	R/W	0h	Destination Address: The 32-bit destination address parameters specify the starting byte address of the destination. If DAM is set to FIFO mode then the user should program the Destination address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true.

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4.4.2.117 TPCC_BIDX Register

4.4.2.117.1 TPCC_BIDX Register (Offset = 4010h) [reset = 0h]

Register description is not available

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Table 4-2268. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4010h

Figure 4-1110. TPCC_BIDX Name Register

31	30	29	28	27	26	25	24
DBIDX							
R/W							
0h							
23	22	21	20	19	18	17	16
DBIDX							
R/W							
0h							
15	14	13	12	11	10	9	8
SBIDX							
R/W							
0h							
7	6	5	4	3	2	1	0
SBIDX							
R/W							
0h							

Table 4-2269. TPCC_BIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DBIDX	R/W	0h	Destination 2nd Dimension Index: DBIDX is a 16-bit signed value [2's complement] used for destination address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the destination array to the beginning of the next destination array within the current frame. It applies to both A-Sync and AB-Sync transfers.
15:0	SBIDX	R/W	0h	Source 2nd Dimension Index: SBIDX is a 16-bit signed value [2's complement] used for source address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the source array to the beginning of the next source array. It applies to both A-sync and AB-sync transfers.

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4.4.2.118 TPCC_LNK Register

4.4.2.118.1 TPCC_LNK Register (Offset = 4014h) [reset = 0h]

Link and Reload parameters

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Table 4-2270. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4014h

Figure 4-1111. TPCC_LNK Name Register

31	30	29	28	27	26	25	24
BCNTRLD							
R/W							
0h							
23	22	21	20	19	18	17	16
BCNTRLD							
R/W							
0h							
15	14	13	12	11	10	9	8
LINK							
R/W							
0h							
7	6	5	4	3	2	1	0
LINK							
R/W							
0h							

Table 4-2271. TPCC_LNK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	BCNTRLD	R/W	0h	BCNT Reload: BCNTRLD is a 16-bit unsigned value used to reload the BCNT field once the last array in the 2nd dimension is transferred. This field is only used for A-Sync'ed transfers. In this case the CC decrements the BCNT value by one on each TR submission. When BCNT [conceptually] reaches zero then the CC decrements CCNT and uses the BCNTRLD value to reinitialize the BCNT value. For AB-synchronized transfers the CC submits the BCNT in the TR and therefore the TC is responsible to keep track of BCNT not thus BCNTRLD is a don't care field.

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Table 4-2271. TPCC_LNK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0	LINK	R/W	0h	Link Address: The CC provides a mechanism to reload the current PaRAM Entry upon its natural termination [i.e. after count fields are decremented to '0'] with a new PaRAM Entry. This is called 'linking'. The 16-bit parameter LINK specifies the byte address offset in the PaRAM from which the CC loads/reloads the next PaRAM entry in the link. The CC should disregard the value in the upper 2 bits of the LINK field as well as the lower 5-bits of the LINK field. The upper two bits are ignored such that the user can program either the 'literal' byte address of the LINK parameter or the 'PaRAM base-relative' address of the link field. Therefore if the user uses the literal address with a range from 0x4000 to 0x7FFF it will be treated as a PaRAM-base-relative value of 0x0000 to 0x3FFF. The lower-5 bits are ignored and treated as 'b00000 thereby guaranteeing that all Link pointers point to a 32-byte aligned PaRAM entry. In the latter case [5-lsbs] behavior is undefined for the user [i.e. don't have to test it]. In the former case [2 msbs] user should be able to take advantage of this feature [i.e. do have to test it]. If a Link Update is requested to a PaRAM address that is beyond the actual range of implemented PaRAM then the Link will be treated as a Null Linkand all 0s plus 0xFFFF will be written to the current entry location. A LINK value of 0xFFFF is referred to as a NULL link which should cause the CC to write 0x0 to all entries of the current PaRAM Entry except for the LINK field which is set to 0xFFFF. The Priv/Privid/Secure state is overwritten to 0x0 when linking. MSBs and LSBS should not be masked when comparing against the 0xFFFF value. I.e. a value of 0x3FFE is a non-NULL PaRAM link field.

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4.4.2.119 TPCC_CIDX Register

4.4.2.119.1 TPCC_CIDX Register (Offset = 4018h) [reset = 0h]

Register description is not available

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Table 4-2272. Instance Table

Instance Name	Physical Address
EDMA0	52A0 4018h

Figure 4-1112. TPCC_CIDX Name Register

31	30	29	28	27	26	25	24
DCIDX							
R/W							
0h							
23	22	21	20	19	18	17	16
DCIDX							
R/W							
0h							
15	14	13	12	11	10	9	8
SCIDX							
R/W							
0h							
7	6	5	4	3	2	1	0
SCIDX							
R/W							
0h							

Table 4-2273. TPCC_CIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DCIDX	R/W	0h	Destination Frame Index: DCIDX is a 16-bit signed value [2's complement] used for destination address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array [pointed to by DST address] to the beginning of the first destination array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when DCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a ABsync transfer is the first array in the frame.
15:0	SCIDX	R/W	0h	Source Frame Index: SCIDX is a 16-bit signed value [2's complement] used for source address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array [pointed to by SRC address] to the beginning of the first source array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when SCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a AB-sync transfer is the first array in the frame.

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4.4.2.120 TPCC_CCNT Register

4.4.2.120.1 TPCC_CCNT Register (Offset = 401Ch) [reset = 0h]

C byte count

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Table 4-2274. Instance Table

Instance Name	Physical Address
EDMA0	52A0 401Ch

Figure 4-1113. TPCC_CCNT Name Register

31	30	29	28	27	26	25	24
RES86							
R							
0h							
23	22	21	20	19	18	17	16
RES86							
R							
0h							
15	14	13	12	11	10	9	8
CCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
CCNT							
R/W							
0h							

Table 4-2275. TPCC_CCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RES86	R	0h	RESERVE FIELD
15:0	CCNT	R/W	0h	CCNT : Count for 3rd Dimension: CCNT is a 16-bit unsigned value that specifies the number of frames in a block. Valid values for CCNT can be anywhere between 1 and 65535. Therefore the maximum number of frames in a block is 65535 [64K-1 frames]. CCNT of '1' means '1' frame in the block and CCNT of '0' means '0' frames in the block. A CCNT value of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. WIMODE has no effect on CCNT operation.

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4.4.2.121 TPTC_PID Register

4.4.2.121.1 TPTC_PID Register (Offset = 0h) [reset = 40000B01h]

Peripheral ID Register.

Return to Summary Table

Table 4-2276. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0000h
EDMA1	52A6 0000h

Figure 4-1114. TPTC_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		NONE		R			
1h		0h		0h			
23	22	21	20	19	18	17	16
FUNC							
R							
0h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
1h					3h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		1h					

Table 4-2277. TPTC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1.
29:28	RESERVED	NONE	0h	Reserved
27:16	FUNC	R	0h	Function indicates a software compatible module family.
15:11	RTL	R	1h	RTL Version
10:8	MAJOR	R	3h	Major Revision
7:6	CUSTOM	R	0h	Custom revision field: Not used on this version of EDMA.
5:0	MINOR	R	1h	Minor Revision

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4.4.2.122 TPTC_TCCFG Register

4.4.2.122.1 TPTC_TCCFG Register (Offset = 4h) [reset = 224h]

TC Configuration Register.

Return to Summary Table

Table 4-2278. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0004h
EDMA1	52A6 0004h

Figure 4-1115. TPTC_TCCFG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">RESERVED</td><td colspan="2">DREGDEPTH</td></tr>
<tr><td colspan="6">NONE</td><td colspan="2">R</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="2">BUSWIDTH</td><td>RESERVED</td><td colspan="3">FIFOSIZE</td></tr>
<tr><td colspan="2">NONE</td><td colspan="2">R</td><td>NONE</td><td colspan="3">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">2h</td><td>0h</td><td colspan="3">4h</td></tr>
</table>

Table 4-2279. TPTC_TCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	DREGDEPTH	R	2h	Dst Register FIFO Depth Parameterization
7:6	RESERVED	NONE	0h	Reserved
5:4	BUSWIDTH	R	2h	Bus Width Parameterization
3	RESERVED	NONE	0h	Reserved
2:0	FIFOSIZE	R	4h	Fifo Size Parameterization

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4.4.2.123 TPTC_TCSTAT Register

4.4.2.123.1 TPTC_TCSTAT Register (Offset = 100h) [reset = 100h]

TC Status Register.

Return to Summary Table

Table 4-2280. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0100h
EDMA1	52A6 0100h

Figure 4-1116. TPTC_TCSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		DFSTRTPTR		RESERVED			ACTV
NONE		R		NONE			R
0h		0h		0h			1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DSTACTV			RESERVED	WSACTV	SRCACTV	PROGBUSY
NONE	R			NONE	R	R	R
0h	0h			0h	0h	0h	0h

Table 4-2281. TPTC_TCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:12	DFSTRTPTR	R	0h	Dst FIFO Start Pointer Represents the offset to the head entry of Dst Register FIFO in units of entries. Legal values = 0x0 to 0x3
11:9	RESERVED	NONE	0h	Reserved
8	ACTV	R	1h	Channel Active Channel Active is a logical-OR of each of the BUSY/ACTV signals. The ACTV bit must remain high through the life of a TR. ACTV = 0 : Channel is idle. ACTV = 1 : Channel is busy.
7	RESERVED	NONE	0h	Reserved
6:4	DSTACTV	R	0h	Destination Active State Specifies the number of TRs that are resident in the Dst Register FIFO at a given instant. Legal values are constrained by the DSTREGDEPTH parameter.
3	RESERVED	NONE	0h	Reserved

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Table 4-2281. TPTC_TCSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	WSACTV	R	0h	Write Status Active WSACTV = 0 : Write status is not pending. Write status has been received for all previously issued write commands. WSACTV = 1 : Write Status is pending. Write status has not been received for all previously issued write commands.
1	SRCACTV	R	0h	Source Active State SRCACTV = 0 : Source Active set is idle. Any TR written to Prog Set will immediately transition to Source Active set as long as the Dst FIFO Set is not full [DSTFULL == 1]. SRCACTV = 1 : Source Active set is busy either performing read transfers or waiting to perform read transfers for current Transfer Request.
0	PROGBUSY	R	0h	Program Register Set Busy PROGBUSY = 0 : Prog set idle and is available for programming. PROGBUSY = 1 : Prog set busy. User should poll for PROGBUSY equal to '0' prior to re-programming the Program Register set.

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4.4.2.124 TPTC_INTSTAT Register

4.4.2.124.1 TPTC_INTSTAT Register (Offset = 104h) [reset = 0h]

Interrupt Status Register.

Return to Summary Table

Table 4-2282. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0104h
EDMA1	52A6 0104h

Figure 4-1117. TPTC_INTSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TRDONE	PROGEMPTY
NONE						R	R
0h						0h	0h

Table 4-2283. TPTC_INTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TRDONE	R	0h	TR Done Event Status: TRDONE = 0 : Condition not detected. TRDONE = 1 : Set when TC has completed a Transfer Request. TRDONE should be set when the write status is returned for the final write of a TR. Cleared when user writes '1' to INTCLR.TRDONE register bit.
0	PROGEMPTY	R	0h	Program Set Empty Event Status: PROGEMPTY = 0 : Condition not detected. PROGEMPTY = 1 : Set when Program Register set transitions to empty state. Cleared when user writes '1' to INTCLR.PROGEMPTY register bit.

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4.4.2.125 TPTC_INTEN Register

4.4.2.125.1 TPTC_INTEN Register (Offset = 108h) [reset = 0h]

Interrupt Enable Register.

Return to Summary Table

Table 4-2284. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0108h
EDMA1	52A6 0108h

Figure 4-1118. TPTC_INTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						R/W	R/W
0h						0h	0h

Table 4-2285. TPTC_INTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TRDONE	R/W	0h	TR Done Event Enable: INTEN.TRDONE = 0 : TRDONE Event is disabled. INTEN.TRDONE = 1 : TRDONE Event is enabled and contributes to interrupt generation
0	PROGEMPTY	R/W	0h	Program Set Empty Event Enable: INTEN.PROGEMPTY = 0 : PROGEMPTY Event is disabled. INTEN.PROGEMPTY = 1 : PROGEMPTY Event is enabled and contributes to interrupt generation

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4.4.2.126 TPTC_INTCLR Register

4.4.2.126.1 TPTC_INTCLR Register (Offset = 10Ch) [reset = 0h]

Interrupt Clear Register.

Return to Summary Table

Table 4-2286. Instance Table

Instance Name	Physical Address
EDMA0	52A4 010Ch
EDMA1	52A6 010Ch

Figure 4-1119. TPTC_INTCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TRDONE	PROGEMPTY
NONE						W	W
0h						0h	0h

Table 4-2287. TPTC_INTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TRDONE	W	0h	TR Done Event Clear: INTCLR.TRDONE = 0 : Writes of '0' have no effect. INTCLR.TRDONE = 1 : Write of '1' clears INTSTAT.TRDONE bit
0	PROGEMPTY	W	0h	Program Set Empty Event Clear: INTCLR.PROGEMPTY = 0 : Writes of '0' have no effect. INTCLR.PROGEMPTY = 1 : Write of '1' clears INTSTAT.PROGEMPTY bit

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4.4.2.127 TPTC_INTCMD Register

4.4.2.127.1 TPTC_INTCMD Register (Offset = 110h) [reset = 0h]

Interrupt Command Register.

Return to Summary Table

Table 4-2288. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0110h
EDMA1	52A6 0110h

Figure 4-1120. TPTC_INTCMD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						SET	EVAL
NONE						W	W
0h						0h	0h

Table 4-2289. TPTC_INTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SET	W	0h	Set TPTC interrupt: Write of '1' to SET causes TPTC interrupt to be pulsed unconditionally. Writes of '0' have no affect.
0	EVAL	W	0h	Evaluate state of TPTC interrupt Write of '1' to EVAL causes TPTC interrupt to be pulsed if any of the INTSTAT bits are set to '1'. Writes of '0' have no affect.

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4.4.2.128 TPTC_ERRSTAT Register

4.4.2.128.1 TPTC_ERRSTAT Register (Offset = 120h) [reset = 0h]

Error Status Register.

Return to Summary Table

Table 4-2290. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0120h
EDMA1	52A6 0120h

Figure 4-1121. TPTC_ERRSTAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				R	R	NONE	R
0h				0h	0h	0h	0h

Table 4-2291. TPTC_ERRSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MMRAERR	R	0h	MMR Address Error: MMRAERR = 0 : Condition not detected. MMRAERR = 1 : User attempted to read or write to invalid address configuration memory map. [Is only be set for non-emulation accesses]. No additional error information is recorded.
2	TRERR	R	0h	TR Error: TR detected that violates FIFO Mode transfer [SAM or DAM is '1'] alignment rules or has ACNT or BCNT == 0. No additional error information is recorded.
1	RESERVED	NONE	0h	Reserved
0	BUSERR	R	0h	Bus Error Event: BUSERR = 0:Condition not detected. BUSERR = 1:TC has detected an error code on the write response bus or read response bus. Error information is stored in Error Details Register [ERRDET].

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4.4.2.129 TPTC_ERREN Register

4.4.2.129.1 TPTC_ERREN Register (Offset = 124h) [reset = 0h]

Error Enable Register.

Return to Summary Table

Table 4-2292. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0124h
EDMA1	52A6 0124h

Figure 4-1122. TPTC_ERREN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				R/W	R/W	NONE	R/W
0h				0h	0h	0h	0h

Table 4-2293. TPTC_ERREN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MMRAERR	R/W	0h	Interrupt enable for ERRSTAT.MMRAERR: ERREN.MMRAERR = 0 : BUSERR is disabled. ERREN.MMRAERR = 1 : MMRAERR is enabled and contributes to the TPTC error interrupt generation.
2	TRERR	R/W	0h	Interrupt enable for ERRSTAT.TRERR: ERREN.TRERR = 0 : BUSERR is disabled. ERREN.TRERR = 1 : TRERR is enabled and contributes to the TPTC error interrupt generation.
1	RESERVED	NONE	0h	Reserved
0	BUSERR	R/W	0h	Interrupt enable for ERRSTAT.BUSERR: ERREN.BUSERR = 0 : BUSERR is disabled. ERREN.BUSERR = 1 : BUSERR is enabled and contributes to the TPTC error interrupt generation.

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4.4.2.130 TPTC_ERRCLR Register

4.4.2.130.1 TPTC_ERRCLR Register (Offset = 128h) [reset = 0h]

Error Clear Register.

Return to Summary Table

Table 4-2294. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0128h
EDMA1	52A6 0128h

Figure 4-1123. TPTC_ERRCLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MMRAERR	TRERR	RESERVED	BUSERR
NONE				W	W	NONE	W
0h				0h	0h	0h	0h

Table 4-2295. TPTC_ERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	MMRAERR	W	0h	Interrupt clear for ERRSTAT.MMRAERR: ERRCLR.MMRAERR = 0 : Writes of '0' have no effect. ERRCLR.MMRAERR = 1 : Write of '1' clears ERRSTAT.MMRAERR bit. Write of '1' to ERRCLR.MMRAERR does not clear the ERRDET register.
2	TRERR	W	0h	Interrupt clear for ERRSTAT.TRERR: ERRCLR.TRERR = 0 : Writes of '0' have no effect. ERRCLR.TRERR = 1 : Write of '1' clears ERRSTAT.TRERR bit. Write of '1' to ERRCLR.TRERR does not clear the ERRDET register.
1	RESERVED	NONE	0h	Reserved
0	BUSERR	W	0h	Interrupt clear for ERRSTAT.BUSERR: ERRCLR.BUSERR = 0 : Writes of '0' have no effect. ERRCLR.BUSERR = 1 : Write of '1' clears ERRSTAT.BUSERR bit. Write of '1' to ERRCLR.BUSERR clears the ERRDET register.

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4.4.2.131 TPTC_ERRDET Register

4.4.2.131.1 TPTC_ERRDET Register (Offset = 12Ch) [reset = 0h]

Error Details Register.

Return to Summary Table

Table 4-2296. Instance Table

Instance Name	Physical Address
EDMA0	52A4 012Ch
EDMA1	52A6 012Ch

Figure 4-1124. TPTC_ERRDET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						TCCHEN	TCINTEN
NONE						R	R
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TCC					
NONE		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				STAT			
NONE				R			
0h				0h			

Table 4-2297. TPTC_ERRDET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	TCCHEN	R	0h	Contains the OPT.TCCHEN value programmed by the user for the Read or Write transaction that resulted in an error.
16	TCINTEN	R	0h	Contains the OPT.TCINTEN value programmed by the user for the Read or Write transaction that resulted in an error.
15:14	RESERVED	NONE	0h	Reserved
13:8	TCC	R	0h	Transfer Complete Code: Contains the OPT.TCC value programmed by the user for the Read or Write transaction that resulted in an error.
7:4	RESERVED	NONE	0h	Reserved
3:0	STAT	R	0h	Transaction Status: Stores the non-zero status/error code that was detected on the read status or write status bus. MS-bit effectively serves as the read vs. write error code. If read status and write status are returned on the same cycle then the TC chooses non-zero version. If both are non-zero then write status is treated as higher priority. Encoding of errors matches the CBA spec.

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4.4.2.132 TPTC_ERRCMD Register

4.4.2.132.1 TPTC_ERRCMD Register (Offset = 130h) [reset = 0h]

Error Command Register.

Return to Summary Table

Table 4-2298. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0130h
EDMA1	52A6 0130h

Figure 4-1125. TPTC_ERRCMD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SET	EVAL
NONE						W	W
0h						0h	0h

Table 4-2299. TPTC_ERRCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SET	W	0h	Set TPTC error interrupt: Write of '1' to SET causes TPTC error interrupt to be pulsed unconditionally. Writes of '0' have no affect.
0	EVAL	W	0h	Evaluate state of TPTC error interrupt Write of '1' to EVAL causes TPTC error interrupt to be pulsed if any of the ERRSTAT bits are set to '1'. Writes of '0' have no affect.

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4.4.2.133 TPTC_RDRATE Register

4.4.2.133.1 TPTC_RDRATE Register (Offset = 140h) [reset = 0h]

Read Rate Register.

Return to Summary Table

Table 4-2300. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0140h
EDMA1	52A6 0140h

Figure 4-1126. TPTC_RDRATE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					RDRATE		
NONE					R/W		
0h					0h		

Table 4-2301. TPTC_RDRATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	RDRATE	R/W	0h	Read Rate Control: Controls the number of cycles between read commands. This is a global setting that applies to all TRs for this TC.

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4.4.2.134 TPTC_POPT Register

4.4.2.134.1 TPTC_POPT Register (Offset = 200h) [reset = 0h]

Prog Set Options.

Return to Summary Table

Table 4-2302. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0200h
EDMA1	52A6 0200h

Figure 4-1127. TPTC_POPT Name Register

31	30	29	28	27	26	25	24
RESERVED		DBG_ID		RESERVED			
NONE		R/W		NONE			
0h		0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE	R/W	NONE	R/W	NONE		R/W	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TCC				RESERVED	FWID		
R/W				NONE	R/W		
0h				0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI			RESERVED		DAM	SAM
NONE	R/W			NONE		R/W	R/W
0h	0h			0h		0h	0h

Table 4-2303. TPTC_POPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:28	DBG_ID	R/W	0h	Debug ID Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus. Used at system level for trace/profiling of user selected transfers in systems that include this feature.
27:23	RESERVED	NONE	0h	Reserved
22	TCCHEN	R/W	0h	Transfer complete chaining enable: 0:Transfer complete chaining is disabled. 1:Transfer complete chaining is enabled.
21	RESERVED	NONE	0h	Reserved
20	TCINTEN	R/W	0h	Transfer complete interrupt enable: 0:Transfer complete interrupt is disabled. 1:Transfer complete interrupt is enabled.
19:18	RESERVED	NONE	0h	Reserved
17:12	TCC	R/W	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
11	RESERVED	NONE	0h	Reserved
10:8	FWID	R/W	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
7	RESERVED	NONE	0h	Reserved

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Table 4-2303. TPTC_POPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI	R/W	0h	Transfer Priority: 0:Priority 0 - Highest priority 1:Priority 1 ... 7:Priority 7 - Lowest priority
3:2	RESERVED	NONE	0h	Reserved
1	DAM	R/W	0h	Destination Address Mode within an array: 0:INCR Dst addressing within an array increments. 1:FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	R/W	0h	Source Address Mode within an array: 0:INCR Src addressing within an array increments. 1:FIFO Src addressing within an array wraps around upon reaching FIFO width.

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4.4.2.135 TPTC_PSRC Register

4.4.2.135.1 TPTC_PSRC Register (Offset = 204h) [reset = 0h]

Prog Set Src Address.

Return to Summary Table

Table 4-2304. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0204h
EDMA1	52A6 0204h

Figure 4-1128. TPTC_PSRC Name Register

31	30	29	28	27	26	25	24
SADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
SADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
SADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
SADDR							
R/W							
0h							

Table 4-2305. TPTC_PSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDR	R/W	0h	Source address for Program Register Set

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4.4.2.136 TPTC_PCNT Register

4.4.2.136.1 TPTC_PCNT Register (Offset = 208h) [reset = 0h]

Prog Set Count.

Return to Summary Table

Table 4-2306. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0208h
EDMA1	52A6 0208h

Figure 4-1129. TPTC_PCNT Name Register

31	30	29	28	27	26	25	24
BCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
BCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
ACNT							
R/W							
0h							
7	6	5	4	3	2	1	0
ACNT							
R/W							
0h							

Table 4-2307. TPTC_PCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	BCNT	R/W	0h	B-Dimension count. Number of arrays to be transferred where each array is ACNT in length.
15:0	ACNT	R/W	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

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4.4.2.137 TPTC_PDST Register

4.4.2.137.1 TPTC_PDST Register (Offset = 20Ch) [reset = 0h]

Prog Set Dst Address.

Return to Summary Table

Table 4-2308. Instance Table

Instance Name	Physical Address
EDMA0	52A4 020Ch
EDMA1	52A6 020Ch

Figure 4-1130. TPTC_PDST Name Register

31	30	29	28	27	26	25	24
DADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
DADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
DADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
DADDR							
R/W							
0h							

Table 4-2309. TPTC_PDST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DADDR	R/W	0h	Destination address for Program Register Set

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4.4.2.138 TPTC_PBIDX Register

4.4.2.138.1 TPTC_PBIDX Register (Offset = 210h) [reset = 0h]

Prog Set B-Dim Idx.

Return to Summary Table

Table 4-2310. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0210h
EDMA1	52A6 0210h

Figure 4-1131. TPTC_PBIDX Name Register

31	30	29	28	27	26	25	24
DBIDX							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBIDX							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SBIDX							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SBIDX							
R/W							
0h							

Table 4-2311. TPTC_PBIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DBIDX	R/W	0h	Dest B-Idx for Program Register Set: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15:0	SBIDX	R/W	0h	Source B-Idx for Program Register Set: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

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4.4.2.139 TPTC_PMPPRXY Register

4.4.2.139.1 TPTC_PMPPRXY Register (Offset = 214h) [reset = 0h]

Prog Set Mem Protect Proxy.

Return to Summary Table

Table 4-2312. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0214h
EDMA1	52A6 0214h

Figure 4-1132. TPTC_PMPPRXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				R			
0h				0h			

Table 4-2313. TPTC_PMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	SECURE	R	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	R	0h	Privilege Level: PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register]. The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
7:4	RESERVED	NONE	0h	Reserved

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Table 4-2313. TPTC_PMPPRXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PRIVID	R	0h	Privilege ID: PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register]. The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

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4.4.2.140 TPTC_SAOPT Register

4.4.2.140.1 TPTC_SAOPT Register (Offset = 240h) [reset = 0h]

Src Actv Set Options.

Return to Summary Table

Table 4-2314. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0240h
EDMA1	52A6 0240h

Figure 4-1133. TPTC_SAOPT Name Register

31	30	29	28	27	26	25	24
RESERVED		DBG_ID		RESERVED			
NONE		R		NONE			
0h		0h		0h			
23	22	21	20	19	18	17	16
RESERVED	TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE	R	NONE	R	NONE		R	
0h	0h	0h	0h	0h		0h	
15	14	13	12	11	10	9	8
TCC				RESERVED	FWID		
R				NONE	R		
0h				0h	0h		
7	6	5	4	3	2	1	0
RESERVED	PRI			RESERVED		DAM	SAM
NONE	R			NONE		R	R
0h	0h			0h		0h	0h

Table 4-2315. TPTC_SAOPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:28	DBG_ID	R	0h	Debug ID Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus. Used at system level for trace/profiling of user selected transfers in systems that include this feature.
27:23	RESERVED	NONE	0h	Reserved
22	TCCHEN	R	0h	Transfer complete chaining enable: 0:Transfer complete chaining is disabled. 1:Transfer complete chaining is enabled.
21	RESERVED	NONE	0h	Reserved
20	TCINTEN	R	0h	Transfer complete interrupt enable: 0:Transfer complete interrupt is disabled. 1:Transfer complete interrupt is enabled.
19:18	RESERVED	NONE	0h	Reserved
17:12	TCC	R	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
11	RESERVED	NONE	0h	Reserved
10:8	FWID	R	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
7	RESERVED	NONE	0h	Reserved

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Table 4-2315. TPTC_SAOPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI	R	0h	Transfer Priority: 0:Priority 0 - Highest priority 1:Priority 1 ... 7:Priority 7 - Lowest priority
3:2	RESERVED	NONE	0h	Reserved
1	DAM	R	0h	Destination Address Mode within an array: 0:INCR Dst addressing within an array increments. 1:FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	R	0h	Source Address Mode within an array: 0:INCR Src addressing within an array increments. 1:FIFO Src addressing within an array wraps around upon reaching FIFO width.

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4.4.2.141 TPTC_SASRC Register

4.4.2.141.1 TPTC_SASRC Register (Offset = 244h) [reset = 0h]

Src Actv Set Src Address.

Return to Summary Table

Table 4-2316. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0244h
EDMA1	52A6 0244h

Figure 4-1134. TPTC_SASRC Name Register

31	30	29	28	27	26	25	24
SADDR							
R							
0h							
23	22	21	20	19	18	17	16
SADDR							
R							
0h							
15	14	13	12	11	10	9	8
SADDR							
R							
0h							
7	6	5	4	3	2	1	0
SADDR							
R							
0h							

Table 4-2317. TPTC_SASRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDR	R	0h	Source address for Source Active Register Set

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4.4.2.142 TPTC_SACNT Register

4.4.2.142.1 TPTC_SACNT Register (Offset = 248h) [reset = 0h]

Src Actv Set A-Count.

Return to Summary Table

Table 4-2318. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0248h
EDMA1	52A6 0248h

Figure 4-1135. TPTC_SACNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	ACNT						
NONE	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACNT							
R							
0h							

Table 4-2319. TPTC_SACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:0	ACNT	R	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

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4.4.2.143 TPTC_SADST Register

4.4.2.143.1 TPTC_SADST Register (Offset = 24Ch) [reset = 0h]

Src Actv Set Dst Address.

Return to Summary Table

Table 4-2320. Instance Table

Instance Name	Physical Address
EDMA0	52A4 024Ch
EDMA1	52A6 024Ch

Figure 4-1136. TPTC_SADST Name Register

31	30	29	28	27	26	25	24
DADDR							
R							
0h							
23	22	21	20	19	18	17	16
DADDR							
R							
0h							
15	14	13	12	11	10	9	8
DADDR							
R							
0h							
7	6	5	4	3	2	1	0
DADDR							
R							
0h							

Table 4-2321. TPTC_SADST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DADDR	R	0h	Destination address for Source Active Register Set

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4.4.2.144 TPTC_SABIDX Register

4.4.2.144.1 TPTC_SABIDX Register (Offset = 250h) [reset = 0h]

Src Actv Set B-Dim Idx.

Return to Summary Table

Table 4-2322. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0250h
EDMA1	52A6 0250h

Figure 4-1137. TPTC_SABIDX Name Register

31	30	29	28	27	26	25	24
DBIDX							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DBIDX							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SBIDX							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SBIDX							
R							
0h							

Table 4-2323. TPTC_SABIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DBIDX	R	0h	Dest B-Idx for Source Active Register Set: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15:0	SBIDX	R	0h	Source B-Idx for Source Active Register Set: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

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4.4.2.145 TPTC_SAMPPRXY Register

4.4.2.145.1 TPTC_SAMPPRXY Register (Offset = 254h) [reset = 0h]

Src Actv Set Mem Protect Proxy.

Return to Summary Table

Table 4-2324. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0254h
EDMA1	52A6 0254h

Figure 4-1138. TPTC_SAMPPRXY Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				R			
0h				0h			

Table 4-2325. TPTC_SAMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	SECURE	R	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	R	0h	Privilege Level: PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register]. The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
7:4	RESERVED	NONE	0h	Reserved

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Table 4-2325. TPTC_SAMPPRXY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PRIVID	R	0h	Privilege ID: PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register]. The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

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4.4.2.146 TPTC_SACNTRLD Register

4.4.2.146.1 TPTC_SACNTRLD Register (Offset = 258h) [reset = 0h]

Src Actv Set Cnt Reload.

Return to Summary Table

Table 4-2326. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0258h
EDMA1	52A6 0258h

Figure 4-1139. TPTC_SACNTRLD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ACNTRLD							
R							
0h							
7	6	5	4	3	2	1	0
ACNTRLD							
R							
0h							

Table 4-2327. TPTC_SACNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ACNTRLD	R	0h	A-Cnt Reload value for Source Active Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT. The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

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4.4.2.147 TPTC_SASRCBREF Register

4.4.2.147.1 TPTC_SASRCBREF Register (Offset = 25Ch) [reset = 0h]

Src Actv Set Src Addr B-Reference.

Return to Summary Table

Table 4-2328. Instance Table

Instance Name	Physical Address
EDMA0	52A4 025Ch
EDMA1	52A6 025Ch

Figure 4-1140. TPTC_SASRCBREF Name Register

31	30	29	28	27	26	25	24
SADDRBREF							
R							
0h							
23	22	21	20	19	18	17	16
SADDRBREF							
R							
0h							
15	14	13	12	11	10	9	8
SADDRBREF							
R							
0h							
7	6	5	4	3	2	1	0
SADDRBREF							
R							
0h							

Table 4-2329. TPTC_SASRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDRBREF	R	0h	Source address reference for Source Active Register Set: Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

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4.4.2.148 TPTC_SADSTBREF Register

4.4.2.148.1 TPTC_SADSTBREF Register (Offset = 260h) [reset = 0h]

Src Actv Set Dst Addr B-Reference.

Return to Summary Table

Table 4-2330. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0260h
EDMA1	52A6 0260h

Figure 4-1141. TPTC_SADSTBREF Name Register

31	30	29	28	27	26	25	24
DADDRBREF							
R							
0h							
23	22	21	20	19	18	17	16
DADDRBREF							
R							
0h							
15	14	13	12	11	10	9	8
DADDRBREF							
R							
0h							
7	6	5	4	3	2	1	0
DADDRBREF							
R							
0h							

Table 4-2331. TPTC_SADSTBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DADDRBREF	R	0h	Dst address reference is not applicable for Src Active Register Set. Reads return 0x0.

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4.4.2.149 TPTC_SABCNT Register

4.4.2.149.1 TPTC_SABCNT Register (Offset = 264h) [reset = 0h]

Src Actv Set B-Count.

Return to Summary Table

Table 4-2332. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0264h
EDMA1	52A6 0264h

Figure 4-1142. TPTC_SABCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
BCNT							
R							
0h							
7	6	5	4	3	2	1	0
BCNT							
R							
0h							

Table 4-2333. TPTC_SABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	BCNT	R	0h	B-Dimension count: Number of arrays to be transferred where each array is ACNT in length. Count Remaining for Src Active Register Set. Represents the amount of data remaining to be read. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each read command is issued. Final value should be 0 when TR is complete.

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4.4.2.150 TPTC_DFCNTRLD Register

4.4.2.150.1 TPTC_DFCNTRLD Register (Offset = 280h) [reset = 0h]

Dst FIFO Set Cnt Reload.

Return to Summary Table

Table 4-2334. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0280h
EDMA1	52A6 0280h

Figure 4-1143. TPTC_DFCNTRLD Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
ACNTRLD							
R							
0h							
7	6	5	4	3	2	1	0
ACNTRLD							
R							
0h							

Table 4-2335. TPTC_DFCNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	ACNTRLD	R	0h	A-Cnt Reload value for Destination FIFO Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT. The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

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4.4.2.151 TPTC_DFSRCBREF Register

4.4.2.151.1 TPTC_DFSRCBREF Register (Offset = 284h) [reset = 0h]

Dst FIFO Set Src Addr B-Reference.

Return to Summary Table

Table 4-2336. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0284h
EDMA1	52A6 0284h

Figure 4-1144. TPTC_DFSRCBREF Name Register

31	30	29	28	27	26	25	24
SADDRBREF							
R							
0h							
23	22	21	20	19	18	17	16
SADDRBREF							
R							
0h							
15	14	13	12	11	10	9	8
SADDRBREF							
R							
0h							
7	6	5	4	3	2	1	0
SADDRBREF							
R							
0h							

Table 4-2337. TPTC_DFSRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDRBREF	R	0h	Source address reference for Destination FIFO Register Set: Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

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4.4.2.152 TPTC_DFOPT0 Register

4.4.2.152.1 TPTC_DFOPT0 Register (Offset = 300h) [reset = 0h]

Dst FIFO Set Options.

Return to Summary Table

Table 4-2338. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0300h
EDMA1	52A6 0300h

Figure 4-1145. TPTC_DFOPT0 Name Register

31	30	29	28	27	26	25	24
RESERVED		DBG_ID		RESERVED			
NONE		R		NONE			
0h		0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE	R	NONE	R	NONE		R	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TCC				RESERVED	FWID		
R				NONE	R		
0h				0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI			RESERVED		DAM	SAM
NONE	R			NONE		R	R
0h	0h			0h		0h	0h

Table 4-2339. TPTC_DFOPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:28	DBG_ID	R	0h	Debug ID Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus. Used at system level for trace/profiling of user selected transfers in systems that include this feature.
27:23	RESERVED	NONE	0h	Reserved
22	TCCHEN	R	0h	Transfer complete chaining enable: 0:Transfer complete chaining is disabled. 1:Transfer complete chaining is enabled.
21	RESERVED	NONE	0h	Reserved
20	TCINTEN	R	0h	Transfer complete interrupt enable: 0:Transfer complete interrupt is disabled. 1:Transfer complete interrupt is enabled.
19:18	RESERVED	NONE	0h	Reserved
17:12	TCC	R	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
11	RESERVED	NONE	0h	Reserved
10:8	FWID	R	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
7	RESERVED	NONE	0h	Reserved

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Table 4-2339. TPTC_DFOPT0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI	R	0h	Transfer Priority: 0:Priority 0 - Highest priority 1:Priority 1 ... 7:Priority 7 - Lowest priority
3:2	RESERVED	NONE	0h	Reserved
1	DAM	R	0h	Destination Address Mode within an array: 0:INCR Dst addressing within an array increments. 1:FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	R	0h	Source Address Mode within an array: 0:INCR Src addressing within an array increments. 1:FIFO Src addressing within an array wraps around upon reaching FIFO width.

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4.4.2.153 TPTC_DFSRC0 Register

4.4.2.153.1 TPTC_DFSRC0 Register (Offset = 304h) [reset = 0h]

Dst FIFO Set Src Address.

Return to Summary Table

Table 4-2340. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0304h
EDMA1	52A6 0304h

Figure 4-1146. TPTC_DFSRC0 Name Register

31	30	29	28	27	26	25	24
SADDR							
R							
0h							
23	22	21	20	19	18	17	16
SADDR							
R							
0h							
15	14	13	12	11	10	9	8
SADDR							
R							
0h							
7	6	5	4	3	2	1	0
SADDR							
R							
0h							

Table 4-2341. TPTC_DFSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDR	R	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

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4.4.2.154 TPTC_DFACNT0 Register

4.4.2.154.1 TPTC_DFACNT0 Register (Offset = 308h) [reset = 0h]

Dst FIFO Set A-Count.

Return to Summary Table

Table 4-2342. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0308h
EDMA1	52A6 0308h

Figure 4-1147. TPTC_DFACNT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED	ACNT						
NONE	R						
0h	0h						
15	14	13	12	11	10	9	8
ACNT							
R							
0h							
7	6	5	4	3	2	1	0
ACNT							
R							
0h							

Table 4-2343. TPTC_DFACNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:0	ACNT	R	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

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4.4.2.155 TPTC_DFDST0 Register

4.4.2.155.1 TPTC_DFDST0 Register (Offset = 30Ch) [reset = 0h]

Dst FIFO Set Dst Address.

Return to Summary Table

Table 4-2344. Instance Table

Instance Name	Physical Address
EDMA0	52A4 030Ch
EDMA1	52A6 030Ch

Figure 4-1148. TPTC_DFDST0 Name Register

31	30	29	28	27	26	25	24
DADDR							
R							
0h							
23	22	21	20	19	18	17	16
DADDR							
R							
0h							
15	14	13	12	11	10	9	8
DADDR							
R							
0h							
7	6	5	4	3	2	1	0
DADDR							
R							
0h							

Table 4-2345. TPTC_DFDST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DADDR	R	0h	Destination address for Dst FIFO Register Set: Initial value is copied from PDST.DADDR. TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued. When a TR is complete the final value should be the address of the last write command issued.

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4.4.2.156 TPTC_DFBIDX0 Register

4.4.2.156.1 TPTC_DFBIDX0 Register (Offset = 310h) [reset = 0h]

Dst FIFO Set B-Dim Idx.

Return to Summary Table

Table 4-2346. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0310h
EDMA1	52A6 0310h

Figure 4-1149. TPTC_DFBIDX0 Name Register

31	30	29	28	27	26	25	24
DBIDX							
R							
0h							
23	22	21	20	19	18	17	16
DBIDX							
R							
0h							
15	14	13	12	11	10	9	8
SBIDX							
R							
0h							
7	6	5	4	3	2	1	0
SBIDX							
R							
0h							

Table 4-2347. TPTC_DFBIDX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DBIDX	R	0h	Dest B-Idx for Dest FIFO Register Set. Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15:0	SBIDX	R	0h	Src B-Idx for Dest FIFO Register Set. Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

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4.4.2.157 TPTC_DFMPPRXY0 Register

4.4.2.157.1 TPTC_DFMPPRXY0 Register (Offset = 314h) [reset = 0h]

Dst FIFO Set Mem Protect Proxy.

Return to Summary Table

Table 4-2348. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0314h
EDMA1	52A6 0314h

Figure 4-1150. TPTC_DFMPPRXY0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						SECURE	PRIV
NONE						R	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PRIVID			
NONE				R			
0h				0h			

Table 4-2349. TPTC_DFMPPRXY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	SECURE	R	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	R	0h	Privilege Level: PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register]. The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
7:4	RESERVED	NONE	0h	Reserved

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Table 4-2349. TPTC_DFMPPRXY0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PRIVID	R	0h	Privilege ID: PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register]. The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

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4.4.2.158 TPTC_DFBCNT0 Register

4.4.2.158.1 TPTC_DFBCNT0 Register (Offset = 318h) [reset = 0h]

Dst FIFO Set B-Count.

Return to Summary Table

Table 4-2350. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0318h
EDMA1	52A6 0318h

Figure 4-1151. TPTC_DFBCNT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
BCNT							
R							
0h							
7	6	5	4	3	2	1	0
BCNT							
R							
0h							

Table 4-2351. TPTC_DFBCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	BCNT	R	0h	B-Count Remaining for Dst Register Set: Number of arrays to be transferred where each array is ACNT in length. Represents the amount of data remaining to be written. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

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4.4.2.159 TPTC_DFOPT1 Register

4.4.2.159.1 TPTC_DFOPT1 Register (Offset = 340h) [reset = 0h]

Dst FIFO Set Options.

Return to Summary Table

Table 4-2352. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0340h
EDMA1	52A6 0340h

Figure 4-1152. TPTC_DFOPT1 Name Register

31	30	29	28	27	26	25	24
RESERVED		DBG_ID		RESERVED			
NONE		R		NONE			
0h		0h		0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	TCCHEN	RESERVED	TCINTEN	RESERVED		TCC	
NONE	R	NONE	R	NONE		R	
0h	0h	0h	0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TCC				RESERVED	FWID		
R				NONE	R		
0h				0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI			RESERVED		DAM	SAM
NONE	R			NONE		R	R
0h	0h			0h		0h	0h

Table 4-2353. TPTC_DFOPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:28	DBG_ID	R	0h	Debug ID Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus. Used at system level for trace/profiling of user selected transfers in systems that include this feature.
27:23	RESERVED	NONE	0h	Reserved
22	TCCHEN	R	0h	Transfer complete chaining enable: 0:Transfer complete chaining is disabled. 1:Transfer complete chaining is enabled.
21	RESERVED	NONE	0h	Reserved
20	TCINTEN	R	0h	Transfer complete interrupt enable: 0:Transfer complete interrupt is disabled. 1:Transfer complete interrupt is enabled.
19:18	RESERVED	NONE	0h	Reserved
17:12	TCC	R	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
11	RESERVED	NONE	0h	Reserved
10:8	FWID	R	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
7	RESERVED	NONE	0h	Reserved

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Table 4-2353. TPTC_DFOPT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	PRI	R	0h	Transfer Priority: 0:Priority 0 - Highest priority 1:Priority 1 ... 7:Priority 7 - Lowest priority
3:2	RESERVED	NONE	0h	Reserved
1	DAM	R	0h	Destination Address Mode within an array: 0:INCR Dst addressing within an array increments. 1:FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	R	0h	Source Address Mode within an array: 0:INCR Src addressing within an array increments. 1:FIFO Src addressing within an array wraps around upon reaching FIFO width.

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4.4.2.160 TPTC_DFSRC1 Register

4.4.2.160.1 TPTC_DFSRC1 Register (Offset = 344h) [reset = 0h]

Dst FIFO Set Src Address.

Return to Summary Table

Table 4-2354. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0344h
EDMA1	52A6 0344h

Figure 4-1153. TPTC_DFSRC1 Name Register

31	30	29	28	27	26	25	24
SADDR							
R							
0h							
23	22	21	20	19	18	17	16
SADDR							
R							
0h							
15	14	13	12	11	10	9	8
SADDR							
R							
0h							
7	6	5	4	3	2	1	0
SADDR							
R							
0h							

Table 4-2355. TPTC_DFSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SADDR	R	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

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4.4.2.161 TPTC_DFACNT1 Register

4.4.2.161.1 TPTC_DFACNT1 Register (Offset = 348h) [reset = 0h]

Dst FIFO Set A-Count.

Return to Summary Table

Table 4-2356. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0348h
EDMA1	52A6 0348h

Figure 4-1154. TPTC_DFACNT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	ACNT						
NONE	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACNT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACNT							
R							
0h							

Table 4-2357. TPTC_DFACNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	RESERVED	NONE	0h	Reserved
22:0	ACNT	R	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

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4.4.2.162 TPTC_DFDST1 Register

4.4.2.162.1 TPTC_DFDST1 Register (Offset = 34Ch) [reset = 0h]

Dst FIFO Set Dst Address.

Return to Summary Table

Table 4-2358. Instance Table

Instance Name	Physical Address
EDMA0	52A4 034Ch
EDMA1	52A6 034Ch

Figure 4-1155. TPTC_DFDST1 Name Register

31	30	29	28	27	26	25	24
DADDR							
R							
0h							
23	22	21	20	19	18	17	16
DADDR							
R							
0h							
15	14	13	12	11	10	9	8
DADDR							
R							
0h							
7	6	5	4	3	2	1	0
DADDR							
R							
0h							

Table 4-2359. TPTC_DFDST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DADDR	R	0h	Destination address for Dst FIFO Register Set: Initial value is copied from PDST.DADDR. TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued. When a TR is complete the final value should be the address of the last write command issued.

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4.4.2.163 TPTC_DFBIDX1 Register

4.4.2.163.1 TPTC_DFBIDX1 Register (Offset = 350h) [reset = 0h]

Dst FIFO Set B-Dim Idx.

Return to Summary Table

Table 4-2360. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0350h
EDMA1	52A6 0350h

Figure 4-1156. TPTC_DFBIDX1 Name Register

31	30	29	28	27	26	25	24
DBIDX							
R							
0h							
23	22	21	20	19	18	17	16
DBIDX							
R							
0h							
15	14	13	12	11	10	9	8
SBIDX							
R							
0h							
7	6	5	4	3	2	1	0
SBIDX							
R							
0h							

Table 4-2361. TPTC_DFBIDX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DBIDX	R	0h	Dest B-Idx for Dest FIFO Register Set. Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15:0	SBIDX	R	0h	Src B-Idx for Dest FIFO Register Set. Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

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4.4.2.164 TPTC_DFMPPRXY1 Register

4.4.2.164.1 TPTC_DFMPPRXY1 Register (Offset = 354h) [reset = 0h]

Dst FIFO Set Mem Protect Proxy.

Return to Summary Table

Table 4-2362. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0354h
EDMA1	52A6 0354h

Figure 4-1157. TPTC_DFMPPRXY1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						SECURE	PRIV
NONE						R	R
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED				PRIVID			
NONE				R			
0h				0h			

Table 4-2363. TPTC_DFMPPRXY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	SECURE	R	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	R	0h	Privilege Level: PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register]. The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
7:4	RESERVED	NONE	0h	Reserved

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Table 4-2363. TPTC_DFMPPRXY1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	PRIVID	R	0h	Privilege ID: PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register]. The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

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4.4.2.165 TPTC_DFBCNT1 Register

4.4.2.165.1 TPTC_DFBCNT1 Register (Offset = 358h) [reset = 0h]

Dst FIFO Set B-Count.

Return to Summary Table

Table 4-2364. Instance Table

Instance Name	Physical Address
EDMA0	52A4 0358h
EDMA1	52A6 0358h

Figure 4-1158. TPTC_DFBCNT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
BCNT							
R							
0h							
7	6	5	4	3	2	1	0
BCNT							
R							
0h							

Table 4-2365. TPTC_DFBCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	BCNT	R	0h	B-Count Remaining for Dst Register Set: Number of arrays to be transferred where each array is ACNT in length. Represents the amount of data remaining to be written. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

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4.5 EDMA_TRIGXBAR_INTR

EDMA_TRIGXBAR_INTR

4.5.1 EDMA_TRIGXBAR_INTR Summaries

EDMA_TRIGXBAR_INTR Summaries

Table 4-2366. EDMA_TRIGXBAR_INTR Registers, Base Address=52E0 1000h, Length=512

Offset	Length	Register Name	EDMA_TRIGXBAR_INTR Physical Address
0h	32	EDMA_TRIGXBAR_INTR_PID	52E0 1000h
4h	32	EDMA_TRIGXBAR_INTR_MUXCNTL_J	52E0 1004h + formula

4.5.2 EDMA_TRIGXBAR_INTR Registers

EDMA_TRIGXBAR_INTR Registers

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4.5.2.1 EDMA_TRIGXBAR_INTR_PID Register

4.5.2.1.1 EDMA_TRIGXBAR_INTR_PID Register (Offset = 0h) [reset = 66948100h]

Identification register.

Return to Summary Table

Table 4-2367. Instance Table

Instance Name	Physical Address
EDMA_TRIGXBAR_INTR	52E0 1000h

Figure 4-1159. EDMA_TRIGXBAR_INTR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
694h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTLVER					MAJREV		
R					R		
10h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINREV					
R		R					
0h		0h					

Table 4-2368. EDMA_TRIGXBAR_INTR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	FUNCTION	R	694h	function
15:11	RTLVER	R	10h	Rtl version
10:8	MAJREV	R	1h	major version
7:6	CUSTOM	R	0h	custom id
5:0	MINREV	R	0h	minor version

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4.5.2.2 EDMA_TRIGXBAR_INTR_MUXCNTL_J Register

4.5.2.2.1 EDMA_TRIGXBAR_INTR_MUXCNTL_J Register (Offset = 4h) [reset = 0h]

Interrupt mux control register.

Return to Summary Table

Table 4-2369. Instance Table

Instance Name	Physical Address
EDMA_TRIGXBAR_INTR	52E0 1004h + formula

Figure 4-1160. EDMA_TRIGXBAR_INTR_MUXCNTL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							INT_ENABLE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							MUX_CNTL
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
MUX_CNTL							
R/W							
0h							

Table 4-2370. EDMA_TRIGXBAR_INTR_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	Interrupt *j* Output Enable.
15:9	RESERVED	NONE	0h	Reserved
8:0	MUX_CNTL	R/W	0h	Mux Control for Interrupt *j*.

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4.6 CONTROLSS_DMAXBAR

CONTROLSS_DMAXBAR

4.6.1 CONTROLSS_DMAXBAR Summaries

CONTROLSS_DMAXBAR Summaries

Table 4-2371. CONTROLSS Registers, Base Address=502D 6000h, Length=1024

Offset	Length	Register Name	CONTROLSS_DMAXBAR Physical Address
100h	32	CONTROLSS_DMAXBAR0_GSEL	502D 6100h
104h	32	CONTROLSS_DMAXBAR0_G0	502D 6104h
108h	32	CONTROLSS_DMAXBAR0_G1	502D 6108h
10Ch	32	CONTROLSS_DMAXBAR0_G2	502D 610Ch
110h	32	CONTROLSS_DMAXBAR0_G3	502D 6110h
114h	32	CONTROLSS_DMAXBAR0_G4	502D 6114h
118h	32	CONTROLSS_DMAXBAR0_G5	502D 6118h
11Ch	32	CONTROLSS_DMAXBAR0_G6	502D 611Ch
140h	32	CONTROLSS_DMAXBAR1_GSEL	502D 6140h
144h	32	CONTROLSS_DMAXBAR1_G0	502D 6144h
148h	32	CONTROLSS_DMAXBAR1_G1	502D 6148h
14Ch	32	CONTROLSS_DMAXBAR1_G2	502D 614Ch
150h	32	CONTROLSS_DMAXBAR1_G3	502D 6150h
154h	32	CONTROLSS_DMAXBAR1_G4	502D 6154h
158h	32	CONTROLSS_DMAXBAR1_G5	502D 6158h
15Ch	32	CONTROLSS_DMAXBAR1_G6	502D 615Ch
180h	32	CONTROLSS_DMAXBAR2_GSEL	502D 6180h
184h	32	CONTROLSS_DMAXBAR2_G0	502D 6184h
188h	32	CONTROLSS_DMAXBAR2_G1	502D 6188h
18Ch	32	CONTROLSS_DMAXBAR2_G2	502D 618Ch
190h	32	CONTROLSS_DMAXBAR2_G3	502D 6190h
194h	32	CONTROLSS_DMAXBAR2_G4	502D 6194h
198h	32	CONTROLSS_DMAXBAR2_G5	502D 6198h
19Ch	32	CONTROLSS_DMAXBAR2_G6	502D 619Ch
1C0h	32	CONTROLSS_DMAXBAR3_GSEL	502D 61C0h
1C4h	32	CONTROLSS_DMAXBAR3_G0	502D 61C4h
1C8h	32	CONTROLSS_DMAXBAR3_G1	502D 61C8h
1CCh	32	CONTROLSS_DMAXBAR3_G2	502D 61CCh
1D0h	32	CONTROLSS_DMAXBAR3_G3	502D 61D0h
1D4h	32	CONTROLSS_DMAXBAR3_G4	502D 61D4h
1D8h	32	CONTROLSS_DMAXBAR3_G5	502D 61D8h
1DCh	32	CONTROLSS_DMAXBAR3_G6	502D 61DCh
200h	32	CONTROLSS_DMAXBAR4_GSEL	502D 6200h
204h	32	CONTROLSS_DMAXBAR4_G0	502D 6204h
208h	32	CONTROLSS_DMAXBAR4_G1	502D 6208h
20Ch	32	CONTROLSS_DMAXBAR4_G2	502D 620Ch
210h	32	CONTROLSS_DMAXBAR4_G3	502D 6210h
214h	32	CONTROLSS_DMAXBAR4_G4	502D 6214h
218h	32	CONTROLSS_DMAXBAR4_G5	502D 6218h

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Table 4-2371. CONTROLSS Registers, Base Address=502D 6000h, Length=1024 (continued)

Offset	Length	Register Name	CONTROLSS_DMAXBAR Physical Address
21Ch	32	CONTROLSS_DMAXBAR4_G6	502D 621Ch
240h	32	CONTROLSS_DMAXBAR5_GSEL	502D 6240h
244h	32	CONTROLSS_DMAXBAR5_G0	502D 6244h
248h	32	CONTROLSS_DMAXBAR5_G1	502D 6248h
24Ch	32	CONTROLSS_DMAXBAR5_G2	502D 624Ch
250h	32	CONTROLSS_DMAXBAR5_G3	502D 6250h
254h	32	CONTROLSS_DMAXBAR5_G4	502D 6254h
258h	32	CONTROLSS_DMAXBAR5_G5	502D 6258h
25Ch	32	CONTROLSS_DMAXBAR5_G6	502D 625Ch
280h	32	CONTROLSS_DMAXBAR6_GSEL	502D 6280h
284h	32	CONTROLSS_DMAXBAR6_G0	502D 6284h
288h	32	CONTROLSS_DMAXBAR6_G1	502D 6288h
28Ch	32	CONTROLSS_DMAXBAR6_G2	502D 628Ch
290h	32	CONTROLSS_DMAXBAR6_G3	502D 6290h
294h	32	CONTROLSS_DMAXBAR6_G4	502D 6294h
298h	32	CONTROLSS_DMAXBAR6_G5	502D 6298h
29Ch	32	CONTROLSS_DMAXBAR6_G6	502D 629Ch
2C0h	32	CONTROLSS_DMAXBAR7_GSEL	502D 62C0h
2C4h	32	CONTROLSS_DMAXBAR7_G0	502D 62C4h
2C8h	32	CONTROLSS_DMAXBAR7_G1	502D 62C8h
2CCh	32	CONTROLSS_DMAXBAR7_G2	502D 62CCh
2D0h	32	CONTROLSS_DMAXBAR7_G3	502D 62D0h
2D4h	32	CONTROLSS_DMAXBAR7_G4	502D 62D4h
2D8h	32	CONTROLSS_DMAXBAR7_G5	502D 62D8h
2DCh	32	CONTROLSS_DMAXBAR7_G6	502D 62DCh
300h	32	CONTROLSS_DMAXBAR8_GSEL	502D 6300h
304h	32	CONTROLSS_DMAXBAR8_G0	502D 6304h
308h	32	CONTROLSS_DMAXBAR8_G1	502D 6308h
30Ch	32	CONTROLSS_DMAXBAR8_G2	502D 630Ch
310h	32	CONTROLSS_DMAXBAR8_G3	502D 6310h
314h	32	CONTROLSS_DMAXBAR8_G4	502D 6314h
318h	32	CONTROLSS_DMAXBAR8_G5	502D 6318h
31Ch	32	CONTROLSS_DMAXBAR8_G6	502D 631Ch
340h	32	CONTROLSS_DMAXBAR9_GSEL	502D 6340h
344h	32	CONTROLSS_DMAXBAR9_G0	502D 6344h
348h	32	CONTROLSS_DMAXBAR9_G1	502D 6348h
34Ch	32	CONTROLSS_DMAXBAR9_G2	502D 634Ch
350h	32	CONTROLSS_DMAXBAR9_G3	502D 6350h
354h	32	CONTROLSS_DMAXBAR9_G4	502D 6354h
358h	32	CONTROLSS_DMAXBAR9_G5	502D 6358h
35Ch	32	CONTROLSS_DMAXBAR9_G6	502D 635Ch
380h	32	CONTROLSS_DMAXBAR10_GSEL	502D 6380h
384h	32	CONTROLSS_DMAXBAR10_G0	502D 6384h
388h	32	CONTROLSS_DMAXBAR10_G1	502D 6388h
38Ch	32	CONTROLSS_DMAXBAR10_G2	502D 638Ch
390h	32	CONTROLSS_DMAXBAR10_G3	502D 6390h

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Table 4-2371. CONTROLSS Registers, Base Address=502D 6000h, Length=1024 (continued)

Offset	Length	Register Name	CONTROLSS_DMAXBAR Physical Address
394h	32	CONTROLSS_DMAXBAR10_G4	502D 6394h
398h	32	CONTROLSS_DMAXBAR10_G5	502D 6398h
39Ch	32	CONTROLSS_DMAXBAR10_G6	502D 639Ch
3C0h	32	CONTROLSS_DMAXBAR11_GSEL	502D 63C0h
3C4h	32	CONTROLSS_DMAXBAR11_G0	502D 63C4h
3C8h	32	CONTROLSS_DMAXBAR11_G1	502D 63C8h
3CCh	32	CONTROLSS_DMAXBAR11_G2	502D 63CCh
3D0h	32	CONTROLSS_DMAXBAR11_G3	502D 63D0h
3D4h	32	CONTROLSS_DMAXBAR11_G4	502D 63D4h
3D8h	32	CONTROLSS_DMAXBAR11_G5	502D 63D8h
3DCh	32	CONTROLSS_DMAXBAR11_G6	502D 63DCh
400h	32	CONTROLSS_DMAXBAR12_GSEL	502D 6400h
404h	32	CONTROLSS_DMAXBAR12_G0	502D 6404h
408h	32	CONTROLSS_DMAXBAR12_G1	502D 6408h
40Ch	32	CONTROLSS_DMAXBAR12_G2	502D 640Ch
410h	32	CONTROLSS_DMAXBAR12_G3	502D 6410h
414h	32	CONTROLSS_DMAXBAR12_G4	502D 6414h
418h	32	CONTROLSS_DMAXBAR12_G5	502D 6418h
41Ch	32	CONTROLSS_DMAXBAR12_G6	502D 641Ch
440h	32	CONTROLSS_DMAXBAR13_GSEL	502D 6440h
444h	32	CONTROLSS_DMAXBAR13_G0	502D 6444h
448h	32	CONTROLSS_DMAXBAR13_G1	502D 6448h
44Ch	32	CONTROLSS_DMAXBAR13_G2	502D 644Ch
450h	32	CONTROLSS_DMAXBAR13_G3	502D 6450h
454h	32	CONTROLSS_DMAXBAR13_G4	502D 6454h
458h	32	CONTROLSS_DMAXBAR13_G5	502D 6458h
45Ch	32	CONTROLSS_DMAXBAR13_G6	502D 645Ch
480h	32	CONTROLSS_DMAXBAR14_GSEL	502D 6480h
484h	32	CONTROLSS_DMAXBAR14_G0	502D 6484h
488h	32	CONTROLSS_DMAXBAR14_G1	502D 6488h
48Ch	32	CONTROLSS_DMAXBAR14_G2	502D 648Ch
490h	32	CONTROLSS_DMAXBAR14_G3	502D 6490h
494h	32	CONTROLSS_DMAXBAR14_G4	502D 6494h
498h	32	CONTROLSS_DMAXBAR14_G5	502D 6498h
49Ch	32	CONTROLSS_DMAXBAR14_G6	502D 649Ch
4C0h	32	CONTROLSS_DMAXBAR15_GSEL	502D 64C0h
4C4h	32	CONTROLSS_DMAXBAR15_G0	502D 64C4h
4C8h	32	CONTROLSS_DMAXBAR15_G1	502D 64C8h
4CCh	32	CONTROLSS_DMAXBAR15_G2	502D 64CCh
4D0h	32	CONTROLSS_DMAXBAR15_G3	502D 64D0h
4D4h	32	CONTROLSS_DMAXBAR15_G4	502D 64D4h
4D8h	32	CONTROLSS_DMAXBAR15_G5	502D 64D8h
4DCh	32	CONTROLSS_DMAXBAR15_G6	502D 64DCh

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4.6.2 CONTROLSS_DMAXBAR Registers

CONTROLSS_DMAXBAR Registers

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4.6.2.1 CONTROLSS_DMAXBAR0_GSEL Register

4.6.2.1.1 CONTROLSS_DMAXBAR0_GSEL Register (Offset = 100h) [reset = 0h]

DMA XBAR0 Input Select.

Return to Summary Table

Table 4-2372. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6100h

Figure 4-1161. CONTROLSS_DMAXBAR0_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR0_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2373. CONTROLSS_DMAXBAR0_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR0_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.2 CONTROLSS_DMAXBAR0_G0 Register

4.6.2.2.1 CONTROLSS_DMAXBAR0_G0 Register (Offset = 104h) [reset = 0h]

DMA XBAR0 Input Select.

Return to Summary Table

Table 4-2374. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6104h

Figure 4-1162. CONTROLSS_DMAXBAR0_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR0_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2375. CONTROLSS_DMAXBAR0_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR0_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.3 CONTROLSS_DMAXBAR0_G1 Register

4.6.2.3.1 CONTROLSS_DMAXBAR0_G1 Register (Offset = 108h) [reset = 0h]

DMA XBAR0 Input Select.

Return to Summary Table

Table 4-2376. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6108h

Figure 4-1163. CONTROLSS_DMAXBAR0_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR0_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2377. CONTROLSS_DMAXBAR0_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR0_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.4 CONTROLSS_DMAXBAR0_G2 Register

4.6.2.4.1 CONTROLSS_DMAXBAR0_G2 Register (Offset = 10Ch) [reset = 0h]

DMA XBAR0 Input Select.

Return to Summary Table

Table 4-2378. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 610Ch

Figure 4-1164. CONTROLSS_DMAXBAR0_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR0_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2379. CONTROLSS_DMAXBAR0_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR0_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.5 CONTROLSS_DMAXBAR0_G3 Register

4.6.2.5.1 CONTROLSS_DMAXBAR0_G3 Register (Offset = 110h) [reset = 0h]

DMA XBAR0 Input Select.

Return to Summary Table

Table 4-2380. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6110h

Figure 4-1165. CONTROLSS_DMAXBAR0_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR0_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2381. CONTROLSS_DMAXBAR0_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR0_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.6 CONTROLSS_DMAXBAR0_G4 Register

4.6.2.6.1 CONTROLSS_DMAXBAR0_G4 Register (Offset = 114h) [reset = 0h]

DMA XBAR0 Input Select.

Return to Summary Table

Table 4-2382. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6114h

Figure 4-1166. CONTROLSS_DMAXBAR0_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR0_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2383. CONTROLSS_DMAXBAR0_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR0_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.7 CONTROLSS_DMAXBAR0_G5 Register

4.6.2.7.1 CONTROLSS_DMAXBAR0_G5 Register (Offset = 118h) [reset = 0h]

DMA XBAR0 Input Select.

Return to Summary Table

Table 4-2384. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6118h

Figure 4-1167. CONTROLSS_DMAXBAR0_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DMAXBAR0_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2385. CONTROLSS_DMAXBAR0_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR0_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.8 CONTROLSS_DMAXBAR0_G6 Register

4.6.2.8.1 CONTROLSS_DMAXBAR0_G6 Register (Offset = 11Ch) [reset = 0h]

DMA XBAR0 Input Select.

Return to Summary Table

Table 4-2386. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 611Ch

Figure 4-1168. CONTROLSS_DMAXBAR0_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR0_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2387. CONTROLSS_DMAXBAR0_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR0_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.9 CONTROLSS_DMAXBAR1_GSEL Register

4.6.2.9.1 CONTROLSS_DMAXBAR1_GSEL Register (Offset = 140h) [reset = 0h]

DMA XBAR1 Input Select.

Return to Summary Table

Table 4-2388. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6140h

Figure 4-1169. CONTROLSS_DMAXBAR1_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR1_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2389. CONTROLSS_DMAXBAR1_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR1_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.10 CONTROLSS_DMAXBAR1_G0 Register

4.6.2.10.1 CONTROLSS_DMAXBAR1_G0 Register (Offset = 144h) [reset = 0h]

DMA XBAR1 Input Select.

Return to Summary Table

Table 4-2390. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6144h

Figure 4-1170. CONTROLSS_DMAXBAR1_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR1_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2391. CONTROLSS_DMAXBAR1_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR1_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.11 CONTROLSS_DMAXBAR1_G1 Register

4.6.2.11.1 CONTROLSS_DMAXBAR1_G1 Register (Offset = 148h) [reset = 0h]

DMA XBAR1 Input Select.

Return to Summary Table

Table 4-2392. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6148h

Figure 4-1171. CONTROLSS_DMAXBAR1_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR1_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2393. CONTROLSS_DMAXBAR1_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR1_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.12 CONTROLSS_DMAXBAR1_G2 Register

4.6.2.12.1 CONTROLSS_DMAXBAR1_G2 Register (Offset = 14Ch) [reset = 0h]

DMA XBAR1 Input Select.

Return to Summary Table

Table 4-2394. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 614Ch

Figure 4-1172. CONTROLSS_DMAXBAR1_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR1_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2395. CONTROLSS_DMAXBAR1_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR1_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.13 CONTROLSS_DMAXBAR1_G3 Register

4.6.2.13.1 CONTROLSS_DMAXBAR1_G3 Register (Offset = 150h) [reset = 0h]

DMA XBAR1 Input Select.

Return to Summary Table

Table 4-2396. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6150h

Figure 4-1173. CONTROLSS_DMAXBAR1_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DMAXBAR1_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2397. CONTROLSS_DMAXBAR1_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR1_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.14 CONTROLSS_DMAXBAR1_G4 Register

4.6.2.14.1 CONTROLSS_DMAXBAR1_G4 Register (Offset = 154h) [reset = 0h]

DMA XBAR1 Input Select.

Return to Summary Table

Table 4-2398. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6154h

Figure 4-1174. CONTROLSS_DMAXBAR1_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR1_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2399. CONTROLSS_DMAXBAR1_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR1_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.15 CONTROLSS_DMAXBAR1_G5 Register

4.6.2.15.1 CONTROLSS_DMAXBAR1_G5 Register (Offset = 158h) [reset = 0h]

DMA XBAR1 Input Select.

Return to Summary Table

Table 4-2400. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6158h

Figure 4-1175. CONTROLSS_DMAXBAR1_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR1_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2401. CONTROLSS_DMAXBAR1_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR1_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.16 CONTROLSS_DMAXBAR1_G6 Register

4.6.2.16.1 CONTROLSS_DMAXBAR1_G6 Register (Offset = 15Ch) [reset = 0h]

DMA XBAR1 Input Select.

Return to Summary Table

Table 4-2402. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 615Ch

Figure 4-1176. CONTROLSS_DMAXBAR1_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR1_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2403. CONTROLSS_DMAXBAR1_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR1_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.17 CONTROLSS_DMAXBAR2_GSEL Register

4.6.2.17.1 CONTROLSS_DMAXBAR2_GSEL Register (Offset = 180h) [reset = 0h]

DMA XBAR2 Input Select.

Return to Summary Table

Table 4-2404. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6180h

Figure 4-1177. CONTROLSS_DMAXBAR2_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR2_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2405. CONTROLSS_DMAXBAR2_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR2_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.18 CONTROLSS_DMAXBAR2_G0 Register

4.6.2.18.1 CONTROLSS_DMAXBAR2_G0 Register (Offset = 184h) [reset = 0h]

DMA XBAR2 Input Select.

Return to Summary Table

Table 4-2406. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6184h

Figure 4-1178. CONTROLSS_DMAXBAR2_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR2_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2407. CONTROLSS_DMAXBAR2_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR2_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.19 CONTROLSS_DMAXBAR2_G1 Register

4.6.2.19.1 CONTROLSS_DMAXBAR2_G1 Register (Offset = 188h) [reset = 0h]

DMA XBAR2 Input Select.

Return to Summary Table

Table 4-2408. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6188h

Figure 4-1179. CONTROLSS_DMAXBAR2_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR2_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2409. CONTROLSS_DMAXBAR2_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR2_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.20 CONTROLSS_DMAXBAR2_G2 Register

4.6.2.20.1 CONTROLSS_DMAXBAR2_G2 Register (Offset = 18Ch) [reset = 0h]

DMA XBAR2 Input Select.

Return to Summary Table

Table 4-2410. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 618Ch

Figure 4-1180. CONTROLSS_DMAXBAR2_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR2_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2411. CONTROLSS_DMAXBAR2_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR2_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.21 CONTROLSS_DMAXBAR2_G3 Register

4.6.2.21.1 CONTROLSS_DMAXBAR2_G3 Register (Offset = 190h) [reset = 0h]

DMA XBAR2 Input Select.

Return to Summary Table

Table 4-2412. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6190h

Figure 4-1181. CONTROLSS_DMAXBAR2_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR2_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2413. CONTROLSS_DMAXBAR2_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR2_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.22 CONTROLSS_DMAXBAR2_G4 Register

4.6.2.22.1 CONTROLSS_DMAXBAR2_G4 Register (Offset = 194h) [reset = 0h]

DMA XBAR2 Input Select.

Return to Summary Table

Table 4-2414. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6194h

Figure 4-1182. CONTROLSS_DMAXBAR2_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR2_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2415. CONTROLSS_DMAXBAR2_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR2_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.23 CONTROLSS_DMAXBAR2_G5 Register

4.6.2.23.1 CONTROLSS_DMAXBAR2_G5 Register (Offset = 198h) [reset = 0h]

DMA XBAR2 Input Select.

Return to Summary Table

Table 4-2416. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6198h

Figure 4-1183. CONTROLSS_DMAXBAR2_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR2_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2417. CONTROLSS_DMAXBAR2_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR2_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.24 CONTROLSS_DMAXBAR2_G6 Register

4.6.2.24.1 CONTROLSS_DMAXBAR2_G6 Register (Offset = 19Ch) [reset = 0h]

DMA XBAR2 Input Select.

Return to Summary Table

Table 4-2418. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 619Ch

Figure 4-1184. CONTROLSS_DMAXBAR2_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR2_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2419. CONTROLSS_DMAXBAR2_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR2_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.25 CONTROLSS_DMAXBAR3_GSEL Register

4.6.2.25.1 CONTROLSS_DMAXBAR3_GSEL Register (Offset = 1C0h) [reset = 0h]

DMA XBAR3 Input Select.

Return to Summary Table

Table 4-2420. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61C0h

Figure 4-1185. CONTROLSS_DMAXBAR3_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR3_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2421. CONTROLSS_DMAXBAR3_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR3_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.26 CONTROLSS_DMAXBAR3_G0 Register

4.6.2.26.1 CONTROLSS_DMAXBAR3_G0 Register (Offset = 1C4h) [reset = 0h]

DMA XBAR3 Input Select.

Return to Summary Table

Table 4-2422. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61C4h

Figure 4-1186. CONTROLSS_DMAXBAR3_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR3_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2423. CONTROLSS_DMAXBAR3_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR3_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.27 CONTROLSS_DMAXBAR3_G1 Register

4.6.2.27.1 CONTROLSS_DMAXBAR3_G1 Register (Offset = 1C8h) [reset = 0h]

DMA XBAR3 Input Select.

Return to Summary Table

Table 4-2424. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61C8h

Figure 4-1187. CONTROLSS_DMAXBAR3_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR3_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2425. CONTROLSS_DMAXBAR3_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR3_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.28 CONTROLSS_DMAXBAR3_G2 Register

4.6.2.28.1 CONTROLSS_DMAXBAR3_G2 Register (Offset = 1CCh) [reset = 0h]

DMA XBAR3 Input Select.

Return to Summary Table

Table 4-2426. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61CCh

Figure 4-1188. CONTROLSS_DMAXBAR3_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR3_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2427. CONTROLSS_DMAXBAR3_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR3_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.29 CONTROLSS_DMAXBAR3_G3 Register

4.6.2.29.1 CONTROLSS_DMAXBAR3_G3 Register (Offset = 1D0h) [reset = 0h]

DMA XBAR3 Input Select.

Return to Summary Table

Table 4-2428. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61D0h

Figure 4-1189. CONTROLSS_DMAXBAR3_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR3_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2429. CONTROLSS_DMAXBAR3_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR3_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.30 CONTROLSS_DMAXBAR3_G4 Register

4.6.2.30.1 CONTROLSS_DMAXBAR3_G4 Register (Offset = 1D4h) [reset = 0h]

DMA XBAR3 Input Select.

Return to Summary Table

Table 4-2430. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61D4h

Figure 4-1190. CONTROLSS_DMAXBAR3_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR3_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2431. CONTROLSS_DMAXBAR3_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR3_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.31 CONTROLSS_DMAXBAR3_G5 Register

4.6.2.31.1 CONTROLSS_DMAXBAR3_G5 Register (Offset = 1D8h) [reset = 0h]

DMA XBAR3 Input Select.

Return to Summary Table

Table 4-2432. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61D8h

Figure 4-1191. CONTROLSS_DMAXBAR3_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR3_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2433. CONTROLSS_DMAXBAR3_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR3_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.32 CONTROLSS_DMAXBAR3_G6 Register

4.6.2.32.1 CONTROLSS_DMAXBAR3_G6 Register (Offset = 1DCh) [reset = 0h]

DMA XBAR3 Input Select.

Return to Summary Table

Table 4-2434. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 61DCh

Figure 4-1192. CONTROLSS_DMAXBAR3_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR3_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2435. CONTROLSS_DMAXBAR3_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR3_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.33 CONTROLSS_DMAXBAR4_GSEL Register

4.6.2.33.1 CONTROLSS_DMAXBAR4_GSEL Register (Offset = 200h) [reset = 0h]

DMA XBAR4 Input Select.

Return to Summary Table

Table 4-2436. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6200h

Figure 4-1193. CONTROLSS_DMAXBAR4_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR4_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2437. CONTROLSS_DMAXBAR4_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR4_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.34 CONTROLSS_DMAXBAR4_G0 Register

4.6.2.34.1 CONTROLSS_DMAXBAR4_G0 Register (Offset = 204h) [reset = 0h]

DMA XBAR4 Input Select.

Return to Summary Table

Table 4-2438. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6204h

Figure 4-1194. CONTROLSS_DMAXBAR4_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR4_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2439. CONTROLSS_DMAXBAR4_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR4_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.35 CONTROLSS_DMAXBAR4_G1 Register

4.6.2.35.1 CONTROLSS_DMAXBAR4_G1 Register (Offset = 208h) [reset = 0h]

DMA XBAR4 Input Select.

Return to Summary Table

Table 4-2440. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6208h

Figure 4-1195. CONTROLSS_DMAXBAR4_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR4_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2441. CONTROLSS_DMAXBAR4_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR4_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.36 CONTROLSS_DMAXBAR4_G2 Register

4.6.2.36.1 CONTROLSS_DMAXBAR4_G2 Register (Offset = 20Ch) [reset = 0h]

DMA XBAR4 Input Select.

Return to Summary Table

Table 4-2442. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 620Ch

Figure 4-1196. CONTROLSS_DMAXBAR4_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR4_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2443. CONTROLSS_DMAXBAR4_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR4_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.37 CONTROLSS_DMAXBAR4_G3 Register

4.6.2.37.1 CONTROLSS_DMAXBAR4_G3 Register (Offset = 210h) [reset = 0h]

DMA XBAR4 Input Select.

Return to Summary Table

Table 4-2444. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6210h

Figure 4-1197. CONTROLSS_DMAXBAR4_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DMAXBAR4_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2445. CONTROLSS_DMAXBAR4_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR4_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.38 CONTROLSS_DMAXBAR4_G4 Register

4.6.2.38.1 CONTROLSS_DMAXBAR4_G4 Register (Offset = 214h) [reset = 0h]

DMA XBAR4 Input Select.

Return to Summary Table

Table 4-2446. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6214h

Figure 4-1198. CONTROLSS_DMAXBAR4_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR4_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2447. CONTROLSS_DMAXBAR4_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR4_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.39 CONTROLSS_DMAXBAR4_G5 Register

4.6.2.39.1 CONTROLSS_DMAXBAR4_G5 Register (Offset = 218h) [reset = 0h]

DMA XBAR4 Input Select.

Return to Summary Table

Table 4-2448. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6218h

Figure 4-1199. CONTROLSS_DMAXBAR4_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR4_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2449. CONTROLSS_DMAXBAR4_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR4_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.40 CONTROLSS_DMAXBAR4_G6 Register

4.6.2.40.1 CONTROLSS_DMAXBAR4_G6 Register (Offset = 21Ch) [reset = 0h]

DMA XBAR4 Input Select.

Return to Summary Table

Table 4-2450. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 621Ch

Figure 4-1200. CONTROLSS_DMAXBAR4_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR4_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2451. CONTROLSS_DMAXBAR4_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR4_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.41 CONTROLSS_DMAXBAR5_GSEL Register

4.6.2.41.1 CONTROLSS_DMAXBAR5_GSEL Register (Offset = 240h) [reset = 0h]

DMA XBAR5 Input Select.

Return to Summary Table

Table 4-2452. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6240h

Figure 4-1201. CONTROLSS_DMAXBAR5_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DMAXBAR5_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2453. CONTROLSS_DMAXBAR5_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR5_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.42 CONTROLSS_DMAXBAR5_G0 Register

4.6.2.42.1 CONTROLSS_DMAXBAR5_G0 Register (Offset = 244h) [reset = 0h]

DMA XBAR5 Input Select.

Return to Summary Table

Table 4-2454. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6244h

Figure 4-1202. CONTROLSS_DMAXBAR5_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR5_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2455. CONTROLSS_DMAXBAR5_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR5_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.43 CONTROLSS_DMAXBAR5_G1 Register

4.6.2.43.1 CONTROLSS_DMAXBAR5_G1 Register (Offset = 248h) [reset = 0h]

DMA XBAR5 Input Select.

Return to Summary Table

Table 4-2456. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6248h

Figure 4-1203. CONTROLSS_DMAXBAR5_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR5_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2457. CONTROLSS_DMAXBAR5_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR5_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.44 CONTROLSS_DMAXBAR5_G2 Register

4.6.2.44.1 CONTROLSS_DMAXBAR5_G2 Register (Offset = 24Ch) [reset = 0h]

DMA XBAR5 Input Select.

Return to Summary Table

Table 4-2458. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 624Ch

Figure 4-1204. CONTROLSS_DMAXBAR5_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR5_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2459. CONTROLSS_DMAXBAR5_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR5_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.45 CONTROLSS_DMAXBAR5_G3 Register

4.6.2.45.1 CONTROLSS_DMAXBAR5_G3 Register (Offset = 250h) [reset = 0h]

DMA XBAR5 Input Select.

Return to Summary Table

Table 4-2460. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6250h

Figure 4-1205. CONTROLSS_DMAXBAR5_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR5_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2461. CONTROLSS_DMAXBAR5_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR5_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.46 CONTROLSS_DMAXBAR5_G4 Register

4.6.2.46.1 CONTROLSS_DMAXBAR5_G4 Register (Offset = 254h) [reset = 0h]

DMA XBAR5 Input Select.

Return to Summary Table

Table 4-2462. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6254h

Figure 4-1206. CONTROLSS_DMAXBAR5_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR5_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2463. CONTROLSS_DMAXBAR5_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR5_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.47 CONTROLSS_DMAXBAR5_G5 Register

4.6.2.47.1 CONTROLSS_DMAXBAR5_G5 Register (Offset = 258h) [reset = 0h]

DMA XBAR5 Input Select.

Return to Summary Table

Table 4-2464. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6258h

Figure 4-1207. CONTROLSS_DMAXBAR5_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR5_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2465. CONTROLSS_DMAXBAR5_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR5_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.48 CONTROLSS_DMAXBAR5_G6 Register

4.6.2.48.1 CONTROLSS_DMAXBAR5_G6 Register (Offset = 25Ch) [reset = 0h]

DMA XBAR5 Input Select.

Return to Summary Table

Table 4-2466. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 625Ch

Figure 4-1208. CONTROLSS_DMAXBAR5_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR5_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2467. CONTROLSS_DMAXBAR5_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR5_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.49 CONTROLSS_DMAXBAR6_GSEL Register

4.6.2.49.1 CONTROLSS_DMAXBAR6_GSEL Register (Offset = 280h) [reset = 0h]

DMA XBAR6 Input Select.

Return to Summary Table

Table 4-2468. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6280h

Figure 4-1209. CONTROLSS_DMAXBAR6_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR6_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2469. CONTROLSS_DMAXBAR6_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR6_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.50 CONTROLSS_DMAXBAR6_G0 Register

4.6.2.50.1 CONTROLSS_DMAXBAR6_G0 Register (Offset = 284h) [reset = 0h]

DMA XBAR6 Input Select.

Return to Summary Table

Table 4-2470. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6284h

Figure 4-1210. CONTROLSS_DMAXBAR6_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DMAXBAR6_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2471. CONTROLSS_DMAXBAR6_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR6_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.51 CONTROLSS_DMAXBAR6_G1 Register

4.6.2.51.1 CONTROLSS_DMAXBAR6_G1 Register (Offset = 288h) [reset = 0h]

DMA XBAR6 Input Select.

Return to Summary Table

Table 4-2472. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6288h

Figure 4-1211. CONTROLSS_DMAXBAR6_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR6_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2473. CONTROLSS_DMAXBAR6_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR6_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.52 CONTROLSS_DMAXBAR6_G2 Register

4.6.2.52.1 CONTROLSS_DMAXBAR6_G2 Register (Offset = 28Ch) [reset = 0h]

DMA XBAR6 Input Select.

Return to Summary Table

Table 4-2474. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 628Ch

Figure 4-1212. CONTROLSS_DMAXBAR6_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR6_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2475. CONTROLSS_DMAXBAR6_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR6_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.53 CONTROLSS_DMAXBAR6_G3 Register

4.6.2.53.1 CONTROLSS_DMAXBAR6_G3 Register (Offset = 290h) [reset = 0h]

DMA XBAR6 Input Select.

Return to Summary Table

Table 4-2476. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6290h

Figure 4-1213. CONTROLSS_DMAXBAR6_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR6_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2477. CONTROLSS_DMAXBAR6_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR6_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.54 CONTROLSS_DMAXBAR6_G4 Register

4.6.2.54.1 CONTROLSS_DMAXBAR6_G4 Register (Offset = 294h) [reset = 0h]

DMA XBAR6 Input Select.

Return to Summary Table

Table 4-2478. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6294h

Figure 4-1214. CONTROLSS_DMAXBAR6_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR6_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2479. CONTROLSS_DMAXBAR6_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR6_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.55 CONTROLSS_DMAXBAR6_G5 Register

4.6.2.55.1 CONTROLSS_DMAXBAR6_G5 Register (Offset = 298h) [reset = 0h]

DMA XBAR6 Input Select.

Return to Summary Table

Table 4-2480. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6298h

Figure 4-1215. CONTROLSS_DMAXBAR6_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR6_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2481. CONTROLSS_DMAXBAR6_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR6_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.56 CONTROLSS_DMAXBAR6_G6 Register

4.6.2.56.1 CONTROLSS_DMAXBAR6_G6 Register (Offset = 29Ch) [reset = 0h]

DMA XBAR6 Input Select.

Return to Summary Table

Table 4-2482. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 629Ch

Figure 4-1216. CONTROLSS_DMAXBAR6_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR6_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2483. CONTROLSS_DMAXBAR6_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR6_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.57 CONTROLSS_DMAXBAR7_GSEL Register

4.6.2.57.1 CONTROLSS_DMAXBAR7_GSEL Register (Offset = 2C0h) [reset = 0h]

DMA XBAR7 Input Select.

Return to Summary Table

Table 4-2484. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62C0h

Figure 4-1217. CONTROLSS_DMAXBAR7_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DMAXBAR7_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2485. CONTROLSS_DMAXBAR7_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR7_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.58 CONTROLSS_DMAXBAR7_G0 Register

4.6.2.58.1 CONTROLSS_DMAXBAR7_G0 Register (Offset = 2C4h) [reset = 0h]

DMA XBAR7 Input Select.

Return to Summary Table

Table 4-2486. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62C4h

Figure 4-1218. CONTROLSS_DMAXBAR7_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR7_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2487. CONTROLSS_DMAXBAR7_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR7_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.59 CONTROLSS_DMAXBAR7_G1 Register

4.6.2.59.1 CONTROLSS_DMAXBAR7_G1 Register (Offset = 2C8h) [reset = 0h]

DMA XBAR7 Input Select.

Return to Summary Table

Table 4-2488. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62C8h

Figure 4-1219. CONTROLSS_DMAXBAR7_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR7_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2489. CONTROLSS_DMAXBAR7_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR7_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.60 CONTROLSS_DMAXBAR7_G2 Register

4.6.2.60.1 CONTROLSS_DMAXBAR7_G2 Register (Offset = 2CCh) [reset = 0h]

DMA XBAR7 Input Select.

Return to Summary Table

Table 4-2490. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62CCh

Figure 4-1220. CONTROLSS_DMAXBAR7_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR7_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2491. CONTROLSS_DMAXBAR7_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR7_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.61 CONTROLSS_DMAXBAR7_G3 Register

4.6.2.61.1 CONTROLSS_DMAXBAR7_G3 Register (Offset = 2D0h) [reset = 0h]

DMA XBAR7 Input Select.

Return to Summary Table

Table 4-2492. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62D0h

Figure 4-1221. CONTROLSS_DMAXBAR7_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR7_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2493. CONTROLSS_DMAXBAR7_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR7_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.62 CONTROLSS_DMAXBAR7_G4 Register

4.6.2.62.1 CONTROLSS_DMAXBAR7_G4 Register (Offset = 2D4h) [reset = 0h]

DMA XBAR7 Input Select.

Return to Summary Table

Table 4-2494. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62D4h

Figure 4-1222. CONTROLSS_DMAXBAR7_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR7_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2495. CONTROLSS_DMAXBAR7_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR7_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.63 CONTROLSS_DMAXBAR7_G5 Register

4.6.2.63.1 CONTROLSS_DMAXBAR7_G5 Register (Offset = 2D8h) [reset = 0h]

DMA XBAR7 Input Select.

Return to Summary Table

Table 4-2496. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62D8h

Figure 4-1223. CONTROLSS_DMAXBAR7_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DMAXBAR7_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2497. CONTROLSS_DMAXBAR7_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR7_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.64 CONTROLSS_DMAXBAR7_G6 Register

4.6.2.64.1 CONTROLSS_DMAXBAR7_G6 Register (Offset = 2DCh) [reset = 0h]

DMA XBAR7 Input Select.

Return to Summary Table

Table 4-2498. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 62DCh

Figure 4-1224. CONTROLSS_DMAXBAR7_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR7_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2499. CONTROLSS_DMAXBAR7_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR7_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.65 CONTROLSS_DMAXBAR8_GSEL Register

4.6.2.65.1 CONTROLSS_DMAXBAR8_GSEL Register (Offset = 300h) [reset = 0h]

DMA XBAR8 Input Select.

Return to Summary Table

Table 4-2500. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6300h

Figure 4-1225. CONTROLSS_DMAXBAR8_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR8_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2501. CONTROLSS_DMAXBAR8_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR8_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.66 CONTROLSS_DMAXBAR8_G0 Register

4.6.2.66.1 CONTROLSS_DMAXBAR8_G0 Register (Offset = 304h) [reset = 0h]

DMA XBAR8 Input Select.

Return to Summary Table

Table 4-2502. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6304h

Figure 4-1226. CONTROLSS_DMAXBAR8_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR8_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2503. CONTROLSS_DMAXBAR8_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR8_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.67 CONTROLSS_DMAXBAR8_G1 Register

4.6.2.67.1 CONTROLSS_DMAXBAR8_G1 Register (Offset = 308h) [reset = 0h]

DMA XBAR8 Input Select.

Return to Summary Table

Table 4-2504. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6308h

Figure 4-1227. CONTROLSS_DMAXBAR8_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR8_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2505. CONTROLSS_DMAXBAR8_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR8_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.68 CONTROLSS_DMAXBAR8_G2 Register

4.6.2.68.1 CONTROLSS_DMAXBAR8_G2 Register (Offset = 30Ch) [reset = 0h]

DMA XBAR8 Input Select.

Return to Summary Table

Table 4-2506. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 630Ch

Figure 4-1228. CONTROLSS_DMAXBAR8_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR8_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2507. CONTROLSS_DMAXBAR8_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR8_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.69 CONTROLSS_DMAXBAR8_G3 Register

4.6.2.69.1 CONTROLSS_DMAXBAR8_G3 Register (Offset = 310h) [reset = 0h]

DMA XBAR8 Input Select.

Return to Summary Table

Table 4-2508. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6310h

Figure 4-1229. CONTROLSS_DMAXBAR8_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR8_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2509. CONTROLSS_DMAXBAR8_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR8_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.70 CONTROLSS_DMAXBAR8_G4 Register

4.6.2.70.1 CONTROLSS_DMAXBAR8_G4 Register (Offset = 314h) [reset = 0h]

DMA XBAR8 Input Select.

Return to Summary Table

Table 4-2510. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6314h

Figure 4-1230. CONTROLSS_DMAXBAR8_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR8_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2511. CONTROLSS_DMAXBAR8_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR8_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.71 CONTROLSS_DMAXBAR8_G5 Register

4.6.2.71.1 CONTROLSS_DMAXBAR8_G5 Register (Offset = 318h) [reset = 0h]

DMA XBAR8 Input Select.

Return to Summary Table

Table 4-2512. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6318h

Figure 4-1231. CONTROLSS_DMAXBAR8_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR8_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2513. CONTROLSS_DMAXBAR8_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR8_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.72 CONTROLSS_DMAXBAR8_G6 Register

4.6.2.72.1 CONTROLSS_DMAXBAR8_G6 Register (Offset = 31Ch) [reset = 0h]

DMA XBAR8 Input Select.

Return to Summary Table

Table 4-2514. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 631Ch

Figure 4-1232. CONTROLSS_DMAXBAR8_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR8_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2515. CONTROLSS_DMAXBAR8_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR8_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.73 CONTROLSS_DMAXBAR9_GSEL Register

4.6.2.73.1 CONTROLSS_DMAXBAR9_GSEL Register (Offset = 340h) [reset = 0h]

DMA XBAR9 Input Select.

Return to Summary Table

Table 4-2516. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6340h

Figure 4-1233. CONTROLSS_DMAXBAR9_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR9_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2517. CONTROLSS_DMAXBAR9_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR9_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.74 CONTROLSS_DMAXBAR9_G0 Register

4.6.2.74.1 CONTROLSS_DMAXBAR9_G0 Register (Offset = 344h) [reset = 0h]

DMA XBAR9 Input Select.

Return to Summary Table

Table 4-2518. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6344h

Figure 4-1234. CONTROLSS_DMAXBAR9_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR9_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2519. CONTROLSS_DMAXBAR9_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR9_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.75 CONTROLSS_DMAXBAR9_G1 Register

4.6.2.75.1 CONTROLSS_DMAXBAR9_G1 Register (Offset = 348h) [reset = 0h]

DMA XBAR9 Input Select.

Return to Summary Table

Table 4-2520. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6348h

Figure 4-1235. CONTROLSS_DMAXBAR9_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR9_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2521. CONTROLSS_DMAXBAR9_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR9_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.76 CONTROLSS_DMAXBAR9_G2 Register

4.6.2.76.1 CONTROLSS_DMAXBAR9_G2 Register (Offset = 34Ch) [reset = 0h]

DMA XBAR9 Input Select.

Return to Summary Table

Table 4-2522. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 634Ch

Figure 4-1236. CONTROLSS_DMAXBAR9_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR9_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2523. CONTROLSS_DMAXBAR9_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR9_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.77 CONTROLSS_DMAXBAR9_G3 Register

4.6.2.77.1 CONTROLSS_DMAXBAR9_G3 Register (Offset = 350h) [reset = 0h]

DMA XBAR9 Input Select.

Return to Summary Table

Table 4-2524. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6350h

Figure 4-1237. CONTROLSS_DMAXBAR9_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR9_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2525. CONTROLSS_DMAXBAR9_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR9_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.78 CONTROLSS_DMAXBAR9_G4 Register

4.6.2.78.1 CONTROLSS_DMAXBAR9_G4 Register (Offset = 354h) [reset = 0h]

DMA XBAR9 Input Select.

Return to Summary Table

Table 4-2526. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6354h

Figure 4-1238. CONTROLSS_DMAXBAR9_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR9_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2527. CONTROLSS_DMAXBAR9_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR9_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.79 CONTROLSS_DMAXBAR9_G5 Register

4.6.2.79.1 CONTROLSS_DMAXBAR9_G5 Register (Offset = 358h) [reset = 0h]

DMA XBAR9 Input Select.

Return to Summary Table

Table 4-2528. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6358h

Figure 4-1239. CONTROLSS_DMAXBAR9_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DMAXBAR9_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2529. CONTROLSS_DMAXBAR9_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR9_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.80 CONTROLSS_DMAXBAR9_G6 Register

4.6.2.80.1 CONTROLSS_DMAXBAR9_G6 Register (Offset = 35Ch) [reset = 0h]

DMA XBAR9 Input Select.

Return to Summary Table

Table 4-2530. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 635Ch

Figure 4-1240. CONTROLSS_DMAXBAR9_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR9_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2531. CONTROLSS_DMAXBAR9_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR9_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.81 CONTROLSS_DMAXBAR10_GSEL Register

4.6.2.81.1 CONTROLSS_DMAXBAR10_GSEL Register (Offset = 380h) [reset = 0h]

DMA XBAR10 Input Select.

Return to Summary Table

Table 4-2532. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6380h

Figure 4-1241. CONTROLSS_DMAXBAR10_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR10_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2533. CONTROLSS_DMAXBAR10_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR10_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.82 CONTROLSS_DMAXBAR10_G0 Register

4.6.2.82.1 CONTROLSS_DMAXBAR10_G0 Register (Offset = 384h) [reset = 0h]

DMA XBAR10 Input Select.

Return to Summary Table

Table 4-2534. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6384h

Figure 4-1242. CONTROLSS_DMAXBAR10_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR10_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2535. CONTROLSS_DMAXBAR10_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR10_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.83 CONTROLSS_DMAXBAR10_G1 Register

4.6.2.83.1 CONTROLSS_DMAXBAR10_G1 Register (Offset = 388h) [reset = 0h]

DMA XBAR10 Input Select.

Return to Summary Table

Table 4-2536. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6388h

Figure 4-1243. CONTROLSS_DMAXBAR10_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR10_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2537. CONTROLSS_DMAXBAR10_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR10_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.84 CONTROLSS_DMAXBAR10_G2 Register

4.6.2.84.1 CONTROLSS_DMAXBAR10_G2 Register (Offset = 38Ch) [reset = 0h]

DMA XBAR10 Input Select.

Return to Summary Table

Table 4-2538. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 638Ch

Figure 4-1244. CONTROLSS_DMAXBAR10_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR10_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2539. CONTROLSS_DMAXBAR10_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR10_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.85 CONTROLSS_DMAXBAR10_G3 Register

4.6.2.85.1 CONTROLSS_DMAXBAR10_G3 Register (Offset = 390h) [reset = 0h]

DMA XBAR10 Input Select.

Return to Summary Table

Table 4-2540. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6390h

Figure 4-1245. CONTROLSS_DMAXBAR10_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR10_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2541. CONTROLSS_DMAXBAR10_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR10_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.86 CONTROLSS_DMAXBAR10_G4 Register

4.6.2.86.1 CONTROLSS_DMAXBAR10_G4 Register (Offset = 394h) [reset = 0h]

DMA XBAR10 Input Select.

Return to Summary Table

Table 4-2542. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6394h

Figure 4-1246. CONTROLSS_DMAXBAR10_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR10_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2543. CONTROLSS_DMAXBAR10_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR10_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.87 CONTROLSS_DMAXBAR10_G5 Register

4.6.2.87.1 CONTROLSS_DMAXBAR10_G5 Register (Offset = 398h) [reset = 0h]

DMA XBAR10 Input Select.

Return to Summary Table

Table 4-2544. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6398h

Figure 4-1247. CONTROLSS_DMAXBAR10_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR10_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2545. CONTROLSS_DMAXBAR10_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR10_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.88 CONTROLSS_DMAXBAR10_G6 Register

4.6.2.88.1 CONTROLSS_DMAXBAR10_G6 Register (Offset = 39Ch) [reset = 0h]

DMA XBAR10 Input Select.

Return to Summary Table

Table 4-2546. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 639Ch

Figure 4-1248. CONTROLSS_DMAXBAR10_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR10_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2547. CONTROLSS_DMAXBAR10_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR10_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.89 CONTROLSS_DMAXBAR11_GSEL Register

4.6.2.89.1 CONTROLSS_DMAXBAR11_GSEL Register (Offset = 3C0h) [reset = 0h]

DMA XBAR11 Input Select.

Return to Summary Table

Table 4-2548. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63C0h

Figure 4-1249. CONTROLSS_DMAXBAR11_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR11_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2549. CONTROLSS_DMAXBAR11_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR11_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.90 CONTROLSS_DMAXBAR11_G0 Register

4.6.2.90.1 CONTROLSS_DMAXBAR11_G0 Register (Offset = 3C4h) [reset = 0h]

DMA XBAR11 Input Select.

Return to Summary Table

Table 4-2550. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63C4h

Figure 4-1250. CONTROLSS_DMAXBAR11_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR11_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2551. CONTROLSS_DMAXBAR11_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR11_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.91 CONTROLSS_DMAXBAR11_G1 Register

4.6.2.91.1 CONTROLSS_DMAXBAR11_G1 Register (Offset = 3C8h) [reset = 0h]

DMA XBAR11 Input Select.

Return to Summary Table

Table 4-2552. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63C8h

Figure 4-1251. CONTROLSS_DMAXBAR11_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DMAXBAR11_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2553. CONTROLSS_DMAXBAR11_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR11_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.92 CONTROLSS_DMAXBAR11_G2 Register

4.6.2.92.1 CONTROLSS_DMAXBAR11_G2 Register (Offset = 3CCh) [reset = 0h]

DMA XBAR11 Input Select.

Return to Summary Table

Table 4-2554. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63CCh

Figure 4-1252. CONTROLSS_DMAXBAR11_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR11_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2555. CONTROLSS_DMAXBAR11_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR11_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.93 CONTROLSS_DMAXBAR11_G3 Register

4.6.2.93.1 CONTROLSS_DMAXBAR11_G3 Register (Offset = 3D0h) [reset = 0h]

DMA XBAR11 Input Select.

Return to Summary Table

Table 4-2556. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63D0h

Figure 4-1253. CONTROLSS_DMAXBAR11_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DMAXBAR11_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2557. CONTROLSS_DMAXBAR11_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR11_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.94 CONTROLSS_DMAXBAR11_G4 Register

4.6.2.94.1 CONTROLSS_DMAXBAR11_G4 Register (Offset = 3D4h) [reset = 0h]

DMA XBAR11 Input Select.

Return to Summary Table

Table 4-2558. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63D4h

Figure 4-1254. CONTROLSS_DMAXBAR11_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DMAXBAR11_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2559. CONTROLSS_DMAXBAR11_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR11_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.95 CONTROLSS_DMAXBAR11_G5 Register

4.6.2.95.1 CONTROLSS_DMAXBAR11_G5 Register (Offset = 3D8h) [reset = 0h]

DMA XBAR11 Input Select.

Return to Summary Table

Table 4-2560. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63D8h

Figure 4-1255. CONTROLSS_DMAXBAR11_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR11_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2561. CONTROLSS_DMAXBAR11_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR11_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.96 CONTROLSS_DMAXBAR11_G6 Register

4.6.2.96.1 CONTROLSS_DMAXBAR11_G6 Register (Offset = 3DCh) [reset = 0h]

DMA XBAR11 Input Select.

Return to Summary Table

Table 4-2562. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 63DCh

Figure 4-1256. CONTROLSS_DMAXBAR11_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR11_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2563. CONTROLSS_DMAXBAR11_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR11_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.97 CONTROLSS_DMAXBAR12_GSEL Register

4.6.2.97.1 CONTROLSS_DMAXBAR12_GSEL Register (Offset = 400h) [reset = 0h]

DMA XBAR12 Input Select.

Return to Summary Table

Table 4-2564. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6400h

Figure 4-1257. CONTROLSS_DMAXBAR12_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DMAXBAR12_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2565. CONTROLSS_DMAXBAR12_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR12_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.98 CONTROLSS_DMAXBAR12_G0 Register

4.6.2.98.1 CONTROLSS_DMAXBAR12_G0 Register (Offset = 404h) [reset = 0h]

DMA XBAR12 Input Select.

Return to Summary Table

Table 4-2566. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6404h

Figure 4-1258. CONTROLSS_DMAXBAR12_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR12_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2567. CONTROLSS_DMAXBAR12_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR12_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.99 CONTROLSS_DMAXBAR12_G1 Register

4.6.2.99.1 CONTROLSS_DMAXBAR12_G1 Register (Offset = 408h) [reset = 0h]

DMA XBAR12 Input Select.

Return to Summary Table

Table 4-2568. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6408h

Figure 4-1259. CONTROLSS_DMAXBAR12_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR12_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2569. CONTROLSS_DMAXBAR12_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR12_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.100 CONTROLSS_DMAXBAR12_G2 Register

4.6.2.100.1 CONTROLSS_DMAXBAR12_G2 Register (Offset = 40Ch) [reset = 0h]

DMA XBAR12 Input Select.

Return to Summary Table

Table 4-2570. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 640Ch

Figure 4-1260. CONTROLSS_DMAXBAR12_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DMAXBAR12_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2571. CONTROLSS_DMAXBAR12_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR12_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.101 CONTROLSS_DMAXBAR12_G3 Register

4.6.2.101.1 CONTROLSS_DMAXBAR12_G3 Register (Offset = 410h) [reset = 0h]

DMA XBAR12 Input Select.

Return to Summary Table

Table 4-2572. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6410h

Figure 4-1261. CONTROLSS_DMAXBAR12_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DMAXBAR12_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2573. CONTROLSS_DMAXBAR12_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR12_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.102 CONTROLSS_DMAXBAR12_G4 Register

4.6.2.102.1 CONTROLSS_DMAXBAR12_G4 Register (Offset = 414h) [reset = 0h]

DMA XBAR12 Input Select.

Return to Summary Table

Table 4-2574. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6414h

Figure 4-1262. CONTROLSS_DMAXBAR12_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR12_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2575. CONTROLSS_DMAXBAR12_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR12_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.103 CONTROLSS_DMAXBAR12_G5 Register

4.6.2.103.1 CONTROLSS_DMAXBAR12_G5 Register (Offset = 418h) [reset = 0h]

DMA XBAR12 Input Select.

Return to Summary Table

Table 4-2576. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6418h

Figure 4-1263. CONTROLSS_DMAXBAR12_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR12_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2577. CONTROLSS_DMAXBAR12_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR12_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.104 CONTROLSS_DMAXBAR12_G6 Register

4.6.2.104.1 CONTROLSS_DMAXBAR12_G6 Register (Offset = 41Ch) [reset = 0h]

DMA XBAR12 Input Select.

Return to Summary Table

Table 4-2578. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 641Ch

Figure 4-1264. CONTROLSS_DMAXBAR12_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR12_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2579. CONTROLSS_DMAXBAR12_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR12_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.105 CONTROLSS_DMAXBAR13_GSEL Register

4.6.2.105.1 CONTROLSS_DMAXBAR13_GSEL Register (Offset = 440h) [reset = 0h]

DMA XBAR13 Input Select.

Return to Summary Table

Table 4-2580. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6440h

Figure 4-1265. CONTROLSS_DMAXBAR13_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR13_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2581. CONTROLSS_DMAXBAR13_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR13_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.106 CONTROLSS_DMAXBAR13_G0 Register

4.6.2.106.1 CONTROLSS_DMAXBAR13_G0 Register (Offset = 444h) [reset = 0h]

DMA XBAR13 Input Select.

Return to Summary Table

Table 4-2582. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6444h

Figure 4-1266. CONTROLSS_DMAXBAR13_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR13_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2583. CONTROLSS_DMAXBAR13_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR13_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.107 CONTROLSS_DMAXBAR13_G1 Register

4.6.2.107.1 CONTROLSS_DMAXBAR13_G1 Register (Offset = 448h) [reset = 0h]

DMA XBAR13 Input Select.

Return to Summary Table

Table 4-2584. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6448h

Figure 4-1267. CONTROLSS_DMAXBAR13_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR13_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2585. CONTROLSS_DMAXBAR13_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR13_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.108 CONTROLSS_DMAXBAR13_G2 Register

4.6.2.108.1 CONTROLSS_DMAXBAR13_G2 Register (Offset = 44Ch) [reset = 0h]

DMA XBAR13 Input Select.

Return to Summary Table

Table 4-2586. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 644Ch

Figure 4-1268. CONTROLSS_DMAXBAR13_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR13_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2587. CONTROLSS_DMAXBAR13_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR13_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.109 CONTROLSS_DMAXBAR13_G3 Register

4.6.2.109.1 CONTROLSS_DMAXBAR13_G3 Register (Offset = 450h) [reset = 0h]

DMA XBAR13 Input Select.

Return to Summary Table

Table 4-2588. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6450h

Figure 4-1269. CONTROLSS_DMAXBAR13_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DMAXBAR13_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2589. CONTROLSS_DMAXBAR13_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR13_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.110 CONTROLSS_DMAXBAR13_G4 Register

4.6.2.110.1 CONTROLSS_DMAXBAR13_G4 Register (Offset = 454h) [reset = 0h]

DMA XBAR13 Input Select.

Return to Summary Table

Table 4-2590. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6454h

Figure 4-1270. CONTROLSS_DMAXBAR13_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR13_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2591. CONTROLSS_DMAXBAR13_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR13_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.111 CONTROLSS_DMAXBAR13_G5 Register

4.6.2.111.1 CONTROLSS_DMAXBAR13_G5 Register (Offset = 458h) [reset = 0h]

DMA XBAR13 Input Select.

Return to Summary Table

Table 4-2592. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6458h

Figure 4-1271. CONTROLSS_DMAXBAR13_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DMAXBAR13_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2593. CONTROLSS_DMAXBAR13_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR13_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.112 CONTROLSS_DMAXBAR13_G6 Register

4.6.2.112.1 CONTROLSS_DMAXBAR13_G6 Register (Offset = 45Ch) [reset = 0h]

DMA XBAR13 Input Select.

Return to Summary Table

Table 4-2594. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 645Ch

Figure 4-1272. CONTROLSS_DMAXBAR13_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR13_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2595. CONTROLSS_DMAXBAR13_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR13_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.113 CONTROLSS_DMAXBAR14_GSEL Register

4.6.2.113.1 CONTROLSS_DMAXBAR14_GSEL Register (Offset = 480h) [reset = 0h]

DMA XBAR14 Input Select.

Return to Summary Table

Table 4-2596. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6480h

Figure 4-1273. CONTROLSS_DMAXBAR14_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR14_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2597. CONTROLSS_DMAXBAR14_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR14_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.114 CONTROLSS_DMAXBAR14_G0 Register

4.6.2.114.1 CONTROLSS_DMAXBAR14_G0 Register (Offset = 484h) [reset = 0h]

DMA XBAR14 Input Select.

Return to Summary Table

Table 4-2598. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6484h

Figure 4-1274. CONTROLSS_DMAXBAR14_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR14_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2599. CONTROLSS_DMAXBAR14_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR14_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.115 CONTROLSS_DMAXBAR14_G1 Register

4.6.2.115.1 CONTROLSS_DMAXBAR14_G1 Register (Offset = 488h) [reset = 0h]

DMA XBAR14 Input Select.

Return to Summary Table

Table 4-2600. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6488h

Figure 4-1275. CONTROLSS_DMAXBAR14_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR14_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2601. CONTROLSS_DMAXBAR14_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR14_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.116 CONTROLSS_DMAXBAR14_G2 Register

4.6.2.116.1 CONTROLSS_DMAXBAR14_G2 Register (Offset = 48Ch) [reset = 0h]

DMA XBAR14 Input Select.

Return to Summary Table

Table 4-2602. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 648Ch

Figure 4-1276. CONTROLSS_DMAXBAR14_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR14_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2603. CONTROLSS_DMAXBAR14_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR14_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.117 CONTROLSS_DMAXBAR14_G3 Register

4.6.2.117.1 CONTROLSS_DMAXBAR14_G3 Register (Offset = 490h) [reset = 0h]

DMA XBAR14 Input Select.

Return to Summary Table

Table 4-2604. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6490h

Figure 4-1277. CONTROLSS_DMAXBAR14_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR14_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2605. CONTROLSS_DMAXBAR14_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR14_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.118 CONTROLSS_DMAXBAR14_G4 Register

4.6.2.118.1 CONTROLSS_DMAXBAR14_G4 Register (Offset = 494h) [reset = 0h]

DMA XBAR14 Input Select.

Return to Summary Table

Table 4-2606. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6494h

Figure 4-1278. CONTROLSS_DMAXBAR14_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR14_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2607. CONTROLSS_DMAXBAR14_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR14_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.119 CONTROLSS_DMAXBAR14_G5 Register

4.6.2.119.1 CONTROLSS_DMAXBAR14_G5 Register (Offset = 498h) [reset = 0h]

DMA XBAR14 Input Select.

Return to Summary Table

Table 4-2608. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6498h

Figure 4-1279. CONTROLSS_DMAXBAR14_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR14_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2609. CONTROLSS_DMAXBAR14_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR14_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.120 CONTROLSS_DMAXBAR14_G6 Register

4.6.2.120.1 CONTROLSS_DMAXBAR14_G6 Register (Offset = 49Ch) [reset = 0h]

DMA XBAR14 Input Select.

Return to Summary Table

Table 4-2610. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 649Ch

Figure 4-1280. CONTROLSS_DMAXBAR14_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR14_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2611. CONTROLSS_DMAXBAR14_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR14_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

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4.6.2.121 CONTROLSS_DMAXBAR15_GSEL Register

4.6.2.121.1 CONTROLSS_DMAXBAR15_GSEL Register (Offset = 4C0h) [reset = 0h]

DMA XBAR15 Input Select.

Return to Summary Table

Table 4-2612. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64C0h

Figure 4-1281. CONTROLSS_DMAXBAR15_GSEL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					DMAXBAR15_GSEL_GSEL		
NONE					R/W		
0h					0h		

Table 4-2613. CONTROLSS_DMAXBAR15_GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR15_GSEL_GSEL	R/W	0h	Select input source: 0:G0 selected .. 6:G6 selected

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4.6.2.122 CONTROLSS_DMAXBAR15_G0 Register

4.6.2.122.1 CONTROLSS_DMAXBAR15_G0 Register (Offset = 4C4h) [reset = 0h]

DMA XBAR15 Input Select.

Return to Summary Table

Table 4-2614. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64C4h

Figure 4-1282. CONTROLSS_DMAXBAR15_G0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR15_G0_SEL				
NONE			R/W				
0h			0h				

Table 4-2615. CONTROLSS_DMAXBAR15_G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR15_G0_SEL	R/W	0h	EPWM SOCA to corresponding XBAR 0:PWM0.SOCA is selected 1:PWM1.SOCA is selected . . 31:PWM31.SOCA is selected

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4.6.2.123 CONTROLSS_DMAXBAR15_G1 Register

4.6.2.123.1 CONTROLSS_DMAXBAR15_G1 Register (Offset = 4C8h) [reset = 0h]

DMA XBAR15 Input Select.

Return to Summary Table

Table 4-2616. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64C8h

Figure 4-1283. CONTROLSS_DMAXBAR15_G1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR15_G1_SEL				
NONE			R/W				
0h			0h				

Table 4-2617. CONTROLSS_DMAXBAR15_G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR15_G1_SEL	R/W	0h	EPWM SOCB to corresponding XBAR 0:PWM0.SOCB is selected 1:PWM1.SOCB is selected . . 31:PWM31.SOCB is selected

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4.6.2.124 CONTROLSS_DMAXBAR15_G2 Register

4.6.2.124.1 CONTROLSS_DMAXBAR15_G2 Register (Offset = 4CCh) [reset = 0h]

DMA XBAR15 Input Select.

Return to Summary Table

Table 4-2618. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64CCh

Figure 4-1284. CONTROLSS_DMAXBAR15_G2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DMAXBAR15_G2_SEL				
NONE			R/W				
0h			0h				

Table 4-2619. CONTROLSS_DMAXBAR15_G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMAXBAR15_G2_SEL	R/W	0h	ADC DMA requests to corresponding XBAR 0:ADC0.INT1 1:ADC0.INT2 2:ADC0.INT3 3:ADC0.INT4 4:ADC0.EVTINT 5:ADC1.INT1 6:ADC1.INT2 7:ADC1.INT3 8:ADC1.INT4 9:ADC1.EVTINT 10:ADC2.INT1 11:ADC2.INT2 12:ADC2.INT3 13:ADC2.INT4 14:ADC2.EVTINT 15:ADC3.INT1 16:ADC3.INT2 17:ADC3.INT3 18:ADC3.INT4 19:ADC3.EVTINT 20:ADC4.INT1 21:ADC4.INT2 22:ADC4.INT3 23:ADC4.INT4 24:ADC4.EVTINT

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4.6.2.125 CONTROLSS_DMAXBAR15_G3 Register

4.6.2.125.1 CONTROLSS_DMAXBAR15_G3 Register (Offset = 4D0h) [reset = 0h]

DMA XBAR15 Input Select.

Return to Summary Table

Table 4-2620. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64D0h

Figure 4-1285. CONTROLSS_DMAXBAR15_G3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR15_G3_SEL			
NONE				R/W			
0h				0h			

Table 4-2621. CONTROLSS_DMAXBAR15_G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR15_G3_SEL	R/W	0h	FSI DMA requests to corresponding XBAR 0:FSIRX0.RX_DMA_EVT 1; FSIRX0_RX_data_tag_match 2:FSIRX0_RX_ping_tag_match 3:FSIRX1.RX_DMA_EVT 4; FSIRX1_RX_data_tag_match 5:FSIRX1_RX_ping_tag_match 6:FSIRX2.RX_DMA_EVT 7; FSIRX2_RX_data_tag_match 8:FSIRX2_RX_ping_tag_match 9:FSIRX3.RX_DMA_EVT 10; FSIRX3_RX_data_tag_match 11:FSIRX3_RX_ping_tag_match 12:FSITX0.TX_DMA_EVT 13:FSITX1.TX_DMA_EVT 14:FSITX2.TX_DMA_EVT 15:FSITX3.TX_DMA_EVT

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4.6.2.126 CONTROLSS_DMAXBAR15_G4 Register

4.6.2.126.1 CONTROLSS_DMAXBAR15_G4 Register (Offset = 4D4h) [reset = 0h]

DMA XBAR15 Input Select.

Return to Summary Table

Table 4-2622. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64D4h

Figure 4-1286. CONTROLSS_DMAXBAR15_G4 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DMAXBAR15_G4_SEL		
NONE					R/W		
0h					0h		

Table 4-2623. CONTROLSS_DMAXBAR15_G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	DMAXBAR15_G4_SEL	R/W	0h	SDFM DMA requests to corresponding XBAR 0:SD0.FILT1.DRINT 1:SD0.FILT2.DRINT 2:SD0.FILT3.DRINT 3:SD0.FILT4.DRINT 4:SD1.FILT1.DRINT 5:SD1.FILT2.DRINT 6:SD1.FILT3.DRINT 7:SD1.FILT4.DRINT

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4.6.2.127 CONTROLSS_DMAXBAR15_G5 Register

4.6.2.127.1 CONTROLSS_DMAXBAR15_G5 Register (Offset = 4D8h) [reset = 0h]

DMA XBAR15 Input Select.

Return to Summary Table

Table 4-2624. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64D8h

Figure 4-1287. CONTROLSS_DMAXBAR15_G5 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				DMAXBAR15_G5_SEL			
NONE				R/W			
0h				0h			

Table 4-2625. CONTROLSS_DMAXBAR15_G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR15_G5_SEL	R/W	0h	ECAP DMA requests to corresponding XBAR 0:ECAP0.DMA_INT 1:ECAP1.DMA_INT 2:ECAP2.DMA_INT 3:ECAP3.DMA_INT 4:ECAP4.DMA_INT 5:ECAP5.DMA_INT 6:ECAP6.DMA_INT 7:ECAP7.DMA_INT 8:ECAP8.DMA_INT 9:ECAP9.DMA_INT 10:ECAP10.DMA_INT 11:ECAP11.DMA_INT 12:ECAP12.DMA_INT 13:ECAP13.DMA_INT 14:ECAP14.DMA_INT 15:ECAP15.DMA_INT

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4.6.2.128 CONTROLSS_DMAXBAR15_G6 Register

4.6.2.128.1 CONTROLSS_DMAXBAR15_G6 Register (Offset = 4DCh) [reset = 0h]

DMA XBAR15 Input Select.

Return to Summary Table

Table 4-2626. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 64DCh

Figure 4-1288. CONTROLSS_DMAXBAR15_G6 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				DMAXBAR15_G6_SEL			
NONE				R/W			
0h				0h			

Table 4-2627. CONTROLSS_DMAXBAR15_G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	DMAXBAR15_G6_SEL	R/W	0h	ADC_R DMA requests to corresponding XBAR 0:ADCR0.INT1 1:ADCR0.INT2 2:ADCR0.INT3 3:ADCR0.INT4 4:ADCR0.EVTINT 5:ADCR1.INT1 6:ADCR1.INT2 7:ADCR1.INT3 8:ADCR1.INT4 9:ADCR1.EVTINT

5 System-on-chip (SoC) Registers

The System-on-chip (SoC) module registers are described in the following sections.

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5.1 MCAN

MCAN

5.1.1 MCAN Summaries

MCAN Summaries

Table 5-1. MSG_RAM Registers, Base Address=5260 0000h, Length=32768

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
0h	32	MSG_RAM_START	5260 0000h	5261 0000h	5262 0000h
10FFCh	32	MSG_RAM_END	5261 0FFCh	5262 0FFCh	5263 0FFCh

Table 5-2. MSG_RAM Registers, Base Address=5260 0000h, Length=32768

Offset	Length	Register Name	MCAN3 Physical Address	MCAN4 Physical Address	MCAN5 Physical Address
0h	32	MSG_RAM_START	5263 0000h	5264 0000h	5265 0000h
10FFCh	32	MSG_RAM_END	5264 0FFCh	5265 0FFCh	5266 0FFCh

Table 5-3. MSG_RAM Registers, Base Address=5260 0000h, Length=32768

Offset	Length	Register Name	MCAN6 Physical Address	MCAN7 Physical Address
0h	32	MSG_RAM_START	5266 0000h	5267 0000h
10FFCh	32	MSG_RAM_END	5267 0FFCh	5268 0FFCh

Table 5-4. CFG Registers, Base Address=5260 8000h, Length=1024

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
0h	32	CFG_SS_PID	5260 8000h	5261 8000h	5262 8000h
4h	32	CFG_SS_CTRL	5260 8004h	5261 8004h	5262 8004h
8h	32	CFG_SS_STAT	5260 8008h	5261 8008h	5262 8008h
Ch	32	CFG_SS_ICS	5260 800Ch	5261 800Ch	5262 800Ch
10h	32	CFG_SS_IRS	5260 8010h	5261 8010h	5262 8010h
14h	32	CFG_SS_IECS	5260 8014h	5261 8014h	5262 8014h
18h	32	CFG_SS_IE	5260 8018h	5261 8018h	5262 8018h
1Ch	32	CFG_SS_IES	5260 801Ch	5261 801Ch	5262 801Ch
20h	32	CFG_SS_EOI	5260 8020h	5261 8020h	5262 8020h
24h	32	CFG_SS_EXT_TS_PS	5260 8024h	5261 8024h	5262 8024h
28h	32	CFG_SS_EXT_TS_USIC	5260 8028h	5261 8028h	5262 8028h
200h	32	CFG_CREL	5260 8200h	5261 8200h	5262 8200h
204h	32	CFG_ENDN	5260 8204h	5261 8204h	5262 8204h
208h	32	CFG_CUST	5260 8208h	5261 8208h	5262 8208h
20Ch	32	CFG_DBTP	5260 820Ch	5261 820Ch	5262 820Ch
210h	32	CFG_TEST	5260 8210h	5261 8210h	5262 8210h
214h	32	CFG_RWD	5260 8214h	5261 8214h	5262 8214h
218h	32	CFG_CCCR	5260 8218h	5261 8218h	5262 8218h
21Ch	32	CFG_NBTP	5260 821Ch	5261 821Ch	5262 821Ch
220h	32	CFG_TSCC	5260 8220h	5261 8220h	5262 8220h

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Table 5-4. CFG Registers, Base Address=5260 8000h, Length=1024 (continued)

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
224h	32	CFG_TSCV	5260 8224h	5261 8224h	5262 8224h
228h	32	CFG_TOCC	5260 8228h	5261 8228h	5262 8228h
22Ch	32	CFG_TOCV	5260 822Ch	5261 822Ch	5262 822Ch
240h	32	CFG_ECR	5260 8240h	5261 8240h	5262 8240h
244h	32	CFG_PSR	5260 8244h	5261 8244h	5262 8244h
248h	32	CFG_TDCR	5260 8248h	5261 8248h	5262 8248h
250h	32	CFG_IR	5260 8250h	5261 8250h	5262 8250h
254h	32	CFG_IE	5260 8254h	5261 8254h	5262 8254h
258h	32	CFG_ILS	5260 8258h	5261 8258h	5262 8258h
25Ch	32	CFG_ILE	5260 825Ch	5261 825Ch	5262 825Ch
280h	32	CFG_GFC	5260 8280h	5261 8280h	5262 8280h
284h	32	CFG_SIDFC	5260 8284h	5261 8284h	5262 8284h
288h	32	CFG_XIDFC	5260 8288h	5261 8288h	5262 8288h
290h	32	CFG_XIDAM	5260 8290h	5261 8290h	5262 8290h
294h	32	CFG_HPMS	5260 8294h	5261 8294h	5262 8294h
298h	32	CFG_NDAT1	5260 8298h	5261 8298h	5262 8298h
29Ch	32	CFG_NDAT2	5260 829Ch	5261 829Ch	5262 829Ch
2A0h	32	CFG_RXF0C	5260 82A0h	5261 82A0h	5262 82A0h
2A4h	32	CFG_RXF0S	5260 82A4h	5261 82A4h	5262 82A4h
2A8h	32	CFG_RXF0A	5260 82A8h	5261 82A8h	5262 82A8h
2ACh	32	CFG_RXBC	5260 82ACh	5261 82ACh	5262 82ACh
2B0h	32	CFG_RXF1C	5260 82B0h	5261 82B0h	5262 82B0h
2B4h	32	CFG_RXF1S	5260 82B4h	5261 82B4h	5262 82B4h
2B8h	32	CFG_RXF1A	5260 82B8h	5261 82B8h	5262 82B8h
2BCh	32	CFG_RXESC	5260 82BCh	5261 82BCh	5262 82BCh
2C0h	32	CFG_TXBC	5260 82C0h	5261 82C0h	5262 82C0h
2C4h	32	CFG_TXFQS	5260 82C4h	5261 82C4h	5262 82C4h
2C8h	32	CFG_TXESC	5260 82C8h	5261 82C8h	5262 82C8h
2CCh	32	CFG_TXBRP	5260 82CCh	5261 82CCh	5262 82CCh
2D0h	32	CFG_TXBAR	5260 82D0h	5261 82D0h	5262 82D0h
2D4h	32	CFG_TXBCR	5260 82D4h	5261 82D4h	5262 82D4h
2D8h	32	CFG_TXBTO	5260 82D8h	5261 82D8h	5262 82D8h
2DCh	32	CFG_TXBCF	5260 82DCh	5261 82DCh	5262 82DCh
2E0h	32	CFG_TXBTIE	5260 82E0h	5261 82E0h	5262 82E0h
2E4h	32	CFG_TXBCIE	5260 82E4h	5261 82E4h	5262 82E4h
2F0h	32	CFG_TXEFC	5260 82F0h	5261 82F0h	5262 82F0h
2F4h	32	CFG_TXEFS	5260 82F4h	5261 82F4h	5262 82F4h
2F8h	32	CFG_TXEFA	5260 82F8h	5261 82F8h	5262 82F8h

Table 5-5. CFG Registers, Base Address=5260 8000h, Length=1024

Offset	Length	Register Name	MCAN3 Physical Address	MCAN4 Physical Address	MCAN5 Physical Address
0h	32	CFG_SS_PID	5263 8000h	5264 8000h	5265 8000h
4h	32	CFG_SS_CTRL	5263 8004h	5264 8004h	5265 8004h
8h	32	CFG_SS_STAT	5263 8008h	5264 8008h	5265 8008h
Ch	32	CFG_SS_ICS	5263 800Ch	5264 800Ch	5265 800Ch

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Table 5-5. CFG Registers, Base Address=5260 8000h, Length=1024 (continued)

Offset	Length	Register Name	MCAN3 Physical Address	MCAN4 Physical Address	MCAN5 Physical Address
10h	32	CFG_SS_IRS	5263 8010h	5264 8010h	5265 8010h
14h	32	CFG_SS_IECS	5263 8014h	5264 8014h	5265 8014h
18h	32	CFG_SS_IE	5263 8018h	5264 8018h	5265 8018h
1Ch	32	CFG_SS_IES	5263 801Ch	5264 801Ch	5265 801Ch
20h	32	CFG_SS_EOI	5263 8020h	5264 8020h	5265 8020h
24h	32	CFG_SS_EXT_TS_PS	5263 8024h	5264 8024h	5265 8024h
28h	32	CFG_SS_EXT_TS_USIC	5263 8028h	5264 8028h	5265 8028h
200h	32	CFG_CREL	5263 8200h	5264 8200h	5265 8200h
204h	32	CFG_ENDN	5263 8204h	5264 8204h	5265 8204h
208h	32	CFG_CUST	5263 8208h	5264 8208h	5265 8208h
20Ch	32	CFG_DBTP	5263 820Ch	5264 820Ch	5265 820Ch
210h	32	CFG_TEST	5263 8210h	5264 8210h	5265 8210h
214h	32	CFG_RWD	5263 8214h	5264 8214h	5265 8214h
218h	32	CFG_CCCR	5263 8218h	5264 8218h	5265 8218h
21Ch	32	CFG_NBTP	5263 821Ch	5264 821Ch	5265 821Ch
220h	32	CFG_TSCC	5263 8220h	5264 8220h	5265 8220h
224h	32	CFG_TSCV	5263 8224h	5264 8224h	5265 8224h
228h	32	CFG_TOCC	5263 8228h	5264 8228h	5265 8228h
22Ch	32	CFG_TOCV	5263 822Ch	5264 822Ch	5265 822Ch
240h	32	CFG_ECR	5263 8240h	5264 8240h	5265 8240h
244h	32	CFG_PSR	5263 8244h	5264 8244h	5265 8244h
248h	32	CFG_TDCR	5263 8248h	5264 8248h	5265 8248h
250h	32	CFG_IR	5263 8250h	5264 8250h	5265 8250h
254h	32	CFG_IE	5263 8254h	5264 8254h	5265 8254h
258h	32	CFG_ILS	5263 8258h	5264 8258h	5265 8258h
25Ch	32	CFG_ILE	5263 825Ch	5264 825Ch	5265 825Ch
280h	32	CFG_GFC	5263 8280h	5264 8280h	5265 8280h
284h	32	CFG_SIDFC	5263 8284h	5264 8284h	5265 8284h
288h	32	CFG_XIDFC	5263 8288h	5264 8288h	5265 8288h
290h	32	CFG_XIDAM	5263 8290h	5264 8290h	5265 8290h
294h	32	CFG_HPMS	5263 8294h	5264 8294h	5265 8294h
298h	32	CFG_NDAT1	5263 8298h	5264 8298h	5265 8298h
29Ch	32	CFG_NDAT2	5263 829Ch	5264 829Ch	5265 829Ch
2A0h	32	CFG_RXF0C	5263 82A0h	5264 82A0h	5265 82A0h
2A4h	32	CFG_RXF0S	5263 82A4h	5264 82A4h	5265 82A4h
2A8h	32	CFG_RXF0A	5263 82A8h	5264 82A8h	5265 82A8h
2ACh	32	CFG_RXBC	5263 82ACh	5264 82ACh	5265 82ACh
2B0h	32	CFG_RXF1C	5263 82B0h	5264 82B0h	5265 82B0h
2B4h	32	CFG_RXF1S	5263 82B4h	5264 82B4h	5265 82B4h
2B8h	32	CFG_RXF1A	5263 82B8h	5264 82B8h	5265 82B8h
2BCh	32	CFG_RXESC	5263 82BCh	5264 82BCh	5265 82BCh
2C0h	32	CFG_TXBC	5263 82C0h	5264 82C0h	5265 82C0h
2C4h	32	CFG_TXFQS	5263 82C4h	5264 82C4h	5265 82C4h
2C8h	32	CFG_TXESC	5263 82C8h	5264 82C8h	5265 82C8h
2CCh	32	CFG_TXBRP	5263 82CCh	5264 82CCh	5265 82CCh
2D0h	32	CFG_TXBAR	5263 82D0h	5264 82D0h	5265 82D0h

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Table 5-5. CFG Registers, Base Address=5260 8000h, Length=1024 (continued)

Offset	Length	Register Name	MCAN3 Physical Address	MCAN4 Physical Address	MCAN5 Physical Address
2D4h	32	CFG_TXBCR	5263 82D4h	5264 82D4h	5265 82D4h
2D8h	32	CFG_TXBTO	5263 82D8h	5264 82D8h	5265 82D8h
2DCh	32	CFG_TXBCF	5263 82DCh	5264 82DCh	5265 82DCh
2E0h	32	CFG_TXBTIE	5263 82E0h	5264 82E0h	5265 82E0h
2E4h	32	CFG_TXBCIE	5263 82E4h	5264 82E4h	5265 82E4h
2F0h	32	CFG_TXEFC	5263 82F0h	5264 82F0h	5265 82F0h
2F4h	32	CFG_TXEFS	5263 82F4h	5264 82F4h	5265 82F4h
2F8h	32	CFG_TXEFA	5263 82F8h	5264 82F8h	5265 82F8h

Table 5-6. CFG Registers, Base Address=5260 8000h, Length=1024

Offset	Length	Register Name	MCAN6 Physical Address	MCAN7 Physical Address
0h	32	CFG_SS_PID	5266 8000h	5267 8000h
4h	32	CFG_SS_CTRL	5266 8004h	5267 8004h
8h	32	CFG_SS_STAT	5266 8008h	5267 8008h
Ch	32	CFG_SS_ICS	5266 800Ch	5267 800Ch
10h	32	CFG_SS_IRS	5266 8010h	5267 8010h
14h	32	CFG_SS_IECS	5266 8014h	5267 8014h
18h	32	CFG_SS_IE	5266 8018h	5267 8018h
1Ch	32	CFG_SS_IES	5266 801Ch	5267 801Ch
20h	32	CFG_SS_EOI	5266 8020h	5267 8020h
24h	32	CFG_SS_EXT_TS_PS	5266 8024h	5267 8024h
28h	32	CFG_SS_EXT_TS_USIC	5266 8028h	5267 8028h
200h	32	CFG_CREL	5266 8200h	5267 8200h
204h	32	CFG_ENDN	5266 8204h	5267 8204h
208h	32	CFG_CUST	5266 8208h	5267 8208h
20Ch	32	CFG_DBTP	5266 820Ch	5267 820Ch
210h	32	CFG_TEST	5266 8210h	5267 8210h
214h	32	CFG_RWD	5266 8214h	5267 8214h
218h	32	CFG_CCCR	5266 8218h	5267 8218h
21Ch	32	CFG_NBTP	5266 821Ch	5267 821Ch
220h	32	CFG_TSCC	5266 8220h	5267 8220h
224h	32	CFG_TSCV	5266 8224h	5267 8224h
228h	32	CFG_TOCC	5266 8228h	5267 8228h
22Ch	32	CFG_TOCV	5266 822Ch	5267 822Ch
240h	32	CFG_ECR	5266 8240h	5267 8240h
244h	32	CFG_PSR	5266 8244h	5267 8244h
248h	32	CFG_TDCR	5266 8248h	5267 8248h
250h	32	CFG_IR	5266 8250h	5267 8250h
254h	32	CFG_IE	5266 8254h	5267 8254h
258h	32	CFG_ILS	5266 8258h	5267 8258h
25Ch	32	CFG_ILE	5266 825Ch	5267 825Ch
280h	32	CFG_GFC	5266 8280h	5267 8280h
284h	32	CFG_SIDFC	5266 8284h	5267 8284h
288h	32	CFG_XIDFC	5266 8288h	5267 8288h
290h	32	CFG_XIDAM	5266 8290h	5267 8290h
294h	32	CFG_HPMS	5266 8294h	5267 8294h

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Table 5-6. CFG Registers, Base Address=5260 8000h, Length=1024 (continued)

Offset	Length	Register Name	MCAN6 Physical Address	MCAN7 Physical Address
298h	32	CFG_NDAT1	5266 8298h	5267 8298h
29Ch	32	CFG_NDAT2	5266 829Ch	5267 829Ch
2A0h	32	CFG_RXF0C	5266 82A0h	5267 82A0h
2A4h	32	CFG_RXF0S	5266 82A4h	5267 82A4h
2A8h	32	CFG_RXF0A	5266 82A8h	5267 82A8h
2ACh	32	CFG_RXBC	5266 82ACh	5267 82ACh
2B0h	32	CFG_RXF1C	5266 82B0h	5267 82B0h
2B4h	32	CFG_RXF1S	5266 82B4h	5267 82B4h
2B8h	32	CFG_RXF1A	5266 82B8h	5267 82B8h
2BCh	32	CFG_RXESC	5266 82BCh	5267 82BCh
2C0h	32	CFG_TXBC	5266 82C0h	5267 82C0h
2C4h	32	CFG_TXFQS	5266 82C4h	5267 82C4h
2C8h	32	CFG_TXESC	5266 82C8h	5267 82C8h
2CCh	32	CFG_TXBRP	5266 82CCh	5267 82CCh
2D0h	32	CFG_TXBAR	5266 82D0h	5267 82D0h
2D4h	32	CFG_TXBCR	5266 82D4h	5267 82D4h
2D8h	32	CFG_TXBTO	5266 82D8h	5267 82D8h
2DCh	32	CFG_TXBCF	5266 82DCh	5267 82DCh
2E0h	32	CFG_TXBTIE	5266 82E0h	5267 82E0h
2E4h	32	CFG_TXBCIE	5266 82E4h	5267 82E4h
2F0h	32	CFG_TXEFC	5266 82F0h	5267 82F0h
2F4h	32	CFG_TXEFS	5266 82F4h	5267 82F4h
2F8h	32	CFG_TXEFA	5266 82F8h	5267 82F8h

Table 5-7. ECC Registers, Base Address=5270 0000h, Length=1024

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
0h	32	ECC_REV	5270 0000h	5270 1000h	5270 2000h
8h	32	ECC_VECTOR	5270 0008h	5270 1008h	5270 2008h
Ch	32	ECC_STAT	5270 000Ch	5270 100Ch	5270 200Ch
14h	32	ECC_CTRL	5270 0014h	5270 1014h	5270 2014h
18h	32	ECC_ERR_CTRL1	5270 0018h	5270 1018h	5270 2018h
1Ch	32	ECC_ERR_CTRL2	5270 001Ch	5270 101Ch	5270 201Ch
20h	32	ECC_ERR_STAT1	5270 0020h	5270 1020h	5270 2020h
24h	32	ECC_ERR_STAT2	5270 0024h	5270 1024h	5270 2024h
28h	32	ECC_ERR_STAT3	5270 0028h	5270 1028h	5270 2028h
3Ch	32	ECC_SEC_EOI_REG	5270 003Ch	5270 103Ch	5270 203Ch
40h	32	ECC_SEC_STATUS_REG0	5270 0040h	5270 1040h	5270 2040h
80h	32	ECC_SEC_ENABLE_SET_REG0	5270 0080h	5270 1080h	5270 2080h
C0h	32	ECC_SEC_ENABLE_CLR_REG0	5270 00C0h	5270 10C0h	5270 20C0h
13Ch	32	ECC_DED_EOI_REG	5270 013Ch	5270 113Ch	5270 213Ch
140h	32	ECC_DED_STATUS_REG0	5270 0140h	5270 1140h	5270 2140h
180h	32	ECC_DED_ENABLE_SET_REG0	5270 0180h	5270 1180h	5270 2180h
1C0h	32	ECC_DED_ENABLE_CLR_REG0	5270 01C0h	5270 11C0h	5270 21C0h
200h	32	ECC_AGGR_ENABLE_SET	5270 0200h	5270 1200h	5270 2200h
204h	32	ECC_AGGR_ENABLE_CLR	5270 0204h	5270 1204h	5270 2204h
208h	32	ECC_AGGR_STATUS_SET	5270 0208h	5270 1208h	5270 2208h

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Table 5-7. ECC Registers, Base Address=5270 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCAN0 Physical Address	MCAN1 Physical Address	MCAN2 Physical Address
20Ch	32	ECC_AGGR_STATUS_CLR	5270 020Ch	5270 120Ch	5270 220Ch

Table 5-8. ECC Registers, Base Address=5270 0000h, Length=1024

Offset	Length	Register Name	MCAN3 Physical Address	MCAN4 Physical Address	MCAN5 Physical Address
0h	32	ECC_REV	5270 3000h	5270 4000h	5270 5000h
8h	32	ECC_VECTOR	5270 3008h	5270 4008h	5270 5008h
Ch	32	ECC_STAT	5270 300Ch	5270 400Ch	5270 500Ch
14h	32	ECC_CTRL	5270 3014h	5270 4014h	5270 5014h
18h	32	ECC_ERR_CTRL1	5270 3018h	5270 4018h	5270 5018h
1Ch	32	ECC_ERR_CTRL2	5270 301Ch	5270 401Ch	5270 501Ch
20h	32	ECC_ERR_STAT1	5270 3020h	5270 4020h	5270 5020h
24h	32	ECC_ERR_STAT2	5270 3024h	5270 4024h	5270 5024h
28h	32	ECC_ERR_STAT3	5270 3028h	5270 4028h	5270 5028h
3Ch	32	ECC_SEC_EOI_REG	5270 303Ch	5270 403Ch	5270 503Ch
40h	32	ECC_SEC_STATUS_REG0	5270 3040h	5270 4040h	5270 5040h
80h	32	ECC_SEC_ENABLE_SET_REG0	5270 3080h	5270 4080h	5270 5080h
C0h	32	ECC_SEC_ENABLE_CLR_REG0	5270 30C0h	5270 40C0h	5270 50C0h
13Ch	32	ECC_DED_EOI_REG	5270 313Ch	5270 413Ch	5270 513Ch
140h	32	ECC_DED_STATUS_REG0	5270 3140h	5270 4140h	5270 5140h
180h	32	ECC_DED_ENABLE_SET_REG0	5270 3180h	5270 4180h	5270 5180h
1C0h	32	ECC_DED_ENABLE_CLR_REG0	5270 31C0h	5270 41C0h	5270 51C0h
200h	32	ECC_AGGR_ENABLE_SET	5270 3200h	5270 4200h	5270 5200h
204h	32	ECC_AGGR_ENABLE_CLR	5270 3204h	5270 4204h	5270 5204h
208h	32	ECC_AGGR_STATUS_SET	5270 3208h	5270 4208h	5270 5208h
20Ch	32	ECC_AGGR_STATUS_CLR	5270 320Ch	5270 420Ch	5270 520Ch

Table 5-9. ECC Registers, Base Address=5270 0000h, Length=1024

Offset	Length	Register Name	MCAN6 Physical Address	MCAN7 Physical Address
0h	32	ECC_REV	5270 6000h	5270 7000h
8h	32	ECC_VECTOR	5270 6008h	5270 7008h
Ch	32	ECC_STAT	5270 600Ch	5270 700Ch
14h	32	ECC_CTRL	5270 6014h	5270 7014h
18h	32	ECC_ERR_CTRL1	5270 6018h	5270 7018h
1Ch	32	ECC_ERR_CTRL2	5270 601Ch	5270 701Ch
20h	32	ECC_ERR_STAT1	5270 6020h	5270 7020h
24h	32	ECC_ERR_STAT2	5270 6024h	5270 7024h
28h	32	ECC_ERR_STAT3	5270 6028h	5270 7028h
3Ch	32	ECC_SEC_EOI_REG	5270 603Ch	5270 703Ch
40h	32	ECC_SEC_STATUS_REG0	5270 6040h	5270 7040h
80h	32	ECC_SEC_ENABLE_SET_REG0	5270 6080h	5270 7080h
C0h	32	ECC_SEC_ENABLE_CLR_REG0	5270 60C0h	5270 70C0h
13Ch	32	ECC_DED_EOI_REG	5270 613Ch	5270 713Ch
140h	32	ECC_DED_STATUS_REG0	5270 6140h	5270 7140h
180h	32	ECC_DED_ENABLE_SET_REG0	5270 6180h	5270 7180h

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Table 5-9. ECC Registers, Base Address=5270 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCAN6 Physical Address	MCAN7 Physical Address
1C0h	32	ECC_DED_ENABLE_CLR_REG0	5270 61C0h	5270 71C0h
200h	32	ECC_AGGR_ENABLE_SET	5270 6200h	5270 7200h
204h	32	ECC_AGGR_ENABLE_CLR	5270 6204h	5270 7204h
208h	32	ECC_AGGR_STATUS_SET	5270 6208h	5270 7208h
20Ch	32	ECC_AGGR_STATUS_CLR	5270 620Ch	5270 720Ch

5.1.2 MCAN Registers

MCAN Registers

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5.1.2.1 MSG_RAM_START Register

5.1.2.1.1 MSG_RAM_START Register (Offset = 0h) [reset = 0h]

START.

Return to Summary Table

Table 5-10. Instance Table

Instance Name	Physical Address
MCAN0	5260 0000h
MCAN1	5261 0000h
MCAN2	5262 0000h
MCAN3	5263 0000h
MCAN4	5264 0000h
MCAN5	5265 0000h
MCAN6	5266 0000h
MCAN7	5267 0000h

Figure 5-1. MSG_RAM_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 5-11. MSG_RAM_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	MCAN message mem Start address

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5.1.2.2 MSG_RAM_END Register

5.1.2.2.1 MSG_RAM_END Register (Offset = 10FFCh) [reset = 0h]

END.

Return to Summary Table

Table 5-12. Instance Table

Instance Name	Physical Address
MCAN0	5261 0FFCh
MCAN1	5262 0FFCh
MCAN2	5263 0FFCh
MCAN3	5264 0FFCh
MCAN4	5265 0FFCh
MCAN5	5266 0FFCh
MCAN6	5267 0FFCh
MCAN7	5268 0FFCh

Figure 5-2. MSG_RAM_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 5-13. MSG_RAM_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	MCAN message mem End address

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5.1.2.3 CFG_SS_PID Register

5.1.2.3.1 CFG_SS_PID Register (Offset = 0h) [reset = 68E05901h]

Revision Register. The Revision Register contains the major and minor revisions for the MCANSS.

Return to Summary Table

Table 5-14. Instance Table

Instance Name	Physical Address
MCAN0	5260 8000h
MCAN1	5261 8000h
MCAN2	5262 8000h
MCAN3	5263 8000h
MCAN4	5264 8000h
MCAN5	5265 8000h
MCAN6	5266 8000h
MCAN7	5267 8000h

Figure 5-3. CFG_SS_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		8E0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
8E0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
Bh					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		1h					

Table 5-15. CFG_SS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme
29:28	BU	R	2h	Business Unit: 10 = Processors
27:16	MODULE_ID	R	8E0h	Module ID
15:11	RTL	R	Bh	RTL revision. Will vary depending on release.
10:8	MAJOR	R	1h	Major revision
7:6	CUSTOM	R	0h	Custom
5:0	MINOR	R	1h	Minor revision

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5.1.2.4 CFG_SS_CTRL Register

5.1.2.4.1 CFG_SS_CTRL Register (Offset = 4h) [reset = 8h]

Control Register. The Control Register contains general control bits for the MCANSS.

Return to Summary Table

Table 5-16. Instance Table

Instance Name	Physical Address
MCAN0	5260 8004h
MCAN1	5261 8004h
MCAN2	5262 8004h
MCAN3	5263 8004h
MCAN4	5264 8004h
MCAN5	5265 8004h
MCAN6	5266 8004h
MCAN7	5267 8004h

Figure 5-4. CFG_SS_CTRL Name Register

31	30	29	28	27	26	25	24
NU0							
R							
0h							
23	22	21	20	19	18	17	16
NU0							
R							
0h							
15	14	13	12	11	10	9	8
NU0							
R							
0h							
7	6	5	4	3	2	1	0
NU0	EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREGEN	DBGSUSP_FREE	NU		
R	R/W	R/W	R/W	R/W	R		
0h	0h	0h	0h	1h	0h		

Table 5-17. CFG_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	NU0	R	0h	Reserved
6	EXT_TS_CNTR_EN	R/W	0h	External TimeStamp Counter Enable
5	AUTOWAKEUP	R/W	0h	Automatic Wakeup Enable
4	WAKEUPREGEN	R/W	0h	Wakeup Request Enable
3	DBGSUSP_FREE	R/W	1h	0-Honor Debug Suspend, 1-Disregard debug suspend
2:0	NU	R	0h	Reserved

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5.1.2.5 CFG_SS_STAT Register

5.1.2.5.1 CFG_SS_STAT Register (Offset = 8h) [reset = 6h]

Status Register. The Status Register provides general status bits for the MCANSS.

Return to Summary Table

Table 5-18. Instance Table

Instance Name	Physical Address
MCAN0	5260 8008h
MCAN1	5261 8008h
MCAN2	5262 8008h
MCAN3	5263 8008h
MCAN4	5264 8008h
MCAN5	5265 8008h
MCAN6	5266 8008h
MCAN7	5267 8008h

Figure 5-5. CFG_SS_STAT Name Register

31	30	29	28	27	26	25	24
NU1							
NU1							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU1							
NU1							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU1							
NU1							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU1					EN_FDOE	MMI_DONE	NU
NU1					R	R	R
0h					1h	1h	0h

Table 5-19. CFG_SS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	NU1	NU1	0h	Reserved
2	EN_FDOE	R	1h	Enable FD configuration. Reflects the value of mcanss_enable_fdoe configuration port
1	MMI_DONE	R	1h	0:Memory Initialization is in progress, 1:Memory Intialization Done
0	NU	R	0h	Reserved

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5.1.2.6 CFG_SS_ICS Register

5.1.2.6.1 CFG_SS_ICS Register (Offset = Ch) [reset = 0h]

Interrupt Clear Shadow Register. Write 1 to clear interrupt bits.

Return to Summary Table

Table 5-20. Instance Table

Instance Name	Physical Address
MCAN0	5260 800Ch
MCAN1	5261 800Ch
MCAN2	5262 800Ch
MCAN3	5263 800Ch
MCAN4	5264 800Ch
MCAN5	5265 800Ch
MCAN6	5266 800Ch
MCAN7	5267 800Ch

Figure 5-6. CFG_SS_ICS Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">NU2</td></tr>
<tr><td colspan="8">NU2</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">NU2</td></tr>
<tr><td colspan="8">NU2</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NU2</td></tr>
<tr><td colspan="8">NU2</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">NU2</td><td>ICS</td></tr>
<tr><td colspan="7">NU2</td><td>W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 5-21. CFG_SS_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU2	NU2	0h	Reserved
0	ICS	W	0h	This bit contains the External TimeStamp Counter Overflow Interrupt status. Write '1' to clear bits. [ICS - Interrupt Clear Shadow Register]

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5.1.2.7 CFG_SS_IRS Register

5.1.2.7.1 CFG_SS_IRS Register (Offset = 10h) [reset = 0h]

Interrupt Raw Status Register. Write 1 to set interrupt bits.

Return to Summary Table

Table 5-22. Instance Table

Instance Name	Physical Address
MCAN0	5260 8010h
MCAN1	5261 8010h
MCAN2	5262 8010h
MCAN3	5263 8010h
MCAN4	5264 8010h
MCAN5	5265 8010h
MCAN6	5266 8010h
MCAN7	5267 8010h

Figure 5-7. CFG_SS_IRS Name Register

31	30	29	28	27	26	25	24
NU3							
R							
0h							
23	22	21	20	19	18	17	16
NU3							
R							
0h							
15	14	13	12	11	10	9	8
NU3							
R							
0h							
7	6	5	4	3	2	1	0
NU3							IRS
R							R
0h							0h

Table 5-23. CFG_SS_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU3	R	0h	Reserved
0	IRS	R	0h	External TimeStamp Counter Overflow Interrupt status. Read raw interrupt status. [IRS - Interrupt Raw Status Register]

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5.1.2.8 CFG_SS_IECS Register

5.1.2.8.1 CFG_SS_IECS Register (Offset = 14h) [reset = 0h]

Interrupt Enable Clear Shadow Register. Write 1 to clear interrupt enable bits.

Return to Summary Table

Table 5-24. Instance Table

Instance Name	Physical Address
MCAN0	5260 8014h
MCAN1	5261 8014h
MCAN2	5262 8014h
MCAN3	5263 8014h
MCAN4	5264 8014h
MCAN5	5265 8014h
MCAN6	5266 8014h
MCAN7	5267 8014h

Figure 5-8. CFG_SS_IECS Name Register

31	30	29	28	27	26	25	24
NU4							
R							
0h							
23	22	21	20	19	18	17	16
NU4							
R							
0h							
15	14	13	12	11	10	9	8
NU4							
R							
0h							
7	6	5	4	3	2	1	0
NU4							IECS
R							W
0h							0h

Table 5-25. CFG_SS_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU4	R	0h	Reserved
0	IECS	W	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to clear bits. [IECS - Interrupt Enable Clear Shadow Register]

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5.1.2.9 CFG_SS_IE Register

5.1.2.9.1 CFG_SS_IE Register (Offset = 18h) [reset = 0h]

Interrupt Enable Register. Write 1 to set interrupt bits.

Return to Summary Table

Table 5-26. Instance Table

Instance Name	Physical Address
MCAN0	5260 8018h
MCAN1	5261 8018h
MCAN2	5262 8018h
MCAN3	5263 8018h
MCAN4	5264 8018h
MCAN5	5265 8018h
MCAN6	5266 8018h
MCAN7	5267 8018h

Figure 5-9. CFG_SS_IE Name Register

31	30	29	28	27	26	25	24
NU5							
R							
0h							
23	22	21	20	19	18	17	16
NU5							
R							
0h							
15	14	13	12	11	10	9	8
NU5							
R							
0h							
7	6	5	4	3	2	1	0
NU5							IE
R							R/W
0h							0h

Table 5-27. CFG_SS_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU5	R	0h	Reserved
0	IE	R/W	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to set interrupt enable. Read returns interrupt enable. [IE - Interrupt Enable Register]

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5.1.2.10 CFG_SS_IES Register

5.1.2.10.1 CFG_SS_IES Register (Offset = 1Ch) [reset = 0h]

Interrupt Enable Status Register. Read enabled interrupts.

Return to Summary Table

Table 5-28. Instance Table

Instance Name	Physical Address
MCAN0	5260 801Ch
MCAN1	5261 801Ch
MCAN2	5262 801Ch
MCAN3	5263 801Ch
MCAN4	5264 801Ch
MCAN5	5265 801Ch
MCAN6	5266 801Ch
MCAN7	5267 801Ch

Figure 5-10. CFG_SS_IES Name Register

31	30	29	28	27	26	25	24
NU6							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU6							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU6							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU6							IES
R							R
0h							0h

Table 5-29. CFG_SS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU6	R	0h	Reserved
0	IES	R	0h	External TimeStamp Counter Overflow Interrupt. Read Enabled Interrupts. [IES - Interrupt Enable Status]

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5.1.2.11 CFG_SS_EOI Register

5.1.2.11.1 CFG_SS_EOI Register (Offset = 20h) [reset = 0h]

End Of Interrupt (EOI) Register. The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. For level interrupt signals the EOI register is not functional and must not be used.

Return to Summary Table

Table 5-30. Instance Table

Instance Name	Physical Address
MCAN0	5260 8020h
MCAN1	5261 8020h
MCAN2	5262 8020h
MCAN3	5263 8020h
MCAN4	5264 8020h
MCAN5	5265 8020h
MCAN6	5266 8020h
MCAN7	5267 8020h

Figure 5-11. CFG_SS_EOI Name Register

31	30	29	28	27	26	25	24
NU7							
R							
0h							
23	22	21	20	19	18	17	16
NU7							
R							
0h							
15	14	13	12	11	10	9	8
NU7							
R							
0h							
7	6	5	4	3	2	1	0
EOI							
W							
0h							

Table 5-31. CFG_SS_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	NU7	R	0h	Reserved
7:0	EOI	W	0h	Write with bit position of targeted interrupt. [E.g. Ext TS is bit 0]. Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt. Field values: 8'h00: EOI value for External TS interrupt 8'h01: EOI value for mcan[0] interrupt 8'h02: EOI value for mcan[1] interrupt All other values are not applicable [EOI - End Of Interrupt]

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5.1.2.12 CFG_SS_EXT_TS_PS Register

5.1.2.12.1 CFG_SS_EXT_TS_PS Register (Offset = 24h) [reset = 0h]

External Timestamp Prescaler Register.

Return to Summary Table

Table 5-32. Instance Table

Instance Name	Physical Address
MCAN0	5260 8024h
MCAN1	5261 8024h
MCAN2	5262 8024h
MCAN3	5263 8024h
MCAN4	5264 8024h
MCAN5	5265 8024h
MCAN6	5266 8024h
MCAN7	5267 8024h

Figure 5-12. CFG_SS_EXT_TS_PS Name Register

31	30	29	28	27	26	25	24
NU8							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRESCALE							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRESCALE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRESCALE							
R/W							
0h							

Table 5-33. CFG_SS_EXT_TS_PS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NU8	R	0h	Reserved
23:0	PRESCALE	R/W	0h	External Timestamp Prescaler reload value. External Timestamp count rate is host clock rate divided by this value with one exception: a value of 0 has the same effect as 1 .

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5.1.2.13 CFG_SS_EXT_TS_USIC Register

5.1.2.13.1 CFG_SS_EXT_TS_USIC Register (Offset = 28h) [reset = 0h]

External Timestamp Unserviced Interrupts Counter Register.

Return to Summary Table

Table 5-34. Instance Table

Instance Name	Physical Address
MCAN0	5260 8028h
MCAN1	5261 8028h
MCAN2	5262 8028h
MCAN3	5263 8028h
MCAN4	5264 8028h
MCAN5	5265 8028h
MCAN6	5266 8028h
MCAN7	5267 8028h

Figure 5-13. CFG_SS_EXT_TS_USIC Name Register

31	30	29	28	27	26	25	24
NU9							
R							
0h							
23	22	21	20	19	18	17	16
NU9							
R							
0h							
15	14	13	12	11	10	9	8
NU9							
R							
0h							
7	6	5	4	3	2	1	0
NU9			EXT_TS_INTR_CNTR				
R			R				
0h			0h				

Table 5-35. CFG_SS_EXT_TS_USIC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	NU9	R	0h	Reserved
4:0	EXT_TS_INTR_CNTR	R	0h	Number of unserviced rollover interrupts. If >1 an EOI write will issue another pulse interrupt [EXT_TS_USIC - External TImeStamp Unserviced Interrupts Counter]

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5.1.2.14 CFG_CREL Register

5.1.2.14.1 CFG_CREL Register (Offset = 200h) [reset = 32380608h]

Core Release Register. Release dependent constant (version + date).

Return to Summary Table

Table 5-36. Instance Table

Instance Name	Physical Address
MCAN0	5260 8200h
MCAN1	5261 8200h
MCAN2	5262 8200h
MCAN3	5263 8200h
MCAN4	5264 8200h
MCAN5	5265 8200h
MCAN6	5266 8200h
MCAN7	5267 8200h

Figure 5-14. CFG_CREL Name Register

31	30	29	28	27	26	25	24
REL				STEP			
R				R			
3h				2h			
23	22	21	20	19	18	17	16
SUBSTEP				YEAR			
R				R			
3h				8h			
15	14	13	12	11	10	9	8
MON							
R							
6h							
7	6	5	4	3	2	1	0
DAY							
R							
8h							

Table 5-37. CFG_CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	REL	R	3h	Core Release
27:24	STEP	R	2h	Step of Core Release
23:20	SUBSTEP	R	3h	Sub-Step of Core Release
19:16	YEAR	R	8h	Time Stamp Year
15:8	MON	R	6h	Time Stamp Month
7:0	DAY	R	8h	Time Stamp Day

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5.1.2.15 CFG_ENDN Register

5.1.2.15.1 CFG_ENDN Register (Offset = 204h) [reset = 87654321h]

Endian Register. Constant 8765 4321h.

Return to Summary Table

Table 5-38. Instance Table

Instance Name	Physical Address
MCAN0	5260 8204h
MCAN1	5261 8204h
MCAN2	5262 8204h
MCAN3	5263 8204h
MCAN4	5264 8204h
MCAN5	5265 8204h
MCAN6	5266 8204h
MCAN7	5267 8204h

Figure 5-15. CFG_ENDN Name Register

31	30	29	28	27	26	25	24
ETV							
R							
87654321h							
23	22	21	20	19	18	17	16
ETV							
R							
87654321h							
15	14	13	12	11	10	9	8
ETV							
R							
87654321h							
7	6	5	4	3	2	1	0
ETV							
R							
87654321h							

Table 5-39. CFG_ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ETV	R	87654321h	Endianess test value

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5.1.2.16 CFG_CUST Register

5.1.2.16.1 CFG_CUST Register (Offset = 208h) [reset = 0h]

Custom Register.

Return to Summary Table

Table 5-40. Instance Table

Instance Name	Physical Address
MCAN0	5260 8208h
MCAN1	5261 8208h
MCAN2	5262 8208h
MCAN3	5263 8208h
MCAN4	5264 8208h
MCAN5	5265 8208h
MCAN6	5266 8208h
MCAN7	5267 8208h

Figure 5-16. CFG_CUST Name Register

31	30	29	28	27	26	25	24
CUST							
R							
0h							
23	22	21	20	19	18	17	16
CUST							
R							
0h							
15	14	13	12	11	10	9	8
CUST							
R							
0h							
7	6	5	4	3	2	1	0
CUST							
R							
0h							

Table 5-41. CFG_CUST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CUST	R	0h	Custom

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5.1.2.17 CFG_DBTP Register

5.1.2.17.1 CFG_DBTP Register (Offset = 20Ch) [reset = A33h]

Data Bit Timing & Prescaler Register.
Configuration of data phase bit timing, transmitter delay compensation enable. This register is only writable if the MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set. The CAN bit time may be programed in the range of 4 to 49 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 MCAN functional clock periods. tq = (MCAN_DBTP[20-16] DBRP + 1) mtq (minimum time quantum = CAN clock period (MCAN functional clock)). The MCAN_DBTP[12-8] DTSEG1 field is the sum of Prop_Seg and Phase_Seg1. The MCAN_DBTP[7-4] DTSEG2 field is Phase_Seg2. Therefore the length of the bit time is (programmed values) [MCAN_DBTP[12-8] DTSEG1 + MCAN_DBTP[7-4] DTSEG2 + 3] tq or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] tq. The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.
Note: With a CAN clock (MCAN functional clock) of 8 MHz, the reset value of 0000 0A33h configures the MCAN module for a data phase bit rate of 500 kbit/s.
Note: The bit rate configured for the CAN FD data phase via the MCAN_DBTP register must be higher or equal to the bit rate configured for the arbitration phase via the MCAN_DBTP register.

Return to Summary Table

Table 5-42. Instance Table

Instance Name	Physical Address
MCAN0	5260 820Ch
MCAN1	5261 820Ch
MCAN2	5262 820Ch
MCAN3	5263 820Ch
MCAN4	5264 820Ch
MCAN5	5265 820Ch
MCAN6	5266 820Ch
MCAN7	5267 820Ch

Figure 5-17. CFG_DBTP Name Register

31	30	29	28	27	26	25	24
NU13							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TDC	NU12		DBRP				
R/W	R		R/W				
0h	0h		0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU11			DTSEG1				
R			R/W				
0h			Ah				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DTSEG2				DSJW			
R/W				R/W			
3h				3h			

Table 5-43. CFG_DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NU13	R	0h	Reserved

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Table 5-43. CFG_DBTP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	TDC	R/W	0h	Transmitter Delay Compensation 1'b0 = Transmitter Delay Compensation disabled 1'b1 = Transmitter Delay Compensation enabled
22:21	NU12	R	0h	Reserved
20:16	DBRP	R/W	0h	Data Baud Rate Prescaler The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
15:13	NU11	R	0h	Reserved
12:8	DTSEG1	R/W	Ah	Data time segment before smaple point. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
7:4	DTSEG2	R/W	3h	Data time segment after sample point. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.
3:0	DSJW	R/W	3h	Data resynchronization Jump Width. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

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5.1.2.18 CFG_TEST Register

5.1.2.18.1 CFG_TEST Register (Offset = 210h) [reset = 0h]

Test Register. Test mode selection. Write access to the MCAN_TEST register has to be enabled by setting the MCAN_CCCR[7] TEST bit.

Return to Summary Table

Table 5-44. Instance Table

Instance Name	Physical Address
MCAN0	5260 8210h
MCAN1	5261 8210h
MCAN2	5262 8210h
MCAN3	5263 8210h
MCAN4	5264 8210h
MCAN5	5265 8210h
MCAN6	5266 8210h
MCAN7	5267 8210h

Figure 5-18. CFG_TEST Name Register

31	30	29	28	27	26	25	24
NU15							
R							
0h							
23	22	21	20	19	18	17	16
NU15							
R							
0h							
15	14	13	12	11	10	9	8
NU15							
R							
0h							
7	6	5	4	3	2	1	0
RX	TX		LBCK	NU14			
R	R/W		R/W	R			
0h	0h		0h	0h			

Table 5-45. CFG_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	NU15	R	0h	Reserved
7	RX	R	0h	Receive Pin Monitors the actual value of the MCAN RX pin 1'b0 = The CAN bus is dominant 1'b1 = The CAN bus is recessive
6:5	TX	R/W	0h	Control of Transmit Pin 2'b00 = Reset value, the MCAN TX pin controlled by the CAN Core, updated at the end of the CAN bit time 2'b01 = Sample Point can be monitored at the MCAN TX pin 2'b10 = Dominant ('0') level at the MCAN TX pin 2'b11 = Recessive ('1') at the MCAN TX pin
4	LBCK	R/W	0h	Loop Back Mode 1'b0 = Reset value, Loopback Mode is disabled 1'b1 = Loopback Mode is enabled(see Test Modes)

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Table 5-45. CFG_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	NU14	R	0h	Reserved

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5.1.2.19 CFG_RWD Register

5.1.2.19.1 CFG_RWD Register (Offset = 214h) [reset = 0h]

RAM Watchdog. Monitors the READY output of the Message RAM.

Return to Summary Table

Table 5-46. Instance Table

Instance Name	Physical Address
MCAN0	5260 8214h
MCAN1	5261 8214h
MCAN2	5262 8214h
MCAN3	5263 8214h
MCAN4	5264 8214h
MCAN5	5265 8214h
MCAN6	5266 8214h
MCAN7	5267 8214h

Figure 5-19. CFG_RWD Name Register

31	30	29	28	27	26	25	24
NU16							
R							
0h							
23	22	21	20	19	18	17	16
NU16							
R							
0h							
15	14	13	12	11	10	9	8
WDV							
R							
0h							
7	6	5	4	3	2	1	0
WDC							
R/W							
0h							

Table 5-47. CFG_RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU16	R	0h	Reserved
15:8	WDV	R	0h	Watchdog Value Actual Message RAM Watchdog Counter Value.
7:0	WDC	R/W	0h	Watchdog Counter Value Start value of the Message RAM Watchdog Counter. With the reset value of 8'h0 the counter is disabled.

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5.1.2.20 CFG_CCCR Register

5.1.2.20.1 CFG_CCCR Register (Offset = 218h) [reset = 1h]

CC Control Register. Operation mode configuration.

Return to Summary Table

Table 5-48. Instance Table

Instance Name	Physical Address
MCAN0	5260 8218h
MCAN1	5261 8218h
MCAN2	5262 8218h
MCAN3	5263 8218h
MCAN4	5264 8218h
MCAN5	5265 8218h
MCAN6	5266 8218h
MCAN7	5267 8218h

Figure 5-20. CFG_CCCR Name Register

31	30	29	28	27	26	25	24
NU18							
R/W							
0h							
23	22	21	20	19	18	17	16
NU18							
R/W							
0h							
15	14	13	12	11	10	9	8
NU18	TXP	EFBI	PXHD	NU17		BRSE	FDOE
R/W	R/W	R/W	R/W	R		R/W	R/W
0h	0h	0h	0h	0h		0h	0h
7	6	5	4	3	2	1	0
TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	1h

Table 5-49. CFG_CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	NU18	R/W	0h	Reserved
14	TXP	R/W	0h	Transmit Pause If this bit is set, the MCAN module pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame(see Tx Handling) . 1'b0 = Transmit pause disabled 1'b1 = Transmit pause enabled
13	EFBI	R/W	0h	Edge Filtering durign Bus Integration 1'b0 = Edge filtering disabled 1'b1 = Two consecutive dominant tq required to detect an edge for hard synchronization
12	PXHD	R/W	0h	Protocol Exception Handling Disable 1'b0 = Protocol exception handling enabled 1'b1 = Protocol exception handling disabled Note: When protocol exception handling is disabled, the MCAN module will transmit an error frame when it detects a protocol exception condition.

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Table 5-49. CFG_CCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:10	NU17	R	0h	Reserved
9	BRSE	R/W	0h	Bit Rate Switch Enable 1'b0 = Bit rate switching for transmissions disabled 1'b1 = Bit rate switching for transmissions enabled Note: When CAN FD operation is disabled the MCAN_CCCR[8] FDOE = 1'b0, the MCAN_CCCR[9] BRSE bit is not evaluated.
8	FDOE	R/W	0h	FD Operation Enable 1'b0 = FD operation disabled 1'b1 = FD operation enabled
7	TEST	R/W	0h	Test Mode enable 1'b0 = Normal operation. The MCAN_TEST register holds reset values. 1'b1 = Test Mode. Write access to the MCAN_TEST register enabled
6	DAR	R/W	0h	Disable Automatic Regransmission 1'b0 = Automatic retransmission of messages not transmitted successfully enabled 1'b1 = Automatic retransmission disabled
5	MON	R/W	0h	Bus Monitoring Mode The MCAN_CCCR[5] MON bit can only be set by the Host CPU when both MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set to 1. The bit can be reset by the Host CPU at any time. 1'b0 = Bus Monitoring Mode is disabled 1'b1 = Bus Monitoring Mode is enabled
4	CSR	R/W	0h	Clock Stop Request 1'b0 = No clock stop is requested 1'b1 = Clock stop requested. When clock stop is requested, first the MCAN_CCCR[0] INIT bit and then the MCAN_CCCR[3] CSA bit will be set after all pending transfer requests have been completed and the CAN bus reached idle.
3	CSA	R	0h	Clock Stop Acknowledge 1'b0 = No clock stop acknowledged 1'b1 = The MCAN module may be set in power down by stopping MCAN interface clock and MCAN functional clock
2	ASM	R/W	0h	Restricted Operation Mode The MCAN_CCCR[2] ASM bit can only be set by the Host CPU when both MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set to 1. The bit can be reset by the Host CPU at any time. For a description of the Restricted Operation Mode, see Restricted Operation Mode. 1'b0 = Normal CAN operation 1'b1 = Restricted Operation Mode active
1	CCE	R/W	0h	Configuration Change Enable 1'b0 = The Host CPU has no write access to the protected configuration registers 1'b1 = The Host CPU has write access to the protected configuration registers (while the MCAN_CCCR[0] INIT = 1)
0	INIT	R/W	1h	Initialization 1'b0 = Normal Operation 1'b1 = Initialization is started Note: Due to the synchronization mechanism between the two clock domains, there may be a delay until the value written to the MCAN_CCCR[0] INIT bit can be read back. Therefore the software has to assure that the previous value written to the MCAN_CCCR[0] INIT bit has been accepted by Reading the MCAN_CCCR[0] INIT bit before setting the MCAN_CCCR[0] INIT bit to a new value.

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5.1.2.21 CFG_NBTP Register

5.1.2.21.1 CFG_NBTP Register (Offset = 21Ch) [reset = 6000A03h]

Nominal Bit Timing & Prescaler Register. Configuration of arbitration phase bit timing.
This register is only writable if the MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set. The CAN bit time may be programed in the range of 4 to 385 time quanta. The CAN time quantum may be programmed in the range of 1 to 512 MCAN functional clock periods. tq = (MCAN_NBTP[24-16] NBRP + 1) mtq. The MCAN_NBTP[15-8] NTSEG1 field is the sum of Prop_Seg and Phase_Seg1. The MCAN_NBTP[6-0] NTSEG2 field is Phase_Seg2.
Therefore the length of the bit time is (programmed values) [MCAN_NBTP[15-8] NTSEG1 + MCAN_NBTP[6-0] NTSEG2 + 3] tq or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] tq.
The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Return to Summary Table

Table 5-50. Instance Table

Instance Name	Physical Address
MCAN0	5260 821Ch
MCAN1	5261 821Ch
MCAN2	5262 821Ch
MCAN3	5263 821Ch
MCAN4	5264 821Ch
MCAN5	5265 821Ch
MCAN6	5266 821Ch
MCAN7	5267 821Ch

Figure 5-21. CFG_NBTP Name Register

31	30	29	28	27	26	25	24
NSJW							NBRP
R/W							R/W
3h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NBRP							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NTSEG1							
R/W							
Ah							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU19	NTSEG2						
R	R/W						
0h	3h						

Table 5-51. CFG_NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	NSJW	R/W	3h	Nominal Resynchronization Jump Width
24:16	NBRP	R/W	0h	Nominal Baud Rate Prescaler
15:8	NTSEG1	R/W	Ah	Nominal Time segment before sample point
7	NU19	R	0h	Reserved

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Table 5-51. CFG_NBTP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	NTSEG2	R/W	3h	Nominal Time segment after sample point

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5.1.2.22 CFG_TSCC Register

5.1.2.22.1 CFG_TSCC Register (Offset = 220h) [reset = 0h]

Timestamp Counter Configuration. Timestamp counter prescaler setting, selection of internal/external timestamp vector.

Return to Summary Table

Table 5-52. Instance Table

Instance Name	Physical Address
MCAN0	5260 8220h
MCAN1	5261 8220h
MCAN2	5262 8220h
MCAN3	5263 8220h
MCAN4	5264 8220h
MCAN5	5265 8220h
MCAN6	5266 8220h
MCAN7	5267 8220h

Figure 5-22. CFG_TSCC Name Register

31	30	29	28	27	26	25	24
NU21							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU21				TCP			
R				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU20							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU20						TSS	
R						R/W	
0h						0h	

Table 5-53. CFG_TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	NU21	R	0h	Reserved
19:16	TCP	R/W	0h	Timestamp Counter Prescaler Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1-16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Note: With CAN FD an external counter is required for timestamp generation. MCAN_TSCC[1-0] TSS = 2'b10
15:2	NU20	R	0h	Reserved
1:0	TSS	R/W	0h	Timestamp Select 2'b00 = Timestamp counter value always 0 2'b01 = Timestamp counter value incremented according to the MCAN_TSCC[19-16] TCP field 2'b10 = External timestamp counter value used 2'b11 = Same as 2'b00

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5.1.2.23 CFG_TSCV Register

5.1.2.23.1 CFG_TSCV Register (Offset = 224h) [reset = 0h]

Timestamp Counter Value.

Return to Summary Table

Table 5-54. Instance Table

Instance Name	Physical Address
MCAN0	5260 8224h
MCAN1	5261 8224h
MCAN2	5262 8224h
MCAN3	5263 8224h
MCAN4	5264 8224h
MCAN5	5265 8224h
MCAN6	5266 8224h
MCAN7	5267 8224h

Figure 5-23. CFG_TSCV Name Register

31	30	29	28	27	26	25	24
NU22							
R							
0h							
23	22	21	20	19	18	17	16
NU22							
R							
0h							
15	14	13	12	11	10	9	8
TSC							
R/W							
0h							
7	6	5	4	3	2	1	0
TSC							
R/W							
0h							

Table 5-55. CFG_TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU22	R	0h	Reserved
15:0	TSC	R/W	0h	Timestamp Counter The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When the MCAN_TSCC[1-0] TSS = 2'b01, the Timestamp Counter is incremented in multiples of CAN bit times [1-16] depending on the configuration of the MCAN_TSCC[19-16] TCP field. A wrap around sets interrupt flag MCAN_IR[16] TSW. Write access resets the counter to zero. When the MCAN_TSCC[1-0] TSS = 2'b10, the MCAN_TSCV[15-0] TSC field reflects the external Timestamp Counter value. A write access has no impact. Note: A 'wrap around' is a change of the Timestamp Counter value from non-zero to zero not caused by write access to the MCAN_TSCV register.

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5.1.2.24 CFG_TOCC Register

5.1.2.24.1 CFG_TOCC Register (Offset = 228h) [reset = FFFF0000h]

Timeout Counter Configuration
Configuration of timeout period, selection of timeout counter operation mode.

Return to Summary Table

Table 5-56. Instance Table

Instance Name	Physical Address
MCAN0	5260 8228h
MCAN1	5261 8228h
MCAN2	5262 8228h
MCAN3	5263 8228h
MCAN4	5264 8228h
MCAN5	5265 8228h
MCAN6	5266 8228h
MCAN7	5267 8228h

Figure 5-24. CFG_TOCC Name Register

31	30	29	28	27	26	25	24
TOP							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
TOP							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
NU23							
R							
0h							
7	6	5	4	3	2	1	0
NU23					TOS		ETOC
R					R/W		R/W
0h					0h		0h

Table 5-57. CFG_TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TOP	R/W	FFFFh	Timeout Period Start value of the Timeout Counter (down-counter). Configures the Timeout Period.
15:3	NU23	R	0h	Reserved
2:1	TOS	R/W	0h	Timeout Select When operating in Continuous mode, a write to the MCAN_TOCV[15-0] TOC field presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field. Down-counting is started when the first FIFO element is stored. 2'b00 = Continuous operation 2'b01 = Timeout controlled by Tx Event FIFO 2'b10 = Timeout controlled by Rx FIFO 0 2'b11 = Timeout controlled by Rx FIFO 1

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Table 5-57. CFG_TOCC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ETOC	R/W	0h	Enable Timeout Counter 1'b0 = Timeout Counter disabled 1'b1 = Timeout Counter enabled

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5.1.2.25 CFG_TOCV Register

5.1.2.25.1 CFG_TOCV Register (Offset = 22Ch) [reset = FFFFh]

Timeout Counter Value. Read/reset timeout counter.

Return to Summary Table

Table 5-58. Instance Table

Instance Name	Physical Address
MCAN0	5260 822Ch
MCAN1	5261 822Ch
MCAN2	5262 822Ch
MCAN3	5263 822Ch
MCAN4	5264 822Ch
MCAN5	5265 822Ch
MCAN6	5266 822Ch
MCAN7	5267 822Ch

Figure 5-25. CFG_TOCV Name Register

31	30	29	28	27	26	25	24
NU24							
R							
0h							
23	22	21	20	19	18	17	16
NU24							
R							
0h							
15	14	13	12	11	10	9	8
TOC							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
TOC							
R/W							
FFFFh							

Table 5-59. CFG_TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU24	R	0h	Reserved
15:0	TOC	R/W	FFFFh	Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1-16] depending on the configuration of the MCAN_TSCC[19-16] TCP field. When decremented to zero, interrupt flag MCAN_IR[18] TOO is set and the Timeout Counter is stopped. Start and reset/ restart conditions are configured via the MCAN_TOCC[2-1] TOS field.

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5.1.2.26 CFG_ECR Register

5.1.2.26.1 CFG_ECR Register (Offset = 240h) [reset = 0h]

Error Counter Register. State of Rx/Tx Error counter, CAN error logging.

Return to Summary Table

Table 5-60. Instance Table

Instance Name	Physical Address
MCAN0	5260 8240h
MCAN1	5261 8240h
MCAN2	5262 8240h
MCAN3	5263 8240h
MCAN4	5264 8240h
MCAN5	5265 8240h
MCAN6	5266 8240h
MCAN7	5267 8240h

Figure 5-26. CFG_ECR Name Register

31	30	29	28	27	26	25	24
NU25							
R							
0h							
23	22	21	20	19	18	17	16
CEL							
R							
0h							
15	14	13	12	11	10	9	8
RP	REC						
R	R						
0h	0h						
7	6	5	4	3	2	1	0
TEC							
R							
0h							

Table 5-61. CFG_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NU25	R	0h	Reserved
23:16	CEL	R	0h	CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to the MCAN_ECR[23-16] CEL field. The counter stops at FFh; the next increment of the MCAN_ECR[7-0] TEC or MCAN_ECR[14-8] REC fields sets interrupt flag MCAN_IR[22] ELO.
15	RP	R	0h	Recieve Error Passive 1'b0 = The Receive Error Counter is below the error passive level of 128 1'b1 = The Receive Error Counter has reached the error passive level of 128
14:8	REC	R	0h	Recieve Error Counter Actual state of the Receive Error Counter, values between 0 and 127.

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Table 5-61. CFG_ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	TEC	R	0h	Transmit Error Counter Actual state of the Transmit Error Counter, values between 0 and 255. Note: When the MCAN_CCCR[2] ASM bit is set, the CAN protocol controller does not increment the MCAN_ECR[7-0] TEC and MCAN_ECR[14-8] REC fields when a CAN protocol error is detected, but the MCAN_ECR[23-16] CEL field is still incremented.

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5.1.2.27 CFG_PSR Register

5.1.2.27.1 CFG_PSR Register (Offset = 244h) [reset = 707h]

Protocol Status Register. CAN protocol controller status, transmitter delay compensation value.

Return to Summary Table

Table 5-62. Instance Table

Instance Name	Physical Address
MCAN0	5260 8244h
MCAN1	5261 8244h
MCAN2	5262 8244h
MCAN3	5263 8244h
MCAN4	5264 8244h
MCAN5	5265 8244h
MCAN6	5266 8244h
MCAN7	5267 8244h

Figure 5-27. CFG_PSR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">NU27</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td>NU27</td><td colspan="7">TDCV</td></tr>
<tr><td>R</td><td colspan="7">R</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>NU26</td><td>PXE</td><td>RFDF</td><td>RBRS</td><td>RESI</td><td colspan="3">DLEC</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td>R</td><td>R</td><td colspan="3">R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td colspan="3">7h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>BO</td><td>EW</td><td>EP</td><td colspan="2">ACT</td><td colspan="3">LEC</td></tr>
<tr><td>R</td><td>R</td><td>R</td><td colspan="2">R</td><td colspan="3">R</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td colspan="2">0h</td><td colspan="3">7h</td></tr>
</table>

Table 5-63. CFG_PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	NU27	R	0h	Reserved
22:16	TDCV	R	0h	Transmitter Delay Compensation Value Position of the secondary sample point, defined by the sum of the measured delay from the MCAN TX to MCAN RX pins and the MCAN_TDCR[14-8] TDCO field. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq.
15	NU26	R	0h	Reserved
14	PXE	R	0h	Protocol Exception Event 1'b0 = No protocol exception event occurred since last read access 1'b1 = Protocol exception event occurred

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Table 5-63. CFG_PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RFDF	R	0h	Recieved a CAN FD Message This bit is set independent of acceptance filtering. 1'b0 = Since this bit was reset by the Host CPU, no CAN FD message has been received 1'b1 = Message in CAN FD format with FDF flag set has been received
12	RBRS	R	0h	BRS flag of last recieved CAN FD Message This bit is set together with the MCAN_PSR[13] RFDF bit, independent of acceptance filtering. 1'b0 = Last received CAN FD message did not have its BRS flag set 1'b1 = Last received CAN FD message had its BRS flag set
11	RESI	R	0h	ESI flag of last recieved CAN FD Message This bit is set together with the MCAN_PSR[13] RFDF bit, independent of acceptance filtering. 1'b0 = Last received CAN FD message did not have its ESI flag set 1'b1 = Last received CAN FD message had its ESI flag set
10:8	DLEC	R	7h	Data Phase Last Error Code Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for the MCAN_PSR[2-0] LEC field. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error.
7	BO	R	0h	Bus_Off status 1'b0 = The MCAN module is not Bus_Off 1'b1 = The MCAN module is in Bus_Off state
6	EW	R	0h	Warning Status 1'b0 = Both error counters are below the Error_Warning limit of 96 1'b1 = At least one of error counter has reached the Error_Warning limit of 96
5	EP	R	0h	Error Passive 1'b0 = The MCAN module is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1'b1 = The MCAN module is in the Error_Passive state
4:3	ACT	R	0h	Activity Monitors the module's CAN communication state. 2'b00 = Synchronizing - node is synchronizing on CAN communication 2'b01 = Idle - node is neither receiver nor transmitter 2'b10 = Receiver - node is operating as receiver 2'b11 = Transmitter - node is operating as transmitter Note: ACT is set to 0 by a Protocol Exception Event.

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Table 5-63. CFG_PSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	LEC	R	7h	Last Error Code The MCAN_PSR[2-0] LEC field indicates the type of the last error to occur on the CAN bus. This field will be cleared to 0hwhen a message has been transferred (reception or transmission) without error. 3'b000 = No Error: No error occurred since the MCAN_PSR[2-0] LEC field has been reset by successful reception or transmission. 3'b001 = Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 3'b010 = Form Error: A fixed format part of a received frame has the wrong format. 3'b011 = AckError: The message transmitted by the MCAN module was not acknowledged by another node. 3'b100 = Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant. 3'b101 = Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the Host CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 3'b110 = CRCError: The CRC check sum of a received message was incorrect. The CRC of an incom-ing message does not match with the CRC calculated from the received data. 3'b111 = NoChange: Any read access to the Protocol Status Register re-initializes the MCAN_PSR[2-0] LEC field to 3'b111. When the MCAN_PSR[2-0] LEC field shows the value 3'b111, no CAN bus event was detected since the last Host CPU read access to the Protocol Status Register. Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in the MCAN_PSR[10-8] DLEC field instead of the MCAN_PSR[2-0] LEC field. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error.

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5.1.2.28 CFG_TDCR Register

5.1.2.28.1 CFG_TDCR Register (Offset = 248h) [reset = 0h]

Transmitter Delay Comensation Register. Configuration of transmitter delay compensation offset and filter window length.

Return to Summary Table

Table 5-64. Instance Table

Instance Name	Physical Address
MCAN0	5260 8248h
MCAN1	5261 8248h
MCAN2	5262 8248h
MCAN3	5263 8248h
MCAN4	5264 8248h
MCAN5	5265 8248h
MCAN6	5266 8248h
MCAN7	5267 8248h

Figure 5-28. CFG_TDCR Name Register

31	30	29	28	27	26	25	24
NU29							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU29							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU29	TDCO						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU28	TDCF						
R	R/W						
0h	0h						

Table 5-65. CFG_TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	NU29	R	0h	Reserved
14:8	TDCO	R/W	0h	Transmitter Delay Compensation Offset Offset value defining the distance between the measured delay from the MCAN RX and MCAN TX pins and the secondary sample point. Valid values are 0 to 127 mtq 0h7Fh).
7	NU28	R	0h	Reserved
6:0	TDCF	R/W	0h	Transmitter Delay Compensation Filter Window Length Defines the minimum value for the SSP position, dominant edges on the MCAN RX pin that would result in an earlier SSP position are ignored for transmitter delay measure-ment. The feature is enabled when the MCAN_TDCR[6-0] TDCF field is configured to a value greater than the MCAN_TDCR[14-8] TDCO field. Valid values are 0 to 127 mtq

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5.1.2.29 CFG_IR Register

5.1.2.29.1 CFG_IR Register (Offset = 250h) [reset = 0h]

Interrupt Register. The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host CPU clears them. A flag is cleared by writing a 1h to the corresponding bit position. Writing a 0h has no effect.

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Table 5-66. Instance Table

Instance Name	Physical Address
MCAN0	5260 8250h
MCAN1	5261 8250h
MCAN2	5262 8250h
MCAN3	5263 8250h
MCAN4	5264 8250h
MCAN5	5265 8250h
MCAN6	5266 8250h
MCAN7	5267 8250h

Figure 5-29. CFG_IR Name Register

31	30	29	28	27	26	25	24
NU30		ARA	PED	PEA	WDI	BO	EW
R		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-67. CFG_IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	NU30	R	0h	Reserved
29	ARA	R/W	0h	Access to Reserved Address
28	PED	R/W	0h	Protocol Error in data Phase
27	PEA	R/W	0h	Protocol Error in Arbitration Phase
26	WDI	R/W	0h	Watchdog Interrupt
25	BO	R/W	0h	Bus_Off Status
24	EW	R/W	0h	Warning Status
23	EP	R/W	0h	Error Passive
22	ELO	R/W	0h	Error Logging Overflow
21	BEU	R/W	0h	Bit Error Uncorrected
20	BEC	R/W	0h	Bit Error Corrected

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Table 5-67. CFG_IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	DRX	R/W	0h	Message stored to Dedicated Rx Buffer
18	TOO	R/W	0h	Timeout Occurred
17	MRAF	R/W	0h	Message RAM Access Failure The flag is set, when the Rx Handler: i. has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. ii. was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated respectively the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the MCAN module is switched into Restricted Operation Mode (see Restricted Operation Mode). To leave Restricted Operation Mode, the Host CPU has to reset the MCAN_CCCR[2] ASM bit. 1'b0 = No Message RAM access failure occurred 1'b1 = Message RAM access failure occurred
16	TSW	R/W	0h	Timestamp Wraparound
15	TEFL	R/W	0h	Tx Event FIFO Element Lost
14	TEFF	R/W	0h	Tx Event FIFO Full
13	TEFW	R/W	0h	Tx Event FIFO Watermark Reached
12	TEFN	R/W	0h	Tx Event FIFO New Entry
11	TFE	R/W	0h	Tx FIFO Empty
10	TCF	R/W	0h	Transmission Cancellation Finished
9	TC	R/W	0h	Transmission Complete
8	HPM	R/W	0h	High Priority Message
7	RF1L	R/W	0h	Rx FIFO 1 Message Lost
6	RF1F	R/W	0h	Rx FIFO 1 Full
5	RF1W	R/W	0h	Rx FIFO 1 Watermark Reached
4	RF1N	R/W	0h	Rx FIFO 1 New Message
3	RF0L	R/W	0h	Rx FIFO 0 Message Lost
2	RF0F	R/W	0h	Rx FIFO 0 Full
1	RF0W	R/W	0h	Rx FIFO 0 Watermark Reached
0	RF0N	R/W	0h	Rx FIFO 0 New Message

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5.1.2.30 CFG_IE Register

5.1.2.30.1 CFG_IE Register (Offset = 254h) [reset = 0h]

Interrupt Enable Register. The settings in the Interrupt Enable register determine which status changes in the MCAN_IR register are signalled on an interrupt line.

Return to Summary Table

Table 5-68. Instance Table

Instance Name	Physical Address
MCAN0	5260 8254h
MCAN1	5261 8254h
MCAN2	5262 8254h
MCAN3	5263 8254h
MCAN4	5264 8254h
MCAN5	5265 8254h
MCAN6	5266 8254h
MCAN7	5267 8254h

Figure 5-30. CFG_IE Name Register

31	30	29	28	27	26	25	24
NU31		ARAE	PEDE	PEAE	WDIE	BOE	EWE
R		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-69. CFG_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	NU31	R	0h	Reserved
29	ARAE	R/W	0h	Accees to Reserve Address Interrupt Enable
28	PEDE	R/W	0h	Protocol Error in Data Phase Interrupt Enable
27	PEAE	R/W	0h	Protocol Error in Arbitration Phase Interrupt Enable
26	WDIE	R/W	0h	Watchdog Interrupt Enable
25	BOE	R/W	0h	Bus_Off Status Interrupt Enable
24	EWE	R/W	0h	Warning Status Interrupt Enable
23	EPE	R/W	0h	Error Passive Interrupt Enable
22	ELOE	R/W	0h	Error Logging Overflow Interrupt Enable
21	BEUE	R/W	0h	Bit Error Uncorrected Interrupt Enable
20	BECE	R/W	0h	Bit Error Corrected Interrupt Enable
19	DRX	R/W	0h	Message stored to Dedicated Rx Buffer Interrupt Enable

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Table 5-69. CFG_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	TOOE	R/W	0h	Timeout Occurred Interrupt Enable
17	MRAFE	R/W	0h	Message RAM Access Failure Interrupt Enable
16	TSWE	R/W	0h	Timestamp Wraparound Interrupt Enable
15	TEFLE	R/W	0h	Tx Event FIFO Event Lost Interrupt Enable
14	TEFFE	R/W	0h	Tx Event FIFO Full Interrupt Enable
13	TEFWE	R/W	0h	Tx Event FIFO Watermark Reached Interrupt enable
12	TEFNE	R/W	0h	Tx Event FIFO New Entry Interrupt Enable
11	TFEE	R/W	0h	Tx FIFO Empty Interrupt Enable
10	TCFE	R/W	0h	Transmission Cancellation Finishied Interrupt Enable
9	TCE	R/W	0h	Transmission Completed Interrupt Enable
8	HPME	R/W	0h	High Priority message Interrupt Enable
7	RF1LE	R/W	0h	Rx FIFO 1 Message Lost Interrupt Enable
6	RF1FE	R/W	0h	Rx FIFO 1 Full Interrupt Enable
5	RF1WE	R/W	0h	Rx FIFO 1 Watermark Reached Interrupt Enable
4	RF1NE	R/W	0h	Rx FIFO 1 New Message Interrupt Enable
3	RF0LE	R/W	0h	Rx FIFO 0 Message Lost Interrupt Enable
2	RF0FE	R/W	0h	Rx FIFO 0 Full Interrupt Enable
1	RF0WE	R/W	0h	Rx FIFO 0 Watermark Reached Interrupt Enable
0	RF0NE	R/W	0h	Rx FIFO 0 New Message Interrupt Enable

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5.1.2.31 CFG_ILS Register

5.1.2.31.1 CFG_ILS Register (Offset = 258h) [reset = 0h]

Interrupt line select. The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the MCAN_IR register to one of the two module interrupt lines. For assigning interrupt to INT0, write 0 to corresponding bit field and for assigning interrupt to INT1, write 1 to corresponding bit field.

Return to Summary Table

Table 5-70. Instance Table

Instance Name	Physical Address
MCAN0	5260 8258h
MCAN1	5261 8258h
MCAN2	5262 8258h
MCAN3	5263 8258h
MCAN4	5264 8258h
MCAN5	5265 8258h
MCAN6	5266 8258h
MCAN7	5267 8258h

Figure 5-31. CFG_ILS Name Register

31	30	29	28	27	26	25	24
NU32		ARAL	PEDL	PEAL	WDIL	BOL	EWL
R		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-71. CFG_ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	NU32	R	0h	Reserved
29	ARAL	R/W	0h	Accees to Reserve Address Interrupt Line
28	PEDL	R/W	0h	Protocol Error in Data Phase Interrupt Line
27	PEAL	R/W	0h	Protocol Error in Arbitration Phase Interrupt Line
26	WDIL	R/W	0h	Watchdog Interrupt Line
25	BOL	R/W	0h	Bus_Off Status Interrupt Line
24	EWL	R/W	0h	Warning Status Interrupt Line
23	EPL	R/W	0h	Error Passive Interrupt Line
22	ELOL	R/W	0h	Error Logging Overflow Interrupt Line
21	BEUL	R/W	0h	Bit Error Uncorrected Interrupt Line
20	BECL	R/W	0h	Bit Error Corrected Interrupt Line

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Table 5-71. CFG_ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	DRXL	R/W	0h	Message stored to Dedicated Rx Buffer Interrupt Line
18	TOOL	R/W	0h	Timeout Occurred Interrupt Line
17	MRAFL	R/W	0h	Message RAM Access Failure Interrupt Line
16	TSWL	R/W	0h	Timestamp Wraparound Interrupt Line
15	TEFLL	R/W	0h	Tx Event FIFO Event Lost Interrupt Line
14	TEFFL	R/W	0h	Tx Event FIFO Full Interrupt Line
13	TEFWL	R/W	0h	Tx Event FIFO Watermark Reached Interrupt Line
12	TEFNL	R/W	0h	Tx Event FIFO New Entry Interrupt Line
11	TFEL	R/W	0h	Tx FIFO Empty Interrupt Line
10	TCFL	R/W	0h	Transmission Cancellation Finishied Interrupt Line
9	TCL	R/W	0h	Transmission Completed Interrupt Line
8	HPML	R/W	0h	High Priority message Interrupt Line
7	RF1LL	R/W	0h	Rx FIFO 1 Message Lost Interrupt Line
6	RF1FL	R/W	0h	Rx FIFO 1 Full Interrupt Line
5	RF1WL	R/W	0h	Rx FIFO 1 Watermark Reached Interrupt Line
4	RF1NL	R/W	0h	Rx FIFO 1 New Message Interrupt Line
3	RF0LL	R/W	0h	Rx FIFO 0 Message Lost Interrupt Line
2	RF0FL	R/W	0h	Rx FIFO 0 Full Interrupt Line
1	RF0WL	R/W	0h	Rx FIFO 0 Watermark Reached Interrupt Line
0	RF0NL	R/W	0h	Rx FIFO 0 New Message Interrupt Line

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5.1.2.32 CFG_ILE Register

5.1.2.32.1 CFG_ILE Register (Offset = 25Ch) [reset = 0h]

Interrupt line enable Register. Enable/Disable interrupt lines INT0/INT1.

Return to Summary Table

Table 5-72. Instance Table

Instance Name	Physical Address
MCAN0	5260 825Ch
MCAN1	5261 825Ch
MCAN2	5262 825Ch
MCAN3	5263 825Ch
MCAN4	5264 825Ch
MCAN5	5265 825Ch
MCAN6	5266 825Ch
MCAN7	5267 825Ch

Figure 5-32. CFG_ILE Name Register

31	30	29	28	27	26	25	24
NU33							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU33							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU33							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU33						EINT1	EINT0
R						R/W	R/W
0h						0h	0h

Table 5-73. CFG_ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU33	R	0h	Reserved
1	EINT1	R/W	0h	Enable Interrupt Line 1
0	EINT0	R/W	0h	Enable Interrupt Line 0

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5.1.2.33 CFG_GFC Register

5.1.2.33.1 CFG_GFC Register (Offset = 280h) [reset = 0h]

Global Filter Configuration. Handling of non-matching frames and remote frames. Global settings for Message ID filtering. The MCAN_GFC register controls the filter path for standard and extended messages.

Return to Summary Table

Table 5-74. Instance Table

Instance Name	Physical Address
MCAN0	5260 8280h
MCAN1	5261 8280h
MCAN2	5262 8280h
MCAN3	5263 8280h
MCAN4	5264 8280h
MCAN5	5265 8280h
MCAN6	5266 8280h
MCAN7	5267 8280h

Figure 5-33. CFG_GFC Name Register

31	30	29	28	27	26	25	24
NU34							
R							
0h							
23	22	21	20	19	18	17	16
NU34							
R							
0h							
15	14	13	12	11	10	9	8
NU34							
R							
0h							
7	6	5	4	3	2	1	0
NU34		ANFS		ANFE		RRFS	RRFE
R		R/W		R/W		R/W	R/W
0h		0h		0h		0h	0h

Table 5-75. CFG_GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	NU34	R	0h	Reserved
5:4	ANFS	R/W	0h	Accept Non-matching Frames Standard Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 2'b00 = Accept in Rx FIFO 0 2'b01 = Accept in Rx FIFO 1 2'b10 = Reject 2'b11 = Reject
3:2	ANFE	R/W	0h	Accept Non-matching Frames Extended Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 2'b00 = Accept in Rx FIFO 0 2'b01 = Accept in Rx FIFO 1 2'b10 = Reject 2'b11 = Reject

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Table 5-75. CFG_GFC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RRFS	R/W	0h	Reject Remote Frames Standard 1'b0 = Filter remote frames with 11-bit standard IDs 1'b1 = Reject all remote frames with 11-bit standard IDs
0	RRFE	R/W	0h	Reject Remote Frames Extended 1'b0 = Filter remote frames with 29-bit extended IDs 1'b1 = Reject all remote frames with 29-bit extended IDs

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5.1.2.34 CFG_SIDFC Register

5.1.2.34.1 CFG_SIDFC Register (Offset = 284h) [reset = 0h]

Standard ID Filter Configuration. Settings for 11-bit standard Message ID filtering. The Standard ID Filter Configuration controls the filter path for standard messages.

Return to Summary Table

Table 5-76. Instance Table

Instance Name	Physical Address
MCAN0	5260 8284h
MCAN1	5261 8284h
MCAN2	5262 8284h
MCAN3	5263 8284h
MCAN4	5264 8284h
MCAN5	5265 8284h
MCAN6	5266 8284h
MCAN7	5267 8284h

Figure 5-34. CFG_SIDFC Name Register

31	30	29	28	27	26	25	24
NU36							
R							
0h							
23	22	21	20	19	18	17	16
LSS_S							
R/W							
0h							
15	14	13	12	11	10	9	8
FLSSA_S							
R/W							
0h							
7	6	5	4	3	2	1	0
FLSSA_S						NU35	
R/W						R	
0h						0h	

Table 5-77. CFG_SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NU36	R	0h	Reserved
23:16	LSS_S	R/W	0h	List Size Standard 8'h00 = No standard Message ID filter 8'h01-8'h80 (1-128) = Number of standard Message ID filter elements > 8'h80 (128) = Values greater than 128 are interpreted as 128
15:2	FLSSA_S	R/W	0h	Filter List Standard Start Address Start address of standard Message ID filter list (32-bit word address, see Message RAM Configuration).
1:0	NU35	R	0h	Reserved

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5.1.2.35 CFG_XIDFC Register

5.1.2.35.1 CFG_XIDFC Register (Offset = 288h) [reset = 0h]

Extended ID Filter Configuration. Settings for 29-bit extended Message ID filtering. The Extended ID Filter Configuration controls the filter path for standard messages.

Return to Summary Table

Table 5-78. Instance Table

Instance Name	Physical Address
MCAN0	5260 8288h
MCAN1	5261 8288h
MCAN2	5262 8288h
MCAN3	5263 8288h
MCAN4	5264 8288h
MCAN5	5265 8288h
MCAN6	5266 8288h
MCAN7	5267 8288h

Figure 5-35. CFG_XIDFC Name Register

31	30	29	28	27	26	25	24
NU38							
R							
0h							
23	22	21	20	19	18	17	16
LSS_X							
R/W							
0h							
15	14	13	12	11	10	9	8
FLSSA_X							
R/W							
0h							
7	6	5	4	3	2	1	0
FLSSA_X						NU37	
R/W						R	
0h						0h	

Table 5-79. CFG_XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NU38	R	0h	Reserved
23:16	LSS_X	R/W	0h	List Size Extended 8'h00 = No extended Message ID filter 8'h01-8'h40 (1-64) = Number of extended Message ID filter elements > 8'h40 (64) = Values greater than 64 are interpreted as 64
15:2	FLSSA_X	R/W	0h	Filter List Extended Start Address Start address of extended Message ID filter list (32-bit word address, see Message RAM Configuration).
1:0	NU37	R	0h	Reserved

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5.1.2.36 CFG_XIDAM Register

5.1.2.36.1 CFG_XIDAM Register (Offset = 290h) [reset = 1FFFFFFFh]

Extended ID and Mask.

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Table 5-80. Instance Table

Instance Name	Physical Address
MCAN0	5260 8290h
MCAN1	5261 8290h
MCAN2	5262 8290h
MCAN3	5263 8290h
MCAN4	5264 8290h
MCAN5	5265 8290h
MCAN6	5266 8290h
MCAN7	5267 8290h

Figure 5-36. CFG_XIDAM Name Register

31	30	29	28	27	26	25	24
NU39			EIDM				
R			R/W				
0h			1FFFFFFFh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EIDM							
R/W							
1FFFFFFFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EIDM							
R/W							
1FFFFFFFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EIDM							
R/W							
1FFFFFFFh							

Table 5-81. CFG_XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	NU39	R	0h	Reserved
28:0	EIDM	R/W	1FFFFFFFh	Extended ID Mask. For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active.

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5.1.2.37 CFG_HPMS Register

5.1.2.37.1 CFG_HPMS Register (Offset = 294h) [reset = 0h]

High Priority Message Status. Status monitoring of incoming high priority messages. This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

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Table 5-82. Instance Table

Instance Name	Physical Address
MCAN0	5260 8294h
MCAN1	5261 8294h
MCAN2	5262 8294h
MCAN3	5263 8294h
MCAN4	5264 8294h
MCAN5	5265 8294h
MCAN6	5266 8294h
MCAN7	5267 8294h

Figure 5-37. CFG_HPMS Name Register

31	30	29	28	27	26	25	24
NU40							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU40							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FLST	FIDX						
R	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MSI		BIDX					
R		R					
0h		0h					

Table 5-83. CFG_HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU40	R	0h	Reserved
15	FLST	R	0h	Filter List Indicates the filter list of the matching filter element. 1'b0 = Standard Filter List 1'b1 = Extended Filter List
14:8	FIDX	R	0h	Filter Index Index of matching filter element. Range is 0 to MCAN_SIDFC[23-16] LSS - 1 respectively MCAN_XIDFC[22-16] LSE - 1.
7:6	MSI	R	0h	Message Storeage Indicator 2'b00 = No FIFO selected 2'b01 = FIFO message lost 2'b10 = Message stored in FIFO 0 2'b11 = Message stored in FIFO 1

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Table 5-83. CFG_HPMS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	BIDX	R	0h	Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when the MCAN_HPMS[7-6] MSI = 1.

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5.1.2.38 CFG_NDAT1 Register

5.1.2.38.1 CFG_NDAT1 Register (Offset = 298h) [reset = 0h]

New Data 1 register. NewData flags of dedicated Rx buffers 0-31. The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host CPU clears them. Aflag is cleared by writing a 1h to the corresponding bit position. Writing a 0h has no effect. A hard reset will clear the register .

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Table 5-84. Instance Table

Instance Name	Physical Address
MCAN0	5260 8298h
MCAN1	5261 8298h
MCAN2	5262 8298h
MCAN3	5263 8298h
MCAN4	5264 8298h
MCAN5	5265 8298h
MCAN6	5266 8298h
MCAN7	5267 8298h

Figure 5-38. CFG_NDAT1 Name Register

31	30	29	28	27	26	25	24
ND0_31							
R/W							
0h							
23	22	21	20	19	18	17	16
ND0_31							
R/W							
0h							
15	14	13	12	11	10	9	8
ND0_31							
R/W							
0h							
7	6	5	4	3	2	1	0
ND0_31							
R/W							
0h							

Table 5-85. CFG_NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ND0_31	R/W	0h	New Data 31-0

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5.1.2.39 CFG_NDAT2 Register

5.1.2.39.1 CFG_NDAT2 Register (Offset = 29Ch) [reset = 0h]

New Data 2 register. NewData flags of dedicated Rx buffers 32-63. The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host CPU clears them. A flag is cleared by writing a 1h to the corresponding bit position. Writing a 0h has no effect. A hard reset will clear the register .

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Table 5-86. Instance Table

Instance Name	Physical Address
MCAN0	5260 829Ch
MCAN1	5261 829Ch
MCAN2	5262 829Ch
MCAN3	5263 829Ch
MCAN4	5264 829Ch
MCAN5	5265 829Ch
MCAN6	5266 829Ch
MCAN7	5267 829Ch

Figure 5-39. CFG_NDAT2 Name Register

31	30	29	28	27	26	25	24
ND32_63							
R/W							
0h							
23	22	21	20	19	18	17	16
ND32_63							
R/W							
0h							
15	14	13	12	11	10	9	8
ND32_63							
R/W							
0h							
7	6	5	4	3	2	1	0
ND32_63							
R/W							
0h							

Table 5-87. CFG_NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ND32_63	R/W	0h	New Data 63-32

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5.1.2.40 CFG_RXF0C Register

5.1.2.40.1 CFG_RXF0C Register (Offset = 2A0h) [reset = 0h]

Rx FIFO 0 Configuration register. FIFO 0 operation mode, watermark, size and start address.

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Table 5-88. Instance Table

Instance Name	Physical Address
MCAN0	5260 82A0h
MCAN1	5261 82A0h
MCAN2	5262 82A0h
MCAN3	5263 82A0h
MCAN4	5264 82A0h
MCAN5	5265 82A0h
MCAN6	5266 82A0h
MCAN7	5267 82A0h

Figure 5-40. CFG_RXF0C Name Register

31	30	29	28	27	26	25	24
F0OM	F0WM						
R/W	R/W						
0h	0h						
23	22	21	20	19	18	17	16
NU42_1	F0S						
R	R/W						
0h	0h						
15	14	13	12	11	10	9	8
NU42	F0SA						
R	R/W						
0h	0h						
7	6	5	4	3	2	1	0
F0SA						NU41	
R/W						R	
0h						0h	

Table 5-89. CFG_RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	R/W	0h	Rx FIFO 0 Operation Mode FIFO 0 can be operated in blocking or in overwrite mode (see Rx FIFOs). 1'b0 = FIFO 0 blocking mode 1'b1 = FIFO 0 overwrite mode
30:24	F0WM	R/W	0h	Rx FIFO 0 Watermark 7'h00 = Watermark interrupt disabled 7'h01-7'h40 (1-64) = Level for Rx FIFO 0 watermark interrupt (MCAN_IR[1] RF0W) > 7'h40 (64) = Watermark interrupt disabled
23	NU42_1	R	0h	Reserved
22:16	F0S	R/W	0h	Rx FIFO 0 Size 7'h00 = No Rx FIFO 0 7'h01-7'h40 (1-64) = Number of Rx FIFO 0 elements > 7'h40 (64) = Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to MCAN_RXF0C[22-16] F0S - 1.

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Table 5-89. CFG_RXF0C Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	NU42	R	0h	Reserved
14:2	F0SA	R/W	0h	Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM (32-bit word address, see Message RAM Configuration).
1:0	NU41	R	0h	Reserved

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5.1.2.41 CFG_RXF0S Register

5.1.2.41.1 CFG_RXF0S Register (Offset = 2A4h) [reset = 0h]

Rx FIFO 0 Status register. FIFO 0 message lost/full indication, put index, get index and fill level.

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Table 5-90. Instance Table

Instance Name	Physical Address
MCAN0	5260 82A4h
MCAN1	5261 82A4h
MCAN2	5262 82A4h
MCAN3	5263 82A4h
MCAN4	5264 82A4h
MCAN5	5265 82A4h
MCAN6	5266 82A4h
MCAN7	5267 82A4h

Figure 5-41. CFG_RXF0S Name Register

31	30	29	28	27	26	25	24
NU46						RF0L	F0F
R						R	R
0h						0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU45		F0PI					
R		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU44		F0GI					
R		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU43	F0FL						
R	R						
0h	0h						

Table 5-91. CFG_RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	NU46	R	0h	Reserved
25	RF0L	R	0h	Rx FIFO 0 Message Lost This bit is a copy of interrupt flag MCAN_IR[3] RF0L. When the MCAN_IR[3] RF0L flag is reset, this bit is also reset. 1'b0 = No Rx FIFO 0 message lost 1'b1 = Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Note: OverWriting the oldest message when the MCAN_RXF0C[31] F0OM = 1'b1 will not set this flag.
24	F0F	R	0h	Rx FIFO 0 Full
23:22	NU45	R	0h	Reserved
21:16	F0PI	R	0h	Rx FIFO 0 Put Index
15:14	NU44	R	0h	Reserved
13:8	F0GI	R	0h	Rx FIFO 0 Get Index
7	NU43	R	0h	Reserved

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Table 5-91. CFG_RXF0S Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	F0FL	R	0h	Rx FIFO 0 Fill Level

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5.1.2.42 CFG_RXF0A Register

5.1.2.42.1 CFG_RXF0A Register (Offset = 2A8h) [reset = 0h]

Rx FIFO 0 Acknowledge register. FIFO 0 acknowledge last index of read buffers, updates get index and fill level.

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Table 5-92. Instance Table

Instance Name	Physical Address
MCAN0	5260 82A8h
MCAN1	5261 82A8h
MCAN2	5262 82A8h
MCAN3	5263 82A8h
MCAN4	5264 82A8h
MCAN5	5265 82A8h
MCAN6	5266 82A8h
MCAN7	5267 82A8h

Figure 5-42. CFG_RXF0A Name Register

31	30	29	28	27	26	25	24
NU47							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU47							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU47							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU47		F0AI					
R		R/W					
0h		0h					

Table 5-93. CFG_RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	NU47	R	0h	Reserved
5:0	F0AI	R/W	0h	Rx FIFO 0 Acknowledge Index After the Host CPU has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to the MCAN_RXF0A[5-0] F0AI field. This will set the Rx FIFO 0 Get Index MCAN_RXF0S[13-8] F0GI field to the MCAN_RXF0A[5-0] F0AI field + 1 and update the FIFO 0 Fill Level MCAN_RXF0S[6-0] F0FL field.

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5.1.2.43 CFG_RXBC Register

5.1.2.43.1 CFG_RXBC Register (Offset = 2ACh) [reset = 0h]

Rx Buffer Configuration register. Start address of Rx buffer section.

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Table 5-94. Instance Table

Instance Name	Physical Address
MCAN0	5260 82ACh
MCAN1	5261 82ACh
MCAN2	5262 82ACh
MCAN3	5263 82ACh
MCAN4	5264 82ACh
MCAN5	5265 82ACh
MCAN6	5266 82ACh
MCAN7	5267 82ACh

Figure 5-43. CFG_RXBC Name Register

31	30	29	28	27	26	25	24
NU49							
R							
0h							
23	22	21	20	19	18	17	16
NU49							
R							
0h							
15	14	13	12	11	10	9	8
RBSA							
R/W							
0h							
7	6	5	4	3	2	1	0
RBSA						NU48	
R/W						R	
0h						0h	

Table 5-95. CFG_RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU49	R	0h	Reserved
15:2	RBSA	R/W	0h	Rx Buffer Start Address
1:0	NU48	R	0h	Reserved

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5.1.2.44 CFG_RXF1C Register

5.1.2.44.1 CFG_RXF1C Register (Offset = 2B0h) [reset = 0h]

Rx FIFO 1 Configuration register. FIFO 1 operation mode, watermark, size and start address.

Return to Summary Table

Table 5-96. Instance Table

Instance Name	Physical Address
MCAN0	5260 82B0h
MCAN1	5261 82B0h
MCAN2	5262 82B0h
MCAN3	5263 82B0h
MCAN4	5264 82B0h
MCAN5	5265 82B0h
MCAN6	5266 82B0h
MCAN7	5267 82B0h

Figure 5-44. CFG_RXF1C Name Register

31	30	29	28	27	26	25	24
F1OM	F1WM						
R/W	R/W						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU50_1	F1S						
R	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU50	F1SA						
R	R/W						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
F1SA						NU499	
R/W						R	
0h						0h	

Table 5-97. CFG_RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	R/W	0h	Rx FIFO 1 Operation Mode FIFO 1 can be operated in blocking or in overwrite mode (see Rx FIFOs). 1'b0 = FIFO 1 blocking mode 1'b1 = FIFO 1 overwrite mode
30:24	F1WM	R/W	0h	Rx FIFO 1 Watermark 7'h00 = Watermark interrupt disabled 7'h01-7'h40 (1-64) = Level for Rx FIFO 1 watermark interrupt (MCAN_IR[5] RF1W) > 7'h40 (64) = Watermark interrupt disabled
23	NU50_1	R	0h	Reserved
22:16	F1S	R/W	0h	Rx FIFO 1 Size 7'h00 = No Rx FIFO 1 7'h01-7'h40 (1-64) = Number of Rx FIFO 1 elements > 7'h40 (64) = Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to MCAN_RXF1C[22-16] F1S - 1.

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Table 5-97. CFG_RXF1C Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	NU50	R	0h	Reserved
14:2	F1SA	R/W	0h	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see Message RAM Configuration).
1:0	NU499	R	0h	Reserved

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5.1.2.45 CFG_RXF1S Register

5.1.2.45.1 CFG_RXF1S Register (Offset = 2B4h) [reset = 0h]

Rx FIFO 1 Status register. FIFO 1 message lost/full indication, put index, get index and fill level.

Return to Summary Table

Table 5-98. Instance Table

Instance Name	Physical Address
MCAN0	5260 82B4h
MCAN1	5261 82B4h
MCAN2	5262 82B4h
MCAN3	5263 82B4h
MCAN4	5264 82B4h
MCAN5	5265 82B4h
MCAN6	5266 82B4h
MCAN7	5267 82B4h

Figure 5-45. CFG_RXF1S Name Register

31	30	29	28	27	26	25	24
NU54						RF1L	F1F
R						R	R
0h						0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU53		F1PI					
R		R					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU52		F1GI					
R		R					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU51	F1FL						
R	R						
0h	0h						

Table 5-99. CFG_RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	NU54	R	0h	Reserved
25	RF1L	R	0h	Rx FIFO 1 Message Lost This bit is a copy of interrupt flag MCAN_IR[7] RF1L. When the MCAN_IR[7] RF1L flag is reset, this bit is also reset. 1'b0 = No Rx FIFO 1 message lost 1'b1 = Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Note: OverWriting the oldest message when the MCAN_RXF1C[31] F1OM = 1'b1 will not set this flag.
24	F1F	R	0h	Rx FIFO 1 Full
23:22	NU53	R	0h	Reserved
21:16	F1PI	R	0h	Rx FIFO 1 Put Index
15:14	NU52	R	0h	Reserved
13:8	F1GI	R	0h	Rx FIFO 1 Get Index
7	NU51	R	0h	Reserved

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Table 5-99. CFG_RXF1S Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	F1FL	R	0h	Rx FIFO 1 Fill Level

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5.1.2.46 CFG_RXF1A Register

5.1.2.46.1 CFG_RXF1A Register (Offset = 2B8h) [reset = 0h]

Rx FIFO 1 Acknowledge register. FIFO 1 acknowledge last index of read buffers, updates get index and fill level.

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Table 5-100. Instance Table

Instance Name	Physical Address
MCAN0	5260 82B8h
MCAN1	5261 82B8h
MCAN2	5262 82B8h
MCAN3	5263 82B8h
MCAN4	5264 82B8h
MCAN5	5265 82B8h
MCAN6	5266 82B8h
MCAN7	5267 82B8h

Figure 5-46. CFG_RXF1A Name Register

31	30	29	28	27	26	25	24
NU55							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU55							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU55							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU55		F1AI					
R		R/W					
0h		0h					

Table 5-101. CFG_RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	NU55	R	0h	Reserved
5:0	F1AI	R/W	0h	Rx FIFO 1 Acknowledge Index After the Host CPU has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to the MCAN_RXF1A[5-0] F1AI field. This will set the Rx FIFO 1 Get Index MCAN_RXF1S[13-8] F1GI field to the MCAN_RXF1A[5-0] F1AI field + 1 and update the FIFO 1 Fill Level MCAN_RXF1S[6-0] F1FL field.

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5.1.2.47 CFG_RXESC Register

5.1.2.47.1 CFG_RXESC Register (Offset = 2BCh) [reset = 0h]

Rx Buffer/FIFO Element Size Configuration register. Configure data field size for storage of accepted frames.

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Table 5-102. Instance Table

Instance Name	Physical Address
MCAN0	5260 82BCh
MCAN1	5261 82BCh
MCAN2	5262 82BCh
MCAN3	5263 82BCh
MCAN4	5264 82BCh
MCAN5	5265 82BCh
MCAN6	5266 82BCh
MCAN7	5267 82BCh

Figure 5-47. CFG_RXESC Name Register

31	30	29	28	27	26	25	24
NU58							
R							
0h							
23	22	21	20	19	18	17	16
NU58							
R							
0h							
15	14	13	12	11	10	9	8
NU58					RBDS		
R					R/W		
0h					0h		
7	6	5	4	3	2	1	0
NU57	F1DS			NU56	F0DS		
R	R/W			R	R/W		
0h	0h			0h	0h		

Table 5-103. CFG_RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	NU58	R	0h	Reserved
10:8	RBDS	R/W	0h	Rx Buffer data Field Size 3'b000 = 8 byte data field 3'b001 = 12 byte data field 3'b010 = 16 byte data field 3'b011 = 20 byte data field 3'b100 = 24 byte data field 3'b101 = 32 byte data field 3'b110 = 48 byte data field 3'b111 = 64 byte data field
7	NU57	R	0h	Reserved

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Table 5-103. CFG_RXESC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	F1DS	R/W	0h	Rx FIFO 1 Data Field Size 3'b000 = 8 byte data field 3'b001 = 12 byte data field 3'b010 = 16 byte data field 3'b011 = 20 byte data field 3'b100 = 24 byte data field 3'b101 = 32 byte data field 3'b110 = 48 byte data field 3'b111 = 64 byte data field
3	NU56	R	0h	Reserved
2:0	F0DS	R/W	0h	Rx FIFO 0 Data Field Size 3'b000 = 8 byte data field 3'b001 = 12 byte data field 3'b010 = 16 byte data field 3'b011 = 20 byte data field 3'b100 = 24 byte data field 3'b101 = 32 byte data field 3'b110 = 48 byte data field 3'b111 = 64 byte data field Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by the MCAN_RXESC register are stored to the Rx Buffer respectively Rx FIFO element. The rest of the frame's data field is ignored.

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5.1.2.48 CFG_TXBC Register

5.1.2.48.1 CFG_TXBC Register (Offset = 2C0h) [reset = 0h]

Tx Buffer Configuration register. Configure Tx FIFO/Queue mode, Tx FIFO/Queue size, number of dedicated Tx buffers, Tx buffer start address.

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Table 5-104. Instance Table

Instance Name	Physical Address
MCAN0	5260 82C0h
MCAN1	5261 82C0h
MCAN2	5262 82C0h
MCAN3	5263 82C0h
MCAN4	5264 82C0h
MCAN5	5265 82C0h
MCAN6	5266 82C0h
MCAN7	5267 82C0h

Figure 5-48. CFG_TXBC Name Register

31	30	29	28	27	26	25	24
NU61	TFQM	TFQS					
R	R	R					
0h	0h	0h					
23	22	21	20	19	18	17	16
NU60		NDTB					
R		R					
0h		0h					
15	14	13	12	11	10	9	8
TBSA							
R							
0h							
7	6	5	4	3	2	1	0
TBSA						NU59	
R						R	
0h						0h	

Table 5-105. CFG_TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU61	R	0h	Reserved
30	TFQM	R	0h	Tx FIFO/Queue Mode 1'b0 = Tx FIFO operation 1'b1 = Tx Queue operation
29:24	TFQS	R	0h	Transmit FIFO/Queue Size 6'h00 = No Tx FIFO/Queue 6'b01-6'h20 (1-32) = Number of Tx Buffers used for Tx FIFO/Queue > 6'h20 (32) = Values greater than 32 are interpreted as 32
23:22	NU60	R	0h	Reserved
21:16	NDTB	R	0h	Number of Dedicated Transmit Buffers 6'h00 = No Dedicated Tx Buffers 6'h01-6'h20 (1-32) = Number of Dedicated Tx Buffers > 6'h20 (32) = Values greater than 32 are interpreted as 32

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Table 5-105. CFG_TXBC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:2	TBSA	R	0h	Tx Buffers Start Address Start address of Tx Buffers section in Message RAM (32-bit word address, see Message RAM Configuration). Note: Be aware that the sum of the MCAN_TXBC[29-24] TFQS and MCAN_TXBC[21-16] NDTB fields may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.
1:0	NU59	R	0h	Reserved

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5.1.2.49 CFG_TXFQS Register

5.1.2.49.1 CFG_TXFQS Register (Offset = 2C4h) [reset = 0h]

Tx FIFO/Queue Status register. Tx FIFO/Queue full indication and put index, Tx FIFO get index and fill level. The Tx FIFO/Queue status is related to the pending Tx requests listed in the MCAN_TXBRP register. Therefore the effect of Add/Cancellation requests may be delayed due to a running Tx scan (the MCAN_TXBRP register not yet updated).

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Table 5-106. Instance Table

Instance Name	Physical Address
MCAN0	5260 82C4h
MCAN1	5261 82C4h
MCAN2	5262 82C4h
MCAN3	5263 82C4h
MCAN4	5264 82C4h
MCAN5	5265 82C4h
MCAN6	5266 82C4h
MCAN7	5267 82C4h

Figure 5-49. CFG_TXFQS Name Register

31	30	29	28	27	26	25	24
NU64							
R							
0h							
23	22	21	20	19	18	17	16
NU64		TFQF	TFQPI				
R		R	R				
0h		0h	0h				
15	14	13	12	11	10	9	8
NU63			TFGI				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
NU62		TFFL					
R		R					
0h		0h					

Table 5-107. CFG_TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	NU64	R	0h	Reserved
21	TFQF	R	0h	Tx FIFO/Queue Full
20:16	TFQPI	R	0h	Tx FIFO/Queue Put Index
15:13	NU63	R	0h	Reserved
12:8	TFGI	R	0h	Tx Queue Get Index
7:6	NU62	R	0h	Reserved

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Table 5-107. CFG_TXFQS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	TFFL	R	0h	Tx FIFO Free Level. Number of consecutive free Tx FIFO elements starting from the MCAN_TXFQS[12-8] TFGI field, range 0 to 32. Read as zero when Tx Queue operation is configured (MCAN_TXBC[30] TFQM = 1'b1). Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers.

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5.1.2.50 CFG_TXESC Register

5.1.2.50.1 CFG_TXESC Register (Offset = 2C8h) [reset = 0h]

Tx Buffer Element Size Configuration register. ConfigurationConfigure data field size for frame transmission. Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes > 8 bytes are intended for CAN FD operation only.

Return to Summary Table

Table 5-108. Instance Table

Instance Name	Physical Address
MCAN0	5260 82C8h
MCAN1	5261 82C8h
MCAN2	5262 82C8h
MCAN3	5263 82C8h
MCAN4	5264 82C8h
MCAN5	5265 82C8h
MCAN6	5266 82C8h
MCAN7	5267 82C8h

Figure 5-50. CFG_TXESC Name Register

31	30	29	28	27	26	25	24
NU65							
R							
0h							
23	22	21	20	19	18	17	16
NU65							
R							
0h							
15	14	13	12	11	10	9	8
NU65							
R							
0h							
7	6	5	4	3	2	1	0
NU65					TBDS		
R					R/W		
0h					0h		

Table 5-109. CFG_TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	NU65	R	0h	Reserved
2:0	TBDS	R/W	0h	Tx Buffer Data Field Size 3'b000 = 8 byte data field 3'b001 = 12 byte data field 3'b010 = 16 byte data field 3'b011 = 20 byte data field 3'b100 = 24 byte data field 3'b101 = 32 byte data field 3'b110 = 48 byte data field 3'b111 = 64 byte data field Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size MCAN_TXESC[2-0] TBDS, the bytes not defined by the Tx Buffer are transmitted as CCh (padding bytes).

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5.1.2.51 CFG_TXBRP Register

5.1.2.51.1 CFG_TXBRP Register (Offset = 2CCh) [reset = 0h]

Tx Buffer Request Pending register. PendingTx buffers with pending transmission request. Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via the MCAN_TXBAR register. The bits are reset after a requested transmission has completed or has been cancelled via the MCAN_TXBCR register. The MCAN_TXBRP bits are set only for those Tx Buffers configured via the MCAN_TXBC register. After a MCAN_TXBRP bit has been set, a Tx scan (see Tx Handling) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID).

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Table 5-110. Instance Table

Instance Name	Physical Address
MCAN0	5260 82CCh
MCAN1	5261 82CCh
MCAN2	5262 82CCh
MCAN3	5263 82CCh
MCAN4	5264 82CCh
MCAN5	5265 82CCh
MCAN6	5266 82CCh
MCAN7	5267 82CCh

Figure 5-51. CFG_TXBRP Name Register

31	30	29	28	27	26	25	24
TRP							
R							
0h							
23	22	21	20	19	18	17	16
TRP							
R							
0h							
15	14	13	12	11	10	9	8
TRP							
R							
0h							
7	6	5	4	3	2	1	0
TRP							
R							
0h							

Table 5-111. CFG_TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRP	R	0h	Transmission Request Pending

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5.1.2.52 CFG_TXBAR Register

5.1.2.52.1 CFG_TXBAR Register (Offset = 2D0h) [reset = 0h]

Tx Buffer Add Request register. Add transmission requests. Each Tx Buffer has its own Add Request bit. Writing 1h will set the corresponding Add Request bit; writing a 0h has no impact. This enables the Host CPU to set transmission requests for multiple Tx Buffers with one write to the MCAN_TXBAR register. The MCAN_TXBAR bits are set only for those Tx Buffers configured via the MCAN_TXBC register. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. Note: If an add request is applied for a Tx Buffer with pending transmission request (corresponding MCAN_TXBRP bit already set), this add request is ignored.

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Table 5-112. Instance Table

Instance Name	Physical Address
MCAN0	5260 82D0h
MCAN1	5261 82D0h
MCAN2	5262 82D0h
MCAN3	5263 82D0h
MCAN4	5264 82D0h
MCAN5	5265 82D0h
MCAN6	5266 82D0h
MCAN7	5267 82D0h

Figure 5-52. CFG_TXBAR Name Register

31	30	29	28	27	26	25	24
AR							
R/W0TC							
0h							
23	22	21	20	19	18	17	16
AR							
R/W0TC							
0h							
15	14	13	12	11	10	9	8
AR							
R/W0TC							
0h							
7	6	5	4	3	2	1	0
AR							
R/W0TC							
0h							

Table 5-113. CFG_TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	AR	R/W0TC	0h	Add request

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5.1.2.53 CFG_TXBCR Register

5.1.2.53.1 CFG_TXBCR Register (Offset = 2D4h) [reset = 0h]

Tx Buffer Cancellation Request register. Request cancellation of pending transmissions. Each Tx Buffer has its own Cancellation Request bit. Writing a 1h will set the corresponding Cancellation Request bit; writing a 0h has no impact. This enables the Host CPU to set cancellation requests for multiple Tx Buffers with one write to the MCAN_TXBCR register. The MCAN_TXBCR bits are set only for those Tx Buffers configured via the MCAN_TXBC register. The bits remain set until the corresponding bit of the MCAN_TXBRP register is reset.

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Table 5-114. Instance Table

Instance Name	Physical Address
MCAN0	5260 82D4h
MCAN1	5261 82D4h
MCAN2	5262 82D4h
MCAN3	5263 82D4h
MCAN4	5264 82D4h
MCAN5	5265 82D4h
MCAN6	5266 82D4h
MCAN7	5267 82D4h

Figure 5-53. CFG_TXBCR Name Register

31	30	29	28	27	26	25	24
CR							
R/W0TC							
0h							
23	22	21	20	19	18	17	16
CR							
R/W0TC							
0h							
15	14	13	12	11	10	9	8
CR							
R/W0TC							
0h							
7	6	5	4	3	2	1	0
CR							
R/W0TC							
0h							

Table 5-115. CFG_TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CR	R/W0TC	0h	Cancellation Request

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5.1.2.54 CFG_TXBTO Register

5.1.2.54.1 CFG_TXBTO Register (Offset = 2D8h) [reset = 0h]

Tx Buffer Transmission Occurred register. Signals successful transmissions, set when corresponding MCAN_TXBRP flag is cleared. Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding MCAN_TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a 1h to the corresponding bit of register the MCAN_TXBAR register.

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Table 5-116. Instance Table

Instance Name	Physical Address
MCAN0	5260 82D8h
MCAN1	5261 82D8h
MCAN2	5262 82D8h
MCAN3	5263 82D8h
MCAN4	5264 82D8h
MCAN5	5265 82D8h
MCAN6	5266 82D8h
MCAN7	5267 82D8h

Figure 5-54. CFG_TXBTO Name Register

31	30	29	28	27	26	25	24
TO							
R							
0h							
23	22	21	20	19	18	17	16
TO							
R							
0h							
15	14	13	12	11	10	9	8
TO							
R							
0h							
7	6	5	4	3	2	1	0
TO							
R							
0h							

Table 5-117. CFG_TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TO	R	0h	Transmission Occurred

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5.1.2.55 CFG_TXBCF Register

5.1.2.55.1 CFG_TXBCF Register (Offset = 2DCh) [reset = 0h]

Tx Buffer Cancellation Finished register. Signals successful transmit cancellation, set when corresponding MCAN_TXBRP flag is cleared after cancellation request. Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding MCAN_TXBRP bit is cleared after a cancellation was requested via the MCAN_TXBCR register. In case the corresponding MCAN_TXBRP bit was not set at the point of cancellation, MCAN_TXBCF[n] CF bit is set immediately. The bits are reset when a new transmission is requested by writing a 1h to the corresponding bit of the MCAN_TXBAR register.

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Table 5-118. Instance Table

Instance Name	Physical Address
MCAN0	5260 82DCh
MCAN1	5261 82DCh
MCAN2	5262 82DCh
MCAN3	5263 82DCh
MCAN4	5264 82DCh
MCAN5	5265 82DCh
MCAN6	5266 82DCh
MCAN7	5267 82DCh

Figure 5-55. CFG_TXBCF Name Register

31	30	29	28	27	26	25	24
CF							
R							
0h							
23	22	21	20	19	18	17	16
CF							
R							
0h							
15	14	13	12	11	10	9	8
CF							
R							
0h							
7	6	5	4	3	2	1	0
CF							
R							
0h							

Table 5-119. CFG_TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CF	R	0h	Cancellation Finished

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5.1.2.56 CFG_TXBTIE Register

5.1.2.56.1 CFG_TXBTIE Register (Offset = 2E0h) [reset = 0h]

Tx Buffer Transmission Interrupt Enable register. Enable transmit interrupts for selected Tx buffers.

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Table 5-120. Instance Table

Instance Name	Physical Address
MCAN0	5260 82E0h
MCAN1	5261 82E0h
MCAN2	5262 82E0h
MCAN3	5263 82E0h
MCAN4	5264 82E0h
MCAN5	5265 82E0h
MCAN6	5266 82E0h
MCAN7	5267 82E0h

Figure 5-56. CFG_TXBTIE Name Register

31	30	29	28	27	26	25	24
TIE							
R/W							
0h							
23	22	21	20	19	18	17	16
TIE							
R/W							
0h							
15	14	13	12	11	10	9	8
TIE							
R/W							
0h							
7	6	5	4	3	2	1	0
TIE							
R/W							
0h							

Table 5-121. CFG_TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIE	R/W	0h	Transmission Interrupt Enable

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5.1.2.57 CFG_TXBCIE Register

5.1.2.57.1 CFG_TXBCIE Register (Offset = 2E4h) [reset = 0h]

Tx Buffer Cancellation Finished Interrupt Enable register. Enable cancellation finished interrupts for selected Tx buffers.

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Table 5-122. Instance Table

Instance Name	Physical Address
MCAN0	5260 82E4h
MCAN1	5261 82E4h
MCAN2	5262 82E4h
MCAN3	5263 82E4h
MCAN4	5264 82E4h
MCAN5	5265 82E4h
MCAN6	5266 82E4h
MCAN7	5267 82E4h

Figure 5-57. CFG_TXBCIE Name Register

31	30	29	28	27	26	25	24
CFIE							
R/W							
0h							
23	22	21	20	19	18	17	16
CFIE							
R/W							
0h							
15	14	13	12	11	10	9	8
CFIE							
R/W							
0h							
7	6	5	4	3	2	1	0
CFIE							
R/W							
0h							

Table 5-123. CFG_TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CFIE	R/W	0h	Cancellation Finished Interrupt Enable

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5.1.2.58 CFG_TXEFC Register

5.1.2.58.1 CFG_TXEFC Register (Offset = 2F0h) [reset = 0h]

Tx Event FIFO Configuration register. Tx event FIFO watermark, size and start address.

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Table 5-124. Instance Table

Instance Name	Physical Address
MCAN0	5260 82F0h
MCAN1	5261 82F0h
MCAN2	5262 82F0h
MCAN3	5263 82F0h
MCAN4	5264 82F0h
MCAN5	5265 82F0h
MCAN6	5266 82F0h
MCAN7	5267 82F0h

Figure 5-58. CFG_TXEFC Name Register

31	30	29	28	27	26	25	24
NU68		EFWM					
R/W		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU67		EFS					
R/W		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EFSA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EFSA						NU66	
R/W						R/W	
0h						0h	

Table 5-125. CFG_TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	NU68	R/W	0h	Reserved
29:24	EFWM	R/W	0h	Event FIFO Watermark 6'h00 = Watermark interrupt disabled 6'h01-6'h20 (1-32) = Level for Tx Event FIFO watermark interrupt (MCAN_IR[13] TEFW) > 6'h20 (32) = Watermark interrupt disabled
23:22	NU67	R/W	0h	Reserved
21:16	EFS	R/W	0h	Event FIFO Size 6'h00 = Tx Event FIFO disabled 6'h01-6'h20 (1-32) = Number of Tx Event FIFO elements > 6'h20 (32) = Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to MCAN_TXEFC[21-16] EFS field - 1.
15:2	EFSA	R/W	0h	Event FIFO Start Address Start address of Tx Event FIFO in Message RAM (32-bit word address, see Message RAM Configuration).

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Table 5-125. CFG_TXEFC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	NU66	R/W	0h	Reserved

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5.1.2.59 CFG_TXEFS Register

5.1.2.59.1 CFG_TXEFS Register (Offset = 2F4h) [reset = 0h]

Tx Event FIFO Status register. Tx event FIFO element lost/full indication, put index, get index, and fill level.

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Table 5-126. Instance Table

Instance Name	Physical Address
MCAN0	5260 82F4h
MCAN1	5261 82F4h
MCAN2	5262 82F4h
MCAN3	5263 82F4h
MCAN4	5264 82F4h
MCAN5	5265 82F4h
MCAN6	5266 82F4h
MCAN7	5267 82F4h

Figure 5-59. CFG_TXEFS Name Register

31	30	29	28	27	26	25	24
NU72						TEFL	EFF
R						R	R
0h						0h	0h
23	22	21	20	19	18	17	16
NU71			EFPI				
R			R				
0h			0h				
15	14	13	12	11	10	9	8
NU70			EFGI				
R			R				
0h			0h				
7	6	5	4	3	2	1	0
NU69		EFFL					
R		R					
0h		0h					

Table 5-127. CFG_TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	NU72	R	0h	Reserved
25	TEFL	R	0h	Tx Event FIFO Element Lost This bit is a copy of interrupt flag MCAN_IR[15] TEFL. When the MCAN_IR[15] TEFL flag is reset, this bit is also reset. 1'b0 = No Tx Event FIFO element lost 1'b1 = Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.
24	EFF	R	0h	Event FIFO Full
23:21	NU71	R	0h	Reserved
20:16	EFPI	R	0h	Event FIFO Put Index
15:13	NU70	R	0h	Reserved
12:8	EFGI	R	0h	Event FIFO Get Index
7:6	NU69	R	0h	Reserved
5:0	EFFL	R	0h	Event FIFO FIll Level

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5.1.2.60 CFG_TXEFA Register

5.1.2.60.1 CFG_TXEFA Register (Offset = 2F8h) [reset = 0h]

Tx Event FIFO Acknowledge register. Tx event FIFO acknowledge last index of read elements, updates get index and fill level.

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Table 5-128. Instance Table

Instance Name	Physical Address
MCAN0	5260 82F8h
MCAN1	5261 82F8h
MCAN2	5262 82F8h
MCAN3	5263 82F8h
MCAN4	5264 82F8h
MCAN5	5265 82F8h
MCAN6	5266 82F8h
MCAN7	5267 82F8h

Figure 5-60. CFG_TXEFA Name Register

31	30	29	28	27	26	25	24
NU73							
R							
0h							
23	22	21	20	19	18	17	16
NU73							
R							
0h							
15	14	13	12	11	10	9	8
NU73							
R							
0h							
7	6	5	4	3	2	1	0
NU73			EFAI				
R			R				
0h			0h				

Table 5-129. CFG_TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	NU73	R	0h	Reserved
4:0	EFAI	R	0h	Event FIFO Acknowledge Index After the Host CPU has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to the MCAN_TXEFA[4-0] EFAI field. This will set the Tx Event FIFO Get Index MCAN_TXEFS[12-8] EFGI field to the MCAN_TXEFA[4-0] EFAI field + 1 and update the Event FIFO Fill Level MCAN_TXEFS[5-0] EFFL field.

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5.1.2.61 ECC_REV Register

5.1.2.61.1 ECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

Aggregator Revision Register. The Aggregator Revision Register contains the revision parameters for the ECC Aggregator.

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Table 5-130. Instance Table

Instance Name	Physical Address
MCAN0	5270 0000h
MCAN1	5270 1000h
MCAN2	5270 2000h
MCAN3	5270 3000h
MCAN4	5270 4000h
MCAN5	5270 5000h
MCAN6	5270 6000h
MCAN7	5270 7000h

Figure 5-61. ECC_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
1Dh					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 5-131. ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business Unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	1Dh	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

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5.1.2.62 ECC_VECTOR Register

5.1.2.62.1 ECC_VECTOR Register (Offset = 8h) [reset = 0h]

ECC RAM ID to select which ECC RAM to control or read status from.

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Table 5-132. Instance Table

Instance Name	Physical Address
MCAN0	5270 0008h
MCAN1	5270 1008h
MCAN2	5270 2008h
MCAN3	5270 3008h
MCAN4	5270 4008h
MCAN5	5270 5008h
MCAN6	5270 6008h
MCAN7	5270 7008h

Figure 5-62. ECC_VECTOR Name Register

31	30	29	28	27	26	25	24
NU1							RD_SVBUS_DONE
NU1							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	NU0				ECC_VEC		
R/W	R				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VEC							
R/W							
0h							

Table 5-133. ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	NU1	NU1	0h	Reserved
24	RD_SVBUS_DONE	R/W	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field.
23:16	RD_SVBUS_ADDR	R/W	0h	Read address
15	RD_SVBUS	R/W	0h	Write 1 to trigger a read on the serial VBUS. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
14:11	NU0	R	0h	Reserved
10:0	ECC_VEC	R/W	0h	Value written to select the corresponding ECC RAM for control or status

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5.1.2.63 ECC_STAT Register

5.1.2.63.1 ECC_STAT Register (Offset = Ch) [reset = 2h]

Contains misc status such as number of ECC RAMs serviced by the ECC aggregator.

Return to Summary Table

Table 5-134. Instance Table

Instance Name	Physical Address
MCAN0	5270 000Ch
MCAN1	5270 100Ch
MCAN2	5270 200Ch
MCAN3	5270 300Ch
MCAN4	5270 400Ch
MCAN5	5270 500Ch
MCAN6	5270 600Ch
MCAN7	5270 700Ch

Figure 5-63. ECC_STAT Name Register

31	30	29	28	27	26	25	24
NU2							
NU2							
0h							
23	22	21	20	19	18	17	16
NU2							
NU2							
0h							
15	14	13	12	11	10	9	8
NU2					NUM_RAMS		
NU2					R		
0h					2h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
2h							

Table 5-135. ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	NU2	NU2	0h	Reserved
10:0	NUM_RAMS	R	2h	Indicates the number of RAMS serviced by the ECC aggregator

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5.1.2.64 ECC_CTRL Register

5.1.2.64.1 ECC_CTRL Register (Offset = 14h) [reset = 107h]

ECC Control Register.

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Table 5-136. Instance Table

Instance Name	Physical Address
MCAN0	5270 0014h
MCAN1	5270 1014h
MCAN2	5270 2014h
MCAN3	5270 3014h
MCAN4	5270 4014h
MCAN5	5270 5014h
MCAN6	5270 6014h
MCAN7	5270 7014h

Figure 5-64. ECC_CTRL Name Register

31	30	29	28	27	26	25	24
NU3							
R							
0h							
23	22	21	20	19	18	17	16
NU3							
R							
0h							
15	14	13	12	11	10	9	8
NU3							CHECK
R							R/W
0h							1h
7	6	5	4	3	2	1	0
RESERVED	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	EN_RMW	ECC_CHK	ECC_EN
NONE	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	1h	1h	1h

Table 5-137. ECC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	NU3	R	0h	TI Internal : Reserved
8	CHECK	R/W	1h	TI Internal : Check Parity TI Internal : Check timeout
7	RESERVED	NONE	0h	Reserved
6	ERROR_ONCE	W	0h	TI Internal : Force Error only once
5	FORCE_N_ROW	W	0h	TI Internal : Force Error on any RAM read
4	FORCE_DED	W	0h	TI Internal : Force Double Bit Error
3	FORCE_SEC	W	0h	TI Internal : Force Single Bit Error
2	EN_RMW	W	1h	TI Internal : Enable rmw
1	ECC_CHK	W	1h	TI Internal : Enable ECC check
0	ECC_EN	W	1h	TI Internal : Enable ECC

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5.1.2.65 ECC_ERR_CTRL1 Register

5.1.2.65.1 ECC_ERR_CTRL1 Register (Offset = 18h) [reset = 0h]

ECC Error Control1 Register.

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Table 5-138. Instance Table

Instance Name	Physical Address
MCAN0	5270 0018h
MCAN1	5270 1018h
MCAN2	5270 2018h
MCAN3	5270 3018h
MCAN4	5270 4018h
MCAN5	5270 5018h
MCAN6	5270 6018h
MCAN7	5270 7018h

Figure 5-65. ECC_ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24
ECC_ROW							
R/W							
0h							
23	22	21	20	19	18	17	16
ECC_ROW							
R/W							
0h							
15	14	13	12	11	10	9	8
ECC_ROW							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_ROW							
R/W							
0h							

Table 5-139. ECC_ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R/W	0h	TI Internal : Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

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5.1.2.66 ECC_ERR_CTRL2 Register

5.1.2.66.1 ECC_ERR_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ECC Error Control2 Register.

Return to Summary Table

Table 5-140. Instance Table

Instance Name	Physical Address
MCAN0	5270 001Ch
MCAN1	5270 101Ch
MCAN2	5270 201Ch
MCAN3	5270 301Ch
MCAN4	5270 401Ch
MCAN5	5270 501Ch
MCAN6	5270 601Ch
MCAN7	5270 701Ch

Figure 5-66. ECC_ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24
ECC_BIT2							
R/W							
0h							
23	22	21	20	19	18	17	16
ECC_BIT2							
R/W							
0h							
15	14	13	12	11	10	9	8
ECC_BIT1							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_BIT1							
R/W							
0h							

Table 5-141. ECC_ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT2	R/W	0h	TI Internal : Data bit that needs to be flipped if double bit error needs to be forced
15:0	ECC_BIT1	R/W	0h	TI Internal : Data bit that needs to be flipped when force_sec is set

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5.1.2.67 ECC_ERR_STAT1 Register

5.1.2.67.1 ECC_ERR_STAT1 Register (Offset = 20h) [reset = 0h]

ECC Error Status1 Register.

Return to Summary Table

Table 5-142. Instance Table

Instance Name	Physical Address
MCAN0	5270 0020h
MCAN1	5270 1020h
MCAN2	5270 2020h
MCAN3	5270 3020h
MCAN4	5270 4020h
MCAN5	5270 5020h
MCAN6	5270 6020h
MCAN7	5270 7020h

Figure 5-67. ECC_ERR_STAT1 Name Register

31	30	29	28	27	26	25	24
ECC_BIT1_STS							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ECC_BIT1_STS							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLR_ECC_CTRL_REG	CLR_ECC_PAR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC	
W	W		W	W		W	
0h	0h		0h	0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_CTRL_REG	ECC_PAR		ECC_OTHER	ECC_DED		ECC_SEC	
W	W		W	W		W	
0h	0h		0h	0h		0h	

Table 5-143. ECC_ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT1_STS	R	0h	TI Internal : Data bit that corresponds to the single-bit error
15	CLR_ECC_CTRL_REG	W	0h	TI Internal : Clear Ctrl Reg Error Status. Write 1 to clear. This bit is self clearing.
14:13	CLR_ECC_PAR	W	0h	TI Internal : Clear Parity Error Status. Write 1 to clear. This bit is self clearing.
12	CLR_ECC_OTHER	W	0h	TI Internal : Clear Other Error Status. Write 1 to clear. This bit is self clearing.
11:10	CLR_ECC_DED	W	0h	TI Internal : Clear Double Bit Error Status. Write 1 to clear. This bit is self clearing.
9:8	CLR_ECC_SEC	W	0h	TI Internal : Clear Single Bit Error Status. Write 1 to clear. This bit is self clearing.
7	ECC_CTRL_REG	W	0h	TI Internal : Force ctrl reg pending interrupt. Write 1 to set. This bit is self clearing.

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Table 5-143. ECC_ERR_STAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	ECC_PAR	W	0h	TI Internal : Force ECC parity pending interrupt. Write 1 to set. This bit is self clearing.
4	ECC_OTHER	W	0h	TI Internal : Force ECC other pending interrupt. Write 1 to set. This bit is self clearing.
3:2	ECC_DED	W	0h	TI Internal : Force ECC DED pending interrupt. Write 1 to set. This bit is self clearing.
1:0	ECC_SEC	W	0h	TI Internal : Force ECC SEC pending interrupt. Write 1 to set. This bit is self clearing.

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5.1.2.68 ECC_ERR_STAT2 Register

5.1.2.68.1 ECC_ERR_STAT2 Register (Offset = 24h) [reset = 0h]

ECC Error Status2 Register.

Return to Summary Table

Table 5-144. Instance Table

Instance Name	Physical Address
MCAN0	5270 0024h
MCAN1	5270 1024h
MCAN2	5270 2024h
MCAN3	5270 3024h
MCAN4	5270 4024h
MCAN5	5270 5024h
MCAN6	5270 6024h
MCAN7	5270 7024h

Figure 5-68. ECC_ERR_STAT2 Name Register

31	30	29	28	27	26	25	24
ECC_ROW							
R							
0h							
23	22	21	20	19	18	17	16
ECC_ROW							
R							
0h							
15	14	13	12	11	10	9	8
ECC_ROW							
R							
0h							
7	6	5	4	3	2	1	0
ECC_ROW							
R							
0h							

Table 5-145. ECC_ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R	0h	TI Internal : Row address where the single or double-bit error has occurred

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5.1.2.69 ECC_ERR_STAT3 Register

5.1.2.69.1 ECC_ERR_STAT3 Register (Offset = 28h) [reset = 0h]

ECC Error Status3 Register.

Return to Summary Table

Table 5-146. Instance Table

Instance Name	Physical Address
MCAN0	5270 0028h
MCAN1	5270 1028h
MCAN2	5270 2028h
MCAN3	5270 3028h
MCAN4	5270 4028h
MCAN5	5270 5028h
MCAN6	5270 6028h
MCAN7	5270 7028h

Figure 5-69. ECC_ERR_STAT3 Name Register

31	30	29	28	27	26	25	24
NU6							
R							
0h							
23	22	21	20	19	18	17	16
NU6							
R							
0h							
15	14	13	12	11	10	9	8
NU6						CLR_TIMEOUT_PEND	NU5
R						W	R
0h						0h	0h
7	6	5	4	3	2	1	0
NU5						TIMEOUT_PEND	NU4
R						W	R
0h						0h	0h

Table 5-147. ECC_ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	NU6	R	0h	TI Internal : Reserved
9	CLR_TIMEOUT_PEND	W	0h	TI Internal : Clear timeout pending
8:2	NU5	R	0h	TI Internal : Reserved
1	TIMEOUT_PEND	W	0h	TI Internal : Timeout pending
0	NU4	R	0h	TI Internal : Reserved

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5.1.2.70 ECC_SEC_EOI_REG Register

5.1.2.70.1 ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

Return to Summary Table

Table 5-148. Instance Table

Instance Name	Physical Address
MCAN0	5270 003Ch
MCAN1	5270 103Ch
MCAN2	5270 203Ch
MCAN3	5270 303Ch
MCAN4	5270 403Ch
MCAN5	5270 503Ch
MCAN6	5270 603Ch
MCAN7	5270 703Ch

Figure 5-70. ECC_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
NU7							
R							
0h							
23	22	21	20	19	18	17	16
NU7							
R							
0h							
15	14	13	12	11	10	9	8
NU7							
R							
0h							
7	6	5	4	3	2	1	0
NU7							SEC_EOI_WR
R							R/W
0h							0h

Table 5-149. ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU7	R	0h	Reserved
0	SEC_EOI_WR	R/W	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, Reading this bit will return 0.

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5.1.2.71 ECC_SEC_STATUS_REG0 Register

5.1.2.71.1 ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 5-150. Instance Table

Instance Name	Physical Address
MCAN0	5270 0040h
MCAN1	5270 1040h
MCAN2	5270 2040h
MCAN3	5270 3040h
MCAN4	5270 4040h
MCAN5	5270 5040h
MCAN6	5270 6040h
MCAN7	5270 7040h

Figure 5-71. ECC_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
NU8							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU8							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU8							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU8						CTRL_EDC_VBUSS_PEND	SEC_PEND
R						R	R
0h						0h	0h

Table 5-151. ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU8	R	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	R	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	SEC_PEND	R	0h	Interrupt Pending Status for msgmem_pend.

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5.1.2.72 ECC_SEC_ENABLE_SET_REG0 Register

5.1.2.72.1 ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 5-152. Instance Table

Instance Name	Physical Address
MCAN0	5270 0080h
MCAN1	5270 1080h
MCAN2	5270 2080h
MCAN3	5270 3080h
MCAN4	5270 4080h
MCAN5	5270 5080h
MCAN6	5270 6080h
MCAN7	5270 7080h

Figure 5-72. ECC_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
NU9							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU9							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU9							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU9						CTRL_EDC_VBUSS_ENABLE_SET	SEC_EN_SET
R						R/W	R/W
0h						0h	0h

Table 5-153. ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU9	R	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	R/W	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	SEC_EN_SET	R/W	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

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5.1.2.73 ECC_SEC_ENABLE_CLR_REG0 Register

5.1.2.73.1 ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 5-154. Instance Table

Instance Name	Physical Address
MCAN0	5270 00C0h
MCAN1	5270 10C0h
MCAN2	5270 20C0h
MCAN3	5270 30C0h
MCAN4	5270 40C0h
MCAN5	5270 50C0h
MCAN6	5270 60C0h
MCAN7	5270 70C0h

Figure 5-73. ECC_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
NU10							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU10							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU10							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU10						CTRL_EDC_VBUSS_ENABLE_CLR	SEC_EN_CLR
R						R/W	R/W
0h						0h	0h

Table 5-155. ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU10	R	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	R/W	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	SEC_EN_CLR	R/W	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

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5.1.2.74 ECC_DED_EOI_REG Register

5.1.2.74.1 ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

Return to Summary Table

Table 5-156. Instance Table

Instance Name	Physical Address
MCAN0	5270 013Ch
MCAN1	5270 113Ch
MCAN2	5270 213Ch
MCAN3	5270 313Ch
MCAN4	5270 413Ch
MCAN5	5270 513Ch
MCAN6	5270 613Ch
MCAN7	5270 713Ch

Figure 5-74. ECC_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
NU11							
R							
0h							
23	22	21	20	19	18	17	16
NU11							
R							
0h							
15	14	13	12	11	10	9	8
NU11							
R							
0h							
7	6	5	4	3	2	1	0
NU11							DED_EOI_WR
R							R/W
0h							0h

Table 5-157. ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU11	R	0h	Reserved
0	DED_EOI_WR	R/W	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, Reading this bit will return 0.

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5.1.2.75 ECC_DED_STATUS_REG0 Register

5.1.2.75.1 ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 5-158. Instance Table

Instance Name	Physical Address
MCAN0	5270 0140h
MCAN1	5270 1140h
MCAN2	5270 2140h
MCAN3	5270 3140h
MCAN4	5270 4140h
MCAN5	5270 5140h
MCAN6	5270 6140h
MCAN7	5270 7140h

Figure 5-75. ECC_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
NU12							
R							
0h							
23	22	21	20	19	18	17	16
NU12							
R							
0h							
15	14	13	12	11	10	9	8
NU12							
R							
0h							
7	6	5	4	3	2	1	0
NU12						CTRL_EDC_VBUSS_PEND	DED_PEND
R						R	R
0h						0h	0h

Table 5-159. ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU12	R	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	R	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	DED_PEND	R	0h	Interrupt Pending Status for msgmem_pend.

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5.1.2.76 ECC_DED_ENABLE_SET_REG0 Register

5.1.2.76.1 ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 5-160. Instance Table

Instance Name	Physical Address
MCAN0	5270 0180h
MCAN1	5270 1180h
MCAN2	5270 2180h
MCAN3	5270 3180h
MCAN4	5270 4180h
MCAN5	5270 5180h
MCAN6	5270 6180h
MCAN7	5270 7180h

Figure 5-76. ECC_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
NU13							
R							
0h							
23	22	21	20	19	18	17	16
NU13							
R							
0h							
15	14	13	12	11	10	9	8
NU13							
R							
0h							
7	6	5	4	3	2	1	0
NU13						CTRL_EDC_VBUSS_ENABLE_SET	DED_EN_SET
R						R/W	R/W
0h						0h	0h

Table 5-161. ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU13	R	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	R/W	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	DED_EN_SET	R/W	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

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5.1.2.77 ECC_DED_ENABLE_CLR_REG0 Register

5.1.2.77.1 ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 5-162. Instance Table

Instance Name	Physical Address
MCAN0	5270 01C0h
MCAN1	5270 11C0h
MCAN2	5270 21C0h
MCAN3	5270 31C0h
MCAN4	5270 41C0h
MCAN5	5270 51C0h
MCAN6	5270 61C0h
MCAN7	5270 71C0h

Figure 5-77. ECC_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
NU14							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU14							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU14							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU14						CTRL_EDC_VBUSS_ENABLE_CLR	DED_EN_CLR
R						R/W	R/W
0h						0h	0h

Table 5-163. ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU14	R	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	R/W	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	DED_EN_CLR	R/W	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

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5.1.2.78 ECC_AGGR_ENABLE_SET Register

5.1.2.78.1 ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register.

Return to Summary Table

Table 5-164. Instance Table

Instance Name	Physical Address
MCAN0	5270 0200h
MCAN1	5270 1200h
MCAN2	5270 2200h
MCAN3	5270 3200h
MCAN4	5270 4200h
MCAN5	5270 5200h
MCAN6	5270 6200h
MCAN7	5270 7200h

Figure 5-78. ECC_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
NU15							
R							
0h							
23	22	21	20	19	18	17	16
NU15							
R							
0h							
15	14	13	12	11	10	9	8
NU15							
R							
0h							
7	6	5	4	3	2	1	0
NU15						TIMEOUT	PARITY
R						R/W	R/W
0h						0h	0h

Table 5-165. ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU15	R	0h	Reserved
1	TIMEOUT	R/W	0h	Interrupt Enable Set Register for svbus timeout errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	PARITY	R/W	0h	Interrupt Enable Set Register for parity errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

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5.1.2.79 ECC_AGGR_ENABLE_CLR Register

5.1.2.79.1 ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register.

Return to Summary Table

Table 5-166. Instance Table

Instance Name	Physical Address
MCAN0	5270 0204h
MCAN1	5270 1204h
MCAN2	5270 2204h
MCAN3	5270 3204h
MCAN4	5270 4204h
MCAN5	5270 5204h
MCAN6	5270 6204h
MCAN7	5270 7204h

Figure 5-79. ECC_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
NU16							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU16							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU16							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU16						TIMEOUT	PARITY
R						R/W	R/W
0h						0h	0h

Table 5-167. ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU16	R	0h	Reserved
1	TIMEOUT	R/W	0h	Interrupt Enable Clear for svbus timeout errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	PARITY	R/W	0h	Interrupt Enable Clear for parity errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

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5.1.2.80 ECC_AGGR_STATUS_SET Register

5.1.2.80.1 ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register.

Return to Summary Table

Table 5-168. Instance Table

Instance Name	Physical Address
MCAN0	5270 0208h
MCAN1	5270 1208h
MCAN2	5270 2208h
MCAN3	5270 3208h
MCAN4	5270 4208h
MCAN5	5270 5208h
MCAN6	5270 6208h
MCAN7	5270 7208h

Figure 5-80. ECC_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
NU17							
R							
0h							
23	22	21	20	19	18	17	16
NU17							
R							
0h							
15	14	13	12	11	10	9	8
NU17							
R							
0h							
7	6	5	4	3	2	1	0
NU17				TIMEOUT		PARITY	
R				R/W		R/W	
0h				0h		0h	

Table 5-169. ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU17	R	0h	Reserved
3:2	TIMEOUT	R/W	0h	2-bit saturating counter of the number of timeout errors that have occurred since last cleared. 2'b00 - No timeout errors have occurred 2'b01 - 1 timeout erro has occurred 2'b10 - 2 timeout error has occurred 2'b11 - 3 or more timeout errors have occurred A write of a non-zero value to this register increments that many from the timeout fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. . If this register goes from 0 ot non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.

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Table 5-169. ECC_AGGR_STATUS_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PARITY	R/W	0h	2-bit saturating counter of the number of parity errors that have occurred since last cleared. 2'b00 - No parity errors have occurred 2'b01 - 1 parity error has occurred 2'b10 - 2 parity error has occurred 2'b11 - 3 or more parity error have occurred A write of a non-zero value to this register incrments that many from the parity fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. If this register goes from 0 ot non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.

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5.1.2.81 ECC_AGGR_STATUS_CLR Register

5.1.2.81.1 ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register.

Return to Summary Table

Table 5-170. Instance Table

Instance Name	Physical Address
MCAN0	5270 020Ch
MCAN1	5270 120Ch
MCAN2	5270 220Ch
MCAN3	5270 320Ch
MCAN4	5270 420Ch
MCAN5	5270 520Ch
MCAN6	5270 620Ch
MCAN7	5270 720Ch

Figure 5-81. ECC_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
NU18							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU18							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU18							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NU18				TIMEOUT		PARITY	
R				R/W		R/W	
0h				0h		0h	

Table 5-171. ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	NU18	R	0h	Reserved
3:2	TIMEOUT	R/W	0h	2'b00 - No timeout errors have occurred 2'b01 - 1 timeout erro has occurred 2'b10 - 2 timeout error has occurred 2'b11 - 3 or more timeout errors have occurred A write of a non-zero value to this register decrements that many from the timeout fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will nto be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.

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Table 5-171. ECC_AGGR_STATUS_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PARITY	R/W	0h	2'b00 - No parity errors have occurred 2'b01 - 1 parity error has occurred 2'b10 - 2 parity error has occurred 2'b11 - 3 or more parity error have occurred A write of a non-zero value to this register decrements that many from the parity fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will nto be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.

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5.2 CPSW

CPSW

5.2.1 CPSW Summaries

CPSW Summaries

Table 5-172. CPSW Registers, Base Address=5280 0000h, Length=2097152

Offset	Length	Register Name	CPSW0 Physical Address
0h	32	CPSW_IDVER_REG	5280 0000h
4h	32	CPSW_SS_SYNCE_COUNT_REG	5280 0004h
8h	32	CPSW_SS_SYNCE_MUX_REG	5280 0008h
Ch	32	CPSW_SS_CONTROL_REG	5280 000Ch
18h	32	CPSW_SS_INT_CONTROL_REG	5280 0018h
1Ch	32	CPSW_SS_STATUS_REG	5280 001Ch
20h	32	CPSW_SUBSYSTEM_CONFIG_REG	5280 0020h
30h	32	CPSW_RGMII1_STATUS_REG	5280 0030h
34h	32	CPSW_RGMII2_STATUS_REG	5280 0034h
F00h	32	CPSW_MDIO_VERSION_REG	5280 0F00h + formula
F04h	32	CPSW_MDIO_CONTROL_REG	5280 0F04h + formula
F08h	32	CPSW_MDIO_ALIVE_REG	5280 0F08h + formula
F0Ch	32	CPSW_MDIO_LINK_REG	5280 0F0Ch + formula
F10h	32	CPSW_MDIO_LINK_INT_RAW_REG	5280 0F10h + formula
F14h	32	CPSW_MDIO_LINK_INT_MASKED_REG	5280 0F14h + formula
F18h	32	CPSW_MDIO_LINK_INT_MASK_SET_REG	5280 0F18h + formula
F1Ch	32	CPSW_MDIO_LINK_INT_MASK_CLEAR_REG	5280 0F1Ch + formula
F20h	32	CPSW_MDIO_USER_INT_RAW_REG	5280 0F20h + formula
F24h	32	CPSW_MDIO_USER_INT_MASKED_REG	5280 0F24h + formula
F28h	32	CPSW_MDIO_USER_INT_MASK_SET_REG	5280 0F28h + formula
F2Ch	32	CPSW_MDIO_USER_INT_MASK_CLEAR_REG	5280 0F2Ch + formula
F30h	32	CPSW_MDIO_MANUAL_IF_REG	5280 0F30h + formula
F34h	32	CPSW_MDIO_POLL_REG	5280 0F34h + formula
F38h	32	CPSW_MDIO_POLL_EN_REG	5280 0F38h + formula
F3Ch	32	CPSW_MDIO_CLAUS45_REG	5280 0F3Ch + formula
F40h	32	CPSW_MDIO_USER_ADDR0_REG	5280 0F40h + formula
F44h	32	CPSW_MDIO_USER_ADDR1_REG	5280 0F44h + formula
1800h	32	CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG	5280 1800h + formula
1804h	32	CPSW_REGS_INT_SS_C0_TH_PULSE_EN_REG	5280 1804h + formula
1808h	32	CPSW_REGS_INT_SS_C0_FH_PULSE_EN_REG	5280 1808h + formula
180Ch	32	CPSW_REGS_INT_SS_C0_MISC_EN_REG	5280 180Ch + formula
1810h	32	CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG	5280 1810h + formula
1814h	32	CPSW_REGS_INT_SS_C0_TH_PULSE_STATUS_REG	5280 1814h + formula
1818h	32	CPSW_REGS_INT_SS_C0_FH_PULSE_STATUS_REG	5280 1818h + formula
181Ch	32	CPSW_REGS_INT_SS_C0_MISC_STATUS_REG	5280 181Ch + formula
1820h	32	CPSW_REGS_INT_SS_C0_TH_IMAX_REG	5280 1820h + formula
1824h	32	CPSW_REGS_INT_SS_C0_FH_IMAX_REG	5280 1824h + formula
1840h	32	CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG	5280 1840h + formula

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Table 5-172. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
1844h	32	CPSW_REGS_INT_SS_C1_TH_PULSE_EN_REG	5280 1844h + formula
1848h	32	CPSW_REGS_INT_SS_C1_FH_PULSE_EN_REG	5280 1848h + formula
184Ch	32	CPSW_REGS_INT_SS_C1_MISC_EN_REG	5280 184Ch + formula
1850h	32	CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG	5280 1850h + formula
1854h	32	CPSW_REGS_INT_SS_C1_TH_PULSE_STATUS_REG	5280 1854h + formula
1858h	32	CPSW_REGS_INT_SS_C1_FH_PULSE_STATUS_REG	5280 1858h + formula
185Ch	32	CPSW_REGS_INT_SS_C1_MISC_STATUS_REG	5280 185Ch + formula
1860h	32	CPSW_REGS_INT_SS_C1_TH_IMAX_REG	5280 1860h + formula
1864h	32	CPSW_REGS_INT_SS_C1_FH_IMAX_REG	5280 1864h + formula
1880h	32	CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG	5280 1880h + formula
1884h	32	CPSW_REGS_INT_SS_C2_TH_PULSE_EN_REG	5280 1884h + formula
1888h	32	CPSW_REGS_INT_SS_C2_FH_PULSE_EN_REG	5280 1888h + formula
188Ch	32	CPSW_REGS_INT_SS_C2_MISC_EN_REG	5280 188Ch + formula
1890h	32	CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG	5280 1890h + formula
1894h	32	CPSW_REGS_INT_SS_C2_TH_PULSE_STATUS_REG	5280 1894h + formula
1898h	32	CPSW_REGS_INT_SS_C2_FH_PULSE_STATUS_REG	5280 1898h + formula
189Ch	32	CPSW_REGS_INT_SS_C2_MISC_STATUS_REG	5280 189Ch + formula
18A0h	32	CPSW_REGS_INT_SS_C2_TH_IMAX_REG	5280 18A0h + formula
18A4h	32	CPSW_REGS_INT_SS_C2_FH_IMAX_REG	5280 18A4h + formula
18C0h	32	CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG	5280 18C0h + formula
18C4h	32	CPSW_REGS_INT_SS_C3_TH_PULSE_EN_REG	5280 18C4h + formula
18C8h	32	CPSW_REGS_INT_SS_C3_FH_PULSE_EN_REG	5280 18C8h + formula
18CCh	32	CPSW_REGS_INT_SS_C3_MISC_EN_REG	5280 18CCh + formula
18D0h	32	CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG	5280 18D0h + formula
18D4h	32	CPSW_REGS_INT_SS_C3_TH_PULSE_STATUS_REG	5280 18D4h + formula
18D8h	32	CPSW_REGS_INT_SS_C3_FH_PULSE_STATUS_REG	5280 18D8h + formula
18DCh	32	CPSW_REGS_INT_SS_C3_MISC_STATUS_REG	5280 18DCh + formula
18E0h	32	CPSW_REGS_INT_SS_C3_TH_IMAX_REG	5280 18E0h + formula
18E4h	32	CPSW_REGS_INT_SS_C3_FH_IMAX_REG	5280 18E4h + formula
20000h	32	CPSW_NC_VER_REG	5282 0000h + formula
20004h	32	CPSW_NC_CONTROL_REG	5282 0004h + formula
2000Ch	32	CPSW_NC_STATUS_REG	5282 000Ch + formula
20010h	32	CPSW_NC_EM_CONTROL_REG	5282 0010h + formula
20014h	32	CPSW_NC_STAT_PORT_EN_REG	5282 0014h + formula
20018h	32	CPSW_NC_PTYPE_REG	5282 0018h + formula
2001Ch	32	CPSW_NC_SOFT_IDLE_REG	5282 001Ch + formula
20020h	32	CPSW_NC_THRU_RATE_REG	5282 0020h + formula
20024h	32	CPSW_NC_GAP_THRESH_REG	5282 0024h + formula
2002Ch	32	CPSW_NC_EEE_PRESCALE_REG	5282 002Ch + formula
20030h	32	CPSW_NC_TX_G_OFLOW_THRESH_SET_REG	5282 0030h + formula
20034h	32	CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG	5282 0034h + formula
20038h	32	CPSW_NC_TX_G_BUF_THRESH_SET_L_REG	5282 0038h + formula
2003Ch	32	CPSW_NC_TX_G_BUF_THRESH_SET_H_REG	5282 003Ch + formula

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Table 5-172. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
20040h	32	CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG	5282 0040h + formula
20044h	32	CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG	5282 0044h + formula
20050h	32	CPSW_NC_VLAN_LTYPE_REG	5282 0050h + formula
20054h	32	CPSW_NC_EST_TS_DOMAIN_REG	5282 0054h + formula
20100h	32	CPSW_NC_TX_PRI0_MAXLEN_REG	5282 0100h + formula
20104h	32	CPSW_NC_TX_PRI1_MAXLEN_REG	5282 0104h + formula
20108h	32	CPSW_NC_TX_PRI2_MAXLEN_REG	5282 0108h + formula
2010Ch	32	CPSW_NC_TX_PRI3_MAXLEN_REG	5282 010Ch + formula
20110h	32	CPSW_NC_TX_PRI4_MAXLEN_REG	5282 0110h + formula
20114h	32	CPSW_NC_TX_PRI5_MAXLEN_REG	5282 0114h + formula
20118h	32	CPSW_NC_TX_PRI6_MAXLEN_REG	5282 0118h + formula
2011Ch	32	CPSW_NC_TX_PRI7_MAXLEN_REG	5282 011Ch + formula
F80h	32	CPSW_MDIO_USER_GROUP_USER_ACCESS_REG_J	5280 0F80h + formula
F84h	32	CPSW_MDIO_USER_GROUP_USER_PHY_SEL_REG_J	5280 0F84h + formula
21004h	32	CPSW_NC_CPPI_P0_CONTROL_REG	5282 1004h + formula
21010h	32	CPSW_NC_CPPI_P0_BLK_CNT_REG	5282 1010h + formula
21014h	32	CPSW_NC_CPPI_P0_PORT_VLAN_REG	5282 1014h + formula
21018h	32	CPSW_NC_CPPI_P0_TH_PRI_MAP_REG	5282 1018h + formula
2101Ch	32	CPSW_NC_CPPI_P0_PRI_CTL_REG	5282 101Ch + formula
21020h	32	CPSW_NC_CPPI_P0_FH_PRI_MAP_REG	5282 1020h + formula
21024h	32	CPSW_NC_CPPI_P0_FH_MAXLEN_REG	5282 1024h + formula
21028h	32	CPSW_NC_CPPI_P0_TH_BLKS_PRI_REG	5282 1028h + formula
21030h	32	CPSW_NC_CPPI_P0_IDLE2LPI_REG	5282 1030h + formula
21034h	32	CPSW_NC_CPPI_P0_LPI2WAKE_REG	5282 1034h + formula
21038h	32	CPSW_NC_CPPI_P0_EEE_STATUS_REG	5282 1038h + formula
21050h	32	CPSW_NC_CPPI_P0_FIFO_STATUS_REG	5282 1050h + formula
21120h	32	CPSW_NC_CPPI_FH_DSCP_MAP_REG_J	5282 1120h + formula
21140h	32	CPSW_NC_CPPI_P0_PRI_CIR_REG_J	5282 1140h + formula
21160h	32	CPSW_NC_CPPI_P0_PRI_EIR_REG_J	5282 1160h + formula
21180h	32	CPSW_NC_CPPI_P0_TH_D_THRESH_SET_L_REG	5282 1180h + formula
21184h	32	CPSW_NC_CPPI_P0_TH_D_THRESH_SET_H_REG	5282 1184h + formula
21188h	32	CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_L_REG	5282 1188h + formula
2118Ch	32	CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_H_REG	5282 118Ch + formula
21190h	32	CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_L_REG	5282 1190h + formula
21194h	32	CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_H_REG	5282 1194h + formula
21198h	32	CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_L_REG	5282 1198h + formula
2119Ch	32	CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_H_REG	5282 119Ch + formula
21300h	32	CPSW_NC_CPPI_P0_SRC_ID_A_REG	5282 1300h + formula
21304h	32	CPSW_NC_CPPI_P0_SRC_ID_B_REG	5282 1304h + formula
21320h	32	CPSW_NC_CPPI_P0_HOST_BLKS_PRI_REG	5282 1320h + formula
22004h	32	CPSW_NC_ETH_MAC_PN_CONTROL_REG_J	5282 2004h + formula
22008h	32	CPSW_NC_ETH_MAC_PN_MAX_BLKS_REG_J	5282 2008h + formula
22010h	32	CPSW_NC_ETH_MAC_PN_BLK_CNT_REG_J	5282 2010h + formula
22014h	32	CPSW_NC_ETH_MAC_PN_PORT_VLAN_REG_J	5282 2014h + formula
22018h	32	CPSW_NC_ETH_MAC_PN_TX_PRI_MAP_REG_J	5282 2018h + formula

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Table 5-172. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
2201Ch	32	CPSW_NC_ETH_MAC_PN_PRI_CTL_REG_J	5282 201Ch + formula
22020h	32	CPSW_NC_ETH_MAC_PN_RX_PRI_MAP_REG_J	5282 2020h + formula
22024h	32	CPSW_NC_ETH_MAC_PN_RX_MAXLEN_REG_J	5282 2024h + formula
22028h	32	CPSW_NC_ETH_MAC_PN_TX_BLKS_PRI_REG_J	5282 2028h + formula
22030h	32	CPSW_NC_ETH_MAC_PN_IDLE2LPI_REG_J	5282 2030h + formula
22034h	32	CPSW_NC_ETH_MAC_PN_LPI2WAKE_REG_J	5282 2034h + formula
22038h	32	CPSW_NC_ETH_MAC_PN_EEE_STATUS_REG_J	5282 2038h + formula
22050h	32	CPSW_NC_ETH_MAC_PN_FIFO_STATUS_REG_J	5282 2050h + formula
22060h	32	CPSW_NC_ETH_MAC_PN_EST_CONTROL_REG_J	5282 2060h + formula
22120h	32	CPSW_NC_ETH_MAC_PN_FH_DSCP_MAP_REG_J_K	5282 2120h + formula
22140h	32	CPSW_NC_ETH_MAC_PN_PRI_CIR_REG_J_K	5282 2140h + formula
22160h	32	CPSW_NC_ETH_MAC_PN_PRI_EIR_REG_J_K	5282 2160h + formula
22180h	32	CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_L_REG_J	5282 2180h + formula
22184h	32	CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_H_REG_J	5282 2184h + formula
22188h	32	CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_L_REG_J	5282 2188h + formula
2218Ch	32	CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_H_REG_J	5282 218Ch + formula
22190h	32	CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_L_REG_J	5282 2190h + formula
22194h	32	CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_H_REG_J	5282 2194h + formula
22198h	32	CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_L_REG_J	5282 2198h + formula
2219Ch	32	CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_H_REG_J	5282 219Ch + formula
22300h	32	CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_L_REG_J	5282 2300h + formula
22304h	32	CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_H_REG_J	5282 2304h + formula
22308h	32	CPSW_NC_ETH_MAC_PN_SA_L_REG_J	5282 2308h + formula
2230Ch	32	CPSW_NC_ETH_MAC_PN_SA_H_REG_J	5282 230Ch + formula
22310h	32	CPSW_NC_ETH_MAC_PN_TS_CTL_REG_J	5282 2310h + formula
22314h	32	CPSW_NC_ETH_MAC_PN_TS_SEQ_LTYPE_REG_J	5282 2314h + formula
22318h	32	CPSW_NC_ETH_MAC_PN_TS_VLAN_LTYPE_REG_J	5282 2318h + formula
2231Ch	32	CPSW_NC_ETH_MAC_PN_TS_CTL_LTYPE2_REG_J	5282 231Ch + formula
22320h	32	CPSW_NC_ETH_MAC_PN_TS_CTL2_REG_J	5282 2320h + formula
22330h	32	CPSW_NC_ETH_MAC_PN_MAC_CONTROL_REG_J	5282 2330h + formula
22334h	32	CPSW_NC_ETH_MAC_PN_MAC_STATUS_REG_J	5282 2334h + formula
22338h	32	CPSW_NC_ETH_MAC_PN_MAC_SOFT_RESET_REG_J	5282 2338h + formula
2233Ch	32	CPSW_NC_ETH_MAC_PN_MAC_BOFFTEST_REG_J	5282 233Ch + formula
22340h	32	CPSW_NC_ETH_MAC_PN_MAC_RX_PAUSETIMER_REG_J	5282 2340h + formula
22350h	32	CPSW_NC_ETH_MAC_PN_MAC_RXN_PAUSETIMER_REG_J_K	5282 2350h + formula
22370h	32	CPSW_NC_ETH_MAC_PN_MAC_TX_PAUSETIMER_REG_J	5282 2370h + formula
22380h	32	CPSW_NC_ETH_MAC_PN_MAC_TX0_PAUSETIMER_REG_J_K	5282 2380h + formula

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Table 5-172. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
223A0h	32	CPSW_NC_ETH_MAC_PN_MAC_EMCONTROL_REG_J	5282 23A0h + formula
223A4h	32	CPSW_NC_ETH_MAC_PN_MAC_TX_GAP_REG_J	5282 23A4h + formula
223A8h	32	CPSW_NC_ETH_MAC_PN_MAC_PORT_CONFIG_J	5282 23A8h + formula
223ACh	32	CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_POINTER_REG_J	5282 23ACh + formula
223B0h	32	CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_A_REG_J	5282 23B0h + formula
223B4h	32	CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_B_REG_J	5282 23B4h + formula
223B8h	32	CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_C_REG_J	5282 23B8h + formula
223BCh	32	CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_D_REG_J	5282 23BCh + formula
32000h	32	CPSW_NC_EST_FETCH_LOC	5283 2000h + formula
34000h	32	CPSW_NC_CPDMA_REGS_FH_IDVER_REG	5283 4000h + formula
34004h	32	CPSW_NC_CPDMA_REGS_FH_CONTROL_REG	5283 4004h + formula
34008h	32	CPSW_NC_CPDMA_REGS_FH_TEARDOWN_REG	5283 4008h + formula
3400Ch	32	CPSW_NC_CPDMA_REGS_FH_CONTROL2_REG	5283 400Ch + formula
34010h	32	CPSW_NC_CPDMA_REGS_TH_IDVER_REG	5283 4010h + formula
34014h	32	CPSW_NC_CPDMA_REGS_TH_CONTROL_REG	5283 4014h + formula
34018h	32	CPSW_NC_CPDMA_REGS_TH_TEARDOWN_REG	5283 4018h + formula
3401Ch	32	CPSW_NC_CPDMA_REGS_SOFT_RESET_REG	5283 401Ch + formula
34020h	32	CPSW_NC_CPDMA_REGS_CONTROL_REG	5283 4020h + formula
34024h	32	CPSW_NC_CPDMA_REGS_STATUS_REG	5283 4024h + formula
34028h	32	CPSW_NC_CPDMA_REGS_TH_BUFFER_OFFSET_REG	5283 4028h + formula
3402Ch	32	CPSW_NC_CPDMA_REGS_EMULATION_CONTROL_REG	5283 402Ch + formula
34080h	32	CPSW_NC_CPDMA_INT_FH_INTSTAT_RAW_REG	5283 4080h + formula
34084h	32	CPSW_NC_CPDMA_INT_FH_INTSTAT_MASKED_REG	5283 4084h + formula
34088h	32	CPSW_NC_CPDMA_INT_FH_INTMASK_SET_REG	5283 4088h + formula
3408Ch	32	CPSW_NC_CPDMA_INT_FH_INTMASK_CLEAR_REG	5283 408Ch + formula
34090h	32	CPSW_NC_CPDMA_INT_IN_VECTOR_REG	5283 4090h + formula
34094h	32	CPSW_NC_CPDMA_INT_EOI_VECTOR_REG	5283 4094h + formula
340A0h	32	CPSW_NC_CPDMA_INT_TH_INTSTAT_RAW_REG	5283 40A0h + formula
340A4h	32	CPSW_NC_CPDMA_INT_TH_INTSTAT_MASKED_REG	5283 40A4h + formula
340A8h	32	CPSW_NC_CPDMA_INT_TH_INTMASK_SET_REG	5283 40A8h + formula
340ACh	32	CPSW_NC_CPDMA_INT_TH_INTMASK_CLEAR_REG	5283 40ACh + formula
340B0h	32	CPSW_NC_CPDMA_INT_INTSTAT_RAW_REG	5283 40B0h + formula
340B4h	32	CPSW_NC_CPDMA_INT_INTSTAT_MASKED_REG	5283 40B4h + formula
340B8h	32	CPSW_NC_CPDMA_INT_INTMASK_SET_REG	5283 40B8h + formula
340BCh	32	CPSW_NC_CPDMA_INT_INTMASK_CLEAR_REG	5283 40BCh + formula
340C0h	32	CPSW_NC_CPDMA_INT_TH0_PENDTHRESH_REG	5283 40C0h + formula
340C4h	32	CPSW_NC_CPDMA_INT_TH1_PENDTHRESH_REG	5283 40C4h + formula
340C8h	32	CPSW_NC_CPDMA_INT_TH2_PENDTHRESH_REG	5283 40C8h + formula
340CCh	32	CPSW_NC_CPDMA_INT_TH3_PENDTHRESH_REG	5283 40CCh + formula
340D0h	32	CPSW_NC_CPDMA_INT_TH4_PENDTHRESH_REG	5283 40D0h + formula
340D4h	32	CPSW_NC_CPDMA_INT_TH5_PENDTHRESH_REG	5283 40D4h + formula
340D8h	32	CPSW_NC_CPDMA_INT_TH6_PENDTHRESH_REG	5283 40D8h + formula
340DCh	32	CPSW_NC_CPDMA_INT_TH7_PENDTHRESH_REG	5283 40DCh + formula
340E0h	32	CPSW_NC_CPDMA_INT_TH0_FREEBUFFER_REG	5283 40E0h + formula
340E4h	32	CPSW_NC_CPDMA_INT_TH1_FREEBUFFER_REG	5283 40E4h + formula

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Table 5-172. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
340E8h	32	CPSW_NC_CPDMA_INT_TH2_FREEBUFFER_REG	5283 40E8h + formula
340ECh	32	CPSW_NC_CPDMA_INT_TH3_FREEBUFFER_REG	5283 40ECh + formula
340F0h	32	CPSW_NC_CPDMA_INT_TH4_FREEBUFFER_REG	5283 40F0h + formula
340F4h	32	CPSW_NC_CPDMA_INT_TH5_FREEBUFFER_REG	5283 40F4h + formula
340F8h	32	CPSW_NC_CPDMA_INT_TH6_FREEBUFFER_REG	5283 40F8h + formula
340FCh	32	CPSW_NC_CPDMA_INT_TH7_FREEBUFFER_REG	5283 40FCh + formula
34200h	32	CPSW_NC_CPDMA_SRAM_FH0_HDP_REG	5283 4200h + formula
34204h	32	CPSW_NC_CPDMA_SRAM_FH1_HDP_REG	5283 4204h + formula
34208h	32	CPSW_NC_CPDMA_SRAM_FH2_HDP_REG	5283 4208h + formula
3420Ch	32	CPSW_NC_CPDMA_SRAM_FH3_HDP_REG	5283 420Ch + formula
34210h	32	CPSW_NC_CPDMA_SRAM_FH4_HDP_REG	5283 4210h + formula
34214h	32	CPSW_NC_CPDMA_SRAM_FH5_HDP_REG	5283 4214h + formula
34218h	32	CPSW_NC_CPDMA_SRAM_FH6_HDP_REG	5283 4218h + formula
3421Ch	32	CPSW_NC_CPDMA_SRAM_FH7_HDP_REG	5283 421Ch + formula
34220h	32	CPSW_NC_CPDMA_SRAM_TH0_HDP_REG	5283 4220h + formula
34224h	32	CPSW_NC_CPDMA_SRAM_TH1_HDP_REG	5283 4224h + formula
34228h	32	CPSW_NC_CPDMA_SRAM_TH2_HDP_REG	5283 4228h + formula
3422Ch	32	CPSW_NC_CPDMA_SRAM_TH3_HDP_REG	5283 422Ch + formula
34230h	32	CPSW_NC_CPDMA_SRAM_TH4_HDP_REG	5283 4230h + formula
34234h	32	CPSW_NC_CPDMA_SRAM_TH5_HDP_REG	5283 4234h + formula
34238h	32	CPSW_NC_CPDMA_SRAM_TH6_HDP_REG	5283 4238h + formula
3423Ch	32	CPSW_NC_CPDMA_SRAM_TH7_HDP_REG	5283 423Ch + formula
34240h	32	CPSW_NC_CPDMA_SRAM_FH0_CP_REG	5283 4240h + formula
34244h	32	CPSW_NC_CPDMA_SRAM_FH1_CP_REG	5283 4244h + formula
34248h	32	CPSW_NC_CPDMA_SRAM_FH2_CP_REG	5283 4248h + formula
3424Ch	32	CPSW_NC_CPDMA_SRAM_FH3_CP_REG	5283 424Ch + formula
34250h	32	CPSW_NC_CPDMA_SRAM_FH4_CP_REG	5283 4250h + formula
34254h	32	CPSW_NC_CPDMA_SRAM_FH5_CP_REG	5283 4254h + formula
34258h	32	CPSW_NC_CPDMA_SRAM_FH6_CP_REG	5283 4258h + formula
3425Ch	32	CPSW_NC_CPDMA_SRAM_FH7_CP_REG	5283 425Ch + formula
34260h	32	CPSW_NC_CPDMA_SRAM_TH0_CP_REG	5283 4260h + formula
34264h	32	CPSW_NC_CPDMA_SRAM_TH1_CP_REG	5283 4264h + formula
34268h	32	CPSW_NC_CPDMA_SRAM_TH2_CP_REG	5283 4268h + formula
3426Ch	32	CPSW_NC_CPDMA_SRAM_TH3_CP_REG	5283 426Ch + formula
34270h	32	CPSW_NC_CPDMA_SRAM_TH4_CP_REG	5283 4270h + formula
34274h	32	CPSW_NC_CPDMA_SRAM_TH5_CP_REG	5283 4274h + formula
34278h	32	CPSW_NC_CPDMA_SRAM_TH6_CP_REG	5283 4278h + formula
3427Ch	32	CPSW_NC_CPDMA_SRAM_TH7_CP_REG	5283 427Ch + formula
34300h	32	CPSW_NC_CPDMA_SRAM_TEST_FH0_HDP_REG	5283 4300h + formula
34304h	32	CPSW_NC_CPDMA_SRAM_TEST_FH1_HDP_REG	5283 4304h + formula
34308h	32	CPSW_NC_CPDMA_SRAM_TEST_FH2_HDP_REG	5283 4308h + formula
3430Ch	32	CPSW_NC_CPDMA_SRAM_TEST_FH3_HDP_REG	5283 430Ch + formula
34310h	32	CPSW_NC_CPDMA_SRAM_TEST_FH4_HDP_REG	5283 4310h + formula
34314h	32	CPSW_NC_CPDMA_SRAM_TEST_FH5_HDP_REG	5283 4314h + formula
34318h	32	CPSW_NC_CPDMA_SRAM_TEST_FH6_HDP_REG	5283 4318h + formula
3431Ch	32	CPSW_NC_CPDMA_SRAM_TEST_FH7_HDP_REG	5283 431Ch + formula
34320h	32	CPSW_NC_CPDMA_SRAM_TEST_TH0_HDP_REG	5283 4320h + formula

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Table 5-172. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
34324h	32	CPSW_NC_CPDMA_SRAM_TEST_TH1_HDP_REG	5283 4324h + formula
34328h	32	CPSW_NC_CPDMA_SRAM_TEST_TH2_HDP_REG	5283 4328h + formula
3432Ch	32	CPSW_NC_CPDMA_SRAM_TEST_TH3_HDP_REG	5283 432Ch + formula
34330h	32	CPSW_NC_CPDMA_SRAM_TEST_TH4_HDP_REG	5283 4330h + formula
34334h	32	CPSW_NC_CPDMA_SRAM_TEST_TH5_HDP_REG	5283 4334h + formula
34338h	32	CPSW_NC_CPDMA_SRAM_TEST_TH6_HDP_REG	5283 4338h + formula
3433Ch	32	CPSW_NC_CPDMA_SRAM_TEST_TH7_HDP_REG	5283 433Ch + formula
34340h	32	CPSW_NC_CPDMA_SRAM_TEST_FH0_CP_REG	5283 4340h + formula
34344h	32	CPSW_NC_CPDMA_SRAM_TEST_FH1_CP_REG	5283 4344h + formula
34348h	32	CPSW_NC_CPDMA_SRAM_TEST_FH2_CP_REG	5283 4348h + formula
3434Ch	32	CPSW_NC_CPDMA_SRAM_TEST_FH3_CP_REG	5283 434Ch + formula
34350h	32	CPSW_NC_CPDMA_SRAM_TEST_FH4_CP_REG	5283 4350h + formula
34354h	32	CPSW_NC_CPDMA_SRAM_TEST_FH5_CP_REG	5283 4354h + formula
34358h	32	CPSW_NC_CPDMA_SRAM_TEST_FH6_CP_REG	5283 4358h + formula
3435Ch	32	CPSW_NC_CPDMA_SRAM_TEST_FH7_CP_REG	5283 435Ch + formula
34360h	32	CPSW_NC_CPDMA_SRAM_TEST_TH0_CP_REG	5283 4360h + formula
34364h	32	CPSW_NC_CPDMA_SRAM_TEST_TH1_CP_REG	5283 4364h + formula
34368h	32	CPSW_NC_CPDMA_SRAM_TEST_TH2_CP_REG	5283 4368h + formula
3436Ch	32	CPSW_NC_CPDMA_SRAM_TEST_TH3_CP_REG	5283 436Ch + formula
34370h	32	CPSW_NC_CPDMA_SRAM_TEST_TH4_CP_REG	5283 4370h + formula
34374h	32	CPSW_NC_CPDMA_SRAM_TEST_TH5_CP_REG	5283 4374h + formula
34378h	32	CPSW_NC_CPDMA_SRAM_TEST_TH6_CP_REG	5283 4378h + formula
3437Ch	32	CPSW_NC_CPDMA_SRAM_TEST_TH7_CP_REG	5283 437Ch + formula
3A000h	32	CPSW_NC_STAT_RXGOODFRAMES_J	5283 A000h + formula
3A004h	32	CPSW_NC_STAT_RXBROADCASTFRAMES_J	5283 A004h + formula
3A008h	32	CPSW_NC_STAT_RXMULTICASTFRAMES_J	5283 A008h + formula
3A00Ch	32	CPSW_NC_STAT_RXPAUSEFRAMES_J	5283 A00Ch + formula
3A010h	32	CPSW_NC_STAT_RXCRCERRORS_J	5283 A010h + formula
3A014h	32	CPSW_NC_STAT_RXALIGNCODEERRORS_J	5283 A014h + formula
3A018h	32	CPSW_NC_STAT_RXOVERSIZEDFRAMES_J	5283 A018h + formula
3A01Ch	32	CPSW_NC_STAT_RXJABBERFRAMES_J	5283 A01Ch + formula
3A020h	32	CPSW_NC_STAT_RXUNDERSIZEDFRAMES_J	5283 A020h + formula
3A024h	32	CPSW_NC_STAT_RXFRAGMENTS_J	5283 A024h + formula
3A028h	32	CPSW_NC_STAT_ALE_DROP_J	5283 A028h + formula
3A02Ch	32	CPSW_NC_STAT_ALE_OVERRUN_DROP_J	5283 A02Ch + formula
3A030h	32	CPSW_NC_STAT_RXOCTETS_J	5283 A030h + formula
3A034h	32	CPSW_NC_STAT_TXGOODFRAMES_J	5283 A034h + formula
3A038h	32	CPSW_NC_STAT_TXBROADCASTFRAMES_J	5283 A038h + formula
3A03Ch	32	CPSW_NC_STAT_TXMULTICASTFRAMES_J	5283 A03Ch + formula
3A040h	32	CPSW_NC_STAT_TXPAUSEFRAMES_J	5283 A040h + formula
3A044h	32	CPSW_NC_STAT_TXDEFERREDFRAMES_J	5283 A044h + formula
3A048h	32	CPSW_NC_STAT_TXCOLLISIONFRAMES_J	5283 A048h + formula
3A04Ch	32	CPSW_NC_STAT_TXSINGLECOLLFRAMES_J	5283 A04Ch + formula
3A050h	32	CPSW_NC_STAT_TXMULTCOLLFRAMES_J	5283 A050h + formula
3A054h	32	CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_J	5283 A054h + formula
3A058h	32	CPSW_NC_STAT_TXLATECOLLISIONS_J	5283 A058h + formula
3A05Ch	32	CPSW_NC_STAT_RXIPGERROR_J	5283 A05Ch + formula

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Table 5-172. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
3A060h	32	CPSW_NC_STAT_TXCARRIERSENSEERRORS_J	5283 A060h + formula
3A064h	32	CPSW_NC_STAT_TXOCTETS_J	5283 A064h + formula
3A068h	32	CPSW_NC_STAT_OCTETFRAMES64_J	5283 A068h + formula
3A06Ch	32	CPSW_NC_STAT_OCTETFRAMES65T127_J	5283 A06Ch + formula
3A070h	32	CPSW_NC_STAT_OCTETFRAMES128T255_J	5283 A070h + formula
3A074h	32	CPSW_NC_STAT_OCTETFRAMES256T511_J	5283 A074h + formula
3A078h	32	CPSW_NC_STAT_OCTETFRAMES512T1023_J	5283 A078h + formula
3A07Ch	32	CPSW_NC_STAT_OCTETFRAMES1024TUP_J	5283 A07Ch + formula
3A080h	32	CPSW_NC_STAT_NETOCTETS_J	5283 A080h + formula
3A084h	32	CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_J	5283 A084h + formula
3A088h	32	CPSW_NC_STAT_PORTMASK_DROP_J	5283 A088h + formula
3A08Ch	32	CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_J	5283 A08Ch + formula
3A090h	32	CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_J	5283 A090h + formula
3A094h	32	CPSW_NC_STAT_ALE_VID_INGRESS_DROP_J	5283 A094h + formula
3A098h	32	CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_J	5283 A098h + formula
3A09Ch	32	CPSW_NC_STAT_ALE_BLOCK_DROP_J	5283 A09Ch + formula
3A0A0h	32	CPSW_NC_STAT_ALE_SECURE_DROP_J	5283 A0A0h + formula
3A0A4h	32	CPSW_NC_STAT_ALE_AUTH_DROP_J	5283 A0A4h + formula
3A0A8h	32	CPSW_NC_STAT_ALE_UNKN_UNI_J	5283 A0A8h + formula
3A0ACh	32	CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_J	5283 A0ACh + formula
3A0B0h	32	CPSW_NC_STAT_ALE_UNKN_MLT_J	5283 A0B0h + formula
3A0B4h	32	CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_J	5283 A0B4h + formula
3A0B8h	32	CPSW_NC_STAT_ALE_UNKN_BRD_J	5283 A0B8h + formula
3A0BCh	32	CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_J	5283 A0BCh + formula
3A0C0h	32	CPSW_NC_STAT_ALE_POL_MATCH_J	5283 A0C0h + formula
3A0C4h	32	CPSW_NC_STAT_ALE_POL_MATCH_RED_J	5283 A0C4h + formula
3A0C8h	32	CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_J	5283 A0C8h + formula
3A0CCh	32	CPSW_NC_STAT_ALE_MULT_SA_DROP_J	5283 A0CCh + formula
3A0D0h	32	CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_J	5283 A0D0h + formula
3A0D4h	32	CPSW_NC_STAT_ALE_LEN_ERROR_DROP_J	5283 A0D4h + formula
3A0D8h	32	CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_J	5283 A0D8h + formula
3A0DCh	32	CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_J	5283 A0DCh + formula
3A17Ch	32	CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_J	5283 A17Ch + formula
3A180h	32	CPSW_NC_STAT_ENET_PN_TX_PRI_REG_J_K	5283 A180h + formula
3A1A0h	32	CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_J_K	5283 A1A0h + formula
3A1C0h	32	CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_J_K	5283 A1C0h + formula
3A1E0h	32	CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_K	5283 A1E0h + formula
3D000h	32	CPSW_NC_CPTS_IDVER_REG	5283 D000h + formula
3D004h	32	CPSW_NC_CPTS_CONTROL_REG	5283 D004h + formula
3D008h	32	CPSW_NC_CPTS_RFTCLK_SEL_REG	5283 D008h + formula
3D00Ch	32	CPSW_NC_CPTS_TS_PUSH_REG	5283 D00Ch + formula
3D010h	32	CPSW_NC_CPTS_TS_LOAD_VAL_REG	5283 D010h + formula
3D014h	32	CPSW_NC_CPTS_TS_LOAD_EN_REG	5283 D014h + formula
3D018h	32	CPSW_NC_CPTS_TS_COMP_VAL_REG	5283 D018h + formula
3D01Ch	32	CPSW_NC_CPTS_TS_COMP_LEN_REG	5283 D01Ch + formula
3D020h	32	CPSW_NC_CPTS_INTSTAT_RAW_REG	5283 D020h + formula

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Table 5-172. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
3D024h	32	CPSW_NC_CPTS_INTSTAT_MASKED_REG	5283 D024h + formula
3D028h	32	CPSW_NC_CPTS_INT_ENABLE_REG	5283 D028h + formula
3D02Ch	32	CPSW_NC_CPTS_TS_COMP_NUDGE_REG	5283 D02Ch + formula
3D030h	32	CPSW_NC_CPTS_EVENT_POP_REG	5283 D030h + formula
3D034h	32	CPSW_NC_CPTS_EVENT_0_REG	5283 D034h + formula
3D038h	32	CPSW_NC_CPTS_EVENT_1_REG	5283 D038h + formula
3D03Ch	32	CPSW_NC_CPTS_EVENT_2_REG	5283 D03Ch + formula
3D040h	32	CPSW_NC_CPTS_EVENT_3_REG	5283 D040h + formula
3D044h	32	CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG	5283 D044h + formula
3D048h	32	CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG	5283 D048h + formula
3D04Ch	32	CPSW_NC_CPTS_TS_ADD_VAL_REG	5283 D04Ch + formula
3D050h	32	CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG	5283 D050h + formula
3D054h	32	CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG	5283 D054h + formula
3D058h	32	CPSW_NC_CPTS_TS_NUDGE_VAL_REG	5283 D058h + formula
3D0D0h	32	CPSW_NC_CPTS_TS_CONFIG	5283 D0D0h + formula
3E000h	32	CPSW_NC_ALE_MOD_VER	5283 E000h + formula
3E004h	32	CPSW_NC_ALE_STATUS	5283 E004h + formula
3E008h	32	CPSW_NC_ALE_CONTROL	5283 E008h + formula
3E00Ch	32	CPSW_NC_ALE_CTRL2	5283 E00Ch + formula
3E010h	32	CPSW_NC_ALE_PRESCALE	5283 E010h + formula
3E014h	32	CPSW_NC_ALE_AGING_CTRL	5283 E014h + formula
3E01Ch	32	CPSW_NC_ALE_NXT_HDR	5283 E01Ch + formula
3E020h	32	CPSW_NC_ALE_TBLCTL	5283 E020h + formula
3E034h	32	CPSW_NC_ALE_TBLW2	5283 E034h + formula
3E038h	32	CPSW_NC_ALE_TBLW1	5283 E038h + formula
3E03Ch	32	CPSW_NC_ALE_TBLW0	5283 E03Ch + formula
3E040h	32	CPSW_NC_ALE_I0_PORTCTL0_J	5283 E040h + formula
3E090h	32	CPSW_NC_ALE_UVLAN_MEMBER	5283 E090h + formula
3E094h	32	CPSW_NC_ALE_UVLAN_URCAST	5283 E094h + formula
3E098h	32	CPSW_NC_ALE_UVLAN_RMCAST	5283 E098h + formula
3E09Ch	32	CPSW_NC_ALE_UVLAN_UNTAG	5283 E09Ch + formula
3E0B4h	32	CPSW_NC_ALE_FAST_LUT	5283 E0B4h + formula
3E0B8h	32	CPSW_NC_ALE_STAT_DIAG	5283 E0B8h + formula
3E0BCh	32	CPSW_NC_ALE_OAM_LB_CTRL	5283 E0BCh + formula
3E0FCh	32	CPSW_NC_ALE_EGRESSOP	5283 E0FCh + formula
3E100h	32	CPSW_NC_ALE_POLICECFG0	5283 E100h + formula
3E104h	32	CPSW_NC_ALE_POLICECFG1	5283 E104h + formula
3E108h	32	CPSW_NC_ALE_POLICECFG2	5283 E108h + formula
3E10Ch	32	CPSW_NC_ALE_POLICECFG3	5283 E10Ch + formula
3E110h	32	CPSW_NC_ALE_POLICECFG4	5283 E110h + formula
3E118h	32	CPSW_NC_ALE_POLICECFG6	5283 E118h + formula
3E11Ch	32	CPSW_NC_ALE_POLICECFG7	5283 E11Ch + formula
3E120h	32	CPSW_NC_ALE_POLICETBLCTL	5283 E120h + formula
3E124h	32	CPSW_NC_ALE_POLICECONTROL	5283 E124h + formula
3E128h	32	CPSW_NC_ALE_POLICETESTCTL	5283 E128h + formula
3E12Ch	32	CPSW_NC_ALE_POLICEHSTAT	5283 E12Ch + formula
3E134h	32	CPSW_NC_ALE_THREADMAPDEF	5283 E134h + formula

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Table 5-172. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)

Offset	Length	Register Name	CPSW0 Physical Address
3E138h	32	CPSW_NC_ALE_THREADMAPCTL	5283 E138h + formula
3E13Ch	32	CPSW_NC_ALE_THREADMAPVAL	5283 E13Ch + formula
3F000h	32	CPSW_NC_ECC_REV	5283 F000h + formula
3F008h	32	CPSW_NC_ECC_VECTOR	5283 F008h + formula
3F00Ch	32	CPSW_NC_ECC_STAT	5283 F00Ch + formula
3F010h	32	CPSW_NC_ECC_RESERVED_SVBUS_J	5283 F010h + formula
3F03Ch	32	CPSW_NC_ECC_SEC_EOI_REG	5283 F03Ch + formula
3F040h	32	CPSW_NC_ECC_SEC_STATUS_REG0	5283 F040h + formula
3F080h	32	CPSW_NC_ECC_SEC_ENABLE_SET_REG0	5283 F080h + formula
3F0C0h	32	CPSW_NC_ECC_SEC_ENABLE_CLR_REG0	5283 F0C0h + formula
3F13Ch	32	CPSW_NC_ECC_DED_EOI_REG	5283 F13Ch + formula
3F140h	32	CPSW_NC_ECC_DED_STATUS_REG0	5283 F140h + formula
3F180h	32	CPSW_NC_ECC_DED_ENABLE_SET_REG0	5283 F180h + formula
3F1C0h	32	CPSW_NC_ECC_DED_ENABLE_CLR_REG0	5283 F1C0h + formula
3F200h	32	CPSW_NC_ECC_AGGR_ENABLE_SET	5283 F200h + formula
3F204h	32	CPSW_NC_ECC_AGGR_ENABLE_CLR	5283 F204h + formula
3F208h	32	CPSW_NC_ECC_AGGR_STATUS_SET	5283 F208h + formula
3F20Ch	32	CPSW_NC_ECC_AGGR_STATUS_CLR	5283 F20Ch + formula
3D0E0h	32	CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_J	5283 D0E0h + formula
3D0E4h	32	CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_J	5283 D0E4h + formula
3D0E8h	32	CPSW_NC_CPTS_TS_GENF_CONTROL_REG_J	5283 D0E8h + formula
3D0ECh	32	CPSW_NC_CPTS_TS_GENF_LENGTH_REG_J	5283 D0ECh + formula
3D0F0h	32	CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_J	5283 D0F0h + formula
3D0F4h	32	CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_J	5283 D0F4h + formula
3D0F8h	32	CPSW_NC_CPTS_TS_GENF_NUDGE_REG_J	5283 D0F8h + formula
3D200h	32	CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_J	5283 D200h + formula
3D204h	32	CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_J	5283 D204h + formula
3D208h	32	CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_J	5283 D208h + formula
3D20Ch	32	CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_J	5283 D20Ch + formula
3D210h	32	CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_J	5283 D210h + formula
3D214h	32	CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_J	5283 D214h + formula
3D218h	32	CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_J	5283 D218h + formula

5.2.2 CPSW Registers

CPSW Registers

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5.2.2.1 CPSW_IDVER_REG Register

5.2.2.1.1 CPSW_IDVER_REG Register (Offset = 0h) [reset = 6BA03103h]

ID Version Register.

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Table 5-173. Instance Table

Instance Name	Physical Address
CPSW0	5280 0000h

Figure 5-82. CPSW_IDVER_REG Name Register

31	30	29	28	27	26	25	24
IDENT							
R							
6BA0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IDENT							
R							
6BA0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VER					MAJOR_VER		
R					R		
3h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MINOR_VER							
R							
3h							

Table 5-174. CPSW_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	6BA0h	Identification value
15:11	RTL_VER	R	3h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	3h	Minor version value

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5.2.2.2 CPSW_SS_SYNCE_COUNT_REG Register

5.2.2.2.1 CPSW_SS_SYNCE_COUNT_REG Register (Offset = 4h) [reset = 0h]

SS SYNCE Count Register.

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Table 5-175. Instance Table

Instance Name	Physical Address
CPSW0	5280 0004h

Figure 5-83. CPSW_SS_SYNCE_COUNT_REG Name Register

31	30	29	28	27	26	25	24
SYNCE_CNT							
R/W							
0h							
23	22	21	20	19	18	17	16
SYNCE_CNT							
R/W							
0h							
15	14	13	12	11	10	9	8
SYNCE_CNT							
R/W							
0h							
7	6	5	4	3	2	1	0
SYNCE_CNT							
R/W							
0h							

Table 5-176. CPSW_SS_SYNCE_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SYNCE_CNT	R/W	0h	SyncE Count Value - This value determines the toggle rate of the TS_SYNCE output. When this value is zero the TS_SYNCE output is disabled (low). When this value is non-zero, the TS_SYNCE output toggles each time the synce count value is reached. If this value is to be changed to another non-zero value then it should be written with a zero value before Writing the new non-zero value.

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5.2.2.3 CPSW_SS_SYNCE_MUX_REG Register

5.2.2.3.1 CPSW_SS_SYNCE_MUX_REG Register (Offset = 8h) [reset = 0h]

SS Synce Mux Register.

Return to Summary Table

Table 5-177. Instance Table

Instance Name	Physical Address
CPSW0	5280 0008h

Figure 5-84. CPSW_SS_SYNCE_MUX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		SYNCE_SEL		SYNCE_PORT_SEL			
NONE		R/W		R/W			
0h		0h		0h			

Table 5-178. CPSW_SS_SYNCE_MUX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:4	SYNCE_SEL	R/W	0h	Sync E Interface Select. 00 - GMIIn_MRCLK_I input clock from selected GMII port 01 - RMII_MHZ_50_CLK (same for all ports if RMII included) 10 - RGMIIn_RXC_I input clock from selected port (If RGMII included) 11 - SERDESn_RXCLK from selected port (If SGMII included)
3:0	SYNCE_PORT_SEL	R/W	0h	Sync E Port Select - This field selects the port that will be used for the synchronous Ethernet receive clock. The port interface is selected with synce_sel. 0 - Port 1 1 - Port 2 ... 7 - Port 8 8-15 - Reserved

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5.2.2.4 CPSW_SS_CONTROL_REG Register

5.2.2.4.1 CPSW_SS_CONTROL_REG Register (Offset = Ch) [reset = 0h]

SS Control Register.

Return to Summary Table

Table 5-179. Instance Table

Instance Name	Physical Address
CPSW0	5280 000Ch

Figure 5-85. CPSW_SS_CONTROL_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED</td><td>EEE_PHY_ONLY</td><td>EEE_EN</td></tr>
<tr><td colspan="6">NONE</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-180. CPSW_SS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	EEE_PHY_ONLY	R/W	0h	Energy Efficient Enable Phy Only Mode. 0 - The low power indicate state (LPI) includes gating off the CPPI_GCLK to the CPSW. 1 - The low power indicate state (LPI) does not gate the clock to the CPSW
0	EEE_EN	R/W	0h	Energy Efficient Ethernet Enable. 0 - EEE is disabled 1 - EEE is enabled

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5.2.2.5 CPSW_SS_INT_CONTROL_REG Register

5.2.2.5.1 CPSW_SS_INT_CONTROL_REG Register (Offset = 18h) [reset = 0h]

SS Interrupt Control Register.

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Table 5-181. Instance Table

Instance Name	Physical Address
CPSW0	5280 0018h

Figure 5-86. CPSW_SS_INT_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
INT_TEST	INT_SEL_VEC_EN	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		INT_PACE_EN					
NONE		R/W					
0h		0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				INT_PRESCALE			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INT_PRESCALE							
R/W							
0h							

Table 5-182. CPSW_SS_INT_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_TEST	R/W	0h	Interrupt Test - Test bit to the interrupt pacing blocks
30	INT_SEL_VEC_EN	R/W	0h	Interrupt Select Vector Enable. 0 - in_vector is an 8-bit mask for tx_pend, rx_pend, and rx_thresh_pend. 1 - in_vector is the 3-bit encoded value of the highest interrupt channel set for tx_pend, rx_pend, and rx_thresh_pend.
29:22	RESERVED	NONE	0h	Reserved
21:16	INT_PACE_EN	R/W	0h	Interrupt Pacing Enable Bus. int_pace_en[0] - Enables C0_Rx_Pulse Pacing (0 is pacing bypass) int_pace_en[1] - Enables C0_Tx_Pulse Pacing (0 is pacing bypass) int_pace_en[2] - Enables C1_Rx_Pulse Pacing (0 is pacing bypass) int_pace_en[3] - Enables C1_Tx_Pulse Pacing (0 is pacing bypass) int_pace_en[4] - Enables C2_Rx_Pulse Pacing (0 is pacing bypass) int_pace_en[5] - Enables C2_Tx_Pulse Pacing (0 is pacing bypass)
15:12	RESERVED	NONE	0h	Reserved
11:0	INT_PRESCALE	R/W	0h	Interrupt Counter Prescaler - The number of VBUSP_CLK periods in 4us.

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5.2.2.6 CPSW_SS_STATUS_REG Register

5.2.2.6.1 CPSW_SS_STATUS_REG Register (Offset = 1Ch) [reset = 0h]

SS Status Register.

Return to Summary Table

Table 5-183. Instance Table

Instance Name	Physical Address
CPSW0	5280 001Ch

Figure 5-87. CPSW_SS_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EEE_CLKSTOP_ACK
NONE							R
0h							0h

Table 5-184. CPSW_SS_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EEE_CLKSTOP_ACK	R	0h	Energy Efficient Ethernet clockstop acknowledge from CPSW

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5.2.2.7 CPSW_SUBSYSTEM_CONFIG_REG Register

5.2.2.7.1 CPSW_SUBSYSTEM_CONFIG_REG Register (Offset = 20h) [reset = 30203h]

Subsystem Configuration Register.

Return to Summary Table

Table 5-185. Instance Table

Instance Name	Physical Address
CPSW0	5280 0020h

Figure 5-88. CPSW_SUBSYSTEM_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RESERVED				XGMII			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XGMII				QSGMII	SGMII	RGMII	RMII
R				R	R	R	R
0h				0h	0h	1h	1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			NUM_GENF				
NONE			R				
0h			2h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_PORTS							
R							
3h							

Table 5-186. CPSW_SUBSYSTEM_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:20	XGMII	R	0h	The Number of XGMII Ports included in the CPSW
19	QSGMII	R	0h	QSGMII is included in the CPSW
18	SGMII	R	0h	SGMII is included in the CPSW
17	RGMII	R	1h	RGMII is included in the CPSW
16	RMII	R	1h	RMII is included in the CPSW
15:13	RESERVED	NONE	0h	Reserved
12:8	NUM_GENF	R	2h	The number of CPTS GENF outputs
7:0	NUM_PORTS	R	3h	The total number of ports including the host port 0

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5.2.2.8 CPSW_RGMII1_STATUS_REG Register

5.2.2.8.1 CPSW_RGMII1_STATUS_REG Register (Offset = 30h) [reset = 0h]

RGMII1 Status Register.

Return to Summary Table

Table 5-187. Instance Table

Instance Name	Physical Address
CPSW0	5280 0030h

Figure 5-89. CPSW_RGMII1_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
NONE				R	R		R
0h				0h	0h		0h

Table 5-188. CPSW_RGMII1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	FULLDUPLEX	R	0h	Rgmii1 Full-duplex 0 - Half-duplex 1 - Full-duplex
2:1	SPEED	R	0h	Rgmii1 Speed 00 - 10Mbps 01 - 100Mbps 10 - 1000Mbps 11 - reserved
0	LINK	R	0h	Rgmii1 Link Indicator 0 - Link is down 1 - Link is up

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5.2.2.9 CPSW_RGMII2_STATUS_REG Register

5.2.2.9.1 CPSW_RGMII2_STATUS_REG Register (Offset = 34h) [reset = 0h]

RGMII2 Status Register.

Return to Summary Table

Table 5-189. Instance Table

Instance Name	Physical Address
CPSW0	5280 0034h

Figure 5-90. CPSW_RGMII2_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				FULLDUPLEX	SPEED		LINK
NONE				R	R		R
0h				0h	0h		0h

Table 5-190. CPSW_RGMII2_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3	FULLDUPLEX	R	0h	Rgmii2 Full-duplex 0 - Half-duplex 1 - Full-duplex
2:1	SPEED	R	0h	Rgmii2 Speed 00 - 10Mbps 01 - 100Mbps 10 - 1000Mbps 11 - reserved
0	LINK	R	0h	Rgmii2 Link Indicator 0 - Link is down 1 - Link is up

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5.2.2.10 CPSW_MDIO_VERSION_REG Register

5.2.2.10.1 CPSW_MDIO_VERSION_REG Register (Offset = F00h) [reset = 71107h]

MDIO Version Register

Return to Summary Table

Table 5-191. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F00h + formula

Figure 5-91. CPSW_MDIO_VERSION_REG Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
0h		0h		7h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
7h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
2h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		7h					

Table 5-192. CPSW_MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	0h	Scheme
29:28	BU	R	0h	bu
27:16	MODULE_ID	R	7h	Module ID
15:11	REVRTL	R	2h	RTL version
10:8	REVMAJ	R	1h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	7h	Minor version

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5.2.2.11 CPSW_MDIO_CONTROL_REG Register

5.2.2.11.1 CPSW_MDIO_CONTROL_REG Register (Offset = F04h) [reset = 810000FFh]

MDIO Control Register

Return to Summary Table

Table 5-193. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F04h + formula

Figure 5-92. CPSW_MDIO_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R	R/W	NONE	R				
1h	0h	0h	1h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
NONE			R/W	R/W	R/W	R/W	NONE
0h			0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKDIV							
R/W							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKDIV							
R/W							
FFh							

Table 5-194. CPSW_MDIO_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine IDLE. Set to 1 by the hardware when the state machine is in the idle state.
30	ENABLE	R/W	0h	Enable control. Writing a 1 to this bit enables the MDIO state machine, writing a 0 disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register.
29	RESERVED	NONE	0h	Reserved
28:24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel. This field specifies the highest useraccess channel that is available in the module and is currently set to 1. This implies that MDIOUserAccess1 is the highest available user access channel.
23:21	RESERVED	NONE	0h	Reserved
20	PREAMBLE	R/W	0h	Preamble disable. Writing a 1 to this bit disables this device from sending MDIO frame preambles in clause 22 mode of operation. This bit has no effect in clause 45 mode of operation.
19	FAULT	R/W	0h	Fault indicator. This bit is set to 1 if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1 to it clears this bit.
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable. This bit has to be set to 1 to enable the physical layer fault detection.
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable. This bit can be set to 1 to enable the host to set the userint and linkint bits for test purposes.

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Table 5-194. CPSW_MDIO_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	RESERVED	NONE	0h	Reserved
15:0	CLKDIV	R/W	FFh	Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. MDCLK is disabled when clkdiv is set to 0. MDCLK frequency = clk frequency/(clkdiv+1).

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5.2.2.12 CPSW_MDIO_ALIVE_REG Register

5.2.2.12.1 CPSW_MDIO_ALIVE_REG Register (Offset = F08h) [reset = 0h]

MDIO Alive Register

Return to Summary Table

Table 5-195. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F08h + formula

Figure 5-93. CPSW_MDIO_ALIVE_REG Name Register

31	30	29	28	27	26	25	24
ALIVE							
R/W							
0h							
23	22	21	20	19	18	17	16
ALIVE							
R/W							
0h							
15	14	13	12	11	10	9	8
ALIVE							
R/W							
0h							
7	6	5	4	3	2	1	0
ALIVE							
R/W							
0h							

Table 5-196. CPSW_MDIO_ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ALIVE	R/W	0h	MDIO Alive. Each of the 32 bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are intended to be used to give an indication of the presence or not of the PHY with the corresponding address. Writing a 1 to any bit will clear it, writing a 0 has no effect.

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5.2.2.13 CPSW_MDIO_LINK_REG Register

5.2.2.13.1 CPSW_MDIO_LINK_REG Register (Offset = F0Ch) [reset = 0h]

MDIO Link Register

Return to Summary Table

Table 5-197. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F0Ch + formula

Figure 5-94. CPSW_MDIO_LINK_REG Name Register

31	30	29	28	27	26	25	24
LINK							
R							
0h							
23	22	21	20	19	18	17	16
LINK							
R							
0h							
15	14	13	12	11	10	9	8
LINK							
R							
0h							
7	6	5	4	3	2	1	0
LINK							
R							
0h							

Table 5-198. CPSW_MDIO_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LINK	R	0h	MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The corresponding bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is cleared to zero if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, in Normal Mode Operation, the status of the two PHYs specified in the MDIOUserPhySel registers can be determined using the MLINK input pins. This is determined by the linksel bit in the MDIOUserPhySel register. In State Change Mode the MLINK input pins are unused.

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5.2.2.14 CPSW_MDIO_LINK_INT_RAW_REG Register

5.2.2.14.1 CPSW_MDIO_LINK_INT_RAW_REG Register (Offset = F10h) [reset = 0h]

MDIO Link Interrupt Raw Register

Return to Summary Table

Table 5-199. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F10h + formula

Figure 5-95. CPSW_MDIO_LINK_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTRAW	
NONE						R/W	
0h						0h	

Table 5-200. CPSW_MDIO_LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	LINKINTRAW	R/W	0h	MDIO link change event raw value. Normal mode operation: When asserted, a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register. linkintraw[0] and linkintraw[1] correspond to MDIOUserPhySel0 and MDIOUserPhysel1, respectively. Writing a 1 will clear the event and writing 0 has no effect. If the int_test bit in the MDIOControl register is set, the host may set linkintraw bits to a 1 which may be used for test purposes. MDIO link change event raw value. State Change Mode operation: The linkintraw[0] bit will be asserted when any bit (for any PHY) in the MDIOAlive or MDIOLink registers changes due to MDIO operations. The linkintraw[1] bit is unused in State Change Mode. State Change Mode allows any state change in any PHY to issue an interrupt. If the int_test bit in the MDIOControl register is set, the host may set the linkintraw[0] bit high which may be used for test purposes.

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5.2.2.15 CPSW_MDIO_LINK_INT_MASKED_REG Register

5.2.2.15.1 CPSW_MDIO_LINK_INT_MASKED_REG Register (Offset = F14h) [reset = 0h]

MDIO Link Interrupt Masked Register

Return to Summary Table

Table 5-201. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F14h + formula

Figure 5-96. CPSW_MDIO_LINK_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTMASKED	
NONE						R/W	
0h						0h	

Table 5-202. CPSW_MDIO_LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	LINKINTMASKED	R/W	0h	MDIO link change interrupt masked value. Normal mode operation: When asserted, a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register and the corresponding linkint_enable bit was set. linkintmasked[0] and linkintmasked[1] correspond to MDIOUserPhySel0 and MDIOUserPhysel1, respectively. Writing a 1 will clear the interrupt and writing 0 has no effect. These masked interrupt bits are the MDIO_LINKINT[1:0] pin values. MDIO link change interrupt masked value. State Change Mode operation: The linkintmasked[0] bit will be asserted when linkintraw[0] is asserted and when the linkintmaskset bit is set to 1. Writing a 1 will clear linkintmasked[0] (and the MDIO_LINKINT[0] output) and writing 0 has no effect. The linkintmasked[1] bit is not used in State Change Mode (MDIO_LINKINT[1] is therefore also unused in State Change Mode).

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5.2.2.16 CPSW_MDIO_LINK_INT_MASK_SET_REG Register

5.2.2.16.1 CPSW_MDIO_LINK_INT_MASK_SET_REG Register (Offset = F18h) [reset = 0h]

MDIO Link Interrupt Mask Set Register

Return to Summary Table

Table 5-203. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F18h + formula

Figure 5-97. CPSW_MDIO_LINK_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							LINKINTMASKSET
NONE							R/W
0h							0h

Table 5-204. CPSW_MDIO_LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINKINTMASKSET	R/W	0h	MDIO link interrupt mask set. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask set. State Change Mode Operation: Writing this bit to 1 will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when linkintraw[0] is asserted.

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5.2.2.17 CPSW_MDIO_LINK_INT_MASK_CLEAR_REG Register

5.2.2.17.1 CPSW_MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = F1Ch) [reset = 0h]

MDIO Link Interrupt Mask Clear Register

Return to Summary Table

Table 5-205. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F1Ch + formula

Figure 5-98. CPSW_MDIO_LINK_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK CLR
NONE							R/W
0h							0h

Table 5-206. CPSW_MDIO_LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	LINKINTMASKCLR	R/W	0h	MDIO link interrupt mask clear. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask clear. State Change Mode Operation: Writing this bit to 1 will disable the MDIO link status change interrupt (MDIO_LINKINT[0]) regardless of the linkintraw[0] bit value.

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5.2.2.18 CPSW_MDIO_USER_INT_RAW_REG Register

5.2.2.18.1 CPSW_MDIO_USER_INT_RAW_REG Register (Offset = F20h) [reset = 0h]

MDIO User Interrupt Raw Register

Return to Summary Table

Table 5-207. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F20h + formula

Figure 5-99. CPSW_MDIO_USER_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTRAW	
NONE						R/W	
0h						0h	

Table 5-208. CPSW_MDIO_USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTRAW	R/W	0h	Raw value of MDIO user command complete event for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted, a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed. Writing a 1 will clear the event and writing 0 has no effect. If the int_test bit in the MDIOControl register is set, the host may set the userintraw bits to a 1. This mode may be used for test purposes.

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5.2.2.19 CPSW_MDIO_USER_INT_MASKED_REG Register

5.2.2.19.1 CPSW_MDIO_USER_INT_MASKED_REG Register (Offset = F24h) [reset = 0h]

MDIO User Interrupt Masked Register

Return to Summary Table

Table 5-209. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F24h + formula

Figure 5-100. CPSW_MDIO_USER_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKED	
NONE						R/W	
0h						0h	

Table 5-210. CPSW_MDIO_USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKED	R/W	0h	Masked value of MDIO user command complete interrupt for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted, a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed and the corresponding userintmaskset bit is set to 1. Writing a 1 will clear the interrupt and writing 0 has no effect. If the int_test bit in the MDIOControl register is set, the host may set the userintmasked bits to a 1. This mode may be used for test purposes.

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5.2.2.20 CPSW_MDIO_USER_INT_MASK_SET_REG Register

5.2.2.20.1 CPSW_MDIO_USER_INT_MASK_SET_REG Register (Offset = F28h) [reset = 0h]

MDIO User Interrupt Mask Set Register

Return to Summary Table

Table 5-211. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F28h + formula

Figure 5-101. CPSW_MDIO_USER_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKSET	
NONE						R/W	
0h						0h	

Table 5-212. CPSW_MDIO_USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKSET	R/W	0h	MDIO user interrupt mask set for userintmasked[1:0], respectively. Writing a bit to 1 will enable MDIO user command complete interrupts for that particular MDIOUserAccess register. MDIO user interrupt for a particular MDIOUserAccess register is disabled if the corresponding bit is 0. Writing a 0 to this register has no effect.

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5.2.2.21 CPSW_MDIO_USER_INT_MASK_CLEAR_REG Register

5.2.2.21.1 CPSW_MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = F2Ch) [reset = 0h]

MDIO User Interrupt Mask Clear Register

Return to Summary Table

Table 5-213. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F2Ch + formula

Figure 5-102. CPSW_MDIO_USER_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKCLR	
NONE						R/W	
0h						0h	

Table 5-214. CPSW_MDIO_USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	USERINTMASKCLR	R/W	0h	MDIO user command complete interrupt mask clear for userintmasked[1:0], respectively. Writing a bit to 1 will disable further user command complete interrupts for that particular MDIOUserAccess register. Writing a 0 to this register has no effect.

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5.2.2.22 CPSW_MDIO_MANUAL_IF_REG Register

5.2.2.22.1 CPSW_MDIO_MANUAL_IF_REG Register (Offset = F30h) [reset = 0h]

MDIO Manual Interface Register

Return to Summary Table

Table 5-215. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F30h + formula

Figure 5-103. CPSW_MDIO_MANUAL_IF_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					MDIO_MDCLK_O	MDIO_OE	MDIO_PIN
NONE					R/W	R/W	R/W
0h					0h	0h	0h

Table 5-216. CPSW_MDIO_MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output - This value is the MDCLK_O output value when the manualmode bit is set in the MDIO_POLL_IPG register.
1	MDIO_OE	R/W	0h	MDIO Output Enable - This value is inverted and output on the MDIO_OE_N output when the manualmode bit is set in the MDIO_POLL_IPG register.
0	MDIO_PIN	R/W	0h	MDIO_Pin Value - This is the external MDIO data pin value when the manualmode bit is set in the MDIO_POLL_IPG register. That is, this value is driven on the MDIO_O (the MDIO serial data output) when MDIO_OE is asserted. The read value for this bit comes from MDIO_I (the MDIO serial data input). If MDIO_OE is asserted and MDIO_PIN is written with a 1 then MDIO_PIN should read a 1 if there are no external devices pulling the MDIO data line low.

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5.2.2.23 CPSW_MDIO_POLL_REG Register

5.2.2.23.1 CPSW_MDIO_POLL_REG Register (Offset = F34h) [reset = 0h]

MDIO Poll Register

Return to Summary Table

Table 5-217. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F34h + formula

Figure 5-104. CPSW_MDIO_POLL_REG Name Register

31	30	29	28	27	26	25	24
MANUALMODE	STATECHANGEMODE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPG							
R/W							
0h							

Table 5-218. CPSW_MDIO_POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	Polling Inter Packet Gap Value - This value is the number of MDCLK_O clocks between each poll when polling is enabled.
30	STATECHANGEMODE	R/W	0h	State Change Mode - When set, the MDIO is operating in State Change Mode. When clear, the MDIO is operating in normal mode. State change mode effects interrupt operations.
29:8	RESERVED	NONE	0h	Reserved
7:0	IPG	R/W	0h	Manual Mode - When set, the MDIO pins are directly controlled by software through the bits in the MDIOManual_IF register

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5.2.2.24 CPSW_MDIO_POLL_EN_REG Register

5.2.2.24.1 CPSW_MDIO_POLL_EN_REG Register (Offset = F38h) [reset = FFFFFFFFh]

MDIO Poll Enable Register

Return to Summary Table

Table 5-219. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F38h + formula

Figure 5-105. CPSW_MDIO_POLL_EN_REG Name Register

31	30	29	28	27	26	25	24
POLL_EN							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
POLL_EN							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
POLL_EN							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
POLL_EN							
R/W							
FFFFFFFFh							

Table 5-220. CPSW_MDIO_POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	POLL_EN	R/W	FFFFFFFFh	Poll Enable - When set, the bit indicates that the associated PHY will be included in polling operations. When clear, the associated PHY will not be polled. Each bit in this field is associated with a PHY. Bit zero is associated with PHY 0 and so on. Due to a limitation in the hardware, bit 31 must always be set, regardless of the value of the preamble disable bit in the MDIO_CONTROL register. However, there does not have to be a PHY at address 31.

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5.2.2.25 CPSW_MDIO_CLAUS45_REG Register

5.2.2.25.1 CPSW_MDIO_CLAUS45_REG Register (Offset = F3Ch) [reset = 0h]

MDIO Clause45 Register

Return to Summary Table

Table 5-221. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F3Ch + formula

Figure 5-106. CPSW_MDIO_CLAUS45_REG Name Register

31	30	29	28	27	26	25	24
CLAUSE45							
R/W							
0h							
23	22	21	20	19	18	17	16
CLAUSE45							
R/W							
0h							
15	14	13	12	11	10	9	8
CLAUSE45							
R/W							
0h							
7	6	5	4	3	2	1	0
CLAUSE45							
R/W							
0h							

Table 5-222. CPSW_MDIO_CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CLAUSE45	R/W	0h	MDIO clause 45 mode. When a clause45 bit is cleared, the PHY associated with the clause45 bit is operating in the clause 22 mode. When set, the PHY associated with the clause45 bit is operating in the clause 45 mode. Bit 0 is associated with PHY 0 and so on.

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5.2.2.26 CPSW_MDIO_USER_ADDR0_REG Register

5.2.2.26.1 CPSW_MDIO_USER_ADDR0_REG Register (Offset = F40h) [reset = 0h]

MDIO Address 0 Register

Return to Summary Table

Table 5-223. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F40h + formula

Figure 5-107. CPSW_MDIO_USER_ADDR0_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
USER_ADDR0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
USER_ADDR0							
R/W							
0h							

Table 5-224. CPSW_MDIO_USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	USER_ADDR0	R/W	0h	User Address 0 - In clause 45 mode, this field value is the address transferred in the address transfer inititated before each MDIOUserAccess0 access. This is not used for PHYs operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess0 access.

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5.2.2.27 CPSW_MDIO_USER_ADDR1_REG Register

5.2.2.27.1 CPSW_MDIO_USER_ADDR1_REG Register (Offset = F44h) [reset = 0h]

MDIO Address 1 Register

Return to Summary Table

Table 5-225. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F44h + formula

Figure 5-108. CPSW_MDIO_USER_ADDR1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
USER_ADDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
USER_ADDR1							
R/W							
0h							

Table 5-226. CPSW_MDIO_USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	USER_ADDR1	R/W	0h	User Address 1 - In clause 45 mode, this field value is the address transferred in the address transfer inititated before each MDIOUserAccess1 access. This is not used for PHYs operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess1 access.

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5.2.2.28 CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG Register

5.2.2.28.1 CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG Register (Offset = 1800h) [reset = 0h]

Core 0 THost Threshold Pulse Interrupt Enable Register

Return to Summary Table

Table 5-227. Instance Table

Instance Name	Physical Address
CPSW0	5280 1800h + formula

Figure 5-109. CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_THRESH_PULSE_EN							
R/W							
0h							

Table 5-228. CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_THRESH_PULSE_EN	R/W	0h	Core 0 THost Threshold Enable - Each bit in this register corresponds to the bit in the THost threshold interrupt that is enabled to generate an interrupt on C0_TH_THRESH_PULSE.

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5.2.2.29 CPSW_REGS_INT_SS_C0_TH_PULSE_EN_REG Register

5.2.2.29.1 CPSW_REGS_INT_SS_C0_TH_PULSE_EN_REG Register (Offset = 1804h) [reset = 0h]

Core 0 THost Pulse Interrupt Enable Register

Return to Summary Table

Table 5-229. Instance Table

Instance Name	Physical Address
CPSW0	5280 1804h + formula

Figure 5-110. CPSW_REGS_INT_SS_C0_TH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_PULSE_EN							
R/W							
0h							

Table 5-230. CPSW_REGS_INT_SS_C0_TH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_PULSE_EN	R/W	0h	Core 0 THost Enable - Each bit in this register corresponds to the bit in the THost interrupt that is enabled to generate an interrupt on C0_TH_PULSE.

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5.2.2.30 CPSW_REGS_INT_SS_C0_FH_PULSE_EN_REG Register

5.2.2.30.1 CPSW_REGS_INT_SS_C0_FH_PULSE_EN_REG Register (Offset = 1808h) [reset = 0h]

Core 0 FHost Pulse Interrupt Enable Register

Return to Summary Table

Table 5-231. Instance Table

Instance Name	Physical Address
CPSW0	5280 1808h + formula

Figure 5-111. CPSW_REGS_INT_SS_C0_FH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH_PULSE_EN							
R/W							
0h							

Table 5-232. CPSW_REGS_INT_SS_C0_FH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FH_PULSE_EN	R/W	0h	Core 0 FHost Interrupt Enable - Each bit in this register corresponds to the bit in the FHost interrupt that is enabled to generate an interrupt on C0_FH_PULSE.

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5.2.2.31 CPSW_REGS_INT_SS_C0_MISC_EN_REG Register

5.2.2.31.1 CPSW_REGS_INT_SS_C0_MISC_EN_REG Register (Offset = 180Ch) [reset = 0h]

Core 0 Misc Interrupt Enable Register

Return to Summary Table

Table 5-233. Instance Table

Instance Name	Physical Address
CPSW0	5280 180Ch + formula

Figure 5-112. CPSW_REGS_INT_SS_C0_MISC_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DED_PEND_EN	SEC_PEND_EN	EVNT_PEND_EN	STAT_PEND_EN	HOST_PEND_EN	MDIO_LINKINT_EN	MDIO_USERINT_EN
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-234. CPSW_REGS_INT_SS_C0_MISC_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	DED_PEND_EN	R/W	0h	Core 0 MISC DED Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C0_Misc_PULSE
5	SEC_PEND_EN	R/W	0h	Core 0 MISC SEC Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C0_Misc_PULSE
4	EVNT_PEND_EN	R/W	0h	Core 0 MISC CPTS Event Interrupt Enable - enabled to generate an interrupt on C0_Misc_PULSE
3	STAT_PEND_EN	R/W	0h	Core 0 MISC Statistics Interrupt Enable - Logical OR of all port statistics bits (bits n downto 0) - enabled to generate an interrupt on C0_Misc_PULSE
2	HOST_PEND_EN	R/W	0h	Core 0 MISC Host Interrupt Enable - enabled to generate an interrupt on C0_Misc_PULSE
1	MDIO_LINKINT_EN	R/W	0h	Core 0 MISC MDIO linkint - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C0_Misc_PULSE
0	MDIO_USERINT_EN	R/W	0h	Core 0 MISC_MDIO userint interrupt enable - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C0_Misc_PULSE

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5.2.2.32 CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG Register

5.2.2.32.1 CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG Register (Offset = 1810h) [reset = 0h]

THost Threshold Pulse Interrupt Status Register

Return to Summary Table

Table 5-235. Instance Table

Instance Name	Physical Address
CPSW0	5280 1810h + formula

Figure 5-113. CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_THRESH_PULSE_STATUS							
R							
0h							

Table 5-236. CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_THRESH_PULSE_STATUS	R	0h	Core 0 THost Threshold Masked Interrupt Status - Each bit in this read only register corresponds to the bit in the THost threshold interrupt that is enabled and generating an interrupt on C0_TH_THRESH_PULSE.

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5.2.2.33 CPSW_REGS_INT_SS_C0_TH_PULSE_STATUS_REG Register

5.2.2.33.1 CPSW_REGS_INT_SS_C0_TH_PULSE_STATUS_REG Register (Offset = 1814h) [reset = 0h]

THost Pulse Interrupt Status Register

Return to Summary Table

Table 5-237. Instance Table

Instance Name	Physical Address
CPSW0	5280 1814h + formula

Figure 5-114. CPSW_REGS_INT_SS_C0_TH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_PULSE_STATUS							
R							
0h							

Table 5-238. CPSW_REGS_INT_SS_C0_TH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_PULSE_STATUS	R	0h	Core 0 THost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Rx interrupt that is enabled and generating an interrupt on C0_TH_PULSE.

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5.2.2.34 CPSW_REGS_INT_SS_C0_FH_PULSE_STATUS_REG Register

5.2.2.34.1 CPSW_REGS_INT_SS_C0_FH_PULSE_STATUS_REG Register (Offset = 1818h) [reset = 0h]

FHost Pulse Interrupt Status Register

Return to Summary Table

Table 5-239. Instance Table

Instance Name	Physical Address
CPSW0	5280 1818h + formula

Figure 5-115. CPSW_REGS_INT_SS_C0_FH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH_PULSE_STATUS							
R							
0h							

Table 5-240. CPSW_REGS_INT_SS_C0_FH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FH_PULSE_STATUS	R	0h	Core 0 FHost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Tx interrupt that is enabled and generating an interrupt on C0_FH_PULSE .

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5.2.2.35 CPSW_REGS_INT_SS_C0_MISC_STATUS_REG Register

5.2.2.35.1 CPSW_REGS_INT_SS_C0_MISC_STATUS_REG Register (Offset = 181Ch) [reset = 0h]

Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

Return to Summary Table

Table 5-241. Instance Table

Instance Name	Physical Address
CPSW0	5280 181Ch + formula

Figure 5-116. CPSW_REGS_INT_SS_C0_MISC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DED_PEND	SEC_PEND	EVNT_PEND	STAT_PEND	HOST_PEND	MDIO_LINKINT	MDIO_USERINT
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-242. CPSW_REGS_INT_SS_C0_MISC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	DED_PEND	R/W	0h	Core 0 MISC DED Memory Protect Error Interrupt
5	SEC_PEND	R/W	0h	Core 0 MISC SEC Memory Protect Error Interrupt
4	EVNT_PEND	R/W	0h	Core 0 MISC CPTS Event Interrupt
3	STAT_PEND	R/W	0h	Core 0 MISC Statistics Interrupt - Logical OR of bits n downto 0
2	HOST_PEND	R/W	0h	Core 0 MISC Host Interrupt Enable
1	MDIO_LINKINT	R/W	0h	Core 0 MISC MDIO linkint - Logical OR of bits 1 and 0
0	MDIO_USERINT	R/W	0h	Core 0 MISC_MDIO userint interrupt - Logical OR of bits 1 and 0

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5.2.2.36 CPSW_REGS_INT_SS_C0_TH_IMAX_REG Register

5.2.2.36.1 CPSW_REGS_INT_SS_C0_TH_IMAX_REG Register (Offset = 1820h) [reset = 0h]

Core 0 THost Interrupt Max Register Register

Return to Summary Table

Table 5-243. Instance Table

Instance Name	Physical Address
CPSW0	5280 1820h + formula

Figure 5-117. CPSW_REGS_INT_SS_C0_TH_IMAX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		TH_IMAX					
NONE		R/W					
0h		0h					

Table 5-244. CPSW_REGS_INT_SS_C0_TH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	TH_IMAX	R/W	0h	Core 0 THost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C0_TH_PULSE if pacing is enabled for this interrupt.

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5.2.2.37 CPSW_REGS_INT_SS_C0_FH_IMAX_REG Register

5.2.2.37.1 CPSW_REGS_INT_SS_C0_FH_IMAX_REG Register (Offset = 1824h) [reset = 0h]

Core 0 FHost Interrupt Max Register Register

Return to Summary Table

Table 5-245. Instance Table

Instance Name	Physical Address
CPSW0	5280 1824h + formula

Figure 5-118. CPSW_REGS_INT_SS_C0_FH_IMAX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		FH_IMAX					
NONE		R/W					
0h		0h					

Table 5-246. CPSW_REGS_INT_SS_C0_FH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	FH_IMAX	R/W	0h	Core 0 FHost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C0_FH_PULSE if pacing is enabled for this interrupt.

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5.2.2.38 CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG Register

5.2.2.38.1 CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG Register (Offset = 1840h) [reset = 0h]

Core 1 THost Threshold Pulse Interrupt Enable Register

Return to Summary Table

Table 5-247. Instance Table

Instance Name	Physical Address
CPSW0	5280 1840h + formula

Figure 5-119. CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_THRESH_PULSE_EN							
R/W							
0h							

Table 5-248. CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_THRESH_PULSE_EN	R/W	0h	Core 1 THost Threshold Enable - Each bit in this register corresponds to the bit in the THost threshold interrupt that is enabled to generate an interrupt on C1_TH_THRESH_PULSE.

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5.2.2.39 CPSW_REGS_INT_SS_C1_TH_PULSE_EN_REG Register

5.2.2.39.1 CPSW_REGS_INT_SS_C1_TH_PULSE_EN_REG Register (Offset = 1844h) [reset = 0h]

Core 1 THost Pulse Interrupt Enable Register

Return to Summary Table

Table 5-249. Instance Table

Instance Name	Physical Address
CPSW0	5280 1844h + formula

Figure 5-120. CPSW_REGS_INT_SS_C1_TH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_PULSE_EN							
R/W							
0h							

Table 5-250. CPSW_REGS_INT_SS_C1_TH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_PULSE_EN	R/W	0h	Core 1 THost Enable - Each bit in this register corresponds to the bit in the THost interrupt that is enabled to generate an interrupt on C1_TH_PULSE.

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5.2.2.40 CPSW_REGS_INT_SS_C1_FH_PULSE_EN_REG Register

5.2.2.40.1 CPSW_REGS_INT_SS_C1_FH_PULSE_EN_REG Register (Offset = 1848h) [reset = 0h]

Core 1 FHost Pulse Interrupt Enable Register

Return to Summary Table

Table 5-251. Instance Table

Instance Name	Physical Address
CPSW0	5280 1848h + formula

Figure 5-121. CPSW_REGS_INT_SS_C1_FH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH_PULSE_EN							
R/W							
0h							

Table 5-252. CPSW_REGS_INT_SS_C1_FH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FH_PULSE_EN	R/W	0h	Core 1 FHost Interrupt Enable - Each bit in this register corresponds to the bit in the FHost interrupt that is enabled to generate an interrupt on C1_FH_PULSE.

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5.2.2.41 CPSW_REGS_INT_SS_C1_MISC_EN_REG Register

5.2.2.41.1 CPSW_REGS_INT_SS_C1_MISC_EN_REG Register (Offset = 184Ch) [reset = 0h]

Core 1 Misc Interrupt Enable Register

Return to Summary Table

Table 5-253. Instance Table

Instance Name	Physical Address
CPSW0	5280 184Ch + formula

Figure 5-122. CPSW_REGS_INT_SS_C1_MISC_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DED_PEND_EN	SEC_PEND_EN	EVNT_PEND_EN	STAT_PEND_EN	HOST_PEND_EN	MDIO_LINKINT_EN	MDIO_USERINT_EN
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-254. CPSW_REGS_INT_SS_C1_MISC_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	DED_PEND_EN	R/W	0h	Core 1 MISC DED Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C1_Misc_PULSE
5	SEC_PEND_EN	R/W	0h	Core 1 MISC SEC Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C1_Misc_PULSE
4	EVNT_PEND_EN	R/W	0h	Core 1 MISC CPTS Event Interrupt Enable - enabled to generate an interrupt on C1_Misc_PULSE
3	STAT_PEND_EN	R/W	0h	Core 1 MISC Statistics Interrupt Enable - Logical OR of all port statistics bits (bits n downto 0) - enabled to generate an interrupt on C1_Misc_PULSE
2	HOST_PEND_EN	R/W	0h	Core 1 MISC Host Interrupt Enable - enabled to generate an interrupt on C1_Misc_PULSE
1	MDIO_LINKINT_EN	R/W	0h	Core 1 MISC MDIO linkint - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C1_Misc_PULSE
0	MDIO_USERINT_EN	R/W	0h	Core 1 MISC_MDIO userint interrupt enable - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C1_Misc_PULSE

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5.2.2.42 CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG Register

5.2.2.42.1 CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG Register (Offset = 1850h) [reset = 0h]

THost Threshold Pulse Interrupt Status Register

Return to Summary Table

Table 5-255. Instance Table

Instance Name	Physical Address
CPSW0	5280 1850h + formula

Figure 5-123. CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_THRESH_PULSE_STATUS							
R							
0h							

Table 5-256. CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_THRESH_PULSE_STATUS	R	0h	Core 1 THost Threshold Masked Interrupt Status - Each bit in this read only register corresponds to the bit in the THost threshold interrupt that is enabled and generating an interrupt on C1_TH_THRESH_PULSE.

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5.2.2.43 CPSW_REGS_INT_SS_C1_TH_PULSE_STATUS_REG Register

5.2.2.43.1 CPSW_REGS_INT_SS_C1_TH_PULSE_STATUS_REG Register (Offset = 1854h) [reset = 0h]

THost Pulse Interrupt Status Register

Return to Summary Table

Table 5-257. Instance Table

Instance Name	Physical Address
CPSW0	5280 1854h + formula

Figure 5-124. CPSW_REGS_INT_SS_C1_TH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_PULSE_STATUS							
R							
0h							

Table 5-258. CPSW_REGS_INT_SS_C1_TH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_PULSE_STATUS	R	0h	Core 1 THost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Rx interrupt that is enabled and generating an interrupt on C1_TH_PULSE.

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5.2.2.44 CPSW_REGS_INT_SS_C1_FH_PULSE_STATUS_REG Register

5.2.2.44.1 CPSW_REGS_INT_SS_C1_FH_PULSE_STATUS_REG Register (Offset = 1858h) [reset = 0h]

FHost Pulse Interrupt Status Register

Return to Summary Table

Table 5-259. Instance Table

Instance Name	Physical Address
CPSW0	5280 1858h + formula

Figure 5-125. CPSW_REGS_INT_SS_C1_FH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH_PULSE_STATUS							
R							
0h							

Table 5-260. CPSW_REGS_INT_SS_C1_FH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FH_PULSE_STATUS	R	0h	Core 1 FHost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Tx interrupt that is enabled and generating an interrupt on C1_FH_PULSE .

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5.2.2.45 CPSW_REGS_INT_SS_C1_MISC_STATUS_REG Register

5.2.2.45.1 CPSW_REGS_INT_SS_C1_MISC_STATUS_REG Register (Offset = 185Ch) [reset = 0h]

Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

Return to Summary Table

Table 5-261. Instance Table

Instance Name	Physical Address
CPSW0	5280 185Ch + formula

Figure 5-126. CPSW_REGS_INT_SS_C1_MISC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DED_PEND	SEC_PEND	EVNT_PEND	STAT_PEND	HOST_PEND	MDIO_LINKINT	MDIO_USERINT
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-262. CPSW_REGS_INT_SS_C1_MISC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	DED_PEND	R/W	0h	Core 1 MISC DED Memory Protect Error Interrupt
5	SEC_PEND	R/W	0h	Core 1 MISC SEC Memory Protect Error Interrupt
4	EVNT_PEND	R/W	0h	Core 1 MISC CPTS Event Interrupt
3	STAT_PEND	R/W	0h	Core 1 MISC Statistics Interrupt - Logical OR of bits n downto 0
2	HOST_PEND	R/W	0h	Core 1 MISC Host Interrupt Enable
1	MDIO_LINKINT	R/W	0h	Core 1 MISC MDIO linkint - Logical OR of bits 1 and 0
0	MDIO_USERINT	R/W	0h	Core 1 MISC_MDIO userint interrupt - Logical OR of bits 1 and 0

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5.2.2.46 CPSW_REGS_INT_SS_C1_TH_IMAX_REG Register

5.2.2.46.1 CPSW_REGS_INT_SS_C1_TH_IMAX_REG Register (Offset = 1860h) [reset = 0h]

Core 1 THost Interrupt Max Register Register

Return to Summary Table

Table 5-263. Instance Table

Instance Name	Physical Address
CPSW0	5280 1860h + formula

Figure 5-127. CPSW_REGS_INT_SS_C1_TH_IMAX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		TH_IMAX					
NONE		R/W					
0h		0h					

Table 5-264. CPSW_REGS_INT_SS_C1_TH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	TH_IMAX	R/W	0h	Core 1 THost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C1_TH_PULSE if pacing is enabled for this interrupt.

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5.2.2.47 CPSW_REGS_INT_SS_C1_FH_IMAX_REG Register

5.2.2.47.1 CPSW_REGS_INT_SS_C1_FH_IMAX_REG Register (Offset = 1864h) [reset = 0h]

Core 1 FHost Interrupt Max Register Register

Return to Summary Table

Table 5-265. Instance Table

Instance Name	Physical Address
CPSW0	5280 1864h + formula

Figure 5-128. CPSW_REGS_INT_SS_C1_FH_IMAX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		FH_IMAX					
NONE		R/W					
0h		0h					

Table 5-266. CPSW_REGS_INT_SS_C1_FH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	FH_IMAX	R/W	0h	Core 1 FHost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C1_FH_PULSE if pacing is enabled for this interrupt.

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5.2.2.48 CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG Register

5.2.2.48.1 CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG Register (Offset = 1880h) [reset = 0h]

Core 2 THost Threshold Pulse Interrupt Enable Register

Return to Summary Table

Table 5-267. Instance Table

Instance Name	Physical Address
CPSW0	5280 1880h + formula

Figure 5-129. CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_THRESH_PULSE_EN							
R/W							
0h							

Table 5-268. CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_THRESH_PULSE_EN	R/W	0h	Core 2 THost Threshold Enable - Each bit in this register corresponds to the bit in the THost threshold interrupt that is enabled to generate an interrupt on C2_TH_THRESH_PULSE.

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5.2.2.49 CPSW_REGS_INT_SS_C2_TH_PULSE_EN_REG Register

5.2.2.49.1 CPSW_REGS_INT_SS_C2_TH_PULSE_EN_REG Register (Offset = 1884h) [reset = 0h]

Core 2 THost Pulse Interrupt Enable Register

Return to Summary Table

Table 5-269. Instance Table

Instance Name	Physical Address
CPSW0	5280 1884h + formula

Figure 5-130. CPSW_REGS_INT_SS_C2_TH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_PULSE_EN							
R/W							
0h							

Table 5-270. CPSW_REGS_INT_SS_C2_TH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_PULSE_EN	R/W	0h	Core 2 THost Enable - Each bit in this register corresponds to the bit in the THost interrupt that is enabled to generate an interrupt on C2_TH_PULSE.

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5.2.2.50 CPSW_REGS_INT_SS_C2_FH_PULSE_EN_REG Register

5.2.2.50.1 CPSW_REGS_INT_SS_C2_FH_PULSE_EN_REG Register (Offset = 1888h) [reset = 0h]

Core 2 FHost Pulse Interrupt Enable Register

Return to Summary Table

Table 5-271. Instance Table

Instance Name	Physical Address
CPSW0	5280 1888h + formula

Figure 5-131. CPSW_REGS_INT_SS_C2_FH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH_PULSE_EN							
R/W							
0h							

Table 5-272. CPSW_REGS_INT_SS_C2_FH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FH_PULSE_EN	R/W	0h	Core 2 FHost Interrupt Enable - Each bit in this register corresponds to the bit in the FHost interrupt that is enabled to generate an interrupt on C2_FH_PULSE.

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5.2.2.51 CPSW_REGS_INT_SS_C2_MISC_EN_REG Register

5.2.2.51.1 CPSW_REGS_INT_SS_C2_MISC_EN_REG Register (Offset = 188Ch) [reset = 0h]

Core 2 Misc Interrupt Enable Register

Return to Summary Table

Table 5-273. Instance Table

Instance Name	Physical Address
CPSW0	5280 188Ch + formula

Figure 5-132. CPSW_REGS_INT_SS_C2_MISC_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	DED_PEND_EN	SEC_PEND_EN	EVNT_PEND_EN	STAT_PEND_EN	HOST_PEND_EN	MDIO_LINKINT_EN	MDIO_USERINT_EN
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-274. CPSW_REGS_INT_SS_C2_MISC_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	DED_PEND_EN	R/W	0h	Core 2 MISC DED Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C2_Misc_PULSE
5	SEC_PEND_EN	R/W	0h	Core 2 MISC SEC Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C2_Misc_PULSE
4	EVNT_PEND_EN	R/W	0h	Core 2 MISC CPTS Event Interrupt Enable - enabled to generate an interrupt on C2_Misc_PULSE
3	STAT_PEND_EN	R/W	0h	Core 2 MISC Statistics Interrupt Enable - Logical OR of all port statistics bits (bits n downto 0) - enabled to generate an interrupt on C2_Misc_PULSE
2	HOST_PEND_EN	R/W	0h	Core 2 MISC Host Interrupt Enable - enabled to generate an interrupt on C2_Misc_PULSE
1	MDIO_LINKINT_EN	R/W	0h	Core 2 MISC MDIO linkint - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C2_Misc_PULSE
0	MDIO_USERINT_EN	R/W	0h	Core 2 MISC_MDIO userint interrupt enable - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C2_Misc_PULSE

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5.2.2.52 CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG Register

5.2.2.52.1 CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG Register (Offset = 1890h) [reset = 0h]

THost Threshold Pulse Interrupt Status Register

Return to Summary Table

Table 5-275. Instance Table

Instance Name	Physical Address
CPSW0	5280 1890h + formula

Figure 5-133. CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_THRESH_PULSE_STATUS							
R							
0h							

Table 5-276. CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_THRESH_PULSE_STATUS	R	0h	Core 2 THost Threshold Masked Interrupt Status - Each bit in this read only register corresponds to the bit in the THost threshold interrupt that is enabled and generating an interrupt on C2_TH_THRESH_PULSE.

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5.2.2.53 CPSW_REGS_INT_SS_C2_TH_PULSE_STATUS_REG Register

5.2.2.53.1 CPSW_REGS_INT_SS_C2_TH_PULSE_STATUS_REG Register (Offset = 1894h) [reset = 0h]

THost Pulse Interrupt Status Register

Return to Summary Table

Table 5-277. Instance Table

Instance Name	Physical Address
CPSW0	5280 1894h + formula

Figure 5-134. CPSW_REGS_INT_SS_C2_TH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_PULSE_STATUS							
R							
0h							

Table 5-278. CPSW_REGS_INT_SS_C2_TH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_PULSE_STATUS	R	0h	Core 2 THost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Rx interrupt that is enabled and generating an interrupt on C2_TH_PULSE.

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5.2.2.54 CPSW_REGS_INT_SS_C2_FH_PULSE_STATUS_REG Register

5.2.2.54.1 CPSW_REGS_INT_SS_C2_FH_PULSE_STATUS_REG Register (Offset = 1898h) [reset = 0h]

FHost Pulse Interrupt Status Register

Return to Summary Table

Table 5-279. Instance Table

Instance Name	Physical Address
CPSW0	5280 1898h + formula

Figure 5-135. CPSW_REGS_INT_SS_C2_FH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH_PULSE_STATUS							
R							
0h							

Table 5-280. CPSW_REGS_INT_SS_C2_FH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FH_PULSE_STATUS	R	0h	Core 2 FHost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Tx interrupt that is enabled and generating an interrupt on C2_FH_PULSE .

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5.2.2.55 CPSW_REGS_INT_SS_C2_MISC_STATUS_REG Register

5.2.2.55.1 CPSW_REGS_INT_SS_C2_MISC_STATUS_REG Register (Offset = 189Ch) [reset = 0h]

Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

Return to Summary Table

Table 5-281. Instance Table

Instance Name	Physical Address
CPSW0	5280 189Ch + formula

Figure 5-136. CPSW_REGS_INT_SS_C2_MISC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DED_PEND	SEC_PEND	EVNT_PEND	STAT_PEND	HOST_PEND	MDIO_LINKINT	MDIO_USERINT
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-282. CPSW_REGS_INT_SS_C2_MISC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	DED_PEND	R/W	0h	Core 2 MISC DED Memory Protect Error Interrupt
5	SEC_PEND	R/W	0h	Core 2 MISC SEC Memory Protect Error Interrupt
4	EVNT_PEND	R/W	0h	Core 2 MISC CPTS Event Interrupt
3	STAT_PEND	R/W	0h	Core 2 MISC Statistics Interrupt - Logical OR of bits n downto 0
2	HOST_PEND	R/W	0h	Core 2 MISC Host Interrupt Enable
1	MDIO_LINKINT	R/W	0h	Core 2 MISC MDIO linkint - Logical OR of bits 1 and 0
0	MDIO_USERINT	R/W	0h	Core 2 MISC_MDIO userint interrupt - Logical OR of bits 1 and 0

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5.2.2.56 CPSW_REGS_INT_SS_C2_TH_IMAX_REG Register

5.2.2.56.1 CPSW_REGS_INT_SS_C2_TH_IMAX_REG Register (Offset = 18A0h) [reset = 0h]

Core 2 THost Interrupt Max Register Register

Return to Summary Table

Table 5-283. Instance Table

Instance Name	Physical Address
CPSW0	5280 18A0h + formula

Figure 5-137. CPSW_REGS_INT_SS_C2_TH_IMAX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		TH_IMAX					
NONE		R/W					
0h		0h					

Table 5-284. CPSW_REGS_INT_SS_C2_TH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	TH_IMAX	R/W	0h	Core 2 THost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C2_TH_PULSE if pacing is enabled for this interrupt.

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5.2.2.57 CPSW_REGS_INT_SS_C2_FH_IMAX_REG Register

5.2.2.57.1 CPSW_REGS_INT_SS_C2_FH_IMAX_REG Register (Offset = 18A4h) [reset = 0h]

Core 2 FHost Interrupt Max Register Register

Return to Summary Table

Table 5-285. Instance Table

Instance Name	Physical Address
CPSW0	5280 18A4h + formula

Figure 5-138. CPSW_REGS_INT_SS_C2_FH_IMAX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		FH_IMAX					
NONE		R/W					
0h		0h					

Table 5-286. CPSW_REGS_INT_SS_C2_FH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	FH_IMAX	R/W	0h	Core 2 FHost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C2_FH_PULSE if pacing is enabled for this interrupt.

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5.2.2.58 CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG Register

5.2.2.58.1 CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG Register (Offset = 18C0h) [reset = 0h]

Core 3 THost Threshold Pulse Interrupt Enable Register

Return to Summary Table

Table 5-287. Instance Table

Instance Name	Physical Address
CPSW0	5280 18C0h + formula

Figure 5-139. CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_THRESH_PULSE_EN							
R/W							
0h							

Table 5-288. CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_THRESH_PULSE_EN	R/W	0h	Core 3 THost Threshold Enable - Each bit in this register corresponds to the bit in the THost threshold interrupt that is enabled to generate an interrupt on C3_TH_THRESH_PULSE.

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5.2.2.59 CPSW_REGS_INT_SS_C3_TH_PULSE_EN_REG Register

5.2.2.59.1 CPSW_REGS_INT_SS_C3_TH_PULSE_EN_REG Register (Offset = 18C4h) [reset = 0h]

Core 3 THost Pulse Interrupt Enable Register

Return to Summary Table

Table 5-289. Instance Table

Instance Name	Physical Address
CPSW0	5280 18C4h + formula

Figure 5-140. CPSW_REGS_INT_SS_C3_TH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_PULSE_EN							
R/W							
0h							

Table 5-290. CPSW_REGS_INT_SS_C3_TH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_PULSE_EN	R/W	0h	Core 3 THost Enable - Each bit in this register corresponds to the bit in the THost interrupt that is enabled to generate an interrupt on C3_TH_PULSE.

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5.2.2.60 CPSW_REGS_INT_SS_C3_FH_PULSE_EN_REG Register

5.2.2.60.1 CPSW_REGS_INT_SS_C3_FH_PULSE_EN_REG Register (Offset = 18C8h) [reset = 0h]

Core 3 FHost Pulse Interrupt Enable Register

Return to Summary Table

Table 5-291. Instance Table

Instance Name	Physical Address
CPSW0	5280 18C8h + formula

Figure 5-141. CPSW_REGS_INT_SS_C3_FH_PULSE_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH_PULSE_EN							
R/W							
0h							

Table 5-292. CPSW_REGS_INT_SS_C3_FH_PULSE_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FH_PULSE_EN	R/W	0h	Core 3 FHost Interrupt Enable - Each bit in this register corresponds to the bit in the FHost interrupt that is enabled to generate an interrupt on C3_FH_PULSE.

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5.2.2.61 CPSW_REGS_INT_SS_C3_MISC_EN_REG Register

5.2.2.61.1 CPSW_REGS_INT_SS_C3_MISC_EN_REG Register (Offset = 18CCh) [reset = 0h]

Core 3 Misc Interrupt Enable Register

Return to Summary Table

Table 5-293. Instance Table

Instance Name	Physical Address
CPSW0	5280 18CCh + formula

Figure 5-142. CPSW_REGS_INT_SS_C3_MISC_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DED_PEND_EN	SEC_PEND_EN	EVNT_PEND_EN	STAT_PEND_EN	HOST_PEND_EN	MDIO_LINKINT_EN	MDIO_USERINT_EN
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-294. CPSW_REGS_INT_SS_C3_MISC_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	DED_PEND_EN	R/W	0h	Core 3 MISC DED Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C3_Misc_PULSE
5	SEC_PEND_EN	R/W	0h	Core 3 MISC SEC Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C3_Misc_PULSE
4	EVNT_PEND_EN	R/W	0h	Core 3 MISC CPTS Event Interrupt Enable - enabled to generate an interrupt on C3_Misc_PULSE
3	STAT_PEND_EN	R/W	0h	Core 3 MISC Statistics Interrupt Enable - Logical OR of all port statistics bits (bits n downto 0) - enabled to generate an interrupt on C3_Misc_PULSE
2	HOST_PEND_EN	R/W	0h	Core 3 MISC Host Interrupt Enable - enabled to generate an interrupt on C3_Misc_PULSE
1	MDIO_LINKINT_EN	R/W	0h	Core 3 MISC MDIO linkint - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C3_Misc_PULSE
0	MDIO_USERINT_EN	R/W	0h	Core 3 MISC_MDIO userint interrupt enable - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C3_Misc_PULSE

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5.2.2.62 CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG Register

5.2.2.62.1 CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG Register (Offset = 18D0h) [reset = 0h]

THost Threshold Pulse Interrupt Status Register

Return to Summary Table

Table 5-295. Instance Table

Instance Name	Physical Address
CPSW0	5280 18D0h + formula

Figure 5-143. CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_THRESH_PULSE_STATUS							
R							
0h							

Table 5-296. CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_THRESH_PULSE_STATUS	R	0h	Core 3 THost Threshold Masked Interrupt Status - Each bit in this read only register corresponds to the bit in the THost threshold interrupt that is enabled and generating an interrupt on C3_TH_THRESH_PULSE.

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5.2.2.63 CPSW_REGS_INT_SS_C3_TH_PULSE_STATUS_REG Register

5.2.2.63.1 CPSW_REGS_INT_SS_C3_TH_PULSE_STATUS_REG Register (Offset = 18D4h) [reset = 0h]

THost Pulse Interrupt Status Register

Return to Summary Table

Table 5-297. Instance Table

Instance Name	Physical Address
CPSW0	5280 18D4h + formula

Figure 5-144. CPSW_REGS_INT_SS_C3_TH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_PULSE_STATUS							
R							
0h							

Table 5-298. CPSW_REGS_INT_SS_C3_TH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_PULSE_STATUS	R	0h	Core 3 THost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Rx interrupt that is enabled and generating an interrupt on C3_TH_PULSE.

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5.2.2.64 CPSW_REGS_INT_SS_C3_FH_PULSE_STATUS_REG Register

5.2.2.64.1 CPSW_REGS_INT_SS_C3_FH_PULSE_STATUS_REG Register (Offset = 18D8h) [reset = 0h]

FHost Pulse Interrupt Status Register

Return to Summary Table

Table 5-299. Instance Table

Instance Name	Physical Address
CPSW0	5280 18D8h + formula

Figure 5-145. CPSW_REGS_INT_SS_C3_FH_PULSE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH_PULSE_STATUS							
R							
0h							

Table 5-300. CPSW_REGS_INT_SS_C3_FH_PULSE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FH_PULSE_STATUS	R	0h	Core 3 FHost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Tx interrupt that is enabled and generating an interrupt on C3_FH_PULSE .

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5.2.2.65 CPSW_REGS_INT_SS_C3_MISC_STATUS_REG Register

5.2.2.65.1 CPSW_REGS_INT_SS_C3_MISC_STATUS_REG Register (Offset = 18DCh) [reset = 0h]

Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

Return to Summary Table

Table 5-301. Instance Table

Instance Name	Physical Address
CPSW0	5280 18DCh + formula

Figure 5-146. CPSW_REGS_INT_SS_C3_MISC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	DED_PEND	SEC_PEND	EVNT_PEND	STAT_PEND	HOST_PEND	MDIO_LINKINT	MDIO_USERINT
NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-302. CPSW_REGS_INT_SS_C3_MISC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	DED_PEND	R/W	0h	Core 3 MISC DED Memory Protect Error Interrupt
5	SEC_PEND	R/W	0h	Core 3 MISC SEC Memory Protect Error Interrupt
4	EVNT_PEND	R/W	0h	Core 3 MISC CPTS Event Interrupt
3	STAT_PEND	R/W	0h	Core 3 MISC Statistics Interrupt - Logical OR of bits n downto 0
2	HOST_PEND	R/W	0h	Core 3 MISC Host Interrupt Enable
1	MDIO_LINKINT	R/W	0h	Core 3 MISC MDIO linkint - Logical OR of bits 1 and 0
0	MDIO_USERINT	R/W	0h	Core 3 MISC_MDIO userint interrupt - Logical OR of bits 1 and 0

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5.2.2.66 CPSW_REGS_INT_SS_C3_TH_IMAX_REG Register

5.2.2.66.1 CPSW_REGS_INT_SS_C3_TH_IMAX_REG Register (Offset = 18E0h) [reset = 0h]

Core 3 THost Interrupt Max Register Register

Return to Summary Table

Table 5-303. Instance Table

Instance Name	Physical Address
CPSW0	5280 18E0h + formula

Figure 5-147. CPSW_REGS_INT_SS_C3_TH_IMAX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		TH_IMAX					
NONE		R/W					
0h		0h					

Table 5-304. CPSW_REGS_INT_SS_C3_TH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	TH_IMAX	R/W	0h	Core 3 THost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C3_TH_PULSE if pacing is enabled for this interrupt.

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5.2.2.67 CPSW_REGS_INT_SS_C3_FH_IMAX_REG Register

5.2.2.67.1 CPSW_REGS_INT_SS_C3_FH_IMAX_REG Register (Offset = 18E4h) [reset = 0h]

Core 3 FHost Interrupt Max Register Register

Return to Summary Table

Table 5-305. Instance Table

Instance Name	Physical Address
CPSW0	5280 18E4h + formula

Figure 5-148. CPSW_REGS_INT_SS_C3_FH_IMAX_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		FH_IMAX					
NONE		R/W					
0h		0h					

Table 5-306. CPSW_REGS_INT_SS_C3_FH_IMAX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5:0	FH_IMAX	R/W	0h	Core 3 FHost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C3_FH_PULSE if pacing is enabled for this interrupt.

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5.2.2.68 CPSW_NC_VER_REG Register

5.2.2.68.1 CPSW_NC_VER_REG Register (Offset = 20000h) [reset = 6B903103h]

CPSW ID Version

Return to Summary Table

Table 5-307. Instance Table

Instance Name	Physical Address
CPSW0	5282 0000h + formula

Figure 5-149. CPSW_NC_VER_REG Name Register

31	30	29	28	27	26	25	24
IDENT							
R							
6B90h							
23	22	21	20	19	18	17	16
IDENT							
R							
6B90h							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_VER		
R					R		
6h					1h		
7	6	5	4	3	2	1	0
MINOR_VER							
R							
3h							

Table 5-308. CPSW_NC_VER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	6B90h	Identification Value
15:11	RTL_VER	R	6h	RTL Version Value
10:8	MAJOR_VER	R	1h	Major Version Value
7:0	MINOR_VER	R	3h	Minor Version Value

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5.2.2.69 CPSW_NC_CONTROL_REG Register

5.2.2.69.1 CPSW_NC_CONTROL_REG Register (Offset = 20004h) [reset = 0h]

CPSW Switch Control

Return to Summary Table

Table 5-309. Instance Table

Instance Name	Physical Address
CPSW0	5282 0004h + formula

Figure 5-150. CPSW_NC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
ECC_CRC_MODE	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					EST_ENABLE	RESERVED	EEE_ENABLE
NONE					R/W	R/W	R/W
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
P0_FH_PASS_CRC_ERR	P0_FH_PAD	P0_TH_CRC_REMOVE	RESERVED	P8_PASS_PRI_TAGGED	P7_PASS_PRI_TAGGED	P6_PASS_PRI_TAGGED	P5_PASS_PRI_TAGGED
R/W	R/W	R/W	NONE	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
P4_PASS_PRI_TAGGED	P3_PASS_PRI_TAGGED	P2_PASS_PRI_TAGGED	P1_PASS_PRI_TAGGED	P0_PASS_PRI_TAGGED	P0_ENABLE	VLAN_AWARE	S_CN_SWITCH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-310. CPSW_NC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_CRC_MODE	R/W	0h	ECC CRC Mode - 0 - ECC errors induced through the ECC aggregator flip bits in the packet headers (not in packet data). 1 - ECC errors induced through the ECC aggregator flip bits in the packet data (not in the packet headers).
30:19	RESERVED	NONE	0h	Reserved
18	EST_ENABLE	R/W	0h	Enhanced Scheduled Traffic enable (EST) - 0 - EST is disabled. 1 - EST is enabled
17	RESERVED	R/W	0h	RESERVED
16	EEE_ENABLE	R/W	0h	Energy Efficient Ethernet enable - 0 - Energy Efficient Ethernet is disabled. 1 - Energy Efficient Ethernet is enabled.
15	P0_FH_PASS_CRC_ERR	R/W	0h	Port 0 Pass Received CRC errors - 0 - Packets received with CRC errors on port 0 are dropped. 1 - Packets received with CRC errors on port 0 are transferred to the destination ports.
14	P0_FH_PAD	R/W	0h	Port 0 Receive Short Packet Pad - 0 - short packets are dropped. 1 - short packets are padded to 64-bytes (with pad and added CRC) if the CRC is not passed in. Short packets are dropped if the CRC is passed (in the Info0 word).

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Table 5-310. CPSW_NC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	P0_TH_CRC_REMOVE	R/W	0h	Port 0 Transmit CRC remove - 0 - Do not remove the CRC on Port 0 THost (egress) packets. 1 - Remove the CRC on all Port 0 THost (egress) packets.
12	RESERVED	NONE	0h	Reserved
11	P8_PASS_PRI_TAGGED	R/W	0h	Port 8 Pass Priority Tagged - 0 - Priority tagged packets have the zero VID replaced with the input port Enet_P8_PORT_VLAN[11:0] on ingress. 1 - Priority tagged packets are processed unchanged.
10	P7_PASS_PRI_TAGGED	R/W	0h	Port 7 Pass Priority Tagged - 0 - Priority tagged packets have the zero VID replaced with the input port Enet_P7_PORT_VLAN[11:0] on ingress. 1 - Priority tagged packets are processed unchanged.
9	P6_PASS_PRI_TAGGED	R/W	0h	Port 6 Pass Priority Tagged - 0 - Priority tagged packets have the zero VID replaced with the input port Enet_P6_PORT_VLAN[11:0] on ingress. 1 - Priority tagged packets are processed unchanged.
8	P5_PASS_PRI_TAGGED	R/W	0h	Port 5 Pass Priority Tagged - 0 - Priority tagged packets have the zero VID replaced with the input port Enet_P5_PORT_VLAN[11:0] on ingress. 1 - Priority tagged packets are processed unchanged.
7	P4_PASS_PRI_TAGGED	R/W	0h	Port 4 Pass Priority Tagged - 0 - Priority tagged packets have the zero VID replaced with the input port Enet_P4_PORT_VLAN[11:0] on ingress. 1 - Priority tagged packets are processed unchanged.
6	P3_PASS_PRI_TAGGED	R/W	0h	Port 3 Pass Priority Tagged - 0 - Priority tagged packets have the zero VID replaced with the input port Enet_P3_PORT_VLAN[11:0] on ingress. 1 - Priority tagged packets are processed unchanged.
5	P2_PASS_PRI_TAGGED	R/W	0h	Port 2 Pass Priority Tagged - 0 - Priority tagged packets have the zero VID replaced with the input port Enet_P2_PORT_VLAN[11:0] on ingress. 1 - Priority tagged packets are processed unchanged.
4	P1_PASS_PRI_TAGGED	R/W	0h	Port 1 Pass Priority Tagged - 0 - Priority tagged packets have the zero VID replaced with the input port Enet_P1_PORT_VLAN[11:0] on ingress. 1 - Priority tagged packets are processed unchanged.
3	P0_PASS_PRI_TAGGED	R/W	0h	Port 0 Pass Priority Tagged - 0 - Priority tagged packets have the zero VID replaced with the input port Enet_P0_PORT_VLAN[11:0] on ingress. 1 - Priority tagged packets are processed unchanged.
2	P0_ENABLE	R/W	0h	Port 0 Enable - 0 - Port 0 is disabled 1 - Port 0 is enabled
1	VLAN_AWARE	R/W	0h	VLAN Aware Mode - 0 - CPSW_NU is in the VLAN unaware mode. 1 - CPSW_NU is in the VLAN aware mode.
0	S_CN_SWITCH	R/W	0h	Service or Customer VLAN switch. 0 - Customer switch. VLAN processing uses the inner_vlan_ltype. 1 - Service switch. VLAN processing uses the outer_vlan_ltype.

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5.2.2.70 CPSW_NC_STATUS_REG Register

5.2.2.70.1 CPSW_NC_STATUS_REG Register (Offset = 2000Ch) [reset = 1h]

CPSW Status

Return to Summary Table

Table 5-311. Instance Table

Instance Name	Physical Address
CPSW0	5282 000Ch + formula

Figure 5-151. CPSW_NC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							CPPI_IDLE
NONE							R
0h							1h

Table 5-312. CPSW_NC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	CPPI_IDLE	R	1h	CPPI Idle - Indicates when set that the CPPI port transmit and receive are idle.

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5.2.2.71 CPSW_NC_EM_CONTROL_REG Register

5.2.2.71.1 CPSW_NC_EM_CONTROL_REG Register (Offset = 20010h) [reset = 0h]

CPSW Emulation Control

Return to Summary Table

Table 5-313. Instance Table

Instance Name	Physical Address
CPSW0	5282 0010h + formula

Figure 5-152. CPSW_NC_EM_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 5-314. CPSW_NC_EM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

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5.2.2.72 CPSW_NC_STAT_PORT_EN_REG Register

5.2.2.72.1 CPSW_NC_STAT_PORT_EN_REG Register (Offset = 20014h) [reset = 0h]

CPSW Statistics Port Enable

Return to Summary Table

Table 5-315. Instance Table

Instance Name	Physical Address
CPSW0	5282 0014h + formula

Figure 5-153. CPSW_NC_STAT_PORT_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							P8_STAT_EN
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
P7_STAT_EN	P6_STAT_EN	P5_STAT_EN	P4_STAT_EN	P3_STAT_EN	P2_STAT_EN	P1_STAT_EN	P0_STAT_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-316. CPSW_NC_STAT_PORT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	P8_STAT_EN	R/W	0h	Port 8 Statistics Enable 0 - Statistics are disabled for the port. 1 - Statistics are enabled for the port.
7	P7_STAT_EN	R/W	0h	Port 7 Statistics Enable 0 - Statistics are disabled for the port. 1 - Statistics are enabled for the port.
6	P6_STAT_EN	R/W	0h	Port 6 Statistics Enable 0 - Statistics are disabled for the port. 1 - Statistics are enabled for the port.
5	P5_STAT_EN	R/W	0h	Port 5 Statistics Enable 0 - Statistics are disabled for the port. 1 - Statistics are enabled for the port.
4	P4_STAT_EN	R/W	0h	Port 4 Statistics Enable 0 - Statistics are disabled for the port. 1 - Statistics are enabled for the port.
3	P3_STAT_EN	R/W	0h	Port 3 Statistics Enable 0 - Statistics are disabled for the port. 1 - Statistics are enabled for the port.
2	P2_STAT_EN	R/W	0h	Port 2 Statistics Enable 0 - Statistics are disabled for the port. 1 - Statistics are enabled for the port.
1	P1_STAT_EN	R/W	0h	Port 1 Statistics Enable 0 - Statistics are disabled for the port. 1 - Statistics are enabled for the port.

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Table 5-316. CPSW_NC_STAT_PORT_EN_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	P0_STAT_EN	R/W	0h	Port 0 Statistics Enable 0 - Statistics are disabled for the port. 1 - Statistics are enabled for the port.

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5.2.2.73 CPSW_NC_PTYPE_REG Register

5.2.2.73.1 CPSW_NC_PTYPE_REG Register (Offset = 20018h) [reset = 0h]

CPSW Transmit Priority Type

Return to Summary Table

Table 5-317. Instance Table

Instance Name	Physical Address
CPSW0	5282 0018h + formula

Figure 5-154. CPSW_NC_PTYPE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							P8_PTYPE_ESC
NONE							R/W
0h							0h

15	14	13	12	11	10	9	8
P7_PTYPE_ESC	P6_PTYPE_ESC	P5_PTYPE_ESC	P4_PTYPE_ESC	P3_PTYPE_ESC	P2_PTYPE_ESC	P1_PTYPE_ESC	P0_PTYPE_ESC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

7	6	5	4	3	2	1	0
RESERVED			ESC_PRI_LD_VAL				
NONE			R/W				
0h			0h				

Table 5-318. CPSW_NC_PTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	P8_PTYPE_ESC	R/W	0h	Port 8 Priority Type Escalate - 0 - Priority Type Fixed. 1 - Priority Type Escalate
15	P7_PTYPE_ESC	R/W	0h	Port 7 Priority Type Escalate - 0 - Priority Type Fixed. 1 - Priority Type Escalate
14	P6_PTYPE_ESC	R/W	0h	Port 6 Priority Type Escalate - 0 - Priority Type Fixed. 1 - Priority Type Escalate
13	P5_PTYPE_ESC	R/W	0h	Port 5 Priority Type Escalate - 0 - Priority Type Fixed. 1 - Priority Type Escalate
12	P4_PTYPE_ESC	R/W	0h	Port 4 Priority Type Escalate - 0 - Priority Type Fixed. 1 - Priority Type Escalate
11	P3_PTYPE_ESC	R/W	0h	Port 3 Priority Type Escalate - 0 - Priority Type Fixed. 1 - Priority Type Escalate
10	P2_PTYPE_ESC	R/W	0h	Port 2 Priority Type Escalate - 0 - Priority Type Fixed. 1 - Priority Type Escalate

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Table 5-318. CPSW_NC_PTYPE_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	P1_PTYPE_ESC	R/W	0h	Port 1 Priority Type Escalate - 0 - Priority Type Fixed. 1 - Priority Type Escalate
8	P0_PTYPE_ESC	R/W	0h	Port 0 Priority Type Escalate - 0 - Priority Type Fixed. 1 - Priority Type Escalate
7:5	RESERVED	NONE	0h	Reserved
4:0	ESC_PRI_LD_VAL	R/W	0h	Escalate Priority Load Value - When a port is in escalate priority, this is the number of higher priority packets sent before the next lower priority is allowed to send a packet. Escalate priority allows lower priority packets to be sent at a fixed rate relative to the next higher priority. The min value of esc_pri_ld_val = 2.

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5.2.2.74 CPSW_NC_SOFT_IDLE_REG Register

5.2.2.74.1 CPSW_NC_SOFT_IDLE_REG Register (Offset = 2001Ch) [reset = 0h]

CPSW Software Idle

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Table 5-319. Instance Table

Instance Name	Physical Address
CPSW0	5282 001Ch + formula

Figure 5-155. CPSW_NC_SOFT_IDLE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_IDLE
NONE							R/W
0h							0h

Table 5-320. CPSW_NC_SOFT_IDLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_IDLE	R/W	0h	Software Idle - 0 - Software idle not commanded. 1 - Command CPSW software idle. When set, port 0 packet DMA operations stop at the next packet boundary.

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5.2.2.75 CPSW_NC_THRU_RATE_REG Register

5.2.2.75.1 CPSW_NC_THRU_RATE_REG Register (Offset = 20020h) [reset = 3001h]

CPSW Thru Rate

Return to Summary Table

Table 5-321. Instance Table

Instance Name	Physical Address
CPSW0	5282 0020h + formula

Figure 5-156. CPSW_NC_THRU_RATE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SL_RX_THRU_RATE				RESERVED			
R/W				NONE			
3h				0h			
7	6	5	4	3	2	1	0
RESERVED				P0_FH_THRU_RATE			
NONE				R/W			
0h				1h			

Table 5-322. CPSW_NC_THRU_RATE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	SL_RX_THRU_RATE	R/W	3h	This is not a field intended to be changed by software
11:4	RESERVED	NONE	0h	Reserved
3:0	P0_FH_THRU_RATE	R/W	1h	This is not a field intended to be changed by software

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5.2.2.76 CPSW_NC_GAP_THRESH_REG Register

5.2.2.76.1 CPSW_NC_GAP_THRESH_REG Register (Offset = 20024h) [reset = Bh]

CPSW Transmit FIFO Short Gap Threshold

Return to Summary Table

Table 5-323. Instance Table

Instance Name	Physical Address
CPSW0	5282 0024h + formula

Figure 5-157. CPSW_NC_GAP_THRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			GAP_THRESH				
NONE			R/W				
0h			Bh				

Table 5-324. CPSW_NC_GAP_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	GAP_THRESH	R/W	Bh	Ethernet Port Short Gap Threshold - This is the Ethernet port associated FIFO transmit block usage value for triggering transmit short gap (when short gap is enabled).

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5.2.2.77 CPSW_NC_EEE_PRESCALE_REG Register

5.2.2.77.1 CPSW_NC_EEE_PRESCALE_REG Register (Offset = 2002Ch) [reset = 0h]

CPSW Energy Efficient Ethernet Prescale Value

Return to Summary Table

Table 5-325. Instance Table

Instance Name	Physical Address
CPSW0	5282 002Ch + formula

Figure 5-158. CPSW_NC_EEE_PRESCALE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				EEE_PRESCALE			
NONE				R/W			
0h				0h			
7	6	5	4	3	2	1	0
EEE_PRESCALE							
R/W							
0h							

Table 5-326. CPSW_NC_EEE_PRESCALE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	EEE_PRESCALE	R/W	0h	Energy Efficient Ethernet Prescale count load value - This value is loaded into the EEE pre-scale counter each time the pre-scale count decrements to zero. The EEE counters are enabled to decrement each time the pre-scale counter reaches zero (and the EEE counters are enabled to count time). If this value is zero then the EEE counters decrement on every clock. If this value is 0x001 then the counters decrement on every other clock (and so on).

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5.2.2.78 CPSW_NC_TX_G_OFLOW_THRESH_SET_REG Register

5.2.2.78.1 CPSW_NC_TX_G_OFLOW_THRESH_SET_REG Register (Offset = 20030h) [reset = FFFFFFFFh]

CPSW PFC Tx Global Out Flow Threshold Set

Return to Summary Table

Table 5-327. Instance Table

Instance Name	Physical Address
CPSW0	5282 0030h + formula

Figure 5-159. CPSW_NC_TX_G_OFLOW_THRESH_SET_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
Fh				Fh			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI5				PRI4			
R/W				R/W			
Fh				Fh			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI3				PRI2			
R/W				R/W			
Fh				Fh			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI1				PRI0			
R/W				R/W			
Fh				Fh			

Table 5-328. CPSW_NC_TX_G_OFLOW_THRESH_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27:24	PRI6	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23:20	PRI5	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19:16	PRI4	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15:12	PRI3	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11:8	PRI2	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7:4	PRI1	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3:0	PRI0	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

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5.2.2.79 CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG Register

5.2.2.79.1 CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG Register (Offset = 20034h) [reset = 0h]

CPSW PFC Tx Global Out Flow Threshold Clear

Return to Summary Table

Table 5-329. Instance Table

Instance Name	Physical Address
CPSW0	5282 0034h + formula

Figure 5-160. CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
0h				0h			

Table 5-330. CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27:24	PRI6	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23:20	PRI5	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19:16	PRI4	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15:12	PRI3	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11:8	PRI2	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7:4	PRI1	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3:0	PRI0	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

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5.2.2.80 CPSW_NC_TX_G_BUF_THRESH_SET_L_REG Register

5.2.2.80.1 CPSW_NC_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 20038h) [reset = FFFFFFFFh]

CPSW PFC Global Tx Buffer Threshold Set Low

Return to Summary Table

Table 5-331. Instance Table

Instance Name	Physical Address
CPSW0	5282 0038h + formula

Figure 5-161. CPSW_NC_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
PRI3							
R/W							
FFh							
23	22	21	20	19	18	17	16
PRI2							
R/W							
FFh							
15	14	13	12	11	10	9	8
PRI1							
R/W							
FFh							
7	6	5	4	3	2	1	0
PRI0							
R/W							
FFh							

Table 5-332. CPSW_NC_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI3	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23:16	PRI2	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15:8	PRI1	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7:0	PRI0	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

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5.2.2.81 CPSW_NC_TX_G_BUF_THRESH_SET_H_REG Register

5.2.2.81.1 CPSW_NC_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 2003Ch) [reset = FFFFFFFFh]

CPSW PFC Global Tx Buffer Threshold Set High

Return to Summary Table

Table 5-333. Instance Table

Instance Name	Physical Address
CPSW0	5282 003Ch + formula

Figure 5-162. CPSW_NC_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
PRI7							
R/W							
FFh							
23	22	21	20	19	18	17	16
PRI6							
R/W							
FFh							
15	14	13	12	11	10	9	8
PRI5							
R/W							
FFh							
7	6	5	4	3	2	1	0
PRI4							
R/W							
FFh							

Table 5-334. CPSW_NC_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI7	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23:16	PRI6	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15:8	PRI5	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7:0	PRI4	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

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5.2.2.82 CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG Register

5.2.2.82.1 CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 20040h) [reset = 0h]

CPSW PFC Global Tx Buffer Threshold Clear Low

Return to Summary Table

Table 5-335. Instance Table

Instance Name	Physical Address
CPSW0	5282 0040h + formula

Figure 5-163. CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
PRI3							
R/W							
0h							
23	22	21	20	19	18	17	16
PRI2							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI1							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI0							
R/W							
0h							

Table 5-336. CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI3	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23:16	PRI2	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15:8	PRI1	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7:0	PRI0	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

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5.2.2.83 CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG Register

5.2.2.83.1 CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 20044h) [reset = 0h]

CPSW PFC Global Tx Buffer Threshold Clear High

Return to Summary Table

Table 5-337. Instance Table

Instance Name	Physical Address
CPSW0	5282 0044h + formula

Figure 5-164. CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
PRI7							
R/W							
0h							
23	22	21	20	19	18	17	16
PRI6							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI5							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI4							
R/W							
0h							

Table 5-338. CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PRI7	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23:16	PRI6	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15:8	PRI5	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7:0	PRI4	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

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5.2.2.84 CPSW_NC_VLAN_LTYPE_REG Register

5.2.2.84.1 CPSW_NC_VLAN_LTYPE_REG Register (Offset = 20050h) [reset = 88A88100h]

VLAN Length/type

Return to Summary Table

Table 5-339. Instance Table

Instance Name	Physical Address
CPSW0	5282 0050h + formula

Figure 5-165. CPSW_NC_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24
VLAN_LTYPE_OUTER							
R/W							
88A8h							
23	22	21	20	19	18	17	16
VLAN_LTYPE_OUTER							
R/W							
88A8h							
15	14	13	12	11	10	9	8
VLAN_LTYPE_INNER							
R/W							
8100h							
7	6	5	4	3	2	1	0
VLAN_LTYPE_INNER							
R/W							
8100h							

Table 5-340. CPSW_NC_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	VLAN_LTYPE_OUTER	R/W	88A8h	Outer VLAN LType
15:0	VLAN_LTYPE_INNER	R/W	8100h	Inner VLAN LType

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5.2.2.85 CPSW_NC_EST_TS_DOMAIN_REG Register

5.2.2.85.1 CPSW_NC_EST_TS_DOMAIN_REG Register (Offset = 20054h) [reset = 0h]

Enhanced Scheduled Traffic Host Event Domain

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Table 5-341. Instance Table

Instance Name	Physical Address
CPSW0	5282 0054h + formula

Figure 5-166. CPSW_NC_EST_TS_DOMAIN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EST_TS_DOMAIN							
R/W							
0h							

Table 5-342. CPSW_NC_EST_TS_DOMAIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EST_TS_DOMAIN	R/W	0h	Enhanced Scheduled Traffic domain. This value is used as the domain in the CPTS event to indicate that the event came from EST.

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5.2.2.86 CPSW_NC_TX_PRI0_MAXLEN_REG Register

5.2.2.86.1 CPSW_NC_TX_PRI0_MAXLEN_REG Register (Offset = 20100h) [reset = 7E8h]

Transmit Priority 0 Maximum Length

Return to Summary Table

Table 5-343. Instance Table

Instance Name	Physical Address
CPSW0	5282 0100h + formula

Figure 5-167. CPSW_NC_TX_PRI0_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI0_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI0_MAXLEN							
R/W							
7E8h							

Table 5-344. CPSW_NC_TX_PRI0_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI0_MAXLEN	R/W	7E8h	This value determines the maximum packet length that will be transmitted on priority 0 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped.

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5.2.2.87 CPSW_NC_TX_PRI1_MAXLEN_REG Register

5.2.2.87.1 CPSW_NC_TX_PRI1_MAXLEN_REG Register (Offset = 20104h) [reset = 7E8h]

Transmit Priority 1 Maximum Length

Return to Summary Table

Table 5-345. Instance Table

Instance Name	Physical Address
CPSW0	5282 0104h + formula

Figure 5-168. CPSW_NC_TX_PRI1_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI1_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI1_MAXLEN							
R/W							
7E8h							

Table 5-346. CPSW_NC_TX_PRI1_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI1_MAXLEN	R/W	7E8h	This value determines the maximum packet length that will be transmitted on priority 1 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped.

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5.2.2.88 CPSW_NC_TX_PRI2_MAXLEN_REG Register

5.2.2.88.1 CPSW_NC_TX_PRI2_MAXLEN_REG Register (Offset = 20108h) [reset = 7E8h]

Transmit Priority 2 Maximum Length

Return to Summary Table

Table 5-347. Instance Table

Instance Name	Physical Address
CPSW0	5282 0108h + formula

Figure 5-169. CPSW_NC_TX_PRI2_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI2_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI2_MAXLEN							
R/W							
7E8h							

Table 5-348. CPSW_NC_TX_PRI2_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI2_MAXLEN	R/W	7E8h	This value determines the maximum packet length that will be transmitted on priority 2 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped.

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5.2.2.89 CPSW_NC_TX_PRI3_MAXLEN_REG Register

5.2.2.89.1 CPSW_NC_TX_PRI3_MAXLEN_REG Register (Offset = 2010Ch) [reset = 7E8h]

Transmit Priority 3 Maximum Length

Return to Summary Table

Table 5-349. Instance Table

Instance Name	Physical Address
CPSW0	5282 010Ch + formula

Figure 5-170. CPSW_NC_TX_PRI3_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI3_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI3_MAXLEN							
R/W							
7E8h							

Table 5-350. CPSW_NC_TX_PRI3_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI3_MAXLEN	R/W	7E8h	This value determines the maximum packet length that will be transmitted on priority 3 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped.

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5.2.2.90 CPSW_NC_TX_PRI4_MAXLEN_REG Register

5.2.2.90.1 CPSW_NC_TX_PRI4_MAXLEN_REG Register (Offset = 20110h) [reset = 7E8h]

Transmit Priority 4 Maximum Length

Return to Summary Table

Table 5-351. Instance Table

Instance Name	Physical Address
CPSW0	5282 0110h + formula

Figure 5-171. CPSW_NC_TX_PRI4_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI4_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI4_MAXLEN							
R/W							
7E8h							

Table 5-352. CPSW_NC_TX_PRI4_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI4_MAXLEN	R/W	7E8h	This value determines the maximum packet length that will be transmitted on priority 4 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped.

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5.2.2.91 CPSW_NC_TX_PRI5_MAXLEN_REG Register

5.2.2.91.1 CPSW_NC_TX_PRI5_MAXLEN_REG Register (Offset = 20114h) [reset = 7E8h]

Transmit Priority 5 Maximum Length

Return to Summary Table

Table 5-353. Instance Table

Instance Name	Physical Address
CPSW0	5282 0114h + formula

Figure 5-172. CPSW_NC_TX_PRI5_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI5_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI5_MAXLEN							
R/W							
7E8h							

Table 5-354. CPSW_NC_TX_PRI5_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI5_MAXLEN	R/W	7E8h	This value determines the maximum packet length that will be transmitted on priority 5 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped.

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5.2.2.92 CPSW_NC_TX_PRI6_MAXLEN_REG Register

5.2.2.92.1 CPSW_NC_TX_PRI6_MAXLEN_REG Register (Offset = 20118h) [reset = 7E8h]

Transmit Priority 6 Maximum Length

Return to Summary Table

Table 5-355. Instance Table

Instance Name	Physical Address
CPSW0	5282 0118h + formula

Figure 5-173. CPSW_NC_TX_PRI6_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		TX_PRI6_MAXLEN					
NONE		R/W					
0h		7E8h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI6_MAXLEN							
R/W							
7E8h							

Table 5-356. CPSW_NC_TX_PRI6_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI6_MAXLEN	R/W	7E8h	This value determines the maximum packet length that will be transmitted on priority 6 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped.

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5.2.2.93 CPSW_NC_TX_PRI7_MAXLEN_REG Register

5.2.2.93.1 CPSW_NC_TX_PRI7_MAXLEN_REG Register (Offset = 2011Ch) [reset = 7E8h]

Transmit Priority 7 Maximum Length

Return to Summary Table

Table 5-357. Instance Table

Instance Name	Physical Address
CPSW0	5282 011Ch + formula

Figure 5-174. CPSW_NC_TX_PRI7_MAXLEN_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">TX_PRI7_MAXLEN</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">7E8h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">TX_PRI7_MAXLEN</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">7E8h</td></tr>
</table>

Table 5-358. CPSW_NC_TX_PRI7_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	TX_PRI7_MAXLEN	R/W	7E8h	This value determines the maximum packet length that will be transmitted on priority 7 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped.

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5.2.2.94 CPSW_MDIO_USER_GROUP_USER_ACCESS_REG_J Register

5.2.2.94.1 CPSW_MDIO_USER_GROUP_USER_ACCESS_REG_J Register (Offset = F80h) [reset = 0h]

MDIO User Access Register

Return to Summary Table

Table 5-359. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F80h + formula

Figure 5-175. CPSW_MDIO_USER_GROUP_USER_ACCESS_REG_j Name Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W	R/W	R/W	NONE			R/W	
0h	0h	0h	0h			0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
REGADR			PHYADR				
R/W			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DATA							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA							
R/W							
0h							

Table 5-360. CPSW_MDIO_USER_GROUP_USER_ACCESS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W	0h	Go. Writing a 1 to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0 to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1. If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28:26	RESERVED	NONE	0h	Reserved
25:21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in clause 45 mode.
20:16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.
15:0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

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5.2.2.95 CPSW_MDIO_USER_GROUP_USER_PHY_SEL_REG_J Register

5.2.2.95.1 CPSW_MDIO_USER_GROUP_USER_PHY_SEL_REG_J Register (Offset = F84h) [reset = 0h]

MDIO User PHY Select Register

Return to Summary Table

Table 5-361. Instance Table

Instance Name	Physical Address
CPSW0	5280 0F84h + formula

Figure 5-176. CPSW_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W	R/W	NONE	R/W				
0h	0h	0h	0h				

Table 5-362. CPSW_MDIO_USER_GROUP_USER_PHY_SEL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	LINKSEL	R/W	0h	Link status determination select. Set to 1 to determine link status using the MLINK pin. Default value is 0 which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1 to enable link change status interrupts for PHY address specified in phyadr_mon. Link change interrupts are disabled if this bit is set to 0.
5	RESERVED	NONE	0h	Reserved
4:0	PHYADR_MON	R/W	0h	PHY address whose link status is to be monitored.

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5.2.2.96 CPSW_NC_CPPI_P0_CONTROL_REG Register

5.2.2.96.1 CPSW_NC_CPPI_P0_CONTROL_REG Register (Offset = 21004h) [reset = 0h]

CPPI Port 0 Control

Return to Summary Table

Table 5-363. Instance Table

Instance Name	Physical Address
CPSW0	5282 1004h + formula

Figure 5-177. CPSW_NC_CPPI_P0_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					FH_REMAP_DSCP_V6	FH_REMAP_DSCP_V4	FH_REMAP_VLAN
NONE					R/W	R/W	R/W
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FH_ECC_ERR_EN	TH_ECC_ERR_EN	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				TH_CHECKSUM_EN	FH_DSCP_IPV6_EN	FH_DSCP_IPV4_EN	FH_CHECKSUM_EN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 5-364. CPSW_NC_CPPI_P0_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	FH_REMAP_DSCP_V6	R/W	0h	Port 0 FHost (ingress) remap priority to DSCP IPV6 priority (see packet priority handling section for details). 0 - Hardware switch priority IPV6 DSCP priority remapping is disabled. 1 - Hardware switch priority IPV6 DSCP priority remapping is enabled.
17	FH_REMAP_DSCP_V4	R/W	0h	Port 0 FHost (ingress) remap priority to DSCP IPV4 priority (see packet priority handling section for details). 0 - Hardware switch priority IPV4 DSCP priority remapping is disabled. 1 - Hardware switch priority IPV4 DSCP priority remapping is enabled.
16	FH_REMAP_VLAN	R/W	0h	Port 0 receive (ingress) remap priority to VLAN. See priority remapping section for details.
15	FH_ECC_ERR_EN	R/W	0h	Port 0 FHost ECC Error Enable. This bit must be set to enable FHost ECC error operations
14	TH_ECC_ERR_EN	R/W	0h	Port 0 THost ECC Error Enable. This bit must be set to enable THost ECC error operations.
13:4	RESERVED	NONE	0h	Reserved

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Table 5-364. CPSW_NC_CPPI_P0_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TH_CHECKSUM_EN	R/W	0h	Port 0 THost (egress) Checksum Enable 0 - THost checksum is disabled. 1 - THost checksum is enabled. IPV4/V6 Packets have checksum information (4-bytes) included at the end of the packet data when the chksum_encap descriptor bit is set in the EOP THost buffer descriptor.
2	FH_DSCP_IPV6_EN	R/W	0h	Port 0 FHost IPv6 DSCP enable 0 - Ipv6 DSCP priority mapping is disabled. 1 - Ipv6 DSCP priority mapping is enabled.
1	FH_DSCP_IPV4_EN	R/W	0h	Port 0 FHost IPv4 DSCP enable 0 - Ipv4 DSCP priority mapping is disabled. 1 - Ipv4 DSCP priority mapping is enabled.
0	FH_CHECKSUM_EN	R/W	0h	Port 0 FHost (port 0 ingress) Checksum Enable 0 - FHost checksum is disabled. 1 - FHost checksum is enabled. Four bytes of checksum information can be included at the start of the packet data to be used for checksum packet processing when chksum_encap is set in the SOP FHost buffer descriptor.

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5.2.2.97 CPSW_NC_CPPI_P0_BLK_CNT_REG Register

5.2.2.97.1 CPSW_NC_CPPI_P0_BLK_CNT_REG Register (Offset = 21010h) [reset = 1h]

CPPI Port 0 FIFO Block Usage Count

Return to Summary Table

Table 5-365. Instance Table

Instance Name	Physical Address
CPSW0	5282 1010h + formula

Figure 5-178. CPSW_NC_CPPI_P0_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED			TH_BLK_CNT				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED		FH_BLK_CNT					
NONE		R					
0h		1h					

Table 5-366. CPSW_NC_CPPI_P0_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED	NONE	0h	Reserved
12:8	TH_BLK_CNT	R	0h	Port 0 Transmit Block Count Usage - This value is the number of blocks allocated to the FIFO logical transmit queues. note: for N=2 this field is always zero (no transmit FIFO).
7:6	RESERVED	NONE	0h	Reserved
5:0	FH_BLK_CNT	R	1h	Port 0 Receive Block Count Usage - This value is the number of blocks allocated in the receive FIFO.

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5.2.2.98 CPSW_NC_CPPI_P0_PORT_VLAN_REG Register

5.2.2.98.1 CPSW_NC_CPPI_P0_PORT_VLAN_REG Register (Offset = 21014h) [reset = 0h]

CPPI Port 0 VLAN

Return to Summary Table

Table 5-367. Instance Table

Instance Name	Physical Address
CPSW0	5282 1014h + formula

Figure 5-179. CPSW_NC_CPPI_P0_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PORT_PRI			PORT_CFI	PORT_VID			
R/W			R/W	R/W			
0h			0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PORT_VID							
R/W							
0h							

Table 5-368. CPSW_NC_CPPI_P0_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

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5.2.2.99 CPSW_NC_CPPI_P0_TH_PRI_MAP_REG Register

5.2.2.99.1 CPSW_NC_CPPI_P0_TH_PRI_MAP_REG Register (Offset = 21018h) [reset = 76543210h]

CPPI Port 0 Tx Header Pri to Switch Pri Mapping

Return to Summary Table

Table 5-369. Instance Table

Instance Name	Physical Address
CPSW0	5282 1018h + formula

Figure 5-180. CPSW_NC_CPPI_P0_TH_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 5-370. CPSW_NC_CPPI_P0_TH_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7 - A packet header priority of 0x7 is given this switch queue priority.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6 - A packet header priority of 0x7 is given this switch queue priority.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5 - A packet header priority of 0x7 is given this switch queue priority.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4 - A packet header priority of 0x7 is given this switch queue priority.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3 - A packet header priority of 0x7 is given this switch queue priority.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2 - A packet header priority of 0x7 is given this switch queue priority.
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	1h	Priority 1 - A packet header priority of 0x7 is given this switch queue priority.
3	RESERVED	NONE	0h	Reserved

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Table 5-370. CPSW_NC_CPPI_P0_TH_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PRI0	R/W	0h	Priority 0 - A packet header priority of 0x7 is given this switch queue priority.

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5.2.2.100 CPSW_NC_CPPI_P0_PRI_CTL_REG Register

5.2.2.100.1 CPSW_NC_CPPI_P0_PRI_CTL_REG Register (Offset = 2101Ch) [reset = 0h]

CPPI Port 0 Priority Control

Return to Summary Table

Table 5-371. Instance Table

Instance Name	Physical Address
CPSW0	5282 101Ch + formula

Figure 5-181. CPSW_NC_CPPI_P0_PRI_CTL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
FH_FLOW_PRI							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED							FH_PTYPE
NONE							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-372. CPSW_NC_CPPI_P0_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	FH_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority). Note: for N=2 this field should remain zero.
15:9	RESERVED	NONE	0h	Reserved
8	FH_PTYPE	R/W	0h	Receive Priority Type
7:0	RESERVED	NONE	0h	Reserved

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5.2.2.101 CPSW_NC_CPPI_P0_FH_PRI_MAP_REG Register

5.2.2.101.1 CPSW_NC_CPPI_P0_FH_PRI_MAP_REG Register (Offset = 21020h) [reset = 76543210h]

CPPI Port 0 RX Pkt Pri to Header Pri Map

Return to Summary Table

Table 5-373. Instance Table

Instance Name	Physical Address
CPSW0	5282 1020h + formula

Figure 5-182. CPSW_NC_CPPI_P0_FH_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 5-374. CPSW_NC_CPPI_P0_FH_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7 - A packet priority of 0x7 is mapped (changed) to this header packet priority.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6 - A packet priority of 0x6 is mapped (changed) to this header packet priority.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5 - A packet priority of 0x5 is mapped (changed) to this header packet priority.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4 - A packet priority of 0x4 is mapped (changed) to this header packet priority.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3 - A packet priority of 0x3 is mapped (changed) to this header packet priority.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2 - A packet priority of 0x2 is mapped (changed) to this header packet priority.
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	1h	Priority 1 - A packet priority of 0x1 is mapped (changed) to this header packet priority.
3	RESERVED	NONE	0h	Reserved

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Table 5-374. CPSW_NC_CPPI_P0_FH_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PRI0	R/W	0h	Priority 0 - A packet priority of 0x0 is mapped (changed) to this header packet priority.

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5.2.2.102 CPSW_NC_CPPI_P0_FH_MAXLEN_REG Register

5.2.2.102.1 CPSW_NC_CPPI_P0_FH_MAXLEN_REG Register (Offset = 21024h) [reset = 5EEh]

CPPI Port 0 Receive Frame Max Length

Return to Summary Table

Table 5-375. Instance Table

Instance Name	Physical Address
CPSW0	5282 1024h + formula

Figure 5-183. CPSW_NC_CPPI_P0_FH_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		FH_MAXLEN					
NONE		R/W					
0h		5EEh					
7	6	5	4	3	2	1	0
FH_MAXLEN							
R/W							
5EEh							

Table 5-376. CPSW_NC_CPPI_P0_FH_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	FH_MAXLEN	R/W	5EEh	Port 0 Ingress Maximum Frame Length - This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than p0_fh_maxlen are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN) when the CPSW is configured with 1 = 4. When 1 = 1 the maximum value is 2024 (including VLAN).

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5.2.2.103 CPSW_NC_CPPI_P0_TH_BLKS_PRI_REG Register

5.2.2.103.1 CPSW_NC_CPPI_P0_TH_BLKS_PRI_REG Register (Offset = 21028h) [reset = 1245678h]

CPPI Port 0 Transmit Block Sub Per Priority

Return to Summary Table

Table 5-377. Instance Table

Instance Name	Physical Address
CPSW0	5282 1028h + formula

Figure 5-184. CPSW_NC_CPPI_P0_TH_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 5-378. CPSW_NC_CPPI_P0_TH_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27:24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23:20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19:16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15:12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11:8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7:4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3:0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

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5.2.2.104 CPSW_NC_CPPI_P0_IDLE2LPI_REG Register

5.2.2.104.1 CPSW_NC_CPPI_P0_IDLE2LPI_REG Register (Offset = 21030h) [reset = 0h]

Port 0 EEE Idle to LPI counter

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Table 5-379. Instance Table

Instance Name	Physical Address
CPSW0	5282 1030h + formula

Figure 5-185. CPSW_NC_CPPI_P0_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-380. CPSW_NC_CPPI_P0_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Port 0 EEE Idle to LPI counter load value - After CLKSTOP_REQ is asserted, this value is loaded into the port 0 idle to LPI counter on each clock that the port 0 transmit is not idle. Port 0 enters the transmit LPI state when this counter decrements to zero. This counter decrements each time the EEE prescale counter decrements to zero.

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5.2.2.105 CPSW_NC_CPPI_P0_LPI2WAKE_REG Register

5.2.2.105.1 CPSW_NC_CPPI_P0_LPI2WAKE_REG Register (Offset = 21034h) [reset = 0h]

Port 0 EEE LPI to wake counter

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Table 5-381. Instance Table

Instance Name	Physical Address
CPSW0	5282 1034h + formula

Figure 5-186. CPSW_NC_CPPI_P0_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-382. CPSW_NC_CPPI_P0_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Port 0 EEE LPI to wake counter load value - When the port is in the transmit LPI state and the CLKSTOP_REQ signal is deasserted, this value is loaded into the port 0 LPI to wake counter. Transmit packet operations may begin (resume) when the LPI to wake count decrements to zero (on the pre-scale count). This is the time that the CPDMA transmit must wait before transmit (switch ingress) packet operations begin (resume after wakeup).

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5.2.2.106 CPSW_NC_CPPI_P0_EEE_STATUS_REG Register

5.2.2.106.1 CPSW_NC_CPPI_P0_EEE_STATUS_REG Register (Offset = 21038h) [reset = 60h]

Port 0 EEE status

Return to Summary Table

Table 5-383. Instance Table

Instance Name	Physical Address
CPSW0	5282 1038h + formula

Figure 5-187. CPSW_NC_CPPI_P0_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	TH_FIFO_EMPTY	FH_FIFO_EMPTY	TH_FIFO_HOLD	TH_WAKE	TH_LPI	FH_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 5-384. CPSW_NC_CPPI_P0_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TH_FIFO_EMPTY	R	1h	CPPI port 0 transmit FIFO (switch egress) is empty - contains no packets
5	FH_FIFO_EMPTY	R	1h	CPPI port 0 receive FIFO (switch ingress) is empty - contains no packets
4	TH_FIFO_HOLD	R	0h	CPPI port 0 transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TH_WAKE	R	0h	CPPI port 0 transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TH_LPI	R	0h	CPPI port 0 transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	FH_LPI	R	0h	CPPI port 0 receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

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5.2.2.107 CPSW_NC_CPPI_P0_FIFO_STATUS_REG Register

5.2.2.107.1 CPSW_NC_CPPI_P0_FIFO_STATUS_REG Register (Offset = 21050h) [reset = 0h]

Port 0 FIFO Status

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Table 5-385. Instance Table

Instance Name	Physical Address
CPSW0	5282 1050h + formula

Figure 5-188. CPSW_NC_CPPI_P0_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH_PRI_ACTIVE							
R							
0h							

Table 5-386. CPSW_NC_CPPI_P0_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH_PRI_ACTIVE	R	0h	Port 0 Transmit FIFO Priority Active. Each bit indicates whether the corresponding FIFO priority has one or more queued packets on it or not. note: for N=2 this field is always zero (there is no transmit FIFO).

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5.2.2.108 CPSW_NC_CPPI_FH_DSCP_MAP_REG_J Register

5.2.2.108.1 CPSW_NC_CPPI_FH_DSCP_MAP_REG_J Register (Offset = 21120h) [reset = 0h]

CPPI Receive IPV4/IPV6 DSCP Map N

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Table 5-387. Instance Table

Instance Name	Physical Address
CPSW0	5282 1120h + formula

Figure 5-189. CPSW_NC_CPPI_FH_DSCP_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 5-388. CPSW_NC_CPPI_FH_DSCP_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS 7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS 6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS 5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS 4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS 3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS 2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS 1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS 0 is mapped to this received priority

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5.2.2.109 CPSW_NC_CPPI_P0_PRI_CIR_REG_J Register

5.2.2.109.1 CPSW_NC_CPPI_P0_PRI_CIR_REG_J Register (Offset = 21140h) [reset = 0h]

CPPI Port 0 Rx Priority P Committed Information Rate

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Table 5-389. Instance Table

Instance Name	Physical Address
CPSW0	5282 1140h + formula

Figure 5-190. CPSW_NC_CPPI_P0_PRI_CIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_CIR			
NONE				R/W			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_CIR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_CIR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_CIR							
R/W							
0h							

Table 5-390. CPSW_NC_CPPI_P0_PRI_CIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N Committed Information Rate

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5.2.2.110 CPSW_NC_CPPI_P0_PRI_EIR_REG_J Register

5.2.2.110.1 CPSW_NC_CPPI_P0_PRI_EIR_REG_J Register (Offset = 21160h) [reset = 0h]

CPPI Port 0 Rx Priority P Excess Information Rate

Return to Summary Table

Table 5-391. Instance Table

Instance Name	Physical Address
CPSW0	5282 1160h + formula

Figure 5-191. CPSW_NC_CPPI_P0_PRI_EIR_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_EIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_EIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_EIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_EIR							
R/W							
0h							

Table 5-392. CPSW_NC_CPPI_P0_PRI_EIR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N Excess Information Rate

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5.2.2.111 CPSW_NC_CPPI_P0_TH_D_THRESH_SET_L_REG Register

5.2.2.111.1 CPSW_NC_CPPI_P0_TH_D_THRESH_SET_L_REG Register (Offset = 21180h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Destination Threshold Set Low

Return to Summary Table

Table 5-393. Instance Table

Instance Name	Physical Address
CPSW0	5282 1180h + formula

Figure 5-192. CPSW_NC_CPPI_P0_TH_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 5-394. CPSW_NC_CPPI_P0_TH_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

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5.2.2.112 CPSW_NC_CPPI_P0_TH_D_THRESH_SET_H_REG Register

5.2.2.112.1 CPSW_NC_CPPI_P0_TH_D_THRESH_SET_H_REG Register (Offset = 21184h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Destination Threshold Set High

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Table 5-395. Instance Table

Instance Name	Physical Address
CPSW0	5282 1184h + formula

Figure 5-193. CPSW_NC_CPPI_P0_TH_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 5-396. CPSW_NC_CPPI_P0_TH_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

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5.2.2.113 CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_L_REG Register

5.2.2.113.1 CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_L_REG Register (Offset = 21188h) [reset = 0h]

CPPI Port 0 Tx PFC Destination Threshold Clr Low

Return to Summary Table

Table 5-397. Instance Table

Instance Name	Physical Address
CPSW0	5282 1188h + formula

Figure 5-194. CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 5-398. CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

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5.2.2.114 CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_H_REG Register

5.2.2.114.1 CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_H_REG Register (Offset = 2118Ch) [reset = 0h]

CPPI Port 0 Tx PFC Destination Threshold Clr High

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Table 5-399. Instance Table

Instance Name	Physical Address
CPSW0	5282 118Ch + formula

Figure 5-195. CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 5-400. CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

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5.2.2.115 CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_L_REG Register

5.2.2.115.1 CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_L_REG Register (Offset = 21190h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Global Buffer Threshold Set Low

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Table 5-401. Instance Table

Instance Name	Physical Address
CPSW0	5282 1190h + formula

Figure 5-196. CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 5-402. CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

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5.2.2.116 CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_H_REG Register

5.2.2.116.1 CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_H_REG Register (Offset = 21194h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Global Buffer Threshold Set High

Return to Summary Table

Table 5-403. Instance Table

Instance Name	Physical Address
CPSW0	5282 1194h + formula

Figure 5-197. CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 5-404. CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

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5.2.2.117 CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_L_REG Register

5.2.2.117.1 CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_L_REG Register (Offset = 21198h) [reset = 0h]

CPPI Port 0 Tx PFC Global Buffer Threshold Clr Low

Return to Summary Table

Table 5-405. Instance Table

Instance Name	Physical Address
CPSW0	5282 1198h + formula

Figure 5-198. CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 5-406. CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

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5.2.2.118 CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_H_REG Register

5.2.2.118.1 CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_H_REG Register (Offset = 2119Ch) [reset = 0h]

CPPI Port 0 Tx PFC Global Buffer Threshold Clr High

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Table 5-407. Instance Table

Instance Name	Physical Address
CPSW0	5282 119Ch + formula

Figure 5-199. CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 5-408. CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

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5.2.2.119 CPSW_NC_CPPI_P0_SRC_ID_A_REG Register

5.2.2.119.1 CPSW_NC_CPPI_P0_SRC_ID_A_REG Register (Offset = 21300h) [reset = 4030201h]

CPPI Port 0 CPPI Source ID A

Return to Summary Table

Table 5-409. Instance Table

Instance Name	Physical Address
CPSW0	5282 1300h + formula

Figure 5-200. CPSW_NC_CPPI_P0_SRC_ID_A_REG Name Register

31	30	29	28	27	26	25	24
PORT4							
R/W							
4h							
23	22	21	20	19	18	17	16
PORT3							
R/W							
3h							
15	14	13	12	11	10	9	8
PORT2							
R/W							
2h							
7	6	5	4	3	2	1	0
PORT1							
R/W							
1h							

Table 5-410. CPSW_NC_CPPI_P0_SRC_ID_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PORT4	R/W	4h	Port 4 CPPI Info Word0 Source ID Value
23:16	PORT3	R/W	3h	Port 3 CPPI Info Word0 Source ID Value
15:8	PORT2	R/W	2h	Port 2 CPPI Info Word0 Source ID Value
7:0	PORT1	R/W	1h	Port 1 CPPI Info Word0 Source ID Value

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5.2.2.120 CPSW_NC_CPPI_P0_SRC_ID_B_REG Register

5.2.2.120.1 CPSW_NC_CPPI_P0_SRC_ID_B_REG Register (Offset = 21304h) [reset = 8070605h]

CPPI Port 0 CPPI Source ID B

Return to Summary Table

Table 5-411. Instance Table

Instance Name	Physical Address
CPSW0	5282 1304h + formula

Figure 5-201. CPSW_NC_CPPI_P0_SRC_ID_B_REG Name Register

31	30	29	28	27	26	25	24
PORT8							
R/W							
8h							
23	22	21	20	19	18	17	16
PORT7							
R/W							
7h							
15	14	13	12	11	10	9	8
PORT6							
R/W							
6h							
7	6	5	4	3	2	1	0
PORT5							
R/W							
5h							

Table 5-412. CPSW_NC_CPPI_P0_SRC_ID_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	PORT8	R/W	8h	Port 8 CPPI Info Word0 Source ID Value
23:16	PORT7	R/W	7h	Port 7 CPPI Info Word0 Source ID Value
15:8	PORT6	R/W	6h	Port 6 CPPI Info Word0 Source ID Value
7:0	PORT5	R/W	5h	Port 5 CPPI Info Word0 Source ID Value

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5.2.2.121 CPSW_NC_CPPI_P0_HOST_BLKS_PRI_REG Register

5.2.2.121.1 CPSW_NC_CPPI_P0_HOST_BLKS_PRI_REG Register (Offset = 21320h) [reset = 0h]

CPPI Port 0 Host Blocks Priority

Return to Summary Table

Table 5-413. Instance Table

Instance Name	Physical Address
CPSW0	5282 1320h + formula

Figure 5-202. CPSW_NC_CPPI_P0_HOST_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
0h				0h			

Table 5-414. CPSW_NC_CPPI_P0_HOST_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Priority 7 Host Blocks
27:24	PRI6	R/W	0h	Priority 6 Host Blocks
23:20	PRI5	R/W	0h	Priority 5 Host Blocks
19:16	PRI4	R/W	0h	Priority 4 Host Blocks
15:12	PRI3	R/W	0h	Priority 3 Host Blocks
11:8	PRI2	R/W	0h	Priority 2 Host Blocks
7:4	PRI1	R/W	0h	Priority 1 Host Blocks
3:0	PRI0	R/W	0h	Priority 0 Host Blocks

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5.2.2.122 CPSW_NC_ETH_MAC_PN_CONTROL_REG_J Register

5.2.2.122.1 CPSW_NC_ETH_MAC_PN_CONTROL_REG_J Register (Offset = 22004h) [reset = 0h]

Enet Port N Control

Return to Summary Table

Table 5-415. Instance Table

Instance Name	Physical Address
CPSW0	5282 2004h + formula

Figure 5-203. CPSW_NC_ETH_MAC_PN_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						EST_PORT_EN	RESERVED
NONE						R/W	NONE
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_ECC_ERR_EN	TX_ECC_ERR_EN	RESERVED	TX_LPI_CLKSTOP_EN	RESERVED			
R/W	R/W	NONE	R/W	NONE			
0h	0h	0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
NONE					R/W	R/W	NONE
0h					0h	0h	0h

Table 5-416. CPSW_NC_ETH_MAC_PN_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17	EST_PORT_EN	R/W	0h	EST Port Enable 0 - EST is disabled on the port. 1 - EST is enabled on the port (Does not take effect until the CPSW level est_en is set).
16	RESERVED	NONE	0h	Reserved
15	RX_ECC_ERR_EN	R/W	0h	This bit must be set to enable receive ECC error operations on the port.
14	TX_ECC_ERR_EN	R/W	0h	This bit must be set to enable transmit ECC error operations on the port.
13	RESERVED	NONE	0h	Reserved
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI Clock Stop Enable - When set this bit causes the transmit output clock (GMII_GMTCLK_O) to be stopped when the transmit LPI state is entered if EEE is enabled.
11:3	RESERVED	NONE	0h	Reserved
2	DSCP_IPV6_EN	R/W	0h	IPv6 DSCP enable 0 - Ipv6 DSCP priority mapping is disabled. 1 - Ipv6 DSCP priority mapping is enabled.
1	DSCP_IPV4_EN	R/W	0h	IPv4 DSCP enable 0 - Ipv4 DSCP priority mapping is disabled. 1 - Ipv4 DSCP priority mapping is enabled.

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Table 5-416. CPSW_NC_ETH_MAC_PN_CONTROL_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	NONE	0h	Reserved

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5.2.2.123 CPSW_NC_ETH_MAC_PN_MAX_BLKS_REG_J Register

5.2.2.123.1 CPSW_NC_ETH_MAC_PN_MAX_BLKS_REG_J Register (Offset = 22008h) [reset = 1004h]

Enet Port N FIFO Max Blocks

Return to Summary Table

Table 5-417. Instance Table

Instance Name	Physical Address
CPSW0	5282 2008h + formula

Figure 5-204. CPSW_NC_ETH_MAC_PN_MAX_BLKS_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_MAX_BLKS							
R/W							
10h							
7	6	5	4	3	2	1	0
RX_MAX_BLKS							
R/W							
4h							

Table 5-418. CPSW_NC_ETH_MAC_PN_MAX_BLKS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	TX_MAX_BLKS	R/W	10h	Transmit Max Blocks - The maximum number of blocks allowed on all transmit FIFO priorities combined. If (fifo_oneram = 1) then blocks should be moved from transmit to receive when flow control is enabled to allow for flow control runout.
7:0	RX_MAX_BLKS	R/W	4h	Receive Max Blocks - The maximum number of blocks allowed on the express and prempt receive FIFOs (transmit and receive FIFOs combined when fifo_oneram = 1)

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5.2.2.124 CPSW_NC_ETH_MAC_PN_BLK_CNT_REG_J Register

5.2.2.124.1 CPSW_NC_ETH_MAC_PN_BLK_CNT_REG_J Register (Offset = 22010h) [reset = 1h]

Enet Port N FIFO Block Usage Count

Return to Summary Table

Table 5-419. Instance Table

Instance Name	Physical Address
CPSW0	5282 2010h + formula

Figure 5-205. CPSW_NC_ETH_MAC_PN_BLK_CNT_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		RX_BLK_CNT_P					
NONE		R					
0h		0h					
15	14	13	12	11	10	9	8
RESERVED			TX_BLK_CNT				
NONE			R				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED		RX_BLK_CNT_E					
NONE		R					
0h		1h					

Table 5-420. CPSW_NC_ETH_MAC_PN_BLK_CNT_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	RX_BLK_CNT_P	R	0h	Receive Express Block Count Usage - This value is the number of blocks allocated to the port FIFO prempt receive queue. No blocks are allocated until the iet_en in the CPSW_Control register is set.
15:13	RESERVED	NONE	0h	Reserved
12:8	TX_BLK_CNT	R	0h	Transmit Block Count Usage - This value is the number of blocks allocated to the port FIFO logical transmit queues.
7:6	RESERVED	NONE	0h	Reserved
5:0	RX_BLK_CNT_E	R	1h	Receive Express Block Count Usage - This value is the number of blocks allocated to the ports FIFO express receive queue.

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5.2.2.125 CPSW_NC_ETH_MAC_PN_PORT_VLAN_REG_J Register

5.2.2.125.1 CPSW_NC_ETH_MAC_PN_PORT_VLAN_REG_J Register (Offset = 22014h) [reset = 0h]

Enet Port N VLAN

Return to Summary Table

Table 5-421. Instance Table

Instance Name	Physical Address
CPSW0	5282 2014h + formula

Figure 5-206. CPSW_NC_ETH_MAC_PN_PORT_VLAN_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PORT_PRI			PORT_CFI	PORT_VID			
R/W			R/W	R/W			
0h			0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PORT_VID							
R/W							
0h							

Table 5-422. CPSW_NC_ETH_MAC_PN_PORT_VLAN_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11:0	PORT_VID	R/W	0h	Port VLAN ID

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5.2.2.126 CPSW_NC_ETH_MAC_PN_TX_PRI_MAP_REG_J Register

5.2.2.126.1 CPSW_NC_ETH_MAC_PN_TX_PRI_MAP_REG_J Register (Offset = 22018h) [reset = 76543210h]

Enet Port N Tx Header Pri to Switch Pri Mapping

Return to Summary Table

Table 5-423. Instance Table

Instance Name	Physical Address
CPSW0	5282 2018h + formula

Figure 5-207. CPSW_NC_ETH_MAC_PN_TX_PRI_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 5-424. CPSW_NC_ETH_MAC_PN_TX_PRI_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7 - A packet header priority of 0x7 is given this switch queue priority.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6 - A packet header priority of 0x6 is given this switch queue priority.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5 - A packet header priority of 0x5 is given this switch queue priority.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4 - A packet header priority of 0x4 is given this switch queue priority.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3 - A packet header priority of 0x3 is given this switch queue priority.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2 - A packet header priority of 0x2 is given this switch queue priority.
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	1h	Priority 1 - A packet header priority of 0x1 is given this switch queue priority.

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Table 5-424. CPSW_NC_ETH_MAC_PN_TX_PRI_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0 - A packet header priority of 0x0 is given this switch queue priority.

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5.2.2.127 CPSW_NC_ETH_MAC_PN_PRI_CTL_REG_J Register

5.2.2.127.1 CPSW_NC_ETH_MAC_PN_PRI_CTL_REG_J Register (Offset = 2201Ch) [reset = 9000h]

Enet Port N Priority Control

Return to Summary Table

Table 5-425. Instance Table

Instance Name	Physical Address
CPSW0	5282 201Ch + formula

Figure 5-208. CPSW_NC_ETH_MAC_PN_PRI_CTL_REG_j Name Register

31	30	29	28	27	26	25	24
TX_FLOW_PRI							
R/W							
0h							
23	22	21	20	19	18	17	16
RX_FLOW_PRI							
R/W							
0h							
15	14	13	12	11	10	9	8
TX_HOST_BLKS_REM				RESERVED			
R/W				NONE			
9h				0h			
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-426. CPSW_NC_ETH_MAC_PN_PRI_CTL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23:16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15:12	TX_HOST_BLKS_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11:0	RESERVED	NONE	0h	Reserved

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5.2.2.128 CPSW_NC_ETH_MAC_PN_RX_PRI_MAP_REG_J Register

5.2.2.128.1 CPSW_NC_ETH_MAC_PN_RX_PRI_MAP_REG_J Register (Offset = 22020h) [reset = 76543210h]

Enet Port N RX Pkt Pri to Header Pri Map

Return to Summary Table

Table 5-427. Instance Table

Instance Name	Physical Address
CPSW0	5282 2020h + formula

Figure 5-209. CPSW_NC_ETH_MAC_PN_RX_PRI_MAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	7h			0h	6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	5h			0h	4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	3h			0h	2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	1h			0h	0h		

Table 5-428. CPSW_NC_ETH_MAC_PN_RX_PRI_MAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	7h	Priority 7 - A packet priority of 7 is mapped (changed) to this header packet priority.
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	6h	Priority 6 - A packet priority of 6 is mapped (changed) to this header packet priority.
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	5h	Priority 5 - A packet priority of 5 is mapped (changed) to this header packet priority.
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	4h	Priority 4 - A packet priority of 4 is mapped (changed) to this header packet priority.
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	3h	Priority 3 - A packet priority of 3 is mapped (changed) to this header packet priority.
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	2h	Priority 2 - A packet priority of 2 is mapped (changed) to this header packet priority.
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	1h	Priority 1 - A packet priority of 1 is mapped (changed) to this header packet priority.

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Table 5-428. CPSW_NC_ETH_MAC_PN_RX_PRI_MAP_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	Priority 0 - A packet priority of 0 is mapped (changed) to this header packet priority.

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5.2.2.129 CPSW_NC_ETH_MAC_PN_RX_MAXLEN_REG_J Register

5.2.2.129.1 CPSW_NC_ETH_MAC_PN_RX_MAXLEN_REG_J Register (Offset = 22024h) [reset = 5EEh]

Enet Port N Receive Frame Max Length

Return to Summary Table

Table 5-429. Instance Table

Instance Name	Physical Address
CPSW0	5282 2024h + formula

Figure 5-210. CPSW_NC_ETH_MAC_PN_RX_MAXLEN_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED		RX_MAXLEN					
NONE		R/W					
0h		5EEh					
7	6	5	4	3	2	1	0
RX_MAXLEN							
R/W							
5EEh							

Table 5-430. CPSW_NC_ETH_MAC_PN_RX_MAXLEN_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:14	RESERVED	NONE	0h	Reserved
13:0	RX_MAXLEN	R/W	5EEh	RX Maximum Frame Length - This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than pn_rx_maxlen are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 2024 (including VLAN).

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5.2.2.130 CPSW_NC_ETH_MAC_PN_TX_BLKS_PRI_REG_J Register

5.2.2.130.1 CPSW_NC_ETH_MAC_PN_TX_BLKS_PRI_REG_J Register (Offset = 22028h) [reset = 1245678h]

Enet Port N Transmit Block Sub Per Priority

Return to Summary Table

Table 5-431. Instance Table

Instance Name	Physical Address
CPSW0	5282 2028h + formula

Figure 5-211. CPSW_NC_ETH_MAC_PN_TX_BLKS_PRI_REG_j Name Register

31	30	29	28	27	26	25	24
PRI7				PRI6			
R/W				R/W			
0h				1h			
23	22	21	20	19	18	17	16
PRI5				PRI4			
R/W				R/W			
2h				4h			
15	14	13	12	11	10	9	8
PRI3				PRI2			
R/W				R/W			
5h				6h			
7	6	5	4	3	2	1	0
PRI1				PRI0			
R/W				R/W			
7h				8h			

Table 5-432. CPSW_NC_ETH_MAC_PN_TX_BLKS_PRI_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	PRI7	R/W	0h	Transmit Blocks Per Priority 7 (subtract value)
27:24	PRI6	R/W	1h	Transmit Blocks Per Priority 6 (subtract value)
23:20	PRI5	R/W	2h	Transmit Blocks Per Priority 5 (subtract value)
19:16	PRI4	R/W	4h	Transmit Blocks Per Priority 4 (subtract value)
15:12	PRI3	R/W	5h	Transmit Blocks Per Priority 3 (subtract value)
11:8	PRI2	R/W	6h	Transmit Blocks Per Priority 2 (subtract value)
7:4	PRI1	R/W	7h	Transmit Blocks Per Priority 1 (subtract value)
3:0	PRI0	R/W	8h	Transmit Blocks Per Priority 0 (subtract value)

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5.2.2.131 CPSW_NC_ETH_MAC_PN_IDLE2LPI_REG_J Register

5.2.2.131.1 CPSW_NC_ETH_MAC_PN_IDLE2LPI_REG_J Register (Offset = 22030h) [reset = 0h]

Enet Port N EEE Idle to LPI counter

Return to Summary Table

Table 5-433. Instance Table

Instance Name	Physical Address
CPSW0	5282 2030h + formula

Figure 5-212. CPSW_NC_ETH_MAC_PN_IDLE2LPI_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-434. CPSW_NC_ETH_MAC_PN_IDLE2LPI_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE Idle to LPI counter load value - After CLKSTOP_REQ is asserted, this value is loaded into the port idle to LPI counter on each clock that the port transmit is not idle. The port enters the transmit LPI state when this counter decrements to zero. This counter decrements each time the EEE prescale counter decrements to zero.

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5.2.2.132 CPSW_NC_ETH_MAC_PN_LPI2WAKE_REG_J Register

5.2.2.132.1 CPSW_NC_ETH_MAC_PN_LPI2WAKE_REG_J Register (Offset = 22034h) [reset = 0h]

Enet Port N EEE LPI to wake counter

Return to Summary Table

Table 5-435. Instance Table

Instance Name	Physical Address
CPSW0	5282 2034h + formula

Figure 5-213. CPSW_NC_ETH_MAC_PN_LPI2WAKE_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-436. CPSW_NC_ETH_MAC_PN_LPI2WAKE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	EEE LPI to wake counter load value - When the port is in the transmit LPI state and the CLKSTOP_REQ signal is deasserted, this value is loaded into the LPI to wake counter. Transmit packet operations may begin (resume) when the LPI to wake count decrements to zero (on the pre-scale count). This is the time that the transmit must wait before transmit packet operations resume after wakeup.

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5.2.2.133 CPSW_NC_ETH_MAC_PN_EEE_STATUS_REG_J Register

5.2.2.133.1 CPSW_NC_ETH_MAC_PN_EEE_STATUS_REG_J Register (Offset = 22038h) [reset = 62h]

Enet Port N EEE status

Return to Summary Table

Table 5-437. Instance Table

Instance Name	Physical Address
CPSW0	5282 2038h + formula

Figure 5-214. CPSW_NC_ETH_MAC_PN_EEE_STATUS_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	1h	0h

Table 5-438. CPSW_NC_ETH_MAC_PN_EEE_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	TX_FIFO_EMPTY	R	1h	Transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	Receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	Transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	Transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	1h	Receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

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5.2.2.134 CPSW_NC_ETH_MAC_PN_FIFO_STATUS_REG_J Register

5.2.2.134.1 CPSW_NC_ETH_MAC_PN_FIFO_STATUS_REG_J Register (Offset = 22050h) [reset = FF00h]

Enet Port N FIFO STATUS

Return to Summary Table

Table 5-439. Instance Table

Instance Name	Physical Address
CPSW0	5282 2050h + formula

Figure 5-215. CPSW_NC_ETH_MAC_PN_FIFO_STATUS_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					EST_BUFACT	EST_ADD_ERR	EST_CNT_ERR
NONE					R	R	R
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TX_E_MAC_ALLOW							
R							
FFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_PRI_ACTIVE							
R							
0h							

Table 5-440. CPSW_NC_ETH_MAC_PN_FIFO_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18	EST_BUFACT	R	0h	EST RAM active buffer - Indicates the active 64-word fetch buffer when pn_est_onebuf is cleared to zero. Indicates the fetch ram address MSB when pn_est_onebuf set to one.
17	EST_ADD_ERR	R	0h	EST Address Error - Indicates that the fetch ram was read again after the previous maximum buffer address read (the previous fetch from the maximum address is reused).
16	EST_CNT_ERR	R	0h	EST Fetch Count Error - Indicates that insufficient clocks were programmed into the fetch count and that another fetch was commanded before the previous fetch finished.
15:8	TX_E_MAC_ALLOW	R	FFh	Transmit mac allow - Bus that indicates the actual priorities assigned to the express queue (and inversely the priorities assigned to the prempt queue). The pn_mac_prempt[7:0] field in the Enet_Pn_IET_Control register indicates which priorities should be assigned to the express/prempt queues. The switch between queues happens only when the priority is empty and the actual assignment is shown in this field.
7:0	TX_PRI_ACTIVE	R	0h	Transmit Priority Active - Bus that indicates which priorities have packets (non-empty) at the time of the register read.

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5.2.2.135 CPSW_NC_ETH_MAC_PN_EST_CONTROL_REG_J Register

5.2.2.135.1 CPSW_NC_ETH_MAC_PN_EST_CONTROL_REG_J Register (Offset = 22060h) [reset = 0h]

Enet Port N EST CONTROL

Return to Summary Table

Table 5-441. Instance Table

Instance Name	Physical Address
CPSW0	5282 2060h + formula

Figure 5-216. CPSW_NC_ETH_MAC_PN_EST_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED						EST_FILL_MARGIN	
NONE						R/W	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EST_FILL_MARGIN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EST_PREMPT_COMP							EST_FILL_EN
R/W							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 5-442. CPSW_NC_ETH_MAC_PN_EST_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	EST_FILL_MARGIN	R/W	0h	EST Fill Margin - Sets the fill margin (in bytes) required to ensure that the Ethernet wire is clear so that the timed EST express packet can egress at the correct required time. Setting this value too high will put an unnecessary gap on the wire. Setting this value too low will cause the express packet to egress at a time later than intended (pushed out by non express traffic that did not have sufficient time to finish).
15:9	EST_PREMPT_COMP	R/W	0h	EST Prempt Comparison Value - When the count in a zero allow is less than or equal to this value in bytes (times 8), prempt packets are cleared from the wire. This is the prempt clear margin value.
8	EST_FILL_EN	R/W	0h	EST Fill Enable - Enable EST fill mode when set.
7:5	EST_TS_PRI	R/W	0h	EST Timestamp Express Priority - Selects the express priority that timestamp(s) will be generated on when pn_est_ts_onepri is set.
4	EST_TS_ONEPRI	R/W	0h	EST Timestamp One Express Priority - When set, timestamps are only enabled on packets on the express priority selected by pn_est_ts_pri. When cleared to zero, express packet selection for timestamps is independent of priority.
3	EST_TS_FIRST	R/W	0h	EST Timestamp First Express Packet only - Generate a timestamp only on the first selected express packet in each EST time interval when express timestamps are enabled. (If pn_est_ts_onepri is also set then the timestamp is generated only on the first packet on pn_est_ts_pri).

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Table 5-442. CPSW_NC_ETH_MAC_PN_EST_CONTROL_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EST_TS_EN	R/W	0h	EST Timestamp Enable - Enable express timestamps (when est_en and pn_est_port_en are set).
1	EST_BUFSEL	R/W	0h	EST Buffer Select - If pn_est_onebuf is cleared, this bit selects the upper (when set) or the lower (when cleared) 64-word fetch buffer. The actual fetch buffer used changes only at the start of the EST time interval and can be read in the Enet_Pn_FIFO_Status register pn_est_bufact bit.
0	EST_ONEBUF	R/W	0h	EST One Fetch Buffer - When set indicates that all 128 fetch words are used in one buffer. When cleared, indicates that the 128 fetch words are split into two 64-word fetch buffers. The pn_est_bufsel selects the buffer to be used when pn_est_onebuf is cleared to zero. Two buffers allows software to change a buffer while the hardware is using the other buffer.

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5.2.2.136 CPSW_NC_ETH_MAC_PN_FH_DSCP_MAP_REG_J_K Register

5.2.2.136.1 CPSW_NC_ETH_MAC_PN_FH_DSCP_MAP_REG_J_K Register (Offset = 22120h) [reset = 0h]

Enet Port N Receive IPV4/IPV6 DSCP Map N

Return to Summary Table

Table 5-443. Instance Table

Instance Name	Physical Address
CPSW0	5282 2120h + formula

Figure 5-217. CPSW_NC_ETH_MAC_PN_FH_DSCP_MAP_REG_j_k Name Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	PRI5			RESERVED	PRI4		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED	PRI3			RESERVED	PRI2		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	PRI1			RESERVED	PRI0		
NONE	R/W			NONE	R/W		
0h	0h			0h	0h		

Table 5-444. CPSW_NC_ETH_MAC_PN_FH_DSCP_MAP_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS 7 is mapped to this received priority
27	RESERVED	NONE	0h	Reserved
26:24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS 6 is mapped to this received priority
23	RESERVED	NONE	0h	Reserved
22:20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS 5 is mapped to this received priority
19	RESERVED	NONE	0h	Reserved
18:16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS 4 is mapped to this received priority
15	RESERVED	NONE	0h	Reserved
14:12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS 3 is mapped to this received priority
11	RESERVED	NONE	0h	Reserved
10:8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS 2 is mapped to this received priority
7	RESERVED	NONE	0h	Reserved
6:4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS 1 is mapped to this received priority
3	RESERVED	NONE	0h	Reserved
2:0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS 0 is mapped to this received priority

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5.2.2.137 CPSW_NC_ETH_MAC_PN_PRI_CIR_REG_J_K Register

5.2.2.137.1 CPSW_NC_ETH_MAC_PN_PRI_CIR_REG_J_K Register (Offset = 22140h) [reset = 0h]

Enet Port N Rx Priority P Committed Information Rate Value

Return to Summary Table

Table 5-445. Instance Table

Instance Name	Physical Address
CPSW0	5282 2140h + formula

Figure 5-218. CPSW_NC_ETH_MAC_PN_PRI_CIR_REG_j_k Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_CIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_CIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_CIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_CIR							
R/W							
0h							

Table 5-446. CPSW_NC_ETH_MAC_PN_PRI_CIR_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_CIR	R/W	0h	Priority N committed information rate

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5.2.2.138 CPSW_NC_ETH_MAC_PN_PRI_EIR_REG_J_K Register

5.2.2.138.1 CPSW_NC_ETH_MAC_PN_PRI_EIR_REG_J_K Register (Offset = 22160h) [reset = 0h]

Enet Port N Rx Priority P Excess Informatoin Rate Value

Return to Summary Table

Table 5-447. Instance Table

Instance Name	Physical Address
CPSW0	5282 2160h + formula

Figure 5-219. CPSW_NC_ETH_MAC_PN_PRI_EIR_REG_j_k Name Register

31	30	29	28	27	26	25	24
RESERVED				PRI_EIR			
NONE				R/W			
0h				0h			
23	22	21	20	19	18	17	16
PRI_EIR							
R/W							
0h							
15	14	13	12	11	10	9	8
PRI_EIR							
R/W							
0h							
7	6	5	4	3	2	1	0
PRI_EIR							
R/W							
0h							

Table 5-448. CPSW_NC_ETH_MAC_PN_PRI_EIR_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

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5.2.2.139 CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_L_REG_J Register

5.2.2.139.1 CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_L_REG_J Register (Offset = 22180h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Destination Threshold Set Low

Return to Summary Table

Table 5-449. Instance Table

Instance Name	Physical Address
CPSW0	5282 2180h + formula

Figure 5-220. CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_L_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 5-450. CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_L_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

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5.2.2.140 CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_H_REG_J Register

5.2.2.140.1 CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_H_REG_J Register (Offset = 22184h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Destination Threshold Set High

Return to Summary Table

Table 5-451. Instance Table

Instance Name	Physical Address
CPSW0	5282 2184h + formula

Figure 5-221. CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_H_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 5-452. CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_H_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

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5.2.2.141 CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_L_REG_J Register

5.2.2.141.1 CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_L_REG_J Register (Offset = 22188h) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr Low

Return to Summary Table

Table 5-453. Instance Table

Instance Name	Physical Address
CPSW0	5282 2188h + formula

Figure 5-222. CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_L_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 5-454. CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_L_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

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5.2.2.142 CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_H_REG_J Register

5.2.2.142.1 CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_H_REG_J Register (Offset = 2218Ch) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr High

Return to Summary Table

Table 5-455. Instance Table

Instance Name	Physical Address
CPSW0	5282 218Ch + formula

Figure 5-223. CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_H_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 5-456. CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_H_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

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5.2.2.143 CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_L_REG_J Register

5.2.2.143.1 CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_L_REG_J Register (Offset = 22190h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Global Buffer Threshold Set Low

Return to Summary Table

Table 5-457. Instance Table

Instance Name	Physical Address
CPSW0	5282 2190h + formula

Figure 5-224. CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_L_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			1Fh				

Table 5-458. CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_L_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

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5.2.2.144 CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_H_REG_J Register

5.2.2.144.1 CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_H_REG_J Register (Offset = 22194h) [reset = 1F1F1F1Fh]

Enet Port N Tx PFC Global Buffer Threshold Set High

Return to Summary Table

Table 5-459. Instance Table

Instance Name	Physical Address
CPSW0	5282 2194h + formula

Figure 5-225. CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_H_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			1Fh				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			1Fh				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			1Fh				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			1Fh				

Table 5-460. CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_H_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

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5.2.2.145 CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_L_REG_J Register

5.2.2.145.1 CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_L_REG_J Register (Offset = 22198h) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr Low

Return to Summary Table

Table 5-461. Instance Table

Instance Name	Physical Address
CPSW0	5282 2198h + formula

Figure 5-226. CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_L_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 5-462. CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_L_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

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5.2.2.146 CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_H_REG_J Register

5.2.2.146.1 CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_H_REG_J Register (Offset = 2219Ch) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr High

Return to Summary Table

Table 5-463. Instance Table

Instance Name	Physical Address
CPSW0	5282 219Ch + formula

Figure 5-227. CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_H_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 5-464. CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_H_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

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5.2.2.147 CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_L_REG_J Register

5.2.2.147.1 CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_L_REG_J Register (Offset = 22300h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values Low

Return to Summary Table

Table 5-465. Instance Table

Instance Name	Physical Address
CPSW0	5282 2300h + formula

Figure 5-228. CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_L_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI3				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI2				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI1				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI0				
NONE			R/W				
0h			0h				

Table 5-466. CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_L_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

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5.2.2.148 CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_H_REG_J Register

5.2.2.148.1 CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_H_REG_J Register (Offset = 22304h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values High

Return to Summary Table

Table 5-467. Instance Table

Instance Name	Physical Address
CPSW0	5282 2304h + formula

Figure 5-229. CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_H_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED			PRI7				
NONE			R/W				
0h			0h				
23	22	21	20	19	18	17	16
RESERVED			PRI6				
NONE			R/W				
0h			0h				
15	14	13	12	11	10	9	8
RESERVED			PRI5				
NONE			R/W				
0h			0h				
7	6	5	4	3	2	1	0
RESERVED			PRI4				
NONE			R/W				
0h			0h				

Table 5-468. CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_H_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED	NONE	0h	Reserved
28:24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23:21	RESERVED	NONE	0h	Reserved
20:16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15:13	RESERVED	NONE	0h	Reserved
12:8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7:5	RESERVED	NONE	0h	Reserved
4:0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

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5.2.2.149 CPSW_NC_ETH_MAC_PN_SA_L_REG_J Register

5.2.2.149.1 CPSW_NC_ETH_MAC_PN_SA_L_REG_J Register (Offset = 22308h) [reset = 0h]

Enet Port N Tx Pause Frame Source Address Low

Return to Summary Table

Table 5-469. Instance Table

Instance Name	Physical Address
CPSW0	5282 2308h + formula

Figure 5-230. CPSW_NC_ETH_MAC_PN_SA_L_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_15_8							
R/W							
0h							

Table 5-470. CPSW_NC_ETH_MAC_PN_SA_L_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	MACSRCADDR_7_0	R/W	0h	Source Address bits 7:0
7:0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15:8

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5.2.2.150 CPSW_NC_ETH_MAC_PN_SA_H_REG_J Register

5.2.2.150.1 CPSW_NC_ETH_MAC_PN_SA_H_REG_J Register (Offset = 2230Ch) [reset = 0h]

Enet Port N Tx Pause Frame Source Address High

Return to Summary Table

Table 5-471. Instance Table

Instance Name	Physical Address
CPSW0	5282 230Ch + formula

Figure 5-231. CPSW_NC_ETH_MAC_PN_SA_H_REG_j Name Register

31	30	29	28	27	26	25	24
MACSRCADDR_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
MACSRCADDR_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
MACSRCADDR_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
MACSRCADDR_47_40							
R/W							
0h							

Table 5-472. CPSW_NC_ETH_MAC_PN_SA_H_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23:16
23:16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31:24
15:8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39:32
7:0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47:40

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5.2.2.151 CPSW_NC_ETH_MAC_PN_TS_CTL_REG_J Register

5.2.2.151.1 CPSW_NC_ETH_MAC_PN_TS_CTL_REG_J Register (Offset = 22310h) [reset = 0h]

Enet Port N Time Sync Control

Return to Summary Table

Table 5-473. Instance Table

Instance Name	Physical Address
CPSW0	5282 2310h + formula

Figure 5-232. CPSW_NC_ETH_MAC_PN_TS_CTL_REG_j Name Register

31	30	29	28	27	26	25	24
TS_MSG_TYPE_EN							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_MSG_TYPE_EN							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN
NONE				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-474. CPSW_NC_ETH_MAC_PN_TS_CTL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable - Each bit in this field enables the corresponding message type in receive and transmit time sync messages (Bit 0 enables message type 0 etc.)
15:12	RESERVED	NONE	0h	Reserved
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Synce Transmit Annex E Enable
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Synce Receive Annex E Enable
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 Enable (transmit and receive)
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Synce Transmit Annex D Enable
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Synce Transmit Annex F Enable
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Synce Receive Annex D Enable
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable

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Table 5-474. CPSW_NC_ETH_MAC_PN_TS_CTL_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Synce Receive Annex F Enable

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5.2.2.152 CPSW_NC_ETH_MAC_PN_TS_SEQ_LTYPE_REG_J Register

5.2.2.152.1 CPSW_NC_ETH_MAC_PN_TS_SEQ_LTYPE_REG_J Register (Offset = 22314h) [reset = 1E0000h]

Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET)

Return to Summary Table

Table 5-475. Instance Table

Instance Name	Physical Address
CPSW0	5282 2314h + formula

Figure 5-233. CPSW_NC_ETH_MAC_PN_TS_SEQ_LTYPE_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		TS_SEQ_ID_OFFSET					
NONE		R/W					
0h		1Eh					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_LTYPE1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_LTYPE1							
R/W							
0h							

Table 5-476. CPSW_NC_ETH_MAC_PN_TS_SEQ_LTYPE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset - This is the number of octets that the sequence ID is offset in the tx and rx time sync message header. The minimum value is 6.
15:0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1 - This is the port time sync LTYPE1 value

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5.2.2.153 CPSW_NC_ETH_MAC_PN_TS_VLAN_LTYPE_REG_J Register

5.2.2.153.1 CPSW_NC_ETH_MAC_PN_TS_VLAN_LTYPE_REG_J Register (Offset = 22318h) [reset = 0h]

Enet Port N Time Sync VLAN2 and VLAN2

Return to Summary Table

Table 5-477. Instance Table

Instance Name	Physical Address
CPSW0	5282 2318h + formula

Figure 5-234. CPSW_NC_ETH_MAC_PN_TS_VLAN_LTYPE_REG_j Name Register

31	30	29	28	27	26	25	24
TS_VLAN_LTYPE2							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_VLAN_LTYPE2							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_VLAN_LTYPE1							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_VLAN_LTYPE1							
R/W							
0h							

Table 5-478. CPSW_NC_ETH_MAC_PN_TS_VLAN_LTYPE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2
15:0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1

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5.2.2.154 CPSW_NC_ETH_MAC_PN_TS_CTL_LTYPE2_REG_J Register

5.2.2.154.1 CPSW_NC_ETH_MAC_PN_TS_CTL_LTYPE2_REG_J Register (Offset = 2231Ch) [reset = 0h]

Enet Port N Time Sync Control and LTYPE 2

Return to Summary Table

Table 5-479. Instance Table

Instance Name	Physical Address
CPSW0	5282 231Ch + formula

Figure 5-235. CPSW_NC_ETH_MAC_PN_TS_CTL_LTYPE2_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							TS_UNI_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TS_LTYPE2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_LTYPE2							
R/W							
0h							

Table 5-480. CPSW_NC_ETH_MAC_PN_TS_CTL_LTYPE2_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable
22	TS_320	R/W	0h	Time Sync Destination Port Number 320 Enable
21	TS_319	R/W	0h	Time Sync Destination Port Number 319 Enable
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable
15:0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2 value

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5.2.2.155 CPSW_NC_ETH_MAC_PN_TS_CTL2_REG_J Register

5.2.2.155.1 CPSW_NC_ETH_MAC_PN_TS_CTL2_REG_J Register (Offset = 22320h) [reset = 40000h]

Enet Port N Time Sync Control 2

Return to Summary Table

Table 5-481. Instance Table

Instance Name	Physical Address
CPSW0	5282 2320h + formula

Figure 5-236. CPSW_NC_ETH_MAC_PN_TS_CTL2_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		TS_DOMAIN_OFFSET					
NONE		R/W					
0h		4h					
15	14	13	12	11	10	9	8
TS_MCAST_TYPE_EN							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_MCAST_TYPE_EN							
R/W							
0h							

Table 5-482. CPSW_NC_ETH_MAC_PN_TS_CTL2_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset
15:0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

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5.2.2.156 CPSW_NC_ETH_MAC_PN_MAC_CONTROL_REG_J Register

5.2.2.156.1 CPSW_NC_ETH_MAC_PN_MAC_CONTROL_REG_J Register (Offset = 22330h) [reset = 0h]

Enet Port N Mac Control

Return to Summary Table

Table 5-483. Instance Table

Instance Name	Physical Address
CPSW0	5282 2330h + formula

Figure 5-237. CPSW_NC_ETH_MAC_PN_MAC_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							RX_CMF_EN
NONE							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_CSF_EN	RX_CEF_EN	TX_SHORT_GAP_LIM_EN	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_EN	GIG_FORCE	IFCTL_B
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_ENABLE	RESERVED	
R/W	NONE		R/W	R/W	R/W	NONE	
0h	0h		0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-484. CPSW_NC_ETH_MAC_PN_MAC_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable - Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied/transferred to memory. MAC control frames that are pause frames will be acted upon if enabled in the MacControl register, regardless of the value of pn_rx_cmf_en. Frames transferred to memory due to pn_rx_cmf_en will have the mac_control bit set in their EOP buffer descriptor. 0 - MAC control frames are filtered (but are acted upon if enabled). 1 - MAC control frames are transferred to the host.
23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable - Enables frames or fragments shorter than 64 bytes to be sent to the host. Frames transferred to the host due to pn_rx_csf_en will have the fragment or undersized bit set in their buffer descriptor. Short and fragment frame transfer is not guaranteed for all packet conditions and is best case only. Frames shorter than 33 bytes will be dropped in all cases. Fragments are short frames that contain CRC/align/code errors and undersized are short frames without errors. The pn_rx_cef_en bit must also be set to transfer fragment frames. 0 - Short frames are filtered. 1 - Short frames are transferred to the host.

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Table 5-484. CPSW_NC_ETH_MAC_PN_MAC_CONTROL_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable - Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive buffer descriptor. Frames containing errors will be filtered when this bit is not set. 0 - Frames containing errors are filtered. 1 - Frames containing errors are transferred to the host.
21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable - When set this bit limits the number of short gap packets transmitted to 100ppm. The pn_tx_short_gap_en bit must also be set. Each time a short gap packet is sent, a counter is loaded with 10,000 and decremented on each wireside clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed. This bit is used only with GMII (not XGMII).
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable - Enables the pn_tx_flow_en to be selected from the EXT_TX_FLOW_EN input signal and not from the pn_tx_flow_en bit in this register.
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable - Enables the pn_rx_flow_en to be selected from the EXT_RX_FLOW_EN input signal and not from the pn_rx_flow_en bit in this register.
18	EXT_EN	R/W	0h	External Control Enable - Enables the fullduplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the pn_fullduplex and pn_gig bits in this register. The FULLDUPLEX_MODE bit reflects the actual fullduplex mode selected.
17	GIG_FORCE	R/W	0h	Gigabit Mode Force - This bit is used to force the Enet Mac into gigabit mode if the input GMII_MTCLK has been stopped by the PHY. 0 - GIG mode not forced 1 - GIG mode forced regardless of transmit clock
16	IFCTL_B	R/W	0h	Interface Control B - Intended as a general purpose output bit to be used to control external gaskets associated with the GMII (GMII to RGMII etc).
15	IFCTL_A	R/W	0h	Interface Control A - Intended as a general purpose output bit to be used to control external gaskets associated with the GMII (GMII to RGMII etc).
14:13	RESERVED	NONE	0h	Reserved
12	CRC_TYPE	R/W	0h	Port CRC Type - 0 - Ethernet CRC. 1 - Castagnoli CRC.
11	CMD_IDLE	R/W	0h	Command Idle - 0 - Idle not commanded. 1 - Idle Commanded (read pn_idle in Enet_Pn_Mac_Status).
10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable 0 - Transmit with a short IPG is disabled. 1 - Transmit with a short IPG is enabled.
9:8	RESERVED	NONE	0h	Reserved
7	GIG	R/W	0h	Gigabit Mode - 0 - 10/100 mode. 1 - Gigabit mode (full duplex only) The GIG_OUT output is the value of this bit. This bit is a don't care when pn_xgig is set.
6	TX_PACE	R/W	0h	Transmit Pacing Enable - 0 - Transmit Pacing Disabled. 1 - Transmit Pacing Enabled

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Table 5-484. CPSW_NC_ETH_MAC_PN_MAC_CONTROL_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	GMII_EN	R/W	0h	GMII Enable - 0 - GMII RX and TX held in reset. 1 - GMII RX and TX released from reset. This bit should be written with a logic high before the other bits in this register are written.
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable - Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_Enable bits determine whether or not received pause frames are transferred to memory. 0 - Transmit Flow Control Disabled. Full-duplex mode - Incoming pause frames are not acted upon. 1 - Transmit Flow Control Enabled . Full-duplex mode - Incoming pause frames are acted upon.
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable - 0 - Receive Flow Control Disabled: Half-duplex mode - No flow control generated collisions are sent. Full-duplex mode - No outgoing pause frames are sent. 1 - Receive Flow Control Enabled: Half-duplex mode - Collisions are initiated when receive flow control is triggered. Full-duplex mode - Outgoing pause frames are sent when receive flow control is triggered.
2	MTEST	R/W	0h	Manufacturing Test mode - This bit must be set to allow writes to the Backoff_Test and PauseTimer registers.
1	LOOPBACK	R/W	0h	Loop Back Mode - Loopback mode forces internal fullduplex mode regardless of whether the pn_fullduplex bit is set or not. The pn_loopback bit should be changed only when pn_gmii_en is de-asserted. Loopback is used only with GMII (not XGMII). Loopback is not compatible with timestamp operations (CPTS). 0 - Loop Back Mode disabled. 1 - Loop Back Mode enabled.
0	FULLDUPLEX	R/W	0h	Full Duplex mode - Gigabit mode forces fullduplex mode regardless of whether the pn_fullduplex bit is set or not. The FULLDUPLEX_OUT output is the value of this register bit. 0 - half duplex mode. 1 - full duplex mode.

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5.2.2.157 CPSW_NC_ETH_MAC_PN_MAC_STATUS_REG_J Register

5.2.2.157.1 CPSW_NC_ETH_MAC_PN_MAC_STATUS_REG_J Register (Offset = 22334h) [reset = D0000000h]

Enet Port N Mac Status

Return to Summary Table

Table 5-485. Instance Table

Instance Name	Physical Address
CPSW0	5282 2334h + formula

Figure 5-238. CPSW_NC_ETH_MAC_PN_MAC_STATUS_REG_j Name Register

31	30	29	28	27	26	25	24
IDLE	E_IDLE	RESERVED	MAC_TX_IDLE	TORF	TORF_PRI		
R	R	NONE	R	R	R		
1h	1h	0h	1h	0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TX_PFC_FLOW_ACT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_PFC_FLOW_ACT							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
NONE	R	R	R	R	NONE	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-486. CPSW_NC_ETH_MAC_PN_MAC_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	Enet IDLE - The Ethernet port (express and prempt) is in the idle state when high.
30	E_IDLE	R	1h	Express MAC is idle when high
29	RESERVED	NONE	0h	Reserved
28	MAC_TX_IDLE	R	1h	Mac Transmit Idle - Both Prempt (if iet_incl) and Express MAC Transmit are in idle state.The transmit clock must be running for this to go idle.
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26:24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 0x7 to clear.
23:16	TX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0).
15:8	RX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0).
7	RESERVED	NONE	0h	Reserved
6	EXT_TX_FLOW_EN	R	0h	External Transmit Flow Control Enable - This is the value of the EXT_TX_FLOW_EN input bit.
5	EXT_RX_FLOW_EN	R	0h	External Receive Flow Control Enable - This is the value of the EXT_RX_FLOW_EN input bit.
4	EXT_GIG	R	0h	External GIG - This is the value of the EXT_GIG input bit.
3	EXT_FULLDUPLEX	R	0h	External Fullduplex - This is the value of the EXT_FULLDUPLEX input bit.

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Table 5-486. CPSW_NC_ETH_MAC_PN_MAC_STATUS_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	NONE	0h	Reserved
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active - When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active - When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.

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5.2.2.158 CPSW_NC_ETH_MAC_PN_MAC_SOFT_RESET_REG_J Register

5.2.2.158.1 CPSW_NC_ETH_MAC_PN_MAC_SOFT_RESET_REG_J Register (Offset = 22338h) [reset = 0h]

Enet Port N Mac Soft Reset

Return to Summary Table

Table 5-487. Instance Table

Instance Name	Physical Address
CPSW0	5282 2338h + formula

Figure 5-239. CPSW_NC_ETH_MAC_PN_MAC_SOFT_RESET_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 5-488. CPSW_NC_ETH_MAC_PN_MAC_SOFT_RESET_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Software reset

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5.2.2.159 CPSW_NC_ETH_MAC_PN_MAC_BOFFTEST_REG_J Register

5.2.2.159.1 CPSW_NC_ETH_MAC_PN_MAC_BOFFTEST_REG_J Register (Offset = 2233Ch) [reset = 0h]

Enet Port N Mac Backoff Test

Return to Summary Table

Table 5-489. Instance Table

Instance Name	Physical Address
CPSW0	5282 233Ch + formula

Figure 5-240. CPSW_NC_ETH_MAC_PN_MAC_BOFFTEST_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED	PACEVAL					RNDNUM	
NONE	R/W					R/W	
0h	0h					0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RNDNUM							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COLL_COUNT				RESERVED		TX_BACKOFF	
R				NONE		R	
0h				0h		0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TX_BACKOFF							
R							
0h							

Table 5-490. CPSW_NC_ETH_MAC_PN_MAC_BOFFTEST_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	NONE	0h	Reserved
30:26	PACEVAL	R/W	0h	Pacing Current Value - A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes paceval to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause paceval to be decremented down to zero. When paceval is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce capture effects improving overall network bandwidth.
25:16	RNDNUM	R/W	0h	Backoff Random Number Generator - This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when pn_mtest has previously been set. Reading this field returns the generator's current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.
15:12	COLL_COUNT	R	0h	Collision Count - The number of collisions the current frame has experienced.
11:10	RESERVED	NONE	0h	Reserved
9:0	TX_BACKOFF	R	0h	Backoff Count - This field allows the current value of the backoff counter to be observed for test purposes. This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision.

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5.2.2.160 CPSW_NC_ETH_MAC_PN_MAC_RX_PAUSETIMER_REG_J Register

5.2.2.160.1 CPSW_NC_ETH_MAC_PN_MAC_RX_PAUSETIMER_REG_J Register (Offset = 22340h) [reset = 0h]

Enet Port N 802.3 Receive Pause Timer

Return to Summary Table

Table 5-491. Instance Table

Instance Name	Physical Address
CPSW0	5282 2340h + formula

Figure 5-241. CPSW_NC_ETH_MAC_PN_MAC_RX_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX_PAUSETIMER							
R/W							
0h							

Table 5-492. CPSW_NC_ETH_MAC_PN_MAC_RX_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value - This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Enet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1Qbb Priority Based Flow Control (PFC).

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5.2.2.161 CPSW_NC_ETH_MAC_PN_MAC_RXN_PAUSETIMER_REG_J_K Register

5.2.2.161.1 CPSW_NC_ETH_MAC_PN_MAC_RXN_PAUSETIMER_REG_J_K Register (Offset = 22350h) [reset = 0h]

Enet Port N PFC Priority 0 Rx Pause Timer

Return to Summary Table

Table 5-493. Instance Table

Instance Name	Physical Address
CPSW0	5282 2350h + formula

Figure 5-242. CPSW_NC_ETH_MAC_PN_MAC_RXN_PAUSETIMER_REG_j_k Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RX0_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
RX0_PAUSETIMER							
R/W							
0h							

Table 5-494. CPSW_NC_ETH_MAC_PN_MAC_RXN_PAUSETIMER_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	RX0_PAUSETIMER	R/W	0h	Rx N Pause Timer Value - This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Enet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

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5.2.2.162 CPSW_NC_ETH_MAC_PN_MAC_TX_PAUSETIMER_REG_J Register

5.2.2.162.1 CPSW_NC_ETH_MAC_PN_MAC_TX_PAUSETIMER_REG_J Register (Offset = 22370h) [reset = 0h]

Enet Port N 802.3 Tx Pause Timer

Return to Summary Table

Table 5-495. Instance Table

Instance Name	Physical Address
CPSW0	5282 2370h + formula

Figure 5-243. CPSW_NC_ETH_MAC_PN_MAC_TX_PAUSETIMER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX_PAUSETIMER							
R/W							
0h							

Table 5-496. CPSW_NC_ETH_MAC_PN_MAC_TX_PAUSETIMER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_PAUSETIMER	R/W	0h	802.3 Tx Pause Timer Value - This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

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5.2.2.163 CPSW_NC_ETH_MAC_PN_MAC_TX0_PAUSETIMER_REG_J_K Register

5.2.2.163.1 CPSW_NC_ETH_MAC_PN_MAC_TX0_PAUSETIMER_REG_J_K Register (Offset = 22380h) [reset = 0h]

Enet Port N PFC Priority 0 Tx Pause Timer

Return to Summary Table

Table 5-497. Instance Table

Instance Name	Physical Address
CPSW0	5282 2380h + formula

Figure 5-244. CPSW_NC_ETH_MAC_PN_MAC_TX0_PAUSETIMER_REG_j_k Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX0_PAUSETIMER							
R/W							
0h							
7	6	5	4	3	2	1	0
TX0_PAUSETIMER							
R/W							
0h							

Table 5-498. CPSW_NC_ETH_MAC_PN_MAC_TX0_PAUSETIMER_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX0_PAUSETIMER	R/W	0h	PFC Tx N Pause Timer Value - This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC)

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5.2.2.164 CPSW_NC_ETH_MAC_PN_MAC_EMCONTROL_REG_J Register

5.2.2.164.1 CPSW_NC_ETH_MAC_PN_MAC_EMCONTROL_REG_J Register (Offset = 223A0h) [reset = 0h]

Enet Port N Emulation Control

Return to Summary Table

Table 5-499. Instance Table

Instance Name	Physical Address
CPSW0	5282 23A0h + formula

Figure 5-245. CPSW_NC_ETH_MAC_PN_MAC_EMCONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R/W	R/W
0h						0h	0h

Table 5-500. CPSW_NC_ETH_MAC_PN_MAC_EMCONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

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5.2.2.165 CPSW_NC_ETH_MAC_PN_MAC_TX_GAP_REG_J Register

5.2.2.165.1 CPSW_NC_ETH_MAC_PN_MAC_TX_GAP_REG_J Register (Offset = 223A4h) [reset = Ch]

Enet Port N Tx Inter Packet Gap

Return to Summary Table

Table 5-501. Instance Table

Instance Name	Physical Address
CPSW0	5282 23A4h + formula

Figure 5-246. CPSW_NC_ETH_MAC_PN_MAC_TX_GAP_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TX_GAP							
R/W							
Ch							
7	6	5	4	3	2	1	0
TX_GAP							
R/W							
Ch							

Table 5-502. CPSW_NC_ETH_MAC_PN_MAC_TX_GAP_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap - GMII modes - This is the default gap value and only bits 8:0 are used. This can be increased from 12 to increase the gap between packets. XGMII mode - In 10 gigabit mode this is the short gap rate and should be changed to 5000 (0x1388) to get approximately 200ppm faster when short gap is triggered and enabled.

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5.2.2.166 CPSW_NC_ETH_MAC_PN_MAC_PORT_CONFIG_J Register

5.2.2.166.1 CPSW_NC_ETH_MAC_PN_MAC_PORT_CONFIG_J Register (Offset = 223A8h) [reset = 2h]

Enet Port N Port Configuration

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Table 5-503. Instance Table

Instance Name	Physical Address
CPSW0	5282 23A8h + formula

Figure 5-247. CPSW_NC_ETH_MAC_PN_MAC_PORT_CONFIG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						IET	XGMII
NONE						R	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTERVLAN_ROUTES							
R							
2h							

Table 5-504. CPSW_NC_ETH_MAC_PN_MAC_PORT_CONFIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	IET	R	0h	IET support
8	XGMII	R	0h	No XGMII support on this port
7:0	INTERVLAN_ROUTES	R	2h	The number of InterVLAN routes supported on this port (egress)

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5.2.2.167 CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_POINTER_REG_J Register

5.2.2.167.1 CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_POINTER_REG_J Register (Offset = 223ACh) [reset = 0h]

Enet Port N Tx Egress InterVLAN Operation Pointer

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Table 5-505. Instance Table

Instance Name	Physical Address
CPSW0	5282 23ACh + formula

Figure 5-248. CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_POINTER_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						POINTER	
NONE						R/W	
0h						0h	

Table 5-506. CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_POINTER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	POINTER	R/W	0h	InterVLAN location pointer - This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B/C (the InterVLAN locations are accessed by a maibox). Valid pointer locations are 1 to x (where x is the number of locations - pointer location zero is unused). For example, if configured with 2 intervlan routes then only the values of 1 and 2 are valid.

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5.2.2.168 CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_A_REG_J Register

5.2.2.168.1 CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_A_REG_J Register (Offset = 223B0h) [reset = 0h]

Enet Port N Tx Egress InterVLAN A

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Table 5-507. Instance Table

Instance Name	Physical Address
CPSW0	5282 23B0h + formula

Figure 5-249. CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_A_REG_j Name Register

31	30	29	28	27	26	25	24
DA_23_16							
R/W							
0h							
23	22	21	20	19	18	17	16
DA_31_24							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_39_32							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_47_40							
R/W							
0h							

Table 5-508. CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_A_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DA_23_16	R/W	0h	Destination Address bits 23:16
23:16	DA_31_24	R/W	0h	Destination Address bits 31:24
15:8	DA_39_32	R/W	0h	Destination Address bits 39:32
7:0	DA_47_40	R/W	0h	Destination Address bits 47:40

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5.2.2.169 CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_B_REG_J Register

5.2.2.169.1 CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_B_REG_J Register (Offset = 223B4h) [reset = 0h]

Enet Port N Tx Egress InterVLAN B

Return to Summary Table

Table 5-509. Instance Table

Instance Name	Physical Address
CPSW0	5282 23B4h + formula

Figure 5-250. CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_B_REG_j Name Register

31	30	29	28	27	26	25	24
SA_39_32							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_47_40							
R/W							
0h							
15	14	13	12	11	10	9	8
DA_7_0							
R/W							
0h							
7	6	5	4	3	2	1	0
DA_15_8							
R/W							
0h							

Table 5-510. CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_B_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_39_32	R/W	0h	Source Address bits 39:32
23:16	SA_47_40	R/W	0h	Source Address bits 47:40
15:8	DA_7_0	R/W	0h	Destination Address bits 7:0
7:0	DA_15_8	R/W	0h	Destination Address bits 15:8

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5.2.2.170 CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_C_REG_J Register

5.2.2.170.1 CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_C_REG_J Register (Offset = 223B8h) [reset = 0h]

Enet Port N Tx Egress InterVLAN C

Return to Summary Table

Table 5-511. Instance Table

Instance Name	Physical Address
CPSW0	5282 23B8h + formula

Figure 5-251. CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_C_REG_j Name Register

31	30	29	28	27	26	25	24
SA_7_0							
R/W							
0h							
23	22	21	20	19	18	17	16
SA_15_8							
R/W							
0h							
15	14	13	12	11	10	9	8
SA_23_16							
R/W							
0h							
7	6	5	4	3	2	1	0
SA_31_24							
R/W							
0h							

Table 5-512. CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_C_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	SA_7_0	R/W	0h	Source Address bits 7:0
23:16	SA_15_8	R/W	0h	Source Address bits 15:8
15:8	SA_23_16	R/W	0h	Source Address bits 23:16
7:0	SA_31_24	R/W	0h	Source Address bits 31:24

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5.2.2.171 CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_D_REG_J Register

5.2.2.171.1 CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_D_REG_J Register (Offset = 223BCh) [reset = 0h]

Enet Port N Tx Egress InterVLAN D

Return to Summary Table

Table 5-513. Instance Table

Instance Name	Physical Address
CPSW0	5282 23BCh + formula

Figure 5-252. CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_D_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DECREMENT_TTL	DEST_FORCE_UNTAGGED_EGRESS	REPLACE_DA_SA	REPLACE_VID	VID			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VID							
R/W							
0h							

Table 5-514. CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_D_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DECREMENT_TTL	R/W	0h	Decrement Time To Live - When set, the Time To Live (TTL) field in the header is decremented. IPV4 - Decrement the TTL byte and update the Header Checksum. IPV6 - Decrement the Hop Limit. note: When this bit is set, the ALE should be configured to send any IPv4/6 packet with a zero or one TTL field to the host with the ALE egress operation ttl_check bit.When this bit is cleared the TTL/Hop Limit fields are not checked or modified.
14	DEST_FORCE_UNTAGGED_EGRESS	R/W	0h	Destination VLAN Force Untagged Egress - When set, this bit indicates that the VLAN should be removed on egress for the routed packet. The replace_vid bit should be set for this bit to be used, otherwise force untagged egress comes from the address lookup engine.
13	REPLACE_DA_SA	R/W	0h	Replace Destination Address and Source Address - When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].
12	REPLACE_VID	R/W	0h	Replace VLAN ID - When set this bit indicates that the VLAN ID should be replaced for the routed packet.
11:0	VID	R/W	0h	VLAN ID

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5.2.2.172 CPSW_NC_EST_FETCH_LOC Register

5.2.2.172.1 CPSW_NC_EST_FETCH_LOC Register (Offset = 32000h) [reset = 0h]

The Revision Register contains the ID and revision information.

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Table 5-515. Instance Table

Instance Name	Physical Address
CPSW0	5283 2000h + formula

Figure 5-253. CPSW_NC_EST_FETCH_LOC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED		LOC					
NONE		R/W					
0h		0h					
15	14	13	12	11	10	9	8
LOC							
R/W							
0h							
7	6	5	4	3	2	1	0
LOC							
R/W							
0h							

Table 5-516. CPSW_NC_EST_FETCH_LOC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	NONE	0h	Reserved
21:0	LOC	R/W	0h	RAM Location

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5.2.2.173 CPSW_NC_CPDMA_REGS_FH_IDVER_REG Register

5.2.2.173.1 CPSW_NC_CPDMA_REGS_FH_IDVER_REG Register (Offset = 34000h) [reset = 18010Ah]

CPDMA FHost IDVER

Return to Summary Table

Table 5-517. Instance Table

Instance Name	Physical Address
CPSW0	5283 4000h + formula

Figure 5-254. CPSW_NC_CPDMA_REGS_FH_IDVER_REG Name Register

31	30	29	28	27	26	25	24
FH_IDVER							
R							
18010Ah							
23	22	21	20	19	18	17	16
FH_IDVER							
R							
18010Ah							
15	14	13	12	11	10	9	8
FH_IDVER							
R							
18010Ah							
7	6	5	4	3	2	1	0
FH_IDVER							
R							
18010Ah							

Table 5-518. CPSW_NC_CPDMA_REGS_FH_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH_IDVER	R	18010Ah	CPDMA FHost IDVER

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5.2.2.174 CPSW_NC_CPDMA_REGS_FH_CONTROL_REG Register

5.2.2.174.1 CPSW_NC_CPDMA_REGS_FH_CONTROL_REG Register (Offset = 34004h) [reset = 0h]

CPDMA FHost Control Register

Return to Summary Table

Table 5-519. Instance Table

Instance Name	Physical Address
CPSW0	5283 4004h + formula

Figure 5-255. CPSW_NC_CPDMA_REGS_FH_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FH_EN
NONE							R/W
0h							0h

Table 5-520. CPSW_NC_CPDMA_REGS_FH_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FH_EN	R/W	0h	FHost Enable 0 - Disabled 1 - Enabled

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5.2.2.175 CPSW_NC_CPDMA_REGS_FH_TEARDOWN_REG Register

5.2.2.175.1 CPSW_NC_CPDMA_REGS_FH_TEARDOWN_REG Register (Offset = 34008h) [reset = 0h]

CPDMA FHost Teardown Register

Return to Summary Table

Table 5-521. Instance Table

Instance Name	Physical Address
CPSW0	5283 4008h + formula

Figure 5-256. CPSW_NC_CPDMA_REGS_FH_TEARDOWN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							

23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							

15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							

7	6	5	4	3	2	1	0
RESERVED					FH_TDN_CH		
NONE					R/W		
0h					0h		

Table 5-522. CPSW_NC_CPDMA_REGS_FH_TEARDOWN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FH_TDN_CH	R/W	0h	CPDMA FHost Teardown Channel - FHost channel teardown is commanded by writing the encoded value of the channel to be torn down. The teardown register is read as zero. 000 - teardown channel 0 ... 111 - teardown channel 7

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5.2.2.176 CPSW_NC_CPDMA_REGS_FH_CONTROL2_REG Register

5.2.2.176.1 CPSW_NC_CPDMA_REGS_FH_CONTROL2_REG Register (Offset = 3400Ch) [reset = 0h]

CPDMA FHost Control Two Register

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Table 5-523. Instance Table

Instance Name	Physical Address
CPSW0	5283 400Ch + formula

Figure 5-257. CPSW_NC_CPDMA_REGS_FH_CONTROL2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH_EOQ_INT							
R/W							
0h							

Table 5-524. CPSW_NC_CPDMA_REGS_FH_CONTROL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	FH_EOQ_INT	R/W	0h	FHost Interrupt on EOQ only - When set, a corresponding channel issues an FH_PEND[7:0] interrupt only on end of queue (EOQ). When clear, a corresponding channel issues an interrupt at every end of packet (EOP).

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5.2.2.177 CPSW_NC_CPDMA_REGS_TH_IDVER_REG Register

5.2.2.177.1 CPSW_NC_CPDMA_REGS_TH_IDVER_REG Register (Offset = 34010h) [reset = 18010Ah]

CPDMA THost IDVER

Return to Summary Table

Table 5-525. Instance Table

Instance Name	Physical Address
CPSW0	5283 4010h + formula

Figure 5-258. CPSW_NC_CPDMA_REGS_TH_IDVER_REG Name Register

31	30	29	28	27	26	25	24
TH_IDVER							
R							
18010Ah							
23	22	21	20	19	18	17	16
TH_IDVER							
R							
18010Ah							
15	14	13	12	11	10	9	8
TH_IDVER							
R							
18010Ah							
7	6	5	4	3	2	1	0
TH_IDVER							
R							
18010Ah							

Table 5-526. CPSW_NC_CPDMA_REGS_TH_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH_IDVER	R	18010Ah	CPDMA THost IDVER

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5.2.2.178 CPSW_NC_CPDMA_REGS_TH_CONTROL_REG Register

5.2.2.178.1 CPSW_NC_CPDMA_REGS_TH_CONTROL_REG Register (Offset = 34014h) [reset = 0h]

CPDMA THost Control Register

Return to Summary Table

Table 5-527. Instance Table

Instance Name	Physical Address
CPSW0	5283 4014h + formula

Figure 5-259. CPSW_NC_CPDMA_REGS_TH_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TH_EN
NONE							R/W
0h							0h

Table 5-528. CPSW_NC_CPDMA_REGS_TH_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TH_EN	R/W	0h	THost DMA Enable 0 - Disabled 1 - Enabled

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5.2.2.179 CPSW_NC_CPDMA_REGS_TH_TEARDOWN_REG Register

5.2.2.179.1 CPSW_NC_CPDMA_REGS_TH_TEARDOWN_REG Register (Offset = 34018h) [reset = 0h]

CPDMA THost Teardown Register

Return to Summary Table

Table 5-529. Instance Table

Instance Name	Physical Address
CPSW0	5283 4018h + formula

Figure 5-260. CPSW_NC_CPDMA_REGS_TH_TEARDOWN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					TH_TDN_CH		
NONE					R/W		
0h					0h		

Table 5-530. CPSW_NC_CPDMA_REGS_TH_TEARDOWN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	TH_TDN_CH	R/W	0h	THost Teardown Channel - THost channel teardown is commanded by writing the encoded value of the channel to be torn down. The teardown register is read as zero. 000 - teardown channel 0 ... 111 - teardown channel 7

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5.2.2.180 CPSW_NC_CPDMA_REGS_SOFT_RESET_REG Register

5.2.2.180.1 CPSW_NC_CPDMA_REGS_SOFT_RESET_REG Register (Offset = 3401Ch) [reset = 0h]

CPDMA Soft Reset Register

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Table 5-531. Instance Table

Instance Name	Physical Address
CPSW0	5283 401Ch + formula

Figure 5-261. CPSW_NC_CPDMA_REGS_SOFT_RESET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
NONE							R/W
0h							0h

Table 5-532. CPSW_NC_CPDMA_REGS_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SOFT_RESET	R/W	0h	Software reset - Writing a one to this bit causes the entire CPSW logic to be reset. Software reset occurs when the DMA Controllers are in an idle state to avoid locking up the VBUSP bus. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a one is read, the reset has not yet occurred. If a zero is read then reset has occurred.

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5.2.2.181 CPSW_NC_CPDMA_REGS_CONTROL_REG Register

5.2.2.181.1 CPSW_NC_CPDMA_REGS_CONTROL_REG Register (Offset = 34020h) [reset = 0h]

CPDMA Control Register

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Table 5-533. Instance Table

Instance Name	Physical Address
CPSW0	5283 4020h + formula

Figure 5-262. CPSW_NC_CPDMA_REGS_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							FH_OWNERSHIP
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TH_CH_OVERRIDE	TH_TS_ENCAP	TH_VLAN_ENCAP	TH_CEF	CMD_IDLE	TH_OFFLEN_BLOCK	TH_OWNERSHIP	FH_PTYPE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-534. CPSW_NC_CPDMA_REGS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	FH_OWNERSHIP	R/W	0h	CPDMA FHost Ownership Write Bit Value. 0 - The CPDMA writes the FHost buffer descriptor ownership bit to zero at the end of packet processing as specified in CPPI 3.0. 1 - The CPDMA writes the FHost buffer descriptor ownership bit to one at the end of packet processing. Users who do not use the ownership mechanism can use this mode to preclude the necessity of software having to set this bit each time the buffer descriptor is used. Software must set this bit when building the packet chain.
7	TH_CH_OVERRIDE	R/W	0h	CPDMA THost Channel Classification Match Override Enable 0 - The THost channel is not overridden with the ALE classification match. 1 - The THOST channel is overridden with the lower 3-bits of the ALE classification match value (if a classification match occurred).
6	TH_TS_ENCAP	R/W	0h	CPDMA THost Packet Timestamp Encapsulation 0 - THost packets do not contain a 64-bit timestamp 1 - THost packets contain a 64-bit timestamp prepended to the packet data (32-bit lsword first).
5	TH_VLAN_ENCAP	R/W	0h	CPDMA THost Packet VLAN Encapsulation 0 - THost packets are not VLAN encapsulated 1 - THost packets are VLAN encapsulated

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Table 5-534. CPSW_NC_CPDMA_REGS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TH_CEF	R/W	0h	CPDMA THost Copy Error Frames Enable - Enables THost DMA overrun frames to be transferred to memory (up to the point of buffer overrun). The overrun error bit will be set in the frame EOP buffer descriptor. Overrun frame data will be filtered when thost_cef is not set. THost frames with other error bits set are not affected by this bit. This is related only to frames that overrun on the THost DMA due to buffer limitations. 0 - Frames containing overrun errors are filtered. 1 - Frames containing overrun errors are transferred to memory.
3	CMD_IDLE	R/W	0h	CPDMA Command Idle 0 - Idle not commanded 1 - Idle Commanded (read idle in CPDMA_Status register)
2	TH_OFFLEN_BLOCK	R/W	0h	CPDMA THost Offset/Length word write block 0 - Do not block the DMA writes to the THost buffer descriptor offset/buffer length word. The offset/buffer length word is written as specified in CPPI 3.0. 1 - Block all CPDMA DMA controller writes to the THost buffer descriptor offset/buffer length words during CPPI packet processing. When this bit is set, the CPDMA will never write the third word to any THost buffer descriptor.
1	TH_OWNERSHIP	R/W	0h	CPDMA THost Ownership Write Bit Value 0 - The CPDMA writes the THost buffer descriptor ownership bit to zero at the end of packet processing as specified in CPPI 3.0. 1 - The CPDMA writes the THost buffer descriptor ownership bit to one at the end of packet processing. Users who do not use the ownership mechanism can use this mode to preclude the necessity of software having to set this bit each time the buffer descriptor is used. Software must set this bit when building the packet chain.
0	FH_PTYPE	R/W	0h	CPDMA FHost Queue Priority Type 0 - The queue uses a round robin scheme to select the next channel. 1 - The queue uses a fixed (channel 7 highest priority) priority scheme to select the next channel.

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5.2.2.182 CPSW_NC_CPDMA_REGS_STATUS_REG Register

5.2.2.182.1 CPSW_NC_CPDMA_REGS_STATUS_REG Register (Offset = 34024h) [reset = 80000000h]

CPDMA Status Register

Return to Summary Table

Table 5-535. Instance Table

Instance Name	Physical Address
CPSW0	5283 4024h + formula

Figure 5-263. CPSW_NC_CPDMA_REGS_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IDLE	RESERVED						
R	NONE						
1h	0h						
23	22	21	20	19	18	17	16
FH_HOST_ERROR_CODE				RESERVED	FH_ERR_CH		
R				NONE	R		
0h				0h	0h		
15	14	13	12	11	10	9	8
TH_HOST_ERROR_CODE				RESERVED	TH_ERR_CH		
R				NONE	R		
0h				0h	0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-536. CPSW_NC_CPDMA_REGS_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	CPDMA Idle Status Bit - Indicates when set that the CPDMA is not transferring a packet FHost or THost.
30:24	RESERVED	NONE	0h	Reserved
23:20	FH_HOST_ERROR_CODE	R	0h	CPDMA FHost Error Code - This field is set to indicate CPDMA detected FHost DMA related host errors. The host should read this field after a HOST_ERR_INT to determine the error. Host error Interrupts require hardware reset in order to recover. A zero packet length is an error, but it is not detected. 0000 - No error 0001 - SOP error 0010 - Ownership bit not set in SOP buffer 0011 - Zero Next Buffer Descriptor Pointer Without EOP 0100 - Zero Buffer Pointer 0101 - Zero Buffer Length 0110 - Packet Length Error (sum of buffers < packet length) 0111 - reserved ... 1111 - reserved
19	RESERVED	NONE	0h	Reserved
18:16	FH_ERR_CH	R	0h	CPDMA FHost Error Channel - This field indicates the FHost channel that had a host error. 000 - The host error occurred on TX channel 0 ... 111 - The host error occurred on TX channel 7

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Table 5-536. CPSW_NC_CPDMA_REGS_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	TH_HOST_ERROR_CODE	R	0h	CPDMA THost Error Code - This field is set to indicate CPDMA detected RX DMA related host errors. The host should read this field after a HOST_ERR_INT to determine the error. Host error Interrupts require hardware reset in order to recover. 0000 - No error 0001 - reserved 0010 - Ownership bit not set in input buffer. 0011 - reserved 0100 - Zero Buffer Pointer. 0101 - Zero buffer length on non-SOP descriptor 0110 - SOP buffer length not greater than offset ... 1111 - reserved
11	RESERVED	NONE	0h	Reserved
10:8	TH_ERR_CH	R	0h	CPDMA THost Host Error Channel - This field indicates which THost channel had a host error. 000 - The host error occurred on THost channel 0 ... 111 - The host error occurred on RX channel 7
7:0	RESERVED	NONE	0h	Reserved

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5.2.2.183 CPSW_NC_CPDMA_REGS_TH_BUFFER_OFFSET_REG Register

5.2.2.183.1 CPSW_NC_CPDMA_REGS_TH_BUFFER_OFFSET_REG Register (Offset = 34028h) [reset = 0h]

CPDMA THost Buffer Offset Register

Return to Summary Table

Table 5-537. Instance Table

Instance Name	Physical Address
CPSW0	5283 4028h + formula

Figure 5-264. CPSW_NC_CPDMA_REGS_TH_BUFFER_OFFSET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				TH_BUFFER_OFFSET			
NONE				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TH_BUFFER_OFFSET							
R/W							
0h							

Table 5-538. CPSW_NC_CPDMA_REGS_TH_BUFFER_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:0	TH_BUFFER_OFFSET	R/W	0h	CPDMA THost Buffer Offset Value - The thost_buffer_offset will be written by the port into each frame SOP buffer descriptor buffer_offset field. The frame data will begin after the thost_buffer_offset value of bytes. A value of 0x0 indicates that there are no unused bytes at the beginning of the data and that valid data begins on the first byte of the buffer. A value of 0xF (decimal 15) indicates that the first 15 bytes of the buffer are to be ignored by the port and that valid buffer data starts on byte 16 of the buffer. This value is used for all channels.

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5.2.2.184 CPSW_NC_CPDMA_REGS_EMULATION_CONTROL_REG Register

5.2.2.184.1 CPSW_NC_CPDMA_REGS_EMULATION_CONTROL_REG Register (Offset = 3402Ch) [reset = 0h]

CPDMA Emulation Control Register

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Table 5-539. Instance Table

Instance Name	Physical Address
CPSW0	5283 402Ch + formula

Figure 5-265. CPSW_NC_CPDMA_REGS_EMULATION_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						FREE	SOFT
NONE						R/W	R/W
0h						0h	0h

Table 5-540. CPSW_NC_CPDMA_REGS_EMULATION_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	FREE	R/W	0h	CPDMA Free bit
0	SOFT	R/W	0h	CPDMA Soft bit

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5.2.2.185 CPSW_NC_CPDMA_INT_FH_INTSTAT_RAW_REG Register

5.2.2.185.1 CPSW_NC_CPDMA_INT_FH_INTSTAT_RAW_REG Register (Offset = 34080h) [reset = 0h]

CPDMA FHost Interrupt Status RAW

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Table 5-541. Instance Table

Instance Name	Physical Address
CPSW0	5283 4080h + formula

Figure 5-266. CPSW_NC_CPDMA_INT_FH_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH7_PEND_RAW	FH6_PEND_RAW	FH5_PEND_RAW	FH4_PEND_RAW	FH3_PEND_RAW	FH2_PEND_RAW	FH1_PEND_RAW	FH0_PEND_RAW
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-542. CPSW_NC_CPDMA_INT_FH_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FH7_PEND_RAW	R	0h	CPDMA FHost Channel 7 Interrupt Pending RAW read (before mask)
6	FH6_PEND_RAW	R	0h	CPDMA FHost Channel 6 Interrupt Pending RAW read (before mask)
5	FH5_PEND_RAW	R	0h	CPDMA FHost Channel 5 Interrupt Pending RAW read (before mask)
4	FH4_PEND_RAW	R	0h	CPDMA FHost Channel 4 Interrupt Pending RAW read (before mask)
3	FH3_PEND_RAW	R	0h	CPDMA FHost Channel 3 Interrupt Pending RAW read (before mask)
2	FH2_PEND_RAW	R	0h	CPDMA FHost Channel 2 Interrupt Pending RAW read (before mask)
1	FH1_PEND_RAW	R	0h	CPDMA FHost Channel 1 Interrupt Pending RAW read (before mask)
0	FH0_PEND_RAW	R	0h	CPDMA FHost Channel 0 Interrupt Pending RAW read (before mask)

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5.2.2.186 CPSW_NC_CPDMA_INT_FH_INTSTAT_MASKED_REG Register

5.2.2.186.1 CPSW_NC_CPDMA_INT_FH_INTSTAT_MASKED_REG Register (Offset = 34084h) [reset = 0h]

CPDMA FHost Interrupt Status MASKED

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Table 5-543. Instance Table

Instance Name	Physical Address
CPSW0	5283 4084h + formula

Figure 5-267. CPSW_NC_CPDMA_INT_FH_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH7_PEND_MASKED	FH6_PEND_MASKED	FH5_PEND_MASKED	FH4_PEND_MASKED	FH3_PEND_MASKED	FH2_PEND_MASKED	FH1_PEND_MASKED	FH0_PEND_MASKED
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-544. CPSW_NC_CPDMA_INT_FH_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FH7_PEND_MASKED	R	0h	CPDMA FHost Channel 7 Interrupt Pending MASKED interrupt read
6	FH6_PEND_MASKED	R	0h	CPDMA FHost Channel 6 Interrupt Pending MASKED interrupt read
5	FH5_PEND_MASKED	R	0h	CPDMA FHost Channel 5 Interrupt Pending MASKED interrupt read
4	FH4_PEND_MASKED	R	0h	CPDMA FHost Channel 4 Interrupt Pending MASKED interrupt read
3	FH3_PEND_MASKED	R	0h	CPDMA FHost Channel 3 Interrupt Pending MASKED interrupt read
2	FH2_PEND_MASKED	R	0h	CPDMA FHost Channel 2 Interrupt Pending MASKED interrupt read
1	FH1_PEND_MASKED	R	0h	CPDMA FHost Channel 1 Interrupt Pending MASKED interrupt read
0	FH0_PEND_MASKED	R	0h	CPDMA FHost Channel 0 Interrupt Pending MASKED interrupt read

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5.2.2.187 CPSW_NC_CPDMA_INT_FH_INTMASK_SET_REG Register

5.2.2.187.1 CPSW_NC_CPDMA_INT_FH_INTMASK_SET_REG Register (Offset = 34088h) [reset = 0h]

CPDMA FHost Interrupt Masked SET

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Table 5-545. Instance Table

Instance Name	Physical Address
CPSW0	5283 4088h + formula

Figure 5-268. CPSW_NC_CPDMA_INT_FH_INTMASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH7_PEND_MASKED_SET	FH6_PEND_MASKED_SET	FH5_PEND_MASKED_SET	FH4_PEND_MASKED_SET	FH3_PEND_MASKED_SET	FH2_PEND_MASKED_SET	FH1_PEND_MASKED_SET	FH0_PEND_MASKED_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-546. CPSW_NC_CPDMA_INT_FH_INTMASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FH7_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 7 Interrupt Pending MASKED Set - write one to enable interrupt
6	FH6_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 6 Interrupt Pending MASKED Set - write one to enable interrupt
5	FH5_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 5 Interrupt Pending MASKED Set - write one to enable interrupt
4	FH4_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 4 Interrupt Pending MASKED Set - write one to enable interrupt
3	FH3_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 3 Interrupt Pending MASKED Set - write one to enable interrupt
2	FH2_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 2 Interrupt Pending MASKED Set - write one to enable interrupt
1	FH1_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 1 Interrupt Pending MASKED Set - write one to enable interrupt
0	FH0_PEND_MASKED_SET	R/W1TS	0h	CPDMA FHost Channel 0 Interrupt Pending MASKED Set - write one to enable interrupt

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5.2.2.188 CPSW_NC_CPDMA_INT_FH_INTMASK_CLEAR_REG Register

5.2.2.188.1 CPSW_NC_CPDMA_INT_FH_INTMASK_CLEAR_REG Register (Offset = 3408Ch) [reset = 0h]

CPDMA FHost Interrupt Masked CLR

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Table 5-547. Instance Table

Instance Name	Physical Address
CPSW0	5283 408Ch + formula

Figure 5-269. CPSW_NC_CPDMA_INT_FH_INTMASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
FH7_PEND_MASKED_CLR	FH6_PEND_MASKED_CLR	FH5_PEND_MASKED_CLR	FH4_PEND_MASKED_CLR	FH3_PEND_MASKED_CLR	FH2_PEND_MASKED_CLR	FH1_PEND_MASKED_CLR	FH0_PEND_MASKED_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-548. CPSW_NC_CPDMA_INT_FH_INTMASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	FH7_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 7 Interrupt Pending MASKED Clr - write one to disable interrupt
6	FH6_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 6 Interrupt Pending MASKED Clr - write one to disable interrupt
5	FH5_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 5 Interrupt Pending MASKED Clr - write one to disable interrupt
4	FH4_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 4 Interrupt Pending MASKED Clr - write one to disable interrupt
3	FH3_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 3 Interrupt Pending MASKED Clr - write one to disable interrupt
2	FH2_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 2 Interrupt Pending MASKED Clr - write one to disable interrupt
1	FH1_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 1 Interrupt Pending MASKED Clr - write one to disable interrupt
0	FH0_PEND_MASKED_CLR	R/W1TC	0h	CPDMA FHost Channel 0 Interrupt Pending MASKED Clr - write one to disable interrupt

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5.2.2.189 CPSW_NC_CPDMA_INT_IN_VECTOR_REG Register

5.2.2.189.1 CPSW_NC_CPDMA_INT_IN_VECTOR_REG Register (Offset = 34090h) [reset = 0h]

CPDMA DMA IN Vector

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Table 5-549. Instance Table

Instance Name	Physical Address
CPSW0	5283 4090h + formula

Figure 5-270. CPSW_NC_CPDMA_INT_IN_VECTOR_REG Name Register

31	30	29	28	27	26	25	24
DMA_IN_VECTOR							
R							
0h							
23	22	21	20	19	18	17	16
DMA_IN_VECTOR							
R							
0h							
15	14	13	12	11	10	9	8
DMA_IN_VECTOR							
R							
0h							
7	6	5	4	3	2	1	0
DMA_IN_VECTOR							
R							
0h							

Table 5-550. CPSW_NC_CPDMA_INT_IN_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DMA_IN_VECTOR	R	0h	The value of CPDMA_In_Vector is reset to zero, but will change to the IN_VECTOR input bus value one clock after reset is deasserted. Thereafter, this value will change to a new IN_VECTOR input value one clock after the IN_VECTOR value changes.

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5.2.2.190 CPSW_NC_CPDMA_INT_EOI_VECTOR_REG Register

5.2.2.190.1 CPSW_NC_CPDMA_INT_EOI_VECTOR_REG Register (Offset = 34094h) [reset = 0h]

The CPDMA_EOI_VECTOR(4:0) output bus reflects the value written to this location one VBUSP_GCLK cycle after a write to this location. The EOI_WR signal is asserted for a single clock cycle after a latency of two VBUSP_GCLK cycles when a write is performed to this location.

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Table 5-551. Instance Table

Instance Name	Physical Address
CPSW0	5283 4094h + formula

Figure 5-271. CPSW_NC_CPDMA_INT_EOI_VECTOR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DMA_EOI_VECTOR				
NONE			R/W				
0h			0h				

Table 5-552. CPSW_NC_CPDMA_INT_EOI_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	DMA_EOI_VECTOR	R/W	0h	CPDMA DMA EOI Vector

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5.2.2.191 CPSW_NC_CPDMA_INT_TH_INTSTAT_RAW_REG Register

5.2.2.191.1 CPSW_NC_CPDMA_INT_TH_INTSTAT_RAW_REG Register (Offset = 340A0h) [reset = 0h]

CPDMA Receive Interrupt Status RAW

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Table 5-553. Instance Table

Instance Name	Physical Address
CPSW0	5283 40A0h + formula

Figure 5-272. CPSW_NC_CPDMA_INT_TH_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH7_THRESH_PEND_RAW	TH6_THRESH_PEND_RAW	TH5_THRESH_PEND_RAW	TH4_THRESH_PEND_RAW	TH3_THRESH_PEND_RAW	TH2_THRESH_PEND_RAW	TH1_THRESH_PEND_RAW	TH0_THRESH_PEND_RAW
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TH7_PEND_RAW	TH6_PEND_RAW	TH5_PEND_RAW	TH4_PEND_RAW	TH3_PEND_RAW	TH2_PEND_RAW	TH1_PEND_RAW	TH0_PEND_RAW
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-554. CPSW_NC_CPDMA_INT_TH_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	TH7_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 7 Threshold Interrupt Pending RAW read (before mask)
14	TH6_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 6 Threshold Interrupt Pending RAW read (before mask)
13	TH5_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 5 Threshold Interrupt Pending RAW read (before mask)
12	TH4_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 4 Threshold Interrupt Pending RAW read (before mask)
11	TH3_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 3 Threshold Interrupt Pending RAW read (before mask)
10	TH2_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 2 Threshold Interrupt Pending RAW read (before mask)
9	TH1_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 1 Threshold Interrupt Pending RAW read (before mask)
8	TH0_THRESH_PEND_RAW	R	0h	CPDMA Receive Channel 0 Threshold Interrupt Pending RAW read (before mask)
7	TH7_PEND_RAW	R	0h	CPDMA Receive Channel 7 Interrupt Pending RAW read (before mask)
6	TH6_PEND_RAW	R	0h	CPDMA Receive Channel 6 Interrupt Pending RAW read (before mask)

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Table 5-554. CPSW_NC_CPDMA_INT_TH_INTSTAT_RAW_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TH5_PEND_RAW	R	0h	CPDMA Receive Channel 5 Interrupt Pending RAW read (before mask)
4	TH4_PEND_RAW	R	0h	CPDMA Receive Channel 4 Interrupt Pending RAW read (before mask)
3	TH3_PEND_RAW	R	0h	CPDMA Receive Channel 3 Interrupt Pending RAW read (before mask)
2	TH2_PEND_RAW	R	0h	CPDMA Receive Channel 2 Interrupt Pending RAW read (before mask)
1	TH1_PEND_RAW	R	0h	CPDMA Receive Channel 1 Interrupt Pending RAW read (before mask)
0	TH0_PEND_RAW	R	0h	CPDMA Receive Channel 0 Interrupt Pending RAW read (before mask)

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5.2.2.192 CPSW_NC_CPDMA_INT_TH_INTSTAT_MASKED_REG Register

5.2.2.192.1 CPSW_NC_CPDMA_INT_TH_INTSTAT_MASKED_REG Register (Offset = 340A4h) [reset = 0h]

CPDMA Receive Interrupt Status MASKED

Return to Summary Table

Table 5-555. Instance Table

Instance Name	Physical Address
CPSW0	5283 40A4h + formula

Figure 5-273. CPSW_NC_CPDMA_INT_TH_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH7_THRESH_PEND_MASKED	TH6_THRESH_PEND_MASKED	TH5_THRESH_PEND_MASKED	TH4_THRESH_PEND_MASKED	TH3_THRESH_PEND_MASKED	TH2_THRESH_PEND_MASKED	TH1_THRESH_PEND_MASKED	TH0_THRESH_PEND_MASKED
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TH7_PEND_MASKED	TH6_PEND_MASKED	TH5_PEND_MASKED	TH4_PEND_MASKED	TH3_PEND_MASKED	TH2_PEND_MASKED	TH1_PEND_MASKED	TH0_PEND_MASKED
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-556. CPSW_NC_CPDMA_INT_TH_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	TH7_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 7 Threshold Interrupt Pending MASKED read
14	TH6_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 6 Threshold Interrupt Pending MASKED read
13	TH5_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 5 Threshold Interrupt Pending MASKED read
12	TH4_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 4 Threshold Interrupt Pending MASKED read
11	TH3_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 3 Threshold Interrupt Pending MASKED read
10	TH2_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 2 Threshold Interrupt Pending MASKED read
9	TH1_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 1 Threshold Interrupt Pending MASKED read
8	TH0_THRESH_PEND_MASKED	R	0h	CPDMA Receive Channel 0 Threshold Interrupt Pending MASKED read
7	TH7_PEND_MASKED	R	0h	CPDMA Receive Channel 7 Interrupt Pending MASKED read
6	TH6_PEND_MASKED	R	0h	CPDMA Receive Channel 6 Interrupt Pending MASKED read
5	TH5_PEND_MASKED	R	0h	CPDMA Receive Channel 5 Interrupt Pending MASKED read

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Table 5-556. CPSW_NC_CPDMA_INT_TH_INTSTAT_MASKED_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TH4_PEND_MASKED	R	0h	CPDMA Receive Channel 4 Interrupt Pending MASKED read
3	TH3_PEND_MASKED	R	0h	CPDMA Receive Channel 3 Interrupt Pending MASKED read
2	TH2_PEND_MASKED	R	0h	CPDMA Receive Channel 2 Interrupt Pending MASKED read
1	TH1_PEND_MASKED	R	0h	CPDMA Receive Channel 1 Interrupt Pending MASKED read
0	TH0_PEND_MASKED	R	0h	CPDMA Receive Channel 0 Interrupt Pending MASKED read

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5.2.2.193 CPSW_NC_CPDMA_INT_TH_INTMASK_SET_REG Register

5.2.2.193.1 CPSW_NC_CPDMA_INT_TH_INTMASK_SET_REG Register (Offset = 340A8h) [reset = 0h]

CPDMA THost Interrupt Masked SET

Return to Summary Table

Table 5-557. Instance Table

Instance Name	Physical Address
CPSW0	5283 40A8h + formula

Figure 5-274. CPSW_NC_CPDMA_INT_TH_INTMASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH7_THRESH_PEND_MASKED_SET	TH6_THRESH_PEND_MASKED_SET	TH5_THRESH_PEND_MASKED_SET	TH4_THRESH_PEND_MASKED_SET	TH3_THRESH_PEND_MASKED_SET	TH2_THRESH_PEND_MASKED_SET	TH1_THRESH_PEND_MASKED_SET	TH0_THRESH_PEND_MASKED_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TH7_PEND_MASKED_SET	TH6_PEND_MASKED_SET	TH5_PEND_MASKED_SET	TH4_PEND_MASKED_SET	TH3_PEND_MASKED_SET	TH2_PEND_MASKED_SET	TH1_PEND_MASKED_SET	TH0_PEND_MASKED_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-558. CPSW_NC_CPDMA_INT_TH_INTMASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	TH7_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 7 Threshold Interrupt Pending SET - write one to enable interrupt
14	TH6_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 6 Threshold Interrupt Pending SET - write one to enable interrupt
13	TH5_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 5 Threshold Interrupt Pending SET - write one to enable interrupt
12	TH4_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 4 Threshold Interrupt Pending SET - write one to enable interrupt
11	TH3_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 3 Threshold Interrupt Pending SET - write one to enable interrupt
10	TH2_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 2 Threshold Interrupt Pending SET - write one to enable interrupt
9	TH1_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 1 Threshold Interrupt Pending SET - write one to enable interrupt
8	TH0_THRESH_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 0 Threshold Interrupt Pending SET - write one to enable interrupt
7	TH7_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 7 Interrupt Pending SET - write one to enable interrupt
6	TH6_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 6 Interrupt Pending SET - write one to enable interrupt

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Table 5-558. CPSW_NC_CPDMA_INT_TH_INTMASK_SET_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TH5_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 5 Interrupt Pending SET - write one to enable interrupt
4	TH4_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 4 Interrupt Pending SET - write one to enable interrupt
3	TH3_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 3 Interrupt Pending SET - write one to enable interrupt
2	TH2_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 2 Interrupt Pending SET - write one to enable interrupt
1	TH1_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 1 Interrupt Pending SET - write one to enable interrupt
0	TH0_PEND_MASKED_SET	R/W1TS	0h	CPDMA THost Channel 0 Interrupt Pending SET - write one to enable interrupt

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5.2.2.194 CPSW_NC_CPDMA_INT_TH_INTMASK_CLEAR_REG Register

5.2.2.194.1 CPSW_NC_CPDMA_INT_TH_INTMASK_CLEAR_REG Register (Offset = 340ACh) [reset = 0h]

CPDMA THost Interrupt Masked CLR

Return to Summary Table

Table 5-559. Instance Table

Instance Name	Physical Address
CPSW0	5283 40ACh + formula

Figure 5-275. CPSW_NC_CPDMA_INT_TH_INTMASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH7_THRESH_PEND_MASKED_CLR	TH6_THRESH_PEND_MASKED_CLR	TH5_THRESH_PEND_MASKED_CLR	TH4_THRESH_PEND_MASKED_CLR	TH3_THRESH_PEND_MASKED_CLR	TH2_THRESH_PEND_MASKED_CLR	TH1_THRESH_PEND_MASKED_CLR	TH0_THRESH_PEND_MASKED_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TH7_PEND_MASKED_CLR	TH6_PEND_MASKED_CLR	TH5_PEND_MASKED_CLR	TH4_PEND_MASKED_CLR	TH3_PEND_MASKED_CLR	TH2_PEND_MASKED_CLR	TH1_PEND_MASKED_CLR	TH0_PEND_MASKED_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-560. CPSW_NC_CPDMA_INT_TH_INTMASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	TH7_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 7 Threshold Interrupt Pending CLR - write one to disable interrupt
14	TH6_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 6 Threshold Interrupt Pending CLR - write one to disable interrupt
13	TH5_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 5 Threshold Interrupt Pending CLR - write one to disable interrupt
12	TH4_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 4 Threshold Interrupt Pending CLR - write one to disable interrupt
11	TH3_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 3 Threshold Interrupt Pending CLR - write one to disable interrupt
10	TH2_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 2 Threshold Interrupt Pending CLR - write one to disable interrupt
9	TH1_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 1 Threshold Interrupt Pending CLR - write one to disable interrupt
8	TH0_THRESH_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 0 Threshold Interrupt Pending CLR - write one to disable interrupt
7	TH7_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 7 Interrupt Pending CLR - write one to disable interrupt
6	TH6_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 6 Interrupt Pending CLR - write one to disable interrupt

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Table 5-560. CPSW_NC_CPDMA_INT_TH_INTMASK_CLEAR_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TH5_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 5 Interrupt Pending CLR - write one to disable interrupt
4	TH4_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 4 Interrupt Pending CLR - write one to disable interrupt
3	TH3_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 3 Interrupt Pending CLR - write one to disable interrupt
2	TH2_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 2 Interrupt Pending CLR - write one to disable interrupt
1	TH1_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 1 Interrupt Pending CLR - write one to disable interrupt
0	TH0_PEND_MASKED_CLR	R/W1TC	0h	CPDMA THost Channel 0 Interrupt Pending CLR - write one to disable interrupt

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5.2.2.195 CPSW_NC_CPDMA_INT_INTSTAT_RAW_REG Register

5.2.2.195.1 CPSW_NC_CPDMA_INT_INTSTAT_RAW_REG Register (Offset = 340B0h) [reset = 0h]

CPDMA DMA Interrupt Status RAW

Return to Summary Table

Table 5-561. Instance Table

Instance Name	Physical Address
CPSW0	5283 40B0h + formula

Figure 5-276. CPSW_NC_CPDMA_INT_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						HOST_PEND_RAW	STAT_PEND_RAW
NONE						R	R
0h						0h	0h

Table 5-562. CPSW_NC_CPDMA_INT_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	HOST_PEND_RAW	R	0h	CPDMA HOST Interrupt Pending RAW - read (before mask)
0	STAT_PEND_RAW	R	0h	CPDMA Statistics Interrupt Pending RAW - read (before mask)

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5.2.2.196 CPSW_NC_CPDMA_INT_INTSTAT_MASKED_REG Register

5.2.2.196.1 CPSW_NC_CPDMA_INT_INTSTAT_MASKED_REG Register (Offset = 340B4h) [reset = 0h]

CPDMA DMA Interrupt Status MASKED

Return to Summary Table

Table 5-563. Instance Table

Instance Name	Physical Address
CPSW0	5283 40B4h + formula

Figure 5-277. CPSW_NC_CPDMA_INT_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						HOST_PEND	STAT_PEND
NONE						R	R
0h						0h	0h

Table 5-564. CPSW_NC_CPDMA_INT_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	HOST_PEND	R	0h	CPDMA HOST Interrupt Pending MASKED read
0	STAT_PEND	R	0h	CPDMA Statistics Interrupt Pending MASKED read

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5.2.2.197 CPSW_NC_CPDMA_INT_INTMASK_SET_REG Register

5.2.2.197.1 CPSW_NC_CPDMA_INT_INTMASK_SET_REG Register (Offset = 340B8h) [reset = 0h]

CPDMA DMA Interrupt Status SET

Return to Summary Table

Table 5-565. Instance Table

Instance Name	Physical Address
CPSW0	5283 40B8h + formula

Figure 5-278. CPSW_NC_CPDMA_INT_INTMASK_SET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						HOST_PEND_MASKED_SET	STAT_PEND_MASKED_SET
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 5-566. CPSW_NC_CPDMA_INT_INTMASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	HOST_PEND_MASKED_SET	R/W1TS	0h	CPDMA HOST Interrupt Masked SET - write one to enable interrupt
0	STAT_PEND_MASKED_SET	R/W1TS	0h	CPDMA Statistics Interrupt Masked SET - write one to enable interrupt

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5.2.2.198 CPSW_NC_CPDMA_INT_INTMASK_CLEAR_REG Register

5.2.2.198.1 CPSW_NC_CPDMA_INT_INTMASK_CLEAR_REG Register (Offset = 340BCh) [reset = 0h]

CPDMA DMA Interrupt Status CLR

Return to Summary Table

Table 5-567. Instance Table

Instance Name	Physical Address
CPSW0	5283 40BCh + formula

Figure 5-279. CPSW_NC_CPDMA_INT_INTMASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						HOST_PEND_MASKED_CLR	STAT_PEND_MASKED_CLR
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 5-568. CPSW_NC_CPDMA_INT_INTMASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	HOST_PEND_MASKED_CLR	R/W1TS	0h	CPDMA HOST Interrupt Masked CLR - write one to disable interrupt
0	STAT_PEND_MASKED_CLR	R/W1TS	0h	CPDMA Statistics Interrupt Masked CLR - write one to disable interrupt

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5.2.2.199 CPSW_NC_CPDMA_INT_TH0_PENDTHRESH_REG Register

5.2.2.199.1 CPSW_NC_CPDMA_INT_TH0_PENDTHRESH_REG Register (Offset = 340C0h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to Summary Table

Table 5-569. Instance Table

Instance Name	Physical Address
CPSW0	5283 40C0h + formula

Figure 5-280. CPSW_NC_CPDMA_INT_TH0_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH0_PENDTHRESH							
R/W							
0h							

Table 5-570. CPSW_NC_CPDMA_INT_TH0_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH0_PENDTHRESH	R/W	0h	This field contains the threshold value for issuing threshold pending interrupts (when enabled)

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5.2.2.200 CPSW_NC_CPDMA_INT_TH1_PENDTHRESH_REG Register

5.2.2.200.1 CPSW_NC_CPDMA_INT_TH1_PENDTHRESH_REG Register (Offset = 340C4h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to Summary Table

Table 5-571. Instance Table

Instance Name	Physical Address
CPSW0	5283 40C4h + formula

Figure 5-281. CPSW_NC_CPDMA_INT_TH1_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH1_PENDTHRESH							
R/W							
0h							

Table 5-572. CPSW_NC_CPDMA_INT_TH1_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH1_PENDTHRESH	R/W	0h	This field contains the threshold value for issuing threshold pending interrupts (when enabled)

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5.2.2.201 CPSW_NC_CPDMA_INT_TH2_PENDTHRESH_REG Register

5.2.2.201.1 CPSW_NC_CPDMA_INT_TH2_PENDTHRESH_REG Register (Offset = 340C8h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to Summary Table

Table 5-573. Instance Table

Instance Name	Physical Address
CPSW0	5283 40C8h + formula

Figure 5-282. CPSW_NC_CPDMA_INT_TH2_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH2_PENDTHRESH							
R/W							
0h							

Table 5-574. CPSW_NC_CPDMA_INT_TH2_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH2_PENDTHRESH	R/W	0h	This field contains the threshold value for issuing threshold pending interrupts (when enabled)

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5.2.2.202 CPSW_NC_CPDMA_INT_TH3_PENDTHRESH_REG Register

5.2.2.202.1 CPSW_NC_CPDMA_INT_TH3_PENDTHRESH_REG Register (Offset = 340CCh) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to Summary Table

Table 5-575. Instance Table

Instance Name	Physical Address
CPSW0	5283 40CCh + formula

Figure 5-283. CPSW_NC_CPDMA_INT_TH3_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH3_PENDTHRESH							
R/W							
0h							

Table 5-576. CPSW_NC_CPDMA_INT_TH3_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH3_PENDTHRESH	R/W	0h	This field contains the threshold value for issuing threshold pending interrupts (when enabled)

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5.2.2.203 CPSW_NC_CPDMA_INT_TH4_PENDTHRESH_REG Register

5.2.2.203.1 CPSW_NC_CPDMA_INT_TH4_PENDTHRESH_REG Register (Offset = 340D0h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to Summary Table

Table 5-577. Instance Table

Instance Name	Physical Address
CPSW0	5283 40D0h + formula

Figure 5-284. CPSW_NC_CPDMA_INT_TH4_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH4_PENDTHRESH							
R/W							
0h							

Table 5-578. CPSW_NC_CPDMA_INT_TH4_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH4_PENDTHRESH	R/W	0h	This field contains the threshold value for issuing threshold pending interrupts (when enabled)

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5.2.2.204 CPSW_NC_CPDMA_INT_TH5_PENDTHRESH_REG Register

5.2.2.204.1 CPSW_NC_CPDMA_INT_TH5_PENDTHRESH_REG Register (Offset = 340D4h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to Summary Table

Table 5-579. Instance Table

Instance Name	Physical Address
CPSW0	5283 40D4h + formula

Figure 5-285. CPSW_NC_CPDMA_INT_TH5_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH5_PENDTHRESH							
R/W							
0h							

Table 5-580. CPSW_NC_CPDMA_INT_TH5_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH5_PENDTHRESH	R/W	0h	This field contains the threshold value for issuing threshold pending interrupts (when enabled)

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5.2.2.205 CPSW_NC_CPDMA_INT_TH6_PENDTHRESH_REG Register

5.2.2.205.1 CPSW_NC_CPDMA_INT_TH6_PENDTHRESH_REG Register (Offset = 340D8h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to Summary Table

Table 5-581. Instance Table

Instance Name	Physical Address
CPSW0	5283 40D8h + formula

Figure 5-286. CPSW_NC_CPDMA_INT_TH6_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH6_PENDTHRESH							
R/W							
0h							

Table 5-582. CPSW_NC_CPDMA_INT_TH6_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH6_PENDTHRESH	R/W	0h	This field contains the threshold value for issuing threshold pending interrupts (when enabled)

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5.2.2.206 CPSW_NC_CPDMA_INT_TH7_PENDTHRESH_REG Register

5.2.2.206.1 CPSW_NC_CPDMA_INT_TH7_PENDTHRESH_REG Register (Offset = 340DCh) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to Summary Table

Table 5-583. Instance Table

Instance Name	Physical Address
CPSW0	5283 40DCh + formula

Figure 5-287. CPSW_NC_CPDMA_INT_TH7_PENDTHRESH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TH7_PENDTHRESH							
R/W							
0h							

Table 5-584. CPSW_NC_CPDMA_INT_TH7_PENDTHRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TH7_PENDTHRESH	R/W	0h	This field contains the threshold value for issuing threshold pending interrupts (when enabled)

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5.2.2.207 CPSW_NC_CPDMA_INT_TH0_FREEBUFFER_REG Register

5.2.2.207.1 CPSW_NC_CPDMA_INT_TH0_FREEBUFFER_REG Register (Offset = 340E0h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to Summary Table

Table 5-585. Instance Table

Instance Name	Physical Address
CPSW0	5283 40E0h + formula

Figure 5-288. CPSW_NC_CPDMA_INT_TH0_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH0_FREEBUFFER							
R/W							
0h							
7	6	5	4	3	2	1	0
TH0_FREEBUFFER							
R/W							
0h							

Table 5-586. CPSW_NC_CPDMA_INT_TH0_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TH0_FREEBUFFER	R/W	0h	This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asseted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing.

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5.2.2.208 CPSW_NC_CPDMA_INT_TH1_FREEBUFFER_REG Register

5.2.2.208.1 CPSW_NC_CPDMA_INT_TH1_FREEBUFFER_REG Register (Offset = 340E4h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to Summary Table

Table 5-587. Instance Table

Instance Name	Physical Address
CPSW0	5283 40E4h + formula

Figure 5-289. CPSW_NC_CPDMA_INT_TH1_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH1_FREEBUFFER							
R/W							
0h							
7	6	5	4	3	2	1	0
TH1_FREEBUFFER							
R/W							
0h							

Table 5-588. CPSW_NC_CPDMA_INT_TH1_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TH1_FREEBUFFER	R/W	0h	This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asseted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing.

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5.2.2.209 CPSW_NC_CPDMA_INT_TH2_FREEBUFFER_REG Register

5.2.2.209.1 CPSW_NC_CPDMA_INT_TH2_FREEBUFFER_REG Register (Offset = 340E8h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to Summary Table

Table 5-589. Instance Table

Instance Name	Physical Address
CPSW0	5283 40E8h + formula

Figure 5-290. CPSW_NC_CPDMA_INT_TH2_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH2_FREEBUFFER							
R/W							
0h							
7	6	5	4	3	2	1	0
TH2_FREEBUFFER							
R/W							
0h							

Table 5-590. CPSW_NC_CPDMA_INT_TH2_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TH2_FREEBUFFER	R/W	0h	This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asseted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing.

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5.2.2.210 CPSW_NC_CPDMA_INT_TH3_FREEBUFFER_REG Register

5.2.2.210.1 CPSW_NC_CPDMA_INT_TH3_FREEBUFFER_REG Register (Offset = 340ECh) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to Summary Table

Table 5-591. Instance Table

Instance Name	Physical Address
CPSW0	5283 40ECh + formula

Figure 5-291. CPSW_NC_CPDMA_INT_TH3_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH3_FREEBUFFER							
R/W							
0h							
7	6	5	4	3	2	1	0
TH3_FREEBUFFER							
R/W							
0h							

Table 5-592. CPSW_NC_CPDMA_INT_TH3_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TH3_FREEBUFFER	R/W	0h	This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asseted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing.

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5.2.2.211 CPSW_NC_CPDMA_INT_TH4_FREEBUFFER_REG Register

5.2.2.211.1 CPSW_NC_CPDMA_INT_TH4_FREEBUFFER_REG Register (Offset = 340F0h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to Summary Table

Table 5-593. Instance Table

Instance Name	Physical Address
CPSW0	5283 40F0h + formula

Figure 5-292. CPSW_NC_CPDMA_INT_TH4_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH4_FREEBUFFER							
R/W							
0h							
7	6	5	4	3	2	1	0
TH4_FREEBUFFER							
R/W							
0h							

Table 5-594. CPSW_NC_CPDMA_INT_TH4_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TH4_FREEBUFFER	R/W	0h	This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asseted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing.

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5.2.2.212 CPSW_NC_CPDMA_INT_TH5_FREEBUFFER_REG Register

5.2.2.212.1 CPSW_NC_CPDMA_INT_TH5_FREEBUFFER_REG Register (Offset = 340F4h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to Summary Table

Table 5-595. Instance Table

Instance Name	Physical Address
CPSW0	5283 40F4h + formula

Figure 5-293. CPSW_NC_CPDMA_INT_TH5_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH5_FREEBUFFER							
R/W							
0h							
7	6	5	4	3	2	1	0
TH5_FREEBUFFER							
R/W							
0h							

Table 5-596. CPSW_NC_CPDMA_INT_TH5_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TH5_FREEBUFFER	R/W	0h	This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asseted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing.

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5.2.2.213 CPSW_NC_CPDMA_INT_TH6_FREEBUFFER_REG Register

5.2.2.213.1 CPSW_NC_CPDMA_INT_TH6_FREEBUFFER_REG Register (Offset = 340F8h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to Summary Table

Table 5-597. Instance Table

Instance Name	Physical Address
CPSW0	5283 40F8h + formula

Figure 5-294. CPSW_NC_CPDMA_INT_TH6_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH6_FREEBUFFER							
R/W							
0h							
7	6	5	4	3	2	1	0
TH6_FREEBUFFER							
R/W							
0h							

Table 5-598. CPSW_NC_CPDMA_INT_TH6_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TH6_FREEBUFFER	R/W	0h	This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asseted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing.

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5.2.2.214 CPSW_NC_CPDMA_INT_TH7_FREEBUFFER_REG Register

5.2.2.214.1 CPSW_NC_CPDMA_INT_TH7_FREEBUFFER_REG Register (Offset = 340FCh) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to Summary Table

Table 5-599. Instance Table

Instance Name	Physical Address
CPSW0	5283 40FCh + formula

Figure 5-295. CPSW_NC_CPDMA_INT_TH7_FREEBUFFER_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
TH7_FREEBUFFER							
R/W							
0h							
7	6	5	4	3	2	1	0
TH7_FREEBUFFER							
R/W							
0h							

Table 5-600. CPSW_NC_CPDMA_INT_TH7_FREEBUFFER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	TH7_FREEBUFFER	R/W	0h	This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asseted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing.

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5.2.2.215 CPSW_NC_CPDMA_SRAM_FH0_HDP_REG Register

5.2.2.215.1 CPSW_NC_CPDMA_SRAM_FH0_HDP_REG Register (Offset = 34200h) [reset = 0h]

CPDMA FHost Channel 0 Head Descriptor Pointer

Return to Summary Table

Table 5-601. Instance Table

Instance Name	Physical Address
CPSW0	5283 4200h + formula

Figure 5-296. CPSW_NC_CPDMA_SRAM_FH0_HDP_REG Name Register

31	30	29	28	27	26	25	24
FH0_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH0_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH0_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH0_HDP							
R/W							
0h							

Table 5-602. CPSW_NC_CPDMA_SRAM_FH0_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH0_HDP	R/W	0h	CPDMA FHost Channel 0 Head Descriptor Pointer

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5.2.2.216 CPSW_NC_CPDMA_SRAM_FH1_HDP_REG Register

5.2.2.216.1 CPSW_NC_CPDMA_SRAM_FH1_HDP_REG Register (Offset = 34204h) [reset = 0h]

CPDMA FHost Channel 1 Head Descriptor Pointer

Return to Summary Table

Table 5-603. Instance Table

Instance Name	Physical Address
CPSW0	5283 4204h + formula

Figure 5-297. CPSW_NC_CPDMA_SRAM_FH1_HDP_REG Name Register

31	30	29	28	27	26	25	24
FH1_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH1_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH1_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH1_HDP							
R/W							
0h							

Table 5-604. CPSW_NC_CPDMA_SRAM_FH1_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH1_HDP	R/W	0h	CPDMA FHost Channel 1 Head Descriptor Pointer

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5.2.2.217 CPSW_NC_CPDMA_SRAM_FH2_HDP_REG Register

5.2.2.217.1 CPSW_NC_CPDMA_SRAM_FH2_HDP_REG Register (Offset = 34208h) [reset = 0h]

CPDMA FHost Channel 2 Head Descriptor Pointer

Return to Summary Table

Table 5-605. Instance Table

Instance Name	Physical Address
CPSW0	5283 4208h + formula

Figure 5-298. CPSW_NC_CPDMA_SRAM_FH2_HDP_REG Name Register

31	30	29	28	27	26	25	24
FH2_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH2_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH2_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH2_HDP							
R/W							
0h							

Table 5-606. CPSW_NC_CPDMA_SRAM_FH2_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH2_HDP	R/W	0h	CPDMA FHost Channel 2 Head Descriptor Pointer

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5.2.2.218 CPSW_NC_CPDMA_SRAM_FH3_HDP_REG Register

5.2.2.218.1 CPSW_NC_CPDMA_SRAM_FH3_HDP_REG Register (Offset = 3420Ch) [reset = 0h]

CPDMA FHost Channel 3 Head Descriptor Pointer

Return to Summary Table

Table 5-607. Instance Table

Instance Name	Physical Address
CPSW0	5283 420Ch + formula

Figure 5-299. CPSW_NC_CPDMA_SRAM_FH3_HDP_REG Name Register

31	30	29	28	27	26	25	24
FH3_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH3_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH3_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH3_HDP							
R/W							
0h							

Table 5-608. CPSW_NC_CPDMA_SRAM_FH3_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH3_HDP	R/W	0h	CPDMA FHost Channel 3 Head Descriptor Pointer

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5.2.2.219 CPSW_NC_CPDMA_SRAM_FH4_HDP_REG Register

5.2.2.219.1 CPSW_NC_CPDMA_SRAM_FH4_HDP_REG Register (Offset = 34210h) [reset = 0h]

CPDMA FHost Channel 4 Head Descriptor Pointer

Return to Summary Table

Table 5-609. Instance Table

Instance Name	Physical Address
CPSW0	5283 4210h + formula

Figure 5-300. CPSW_NC_CPDMA_SRAM_FH4_HDP_REG Name Register

31	30	29	28	27	26	25	24
FH4_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH4_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH4_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH4_HDP							
R/W							
0h							

Table 5-610. CPSW_NC_CPDMA_SRAM_FH4_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH4_HDP	R/W	0h	CPDMA FHost Channel 4 Head Descriptor Pointer

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5.2.2.220 CPSW_NC_CPDMA_SRAM_FH5_HDP_REG Register

5.2.2.220.1 CPSW_NC_CPDMA_SRAM_FH5_HDP_REG Register (Offset = 34214h) [reset = 0h]

CPDMA FHost Channel 5 Head Descriptor Pointer

Return to Summary Table

Table 5-611. Instance Table

Instance Name	Physical Address
CPSW0	5283 4214h + formula

Figure 5-301. CPSW_NC_CPDMA_SRAM_FH5_HDP_REG Name Register

31	30	29	28	27	26	25	24
FH5_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH5_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH5_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH5_HDP							
R/W							
0h							

Table 5-612. CPSW_NC_CPDMA_SRAM_FH5_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH5_HDP	R/W	0h	CPDMA FHost Channel 5 Head Descriptor Pointer

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5.2.2.221 CPSW_NC_CPDMA_SRAM_FH6_HDP_REG Register

5.2.2.221.1 CPSW_NC_CPDMA_SRAM_FH6_HDP_REG Register (Offset = 34218h) [reset = 0h]

CPDMA FHost Channel 6 Head Descriptor Pointer

Return to Summary Table

Table 5-613. Instance Table

Instance Name	Physical Address
CPSW0	5283 4218h + formula

Figure 5-302. CPSW_NC_CPDMA_SRAM_FH6_HDP_REG Name Register

31	30	29	28	27	26	25	24
FH6_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH6_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH6_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH6_HDP							
R/W							
0h							

Table 5-614. CPSW_NC_CPDMA_SRAM_FH6_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH6_HDP	R/W	0h	CPDMA FHost Channel 6 Head Descriptor Pointer

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5.2.2.222 CPSW_NC_CPDMA_SRAM_FH7_HDP_REG Register

5.2.2.222.1 CPSW_NC_CPDMA_SRAM_FH7_HDP_REG Register (Offset = 3421Ch) [reset = 0h]

CPDMA FHost Channel 7 Head Descriptor Pointer

Return to Summary Table

Table 5-615. Instance Table

Instance Name	Physical Address
CPSW0	5283 421Ch + formula

Figure 5-303. CPSW_NC_CPDMA_SRAM_FH7_HDP_REG Name Register

31	30	29	28	27	26	25	24
FH7_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH7_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH7_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH7_HDP							
R/W							
0h							

Table 5-616. CPSW_NC_CPDMA_SRAM_FH7_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH7_HDP	R/W	0h	CPDMA FHost Channel 7 Head Descriptor Pointer

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5.2.2.223 CPSW_NC_CPDMA_SRAM_TH0_HDP_REG Register

5.2.2.223.1 CPSW_NC_CPDMA_SRAM_TH0_HDP_REG Register (Offset = 34220h) [reset = 0h]

CPDMA THost Channel 0 Head Descriptor Pointer

Return to Summary Table

Table 5-617. Instance Table

Instance Name	Physical Address
CPSW0	5283 4220h + formula

Figure 5-304. CPSW_NC_CPDMA_SRAM_TH0_HDP_REG Name Register

31	30	29	28	27	26	25	24
TH0_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH0_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH0_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH0_HDP							
R/W							
0h							

Table 5-618. CPSW_NC_CPDMA_SRAM_TH0_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH0_HDP	R/W	0h	CPDMA THost Channel 0 Head Descriptor Pointer

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5.2.2.224 CPSW_NC_CPDMA_SRAM_TH1_HDP_REG Register

5.2.2.224.1 CPSW_NC_CPDMA_SRAM_TH1_HDP_REG Register (Offset = 34224h) [reset = 0h]

CPDMA THost Channel 1 Head Descriptor Pointer

Return to Summary Table

Table 5-619. Instance Table

Instance Name	Physical Address
CPSW0	5283 4224h + formula

Figure 5-305. CPSW_NC_CPDMA_SRAM_TH1_HDP_REG Name Register

31	30	29	28	27	26	25	24
TH1_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH1_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH1_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH1_HDP							
R/W							
0h							

Table 5-620. CPSW_NC_CPDMA_SRAM_TH1_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH1_HDP	R/W	0h	CPDMA THost Channel 1 Head Descriptor Pointer

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5.2.2.225 CPSW_NC_CPDMA_SRAM_TH2_HDP_REG Register

5.2.2.225.1 CPSW_NC_CPDMA_SRAM_TH2_HDP_REG Register (Offset = 34228h) [reset = 0h]

CPDMA THost Channel 2 Head Descriptor Pointer

Return to Summary Table

Table 5-621. Instance Table

Instance Name	Physical Address
CPSW0	5283 4228h + formula

Figure 5-306. CPSW_NC_CPDMA_SRAM_TH2_HDP_REG Name Register

31	30	29	28	27	26	25	24
TH2_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH2_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH2_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH2_HDP							
R/W							
0h							

Table 5-622. CPSW_NC_CPDMA_SRAM_TH2_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH2_HDP	R/W	0h	CPDMA THost Channel 2 Head Descriptor Pointer

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5.2.2.226 CPSW_NC_CPDMA_SRAM_TH3_HDP_REG Register

5.2.2.226.1 CPSW_NC_CPDMA_SRAM_TH3_HDP_REG Register (Offset = 3422Ch) [reset = 0h]

CPDMA THost Channel 3 Head Descriptor Pointer

Return to Summary Table

Table 5-623. Instance Table

Instance Name	Physical Address
CPSW0	5283 422Ch + formula

Figure 5-307. CPSW_NC_CPDMA_SRAM_TH3_HDP_REG Name Register

31	30	29	28	27	26	25	24
TH3_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH3_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH3_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH3_HDP							
R/W							
0h							

Table 5-624. CPSW_NC_CPDMA_SRAM_TH3_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH3_HDP	R/W	0h	CPDMA THost Channel 3 Head Descriptor Pointer

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5.2.2.227 CPSW_NC_CPDMA_SRAM_TH4_HDP_REG Register

5.2.2.227.1 CPSW_NC_CPDMA_SRAM_TH4_HDP_REG Register (Offset = 34230h) [reset = 0h]

CPDMA THost Channel 4 Head Descriptor Pointer

Return to Summary Table

Table 5-625. Instance Table

Instance Name	Physical Address
CPSW0	5283 4230h + formula

Figure 5-308. CPSW_NC_CPDMA_SRAM_TH4_HDP_REG Name Register

31	30	29	28	27	26	25	24
TH4_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH4_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH4_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH4_HDP							
R/W							
0h							

Table 5-626. CPSW_NC_CPDMA_SRAM_TH4_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH4_HDP	R/W	0h	CPDMA THost Channel 4 Head Descriptor Pointer

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5.2.2.228 CPSW_NC_CPDMA_SRAM_TH5_HDP_REG Register

5.2.2.228.1 CPSW_NC_CPDMA_SRAM_TH5_HDP_REG Register (Offset = 34234h) [reset = 0h]

CPDMA THost Channel 5 Head Descriptor Pointer

Return to Summary Table

Table 5-627. Instance Table

Instance Name	Physical Address
CPSW0	5283 4234h + formula

Figure 5-309. CPSW_NC_CPDMA_SRAM_TH5_HDP_REG Name Register

31	30	29	28	27	26	25	24
TH5_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH5_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH5_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH5_HDP							
R/W							
0h							

Table 5-628. CPSW_NC_CPDMA_SRAM_TH5_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH5_HDP	R/W	0h	CPDMA THost Channel 5 Head Descriptor Pointer

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5.2.2.229 CPSW_NC_CPDMA_SRAM_TH6_HDP_REG Register

5.2.2.229.1 CPSW_NC_CPDMA_SRAM_TH6_HDP_REG Register (Offset = 34238h) [reset = 0h]

CPDMA THost Channel 6 Head Descriptor Pointer

Return to Summary Table

Table 5-629. Instance Table

Instance Name	Physical Address
CPSW0	5283 4238h + formula

Figure 5-310. CPSW_NC_CPDMA_SRAM_TH6_HDP_REG Name Register

31	30	29	28	27	26	25	24
TH6_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH6_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH6_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH6_HDP							
R/W							
0h							

Table 5-630. CPSW_NC_CPDMA_SRAM_TH6_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH6_HDP	R/W	0h	CPDMA THost Channel 6 Head Descriptor Pointer

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5.2.2.230 CPSW_NC_CPDMA_SRAM_TH7_HDP_REG Register

5.2.2.230.1 CPSW_NC_CPDMA_SRAM_TH7_HDP_REG Register (Offset = 3423Ch) [reset = 0h]

CPDMA THost Channel 7 Head Descriptor Pointer

Return to Summary Table

Table 5-631. Instance Table

Instance Name	Physical Address
CPSW0	5283 423Ch + formula

Figure 5-311. CPSW_NC_CPDMA_SRAM_TH7_HDP_REG Name Register

31	30	29	28	27	26	25	24
TH7_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH7_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH7_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH7_HDP							
R/W							
0h							

Table 5-632. CPSW_NC_CPDMA_SRAM_TH7_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH7_HDP	R/W	0h	CPDMA THost Channel 7 Head Descriptor Pointer

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5.2.2.231 CPSW_NC_CPDMA_SRAM_FH0_CP_REG Register

5.2.2.231.1 CPSW_NC_CPDMA_SRAM_FH0_CP_REG Register (Offset = 34240h) [reset = 0h]

CPDMA FHost Channel 0 Completion Pointer

Return to Summary Table

Table 5-633. Instance Table

Instance Name	Physical Address
CPSW0	5283 4240h + formula

Figure 5-312. CPSW_NC_CPDMA_SRAM_FH0_CP_REG Name Register

31	30	29	28	27	26	25	24
FH0_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH0_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH0_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH0_CP							
R/W							
0h							

Table 5-634. CPSW_NC_CPDMA_SRAM_FH0_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH0_CP	R/W	0h	CPDMA FHost Channel 0 Completion Pointer

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5.2.2.232 CPSW_NC_CPDMA_SRAM_FH1_CP_REG Register

5.2.2.232.1 CPSW_NC_CPDMA_SRAM_FH1_CP_REG Register (Offset = 34244h) [reset = 0h]

CPDMA FHost Channel 1 Completion Pointer

Return to Summary Table

Table 5-635. Instance Table

Instance Name	Physical Address
CPSW0	5283 4244h + formula

Figure 5-313. CPSW_NC_CPDMA_SRAM_FH1_CP_REG Name Register

31	30	29	28	27	26	25	24
FH1_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH1_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH1_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH1_CP							
R/W							
0h							

Table 5-636. CPSW_NC_CPDMA_SRAM_FH1_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH1_CP	R/W	0h	CPDMA FHost Channel 1 Completion Pointer

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5.2.2.233 CPSW_NC_CPDMA_SRAM_FH2_CP_REG Register

5.2.2.233.1 CPSW_NC_CPDMA_SRAM_FH2_CP_REG Register (Offset = 34248h) [reset = 0h]

CPDMA FHost Channel 2 Completion Pointer

Return to Summary Table

Table 5-637. Instance Table

Instance Name	Physical Address
CPSW0	5283 4248h + formula

Figure 5-314. CPSW_NC_CPDMA_SRAM_FH2_CP_REG Name Register

31	30	29	28	27	26	25	24
FH2_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH2_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH2_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH2_CP							
R/W							
0h							

Table 5-638. CPSW_NC_CPDMA_SRAM_FH2_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH2_CP	R/W	0h	CPDMA FHost Channel 2 Completion Pointer

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5.2.2.234 CPSW_NC_CPDMA_SRAM_FH3_CP_REG Register

5.2.2.234.1 CPSW_NC_CPDMA_SRAM_FH3_CP_REG Register (Offset = 3424Ch) [reset = 0h]

CPDMA FHost Channel 3 Completion Pointer

Return to Summary Table

Table 5-639. Instance Table

Instance Name	Physical Address
CPSW0	5283 424Ch + formula

Figure 5-315. CPSW_NC_CPDMA_SRAM_FH3_CP_REG Name Register

31	30	29	28	27	26	25	24
FH3_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH3_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH3_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH3_CP							
R/W							
0h							

Table 5-640. CPSW_NC_CPDMA_SRAM_FH3_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH3_CP	R/W	0h	CPDMA FHost Channel 3 Completion Pointer

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5.2.2.235 CPSW_NC_CPDMA_SRAM_FH4_CP_REG Register

5.2.2.235.1 CPSW_NC_CPDMA_SRAM_FH4_CP_REG Register (Offset = 34250h) [reset = 0h]

CPDMA FHost Channel 4 Completion Pointer

Return to Summary Table

Table 5-641. Instance Table

Instance Name	Physical Address
CPSW0	5283 4250h + formula

Figure 5-316. CPSW_NC_CPDMA_SRAM_FH4_CP_REG Name Register

31	30	29	28	27	26	25	24
FH4_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH4_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH4_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH4_CP							
R/W							
0h							

Table 5-642. CPSW_NC_CPDMA_SRAM_FH4_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH4_CP	R/W	0h	CPDMA FHost Channel 4 Completion Pointer

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5.2.2.236 CPSW_NC_CPDMA_SRAM_FH5_CP_REG Register

5.2.2.236.1 CPSW_NC_CPDMA_SRAM_FH5_CP_REG Register (Offset = 34254h) [reset = 0h]

CPDMA FHost Channel 5 Completion Pointer

Return to Summary Table

Table 5-643. Instance Table

Instance Name	Physical Address
CPSW0	5283 4254h + formula

Figure 5-317. CPSW_NC_CPDMA_SRAM_FH5_CP_REG Name Register

31	30	29	28	27	26	25	24
FH5_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH5_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH5_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH5_CP							
R/W							
0h							

Table 5-644. CPSW_NC_CPDMA_SRAM_FH5_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH5_CP	R/W	0h	CPDMA FHost Channel 5 Completion Pointer

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5.2.2.237 CPSW_NC_CPDMA_SRAM_FH6_CP_REG Register

5.2.2.237.1 CPSW_NC_CPDMA_SRAM_FH6_CP_REG Register (Offset = 34258h) [reset = 0h]

CPDMA FHost Channel 6 Completion Pointer

Return to Summary Table

Table 5-645. Instance Table

Instance Name	Physical Address
CPSW0	5283 4258h + formula

Figure 5-318. CPSW_NC_CPDMA_SRAM_FH6_CP_REG Name Register

31	30	29	28	27	26	25	24
FH6_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH6_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH6_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH6_CP							
R/W							
0h							

Table 5-646. CPSW_NC_CPDMA_SRAM_FH6_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH6_CP	R/W	0h	CPDMA FHost Channel 6 Completion Pointer

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5.2.2.238 CPSW_NC_CPDMA_SRAM_FH7_CP_REG Register

5.2.2.238.1 CPSW_NC_CPDMA_SRAM_FH7_CP_REG Register (Offset = 3425Ch) [reset = 0h]

CPDMA FHost Channel 7 Completion Pointer

Return to Summary Table

Table 5-647. Instance Table

Instance Name	Physical Address
CPSW0	5283 425Ch + formula

Figure 5-319. CPSW_NC_CPDMA_SRAM_FH7_CP_REG Name Register

31	30	29	28	27	26	25	24
FH7_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
FH7_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
FH7_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
FH7_CP							
R/W							
0h							

Table 5-648. CPSW_NC_CPDMA_SRAM_FH7_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FH7_CP	R/W	0h	CPDMA FHost Channel 7 Completion Pointer

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5.2.2.239 CPSW_NC_CPDMA_SRAM_TH0_CP_REG Register

5.2.2.239.1 CPSW_NC_CPDMA_SRAM_TH0_CP_REG Register (Offset = 34260h) [reset = 0h]

CPDMA THost Channel 0 Completion Pointer

Return to Summary Table

Table 5-649. Instance Table

Instance Name	Physical Address
CPSW0	5283 4260h + formula

Figure 5-320. CPSW_NC_CPDMA_SRAM_TH0_CP_REG Name Register

31	30	29	28	27	26	25	24
TH0_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH0_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH0_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH0_CP							
R/W							
0h							

Table 5-650. CPSW_NC_CPDMA_SRAM_TH0_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH0_CP	R/W	0h	CPDMA THost Channel 0 Completion Pointer

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5.2.2.240 CPSW_NC_CPDMA_SRAM_TH1_CP_REG Register

5.2.2.240.1 CPSW_NC_CPDMA_SRAM_TH1_CP_REG Register (Offset = 34264h) [reset = 0h]

CPDMA THost Channel 1 Completion Pointer

Return to Summary Table

Table 5-651. Instance Table

Instance Name	Physical Address
CPSW0	5283 4264h + formula

Figure 5-321. CPSW_NC_CPDMA_SRAM_TH1_CP_REG Name Register

31	30	29	28	27	26	25	24
TH1_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH1_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH1_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH1_CP							
R/W							
0h							

Table 5-652. CPSW_NC_CPDMA_SRAM_TH1_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH1_CP	R/W	0h	CPDMA THost Channel 1 Completion Pointer

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5.2.2.241 CPSW_NC_CPDMA_SRAM_TH2_CP_REG Register

5.2.2.241.1 CPSW_NC_CPDMA_SRAM_TH2_CP_REG Register (Offset = 34268h) [reset = 0h]

CPDMA THost Channel 2 Completion Pointer

Return to Summary Table

Table 5-653. Instance Table

Instance Name	Physical Address
CPSW0	5283 4268h + formula

Figure 5-322. CPSW_NC_CPDMA_SRAM_TH2_CP_REG Name Register

31	30	29	28	27	26	25	24
TH2_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH2_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH2_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH2_CP							
R/W							
0h							

Table 5-654. CPSW_NC_CPDMA_SRAM_TH2_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH2_CP	R/W	0h	CPDMA THost Channel 2 Completion Pointer

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5.2.2.242 CPSW_NC_CPDMA_SRAM_TH3_CP_REG Register

5.2.2.242.1 CPSW_NC_CPDMA_SRAM_TH3_CP_REG Register (Offset = 3426Ch) [reset = 0h]

CPDMA THost Channel 3 Completion Pointer

Return to Summary Table

Table 5-655. Instance Table

Instance Name	Physical Address
CPSW0	5283 426Ch + formula

Figure 5-323. CPSW_NC_CPDMA_SRAM_TH3_CP_REG Name Register

31	30	29	28	27	26	25	24
TH3_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH3_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH3_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH3_CP							
R/W							
0h							

Table 5-656. CPSW_NC_CPDMA_SRAM_TH3_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH3_CP	R/W	0h	CPDMA THost Channel 3 Completion Pointer

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5.2.2.243 CPSW_NC_CPDMA_SRAM_TH4_CP_REG Register

5.2.2.243.1 CPSW_NC_CPDMA_SRAM_TH4_CP_REG Register (Offset = 34270h) [reset = 0h]

CPDMA THost Channel 4 Completion Pointer

Return to Summary Table

Table 5-657. Instance Table

Instance Name	Physical Address
CPSW0	5283 4270h + formula

Figure 5-324. CPSW_NC_CPDMA_SRAM_TH4_CP_REG Name Register

31	30	29	28	27	26	25	24
TH4_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH4_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH4_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH4_CP							
R/W							
0h							

Table 5-658. CPSW_NC_CPDMA_SRAM_TH4_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH4_CP	R/W	0h	CPDMA THost Channel 4 Completion Pointer

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5.2.2.244 CPSW_NC_CPDMA_SRAM_TH5_CP_REG Register

5.2.2.244.1 CPSW_NC_CPDMA_SRAM_TH5_CP_REG Register (Offset = 34274h) [reset = 0h]

CPDMA THost Channel 5 Completion Pointer

Return to Summary Table

Table 5-659. Instance Table

Instance Name	Physical Address
CPSW0	5283 4274h + formula

Figure 5-325. CPSW_NC_CPDMA_SRAM_TH5_CP_REG Name Register

31	30	29	28	27	26	25	24
TH5_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH5_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH5_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH5_CP							
R/W							
0h							

Table 5-660. CPSW_NC_CPDMA_SRAM_TH5_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH5_CP	R/W	0h	CPDMA THost Channel 5 Completion Pointer

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5.2.2.245 CPSW_NC_CPDMA_SRAM_TH6_CP_REG Register

5.2.2.245.1 CPSW_NC_CPDMA_SRAM_TH6_CP_REG Register (Offset = 34278h) [reset = 0h]

CPDMA THost Channel 6 Completion Pointer

Return to Summary Table

Table 5-661. Instance Table

Instance Name	Physical Address
CPSW0	5283 4278h + formula

Figure 5-326. CPSW_NC_CPDMA_SRAM_TH6_CP_REG Name Register

31	30	29	28	27	26	25	24
TH6_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH6_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH6_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH6_CP							
R/W							
0h							

Table 5-662. CPSW_NC_CPDMA_SRAM_TH6_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH6_CP	R/W	0h	CPDMA THost Channel 6 Completion Pointer

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5.2.2.246 CPSW_NC_CPDMA_SRAM_TH7_CP_REG Register

5.2.2.246.1 CPSW_NC_CPDMA_SRAM_TH7_CP_REG Register (Offset = 3427Ch) [reset = 0h]

CPDMA THost Channel 7 Completion Pointer

Return to Summary Table

Table 5-663. Instance Table

Instance Name	Physical Address
CPSW0	5283 427Ch + formula

Figure 5-327. CPSW_NC_CPDMA_SRAM_TH7_CP_REG Name Register

31	30	29	28	27	26	25	24
TH7_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TH7_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TH7_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TH7_CP							
R/W							
0h							

Table 5-664. CPSW_NC_CPDMA_SRAM_TH7_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TH7_CP	R/W	0h	CPDMA THost Channel 7 Completion Pointer

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5.2.2.247 CPSW_NC_CPDMA_SRAM_TEST_FH0_HDP_REG Register

5.2.2.247.1 CPSW_NC_CPDMA_SRAM_TEST_FH0_HDP_REG Register (Offset = 34300h) [reset = 0h]

Test CPDMA FHost Channel 0 Head Descriptor Pointer

Return to Summary Table

Table 5-665. Instance Table

Instance Name	Physical Address
CPSW0	5283 4300h + formula

Figure 5-328. CPSW_NC_CPDMA_SRAM_TEST_FH0_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH0_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH0_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH0_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH0_HDP							
R/W							
0h							

Table 5-666. CPSW_NC_CPDMA_SRAM_TEST_FH0_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH0_HDP	R/W	0h	Test CPDMA FHost Channel 0 Head Descriptor Pointer

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5.2.2.248 CPSW_NC_CPDMA_SRAM_TEST_FH1_HDP_REG Register

5.2.2.248.1 CPSW_NC_CPDMA_SRAM_TEST_FH1_HDP_REG Register (Offset = 34304h) [reset = 0h]

Test CPDMA FHost Channel 1 Head Descriptor Pointer

Return to Summary Table

Table 5-667. Instance Table

Instance Name	Physical Address
CPSW0	5283 4304h + formula

Figure 5-329. CPSW_NC_CPDMA_SRAM_TEST_FH1_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH1_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH1_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH1_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH1_HDP							
R/W							
0h							

Table 5-668. CPSW_NC_CPDMA_SRAM_TEST_FH1_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH1_HDP	R/W	0h	Test CPDMA FHost Channel 1 Head Descriptor Pointer

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5.2.2.249 CPSW_NC_CPDMA_SRAM_TEST_FH2_HDP_REG Register

5.2.2.249.1 CPSW_NC_CPDMA_SRAM_TEST_FH2_HDP_REG Register (Offset = 34308h) [reset = 0h]

Test CPDMA FHost Channel 2 Head Descriptor Pointer

Return to Summary Table

Table 5-669. Instance Table

Instance Name	Physical Address
CPSW0	5283 4308h + formula

Figure 5-330. CPSW_NC_CPDMA_SRAM_TEST_FH2_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH2_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH2_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH2_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH2_HDP							
R/W							
0h							

Table 5-670. CPSW_NC_CPDMA_SRAM_TEST_FH2_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH2_HDP	R/W	0h	Test CPDMA FHost Channel 2 Head Descriptor Pointer

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5.2.2.250 CPSW_NC_CPDMA_SRAM_TEST_FH3_HDP_REG Register

5.2.2.250.1 CPSW_NC_CPDMA_SRAM_TEST_FH3_HDP_REG Register (Offset = 3430Ch) [reset = 0h]

Test CPDMA FHost Channel 3 Head Descriptor Pointer

Return to Summary Table

Table 5-671. Instance Table

Instance Name	Physical Address
CPSW0	5283 430Ch + formula

Figure 5-331. CPSW_NC_CPDMA_SRAM_TEST_FH3_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH3_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH3_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH3_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH3_HDP							
R/W							
0h							

Table 5-672. CPSW_NC_CPDMA_SRAM_TEST_FH3_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH3_HDP	R/W	0h	Test CPDMA FHost Channel 3 Head Descriptor Pointer

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5.2.2.251 CPSW_NC_CPDMA_SRAM_TEST_FH4_HDP_REG Register

5.2.2.251.1 CPSW_NC_CPDMA_SRAM_TEST_FH4_HDP_REG Register (Offset = 34310h) [reset = 0h]

Test CPDMA FHost Channel 4 Head Descriptor Pointer

Return to Summary Table

Table 5-673. Instance Table

Instance Name	Physical Address
CPSW0	5283 4310h + formula

Figure 5-332. CPSW_NC_CPDMA_SRAM_TEST_FH4_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH4_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH4_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH4_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH4_HDP							
R/W							
0h							

Table 5-674. CPSW_NC_CPDMA_SRAM_TEST_FH4_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH4_HDP	R/W	0h	Test CPDMA FHost Channel 4 Head Descriptor Pointer

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5.2.2.252 CPSW_NC_CPDMA_SRAM_TEST_FH5_HDP_REG Register

5.2.2.252.1 CPSW_NC_CPDMA_SRAM_TEST_FH5_HDP_REG Register (Offset = 34314h) [reset = 0h]

Test CPDMA FHost Channel 5 Head Descriptor Pointer

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Table 5-675. Instance Table

Instance Name	Physical Address
CPSW0	5283 4314h + formula

Figure 5-333. CPSW_NC_CPDMA_SRAM_TEST_FH5_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH5_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH5_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH5_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH5_HDP							
R/W							
0h							

Table 5-676. CPSW_NC_CPDMA_SRAM_TEST_FH5_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH5_HDP	R/W	0h	Test CPDMA FHost Channel 5 Head Descriptor Pointer

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5.2.2.253 CPSW_NC_CPDMA_SRAM_TEST_FH6_HDP_REG Register

5.2.2.253.1 CPSW_NC_CPDMA_SRAM_TEST_FH6_HDP_REG Register (Offset = 34318h) [reset = 0h]

Test CPDMA FHost Channel 6 Head Descriptor Pointer

Return to Summary Table

Table 5-677. Instance Table

Instance Name	Physical Address
CPSW0	5283 4318h + formula

Figure 5-334. CPSW_NC_CPDMA_SRAM_TEST_FH6_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH6_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH6_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH6_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH6_HDP							
R/W							
0h							

Table 5-678. CPSW_NC_CPDMA_SRAM_TEST_FH6_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH6_HDP	R/W	0h	Test CPDMA FHost Channel 6 Head Descriptor Pointer

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5.2.2.254 CPSW_NC_CPDMA_SRAM_TEST_FH7_HDP_REG Register

5.2.2.254.1 CPSW_NC_CPDMA_SRAM_TEST_FH7_HDP_REG Register (Offset = 3431Ch) [reset = 0h]

Test CPDMA FHost Channel 7 Head Descriptor Pointer

Return to Summary Table

Table 5-679. Instance Table

Instance Name	Physical Address
CPSW0	5283 431Ch + formula

Figure 5-335. CPSW_NC_CPDMA_SRAM_TEST_FH7_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH7_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH7_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH7_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH7_HDP							
R/W							
0h							

Table 5-680. CPSW_NC_CPDMA_SRAM_TEST_FH7_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH7_HDP	R/W	0h	Test CPDMA FHost Channel 7 Head Descriptor Pointer

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5.2.2.255 CPSW_NC_CPDMA_SRAM_TEST_TH0_HDP_REG Register

5.2.2.255.1 CPSW_NC_CPDMA_SRAM_TEST_TH0_HDP_REG Register (Offset = 34320h) [reset = 0h]

Test CPDMA THost Channel 0 Head Descriptor Pointer

Return to Summary Table

Table 5-681. Instance Table

Instance Name	Physical Address
CPSW0	5283 4320h + formula

Figure 5-336. CPSW_NC_CPDMA_SRAM_TEST_TH0_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH0_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH0_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH0_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH0_HDP							
R/W							
0h							

Table 5-682. CPSW_NC_CPDMA_SRAM_TEST_TH0_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH0_HDP	R/W	0h	Test CPDMA THost Channel 0 Head Descriptor Pointer

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5.2.2.256 CPSW_NC_CPDMA_SRAM_TEST_TH1_HDP_REG Register

5.2.2.256.1 CPSW_NC_CPDMA_SRAM_TEST_TH1_HDP_REG Register (Offset = 34324h) [reset = 0h]

Test CPDMA THost Channel 1 Head Descriptor Pointer

Return to Summary Table

Table 5-683. Instance Table

Instance Name	Physical Address
CPSW0	5283 4324h + formula

Figure 5-337. CPSW_NC_CPDMA_SRAM_TEST_TH1_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH1_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH1_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH1_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH1_HDP							
R/W							
0h							

Table 5-684. CPSW_NC_CPDMA_SRAM_TEST_TH1_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH1_HDP	R/W	0h	Test CPDMA THost Channel 1 Head Descriptor Pointer

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5.2.2.257 CPSW_NC_CPDMA_SRAM_TEST_TH2_HDP_REG Register

5.2.2.257.1 CPSW_NC_CPDMA_SRAM_TEST_TH2_HDP_REG Register (Offset = 34328h) [reset = 0h]

Test CPDMA THost Channel 2 Head Descriptor Pointer

Return to Summary Table

Table 5-685. Instance Table

Instance Name	Physical Address
CPSW0	5283 4328h + formula

Figure 5-338. CPSW_NC_CPDMA_SRAM_TEST_TH2_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH2_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH2_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH2_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH2_HDP							
R/W							
0h							

Table 5-686. CPSW_NC_CPDMA_SRAM_TEST_TH2_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH2_HDP	R/W	0h	Test CPDMA THost Channel 2 Head Descriptor Pointer

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5.2.2.258 CPSW_NC_CPDMA_SRAM_TEST_TH3_HDP_REG Register

5.2.2.258.1 CPSW_NC_CPDMA_SRAM_TEST_TH3_HDP_REG Register (Offset = 3432Ch) [reset = 0h]

Test CPDMA THost Channel 3 Head Descriptor Pointer

Return to Summary Table

Table 5-687. Instance Table

Instance Name	Physical Address
CPSW0	5283 432Ch + formula

Figure 5-339. CPSW_NC_CPDMA_SRAM_TEST_TH3_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH3_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH3_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH3_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH3_HDP							
R/W							
0h							

Table 5-688. CPSW_NC_CPDMA_SRAM_TEST_TH3_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH3_HDP	R/W	0h	Test CPDMA THost Channel 3 Head Descriptor Pointer

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5.2.2.259 CPSW_NC_CPDMA_SRAM_TEST_TH4_HDP_REG Register

5.2.2.259.1 CPSW_NC_CPDMA_SRAM_TEST_TH4_HDP_REG Register (Offset = 34330h) [reset = 0h]

Test CPDMA THost Channel 4 Head Descriptor Pointer

Return to Summary Table

Table 5-689. Instance Table

Instance Name	Physical Address
CPSW0	5283 4330h + formula

Figure 5-340. CPSW_NC_CPDMA_SRAM_TEST_TH4_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH4_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH4_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH4_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH4_HDP							
R/W							
0h							

Table 5-690. CPSW_NC_CPDMA_SRAM_TEST_TH4_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH4_HDP	R/W	0h	Test CPDMA THost Channel 4 Head Descriptor Pointer

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5.2.2.260 CPSW_NC_CPDMA_SRAM_TEST_TH5_HDP_REG Register

5.2.2.260.1 CPSW_NC_CPDMA_SRAM_TEST_TH5_HDP_REG Register (Offset = 34334h) [reset = 0h]

Test CPDMA THost Channel 5 Head Descriptor Pointer

Return to Summary Table

Table 5-691. Instance Table

Instance Name	Physical Address
CPSW0	5283 4334h + formula

Figure 5-341. CPSW_NC_CPDMA_SRAM_TEST_TH5_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH5_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH5_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH5_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH5_HDP							
R/W							
0h							

Table 5-692. CPSW_NC_CPDMA_SRAM_TEST_TH5_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH5_HDP	R/W	0h	Test CPDMA THost Channel 5 Head Descriptor Pointer

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5.2.2.261 CPSW_NC_CPDMA_SRAM_TEST_TH6_HDP_REG Register

5.2.2.261.1 CPSW_NC_CPDMA_SRAM_TEST_TH6_HDP_REG Register (Offset = 34338h) [reset = 0h]

Test CPDMA THost Channel 6 Head Descriptor Pointer

Return to Summary Table

Table 5-693. Instance Table

Instance Name	Physical Address
CPSW0	5283 4338h + formula

Figure 5-342. CPSW_NC_CPDMA_SRAM_TEST_TH6_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH6_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH6_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH6_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH6_HDP							
R/W							
0h							

Table 5-694. CPSW_NC_CPDMA_SRAM_TEST_TH6_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH6_HDP	R/W	0h	Test CPDMA THost Channel 6 Head Descriptor Pointer

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5.2.2.262 CPSW_NC_CPDMA_SRAM_TEST_TH7_HDP_REG Register

5.2.2.262.1 CPSW_NC_CPDMA_SRAM_TEST_TH7_HDP_REG Register (Offset = 3433Ch) [reset = 0h]

Test CPDMA THost Channel 7 Head Descriptor Pointer

Return to Summary Table

Table 5-695. Instance Table

Instance Name	Physical Address
CPSW0	5283 433Ch + formula

Figure 5-343. CPSW_NC_CPDMA_SRAM_TEST_TH7_HDP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH7_HDP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH7_HDP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH7_HDP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH7_HDP							
R/W							
0h							

Table 5-696. CPSW_NC_CPDMA_SRAM_TEST_TH7_HDP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH7_HDP	R/W	0h	Test CPDMA THost Channel 7 Head Descriptor Pointer

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5.2.2.263 CPSW_NC_CPDMA_SRAM_TEST_FH0_CP_REG Register

5.2.2.263.1 CPSW_NC_CPDMA_SRAM_TEST_FH0_CP_REG Register (Offset = 34340h) [reset = 0h]

Test CPDMA FHost Channel 0 Completion Pointer

Return to Summary Table

Table 5-697. Instance Table

Instance Name	Physical Address
CPSW0	5283 4340h + formula

Figure 5-344. CPSW_NC_CPDMA_SRAM_TEST_FH0_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH0_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH0_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH0_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH0_CP							
R/W							
0h							

Table 5-698. CPSW_NC_CPDMA_SRAM_TEST_FH0_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH0_CP	R/W	0h	Test CPDMA FHost Channel 0 Completion Pointer

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5.2.2.264 CPSW_NC_CPDMA_SRAM_TEST_FH1_CP_REG Register

5.2.2.264.1 CPSW_NC_CPDMA_SRAM_TEST_FH1_CP_REG Register (Offset = 34344h) [reset = 0h]

Test CPDMA FHost Channel 1 Completion Pointer

Return to Summary Table

Table 5-699. Instance Table

Instance Name	Physical Address
CPSW0	5283 4344h + formula

Figure 5-345. CPSW_NC_CPDMA_SRAM_TEST_FH1_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH1_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH1_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH1_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH1_CP							
R/W							
0h							

Table 5-700. CPSW_NC_CPDMA_SRAM_TEST_FH1_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH1_CP	R/W	0h	Test CPDMA FHost Channel 1 Completion Pointer

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5.2.2.265 CPSW_NC_CPDMA_SRAM_TEST_FH2_CP_REG Register

5.2.2.265.1 CPSW_NC_CPDMA_SRAM_TEST_FH2_CP_REG Register (Offset = 34348h) [reset = 0h]

Test CPDMA FHost Channel 2 Completion Pointer

Return to Summary Table

Table 5-701. Instance Table

Instance Name	Physical Address
CPSW0	5283 4348h + formula

Figure 5-346. CPSW_NC_CPDMA_SRAM_TEST_FH2_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH2_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH2_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH2_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH2_CP							
R/W							
0h							

Table 5-702. CPSW_NC_CPDMA_SRAM_TEST_FH2_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH2_CP	R/W	0h	Test CPDMA FHost Channel 2 Completion Pointer

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5.2.2.266 CPSW_NC_CPDMA_SRAM_TEST_FH3_CP_REG Register

5.2.2.266.1 CPSW_NC_CPDMA_SRAM_TEST_FH3_CP_REG Register (Offset = 3434Ch) [reset = 0h]

Test CPDMA FHost Channel 3 Completion Pointer

Return to Summary Table

Table 5-703. Instance Table

Instance Name	Physical Address
CPSW0	5283 434Ch + formula

Figure 5-347. CPSW_NC_CPDMA_SRAM_TEST_FH3_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH3_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH3_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH3_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH3_CP							
R/W							
0h							

Table 5-704. CPSW_NC_CPDMA_SRAM_TEST_FH3_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH3_CP	R/W	0h	Test CPDMA FHost Channel 3 Completion Pointer

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5.2.2.267 CPSW_NC_CPDMA_SRAM_TEST_FH4_CP_REG Register

5.2.2.267.1 CPSW_NC_CPDMA_SRAM_TEST_FH4_CP_REG Register (Offset = 34350h) [reset = 0h]

Test CPDMA FHost Channel 4 Completion Pointer

Return to Summary Table

Table 5-705. Instance Table

Instance Name	Physical Address
CPSW0	5283 4350h + formula

Figure 5-348. CPSW_NC_CPDMA_SRAM_TEST_FH4_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH4_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH4_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH4_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH4_CP							
R/W							
0h							

Table 5-706. CPSW_NC_CPDMA_SRAM_TEST_FH4_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH4_CP	R/W	0h	Test CPDMA FHost Channel 4 Completion Pointer

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5.2.2.268 CPSW_NC_CPDMA_SRAM_TEST_FH5_CP_REG Register

5.2.2.268.1 CPSW_NC_CPDMA_SRAM_TEST_FH5_CP_REG Register (Offset = 34354h) [reset = 0h]

Test CPDMA FHost Channel 5 Completion Pointer

Return to Summary Table

Table 5-707. Instance Table

Instance Name	Physical Address
CPSW0	5283 4354h + formula

Figure 5-349. CPSW_NC_CPDMA_SRAM_TEST_FH5_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH5_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH5_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH5_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH5_CP							
R/W							
0h							

Table 5-708. CPSW_NC_CPDMA_SRAM_TEST_FH5_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH5_CP	R/W	0h	Test CPDMA FHost Channel 5 Completion Pointer

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5.2.2.269 CPSW_NC_CPDMA_SRAM_TEST_FH6_CP_REG Register

5.2.2.269.1 CPSW_NC_CPDMA_SRAM_TEST_FH6_CP_REG Register (Offset = 34358h) [reset = 0h]

Test CPDMA FHost Channel 6 Completion Pointer

Return to Summary Table

Table 5-709. Instance Table

Instance Name	Physical Address
CPSW0	5283 4358h + formula

Figure 5-350. CPSW_NC_CPDMA_SRAM_TEST_FH6_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH6_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH6_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH6_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH6_CP							
R/W							
0h							

Table 5-710. CPSW_NC_CPDMA_SRAM_TEST_FH6_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH6_CP	R/W	0h	Test CPDMA FHost Channel 6 Completion Pointer

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5.2.2.270 CPSW_NC_CPDMA_SRAM_TEST_FH7_CP_REG Register

5.2.2.270.1 CPSW_NC_CPDMA_SRAM_TEST_FH7_CP_REG Register (Offset = 3435Ch) [reset = 0h]

Test CPDMA FHost Channel 7 Completion Pointer

Return to Summary Table

Table 5-711. Instance Table

Instance Name	Physical Address
CPSW0	5283 435Ch + formula

Figure 5-351. CPSW_NC_CPDMA_SRAM_TEST_FH7_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_FH7_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_FH7_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_FH7_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_FH7_CP							
R/W							
0h							

Table 5-712. CPSW_NC_CPDMA_SRAM_TEST_FH7_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_FH7_CP	R/W	0h	Test CPDMA FHost Channel 7 Completion Pointer

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5.2.2.271 CPSW_NC_CPDMA_SRAM_TEST_TH0_CP_REG Register

5.2.2.271.1 CPSW_NC_CPDMA_SRAM_TEST_TH0_CP_REG Register (Offset = 34360h) [reset = 0h]

Test CPDMA THost Channel 0 Completion Pointer

Return to Summary Table

Table 5-713. Instance Table

Instance Name	Physical Address
CPSW0	5283 4360h + formula

Figure 5-352. CPSW_NC_CPDMA_SRAM_TEST_TH0_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH0_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH0_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH0_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH0_CP							
R/W							
0h							

Table 5-714. CPSW_NC_CPDMA_SRAM_TEST_TH0_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH0_CP	R/W	0h	Test CPDMA THost Channel 0 Completion Pointer

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5.2.2.272 CPSW_NC_CPDMA_SRAM_TEST_TH1_CP_REG Register

5.2.2.272.1 CPSW_NC_CPDMA_SRAM_TEST_TH1_CP_REG Register (Offset = 34364h) [reset = 0h]

Test CPDMA THost Channel 1 Completion Pointer

Return to Summary Table

Table 5-715. Instance Table

Instance Name	Physical Address
CPSW0	5283 4364h + formula

Figure 5-353. CPSW_NC_CPDMA_SRAM_TEST_TH1_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH1_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH1_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH1_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH1_CP							
R/W							
0h							

Table 5-716. CPSW_NC_CPDMA_SRAM_TEST_TH1_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH1_CP	R/W	0h	Test CPDMA THost Channel 1 Completion Pointer

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5.2.2.273 CPSW_NC_CPDMA_SRAM_TEST_TH2_CP_REG Register

5.2.2.273.1 CPSW_NC_CPDMA_SRAM_TEST_TH2_CP_REG Register (Offset = 34368h) [reset = 0h]

Test CPDMA THost Channel 2 Completion Pointer

Return to Summary Table

Table 5-717. Instance Table

Instance Name	Physical Address
CPSW0	5283 4368h + formula

Figure 5-354. CPSW_NC_CPDMA_SRAM_TEST_TH2_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH2_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH2_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH2_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH2_CP							
R/W							
0h							

Table 5-718. CPSW_NC_CPDMA_SRAM_TEST_TH2_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH2_CP	R/W	0h	Test CPDMA THost Channel 2 Completion Pointer

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5.2.2.274 CPSW_NC_CPDMA_SRAM_TEST_TH3_CP_REG Register

5.2.2.274.1 CPSW_NC_CPDMA_SRAM_TEST_TH3_CP_REG Register (Offset = 3436Ch) [reset = 0h]

Test CPDMA THost Channel 3 Completion Pointer

Return to Summary Table

Table 5-719. Instance Table

Instance Name	Physical Address
CPSW0	5283 436Ch + formula

Figure 5-355. CPSW_NC_CPDMA_SRAM_TEST_TH3_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH3_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH3_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH3_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH3_CP							
R/W							
0h							

Table 5-720. CPSW_NC_CPDMA_SRAM_TEST_TH3_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH3_CP	R/W	0h	Test CPDMA THost Channel 3 Completion Pointer

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5.2.2.275 CPSW_NC_CPDMA_SRAM_TEST_TH4_CP_REG Register

5.2.2.275.1 CPSW_NC_CPDMA_SRAM_TEST_TH4_CP_REG Register (Offset = 34370h) [reset = 0h]

Test CPDMA THost Channel 4 Completion Pointer

Return to Summary Table

Table 5-721. Instance Table

Instance Name	Physical Address
CPSW0	5283 4370h + formula

Figure 5-356. CPSW_NC_CPDMA_SRAM_TEST_TH4_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH4_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH4_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH4_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH4_CP							
R/W							
0h							

Table 5-722. CPSW_NC_CPDMA_SRAM_TEST_TH4_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH4_CP	R/W	0h	Test CPDMA THost Channel 4 Completion Pointer

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5.2.2.276 CPSW_NC_CPDMA_SRAM_TEST_TH5_CP_REG Register

5.2.2.276.1 CPSW_NC_CPDMA_SRAM_TEST_TH5_CP_REG Register (Offset = 34374h) [reset = 0h]

Test CPDMA THost Channel 5 Completion Pointer

Return to Summary Table

Table 5-723. Instance Table

Instance Name	Physical Address
CPSW0	5283 4374h + formula

Figure 5-357. CPSW_NC_CPDMA_SRAM_TEST_TH5_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH5_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH5_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH5_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH5_CP							
R/W							
0h							

Table 5-724. CPSW_NC_CPDMA_SRAM_TEST_TH5_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH5_CP	R/W	0h	Test CPDMA THost Channel 5 Completion Pointer

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5.2.2.277 CPSW_NC_CPDMA_SRAM_TEST_TH6_CP_REG Register

5.2.2.277.1 CPSW_NC_CPDMA_SRAM_TEST_TH6_CP_REG Register (Offset = 34378h) [reset = 0h]

Test CPDMA THost Channel 6 Completion Pointer

Return to Summary Table

Table 5-725. Instance Table

Instance Name	Physical Address
CPSW0	5283 4378h + formula

Figure 5-358. CPSW_NC_CPDMA_SRAM_TEST_TH6_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH6_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH6_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH6_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH6_CP							
R/W							
0h							

Table 5-726. CPSW_NC_CPDMA_SRAM_TEST_TH6_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH6_CP	R/W	0h	Test CPDMA THost Channel 6 Completion Pointer

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5.2.2.278 CPSW_NC_CPDMA_SRAM_TEST_TH7_CP_REG Register

5.2.2.278.1 CPSW_NC_CPDMA_SRAM_TEST_TH7_CP_REG Register (Offset = 3437Ch) [reset = 0h]

Test CPDMA THost Channel 7 Completion Pointer

Return to Summary Table

Table 5-727. Instance Table

Instance Name	Physical Address
CPSW0	5283 437Ch + formula

Figure 5-359. CPSW_NC_CPDMA_SRAM_TEST_TH7_CP_REG Name Register

31	30	29	28	27	26	25	24
TEST_TH7_CP							
R/W							
0h							
23	22	21	20	19	18	17	16
TEST_TH7_CP							
R/W							
0h							
15	14	13	12	11	10	9	8
TEST_TH7_CP							
R/W							
0h							
7	6	5	4	3	2	1	0
TEST_TH7_CP							
R/W							
0h							

Table 5-728. CPSW_NC_CPDMA_SRAM_TEST_TH7_CP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TEST_TH7_CP	R/W	0h	Test CPDMA THost Channel 7 Completion Pointer

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5.2.2.279 CPSW_NC_STAT_RXGOODFRAMES_J Register

5.2.2.279.1 CPSW_NC_STAT_RXGOODFRAMES_J Register (Offset = 3A000h) [reset = 0h]

Total number of good frames received

Return to Summary Table

Table 5-729. Instance Table

Instance Name	Physical Address
CPSW0	5283 A000h + formula

Figure 5-360. CPSW_NC_STAT_RXGOODFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-730. CPSW_NC_STAT_RXGOODFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good frames received

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5.2.2.280 CPSW_NC_STAT_RXBROADCASTFRAMES_J Register

5.2.2.280.1 CPSW_NC_STAT_RXBROADCASTFRAMES_J Register (Offset = 3A004h) [reset = 0h]

Total number of good broadcast frames received

Return to Summary Table

Table 5-731. Instance Table

Instance Name	Physical Address
CPSW0	5283 A004h + formula

Figure 5-361. CPSW_NC_STAT_RXBROADCASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-732. CPSW_NC_STAT_RXBROADCASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good broadcast frames received

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5.2.2.281 CPSW_NC_STAT_RXMULTICASTFRAMES_J Register

5.2.2.281.1 CPSW_NC_STAT_RXMULTICASTFRAMES_J Register (Offset = 3A008h) [reset = 0h]

Total number of good multicast frames received

Return to Summary Table

Table 5-733. Instance Table

Instance Name	Physical Address
CPSW0	5283 A008h + formula

Figure 5-362. CPSW_NC_STAT_RXMULTICASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-734. CPSW_NC_STAT_RXMULTICASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good multicast frames received

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5.2.2.282 CPSW_NC_STAT_RXPAUSEFRAMES_J Register

5.2.2.282.1 CPSW_NC_STAT_RXPAUSEFRAMES_J Register (Offset = 3A00Ch) [reset = 0h]

Total number of pause frames received

Return to Summary Table

Table 5-735. Instance Table

Instance Name	Physical Address
CPSW0	5283 A00Ch + formula

Figure 5-363. CPSW_NC_STAT_RXPAUSEFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-736. CPSW_NC_STAT_RXPAUSEFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of pause frames received

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5.2.2.283 CPSW_NC_STAT_RXCRCERRORS_J Register

5.2.2.283.1 CPSW_NC_STAT_RXCRCERRORS_J Register (Offset = 3A010h) [reset = 0h]

Total number of CRC errors frames received

Return to Summary Table

Table 5-737. Instance Table

Instance Name	Physical Address
CPSW0	5283 A010h + formula

Figure 5-364. CPSW_NC_STAT_RXCRCERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-738. CPSW_NC_STAT_RXCRCERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of CRC errors frames received

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5.2.2.284 CPSW_NC_STAT_RXALIGNCODEERRORS_J Register

5.2.2.284.1 CPSW_NC_STAT_RXALIGNCODEERRORS_J Register (Offset = 3A014h) [reset = 0h]

Total number of alignment/code errors received

Return to Summary Table

Table 5-739. Instance Table

Instance Name	Physical Address
CPSW0	5283 A014h + formula

Figure 5-365. CPSW_NC_STAT_RXALIGNCODEERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-740. CPSW_NC_STAT_RXALIGNCODEERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of alignment/code errors received

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5.2.2.285 CPSW_NC_STAT_RXOVERSIZEDFRAMES_J Register

5.2.2.285.1 CPSW_NC_STAT_RXOVERSIZEDFRAMES_J Register (Offset = 3A018h) [reset = 0h]

Total number of oversized frames received

Return to Summary Table

Table 5-741. Instance Table

Instance Name	Physical Address
CPSW0	5283 A018h + formula

Figure 5-366. CPSW_NC_STAT_RXOVERSIZEDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-742. CPSW_NC_STAT_RXOVERSIZEDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of oversized frames received

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5.2.2.286 CPSW_NC_STAT_RXJABBERFRAMES_J Register

5.2.2.286.1 CPSW_NC_STAT_RXJABBERFRAMES_J Register (Offset = 3A01Ch) [reset = 0h]

Total number of jabber frames received

Return to Summary Table

Table 5-743. Instance Table

Instance Name	Physical Address
CPSW0	5283 A01Ch + formula

Figure 5-367. CPSW_NC_STAT_RXJABBERFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-744. CPSW_NC_STAT_RXJABBERFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of jabber frames received

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5.2.2.287 CPSW_NC_STAT_RXUNDERSIZEDFRAMES_J Register

5.2.2.287.1 CPSW_NC_STAT_RXUNDERSIZEDFRAMES_J Register (Offset = 3A020h) [reset = 0h]

Total number of undersized frames received

Return to Summary Table

Table 5-745. Instance Table

Instance Name	Physical Address
CPSW0	5283 A020h + formula

Figure 5-368. CPSW_NC_STAT_RXUNDERSIZEDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-746. CPSW_NC_STAT_RXUNDERSIZEDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of undersized frames received

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5.2.2.288 CPSW_NC_STAT_RXFRAGMENTS_J Register

5.2.2.288.1 CPSW_NC_STAT_RXFRAGMENTS_J Register (Offset = 3A024h) [reset = 0h]

Total number of fragmented frames received

Return to Summary Table

Table 5-747. Instance Table

Instance Name	Physical Address
CPSW0	5283 A024h + formula

Figure 5-369. CPSW_NC_STAT_RXFRAGMENTS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-748. CPSW_NC_STAT_RXFRAGMENTS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of fragmented frames received

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5.2.2.289 CPSW_NC_STAT_ALE_DROP_J Register

5.2.2.289.1 CPSW_NC_STAT_ALE_DROP_J Register (Offset = 3A028h) [reset = 0h]

Total number of frames dropped by the ALE

Return to Summary Table

Table 5-749. Instance Table

Instance Name	Physical Address
CPSW0	5283 A028h + formula

Figure 5-370. CPSW_NC_STAT_ALE_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-750. CPSW_NC_STAT_ALE_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames dropped by the ALE

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5.2.2.290 CPSW_NC_STAT_ALE_OVERRUN_DROP_J Register

5.2.2.290.1 CPSW_NC_STAT_ALE_OVERRUN_DROP_J Register (Offset = 3A02Ch) [reset = 0h]

Total number of overrun frames dropped by the ALE

Return to Summary Table

Table 5-751. Instance Table

Instance Name	Physical Address
CPSW0	5283 A02Ch + formula

Figure 5-371. CPSW_NC_STAT_ALE_OVERRUN_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-752. CPSW_NC_STAT_ALE_OVERRUN_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of overrun frames dropped by the ALE

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5.2.2.291 CPSW_NC_STAT_RXOCTETS_J Register

5.2.2.291.1 CPSW_NC_STAT_RXOCTETS_J Register (Offset = 3A030h) [reset = 0h]

Total number of received bytes in good frames

Return to Summary Table

Table 5-753. Instance Table

Instance Name	Physical Address
CPSW0	5283 A030h + formula

Figure 5-372. CPSW_NC_STAT_RXOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 5-754. CPSW_NC_STAT_RXOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of received bytes in good frames

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5.2.2.292 CPSW_NC_STAT_TXGOODFRAMES_J Register

5.2.2.292.1 CPSW_NC_STAT_TXGOODFRAMES_J Register (Offset = 3A034h) [reset = 0h]

Total number of good frames transmitted

Return to Summary Table

Table 5-755. Instance Table

Instance Name	Physical Address
CPSW0	5283 A034h + formula

Figure 5-373. CPSW_NC_STAT_TXGOODFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-756. CPSW_NC_STAT_TXGOODFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good frames transmitted

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5.2.2.293 CPSW_NC_STAT_TXBROADCASTFRAMES_J Register

5.2.2.293.1 CPSW_NC_STAT_TXBROADCASTFRAMES_J Register (Offset = 3A038h) [reset = 0h]

Total number of good broadcast frames transmitted

Return to Summary Table

Table 5-757. Instance Table

Instance Name	Physical Address
CPSW0	5283 A038h + formula

Figure 5-374. CPSW_NC_STAT_TXBROADCASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-758. CPSW_NC_STAT_TXBROADCASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good broadcast frames transmitted

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5.2.2.294 CPSW_NC_STAT_TXMULTICASTFRAMES_J Register

5.2.2.294.1 CPSW_NC_STAT_TXMULTICASTFRAMES_J Register (Offset = 3A03Ch) [reset = 0h]

Total number of good multicast frames transmitted

Return to Summary Table

Table 5-759. Instance Table

Instance Name	Physical Address
CPSW0	5283 A03Ch + formula

Figure 5-375. CPSW_NC_STAT_TXMULTICASTFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-760. CPSW_NC_STAT_TXMULTICASTFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of good multicast frames transmitted

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5.2.2.295 CPSW_NC_STAT_TXPAUSEFRAMES_J Register

5.2.2.295.1 CPSW_NC_STAT_TXPAUSEFRAMES_J Register (Offset = 3A040h) [reset = 0h]

Total number of pause frames transmitted

Return to Summary Table

Table 5-761. Instance Table

Instance Name	Physical Address
CPSW0	5283 A040h + formula

Figure 5-376. CPSW_NC_STAT_TXPAUSEFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-762. CPSW_NC_STAT_TXPAUSEFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of pause frames transmitted

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5.2.2.296 CPSW_NC_STAT_TXDEFERREDFRAMES_J Register

5.2.2.296.1 CPSW_NC_STAT_TXDEFERREDFRAMES_J Register (Offset = 3A044h) [reset = 0h]

Total number of deferred frames transmitted

Return to Summary Table

Table 5-763. Instance Table

Instance Name	Physical Address
CPSW0	5283 A044h + formula

Figure 5-377. CPSW_NC_STAT_TXDEFERREDFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-764. CPSW_NC_STAT_TXDEFERREDFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of deferred frames transmitted

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5.2.2.297 CPSW_NC_STAT_TXCOLLISIONFRAMES_J Register

5.2.2.297.1 CPSW_NC_STAT_TXCOLLISIONFRAMES_J Register (Offset = 3A048h) [reset = 0h]

Total number of transmitted frames experiencing a collision

Return to Summary Table

Table 5-765. Instance Table

Instance Name	Physical Address
CPSW0	5283 A048h + formula

Figure 5-378. CPSW_NC_STAT_TXCOLLISIONFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-766. CPSW_NC_STAT_TXCOLLISIONFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing a collision

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5.2.2.298 CPSW_NC_STAT_TXSINGLECOLLFRAMES_J Register

5.2.2.298.1 CPSW_NC_STAT_TXSINGLECOLLFRAMES_J Register (Offset = 3A04Ch) [reset = 0h]

Total number of transmitted frames experiencing a single collision

Return to Summary Table

Table 5-767. Instance Table

Instance Name	Physical Address
CPSW0	5283 A04Ch + formula

Figure 5-379. CPSW_NC_STAT_TXSINGLECOLLFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-768. CPSW_NC_STAT_TXSINGLECOLLFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing a single collision

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5.2.2.299 CPSW_NC_STAT_TXMULTCOLLFRAMES_J Register

5.2.2.299.1 CPSW_NC_STAT_TXMULTCOLLFRAMES_J Register (Offset = 3A050h) [reset = 0h]

Total number of transmitted frames experiencing multiple collisions

Return to Summary Table

Table 5-769. Instance Table

Instance Name	Physical Address
CPSW0	5283 A050h + formula

Figure 5-380. CPSW_NC_STAT_TXMULTCOLLFRAMES_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-770. CPSW_NC_STAT_TXMULTCOLLFRAMES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames experiencing multiple collisions

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5.2.2.300 CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_J Register

5.2.2.300.1 CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_J Register (Offset = 3A054h) [reset = 0h]

Total number of transmitted frames abandoned due to excessive collisions

Return to Summary Table

Table 5-771. Instance Table

Instance Name	Physical Address
CPSW0	5283 A054h + formula

Figure 5-381. CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-772. CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to excessive collisions

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5.2.2.301 CPSW_NC_STAT_TXLATECOLLISIONS_J Register

5.2.2.301.1 CPSW_NC_STAT_TXLATECOLLISIONS_J Register (Offset = 3A058h) [reset = 0h]

Total number of transmitted frames abandoned due to a late collision

Return to Summary Table

Table 5-773. Instance Table

Instance Name	Physical Address
CPSW0	5283 A058h + formula

Figure 5-382. CPSW_NC_STAT_TXLATECOLLISIONS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-774. CPSW_NC_STAT_TXLATECOLLISIONS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to a late collision

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5.2.2.302 CPSW_NC_STAT_RXIPGERROR_J Register

5.2.2.302.1 CPSW_NC_STAT_RXIPGERROR_J Register (Offset = 3A05Ch) [reset = 0h]

Total number of receive inter-packet gap errors (10G only)

Return to Summary Table

Table 5-775. Instance Table

Instance Name	Physical Address
CPSW0	5283 A05Ch + formula

Figure 5-383. CPSW_NC_STAT_RXIPGERROR_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-776. CPSW_NC_STAT_RXIPGERROR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of receive inter-packet gap errors (10G only)

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5.2.2.303 CPSW_NC_STAT_TXCARRIERSENSEERRORS_J Register

5.2.2.303.1 CPSW_NC_STAT_TXCARRIERSENSEERRORS_J Register (Offset = 3A060h) [reset = 0h]

Total number of transmitted frames that experienced a carrier loss

Return to Summary Table

Table 5-777. Instance Table

Instance Name	Physical Address
CPSW0	5283 A060h + formula

Figure 5-384. CPSW_NC_STAT_TXCARRIERSENSEERRORS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-778. CPSW_NC_STAT_TXCARRIERSENSEERRORS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of transmitted frames that experienced a carrier loss

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5.2.2.304 CPSW_NC_STAT_TXOCTETS_J Register

5.2.2.304.1 CPSW_NC_STAT_TXOCTETS_J Register (Offset = 3A064h) [reset = 0h]

Total number of bytes in all good frames transmitted

Return to Summary Table

Table 5-779. Instance Table

Instance Name	Physical Address
CPSW0	5283 A064h + formula

Figure 5-385. CPSW_NC_STAT_TXOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-780. CPSW_NC_STAT_TXOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of bytes in all good frames transmitted

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5.2.2.305 CPSW_NC_STAT_OCTETFRAMES64_J Register

5.2.2.305.1 CPSW_NC_STAT_OCTETFRAMES64_J Register (Offset = 3A068h) [reset = 0h]

Total number of 64-byte frames received and transmitted

Return to Summary Table

Table 5-781. Instance Table

Instance Name	Physical Address
CPSW0	5283 A068h + formula

Figure 5-386. CPSW_NC_STAT_OCTETFRAMES64_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-782. CPSW_NC_STAT_OCTETFRAMES64_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of 64-byte frames received and transmitted

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5.2.2.306 CPSW_NC_STAT_OCTETFRAMES65T127_J Register

5.2.2.306.1 CPSW_NC_STAT_OCTETFRAMES65T127_J Register (Offset = 3A06Ch) [reset = 0h]

Total number of frames of size 65 to 127 bytes received and transmitted

Return to Summary Table

Table 5-783. Instance Table

Instance Name	Physical Address
CPSW0	5283 A06Ch + formula

Figure 5-387. CPSW_NC_STAT_OCTETFRAMES65T127_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-784. CPSW_NC_STAT_OCTETFRAMES65T127_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 65 to 127 bytes received and transmitted

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5.2.2.307 CPSW_NC_STAT_OCTETFRAMES128T255_J Register

5.2.2.307.1 CPSW_NC_STAT_OCTETFRAMES128T255_J Register (Offset = 3A070h) [reset = 0h]

Total number of frames of size 128 to 255 bytes received and transmitted

Return to Summary Table

Table 5-785. Instance Table

Instance Name	Physical Address
CPSW0	5283 A070h + formula

Figure 5-388. CPSW_NC_STAT_OCTETFRAMES128T255_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 5-786. CPSW_NC_STAT_OCTETFRAMES128T255_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 128 to 255 bytes received and transmitted

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5.2.2.308 CPSW_NC_STAT_OCTETFRAMES256T511_J Register

5.2.2.308.1 CPSW_NC_STAT_OCTETFRAMES256T511_J Register (Offset = 3A074h) [reset = 0h]

Total number of frames of size 256 to 511 bytes received and transmitted

Return to Summary Table

Table 5-787. Instance Table

Instance Name	Physical Address
CPSW0	5283 A074h + formula

Figure 5-389. CPSW_NC_STAT_OCTETFRAMES256T511_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-788. CPSW_NC_STAT_OCTETFRAMES256T511_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 256 to 511 bytes received and transmitted

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5.2.2.309 CPSW_NC_STAT_OCTETFRAMES512T1023_J Register

5.2.2.309.1 CPSW_NC_STAT_OCTETFRAMES512T1023_J Register (Offset = 3A078h) [reset = 0h]

Total number of frames of size 512 to 1023 bytes received and transmitted

Return to Summary Table

Table 5-789. Instance Table

Instance Name	Physical Address
CPSW0	5283 A078h + formula

Figure 5-390. CPSW_NC_STAT_OCTETFRAMES512T1023_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-790. CPSW_NC_STAT_OCTETFRAMES512T1023_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 512 to 1023 bytes received and transmitted

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5.2.2.310 CPSW_NC_STAT_OCTETFRAMES1024TUP_J Register

5.2.2.310.1 CPSW_NC_STAT_OCTETFRAMES1024TUP_J Register (Offset = 3A07Ch) [reset = 0h]

Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

Return to Summary Table

Table 5-791. Instance Table

Instance Name	Physical Address
CPSW0	5283 A07Ch + formula

Figure 5-391. CPSW_NC_STAT_OCTETFRAMES1024TUP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-792. CPSW_NC_STAT_OCTETFRAMES1024TUP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

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5.2.2.311 CPSW_NC_STAT_NETOCTETS_J Register

5.2.2.311.1 CPSW_NC_STAT_NETOCTETS_J Register (Offset = 3A080h) [reset = 0h]

Total number of bytes received and transmitted

Return to Summary Table

Table 5-793. Instance Table

Instance Name	Physical Address
CPSW0	5283 A080h + formula

Figure 5-392. CPSW_NC_STAT_NETOCTETS_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-794. CPSW_NC_STAT_NETOCTETS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of bytes received and transmitted

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5.2.2.312 CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_J Register

5.2.2.312.1 CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_J Register (Offset = 3A084h) [reset = 0h]

Receive Bottom of FIFO Drop

Return to Summary Table

Table 5-795. Instance Table

Instance Name	Physical Address
CPSW0	5283 A084h + formula

Figure 5-393. CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-796. CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Receive Bottom of FIFO Drop

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5.2.2.313 CPSW_NC_STAT_PORTMASK_DROP_J Register

5.2.2.313.1 CPSW_NC_STAT_PORTMASK_DROP_J Register (Offset = 3A088h) [reset = 0h]

Total number of dropped frames received due to portmask

Return to Summary Table

Table 5-797. Instance Table

Instance Name	Physical Address
CPSW0	5283 A088h + formula

Figure 5-394. CPSW_NC_STAT_PORTMASK_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-798. CPSW_NC_STAT_PORTMASK_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames received due to portmask

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5.2.2.314 CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_J Register

5.2.2.314.1 CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_J Register (Offset = 3A08Ch) [reset = 0h]

Receive Top of FIFO Drop

Return to Summary Table

Table 5-799. Instance Table

Instance Name	Physical Address
CPSW0	5283 A08Ch + formula

Figure 5-395. CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-800. CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Receive Top of FIFO Drop

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5.2.2.315 CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_J Register

5.2.2.315.1 CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_J Register (Offset = 3A090h) [reset = 0h]

Total number of dropped frames due to ALE Rate Limiting

Return to Summary Table

Table 5-801. Instance Table

Instance Name	Physical Address
CPSW0	5283 A090h + formula

Figure 5-396. CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COUNT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT							
R/W							
0h							

Table 5-802. CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Rate Limiting

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5.2.2.316 CPSW_NC_STAT_ALE_VID_INGRESS_DROP_J Register

5.2.2.316.1 CPSW_NC_STAT_ALE_VID_INGRESS_DROP_J Register (Offset = 3A094h) [reset = 0h]

Total number of dropped frames due to ALE VID Ingress

Return to Summary Table

Table 5-803. Instance Table

Instance Name	Physical Address
CPSW0	5283 A094h + formula

Figure 5-397. CPSW_NC_STAT_ALE_VID_INGRESS_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-804. CPSW_NC_STAT_ALE_VID_INGRESS_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE VID Ingress

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5.2.2.317 CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_J Register

5.2.2.317.1 CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_J Register (Offset = 3A098h) [reset = 0h]

Total number of dropped frames due to DA=SA

Return to Summary Table

Table 5-805. Instance Table

Instance Name	Physical Address
CPSW0	5283 A098h + formula

Figure 5-398. CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-806. CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to DA=SA

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5.2.2.318 CPSW_NC_STAT_ALE_BLOCK_DROP_J Register

5.2.2.318.1 CPSW_NC_STAT_ALE_BLOCK_DROP_J Register (Offset = 3A09Ch) [reset = 0h]

Total number of dropped frames due to ALE Block Mode

Return to Summary Table

Table 5-807. Instance Table

Instance Name	Physical Address
CPSW0	5283 A09Ch + formula

Figure 5-399. CPSW_NC_STAT_ALE_BLOCK_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-808. CPSW_NC_STAT_ALE_BLOCK_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Block Mode

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5.2.2.319 CPSW_NC_STAT_ALE_SECURE_DROP_J Register

5.2.2.319.1 CPSW_NC_STAT_ALE_SECURE_DROP_J Register (Offset = 3A0A0h) [reset = 0h]

Total number of dropped frames due to ALE Secure Mode

Return to Summary Table

Table 5-809. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0A0h + formula

Figure 5-400. CPSW_NC_STAT_ALE_SECURE_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-810. CPSW_NC_STAT_ALE_SECURE_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Secure Mode

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5.2.2.320 CPSW_NC_STAT_ALE_AUTH_DROP_J Register

5.2.2.320.1 CPSW_NC_STAT_ALE_AUTH_DROP_J Register (Offset = 3A0A4h) [reset = 0h]

Total number of dropped frames due to ALE Authentication

Return to Summary Table

Table 5-811. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0A4h + formula

Figure 5-401. CPSW_NC_STAT_ALE_AUTH_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-812. CPSW_NC_STAT_ALE_AUTH_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Total number of dropped frames due to ALE Authentication

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5.2.2.321 CPSW_NC_STAT_ALE_UNKN_UNI_J Register

5.2.2.321.1 CPSW_NC_STAT_ALE_UNKN_UNI_J Register (Offset = 3A0A8h) [reset = 0h]

ALE Receive Unknown Unicast

Return to Summary Table

Table 5-813. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0A8h + formula

Figure 5-402. CPSW_NC_STAT_ALE_UNKN_UNI_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-814. CPSW_NC_STAT_ALE_UNKN_UNI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Unicast

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5.2.2.322 CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_J Register

5.2.2.322.1 CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_J Register (Offset = 3A0ACh) [reset = 0h]

ALE Receive Unknown Unicast Bytecount

Return to Summary Table

Table 5-815. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0ACh + formula

Figure 5-403. CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-816. CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Unicast Bytecount

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5.2.2.323 CPSW_NC_STAT_ALE_UNKN_MLT_J Register

5.2.2.323.1 CPSW_NC_STAT_ALE_UNKN_MLT_J Register (Offset = 3A0B0h) [reset = 0h]

ALE Receive Unknown Multicast

Return to Summary Table

Table 5-817. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0B0h + formula

Figure 5-404. CPSW_NC_STAT_ALE_UNKN_MLT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-818. CPSW_NC_STAT_ALE_UNKN_MLT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Multicast

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5.2.2.324 CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_J Register

5.2.2.324.1 CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_J Register (Offset = 3A0B4h) [reset = 0h]

ALE Receive Unknown Multicast Bytecount

Return to Summary Table

Table 5-819. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0B4h + formula

Figure 5-405. CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-820. CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Multicast Bytecount

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5.2.2.325 CPSW_NC_STAT_ALE_UNKN_BRD_J Register

5.2.2.325.1 CPSW_NC_STAT_ALE_UNKN_BRD_J Register (Offset = 3A0B8h) [reset = 0h]

ALE Receive Unknown Broadcast

Return to Summary Table

Table 5-821. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0B8h + formula

Figure 5-406. CPSW_NC_STAT_ALE_UNKN_BRD_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-822. CPSW_NC_STAT_ALE_UNKN_BRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Broadcast

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5.2.2.326 CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_J Register

5.2.2.326.1 CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_J Register (Offset = 3A0BCh) [reset = 0h]

ALE Receive Unknown Broadcast Bytecount

Return to Summary Table

Table 5-823. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0BCh + formula

Figure 5-407. CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-824. CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Receive Unknown Broadcast Bytecount

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5.2.2.327 CPSW_NC_STAT_ALE_POL_MATCH_J Register

5.2.2.327.1 CPSW_NC_STAT_ALE_POL_MATCH_J Register (Offset = 3A0C0h) [reset = 0h]

ALE Policer Matched

Return to Summary Table

Table 5-825. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0C0h + formula

Figure 5-408. CPSW_NC_STAT_ALE_POL_MATCH_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-826. CPSW_NC_STAT_ALE_POL_MATCH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched

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5.2.2.328 CPSW_NC_STAT_ALE_POL_MATCH_RED_J Register

5.2.2.328.1 CPSW_NC_STAT_ALE_POL_MATCH_RED_J Register (Offset = 3A0C4h) [reset = 0h]

ALE Policer Matched and Condition Red

Return to Summary Table

Table 5-827. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0C4h + formula

Figure 5-409. CPSW_NC_STAT_ALE_POL_MATCH_RED_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-828. CPSW_NC_STAT_ALE_POL_MATCH_RED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched and Condition Red

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5.2.2.329 CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_J Register

5.2.2.329.1 CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_J Register (Offset = 3A0C8h) [reset = 0h]

ALE Policer Matched and Condition Yellow

Return to Summary Table

Table 5-829. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0C8h + formula

Figure 5-410. CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-830. CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Policer Matched and Condition Yellow

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5.2.2.330 CPSW_NC_STAT_ALE_MULT_SA_DROP_J Register

5.2.2.330.1 CPSW_NC_STAT_ALE_MULT_SA_DROP_J Register (Offset = 3A0CCh) [reset = 0h]

ALE Multicast Source Address Drop

Return to Summary Table

Table 5-831. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0CCh + formula

Figure 5-411. CPSW_NC_STAT_ALE_MULT_SA_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-832. CPSW_NC_STAT_ALE_MULT_SA_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Multicast Source Address drop

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5.2.2.331 CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_J Register

5.2.2.331.1 CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_J Register (Offset = 3A0D0h) [reset = 0h]

ALE Dual VLAN Drop

Return to Summary Table

Table 5-833. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0D0h + formula

Figure 5-412. CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-834. CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Dual VLAN drop

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5.2.2.332 CPSW_NC_STAT_ALE_LEN_ERROR_DROP_J Register

5.2.2.332.1 CPSW_NC_STAT_ALE_LEN_ERROR_DROP_J Register (Offset = 3A0D4h) [reset = 0h]

ALE Length Error Drop

Return to Summary Table

Table 5-835. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0D4h + formula

Figure 5-413. CPSW_NC_STAT_ALE_LEN_ERROR_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-836. CPSW_NC_STAT_ALE_LEN_ERROR_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Length Error drop

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5.2.2.333 CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_J Register

5.2.2.333.1 CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_J Register (Offset = 3A0D8h) [reset = 0h]

ALE IP Next Header Drop

Return to Summary Table

Table 5-837. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0D8h + formula

Figure 5-414. CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-838. CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE Next Header drop

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5.2.2.334 CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_J Register

5.2.2.334.1 CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_J Register (Offset = 3A0DCh) [reset = 0h]

ALE IPV4 Frag Drop

Return to Summary Table

Table 5-839. Instance Table

Instance Name	Physical Address
CPSW0	5283 A0DCh + formula

Figure 5-415. CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_j Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-840. CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	ALE IPV4 Fragment drop

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5.2.2.335 CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_J Register

5.2.2.335.1 CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_J Register (Offset = 3A17Ch) [reset = 0h]

Transmit Memory Protect CRC Error

Return to Summary Table

Table 5-841. Instance Table

Instance Name	Physical Address
CPSW0	5283 A17Ch + formula

Figure 5-416. CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-842. CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	COUNT	R/W	0h	Transmit Memory Protect CRC Error

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5.2.2.336 CPSW_NC_STAT_ENET_PN_TX_PRI_REG_J_K Register

5.2.2.336.1 CPSW_NC_STAT_ENET_PN_TX_PRI_REG_J_K Register (Offset = 3A180h) [reset = 0h]

ENET Port n PRIORITY N Packet Count

Return to Summary Table

Table 5-843. Instance Table

Instance Name	Physical Address
CPSW0	5283 A180h + formula

Figure 5-417. CPSW_NC_STAT_ENET_PN_TX_PRI_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN							
R/W							
0h							

Table 5-844. CPSW_NC_STAT_ENET_PN_TX_PRI_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN	R/W	0h	ENET TX Priority Packet Count

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5.2.2.337 CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_J_K Register

5.2.2.337.1 CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_J_K Register (Offset = 3A1A0h) [reset = 0h]

ENET Port n PRIORITY N Packet Byte Count

Return to Summary Table

Table 5-845. Instance Table

Instance Name	Physical Address
CPSW0	5283 A1A0h + formula

Figure 5-418. CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_BCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_BCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_BCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_BCNT							
R/W							
0h							

Table 5-846. CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Byte Count

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5.2.2.338 CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_J_K Register

5.2.2.338.1 CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_J_K Register (Offset = 3A1C0h) [reset = 0h]

ENET Port n PRIORITY N Packet Drop Count

Return to Summary Table

Table 5-847. Instance Table

Instance Name	Physical Address
CPSW0	5283 A1C0h + formula

Figure 5-419. CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_DROP							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_DROP							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP							
R/W							
0h							

Table 5-848. CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_DROP	R/W	0h	ENET Port n PRIORITY N Packet Drop Count

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5.2.2.339 CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_K Register

5.2.2.339.1 CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_J_K Register (Offset = 3A1E0h) [reset = 0h]

ENET Port n PRIORITY N Packet Drop Byte Count

Return to Summary Table

Table 5-849. Instance Table

Instance Name	Physical Address
CPSW0	5283 A1E0h + formula

Figure 5-420. CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Name Register

31	30	29	28	27	26	25	24
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP_BCNT							
R/W							
0h							

Table 5-850. CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PN_TX_PRIN_DROP_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Drop Byte Count

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5.2.2.340 CPSW_NC_CPTS_IDVER_REG Register

5.2.2.340.1 CPSW_NC_CPTS_IDVER_REG Register (Offset = 3D000h) [reset = 4E8A010Dh]

Identification and Version Register

Return to Summary Table

Table 5-851. Instance Table

Instance Name	Physical Address
CPSW0	5283 D000h + formula

Figure 5-421. CPSW_NC_CPTS_IDVER_REG Name Register

31	30	29	28	27	26	25	24
IDENT							
R							
4E8Ah							
23	22	21	20	19	18	17	16
IDENT							
R							
4E8Ah							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_VER		
R					R		
0h					1h		
7	6	5	4	3	2	1	0
MINOR_VER							
R							
Dh							

Table 5-852. CPSW_NC_CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IDENT	R	4E8Ah	Identification value
15:11	RTL_VER	R	0h	RTL version value
10:8	MAJOR_VER	R	1h	Major version value
7:0	MINOR_VER	R	Dh	Minor version value

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5.2.2.341 CPSW_NC_CPTS_CONTROL_REG Register

5.2.2.341.1 CPSW_NC_CPTS_CONTROL_REG Register (Offset = 3D004h) [reset = 4h]

Time Sync Control Register

Return to Summary Table

Table 5-853. Instance Table

Instance Name	Physical Address
CPSW0	5283 D004h + formula

Figure 5-422. CPSW_NC_CPTS_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
TS_SYNC_SEL				RESERVED			
R/W				NONE			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED						TS_GENF_CLR_EN	TS_RX_NO_EVENT
NONE						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
HW8_TS_PUSH_EN	HW7_TS_PUSH_EN	HW6_TS_PUSH_EN	HW5_TS_PUSH_EN	HW4_TS_PUSH_EN	HW3_TS_PUSH_EN	HW2_TS_PUSH_EN	HW1_TS_PUSH_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
TS_PPM_DIR	TS_COMP_TOG	MODE	SEQUENCE_EN	TSTAMP_EN	TS_COMP_POLARITY	INT_TEST	CPTS_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	1h	0h	0h

Table 5-854. CPSW_NC_CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	TS_SYNC_SEL	R/W	0h	TS_SYNC output timestamp counter bit select - 0000 - TS_SYNC disabled. 0001 - TS_SYNC is timestamp counter bit 17 0010 - TS_SYNC is timestamp counter bit 18 ... 1110 - TS_SYNC is timestamp counter bit 30 1111 - TS_SYNC is timestamp counter bit 31
27:18	RESERVED	NONE	0h	Reserved
17	TS_GENF_CLR_EN	R/W	0h	GENF (and ESTF) Clear Enable - 0 - A TS_GENFn output is not cleared when the associated ts_genf_length[31:0] is cleared to zero. 1 - A TS_GENFn output is cleared when the associated ts_genf_length[31:0] is cleared to zero.
16	TS_RX_NO_EVENT	R/W	0h	Timestamp Ethernet Receive produces no events - 0 - Ethernet receive timesync events enabled. 1 - Ethernet receive timesync events disabled.
15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable

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Table 5-854. CPSW_NC_CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable
7	TS_PPM_DIR	R/W	0h	PPM Correction Direction - 0 - Increase the time_stamp[63:0] value by the PPM value. 1 - Decrease the time_stamp[63:0] value by the PPM value.
6	TS_COMP_TOG	R/W	0h	Timestamp Compare Toggle mode - 0 - TS_COMP is in non-toggle mode. 1 - TS_COMP is in toggle mode.
5	MODE	R/W	0h	64-Bit Mode - 0 - The timestamp is 32-bits with the upper 32-bits forced to zero. 1 - The timestamp is 64-bits.
4	SEQUENCE_EN	R/W	0h	Sequence Enable - 0 - The timestamp value increments with the selected RFTCLK (normal operation). 1 - The timestamp for received packets is the sequence number of the received packet (first packet is 1, second packet is 2, etc). This can be used for test purposes.
3	TSTAMP_EN	R/W	0h	Host Receive Timestamp Enable - 0 - Timestamps are disabled on received packets to host. 1 - Timestamps enabled on received packets to host (cpts_en must be set).
2	TS_COMP_POLARITY	R/W	1h	TS_COMP Polarity 0 - TS_COMP is asserted low 1 - TS_COMP is asserted high
1	INT_TEST	R/W	0h	Interrupt Test - When set, this bit allows the raw interrupt to be written to facilitate interrupt test.
0	CPTS_EN	R/W	0h	Time Sync Enable - When disabled (cleared to zero), the CPTS RCLK domain is held in reset.

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5.2.2.342 CPSW_NC_CPTS_RFTCLK_SEL_REG Register

5.2.2.342.1 CPSW_NC_CPTS_RFTCLK_SEL_REG Register (Offset = 3D008h) [reset = 0h]

RFTCLK Select Register

Return to Summary Table

Table 5-855. Instance Table

Instance Name	Physical Address
CPSW0	5283 D008h + formula

Figure 5-423. CPSW_NC_CPTS_RFTCLK_SEL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			RFTCLK_SEL				
NONE			R/W				
0h			0h				

Table 5-856. CPSW_NC_CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	RFTCLK_SEL	R/W	0h	Reference Clock Select - This signal is used to control an external multiplexor that selects one of up to 32 clocks for time sync reference (RFTCLK). This rftclk_sel value can be written only when the cpts_en bit and the tstamp_en bit are cleared to zero in the TS_Control register.

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5.2.2.343 CPSW_NC_CPTS_TS_PUSH_REG Register

5.2.2.343.1 CPSW_NC_CPTS_TS_PUSH_REG Register (Offset = 3D00Ch) [reset = 0h]

Time Stamp Event Push Register

Return to Summary Table

Table 5-857. Instance Table

Instance Name	Physical Address
CPSW0	5283 D00Ch + formula

Figure 5-424. CPSW_NC_CPTS_TS_PUSH_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PUSH
NONE							W
0h							0h

Table 5-858. CPSW_NC_CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PUSH	W	0h	Time stamp event push - When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time). This bit is write only and always reads zero.

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5.2.2.344 CPSW_NC_CPTS_TS_LOAD_VAL_REG Register

5.2.2.344.1 CPSW_NC_CPTS_TS_LOAD_VAL_REG Register (Offset = 3D010h) [reset = 0h]

Time Stamp Load Low Value Register

Return to Summary Table

Table 5-859. Instance Table

Instance Name	Physical Address
CPSW0	5283 D010h + formula

Figure 5-425. CPSW_NC_CPTS_TS_LOAD_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_LOAD_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_LOAD_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_LOAD_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LOAD_VAL							
R/W							
0h							

Table 5-860. CPSW_NC_CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time Stamp Load Low Value - Writing the ts_load_en bit causes ts_load[63:0] to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register.

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5.2.2.345 CPSW_NC_CPTS_TS_LOAD_EN_REG Register

5.2.2.345.1 CPSW_NC_CPTS_TS_LOAD_EN_REG Register (Offset = 3D014h) [reset = 0h]

Time Stamp Load Enable Register

Return to Summary Table

Table 5-861. Instance Table

Instance Name	Physical Address
CPSW0	5283 D014h + formula

Figure 5-426. CPSW_NC_CPTS_TS_LOAD_EN_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_LOAD_EN
NONE							W
0h							0h

Table 5-862. CPSW_NC_CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_LOAD_EN	W	0h	Time Stamp Load - Writing a one to this bit enables the time stamp value to be written with the value in ts_load[63:0]. This bit is write only and will be cleared by the hardware after one clock. The upper 32-bits of the timestamp are forced to zero in 32-bit mode.

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5.2.2.346 CPSW_NC_CPTS_TS_COMP_VAL_REG Register

5.2.2.346.1 CPSW_NC_CPTS_TS_COMP_VAL_REG Register (Offset = 3D018h) [reset = 0h]

Time Stamp Comparison Low Value Register

Return to Summary Table

Table 5-863. Instance Table

Instance Name	Physical Address
CPSW0	5283 D018h + formula

Figure 5-427. CPSW_NC_CPTS_TS_COMP_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_VAL							
R/W							
0h							

Table 5-864. CPSW_NC_CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_VAL	R/W	0h	Time Stamp Comparison Low Value - Writing a non-zero value to the TS_Comp_Length[31:0] register causes a pulse of TS_Comp_Length RCLK periods on the TS_COMP output and a comparison event when the time_stamp counter value is equivalent to ts_comp_val.

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5.2.2.347 CPSW_NC_CPTS_TS_COMP_LEN_REG Register

5.2.2.347.1 CPSW_NC_CPTS_TS_COMP_LEN_REG Register (Offset = 3D01Ch) [reset = 0h]

Time Stamp Comparison Length Register

Return to Summary Table

Table 5-865. Instance Table

Instance Name	Physical Address
CPSW0	5283 D01Ch + formula

Figure 5-428. CPSW_NC_CPTS_TS_COMP_LEN_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_LENGTH							
R/W							
0h							

Table 5-866. CPSW_NC_CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_LENGTH	R/W	0h	Time Stamp Comparison Length - Writing a non-zero value to this field enables the time stamp comparison event and output. This value should be zero when the TS_Comp_Low and TS_Comp_High registers are written.

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5.2.2.348 CPSW_NC_CPTS_INTSTAT_RAW_REG Register

5.2.2.348.1 CPSW_NC_CPTS_INTSTAT_RAW_REG Register (Offset = 3D020h) [reset = 0h]

Interrupt Status Register Raw

Return to Summary Table

Table 5-867. Instance Table

Instance Name	Physical Address
CPSW0	5283 D020h + formula

Figure 5-429. CPSW_NC_CPTS_INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_RAW
NONE							R/W
0h							0h

Table 5-868. CPSW_NC_CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable). Writable when int_test = 1 A one in this bit indicates that there are one or more events in the event FIFO.

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5.2.2.349 CPSW_NC_CPTS_INTSTAT_MASKED_REG Register

5.2.2.349.1 CPSW_NC_CPTS_INTSTAT_MASKED_REG Register (Offset = 3D024h) [reset = 0h]

Interrupt Status Register Masked

Return to Summary Table

Table 5-869. Instance Table

Instance Name	Physical Address
CPSW0	5283 D024h + formula

Figure 5-430. CPSW_NC_CPTS_INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND
NONE							R
0h							0h

Table 5-870. CPSW_NC_CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable)

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5.2.2.350 CPSW_NC_CPTS_INT_ENABLE_REG Register

5.2.2.350.1 CPSW_NC_CPTS_INT_ENABLE_REG Register (Offset = 3D028h) [reset = 0h]

Interrupt Enable Register

Return to Summary Table

Table 5-871. Instance Table

Instance Name	Physical Address
CPSW0	5283 D028h + formula

Figure 5-431. CPSW_NC_CPTS_INT_ENABLE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_EN
NONE							R/W
0h							0h

Table 5-872. CPSW_NC_CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable

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5.2.2.351 CPSW_NC_CPTS_TS_COMP_NUDGE_REG Register

5.2.2.351.1 CPSW_NC_CPTS_TS_COMP_NUDGE_REG Register (Offset = 3D02Ch) [reset = 0h]

Time Stamp Comparison Nudge Register

Return to Summary Table

Table 5-873. Instance Table

Instance Name	Physical Address
CPSW0	5283 D02Ch + formula

Figure 5-432. CPSW_NC_CPTS_TS_COMP_NUDGE_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 5-874. CPSW_NC_CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	Timestamp Comparison Nudge Value - This two's complement number is added to the ts_comp_length[31:0] value to increase or decrease the TS_COMP length by the ts_comp_nudge amount. Only a single high or low time is adjusted and the ts_comp_nudge value is cleared to zero when the nudge has occurred.

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5.2.2.352 CPSW_NC_CPTS_EVENT_POP_REG Register

5.2.2.352.1 CPSW_NC_CPTS_EVENT_POP_REG Register (Offset = 3D030h) [reset = 0h]

Event Pop Register

Return to Summary Table

Table 5-875. Instance Table

Instance Name	Physical Address
CPSW0	5283 D030h + formula

Figure 5-433. CPSW_NC_CPTS_EVENT_POP_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EVENT_POP
NONE							W
0h							0h

Table 5-876. CPSW_NC_CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EVENT_POP	W	0h	Event Pop - When a logic high is written to this bit an event is popped off the event FIFO. The event FIFO pop occurs as part of the interrupt process after the event has been read from the Event_0-3 registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt.

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5.2.2.353 CPSW_NC_CPTS_EVENT_0_REG Register

5.2.2.353.1 CPSW_NC_CPTS_EVENT_0_REG Register (Offset = 3D034h) [reset = 0h]

Event 0 Register

Return to Summary Table

Table 5-877. Instance Table

Instance Name	Physical Address
CPSW0	5283 D034h + formula

Figure 5-434. CPSW_NC_CPTS_EVENT_0_REG Name Register

31	30	29	28	27	26	25	24
TIME_STAMP							
R							
0h							
23	22	21	20	19	18	17	16
TIME_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
TIME_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
TIME_STAMP							
R							
0h							

Table 5-878. CPSW_NC_CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp lower 32-bits - The timestamp is valid for transmit, receive, and time stamp push event types. The timestamp value is not valid for counter roll event types.

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5.2.2.354 CPSW_NC_CPTS_EVENT_1_REG Register

5.2.2.354.1 CPSW_NC_CPTS_EVENT_1_REG Register (Offset = 3D038h) [reset = 0h]

Event 1 Register

Return to Summary Table

Table 5-879. Instance Table

Instance Name	Physical Address
CPSW0	5283 D038h + formula

Figure 5-435. CPSW_NC_CPTS_EVENT_1_REG Name Register

31	30	29	28	27	26	25	24
RESERVED		PREMPT_QUEUE	PORT_NUMBER				
NONE		R	R				
0h		0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EVENT_TYPE				MESSAGE_TYPE			
R				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SEQUENCE_ID							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SEQUENCE_ID							
R							
0h							

Table 5-880. CPSW_NC_CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29	PREMPT_QUEUE	R	0h	Prempt Queue (iet_incl = 1) - 0 - The packet was received/transmitted on the express queue. 1 - The packet was received/transmitted on the prempt queue.
28:24	PORT_NUMBER	R	0h	Port Number - indicates the port number (encoded) of an Ethernet event or the encoded hardware timestamp number.
23:20	EVENT_TYPE	R	0h	Time Sync Event Type - 0000 - Time Stamp Push Event 0001 - Time Stamp Rollover Event 0010 - Time Stamp Half Rollover Event 0011 - Hardware Time Stamp Push Event 0100 - Ethernet Receive Event 0101 - Ethernet Transmit Event 0110 - Time Stamp Compare Event 0111 - Host Transmit Event 1000 - reserved ... 1111 - reserved
19:16	MESSAGE_TYPE	R	0h	Message type - The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.
15:0	SEQUENCE_ID	R	0h	Sequence ID - The 16-bit sequence id is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

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5.2.2.355 CPSW_NC_CPTS_EVENT_2_REG Register

5.2.2.355.1 CPSW_NC_CPTS_EVENT_2_REG Register (Offset = 3D03Ch) [reset = 0h]

Event 2 Register

Return to Summary Table

Table 5-881. Instance Table

Instance Name	Physical Address
CPSW0	5283 D03Ch + formula

Figure 5-436. CPSW_NC_CPTS_EVENT_2_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
DOMAIN							
R							
0h							

Table 5-882. CPSW_NC_CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	DOMAIN	R	0h	Domain - The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

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5.2.2.356 CPSW_NC_CPTS_EVENT_3_REG Register

5.2.2.356.1 CPSW_NC_CPTS_EVENT_3_REG Register (Offset = 3D040h) [reset = 0h]

Event 3 Register

Return to Summary Table

Table 5-883. Instance Table

Instance Name	Physical Address
CPSW0	5283 D040h + formula

Figure 5-437. CPSW_NC_CPTS_EVENT_3_REG Name Register

31	30	29	28	27	26	25	24
TIME_STAMP							
R							
0h							
23	22	21	20	19	18	17	16
TIME_STAMP							
R							
0h							
15	14	13	12	11	10	9	8
TIME_STAMP							
R							
0h							
7	6	5	4	3	2	1	0
TIME_STAMP							
R							
0h							

Table 5-884. CPSW_NC_CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TIME_STAMP	R	0h	Time Stamp - The timestamp upper 32-bits are valid for transmit, receive, and time stamp push event types. This value is zero in 32-bit mode.

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5.2.2.357 CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG Register

5.2.2.357.1 CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 3D044h) [reset = 0h]

Time Stamp Load High Value Register

Return to Summary Table

Table 5-885. Instance Table

Instance Name	Physical Address
CPSW0	5283 D044h + formula

Figure 5-438. CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_LOAD_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_LOAD_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_LOAD_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_LOAD_VAL							
R/W							
0h							

Table 5-886. CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_LOAD_VAL	R/W	0h	Time Stamp Load high Value - Writing the ts_load_en bit causes the value contained in this register (and the ts_load[63:0]) to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register. This value is unused in 32-bit mode.

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5.2.2.358 CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG Register

5.2.2.358.1 CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 3D048h) [reset = 0h]

Time Stamp Comparison High Value Register

Return to Summary Table

Table 5-887. Instance Table

Instance Name	Physical Address
CPSW0	5283 D048h + formula

Figure 5-439. CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_COMP_HIGH_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_COMP_HIGH_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_COMP_HIGH_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_COMP_HIGH_VAL							
R/W							
0h							

Table 5-888. CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_COMP_HIGH_VAL	R/W	0h	Time Stamp Comparison High Value - Writing a non-zero value to the TS_Comp_Length[31:0] register causes a pulse of TS_Comp_Length RCLK periods on the TS_COMP output and a comparison event when the time_stamp counter value is equivalent to ts_comp_val[63:0]. This value is unused in 32-bit mode. The upper 32-bits in this register should be written before the lower 32-bits in the TS_Comp_Low register.

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5.2.2.359 CPSW_NC_CPTS_TS_ADD_VAL_REG Register

5.2.2.359.1 CPSW_NC_CPTS_TS_ADD_VAL_REG Register (Offset = 3D04Ch) [reset = 0h]

TS Add Value Register

Return to Summary Table

Table 5-889. Instance Table

Instance Name	Physical Address
CPSW0	5283 D04Ch + formula

Figure 5-440. CPSW_NC_CPTS_TS_ADD_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					ADD_VAL		
NONE					R/W		
0h					0h		

Table 5-890. CPSW_NC_CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	ADD_VAL	R/W	0h	The ts_add_value[2:0] is added to 1 to comprise the timestamp increment value. The timestamp increment value is added to the current timestamp (time_stamp[63:0]) on each RCLK. The timestamp increment value can be adjusted by nudge and ppm also. The ts_add_val[2:0] value may be non-zero in 64-bit mode only.

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5.2.2.360 CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG Register

5.2.2.360.1 CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 3D050h) [reset = 0h]

Time Stamp PPM Low Value Register

Return to Summary Table

Table 5-891. Instance Table

Instance Name	Physical Address
CPSW0	5283 D050h + formula

Figure 5-441. CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG Name Register

31	30	29	28	27	26	25	24
TS_PPM_LOW_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
TS_PPM_LOW_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
TS_PPM_LOW_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
TS_PPM_LOW_VAL							
R/W							
0h							

Table 5-892. CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TS_PPM_LOW_VAL	R/W	0h	Time Stamp PPM Low Value - The 64-bit PPM value takes effect when this low value is written. The high value should be written first. Note: There should be at least 10 clocks in between writes to the low register to ensure that the previous operation has been seen.

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5.2.2.361 CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG Register

5.2.2.361.1 CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 3D054h) [reset = 0h]

Time Stamp PPM High Value Register

Return to Summary Table

Table 5-893. Instance Table

Instance Name	Physical Address
CPSW0	5283 D054h + formula

Figure 5-442. CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						TS_PPM_HIGH_VAL	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TS_PPM_HIGH_VAL							
R/W							
0h							

Table 5-894. CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	TS_PPM_HIGH_VAL	R/W	0h	Time Stamp PPM High Value - This value should be written first (before the low value is written). The minimum value of the ts_ppm is 0x400 (all 42 bits).

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5.2.2.362 CPSW_NC_CPTS_TS_NUDGE_VAL_REG Register

5.2.2.362.1 CPSW_NC_CPTS_TS_NUDGE_VAL_REG Register (Offset = 3D058h) [reset = 0h]

Time Stamp Nudge Value Register

Return to Summary Table

Table 5-895. Instance Table

Instance Name	Physical Address
CPSW0	5283 D058h + formula

Figure 5-443. CPSW_NC_CPTS_TS_NUDGE_VAL_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
TS_NUDGE_VAL							
R/W							
0h							

Table 5-896. CPSW_NC_CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	TS_NUDGE_VAL	R/W	0h	Timestamp Nudge Value - This two's complement number is added to the time_stamp[63:0] value to increase or decrease the timestamp value by the ts_nudge amount. The ts_nudge value is cleared to zero when the nudge has occurred.

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5.2.2.363 CPSW_NC_CPTS_TS_CONFIG Register

5.2.2.363.1 CPSW_NC_CPTS_TS_CONFIG Register (Offset = 3D0D0h) [reset = 2002h]

Time Stamp Configuration Read

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Table 5-897. Instance Table

Instance Name	Physical Address
CPSW0	5283 D0D0h + formula

Figure 5-444. CPSW_NC_CPTS_TS_CONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
EVNT_FIFO_DEPTH							
R							
20h							
7	6	5	4	3	2	1	0
NUM_GENF							
R							
2h							

Table 5-898. CPSW_NC_CPTS_TS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	EVNT_FIFO_DEPTH	R	20h	This is the configured value for the depth of the event FIFO. This parameter is passed in at module generation.
7:0	NUM_GENF	R	2h	This is the configured value for the number of GENF outputs. This parameter is passed in at module generation.

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5.2.2.364 CPSW_NC_ALE_MOD_VER Register

5.2.2.364.1 CPSW_NC_ALE_MOD_VER Register (Offset = 3E000h) [reset = 291105h]

The Module and Version Register identifies the module identifier and revision of the ALE_3g512e module.

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Table 5-899. Instance Table

Instance Name	Physical Address
CPSW0	5283 E000h + formula

Figure 5-445. CPSW_NC_ALE_MOD_VER Name Register

31	30	29	28	27	26	25	24
MODULE_ID							
R							
29h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
29h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL_VERSION					MAJOR_REVISION		
R					R		
2h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM_REVISION		MINOR_REVISION					
R		R					
0h		5h					

Table 5-900. CPSW_NC_ALE_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODULE_ID	R	29h	ALE_3g512e module ID.
15:11	RTL_VERSION	R	2h	RTL Version.
10:8	MAJOR_REVISION	R	1h	Major Revision.
7:6	CUSTOM_REVISION	R	0h	Custom Revision.
5:0	MINOR_REVISION	R	5h	Minor Revision.

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5.2.2.365 CPSW_NC_ALE_STATUS Register

5.2.2.365.1 CPSW_NC_ALE_STATUS Register (Offset = 3E004h) [reset = 80000400h]

The ALE status provides information on the ALE configuration and state. The ramdepth is used to determine how IPv6 entries are stored in the table. IPv6 entries are stored in two entries where IPv6 Entry Hi is designated by the odd slice index and Lo is designated by the even slice index. The slice index is above the ram depth like {SliceIndex,RamIndex}. So, for a 64 deep RAM index of 0x005, the Hi portion of the IPv6 entry is located at 0x005|(0x040) and the Lo portion is located at 0x005 & (~0x040).

Return to Summary Table

Table 5-901. Instance Table

Instance Name	Physical Address
CPSW0	5283 E004h + formula

Figure 5-446. CPSW_NC_ALE_STATUS Name Register

31	30	29	28	27	26	25	24
UREGANDREG MSK12	UREGANDREG MSK08	RESERVED					
R	R	NONE					
1h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POLCNTDIV8							
R							
4h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMDEPTH128	RAMDEPTH32	RESERVED	KLUENTRIES				
R	R	NONE	R				
0h	0h	0h	0h				

Table 5-902. CPSW_NC_ALE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UREGANDREGMSK12	R	1h	When set, the unregistered multicast field is a mask versus an index on 12 bit boundary in the ALE table.
30	UREGANDREGMSK08	R	0h	When set, the unregistered multicast field is a mask versus an index on 8 bit boundary in the ALE table.
29:16	RESERVED	NONE	0h	Reserved
15:8	POLCNTDIV8	R	4h	This is the number of Classifiers the ALE implements divided by 8. A value of 4 indicates 32 policer engines total.
7	RAMDEPTH128	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 128 if both ramdepth128 and ramdepth32 are zero the depth is 64.
6	RAMDEPTH32	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 32 if both ramdepth128 and ramdepth32 are zero the depth is 64.
5	RESERVED	NONE	0h	Reserved
4:0	KLUENTRIES	R	0h	This is the number of table entries total divided by 1024. A value of 1 indicates 1024 table entries. A value of 8 indicates 8192 table entries.

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5.2.2.366 CPSW_NC_ALE_CONTROL Register

5.2.2.366.1 CPSW_NC_ALE_CONTROL Register (Offset = 3E008h) [reset = 0h]

The ALE Control Register is used to set the ALE modes used for all ports.

Return to Summary Table

Table 5-903. Instance Table

Instance Name	Physical Address
CPSW0	5283 E008h + formula

Figure 5-447. CPSW_NC_ALE_CONTROL Name Register

31	30	29	28	27	26	25	24
ENABLE_ALE	CLEAR_TABLE	AGE_OUT_NOW	RESERVED			MIRROR_DP	
R/W	R/W	R/W	NONE			R/W	
0h	0h	0h	0h			0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
UPD_BW_CTRL			RESERVED			MIRROR_TOP	
R/W			NONE			R/W	
0h			0h			0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UPD_STATIC	LRN_HOST_DST	UVLAN_NO_LEARN	MIRROR_MEN	MIRROR_DEN	MIRROR_SEN	RESERVED	EN_HOST_UNI_FLOOD
R/W	R/W	R/W	R/W	R/W	R/W	NONE	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LEARN_NO_VLANID	ENABLE_VID0_MODE	ENABLE_OUI_DENY	ENABLE_BYPASS	BCAST_MCAST_CTL	ALE_VLAN_AWARE	ENABLE_AUTH_MODE	ENABLE_RATE_LIMIT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-904. CPSW_NC_ALE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_ALE	R/W	0h	Enable ALE 0 - Drop all packets 1 - Enable ALE packet processing
30	CLEAR_TABLE	R/W	0h	Clear ALE address table - Setting this bit causes the ALE hardware to write all table bit values to zero. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as one because the read is blocked until the clear table is completed at which time this bit is cleared to zero.
29	AGE_OUT_NOW	R/W	0h	Age Out Address Table Now - Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes four times the number of table entries clock cycles (4096 cycles for 1K addresses) best case (no ale packet processing during ageout) and sixty five times the number of table entries clock cycles (66560 cycles for 1K addresses) absolute worst case.
28:26	RESERVED	NONE	0h	Reserved
25:24	MIRROR_DP	R/W	0h	Mirror Destination Port - This field defines the port to which destination traffic destined will be duplicated. That is all traffic that is forwarded to this port will also be mirrored to the mirror_top port.

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Table 5-904. CPSW_NC_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:21	UPD_BW_CTRL	R/W	0h	The upd_bw_ctrl field allows for up to 8 times the rate in which adds, updates, touches, writes, and aging updates can occur. At frequencies of 350Mhz, the table update rate should be at it lowest or 5 Million updates per second. When operating the switch core at frequencies or above, the upd_bw_ctrl can be programmed more aggressive. If the upd_bw_ctrl is set but the frequency of the switch subsystem is below the associated value, ALE will drop packets due to insufficient time to complete lookup under high traffic loads. 0 - 350Mhz, 5M 1 - 359Mhz, 11M 2 - 367Mhz, 16M 3 - 375Mhz, 22M 4 - 384Mhz, 28M 5 - 392Mhz, 34M 6 - 400Mhz, 39M 7 - 409Mhz, 45M
20:18	RESERVED	NONE	0h	Reserved
17:16	MIRROR_TOP	R/W	0h	Mirror To Port - This field defines the destination port for the mirror traffic. If the traffic is received or transmitted on the mirror destination port it will not be duplicated. Traffic defined as mirror traffic only may be dropped by the switch due to congestion.
15	UPD_STATIC	R/W	0h	Update Static Entries - A static Entry is an entry that is not agable. When clear this bit will prevent any static entry (agable bit clear) from being updated due to port change. When set it allows static entries (agable bit clear) to update the source port if required. This bit should normally be '0' for most switch configurations.
14	LRN_HOST_DST	R/W	0h	Learn Host Destination - This field is set to only learn unicast packet source addresses that are destined to the host port. This bit is only valid for 3 port switches and allows the ALE table to only contain addresses the host port is concerned about. This bit is affectively disabled when en_host_uni_flood is set since any unknown unicast is also sent to the host port for extended bridging operations.
13	UVLAN_NO_LEARN	R/W	0h	Unknown VLAN No Learn - This field when set will prevent source addresses of unknown VLAN IDs from being automatically added into the look up table if learning is enabled.
12	MIRROR_MEN	R/W	0h	Mirror Match Entry Enable - This field enables the match mirror option. When this bit is set any traffic whose destination, source, VLAN or OUI matches the mirror_midx entry index will have that traffic also sent to the mirror_top port.
11	MIRROR_DEN	R/W	0h	Mirror Destination Port Enable - This field enables the destination port mirror option. When this bit is set any traffic destined for the mirror_dp port will have its transmit traffic also sent to the mirror_top port.
10	MIRROR_SEN	R/W	0h	Mirror Source Port Enable - This field enables the source port mirror option. When this bit is set any port with the pX_mirror_sp set in the ALE Port Control registers set will have its received traffic also sent to the mirror_top port.
9	RESERVED	NONE	0h	Reserved
8	EN_HOST_UNI_FLOOD	R/W	0h	Unknown unicast packets flood to host 0 - unknown unicast packets are not sent to the host 1 - unknown unicast packets flood to host port as well as other ports
7	LEARN_NO_VLANID	R/W	0h	Learn No VID - 0 - VID is learned with the source address 1 - VID is not learned with the source address (source address is not tied to VID). Determines the entry type.
6	ENABLE_VID0_MODE	R/W	0h	Enable VLAN ID = 0 Mode 0 - Process the priority tagged packet with VID = PORT_VLAN[11:0]. 1 - Process the priority tagged packet with VID = 0.

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Table 5-904. CPSW_NC_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ENABLE_OUI_DENY	R/W	0h	Enable OUI Deny Mode - When set, any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches a supervisory destination address table entry. When cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory destination address table entry.
4	ENABLE_BYPASS	R/W	0h	ALE Bypass - When set, packets received on non-host ports are sent to the host. It is expected that packets from the host are directed to the particular port. 0 - no bypass 1 - bypass the ALE
3	BCAST_MCAST_CTL	R/W	0h	Rate Limit Transmit mode 0 - Broadcast and multicast rate limit counters are received port based 1 - Broadcast and multicast rate limit counters are transmit port based
2	ALE_VLAN_AWARE	R/W	0h	ALE VLAN Aware - Determines how traffic is forwarded using VLAN rules. 0 - Simple switch rules, packets forwarded to all ports for unknown destinations. 1 - VLAN Aware rules, packets forwarded based on VLAN members
1	ENABLE_AUTH_MODE	R/W	0h	Enable MAC Authorization Mode - Mac authorization mode requires that all table entries be made by the host software. There is no auto learning of addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the super table entry bit set). 0 - The ALE is not in MAC authorization mode 1 - The ALE is in MAC authorization mode
0	ENABLE_RATE_LIMIT	R/W	0h	Enable Broadcast and Multicast Rate Limit 0 - Broadcast/Multicast rates not limited 1 - Broadcast/Multicast packet reception limited to the port control register rate limit fields.

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5.2.2.367 CPSW_NC_ALE_CTRL2 Register

5.2.2.367.1 CPSW_NC_ALE_CTRL2 Register (Offset = 3E00Ch) [reset = 0h]

The ALE Control 2 Register is used to set the extended features used for all ports.

Return to Summary Table

Table 5-905. Instance Table

Instance Name	Physical Address
CPSW0	5283 E00Ch + formula

Figure 5-448. CPSW_NC_ALE_CTRL2 Name Register

31	30	29	28	27	26	25	24
TRK_EN_DST	TRK_EN_SRC	TRK_EN_PRI	RESERVED	TRK_EN_IVLAN	RESERVED	TRK_EN_SIP	TRK_EN_DIP
R/W	R/W	R/W	NONE	R/W	NONE	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DROP_BADLEN	NODROP_SRCMCST	DEFNOFRAG	DEFLMTNXTHDR	RESERVED	TRK_BASE		
R/W	R/W	R/W	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MULTIHOST	RESERVED						MIRROR_MIDX
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MIRROR_MIDX							
R/W							
0h							

Table 5-906. CPSW_NC_ALE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRK_EN_DST	R/W	0h	Trunk Enable Destination Address - This field enables the destination MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
30	TRK_EN_SRC	R/W	0h	Trunk Enable Source Address - This field enables the source MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
29	TRK_EN_PRI	R/W	0h	Trunk Enable Priority - This field enables the VLAN Priority bits to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. In the event that DSCP mapping is enabled and there is no VLAN the DSCP priority will be used. For all other non IP frames without VLAN the port default priority is used.
28	RESERVED	NONE	0h	Reserved
27	TRK_EN_IVLAN	R/W	0h	Trunk Enable Inner VLAN - This field enables the inner VLAN ID value (C-VLANID) to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
26	RESERVED	NONE	0h	Reserved
25	TRK_EN_SIP	R/W	0h	Trunk Enable Source IP Address - This field enables the source IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.

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Table 5-906. CPSW_NC_ALE_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	TRK_EN_DIP	R/W	0h	Trunk Enable Destination IP Address - This field enables the destination IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
23	DROP_BADLEN	R/W	0h	Drop Bad Length will drop any packet that the 802.3 length field is larger than the packet. Ethertypes 0-1500 are 802.3 lengths, all others are Ether types.
22	NODROP_SRCMCST	R/W	0h	No Drop Source Multicast will disable the dropping of any source address with the multicast bit set.
21	DEFNOFRAG	R/W	0h	Default No Frag field will cause an IPv4 fragmented packet to be dropped if a VLAN entry is not found.
20	DEFLMTNXTHDR	R/W	0h	Default limit next header field will cause an IPv4 protocol or IPv6 next header packet to be dropped if a VLAN entry is not found and the protocol or next header does not match the ALE_NXT_HDR register values.
19	RESERVED	NONE	0h	Reserved
18:16	TRK_BASE	R/W	0h	Trunk Base - This field is the hash formula starting value. Changing this value will cause the packet distribution on trunk ports to be changed. If all the trk_en_dst, trk_en_src, trk_en_pri and trk_en_vlan are '0', this value is used as the distribution index. That is a '0' will select the 1st bit of an 'N' link trunk, a '1' will select the second, etc. Below is the distribution across the trunk links. The first number in the italic sequence indicates the traffic is sent to the lowest numbered port of a trunk group. For example if you have a 3 port trunk, the hash result 0 will go to the base port (0), hash result 1 will go to the highest port of the trunk group (2), hash result 2 will go to the middle port (1), etc. 1 - 00000000 2 - 01010101 3 - 02102102 4 - 03210321
15	MULTIHOST	R/W	0h	The ~multihost allows host traffic to be sent bact to the host if the DA is market for the host port.
14:9	RESERVED	NONE	0h	Reserved
8:0	MIRROR_MIDX	R/W	0h	Mirror Index - This field is the ALE lookup table entry index that when a match occurs will cause this traffic to be mirrored to the mirror_top port. That is any VLAN, ONU or address with or withou VLAN can be selected for traffic mirroring.

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5.2.2.368 CPSW_NC_ALE_PRESCALE Register

5.2.2.368.1 CPSW_NC_ALE_PRESCALE Register (Offset = 3E010h) [reset = 0h]

The ALE Prescale Register is used to set the Broadcast and Multicast rate limiting prescaler value.

Return to Summary Table

Table 5-907. Instance Table

Instance Name	Physical Address
CPSW0	5283 E010h + formula

Figure 5-449. CPSW_NC_ALE_PRESCALE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				ALE_PRESCALE			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ALE_PRESCALE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ALE_PRESCALE							
R/W							
0h							

Table 5-908. CPSW_NC_ALE_PRESCALE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	ALE_PRESCALE	R/W	0h	ALE Prescale - The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 0x10. The prescaler is off when the value is zero.

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5.2.2.369 CPSW_NC_ALE_AGING_CTRL Register

5.2.2.369.1 CPSW_NC_ALE_AGING_CTRL Register (Offset = 3E014h) [reset = 0h]

The ALE Aging Control sets the aging interval which will cause periodic aging to occur. This value specifies the minimum time between aging starts.

Return to Summary Table

Table 5-909. Instance Table

Instance Name	Physical Address
CPSW0	5283 E014h + formula

Figure 5-450. CPSW_NC_ALE_AGING_CTRL Name Register

31	30	29	28	27	26	25	24
PRESCALE_2_DISABLE	PRESCALE_1_DISABLE	RESERVED					
R/W	R/W	NONE					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ALE_AGING_TIMER							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ALE_AGING_TIMER							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ALE_AGING_TIMER							
R/W							
0h							

Table 5-910. CPSW_NC_ALE_AGING_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRESCALE_2_DISABLE	R/W	0h	ALE Prescaler 2 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
30	PRESCALE_1_DISABLE	R/W	0h	ALE Prescaler 1 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
29:24	RESERVED	NONE	0h	Reserved
23:0	ALE_AGING_TIMER	R/W	0h	ALE Aging Timer - This field specifies the number of clock cycles times 1,000,000 between aging operations.

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5.2.2.370 CPSW_NC_ALE_NXT_HDR Register

5.2.2.370.1 CPSW_NC_ALE_NXT_HDR Register (Offset = 3E01Ch) [reset = 0h]

The ALE Next Header is used to limit the IPv6 Next header or IPv4 Protocol values found in the IP header. It is enabled via the ~iLmtNxtHdr bit in the VLAN entry. All four ~iip_nxt_hdr0-3 are compared when enabled, so if only one is required, set them all to the one value to be tested.

Return to Summary Table

Table 5-911. Instance Table

Instance Name	Physical Address
CPSW0	5283 E01Ch + formula

Figure 5-451. CPSW_NC_ALE_NXT_HDR Name Register

31	30	29	28	27	26	25	24
IP_NXT_HDR3							
R/W							
0h							
23	22	21	20	19	18	17	16
IP_NXT_HDR2							
R/W							
0h							
15	14	13	12	11	10	9	8
IP_NXT_HDR1							
R/W							
0h							
7	6	5	4	3	2	1	0
IP_NXT_HDR0							
R/W							
0h							

Table 5-912. CPSW_NC_ALE_NXT_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	IP_NXT_HDR3	R/W	0h	The ip_nxt_hdr3 is the forth protocol or next header compared when enabled.
23:16	IP_NXT_HDR2	R/W	0h	The ip_nxt_hdr2 is the third protocol or next header compared when enabled.
15:8	IP_NXT_HDR1	R/W	0h	The ip_nxt_hdr1 is the second protocol or next header compared when enabled.
7:0	IP_NXT_HDR0	R/W	0h	The ip_nxt_hdr0 is the first protocol or next header compared when enabled.

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5.2.2.371 CPSW_NC_ALE_TBLCTL Register

5.2.2.371.1 CPSW_NC_ALE_TBLCTL Register (Offset = 3E020h) [reset = 0h]

The ALE table control register is used to read or write that ALE table entries. After writing to this register any read or write to any ALE register will be stalled until the read or write operation completes.

Return to Summary Table

Table 5-913. Instance Table

Instance Name	Physical Address
CPSW0	5283 E020h + formula

Figure 5-452. CPSW_NC_ALE_TBLCTL Name Register

31	30	29	28	27	26	25	24
TABLEWR	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							TABLEIDX
NONE							R/W
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TABLEIDX							
R/W							
0h							

Table 5-914. CPSW_NC_ALE_TBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TABLEWR	R/W	0h	Table Write - This bit is used to write the table words to the lookup table. 0 - Table Read Operation is performed. The contents of the TABLEIDX entry will be read into the ALE_TBLWx registers 1 - Table write operation is performed. This will take the current contents from the ALE_TBLWx registers and write them to the table at the specified TABLEIDX.
30:9	RESERVED	NONE	0h	Reserved
8:0	TABLEIDX	R/W	0h	The table index is used to determine which lookup table entry is read or written.

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5.2.2.372 CPSW_NC_ALE_TBLW2 Register

5.2.2.372.1 CPSW_NC_ALE_TBLW2 Register (Offset = 3E034h) [reset = 0h]

The ALE Table Word 2 is the most significant word of an ALE table entry.

Return to Summary Table

Table 5-915. Instance Table

Instance Name	Physical Address
CPSW0	5283 E034h + formula

Figure 5-453. CPSW_NC_ALE_TBLW2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	TABLEWRD2						
NONE	R/W						
0h	0h						

Table 5-916. CPSW_NC_ALE_TBLW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6:0	TABLEWRD2	R/W	0h	Table Entry bits [71:64]

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5.2.2.373 CPSW_NC_ALE_TBLW1 Register

5.2.2.373.1 CPSW_NC_ALE_TBLW1 Register (Offset = 3E038h) [reset = 0h]

The ALE Table Word 1 is the middle word of an ALE table entry.

Return to Summary Table

Table 5-917. Instance Table

Instance Name	Physical Address
CPSW0	5283 E038h + formula

Figure 5-454. CPSW_NC_ALE_TBLW1 Name Register

31	30	29	28	27	26	25	24
TABLEWRD1							
R/W							
0h							
23	22	21	20	19	18	17	16
TABLEWRD1							
R/W							
0h							
15	14	13	12	11	10	9	8
TABLEWRD1							
R/W							
0h							
7	6	5	4	3	2	1	0
TABLEWRD1							
R/W							
0h							

Table 5-918. CPSW_NC_ALE_TBLW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TABLEWRD1	R/W	0h	Table Entry bits [63:32]

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5.2.2.374 CPSW_NC_ALE_TBLW0 Register

5.2.2.374.1 CPSW_NC_ALE_TBLW0 Register (Offset = 3E03Ch) [reset = 0h]

The ALE Table Word 0 is the least significant word of an ALE table entry.

Return to Summary Table

Table 5-919. Instance Table

Instance Name	Physical Address
CPSW0	5283 E03Ch + formula

Figure 5-455. CPSW_NC_ALE_TBLW0 Name Register

31	30	29	28	27	26	25	24
TABLEWRD0							
R/W							
0h							
23	22	21	20	19	18	17	16
TABLEWRD0							
R/W							
0h							
15	14	13	12	11	10	9	8
TABLEWRD0							
R/W							
0h							
7	6	5	4	3	2	1	0
TABLEWRD0							
R/W							
0h							

Table 5-920. CPSW_NC_ALE_TBLW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TABLEWRD0	R/W	0h	Table Entry bits [31:0]

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5.2.2.375 CPSW_NC_ALE_I0_PORTCTL0_J Register

5.2.2.375.1 CPSW_NC_ALE_I0_PORTCTL0_J Register (Offset = 3E040h) [reset = 0h]

The ALE Port Control Register sets the port specific modes of operation.

Return to Summary Table

Table 5-921. Instance Table

Instance Name	Physical Address
CPSW0	5283 E040h + formula

Figure 5-456. CPSW_NC_ALE_I0_PORTCTL0_j Name Register

31	30	29	28	27	26	25	24
I0_REG_P0_BCAST_LIMIT							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
I0_REG_P0_MCAST_LIMIT							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
I0_REG_P0_DROP_DOUBLE_VLAN	I0_REG_P0_DROP_DUAL_VLAN	I0_REG_P0_MACONLY_CAF	I0_REG_P0_DIS_PAUTHMOD	I0_REG_P0_MACONLY	I0_REG_P0_TRUNKEN	I0_REG_P0_TRUNKNUM	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I0_REG_P0_MIRROR_SP	RESERVED	I0_REG_P0_NO_SA_UPDATE	I0_REG_P0_NO_LEARN	I0_REG_P0_VID_INGRESS_CHECK	I0_REG_P0_DROP_UN_TAGGED	I0_REG_P0_PORTSTATE	
R/W	NONE	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 5-922. CPSW_NC_ALE_I0_PORTCTL0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	I0_REG_P0_BCAST_LIMIT	R/W	0h	Broadcast Packet Rate Limit - Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
23:16	I0_REG_P0_MCAST_LIMIT	R/W	0h	Multicast Packet Rate Limit - Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field.The mcast_limit is the number of Multicast packets that will be forwaded per ale_prescale time.
15	I0_REG_P0_DROP_DOUBLE_VLAN	R/W	0h	Drop Double VLAN - When set cause any received packet with double VLANs to be dropped. That is if there are two ctag or two stag fields in the packet it will be dropped.
14	I0_REG_P0_DROP_DUAL_VLAN	R/W	0h	Drop Dual VLAN - When set will cause any received packet with dual VLAN stag followed by ctag to be dropped.

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Table 5-922. CPSW_NC_ALE_I0_PORTCTL0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	I0_REG_P0_MACONLY_CAF	R/W	0h	Mac Only Copy All Frames - When set a Mac Only port will transfer all received good frames to the host. When clear a Mac Only port will transfer packets to the host based on ALE destination address lookup operation (which operates more like an Ethernet Mac). A Mac Only port is a port with maconly set.
12	I0_REG_P0_DIS_PAUTHMOD	R/W	0h	Disable Port authorization - When set will allow unknown addresses to arrive on a switch in authorization mode. It is intended for device to device network connection on ports which do not require MACSEC encryption.
11	I0_REG_P0_MACONLY	R/W	0h	MAC Only - When set enables this port be treated like a MAC port for the host. All traffic received is only sent to the host. The host must direct traffic to this port as the lookup engine will not send traffic to the ports with the p0_maconly bit set and the p0_no_learn also set. If p0_maconly bit is set and the p0_no_learn is not set, the host can send non-directed packets that can be sent to the destination of a MacOnly port. It is also possible that The host can broadcast to all ports including MacOnly ports in this mode.
10	I0_REG_P0_TRUNKEN	R/W	0h	Trunk Enable - This field is used to enable a port into a trunk. Any port can be used as a trunk port, any two or more ports with the p0_trunken its set and having the same p0_trunknum will be placed in the same trunk. There is no requirement for trunk ports to be adjacent. If all ports are enabled in the same trunk, no traffic can flow as traffic received within a trunk is never trasnmitted out the same trunk. If only a single port is a member of a trunk, it looks like a normal port with exception of entries in the look up table will be noted as a trunk entry.
9:8	I0_REG_P0_TRUNKNUM	R/W	0h	Trunk Number - This field is used as the trunk number when the p0_trunken is also set. Ports with the same trunk number that have the p0_trunken also set will have traffic distributed within the trunk based on the result of the hash function descrived above.
7	I0_REG_P0_MIRROR_SP	R/W	0h	Mirror Source Port - This field enables the source port mirror option. When this bit is set any traffic received on the port with the reg_p0_mirror_sp bit set will have its received traffic also sent to the mirror_top port.
6	RESERVED	NONE	0h	Reserved
5	I0_REG_P0_NO_SA_UPDATE	R/W	0h	No Source Address Update - When set will not update the source addresses for this port.
4	I0_REG_P0_NO_LEARN	R/W	0h	No Learn - When set will not learn the source addresses for this port.
3	I0_REG_P0_VID_INGRESS_CHECK	R/W	0h	VLAN Ingress Check - When set if a packet received is not a member of the VLAN, the packet will be dropped.
2	I0_REG_P0_DROP_UN_TAGGED	R/W	0h	If Drop Untagged - When set will drop packets without a VLAN tag.
1:0	I0_REG_P0_PORTSTATE	R/W	0h	Port State - Defins the current port state used for lookup operations. 0 - Disabled 1 - Blocked 2 - Learning 3 - Forwarding

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5.2.2.376 CPSW_NC_ALE_UVLAN_MEMBER Register

5.2.2.376.1 CPSW_NC_ALE_UVLAN_MEMBER Register (Offset = 3E090h) [reset = 0h]

The ALE Unknown VLAN Member Mask Register is used to specify the member list for unknown VLAN ID.

Return to Summary Table

Table 5-923. Instance Table

Instance Name	Physical Address
CPSW0	5283 E090h + formula

Figure 5-457. CPSW_NC_ALE_UVLAN_MEMBER Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_MEMBER_LIST		
NONE					R/W		
0h					0h		

Table 5-924. CPSW_NC_ALE_UVLAN_MEMBER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_MEMBER_LIST	R/W	0h	Unknown VLAN Member List - Each bit represents the port member status for unknown VLANs.

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5.2.2.377 CPSW_NC_ALE_UVLAN_URCAST Register

5.2.2.377.1 CPSW_NC_ALE_UVLAN_URCAST Register (Offset = 3E094h) [reset = 0h]

The ALE Unknown VLAN Unregistered Multicast Flood Mask Register is used to specify which egress ports unregistered multicast addresses egress for the unregistered VLAN ID.

Return to Summary Table

Table 5-925. Instance Table

Instance Name	Physical Address
CPSW0	5283 E094h + formula

Figure 5-458. CPSW_NC_ALE_UVLAN_URCAST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					UVLAN_UNREG_MCAST_FLOOD_MASK		
NONE					R/W		
0h					0h		

Table 5-926. CPSW_NC_ALE_UVLAN_URCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_UNREG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Unregister Multicast Flood Mask - Each bit represents the port to which unregistered multicast are sent for unregistered VLANs.

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5.2.2.378 CPSW_NC_ALE_UVLAN_RMCAST Register

5.2.2.378.1 CPSW_NC_ALE_UVLAN_RMCAST Register (Offset = 3E098h) [reset = 0h]

The ALE Unknown VLAN Registered Multicast Flood Mask Register is used to specify which egress ports registered multicast addresses egress for the unregistered VLAN ID.

Return to Summary Table

Table 5-927. Instance Table

Instance Name	Physical Address
CPSW0	5283 E098h + formula

Figure 5-459. CPSW_NC_ALE_UVLAN_RMCAST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_REG_MCAST_FLOOD_MASK		
NONE					R/W		
0h					0h		

Table 5-928. CPSW_NC_ALE_UVLAN_RMCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_REG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Register Multicast Flood Mask - Each bit represents the port to which registered multicast are sent for unregistered VLANs. This field is ANDed with the registered multicast mask to determine the destinations for unregistered VLANs.

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5.2.2.379 CPSW_NC_ALE_UVLAN_UNTAG Register

5.2.2.379.1 CPSW_NC_ALE_UVLAN_UNTAG Register (Offset = 3E09Ch) [reset = 0h]

The ALE Unknown VLAN force Untagged Egress Mask Register is used to specify which egress ports the VLAN ID will be removed.

Return to Summary Table

Table 5-929. Instance Table

Instance Name	Physical Address
CPSW0	5283 E09Ch + formula

Figure 5-460. CPSW_NC_ALE_UVLAN_UNTAG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					UVLAN_FORCE_UNTAGGED_EGRESS		
NONE					R/W		
0h					0h		

Table 5-930. CPSW_NC_ALE_UVLAN_UNTAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	UVLAN_FORCE_UNTAGGED_EGRESS	R/W	0h	Unknown VLAN Force Untagged Egress Mask - Each bit represents the port where the VLAN will be removed for unregistered VLANs.

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5.2.2.380 CPSW_NC_ALE_FAST_LUT Register

5.2.2.380.1 CPSW_NC_ALE_FAST_LUT Register (Offset = 3E0B4h) [reset = 0h]

The Fast LUT registers allows the ports to be placed in Fast LUT mode.

Return to Summary Table

Table 5-931. Instance Table

Instance Name	Physical Address
CPSW0	5283 E0B4h + formula

Figure 5-461. CPSW_NC_ALE_FAST_LUT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					FAST_LUT		
NONE					R/W		
0h					0h		

Table 5-932. CPSW_NC_ALE_FAST_LUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	FAST_LUT	R/W	0h	The ~Fast_LUT field alows any port to be Fast_LUT mode, which will cause all lookup operations to start based on DA/SA and VLAN only. That is any data beyong the first 32 are not used in the lookup process.

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5.2.2.381 CPSW_NC_ALE_STAT_DIAG Register

5.2.2.381.1 CPSW_NC_ALE_STAT_DIAG Register (Offset = 3E0B8h) [reset = 0h]

The ALE Statistic Output Diagnostic Register allows the output statistics to diagnose the SW counters. This register is for diagnostice only.

Return to Summary Table

Table 5-933. Instance Table

Instance Name	Physical Address
CPSW0	5283 E0B8h + formula

Figure 5-462. CPSW_NC_ALE_STAT_DIAG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PBCAST_DIAG	RESERVED					PORT_DIAG	
R/W	NONE					R/W	
0h	0h					0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				STAT_DIAG			
NONE				R/W			
0h				0h			

Table 5-934. CPSW_NC_ALE_STAT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	PBCAST_DIAG	R/W	0h	When set and the port_diag is set to zero, will allow all ports to see the same stat diagnostic increment.
14:10	RESERVED	NONE	0h	Reserved
9:8	PORT_DIAG	R/W	0h	The port selected that a received packet will cause the selected error to increment
7:4	RESERVED	NONE	0h	Reserved

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Table 5-934. CPSW_NC_ALE_STAT_DIAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	STAT_DIAG	R/W	0h	When non-zero will cause the selected statistic to increment on the next frame received. For the selected Port. 0: Disabled 1: Destination Equal Source Drop Stat will count 2: VLAN Ingress Check Drop Stat will count 3: Source Multicast Drop Stat will count 4: Dual VLAN Drop Stat will count 5: Ether Type length error Drop Stat will count 6: Next Hop Limit Drop Stat will count 7: IPv4 Fragment Drop Stat will count 8: Classifier Hit Stat will count 9: Classifier Red Drop Stat will count 10: Classifier Yellow Drop Stat will count 11: ALE Overflow Drop Stat will count 12: Rate Limit Drop Stat will count 13: Blocked Address Drop Stat will count 14: Secure Address Drop Stat will count 15: Authorization Drop Stat will count.

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5.2.2.382 CPSW_NC_ALE_OAM_LB_CTRL Register

5.2.2.382.1 CPSW_NC_ALE_OAM_LB_CTRL Register (Offset = 3E0BCh) [reset = 0h]

The ALE OAM Control allows ports to be put into OAM Loopback, only non-supervisor packet are looped back to the source port.

Return to Summary Table

Table 5-935. Instance Table

Instance Name	Physical Address
CPSW0	5283 E0BCh + formula

Figure 5-463. CPSW_NC_ALE_OAM_LB_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					OAM_LB_CTRL		
NONE					R/W		
0h					0h		

Table 5-936. CPSW_NC_ALE_OAM_LB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2:0	OAM_LB_CTRL	R/W	0h	The oam_lb_ctrl allows any port to be put into OAM loopback, that is any packet received will be returned to the same port with an egressop of 0xFF which swaps the source and destination address. BPDUs will still flow through as normal so that OAM can be remotly requested and disabled.

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5.2.2.383 CPSW_NC_ALE_EGRESSOP Register

5.2.2.383.1 CPSW_NC_ALE_EGRESSOP Register (Offset = 3E0FCh) [reset = 0h]

The Egress Operation register allows enabled classifiers with any match like IPSA or IPDA match to use the CPSW Egress Packet Operations Inter VLAN Routing sub functions. If the packet was destined for the host or is destined to any port without any errors, but matches a clasifier that has a programmed egress opcode, it will be forwarded to the destination ports where the destination ports will use the thier egress opcode entry to modify the packet. InterVLAN Routing and mirroring need to be understood, they are orthogonal functions. Care must be taken not to violate VLAN rules as this can redirect packets based on classifier matches.

Return to Summary Table

Table 5-937. Instance Table

Instance Name	Physical Address
CPSW0	5283 E0FCh + formula

Figure 5-464. CPSW_NC_ALE_EGRESSOP Name Register

31	30	29	28	27	26	25	24
EGRESS_OP							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
EGRESS_TRK			TTL_CHECK	RESERVED			
R/W			R/W	NONE			
0h			0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DEST_PORTS		
NONE					R/W		
0h					0h		

Table 5-938. CPSW_NC_ALE_EGRESSOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	EGRESS_OP	R/W	0h	The Egress Operation defines the operation performed by the CPSW Egress Packet Operations 0: NOP : 1-n: Defines which egress Operation will be performed. This allows Inter VLAN routing to be configured for high bandwidth traffic, reducing CPU load. 0xff: Swap SA and DA of packet, this is intended to allow OAM diagnostics for a link.
23:21	EGRESS_TRK	R/W	0h	The Egress Trunk Index is the calculated trunk index from the SA, DA or VLAN if modified to that InterVLAN routing will work on trunks as well. The DA, SA and VLAN are ignored for trunk generation on InterVLAN Routing so that this field is the index generated from the Egress Op replacements elclusive or'd together into a three bit index.
20	TTL_CHECK	R/W	0h	The TTL Check will cause any packet that fails TTL checks to not be routed to the Inter VLAN Routing sub functions. The packet will be routed to the host it was destined to.
19:3	RESERVED	NONE	0h	Reserved

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Table 5-938. CPSW_NC_ALE_EGRESSOP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	DEST_PORTS	R/W	0h	The Destination Ports is a list of the ports the classified packet will be set to. If a destination is a Trunk, all the port bits for that trunck must be set.

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5.2.2.384 CPSW_NC_ALE_POLICECFG0 Register

5.2.2.384.1 CPSW_NC_ALE_POLICECFG0 Register (Offset = 3E100h) [reset = 0h]

The Policing Config 0 holds the port, frame priority and ONU address index as well as match enables for port, frame priority and ONU address matching.

Return to Summary Table

Table 5-939. Instance Table

Instance Name	Physical Address
CPSW0	5283 E100h + formula

Figure 5-465. CPSW_NC_ALE_POLICECFG0 Name Register

31	30	29	28	27	26	25	24
PORT_MEN	TRUNKID	RESERVED			PORT_NUM		RESERVED
R/W	R/W	NONE			R/W		NONE
0h	0h	0h			0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				PRI_MEN	PRI_VAL		
NONE				R/W	R/W		
0h				0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ONU_MEN	RESERVED						ONU_INDEX
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ONU_INDEX							
R/W							
0h							

Table 5-940. CPSW_NC_ALE_POLICECFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PORT_MEN	R/W	0h	Port Match Enable - Enabled port match for the selected policing/ classifier entry
30	TRUNKID	R/W	0h	Trunk ID - When set indicates the port number is a trunk group.
29:27	RESERVED	NONE	0h	Reserved
26:25	PORT_NUM	R/W	0h	Port Number - Specifies the port address to match for the selected policing/classifier entry
24:20	RESERVED	NONE	0h	Reserved
19	PRI_MEN	R/W	0h	Priority Match Enable - Enables frame priority match for the selected policing/classifier entry
18:16	PRI_VAL	R/W	0h	Priority Value - Specifies the frame priority to match for the selected policing/classifier entry
15	ONU_MEN	R/W	0h	OUI Match Enable - Enables frame ONU address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	ONU_INDEX	R/W	0h	OUI Table Entry Index - Specifies the ALE ONU address lookup table index to match for the selected policing/classifier entry

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5.2.2.385 CPSW_NC_ALE_POLICECFG1 Register

5.2.2.385.1 CPSW_NC_ALE_POLICECFG1 Register (Offset = 3E104h) [reset = 0h]

The Policing Config 1 holds the match enable/match index for the L2 Destination and L2 source addresses

Return to Summary Table

Table 5-941. Instance Table

Instance Name	Physical Address
CPSW0	5283 E104h + formula

Figure 5-466. CPSW_NC_ALE_POLICECFG1 Name Register

31	30	29	28	27	26	25	24
DST_MEN	RESERVED						DST_INDEX
R/W	NONE						R/W
0h	0h						0h
23	22	21	20	19	18	17	16
DST_INDEX							
R/W							
0h							
15	14	13	12	11	10	9	8
SRC_MEN	RESERVED						SRC_INDEX
R/W	NONE						R/W
0h	0h						0h
7	6	5	4	3	2	1	0
SRC_INDEX							
R/W							
0h							

Table 5-942. CPSW_NC_ALE_POLICECFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DST_MEN	R/W	0h	Destination Address Match Enable - Enables frame L2 destination address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	DST_INDEX	R/W	0h	Destination Address Table Entry Index - Specifies the ALE L2 destination address lookup table index to match for the selected policing/classifier entry
15	SRC_MEN	R/W	0h	Source Address Match Enable - Enables frame L2 source address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	SRC_INDEX	R/W	0h	Source Address Table Entry Index - Specifies the ALE L2 source address lookup table index to match for the selected policing/classifier entry

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5.2.2.386 CPSW_NC_ALE_POLICECFG2 Register

5.2.2.386.1 CPSW_NC_ALE_POLICECFG2 Register (Offset = 3E108h) [reset = 0h]

The Policing Config 2 holds the match enable/match index for the Outer VLAN and Inner VLAN addresses

Return to Summary Table

Table 5-943. Instance Table

Instance Name	Physical Address
CPSW0	5283 E108h + formula

Figure 5-467. CPSW_NC_ALE_POLICECFG2 Name Register

31	30	29	28	27	26	25	24
OVLAN_MEN	RESERVED						OVLAN_INDEX
R/W	NONE						R/W
0h	0h						0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OVLAN_INDEX							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IVLAN_MEN	RESERVED						IVLAN_INDEX
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IVLAN_INDEX							
R/W							
0h							

Table 5-944. CPSW_NC_ALE_POLICECFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVLAN_MEN	R/W	0h	Outer VLAN Match Enable - Enables frame Outer VLAN address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	OVLAN_INDEX	R/W	0h	Outer VLAN Table Entry Index - Specifies the ALE Outer VLAN address lookup table index to match for the selected policing/ classifier entry
15	IVLAN_MEN	R/W	0h	Inner VLAN Match Enable - Enables frame Inner VLAN address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	IVLAN_INDEX	R/W	0h	Inner VLAN Table Entry Index - Specifies the ALE Inner VLAN address lookup table index to match for the selected policing/ classifier entry

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5.2.2.387 CPSW_NC_ALE_POLICECFG3 Register

5.2.2.387.1 CPSW_NC_ALE_POLICECFG3 Register (Offset = 3E10Ch) [reset = 0h]

The Policing Config 3 holds the match enable/match index for the Ether Type and IP Source address

Return to Summary Table

Table 5-945. Instance Table

Instance Name	Physical Address
CPSW0	5283 E10Ch + formula

Figure 5-468. CPSW_NC_ALE_POLICECFG3 Name Register

31	30	29	28	27	26	25	24
ETHERTYPE_MEN	RESERVED						ETHERTYPE_INDEX
R/W	NONE						R/W
0h	0h						0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ETHERTYPE_INDEX							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IPSRC_MEN	RESERVED						IPSRC_INDEX
R/W	NONE						R/W
0h	0h						0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPSRC_INDEX							
R/W							
0h							

Table 5-946. CPSW_NC_ALE_POLICECFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ETHERTYPE_MEN	R/W	0h	EtherType Match Enable - Enables frame Ether Type match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	ETHERTYPE_INDEX	R/W	0h	EtherType Table Entry Index - Specifies the ALE Ether Type lookup table index to match for the selected policing/classifier entry
15	IPSRC_MEN	R/W	0h	IP Source Address Match Enable - Enables frame IP Source address match for the selected policing/classifier entry
14:9	RESERVED	NONE	0h	Reserved
8:0	IPSRC_INDEX	R/W	0h	IP Source Address Table Entry Index - Specifies the ALE IP Source address lookup table index to match for the selected policing/classifier entry

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5.2.2.388 CPSW_NC_ALE_POLICECFG4 Register

5.2.2.388.1 CPSW_NC_ALE_POLICECFG4 Register (Offset = 3E110h) [reset = 0h]

The Policing Config 4 holds the match enable/match index for the IP Destination address

Return to Summary Table

Table 5-947. Instance Table

Instance Name	Physical Address
CPSW0	5283 E110h + formula

Figure 5-469. CPSW_NC_ALE_POLICECFG4 Name Register

31	30	29	28	27	26	25	24
IPDST_MEN	RESERVED						IPDST_INDEX
R/W	NONE						R/W
0h	0h						0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IPDST_INDEX							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 5-948. CPSW_NC_ALE_POLICECFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPDST_MEN	R/W	0h	IP Destination Address Match Enable - Enables frame IP Destination address match for the selected policing/classifier entry
30:25	RESERVED	NONE	0h	Reserved
24:16	IPDST_INDEX	R/W	0h	IP Destination Address Table Entry Index - Specifies the ALE IP Destination address lookup table index to match for the selected policing/classifier entry
15:0	RESERVED	NONE	0h	Reserved

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5.2.2.389 CPSW_NC_ALE_POLICECFG6 Register

5.2.2.389.1 CPSW_NC_ALE_POLICECFG6 Register (Offset = 3E118h) [reset = 0h]

The PIR counter is a 37 bit internal counter where ~ipir_idle_inc_val is added every clock and the frame size << 18 is subtracted at EOF if not RED at LUT time. If the counter is negative the packet will be marked RED, else it can be YELLOW or GREEN based on the CIR counter. If only this counter is used (aka cir_idle_inc_val==0) Packet are marked RED or GREEN based on PIR counter only.

Return to Summary Table

Table 5-949. Instance Table

Instance Name	Physical Address
CPSW0	5283 E118h + formula

Figure 5-470. CPSW_NC_ALE_POLICECFG6 Name Register

31	30	29	28	27	26	25	24
PIR_IDLE_INC_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
PIR_IDLE_INC_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
PIR_IDLE_INC_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
PIR_IDLE_INC_VAL							
R/W							
0h							

Table 5-950. CPSW_NC_ALE_POLICECFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PIR_IDLE_INC_VAL	R/W	0h	Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle. If zero the PIR counter is disabled and packets will never be marked or processed as RED.

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5.2.2.390 CPSW_NC_ALE_POLICECFG7 Register

5.2.2.390.1 CPSW_NC_ALE_POLICECFG7 Register (Offset = 3E11Ch) [reset = 0h]

The CIR counter is a 37 bit internal counter where ~icir_idle_inc_val is added every clock and the frame size << 18 is subtracted at EOF if not RED or YELLOW at LUT time. If the counter is positive the packet will be marked GREEN, else it can be YELLOW or RED based on the PIR counter. If only this counter is used (aka pir_idle_inc_val==0) Packet are marked YELLOW or GREEN based on CIR counter only.

Return to Summary Table

Table 5-951. Instance Table

Instance Name	Physical Address
CPSW0	5283 E11Ch + formula

Figure 5-471. CPSW_NC_ALE_POLICECFG7 Name Register

31	30	29	28	27	26	25	24
CIR_IDLE_INC_VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
CIR_IDLE_INC_VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
CIR_IDLE_INC_VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
CIR_IDLE_INC_VAL							
R/W							
0h							

Table 5-952. CPSW_NC_ALE_POLICECFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CIR_IDLE_INC_VAL	R/W	0h	Committed Information Idle Increment Value - The number added to the CIR counter every clock cycle. If zero the CIR counter is disabled and packets will never be marked or processed as YELLOW.

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5.2.2.391 CPSW_NC_ALE_POLICETBLCTL Register

5.2.2.391.1 CPSW_NC_ALE_POLICETBLCTL Register (Offset = 3E120h) [reset = 0h]

The Policing Table Control is used to read or write the selected policing/classifier entry. The selected policing/classifier entry is only read or written after this register is written based on the value of the ~iwrite_enable bit.

Return to Summary Table

Table 5-953. Instance Table

Instance Name	Physical Address
CPSW0	5283 E120h + formula

Figure 5-472. CPSW_NC_ALE_POLICETBLCTL Name Register

31	30	29	28	27	26	25	24
WRITE_ENABLE	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			POL_TBL_IDX				
NONE			R/W				
0h			0h				

Table 5-954. CPSW_NC_ALE_POLICETBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRITE_ENABLE	R/W	0h	Write Enable - Setting this bit will write the POLICECFG0-7 to the pol_tbl_idx selected policing/classifier entry. Clearing this bit will read the pol_tbl_idx selected policing/classifier entry into the POLICECFG0-7 registers.
30:5	RESERVED	NONE	0h	Reserved
4:0	POL_TBL_IDX	R/W	0h	Policer Entry Index - This field specifies the policing/classifier entry to be read or written. When writing to this field without setting the write_enable=1 will cause the selected policing/classifier entry to be loaded into the POLICECFG0-7 registers. When writing to this field with setting the write_enable=1 will cause the selected policing/classifier entry to be updated from the POLICECFG0-7 registers.

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5.2.2.392 CPSW_NC_ALE_POLICECONTROL Register

5.2.2.392.1 CPSW_NC_ALE_POLICECONTROL Register (Offset = 3E124h) [reset = 0h]

The Control Enables color marking as well as internal ALE packet dropping rules.

Return to Summary Table

Table 5-955. Instance Table

Instance Name	Physical Address
CPSW0	5283 E124h + formula

Figure 5-473. CPSW_NC_ALE_POLICECONTROL Name Register

31	30	29	28	27	26	25	24
POLICING_EN	RESERVED	RED_DROP_EN	YELLOW_DROP_EN	RESERVED	YELLOWTHRESH		
R/W	NONE	R/W	R/W	NONE	R/W		
0h	0h	0h	0h	0h	0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
POLMCHMODE		PRIORITY_THREAD_EN	MAC_ONLY_DEF_DIS	RESERVED			
R/W		R/W	R/W	NONE			
0h		0h	0h	0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 5-956. CPSW_NC_ALE_POLICECONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLICING_EN	R/W	0h	Policing Enable - Enables the policing to color the packets, this also enables red or yellow drop capabilities.
30	RESERVED	NONE	0h	Reserved
29	RED_DROP_EN	R/W	0h	RED Drop Enable - Enables the ALE to drop the red colored packets.
28	YELLOW_DROP_EN	R/W	0h	WELLOW Drop Enable - Enables the ALE to drop yellow packets based on the yellowthresh value. This field would normally not be used as to let the switch drop packets at a buffer threshold instead. In the event that the switch does not enable buffer threshold dropping, YELLOW packets can be dropped based on this feature.
27	RESERVED	NONE	0h	Reserved
26:24	YELLOWTHRESH	R/W	0h	Yellow Threshold - When set enables a portion of the yellow packets to be dropped based on the yellow_drop_en enable. 0-100% 1=50% 2-33% 3-25% 4=20% 5-17% 6-14% 7-13%

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Table 5-956. CPSW_NC_ALE_POLICECONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	POLMCHMODE	R/W	0h	Policing Match Mode - This field determines what happens to packets that fail to hit any policing/classifier entry. 0 - No Hit packets are marked GREEN 1 - No Hit packets are marked YELLOW 2 - No Hit packets are marked RED 3 - No Hit packets are marked based on policing/classifier entry=0 state.
21	PRIORITY_THREAD_EN	R/W	0h	Priority Thread Enable - This field determines if priority is OR'd to the default thread when no classifiers hit and the default thread is enabled.
20	MAC_ONLY_DEF_DIS	R/W	0h	MAC Only Default Disable - This field when set disables the default thread on MAC Only Ports. That is the default thread will be {port,priority}. If the traffic matches a classifier with a thread mapping, the classifier thread mapping still occurs.
19:0	RESERVED	NONE	0h	Reserved

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5.2.2.393 CPSW_NC_ALE_POLICETESTCTL Register

5.2.2.393.1 CPSW_NC_ALE_POLICETESTCTL Register (Offset = 3E128h) [reset = 0h]

The Policing Test Control enables the ability to determine which policing entry has been hit and whether they reported a red or yellow rate condition.

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Table 5-957. Instance Table

Instance Name	Physical Address
CPSW0	5283 E128h + formula

Figure 5-474. CPSW_NC_ALE_POLICETESTCTL Name Register

31	30	29	28	27	26	25	24
POL_CLRALL_HIT	POL_CLRALL_REDHIT	POL_CLRALL_YELLOWHIT	POL_CLRSEL_ALL	RESERVED			
R/W	R/W	R/W	R/W	NONE			
0h	0h	0h	0h	0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			POL_TEST_IDX				
NONE			R/W				
0h			0h				

Table 5-958. CPSW_NC_ALE_POLICETESTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_CLRALL_HIT	R/W	0h	Policer Clear - This bit clears all the policing/classifier hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit.
30	POL_CLRALL_REDHIT	R/W	0h	Policer Clear RED - This bit clears all the policing/classifier RED hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a RED condition.
29	POL_CLRALL_YELLOWHIT	R/W	0h	Policer Clear YELLOW - This bit clears all the policing/classifier YELLOW hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a YELLOW condition.
28	POL_CLRSEL_ALL	R/W	0h	Police Clear Selected - This bit clears the selected policing/classifier hit, redhit and yellowhit bits. This bit is self clearing.
27:5	RESERVED	NONE	0h	Reserved
4:0	POL_TEST_IDX	R/W	0h	Policer Test Index - This field selects which policing/classifier hit bits will be read or written.

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5.2.2.394 CPSW_NC_ALE_POLICEHSTAT Register

5.2.2.394.1 CPSW_NC_ALE_POLICEHSTAT Register (Offset = 3E12Ch) [reset = 0h]

The policing hit status is a read only register that reads the hit bits of the selected policing/classifier.

Return to Summary Table

Table 5-959. Instance Table

Instance Name	Physical Address
CPSW0	5283 E12Ch + formula

Figure 5-475. CPSW_NC_ALE_POLICEHSTAT Name Register

31	30	29	28	27	26	25	24
POL_HIT	POL_REDHIT	POL_YELLOW HIT	RESERVED				
R	R	R	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-960. CPSW_NC_ALE_POLICEHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_HIT	R	0h	Policer Hit - This indicates that the selected policing/classifier via the pol_test_idx field has been hit by a packet seen on any port that matches the policing/classifier entry match.
30	POL_REDHIT	R	0h	Policer Hit RED - This indicates that the selected policing/classifier via the pol_test_idx field has been hit during a RED condition by a packet seen on any port that matches the policing/classifier entry match.
29	POL_YELLOWHIT	R	0h	Policer Hit YELLOW - This indicates that the selected policing/classifier via the pol_test_idx field has been hit during a YELLOW condition by a packet seen on any port that matches the policing/classifier entry match.
28:0	RESERVED	NONE	0h	Reserved

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5.2.2.395 CPSW_NC_ALE_THREADMAPDEF Register

5.2.2.395.1 CPSW_NC_ALE_THREADMAPDEF Register (Offset = 3E134h) [reset = 0h]

The THREAD Mapping Default Value register is used to set the default thread ID when no classifier is matched,

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Table 5-961. Instance Table

Instance Name	Physical Address
CPSW0	5283 E134h + formula

Figure 5-476. CPSW_NC_ALE_THREADMAPDEF Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DEFTHREAD_EN	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED		DEFTHREADVAL					
NONE		R/W					
0h		0h					

Table 5-962. CPSW_NC_ALE_THREADMAPDEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	DEFTHREAD_EN	R/W	0h	Default Tread Enable - When set the switch will use the defthreadval for the host interface thread ID if no classifier is matched. If clear the switch will generate its own thread ID based on port and priority if there is no classifier match.
14:6	RESERVED	NONE	0h	Reserved
5:0	DEFTHREADVAL	R/W	0h	Default Thread Value - This field specifies the default thread ID value.

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5.2.2.396 CPSW_NC_ALE_THREADMAPCTL Register

5.2.2.396.1 CPSW_NC_ALE_THREADMAPCTL Register (Offset = 3E138h) [reset = 0h]

The THREAD Mapping Control register allows the highest matched classifier to return a particular thread ID for traffic sent to the host. This allows particular classifier matched traffic to be placed an a particular hosts queue.

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Table 5-963. Instance Table

Instance Name	Physical Address
CPSW0	5283 E138h + formula

Figure 5-477. CPSW_NC_ALE_THREADMAPCTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CLASSINDEX				
NONE			R/W				
0h			0h				

Table 5-964. CPSW_NC_ALE_THREADMAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4:0	CLASSINDEX	R/W	0h	Classifier Index - This is the classifier index entry that the thread enable and thread value will be read or written by the THREADMAPVAL register.

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5.2.2.397 CPSW_NC_ALE_THREADMAPVAL Register

5.2.2.397.1 CPSW_NC_ALE_THREADMAPVAL Register (Offset = 3E13Ch) [reset = 0h]

The THREAD Mapping Value register is used to set the thread ID for a particular classifier entry.

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Table 5-965. Instance Table

Instance Name	Physical Address
CPSW0	5283 E13Ch + formula

Figure 5-478. CPSW_NC_ALE_THREADMAPVAL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
THREAD_EN	RESERVED						
R/W	NONE						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED		THREADVAL					
NONE		R/W					
0h		0h					

Table 5-966. CPSW_NC_ALE_THREADMAPVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15	THREAD_EN	R/W	0h	Thread Enable - When set the switch will use the threadval for the selected classifier match. If clear the the thread ID will be determined by the THREADMAPDEF register settings.
14:6	RESERVED	NONE	0h	Reserved
5:0	THREADVAL	R/W	0h	Thread Value - This field is the thread ID value that is used to map a classifier hit to thread ID for host traffic.

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5.2.2.398 CPSW_NC_ECC_REV Register

5.2.2.398.1 CPSW_NC_ECC_REV Register (Offset = 3F000h) [reset = 66A03201h]

Revision parameters

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Table 5-967. Instance Table

Instance Name	Physical Address
CPSW0	5283 F000h + formula

Figure 5-479. CPSW_NC_ECC_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
6h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 5-968. CPSW_NC_ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	6h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

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5.2.2.399 CPSW_NC_ECC_VECTOR Register

5.2.2.399.1 CPSW_NC_ECC_VECTOR Register (Offset = 3F008h) [reset = 0h]

ECC Vector Register

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Table 5-969. Instance Table

Instance Name	Physical Address
CPSW0	5283 F008h + formula

Figure 5-480. CPSW_NC_ECC_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h

23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W							
0h							

15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		

7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W							
0h							

Table 5-970. CPSW_NC_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

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5.2.2.400 CPSW_NC_ECC_STAT Register

5.2.2.400.1 CPSW_NC_ECC_STAT Register (Offset = 3F00Ch) [reset = 14h]

Misc Status

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Table 5-971. Instance Table

Instance Name	Physical Address
CPSW0	5283 F00Ch + formula

Figure 5-481. CPSW_NC_ECC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					14h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
14h							

Table 5-972. CPSW_NC_ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	14h	Indicates the number of RAMS serviced by the ECC aggregator

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5.2.2.401 CPSW_NC_ECC_RESERVED_SVBUS_J Register

5.2.2.401.1 CPSW_NC_ECC_RESERVED_SVBUS_J Register (Offset = 3F010h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 5-973. Instance Table

Instance Name	Physical Address
CPSW0	5283 F010h + formula

Figure 5-482. CPSW_NC_ECC_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 5-974. CPSW_NC_ECC_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

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5.2.2.402 CPSW_NC_ECC_SEC_EOI_REG Register

5.2.2.402.1 CPSW_NC_ECC_SEC_EOI_REG Register (Offset = 3F03Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 5-975. Instance Table

Instance Name	Physical Address
CPSW0	5283 F03Ch + formula

Figure 5-483. CPSW_NC_ECC_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 5-976. CPSW_NC_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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5.2.2.403 CPSW_NC_ECC_SEC_STATUS_REG0 Register

5.2.2.403.1 CPSW_NC_ECC_SEC_STATUS_REG0 Register (Offset = 3F040h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 5-977. Instance Table

Instance Name	Physical Address
CPSW0	5283 F040h + formula

Figure 5-484. CPSW_NC_ECC_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-978. CPSW_NC_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend

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Table 5-978. CPSW_NC_ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

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5.2.2.404 CPSW_NC_ECC_SEC_ENABLE_SET_REG0 Register

5.2.2.404.1 CPSW_NC_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 3F080h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 5-979. Instance Table

Instance Name	Physical Address
CPSW0	5283 F080h + formula

Figure 5-485. CPSW_NC_ECC_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-980. CPSW_NC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend

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Table 5-980. CPSW_NC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

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5.2.2.405 CPSW_NC_ECC_SEC_ENABLE_CLR_REG0 Register

5.2.2.405.1 CPSW_NC_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = 3F0C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 5-981. Instance Table

Instance Name	Physical Address
CPSW0	5283 F0C0h + formula

Figure 5-486. CPSW_NC_ECC_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-982. CPSW_NC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend

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Table 5-982. CPSW_NC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

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5.2.2.406 CPSW_NC_ECC_DED_EOI_REG Register

5.2.2.406.1 CPSW_NC_ECC_DED_EOI_REG Register (Offset = 3F13Ch) [reset = 0h]

EOI Register

Return to Summary Table

Table 5-983. Instance Table

Instance Name	Physical Address
CPSW0	5283 F13Ch + formula

Figure 5-487. CPSW_NC_ECC_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 5-984. CPSW_NC_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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5.2.2.407 CPSW_NC_ECC_DED_STATUS_REG0 Register

5.2.2.407.1 CPSW_NC_ECC_DED_STATUS_REG0 Register (Offset = 3F140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 5-985. Instance Table

Instance Name	Physical Address
CPSW0	5283 F140h + formula

Figure 5-488. CPSW_NC_ECC_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-986. CPSW_NC_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend

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Table 5-986. CPSW_NC_ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend
0	RAMECC0_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

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5.2.2.408 CPSW_NC_ECC_DED_ENABLE_SET_REG0 Register

5.2.2.408.1 CPSW_NC_ECC_DED_ENABLE_SET_REG0 Register (Offset = 3F180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 5-987. Instance Table

Instance Name	Physical Address
CPSW0	5283 F180h + formula

Figure 5-489. CPSW_NC_ECC_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE				R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-988. CPSW_NC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend

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Table 5-988. CPSW_NC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

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5.2.2.409 CPSW_NC_ECC_DED_ENABLE_CLR_REG0 Register

5.2.2.409.1 CPSW_NC_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 3F1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 5-989. Instance Table

Instance Name	Physical Address
CPSW0	5283 F1C0h + formula

Figure 5-490. CPSW_NC_ECC_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-990. CPSW_NC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend

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Table 5-990. CPSW_NC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

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5.2.2.410 CPSW_NC_ECC_AGGR_ENABLE_SET Register

5.2.2.410.1 CPSW_NC_ECC_AGGR_ENABLE_SET Register (Offset = 3F200h) [reset = 0h]

AGGR interrupt enable set Register

Return to Summary Table

Table 5-991. Instance Table

Instance Name	Physical Address
CPSW0	5283 F200h + formula

Figure 5-491. CPSW_NC_ECC_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 5-992. CPSW_NC_ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

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5.2.2.411 CPSW_NC_ECC_AGGR_ENABLE_CLR Register

5.2.2.411.1 CPSW_NC_ECC_AGGR_ENABLE_CLR Register (Offset = 3F204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to Summary Table

Table 5-993. Instance Table

Instance Name	Physical Address
CPSW0	5283 F204h + formula

Figure 5-492. CPSW_NC_ECC_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 5-994. CPSW_NC_ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

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5.2.2.412 CPSW_NC_ECC_AGGR_STATUS_SET Register

5.2.2.412.1 CPSW_NC_ECC_AGGR_STATUS_SET Register (Offset = 3F208h) [reset = 0h]

AGGR interrupt status set Register

Return to Summary Table

Table 5-995. Instance Table

Instance Name	Physical Address
CPSW0	5283 F208h + formula

Figure 5-493. CPSW_NC_ECC_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 5-996. CPSW_NC_ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	interrupt status set for parity errors

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5.2.2.413 CPSW_NC_ECC_AGGR_STATUS_CLR Register

5.2.2.413.1 CPSW_NC_ECC_AGGR_STATUS_CLR Register (Offset = 3F20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to Summary Table

Table 5-997. Instance Table

Instance Name	Physical Address
CPSW0	5283 F20Ch + formula

Figure 5-494. CPSW_NC_ECC_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 5-998. CPSW_NC_ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	interrupt status clear for parity errors

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5.2.2.414 CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_J Register

5.2.2.414.1 CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_J Register (Offset = 3D0E0h) [reset = 0h]

Time Stamp Generate Function Comparison Low Value

Return to Summary Table

Table 5-999. Instance Table

Instance Name	Physical Address
CPSW0	5283 D0E0h + formula

Figure 5-495. CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_LOW							
R/W							
0h							

Table 5-1000. CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	GENFn comparison value lower 32-bits. This value should be written after the upper 32-bits. The ts_GENFn_comp high and low should only be written when the ts_GENFn_length value is zero.

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5.2.2.415 CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_J Register

5.2.2.415.1 CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_J Register (Offset = 3D0E4h) [reset = 0h]

Time Stamp Generate Function Comparison high Value

Return to Summary Table

Table 5-1001. Instance Table

Instance Name	Physical Address
CPSW0	5283 D0E4h + formula

Figure 5-496. CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_HIGH							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_HIGH							
R/W							
0h							

Table 5-1002. CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	GENFn comparison value upper 32-bits. This value should be written before the lower 32-bits are written. The ts_GENFn_comp high and low should only be written when the ts_GENFn_length value is zero.

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5.2.2.416 CPSW_NC_CPTS_TS_GENF_CONTROL_REG_J Register

5.2.2.416.1 CPSW_NC_CPTS_TS_GENF_CONTROL_REG_J Register (Offset = 3D0E8h) [reset = 0h]

Time Stamp Generate Function Control

Return to Summary Table

Table 5-1003. Instance Table

Instance Name	Physical Address
CPSW0	5283 D0E8h + formula

Figure 5-497. CPSW_NC_CPTS_TS_GENF_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PPM_DIR	POLARITY_INV
NONE						R/W	R/W
0h						0h	0h

Table 5-1004. CPSW_NC_CPTS_TS_GENF_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	PPM_DIR	R/W	0h	Generate function N PPM direction - 0 - A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1 - A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.
0	POLARITY_INV	R/W	0h	Generate function N Polarity - 0 - The output TS_GENFn signal asserts high. 1 - The output TS_GENFn signal asserts low

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5.2.2.417 CPSW_NC_CPTS_TS_GENF_LENGTH_REG_J Register

5.2.2.417.1 CPSW_NC_CPTS_TS_GENF_LENGTH_REG_J Register (Offset = 3D0ECh) [reset = 0h]

Time Stamp Generate Function Length Value

Return to Summary Table

Table 5-1005. Instance Table

Instance Name	Physical Address
CPSW0	5283 D0ECh + formula

Figure 5-498. CPSW_NC_CPTS_TS_GENF_LENGTH_REG_j Name Register

31	30	29	28	27	26	25	24
LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
LENGTH							
R/W							
0h							

Table 5-1006. CPSW_NC_CPTS_TS_GENF_LENGTH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	GENFn length - The minimum operational value is decimal 5. Note: Software is advised to write and then read the comparison value before writing a non-zero value to the genf length to ensure that the comparison value is synchronized across the boundary before the length.

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5.2.2.418 CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_J Register

5.2.2.418.1 CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_J Register (Offset = 3D0F0h) [reset = 0h]

Time Stamp Generate Function PPM Low Value

Return to Summary Table

Table 5-1007. Instance Table

Instance Name	Physical Address
CPSW0	5283 D0F0h + formula

Figure 5-499. CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
PPM_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
PPM_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
PPM_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
PPM_LOW							
R/W							
0h							

Table 5-1008. CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	GENFn PPM Low Value - The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

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5.2.2.419 CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_J Register

5.2.2.419.1 CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_J Register (Offset = 3D0F4h) [reset = 0h]

Time Stamp Generate Function PPM High Value

Return to Summary Table

Table 5-1009. Instance Table

Instance Name	Physical Address
CPSW0	5283 D0F4h + formula

Figure 5-500. CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						PPM_HIGH	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PPM_HIGH							
R/W							
0h							

Table 5-1010. CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PPM_HIGH	R/W	0h	GENFn PPM High Value - This value should be written first (before the low value is written).

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5.2.2.420 CPSW_NC_CPTS_TS_GENF_NUDGE_REG_J Register

5.2.2.420.1 CPSW_NC_CPTS_TS_GENF_NUDGE_REG_J Register (Offset = 3D0F8h) [reset = 0h]

Time Stamp Generate Function Nudge Value

Return to Summary Table

Table 5-1011. Instance Table

Instance Name	Physical Address
CPSW0	5283 D0F8h + formula

Figure 5-501. CPSW_NC_CPTS_TS_GENF_NUDGE_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 5-1012. CPSW_NC_CPTS_TS_GENF_NUDGE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	GENFn Nudge Value - This two's complement number is added to the generate counter value to increase or decrease the length by the ts_genfN_nudge amount. Only a single high or low time is adjusted and the ts_genfN_nudge value is cleared to zero when the nudge has occurred.

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5.2.2.421 CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_J Register

5.2.2.421.1 CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_J Register (Offset = 3D200h) [reset = 0h]

Time Stamp ESTF Generate Function Comparison Low Value

Return to Summary Table

Table 5-1013. Instance Table

Instance Name	Physical Address
CPSW0	5283 D200h + formula

Figure 5-502. CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_LOW							
R/W							
0h							

Table 5-1014. CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_LOW	R/W	0h	ESTFn comparison value lower 32-bits. This value should be written after the upper 32-bits. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero.

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5.2.2.422 CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_J Register

5.2.2.422.1 CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_J Register (Offset = 3D204h) [reset = 0h]

Time Stamp ESTF Generate Function Comparison high Value

Return to Summary Table

Table 5-1015. Instance Table

Instance Name	Physical Address
CPSW0	5283 D204h + formula

Figure 5-503. CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
COMP_HIGH							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP_HIGH							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP_HIGH							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP_HIGH							
R/W							
0h							

Table 5-1016. CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP_HIGH	R/W	0h	ESTFn comparison value upper 32-bits. This value should be written before the lower 32-bits are written. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero.

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5.2.2.423 CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_J Register

5.2.2.423.1 CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_J Register (Offset = 3D208h) [reset = 0h]

Time Stamp ESTF Generate Function Control

Return to Summary Table

Table 5-1017. Instance Table

Instance Name	Physical Address
CPSW0	5283 D208h + formula

Figure 5-504. CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						PPM_DIR	POLARITY_INV
NONE						R/W	R/W
0h						0h	0h

Table 5-1018. CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	PPM_DIR	R/W	0h	Generate function N PPM direction - 0 - A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1 - A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.
0	POLARITY_INV	R/W	0h	Generate function N Polarity - 0 - The output TS_ESTFn signal asserts low. 1 - The output TS_ESTFn signal asserts high.

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5.2.2.424 CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_J Register

5.2.2.424.1 CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_J Register (Offset = 3D20Ch) [reset = 0h]

Time Stamp ESTF Generate Function Length Value

Return to Summary Table

Table 5-1019. Instance Table

Instance Name	Physical Address
CPSW0	5283 D20Ch + formula

Figure 5-505. CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_j Name Register

31	30	29	28	27	26	25	24
LENGTH							
R/W							
0h							
23	22	21	20	19	18	17	16
LENGTH							
R/W							
0h							
15	14	13	12	11	10	9	8
LENGTH							
R/W							
0h							
7	6	5	4	3	2	1	0
LENGTH							
R/W							
0h							

Table 5-1020. CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LENGTH	R/W	0h	ESTFn length - The minimum operational value is decimal 5. Note: Software is advised to write and then read the comparison value before writing a non-zero value to the genf length to ensure that the comparison value is synchronized across the boundary before the length.

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5.2.2.425 CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_J Register

5.2.2.425.1 CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_J Register (Offset = 3D210h) [reset = 0h]

Time Stamp ESTF Generate Function PPM Low Value

Return to Summary Table

Table 5-1021. Instance Table

Instance Name	Physical Address
CPSW0	5283 D210h + formula

Figure 5-506. CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_j Name Register

31	30	29	28	27	26	25	24
PPM_LOW							
R/W							
0h							
23	22	21	20	19	18	17	16
PPM_LOW							
R/W							
0h							
15	14	13	12	11	10	9	8
PPM_LOW							
R/W							
0h							
7	6	5	4	3	2	1	0
PPM_LOW							
R/W							
0h							

Table 5-1022. CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PPM_LOW	R/W	0h	ESTFn PPM Low Value - The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

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5.2.2.426 CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_J Register

5.2.2.426.1 CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_J Register (Offset = 3D214h) [reset = 0h]

Time Stamp ESTF Generate Function PPM High Value

Return to Summary Table

Table 5-1023. Instance Table

Instance Name	Physical Address
CPSW0	5283 D214h + formula

Figure 5-507. CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						PPM_HIGH	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
PPM_HIGH							
R/W							
0h							

Table 5-1024. CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	PPM_HIGH	R/W	0h	ESTFn PPM High Value - This value should be written first (before the low value is written).

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5.2.2.427 CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_J Register

5.2.2.427.1 CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_J Register (Offset = 3D218h) [reset = 0h]

Time Stamp ESTF Generate Function Nudge Value

Return to Summary Table

Table 5-1025. Instance Table

Instance Name	Physical Address
CPSW0	5283 D218h + formula

Figure 5-508. CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUDGE							
R/W							
0h							

Table 5-1026. CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	NUDGE	R/W	0h	ESTFn Nudge Value - This two's complement number is added to the generate counter value to increase or decrease the length by the ts_estfN_nudge amount. Only a single high or low time is adjusted and the ts_estfN_nudge value is cleared to zero when the nudge has occurred.

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5.3 DCC

DCC

5.3.1 DCC Summaries

DCC Summaries

Table 5-1027. MSS_DCC Registers, Base Address=52B0 0000h, Length=64

Offset	Length	Register Name	DCC0 Physical Address	DCC1 Physical Address	DCC2 Physical Address
0h	32	MSS_DCC_DCCGCTRL	52B0 0000h	52B0 1000h	52B0 2000h
4h	32	MSS_DCC_DCCREV	52B0 0004h	52B0 1004h	52B0 2004h
8h	32	MSS_DCC_DCCCNTSEED0	52B0 0008h	52B0 1008h	52B0 2008h
Ch	32	MSS_DCC_DCCVALIDSEED0	52B0 000Ch	52B0 100Ch	52B0 200Ch
10h	32	MSS_DCC_DCCCNTSEED1	52B0 0010h	52B0 1010h	52B0 2010h
14h	32	MSS_DCC_DCCSTATUS	52B0 0014h	52B0 1014h	52B0 2014h
18h	32	MSS_DCC_DCCCNT0	52B0 0018h	52B0 1018h	52B0 2018h
1Ch	32	MSS_DCC_DCCVALID0	52B0 001Ch	52B0 101Ch	52B0 201Ch
20h	32	MSS_DCC_DCCCNT1	52B0 0020h	52B0 1020h	52B0 2020h
24h	32	MSS_DCC_DCCCLKSRC1	52B0 0024h	52B0 1024h	52B0 2024h
28h	32	MSS_DCC_DCCCLKSRC0	52B0 0028h	52B0 1028h	52B0 2028h
2Ch	32	MSS_DCC_DCCGCTRL2	52B0 002Ch	52B0 102Ch	52B0 202Ch
30h	32	MSS_DCC_DCCSTATUS2	52B0 0030h	52B0 1030h	52B0 2030h
34h	32	MSS_DCC_DCCERRCNT	52B0 0034h	52B0 1034h	52B0 2034h

Table 5-1028. MSS_DCC Registers, Base Address=52B0 0000h, Length=64

Offset	Length	Register Name	DCC3 Physical Address
0h	32	MSS_DCC_DCCGCTRL	52B0 3000h
4h	32	MSS_DCC_DCCREV	52B0 3004h
8h	32	MSS_DCC_DCCCNTSEED0	52B0 3008h
Ch	32	MSS_DCC_DCCVALIDSEED0	52B0 300Ch
10h	32	MSS_DCC_DCCCNTSEED1	52B0 3010h
14h	32	MSS_DCC_DCCSTATUS	52B0 3014h
18h	32	MSS_DCC_DCCCNT0	52B0 3018h
1Ch	32	MSS_DCC_DCCVALID0	52B0 301Ch
20h	32	MSS_DCC_DCCCNT1	52B0 3020h
24h	32	MSS_DCC_DCCCLKSRC1	52B0 3024h
28h	32	MSS_DCC_DCCCLKSRC0	52B0 3028h
2Ch	32	MSS_DCC_DCCGCTRL2	52B0 302Ch
30h	32	MSS_DCC_DCCSTATUS2	52B0 3030h
34h	32	MSS_DCC_DCCERRCNT	52B0 3034h

5.3.2 DCC Registers

DCC Registers

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5.3.2.1 MSS_DCC_DCCGCTRL Register

5.3.2.1.1 MSS_DCC_DCCGCTRL Register (Offset = 0h) [reset = 5555h]

Starts / stops the counters. Clears the error signal.

Return to Summary Table

Table 5-1029. Instance Table

Instance Name	Physical Address
DCC0	52B0 0000h
DCC1	52B0 1000h
DCC2	52B0 2000h
DCC3	52B0 3000h

Figure 5-509. MSS_DCC_DCCGCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
DONEENA				SINGLESHOT			
R/W				R/W			
5h				5h			
7	6	5	4	3	2	1	0
ERRENA				DCCENA			
R/W				R/W			
5h				5h			

Table 5-1030. MSS_DCC_DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	DONEENA	R/W	5h	The DONEENA bit enables/disables the done interrupt signal, but has no effect on the done status flag in DCCSTAT register. User, privilege, and debug mode (read): 0101= the done signal is disabled others = the done signal is enabled Privilege and debug mode (write): 0101= Disable done signal generation others 1010 = Enable done signal generation. It is recommended to write 1010 to enable each feature to avoid single soft errors.
11:8	SINGLESHOT	R/W	5h	The SINGLESHOT bit enables/disables repetitive operation of the DCC. User, privilege, and debug mode (read): 1010= stop counting when counter0 and valid0 both reach zero 1011= stop counting when counter1 reaches zero others = continuously repeat (until error) Privilege and debug mode (write): 1010= stop counting when counter0 and valid0 both reach zero 1011= stop counting when counter1 reaches zero others = continuously repeat (until error)

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Table 5-1030. MSS_DCC_DCCGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	ERRENA	R/W	5h	The ERRENA bit enables/disables the error signal. User, privilege, and debug mode (read): 0101= the error signal is disabled others = the error signal is enabled Privilege and debug mode (write): 0101= disable error signal generation others 1010 = enable error signal generation. It is recommended to write 1010 to enable each feature to avoid single soft errors.
3:0	DCCENA	R/W	5h	The DCCENA bit starts and stops the operation of the dcc. User, privilege, and debug mode (read): 0101= counters are stopped others = counters are running Privilege and debug mode (write): 0101= stop counters and error-checking others 1010 = load the counters with their seed values and begin counting. It is recommended to write 1010 to enable each feature to avoid single soft errors.

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5.3.2.2 MSS_DCC_DCCREV Register

5.3.2.2.1 MSS_DCC_DCCREV Register (Offset = 4h) [reset = 40010B00h]

Specifies the module version.

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Table 5-1031. Instance Table

Instance Name	Physical Address
DCC0	52B0 0004h
DCC1	52B0 1004h
DCC2	52B0 2004h
DCC3	52B0 3004h

Figure 5-510. MSS_DCC_DCCREV Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		NONE		R			
1h		0h		1h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
1h					3h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 5-1032. MSS_DCC_DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	User, privilege, and debug mode (read): Returns 01. Privilege and debug mode (write): Writes have no effect.
29:28	RESERVED	NONE	0h	Reserved
27:16	FUNC	R	1h	Reflects software-compatability. If there is no level of software compatability, a unique func number is assigned; for compatible modules, the same number is maintained. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
15:11	RTL	R	1h	Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented. User, privilege, and debug mode (read): 0x1 Privilege and debug mode (write): Writes have no effect.
10:8	MAJOR	R	3h	Represents major changes to the module (e.g. entirely new features are added/changed). The major revision number for this module. User, privilege, and debug mode (read): 0x2 Privilege and debug mode (write): Writes have no effect.
7:6	CUSTOM	R	0h	Indicates a special version of the module. May not be supported by standard software. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.

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Table 5-1032. MSS_DCC_DCCREV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	MINOR	R	0h	Represents minor changes to the module (e.g. enhancements to existing features). The minor revision number for this module. User, privilege, and debug mode (read): 0x4 Privilege and debug mode (write): Writes have no effect.

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5.3.2.3 MSS_DCC_DCCCNTSEED0 Register

5.3.2.3.1 MSS_DCC_DCCCNTSEED0 Register (Offset = 8h) [reset = 0h]

Seed value for the counter attached to clock source 0

Return to Summary Table

Table 5-1033. Instance Table

Instance Name	Physical Address
DCC0	52B0 0008h
DCC1	52B0 1008h
DCC2	52B0 2008h
DCC3	52B0 3008h

Figure 5-511. MSS_DCC_DCCCNTSEED0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				COUNTSEED0			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNTSEED0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNTSEED0							
R/W							
0h							

Table 5-1034. MSS_DCC_DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNTSEED0	R/W	0h	This field contains the seed value that gets loaded into counter 0 (clock source 0). User, privilege, and debug mode (read): Returns the current seed value for counter 0. Privilege and debug mode (write): Sets the current seed value for counter 0. NOTE - Operating the DCC with 0 in the COUNTSEED0 register will result in undefined operation.

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5.3.2.4 MSS_DCC_DCCVALIDSEED0 Register

5.3.2.4.1 MSS_DCC_DCCVALIDSEED0 Register (Offset = Ch) [reset = 0h]

Seed value for the timeout counter attached to clock source 0.

Return to Summary Table

Table 5-1035. Instance Table

Instance Name	Physical Address
DCC0	52B0 000Ch
DCC1	52B0 100Ch
DCC2	52B0 200Ch
DCC3	52B0 300Ch

Figure 5-512. MSS_DCC_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
VALIDSEED0							
R/W							
0h							
7	6	5	4	3	2	1	0
VALIDSEED0							
R/W							
0h							

Table 5-1036. MSS_DCC_DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VALIDSEED0	R/W	0h	This field contains the seed value that gets loaded into the valid duration counter for clock source 0. User, privilege, and debug mode (read): Returns the current seed value for VALID0. Privilege and debug mode (write): Sets the current seed value for VALID0. NOTE - Operating the DCC with 0 in the VALIDSEED0 register will result in undefined operation. VALID0 defines a window in which COUNT1 expires. This window is meant to be at least four cycles wide. Do not program a value less than 4 into the VALID0 register.

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5.3.2.5 MSS_DCC_DCCCNTSEED1 Register

5.3.2.5.1 MSS_DCC_DCCCNTSEED1 Register (Offset = 10h) [reset = 0h]

Seed value for the counter attached to clock source 1.

Return to Summary Table

Table 5-1037. Instance Table

Instance Name	Physical Address
DCC0	52B0 0010h
DCC1	52B0 1010h
DCC2	52B0 2010h
DCC3	52B0 3010h

Figure 5-513. MSS_DCC_DCCCNTSEED1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				COUNTSEED1			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
COUNTSEED1							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNTSEED1							
R/W							
0h							

Table 5-1038. MSS_DCC_DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNTSEED1	R/W	0h	This field contains the seed value that gets loaded into counter 1 (clock source 1). User, privilege, and debug mode (read): Returns the current seed value for counter 1. Privilege and debug mode (write): Sets the current seed value for counter 1. NOTE - Operating the DCC with 0 in the COUNTSEED1 register will result in undefined operation.

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5.3.2.6 MSS_DCC_DCCSTATUS Register

5.3.2.6.1 MSS_DCC_DCCSTATUS Register (Offset = 14h) [reset = 0h]

Specifies the status of the DCC Module.

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Table 5-1039. Instance Table

Instance Name	Physical Address
DCC0	52B0 0014h
DCC1	52B0 1014h
DCC2	52B0 2014h
DCC3	52B0 3014h

Figure 5-514. MSS_DCC_DCCSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						DONEFLG	ERRFLG
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 5-1040. MSS_DCC_DCCSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	DONEFLG	R/W1TC	0h	Indicates when single-shot mode is complete without error. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = single-shot mode is not done 1 = single-shot mode is done Privilege and debug mode (write): 0 = no effect 1 = clear the done flag
0	ERRFLG	R/W1TC	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = an error has not occurred 1 = an error has occurred Privilege and debug mode (write): 0 = no effect 1 = clear the error flag

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5.3.2.7 MSS_DCC_DCCCNT0 Register

5.3.2.7.1 MSS_DCC_DCCCNT0 Register (Offset = 18h) [reset = 0h]

Value of the counter attached to clock source 0.

Return to Summary Table

Table 5-1041. Instance Table

Instance Name	Physical Address
DCC0	52B0 0018h
DCC1	52B0 1018h
DCC2	52B0 2018h
DCC3	52B0 3018h

Figure 5-515. MSS_DCC_DCCCNT0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				COUNT0			
NONE				R			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COUNT0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COUNT0							
R							
0h							

Table 5-1042. MSS_DCC_DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNT0	R	0h	This field contains the current value of counter 0. User, privilege, and debug mode (read): Returns either the current value of Count 0 or the Count 0 FIFO location, depending upon DCCGCTRL2.FIFO_READ. Privilege and debug mode (write): Writes have no effect. NOTE - Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

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5.3.2.8 MSS_DCC_DCCVALID0 Register

5.3.2.8.1 MSS_DCC_DCCVALID0 Register (Offset = 1Ch) [reset = 0h]

Value of the valid counter attached to clock source 0.

Return to Summary Table

Table 5-1043. Instance Table

Instance Name	Physical Address
DCC0	52B0 001Ch
DCC1	52B0 101Ch
DCC2	52B0 201Ch
DCC3	52B0 301Ch

Figure 5-516. MSS_DCC_DCCVALID0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
VALID0							
R							
0h							
7	6	5	4	3	2	1	0
VALID0							
R							
0h							

Table 5-1044. MSS_DCC_DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	VALID0	R	0h	This field contains the current value of valid counter 0. User, privilege, and debug mode (read): Returns either the current value of Valid 0 or the Valid 0 FIFO location depending upon DCCGCTRL2.FIFO_READ. Privilege and debug mode (write): writes have no effect. NOTE - Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

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5.3.2.9 MSS_DCC_DCCCNT1 Register

5.3.2.9.1 MSS_DCC_DCCCNT1 Register (Offset = 20h) [reset = 0h]

Value of the counter attached to clock source 1.

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Table 5-1045. Instance Table

Instance Name	Physical Address
DCC0	52B0 0020h
DCC1	52B0 1020h
DCC2	52B0 2020h
DCC3	52B0 3020h

Figure 5-517. MSS_DCC_DCCCNT1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				COUNT1			
NONE				R			
0h				0h			
15	14	13	12	11	10	9	8
COUNT1							
R							
0h							
7	6	5	4	3	2	1	0
COUNT1							
R							
0h							

Table 5-1046. MSS_DCC_DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	COUNT1	R	0h	This field contains the current value of counter 1. User, privilege, and debug mode (read): Returns either the current value of Count 1 or the Count 1 FIFO location depending upon DCCGCTRL2.FIFO_READ 1. Privilege and debug mode (write): writes have no effect. NOTE - Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock.

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5.3.2.10 MSS_DCC_DCCCLKSRC1 Register

5.3.2.10.1 MSS_DCC_DCCCLKSRC1 Register (Offset = 24h) [reset = 0h]

Selects the clock source for counter 1.

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Table 5-1047. Instance Table

Instance Name	Physical Address
DCC0	52B0 0024h
DCC1	52B0 1024h
DCC2	52B0 2024h
DCC3	52B0 3024h

Figure 5-518. MSS_DCC_DCCCLKSRC1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
KEY				RESERVED			
R/W				NONE			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED			CLKSRC1				
NONE			R/W				
0h			0h				

Table 5-1048. MSS_DCC_DCCCLKSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	KEY	R/W	0h	This field enables or disables clock source selection for counter 1. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010 The CLKSRC field selects the clock source for counter 1. others: Clock source selection is disabled.
11:5	RESERVED	NONE	0h	Reserved
4:0	CLKSRC1	R/W	0h	This field specifies the clock source for counter 1, when the KEY field enables this feature. User, privilege, and debug mode (read): Returns the current value of CLKSRC1. Privilege and debug mode (write): Sets the value of CLKSRC1.

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5.3.2.11 MSS_DCC_DCCCLKSRC0 Register

5.3.2.11.1 MSS_DCC_DCCCLKSRC0 Register (Offset = 28h) [reset = 0h]

Selects the clock source for counter 0.

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Table 5-1049. Instance Table

Instance Name	Physical Address
DCC0	52B0 0028h
DCC1	52B0 1028h
DCC2	52B0 2028h
DCC3	52B0 3028h

Figure 5-519. MSS_DCC_DCCCLKSRC0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
KEY				RESERVED			
R/W				NONE			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED				CLKSRC0			
NONE				R/W			
0h				0h			

Table 5-1050. MSS_DCC_DCCCLKSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	KEY	R/W	0h	This field enables or disables clock source selection for counter 0. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010 The CLKSRC field selects the clock source for counter 0. others: Clock source selection is disabled.
11:4	RESERVED	NONE	0h	Reserved
3:0	CLKSRC0	R/W	0h	This field specifies the clock source for counter 0, when the KEY field enables this feature. User, privilege, and debug mode (read): Returns the current value of CLKSRC0. Privilege and debug mode (write): Sets the value of CLKSRC0.

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5.3.2.12 MSS_DCC_DCCGCTRL2 Register

5.3.2.12.1 MSS_DCC_DCCGCTRL2 Register (Offset = 2Ch) [reset = 555h]

Allows configuring different modes of operation for DCC.

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Table 5-1051. Instance Table

Instance Name	Physical Address
DCC0	52B0 002Ch
DCC1	52B0 102Ch
DCC2	52B0 202Ch
DCC3	52B0 302Ch

Figure 5-520. MSS_DCC_DCCGCTRL2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED				FIFO_NONERR			
NONE				R/W			
0h				5h			
7	6	5	4	3	2	1	0
FIFO_READ				CONT_ON_ERR			
R/W				R/W			
5h				5h			

Table 5-1052. MSS_DCC_DCCGCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED	NONE	0h	Reserved
11:8	FIFO_NONERR	R/W	5h	Enables/disables FIFO writes without the error event on completion of comparison window. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101 Counter values are captured to non-full FIFO only upon Error event. Others 1010 : Write counter values to non-full FIFO upon completion of comparison window regardless of error or not. It is recommended to write 1010 to avoid single soft errors.

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Table 5-1052. MSS_DCC_DCCGCTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	FIFO_READ	R/W	5h	Enables the counter read registers reflect FIFO output instead of the live counter value. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101 Counter value is read directly. Others 1010 : Counters FIFO output is read. It is recommended to write 1010 to avoid single soft errors.
3:0	CONT_ON_ERR	R/W	5h	Continues to next window of comparison despite the error condition. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Enable values: 0101 Comparison and counter reload is stopped from advancing if error is detected. Others 1010:Counters get reloaded with seed and continue counting despite the error condition. It is recommended to write 1010 to avoid single soft errors.

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5.3.2.13 MSS_DCC_DCCSTATUS2 Register

5.3.2.13.1 MSS_DCC_DCCSTATUS2 Register (Offset = 30h) [reset = 7h]

Specifies the status of the DCC FIFOs.

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Table 5-1053. Instance Table

Instance Name	Physical Address
DCC0	52B0 0030h
DCC1	52B0 1030h
DCC2	52B0 2030h
DCC3	52B0 3030h

Figure 5-521. MSS_DCC_DCCSTATUS2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		COUNT1_FIFO_FULL	VALID0_FIFO_FULL	COUNT0_FIFO_FULL	COUNT1_FIFO_EMPTY	VALID0_FIFO_EMPTY	COUNT0_FIFO_EMPTY
NONE		R	R	R	R	R	R
0h		0h	0h	0h	1h	1h	1h

Table 5-1054. MSS_DCC_DCCSTATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	COUNT1_FIFO_FULL	R	0h	Count1 FIFO Full. Indicates whether Count1 FIFO is full. User, privilege, and debug mode (read): 0:Count1 FIFO is not full 1:Count1 FIFO is full. Privilege and debug mode (write): Writes have no effect.
4	VALID0_FIFO_FULL	R	0h	Valid0 FIFO Full. Indicates whether Valid0 FIFO is full. User, privilege, and debug mode (read): 0:Valid0 FIFO is not full 1:Valid0 FIFO is full. Privilege and debug mode (write): Writes have no effect.
3	COUNT0_FIFO_FULL	R	0h	Count0 FIFO Full. Indicates whether Count0 FIFO is full. User, privilege, and debug mode (read): 0:Count0 FIFO is not full 1:Count0 FIFO is full. Privilege and debug mode (write): Writes have no effect.
2	COUNT1_FIFO_EMPTY	R	1h	Count1 FIFO Empty. Indicates whether Count1 FIFO is empty. User, privilege, and debug mode (read): 0:Count1 FIFO is not empty 1:Count1 FIFO is empty. Privilege and debug mode (write): Writes have no effect.

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Table 5-1054. MSS_DCC_DCCSTATUS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VALID0_FIFO_EMPTY	R	1h	Valid0 FIFO Empty. Indicates whether Valid0 FIFO is empty. User, privilege, and debug mode (read): 0:Valid0 FIFO is not empty 1:Valid0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.
0	COUNT0_FIFO_EMPTY	R	1h	Count0 FIFO Empty. Indicates whether Count0 FIFO is empty. User, privilege, and debug mode (read): 0:Count0 FIFO is not empty 1:Count0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.

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5.3.2.14 MSS_DCC_DCCERRCNT Register

5.3.2.14.1 MSS_DCC_DCCERRCNT Register (Offset = 34h) [reset = 0h]

Counts number of errors since last clear.

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Table 5-1055. Instance Table

Instance Name	Physical Address
DCC0	52B0 0034h
DCC1	52B0 1034h
DCC2	52B0 2034h
DCC3	52B0 3034h

Figure 5-522. MSS_DCC_DCCERRCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						ERRCNT	
NONE						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERRCNT							
R/W							
0h							

Table 5-1056. MSS_DCC_DCCERRCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:0	ERRCNT	R/W	0h	Counts the number of errors after the last write to this register or reset. If reached terminal count the count freezes. User needs to clear it.

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5.4 ESM

ESM

5.4.1 ESM Summaries

ESM Summaries

Table 5-1057. ESM Registers, Base Address=52D0 0000h, Length=2048

Offset	Length	Register Name	ESM0 Physical Address
0h	32	ESM_PID	52D0 0000h
4h	32	ESM_INFO	52D0 0004h
8h	32	ESM_EN	52D0 0008h
Ch	32	ESM_SFT_RST	52D0 000Ch
10h	32	ESM_ERR_RAW	52D0 0010h
14h	32	ESM_ERR_STS	52D0 0014h
18h	32	ESM_ERR_EN_SET	52D0 0018h
1Ch	32	ESM_ERR_EN_CLR	52D0 001Ch
20h	32	ESM_LOW_PRI	52D0 0020h
24h	32	ESM_HI_PRI	52D0 0024h
28h	32	ESM_LOW	52D0 0028h
2Ch	32	ESM_HI	52D0 002Ch
30h	32	ESM_EOI	52D0 0030h
40h	32	ESM_PIN_CTRL	52D0 0040h
44h	32	ESM_PIN_STS	52D0 0044h
48h	32	ESM_PIN_CNTR	52D0 0048h
4Ch	32	ESM_PIN_CNTR_PRE	52D0 004Ch
50h	32	ESM_PWMH_PIN_CNTR	52D0 0050h
54h	32	ESM_PWMH_PIN_CNTR_PRE	52D0 0054h
58h	32	ESM_PWML_PIN_CNTR	52D0 0058h
5Ch	32	ESM_PWML_PIN_CNTR_PRE	52D0 005Ch
60h	32	ESM_CRIT_DELAY_CNTR	52D0 0060h
64h	32	ESM_CRIT_DELAY_CNTR_PRE	52D0 0064h
400h	32	ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_RAW_J	52D0 0400h + formula
404h	32	ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_STS_J	52D0 0404h + formula
408h	32	ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_SET_J	52D0 0408h + formula
40Ch	32	ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_CLR_J	52D0 040Ch + formula
410h	32	ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INT_PRIO_J	52D0 0410h + formula
414h	32	ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_SET_J	52D0 0414h + formula
418h	32	ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_CLR_J	52D0 0418h + formula
800h	32	ESM_PCR_GENERATED_MEMORY_MAP_ERR_EXT_GRP_CRIT_EN_SET_J	52D0 0800h + formula
804h	32	ESM_PCR_GENERATED_MEMORY_MAP_ERR_EXT_GRP_CRIT_EN_CLR_J	52D0 0804h + formula

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5.4.2 ESM Registers

ESM Registers

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5.4.2.1 ESM_PID Register

5.4.2.1.1 ESM_PID Register (Offset = 0h) [reset = 6FE05100h]

The Revision Register contains the major and minor revisions for the module.

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Table 5-1058. Instance Table

Instance Name	Physical Address
ESM0	52D0 0000h

Figure 5-523. ESM_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		FE0h			
23	22	21	20	19	18	17	16
FUNC							
R							
FE0h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
Ah					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 5-1059. ESM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme
29:28	BU	R	2h	Business Unit: 10 = Processors
27:16	FUNC	R	FE0h	Module ID
15:11	RTL	R	Ah	RTL revision. Will vary depending on release.
10:8	MAJOR	R	1h	Major revision
7:6	CUSTOM	R	0h	Custom
5:0	MINOR	R	0h	Minor revision

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5.4.2.2 ESM_INFO Register

5.4.2.2.1 ESM_INFO Register (Offset = 4h) [reset = 204h]

The Info Register gives the configuration Inforrmation of this ESM.

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Table 5-1060. Instance Table

Instance Name	Physical Address
ESM0	52D0 0004h

Figure 5-524. ESM_INFO Name Register

31	30	29	28	27	26	25	24
LAST_RESET	CRIT_INTR	CRIT_DELAY_CNTR_ERROR	RESERVED				
R	R	R	NONE				
0h	0h	0h	0h				
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
PULSE_GROUPS							
R							
2h							
7	6	5	4	3	2	1	0
GROUPS							
R							
4h							

Table 5-1061. ESM_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LAST_RESET	R	0h	Indicates the Source of the last Reset
30	CRIT_INTR	R	0h	Indicates if the critical priority interrupt output has asserted
29	CRIT_DELAY_CNTR_ERROR	R	0h	Indicates if a bit error has occurred in the critical priority interrupt delay counter
28:16	RESERVED	NONE	0h	Reserved
15:8	PULSE_GROUPS	R	2h	Number of Pulse Error Groups
7:0	GROUPS	R	4h	Total number of Error Groups

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5.4.2.3 ESM_EN Register

5.4.2.3.1 ESM_EN Register (Offset = 8h) [reset = 0h]

The Global Enable Register has the master interrupt mask.

Return to Summary Table

Table 5-1062. Instance Table

Instance Name	Physical Address
ESM0	52D0 0008h

Figure 5-525. ESM_EN Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				R/W			
0h				0h			

Table 5-1063. ESM_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	R/W	0h	Global Enable. This field is a global mask to all interrupts. It is reset by the warm reset. The purpose is to leave all of the raw status and per-interrupt enable bits alone so that, after a warm reset, software may observe the state of the ESM before the warm reset and try to debug what may have caused the reset. 0x0: All events are disabled 0xF: All events are enabled All others are invalid

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5.4.2.4 ESM_SFT_RST Register

5.4.2.4.1 ESM_SFT_RST Register (Offset = Ch) [reset = 0h]

The Global Soft Reset Register controls the global clear for raw status and enables.

Return to Summary Table

Table 5-1064. Instance Table

Instance Name	Physical Address
ESM0	52D0 000Ch

Figure 5-526. ESM_SFT_RST Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				KEY			
NONE				W			
0h				0h			

Table 5-1065. ESM_SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	KEY	W	0h	Global Soft Reset. Writing to this field can cause all of the raw status and all enables to be cleared. This can be used to reset the ESM state after debugging because of a warm reset. Write: 0xF: Clear all raw status and enable bits All others no effect Read: Always read as 0x0

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5.4.2.5 ESM_ERR_RAW Register

5.4.2.5.1 ESM_ERR_RAW Register (Offset = 10h) [reset = 0h]

Raw Status/Set Register for Configuration Errors.

Return to Summary Table

Table 5-1066. Instance Table

Instance Name	Physical Address
ESM0	52D0 0010h

Figure 5-527. ESM_ERR_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				STS			
NONE				R/W1TS			
0h				0h			

Table 5-1067. ESM_ERR_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	STS	R/W1TS	0h	This is the raw status for config errors. This is the raw status for errors in the configuration for Group N. This field is only reset by a Power-On-Reset and not by warm reset. A global soft reset will set this field to 0 Read: 0x0:Inactive 0x1:Active/Pending Write 0x1 to set event raw status Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect.

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5.4.2.6 ESM_ERR_STS Register

5.4.2.6.1 ESM_ERR_STS Register (Offset = 14h) [reset = 0h]

Config Error Enable and Clear Register.

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Table 5-1068. Instance Table

Instance Name	Physical Address
ESM0	52D0 0014h

Figure 5-528. ESM_ERR_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MSK			
NONE				R/W1TC			
0h				0h			

Table 5-1069. ESM_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	MSK	R/W1TC	0h	This is the masked status/clear for config errors. This is the masked status for errors in the configuration for Group N. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0:Inactive 0x1:Active/Pending and Enabled Write 0x1 to clear event raw status. Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect.

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5.4.2.7 ESM_ERR_EN_SET Register

5.4.2.7.1 ESM_ERR_EN_SET Register (Offset = 18h) [reset = 0h]

Config Error Enable Set Register.

Return to Summary Table

Table 5-1070. Instance Table

Instance Name	Physical Address
ESM0	52D0 0018h

Figure 5-529. ESM_ERR_EN_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MSK			
NONE				R/W1TS			
0h				0h			

Table 5-1071. ESM_ERR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	MSK	R/W1TS	0h	This is the mask enable set for config errors. This is the mask enable for errors in the configuration for Group N. If the corresponding bit and the global_enable are set, then then interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0:Disabled 0x1:Enabled Write 1'b1 to set enable Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect.

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5.4.2.8 ESM_ERR_EN_CLR Register

5.4.2.8.1 ESM_ERR_EN_CLR Register (Offset = 1Ch) [reset = 0h]

Config Error Interrupt Enabled Clear register.

Return to Summary Table

Table 5-1072. Instance Table

Instance Name	Physical Address
ESM0	52D0 001Ch

Figure 5-530. ESM_ERR_EN_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				MSK			
NONE				R/W1TC			
0h				0h			

Table 5-1073. ESM_ERR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	MSK	R/W1TC	0h	This is the mask enable clear for config errors. This is the mask clear for errors in the configuration for Group N. If the corresponding bit and the global_enable are set, then then interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0:Disabled 0x1:Enabled Write 1'b1 to clear enable Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect.

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5.4.2.9 ESM_LOW_PRI Register

5.4.2.9.1 ESM_LOW_PRI Register (Offset = 20h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding low priority interrupt.

Return to Summary Table

Table 5-1074. Instance Table

Instance Name	Physical Address
ESM0	52D0 0020h

Figure 5-531. ESM_LOW_PRI Name Register

31	30	29	28	27	26	25	24
PLS							
R							
FFFFh							
23	22	21	20	19	18	17	16
PLS							
R							
FFFFh							
15	14	13	12	11	10	9	8
LVL							
R							
FFFFh							
7	6	5	4	3	2	1	0
LVL							
R							
FFFFh							

Table 5-1075. ESM_LOW_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PLS	R	FFFFh	This is the highest priority outstanding low priority pulse interrupt. Indicates what the highest priority Low Priority interrupt caused by a pulse number is. The lowest event has the highest priority. i.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and are configured for High Priority while Global Events 2, 3, and 4 are configured for Low Priority, then the value of this field will be 0x2. value of all ones (0xFFFF) indicates that there are no low priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.
15:0	LVL	R	FFFFh	This is the highest priority outstanding low priority level interrupt. Indicates what the highest priority Low Priority interrupt caused by a level number is. The lowest event has the highest priority. i.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and are configured for High Priority while Global Events 2, 3, and 4 are configured for Low Priority, then the value of this field will be 0x2. value of all ones (0xFFFF) indicates that there are no low priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.

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5.4.2.10 ESM_HI_PRI Register

5.4.2.10.1 ESM_HI_PRI Register (Offset = 24h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding high priority interrupt.

Return to Summary Table

Table 5-1076. Instance Table

Instance Name	Physical Address
ESM0	52D0 0024h

Figure 5-532. ESM_HI_PRI Name Register

31	30	29	28	27	26	25	24
PLS							
R							
FFFFh							
23	22	21	20	19	18	17	16
PLS							
R							
FFFFh							
15	14	13	12	11	10	9	8
LVL							
R							
FFFFh							
7	6	5	4	3	2	1	0
LVL							
R							
FFFFh							

Table 5-1077. ESM_HI_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	PLS	R	FFFFh	This is the highest priority outstanding high priority pulse interrupt. Indicates what the highest priority High Priority interrupt caused by a pulse number is. The lowest event has the highest priority. i.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and are configured for High Priority while Global Events 2, 3, and 4 are configured for Low Priority, then the value of this field will be 0x2. value of all ones (0xFFFF) indicates that there are no low priority interrupts pending. This field is updated whenever a ew, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.
15:0	LVL	R	FFFFh	This is the highest priority outstanding high priority level interrupt. Indicates what the highest priority High Priority interrupt caused by a level number is. The lowest event has the highest priority. i.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and are configured for High Priority while Global Events 2, 3, and 4 are configured for Low Priority, then the value of this field will be 0x2. value of all ones (0xFFFF) indicates that there are no low priority interrupts pending. This field is updated whenever a ew, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.

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5.4.2.11 ESM_LOW Register

5.4.2.11.1 ESM_LOW Register (Offset = 28h) [reset = 0h]

Shows which groups have oustanding low priority interrupts.

Return to Summary Table

Table 5-1078. Instance Table

Instance Name	Physical Address
ESM0	52D0 0028h

Figure 5-533. ESM_LOW Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 5-1079. ESM_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	This is the raw status for config errors. Indicates which Event Groups have one or more Low Priority interrupts pending. This register is bit oriented where bit 0 is for Event Group 0, bit 1 is for Event Group 1, etc (bit N is for Event Group N).

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5.4.2.12 ESM_HI Register

5.4.2.12.1 ESM_HI Register (Offset = 2Ch) [reset = 0h]

Shows which groups have oustanding high priority interrupts.

Return to Summary Table

Table 5-1080. Instance Table

Instance Name	Physical Address
ESM0	52D0 002Ch

Figure 5-534. ESM_HI Name Register

31	30	29	28	27	26	25	24
STS							
R							
0h							
23	22	21	20	19	18	17	16
STS							
R							
0h							
15	14	13	12	11	10	9	8
STS							
R							
0h							
7	6	5	4	3	2	1	0
STS							
R							
0h							

Table 5-1081. ESM_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R	0h	This is the raw status for config errors. Indicates which Event Groups have one or more High Priority interrupts pending. This register is bit oriented where bit 0 is for Event Group 0, bit 1 is for Event Group 1, etc (bit N is for Event Group N).

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5.4.2.13 ESM_EOI Register

5.4.2.13.1 ESM_EOI Register (Offset = 30h) [reset = 0h]

End of Interrupt Register.

Return to Summary Table

Table 5-1082. Instance Table

Instance Name	Physical Address
ESM0	52D0 0030h

Figure 5-535. ESM_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					KEY		
NONE					W		
0h					0h		
7	6	5	4	3	2	1	0
KEY							
W							
0h							

Table 5-1083. ESM_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	KEY	W	0h	This is the interrupt being serviced. Writing the corresponding vector to this field will cause a reevaluation of interrupts. If, when the vector is written, there are still pending interrupts, a new pulse will be generated. 0x0: Configuration Error Interrupt 0x1: Low Priority Error Interrupt 0x2: High Priority Error Interrupt All other values are reserved(writes have no effect).

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5.4.2.14 ESM_PIN_CTRL Register

5.4.2.14.1 ESM_PIN_CTRL Register (Offset = 40h) [reset = 0h]

This register controls the error_pin_n output.

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Table 5-1084. Instance Table

Instance Name	Physical Address
ESM0	52D0 0040h

Figure 5-536. ESM_PIN_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
PWM_EN				KEY			
R/W				R/W			
0h				0h			

Table 5-1085. ESM_PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	PWM_EN	R/W	0h	PWM enable. PWM mode enable. This field should only be modified when the ESM is disabled, from the Global Enable register. This field is only reset by a Power-On-Reset (not warm reset). 0x0:Error output pin is a level 0xF:Error output pin is a PWM signal All other are invalid

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Table 5-1085. ESM_PIN_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	KEY	R/W	0h	Pin Control Key. This field controls behavior of the Error Pin. Note, during reset the field is 0x0, but the Error Pin is asserted (active low). Immediately after reset, the Error Pin de-asserts. This field is only reset by a Power-On-Reset (not warm reset). 0x0: Normal Mode - Error Pin will activate when an enabled Error Event occurs 0xA: Force Error Mode - Forces the Error Pin active. To clear the Error Pin (return to the ESM_IDLE state) write this field back to Normal Mode (Writing a CLEAR event will also work). You may only write to Force Error Mode while in IDLE. Attempting Force Error while in another state will have no effect 0x5 : CLEAR Event - generates a CLEAR event to the ESM state machine. Key will return to Normal Mode (0x0) on the next cycle. All Other Values - Normal Mode. Writing any of these values will have no effect. Reading any of these values indicate that one or more bits have experienced a single event upset and software should write the field back to 0x0. The ESM will continue to operate in Normal Mode

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5.4.2.15 ESM_PIN_STS Register

5.4.2.15.1 ESM_PIN_STS Register (Offset = 44h) [reset = 0h]

This register reflects the status of the error_pin_n output.

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Table 5-1086. Instance Table

Instance Name	Physical Address
ESM0	52D0 0044h

Figure 5-537. ESM_PIN_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							VAL
NONE							R
0h							0h

Table 5-1087. ESM_PIN_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	VAL	R	0h	Value of the error_pin_n. This field indicates the status of the Error Pin as looped back from the I/O. This field reflects the state of SAFETY_ERRORn I/O. 0x1 - De-Asserted 0x0 - Asserted Note, while in reset the error pin is actually active (asserted low), but goes inactive immediately after the de-assertion of Power-on-Reset. Hence, the value that will be read after Power-on-Reset is 1, but may be 0 after a warm reset.

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5.4.2.16 ESM_PIN_CNTR Register

5.4.2.16.1 ESM_PIN_CNTR Register (Offset = 48h) [reset = 0h]

This register shows the current value of the error pin counter.

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Table 5-1088. Instance Table

Instance Name	Physical Address
ESM0	52D0 0048h

Figure 5-538. ESM_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 5-1089. ESM_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value. This field indicates the current value of the Time Interval Counter. Register is reloaded to the counter preload value on entry to the ESM_ERROR state from ESM_IDLE and counts down by one per clock cycle. Once the counter has reached 0, the Minimum Time Interval has expired. This field is only reset by a Power-On-Reset (not warm reset).

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5.4.2.17 ESM_PIN_CNTR_PRE Register

5.4.2.17.1 ESM_PIN_CNTR_PRE Register (Offset = 4Ch) [reset = 0h]

This register contains the value that is loaded in to the Error Counter.

Return to Summary Table

Table 5-1090. Instance Table

Instance Name	Physical Address
ESM0	52D0 004Ch

Figure 5-539. ESM_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-1091. ESM_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value. This is the value that will be loaded in to the counter field of the Error Pin Counter Value Register whenever the ESM enters the ESM_ERROR state from ESM_IDLE. This field is only reset by a Power-On-Reset (not warm reset).

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5.4.2.18 ESM_PWMH_PIN_CNTR Register

5.4.2.18.1 ESM_PWMH_PIN_CNTR Register (Offset = 50h) [reset = 0h]

This register shows the current value of the error pin PWM high counter.

Return to Summary Table

Table 5-1092. Instance Table

Instance Name	Physical Address
ESM0	52D0 0050h

Figure 5-540. ESM_PWMH_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 5-1093. ESM_PWMH_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value. This field indicates the current value of the PWM High Time Interval Counter. The reset value is the 24'h0186A0. If pwm_en is set to PWM mode, then this register is enabled. This register is reloaded to the PWM high PIN_CNTR_PRE.count value when the error output pin toggles high. It will decrement by 1 each cycle when the error output pin is high. Once the counter has reached 0, the error output pin will toggle low. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 24'h0186A0.

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5.4.2.19 ESM_PWMH_PIN_CNTR_PRE Register

5.4.2.19.1 ESM_PWMH_PIN_CNTR_PRE Register (Offset = 54h) [reset = 0h]

This register contains the value that is loaded in to the Error PWM High Counter.

Return to Summary Table

Table 5-1094. Instance Table

Instance Name	Physical Address
ESM0	52D0 0054h

Figure 5-541. ESM_PWMH_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-1095. ESM_PWMH_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value. This is the value that will be loaded in to the counter field of the Error Pin PWM High Counter Value Register whenever the error output pin toggles high. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 24'h0186A0.

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5.4.2.20 ESM_PWML_PIN_CNTR Register

5.4.2.20.1 ESM_PWML_PIN_CNTR Register (Offset = 58h) [reset = 0h]

This register shows the current value of the error pin PWM low counter.

Return to Summary Table

Table 5-1096. Instance Table

Instance Name	Physical Address
ESM0	52D0 0058h

Figure 5-542. ESM_PWML_PIN_CNTR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 5-1097. ESM_PWML_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R	0h	Current Counter Value. This field indicates the current value of the PWM Low Time Interval Counter. The reset value is the 24'h0186A0. If pwm_en is set to PWM mode, then this register is enabled. This register is reloaded to the PWM low counter_preload value when the error output pin toggles low. It will decrement by 1 each cycle when the error output pin is low. Once the counter has reached 0, the error output pin will toggle high. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 24'h0186A0.

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5.4.2.21 ESM_PWML_PIN_CNTR_PRE Register

5.4.2.21.1 ESM_PWML_PIN_CNTR_PRE Register (Offset = 5Ch) [reset = 0h]

This register contains the value that is loaded in to the Error PWM Low Counter.

Return to Summary Table

Table 5-1098. Instance Table

Instance Name	Physical Address
ESM0	52D0 005Ch

Figure 5-543. ESM_PWML_PIN_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-1099. ESM_PWML_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:0	COUNT	R/W	0h	Counter Pre-Load Value. This is the value that will be loaded in to the counter field of the Error Pin PWM Low Counter Value Register whenever the error output pin toggles low. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 24'h0186A0.

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5.4.2.22 ESM_CRIT_DELAY_CNTR Register

5.4.2.22.1 ESM_CRIT_DELAY_CNTR Register (Offset = 60h) [reset = 0h]

This register shows the current value of the Critical Priority Interrupt Delay Counter.

Return to Summary Table

Table 5-1100. Instance Table

Instance Name	Physical Address
ESM0	52D0 0060h

Figure 5-544. ESM_CRIT_DELAY_CNTR Name Register

31	30	29	28	27	26	25	24
COUNT							
R							
0h							
23	22	21	20	19	18	17	16
COUNT							
R							
0h							
15	14	13	12	11	10	9	8
COUNT							
R							
0h							
7	6	5	4	3	2	1	0
COUNT							
R							
0h							

Table 5-1101. ESM_CRIT_DELAY_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R	0h	Current Counter Value. This field indicates the current value of the Critical Priority Interrupt Delay Counter. The reset value is the crit_delay_cntr_ipcfg tie-off. This register decrements by 1 each cycle there is an input error event asserted which can influence the critical priority interrupt. This register is reloaded to the Critical Priority Interrupt Delay counter_preload value if there are no critical priority interrupt influential events left and the register count value is still non-zero. Once the counter has reached 0, the critical priority interrupt outputs will assert/pulse. A warm reset or global soft reset will set this field to crit_delay_cntr_ipcfg.

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5.4.2.23 ESM_CRIT_DELAY_CNTR_PRE Register

5.4.2.23.1 ESM_CRIT_DELAY_CNTR_PRE Register (Offset = 64h) [reset = 0h]

This register contains the value that is loaded into the Critical Priority Interrupt Delay Counter.

Return to Summary Table

Table 5-1102. Instance Table

Instance Name	Physical Address
ESM0	52D0 0064h

Figure 5-545. ESM_CRIT_DELAY_CNTR_PRE Name Register

31	30	29	28	27	26	25	24
COUNT							
R/W							
0h							
23	22	21	20	19	18	17	16
COUNT							
R/W							
0h							
15	14	13	12	11	10	9	8
COUNT							
R/W							
0h							
7	6	5	4	3	2	1	0
COUNT							
R/W							
0h							

Table 5-1103. ESM_CRIT_DELAY_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COUNT	R/W	0h	Counter Pre-Load Value. This is the value that will be loaded in to the counter field of the Critical Priority Interrupt Delay Counter Value Register whenever there are no critical priority interrupt influential events left and the register count value is still non-zero. The default value is determined by a module tie-off crit_delay_cntr_ipcfg. If an immediate, no-delayed interrupt is needed, the tieoff value can be assigned to 0 or software can program the field to be 0. Note that the ESM clock is required to be active and that the ESM still requires 2-3 cycles to observe aninput error event. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to crit_delay_cntr_ipcfg.

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5.4.2.24 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_RAW_J Register

5.4.2.24.1 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_RAW_J Register (Offset = 400h) [reset = 0h]

Raw Status/Set Register for Group A Errors

Return to Summary Table

Table 5-1104. Instance Table

Instance Name	Physical Address
ESM0	52D0 0400h + formula

Figure 5-546. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_RAW_j Name Register

31	30	29	28	27	26	25	24
STS							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
STS							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
STS							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
STS							
R/W1TS							
0h							

Table 5-1105. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	STS	R/W1TS	0h	This is the raw status/set for errors Group A. This is the raw status of the events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc). For Level events, the raw status is the event input synchronized to the ESM clock and stored in a multi-bit (for redundancy) internal register. For Pulse events, the raw status is multi-bit (for redundancy) internal register that is set when two of the three edge detection circuits on the redundant event capture a rising edge. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0: Inactive 0x1: Active/Pending Write 0x1 to set interrupt raw status.

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5.4.2.25 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_STS_J Register

5.4.2.25.1 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_STS_J Register (Offset = 404h) [reset = 0h]

Error Enable and Clear Register

Return to Summary Table

Table 5-1106. Instance Table

Instance Name	Physical Address
ESM0	52D0 0404h + formula

Figure 5-547. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_STS_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 5-1107. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the masked status/clear for errors in Group A. This is the masked status of the events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc...). This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0: Inactive 0x1: Active/Pending Write 0x1 to clear interrupt raw status.

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5.4.2.26 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_SET_J Register

5.4.2.26.1 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_SET_J Register (Offset = 408h) [reset = 0h]

Level Error Enable Set Register

Return to Summary Table

Table 5-1108. Instance Table

Instance Name	Physical Address
ESM0	52D0 0408h + formula

Figure 5-548. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 5-1109. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the mask enable set for errors in Group A. This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit. If the corresponding bit and the global_enable are set, then then interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0: Disabled 0x1: Enabled Write 0x1 to set enable

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5.4.2.27 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_CLR_J Register

5.4.2.27.1 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_CLR_J Register (Offset = 40Ch) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to Summary Table

Table 5-1110. Instance Table

Instance Name	Physical Address
ESM0	52D0 040Ch + formula

Figure 5-549. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 5-1111. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the mask enable clear for errors in Group A. This field is used to disable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit. If the corresponding bit and the global_enable are set, then then interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0: Disabled 0x1: Enabled Write 1'b1 to clear enable

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5.4.2.28 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INT_PRIO_J Register

5.4.2.28.1 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INT_PRIO_J Register (Offset = 410h) [reset = 0h]

Level Error Interrupt Priority register

Return to Summary Table

Table 5-1112. Instance Table

Instance Name	Physical Address
ESM0	52D0 0410h + formula

Figure 5-550. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INT_PRIO_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W							
0h							

Table 5-1113. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INT_PRIO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W	0h	This is interrupt priority for errors in Group A. This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group N. Each bit corresponds to event Q where Q = N*32+Bit. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. 0x0 - Low Priority Interrupt 0x1 - High Priority Interrupt

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5.4.2.29 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_SET_J Register

5.4.2.29.1 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_SET_J Register (Offset = 414h) [reset = 0h]

Error Pin Enabled Set register

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Table 5-1114. Instance Table

Instance Name	Physical Address
ESM0	52D0 0414h + formula

Figure 5-551. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 5-1115. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the error pin influence enable set for errors in Group A. This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0: Disabled 0x1: Enabled Write 1'b1 to set enable

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5.4.2.30 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_CLR_J Register

5.4.2.30.1 ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_CLR_J Register (Offset = 418h) [reset = 0h]

Error Pin Enabled Clear register

Return to Summary Table

Table 5-1116. Instance Table

Instance Name	Physical Address
ESM0	52D0 0418h + formula

Figure 5-552. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 5-1117. ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the error pin influence enable clear for errors in Group A. This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0: Disabled 0x1: Enabled Write 1'b1 to clear enable

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5.4.2.31 ESM_PCR_GENERATED_MEMORY_MAP_ERR_EXT_GRP_CRIT_EN_SET_J Register

5.4.2.31.1 ESM_PCR_GENERATED_MEMORY_MAP_ERR_EXT_GRP_CRIT_EN_SET_J Register (Offset = 800h) [reset = 0h]

Level Critical Priority Interrupt Enabled Clear register

Return to Summary Table

Table 5-1118. Instance Table

Instance Name	Physical Address
ESM0	52D0 0800h + formula

Figure 5-553. ESM_PCR_GENERATED_MEMORY_MAP_ERR_EXT_GRP_CRIT_EN_SET_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TS							
0h							

Table 5-1119. ESM_PCR_GENERATED_MEMORY_MAP_ERR_EXT_GRP_CRIT_EN_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TS	0h	This is the critical priority interrupt influence enable set for errors in Group A. This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc) This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0: Disabled 0x1: Enabled Write: 0x0: No effect 0x1: Set Enable. Corresponding event, when set, will count as a pending event towards generating a critical priority interrupt if not cleared by cycle count in the critical priority interrupt delay counter register.

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5.4.2.32 ESM_PCR_GENERATED_MEMORY_MAP_ERR_EXT_GRP_CRIT_EN_CLR_J Register

5.4.2.32.1 ESM_PCR_GENERATED_MEMORY_MAP_ERR_EXT_GRP_CRIT_EN_CLR_J Register (Offset = 804h) [reset = 0h]

Level Critical Priority Interrupt Enabled Clear register

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Table 5-1120. Instance Table

Instance Name	Physical Address
ESM0	52D0 0804h + formula

Figure 5-554. ESM_PCR_GENERATED_MEMORY_MAP_ERR_EXT_GRP_CRIT_EN_CLR_j Name Register

31	30	29	28	27	26	25	24
MSK							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
MSK							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
MSK							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
MSK							
R/W1TC							
0h							

Table 5-1121. ESM_PCR_GENERATED_MEMORY_MAP_ERR_EXT_GRP_CRIT_EN_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MSK	R/W1TC	0h	This is the critical priority interrupt influence enable clear for errors in Group A. This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc) This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. Read: 0x0: Disabled 0x1: Enabled Write: 0x0: No effect 0x1: Clear Enable. Corresponding events will no longer count as pending events towards generating a critical priority interrupt.

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5.5 RL2

RL2

5.5.1 RL2 Summaries

RL2 Summaries

Table 5-1122. RL2 Registers, Base Address=5321 2000h, Length=1024

Offset	Length	Register Name	RL2_R5SS0_CORE0 Physical Address	RL2_R5SS0_CORE1 Physical Address	RL2_R5SS1_CORE0 Physical Address
0h	32	RL2_MOD_VER	5321 2000h	5321 3000h	5321 4000h
4h	32	RL2_L2_CTRL	5321 2004h	5321 3004h	5321 4004h
8h	32	RL2_L2_STS	5321 2008h	5321 3008h	5321 4008h
10h	32	RL2_L2_LO	5321 2010h	5321 3010h	5321 4010h
18h	32	RL2_L2_HI	5321 2018h	5321 3018h	5321 4018h
78h	32	RL2_L2HC	5321 2078h	5321 3078h	5321 4078h
7Ch	32	RL2_L2MC	5321 207Ch	5321 307Ch	5321 407Ch
80h	32	RL2_IRQSTATUS_RAW	5321 2080h	5321 3080h	5321 4080h
84h	32	RL2_IRQSTATUS_MSK	5321 2084h	5321 3084h	5321 4084h
88h	32	RL2_IRQENABLE_SET	5321 2088h	5321 3088h	5321 4088h
8Ch	32	RL2_IRQENABLE_CLR	5321 208Ch	5321 308Ch	5321 408Ch
104h	32	RL2_FLC_CFG	5321 2104h	5321 3104h	5321 4104h
108h	32	RL2_FLC_STS	5321 2108h	5321 3108h	5321 4108h
110h	32	RL2_FLC_DBG0	5321 2110h	5321 3110h	5321 4110h
114h	32	RL2_FLC_DBG1	5321 2114h	5321 3114h	5321 4114h
204h	32	RL2_RAT_CFG	5321 2204h	5321 3204h	5321 4204h
20h	32	RL2_REM_ADR_J	5321 2020h + formula	5321 3020h + formula	5321 4020h + formula
28h	32	RL2_REM_LEN_J	5321 2028h + formula	5321 3028h + formula	5321 4028h + formula
120h	32	RL2_FLC_LO_J	5321 2120h + formula	5321 3120h + formula	5321 4120h + formula
128h	32	RL2_FLC_HI_J	5321 2128h + formula	5321 3128h + formula	5321 4128h + formula
130h	32	RL2_FLC_RA_J	5321 2130h + formula	5321 3130h + formula	5321 4130h + formula
138h	32	RL2_FLC_CTL_J	5321 2138h + formula	5321 3138h + formula	5321 4138h + formula
220h	32	RL2_RAT_CTL_J	5321 2220h + formula	5321 3220h + formula	5321 4220h + formula
224h	32	RL2_RAT_RBA_J	5321 2224h + formula	5321 3224h + formula	5321 4224h + formula
228h	32	RL2_RAT_RTA_J	5321 2228h + formula	5321 3228h + formula	5321 4228h + formula

Table 5-1123. RL2 Registers, Base Address=5321 2000h, Length=1024

Offset	Length	Register Name	RL2_R5SS1_CORE1 Physical Address
0h	32	RL2_MOD_VER	5321 5000h
4h	32	RL2_L2_CTRL	5321 5004h
8h	32	RL2_L2_STS	5321 5008h
10h	32	RL2_L2_LO	5321 5010h
18h	32	RL2_L2_HI	5321 5018h
78h	32	RL2_L2HC	5321 5078h
7Ch	32	RL2_L2MC	5321 507Ch
80h	32	RL2_IRQSTATUS_RAW	5321 5080h
84h	32	RL2_IRQSTATUS_MSK	5321 5084h
88h	32	RL2_IRQENABLE_SET	5321 5088h
8Ch	32	RL2_IRQENABLE_CLR	5321 508Ch

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Table 5-1123. RL2 Registers, Base Address=5321 2000h, Length=1024 (continued)

Offset	Length	Register Name	RL2_R5SS1_CORE1 Physical Address
104h	32	RL2_FLC_CFG	5321 5104h
108h	32	RL2_FLC_STS	5321 5108h
110h	32	RL2_FLC_DBG0	5321 5110h
114h	32	RL2_FLC_DBG1	5321 5114h
204h	32	RL2_RAT_CFG	5321 5204h
20h	32	RL2_REM_ADR_J	5321 5020h + formula
28h	32	RL2_REM_LEN_J	5321 5028h + formula
120h	32	RL2_FLC_LO_J	5321 5120h + formula
128h	32	RL2_FLC_HI_J	5321 5128h + formula
130h	32	RL2_FLC_RA_J	5321 5130h + formula
138h	32	RL2_FLC_CTL_J	5321 5138h + formula
220h	32	RL2_RAT_CTL_J	5321 5220h + formula
224h	32	RL2_RAT_RBA_J	5321 5224h + formula
228h	32	RL2_RAT_RTA_J	5321 5228h + formula

5.5.2 RL2 Registers

RL2 Registers

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5.5.2.1 RL2_MOD_VER Register

5.5.2.1.1 RL2_MOD_VER Register (Offset = 0h) [reset = 68841900h]

The Module and Version Register identifies the module identifier and revision of the RL2 module.

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Table 5-1124. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2000h
RL2_R5SS0_CORE1	5321 3000h
RL2_R5SS1_CORE0	5321 4000h
RL2_R5SS1_CORE1	5321 5000h

Figure 5-555. RL2_MOD_VER Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		884h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
884h							
15	14	13	12	11	10	9	8
RTL_VERSION					MAJOR_REVISION		
R					R		
3h					1h		
7	6	5	4	3	2	1	0
CUSTOM_REVISION		MINOR_REVISION					
R		R					
0h		0h					

Table 5-1125. RL2_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Module Scheme
29:28	BU	R	2h	Module Business Unit
27:16	MODULE_ID	R	884h	RL2 module ID.
15:11	RTL_VERSION	R	3h	RTL Version.
10:8	MAJOR_REVISION	R	1h	Major Revision.
7:6	CUSTOM_REVISION	R	0h	Custom Revision.
5:0	MINOR_REVISION	R	0h	Minor Revision.

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5.5.2.2 RL2_L2_CTRL Register

5.5.2.2.1 RL2_L2_CTRL Register (Offset = 4h) [reset = 0h]

The control register defines the size of the remote cache data storage memory to use and whether the L2 is enabled.

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Table 5-1126. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2004h
RL2_R5SS0_CORE1	5321 3004h
RL2_R5SS1_CORE0	5321 4004h
RL2_R5SS1_CORE1	5321 5004h

Figure 5-556. RL2_L2_CTRL Name Register

31	30	29	28	27	26	25	24
ENABLE	RESERVED						
R/W	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					SIZE		
NONE					R/W		
0h					0h		

Table 5-1127. RL2_L2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	The enable field determines whether the L2 is enabled or not. Setting the enable from a 0 to 1 restarts the cache 0:Disabled 1:Enabled
30:3	RESERVED	NONE	0h	Reserved
2:0	SIZE	R/W	0h	The size field determines the size of the remote cache data storage memory that is currently active. This field can be change dynamically, but will cause the entire cache to be invalidated when inflight transactions have completed. Changing the size while enable is already a '1' will restart the cache. 0:8KB 1:16KB 2:32KB 3:64KB 4:128KB 5:256KB (Dual Mode) Note: Setting this field to an invalid value will result in the field being set to '0'. The remote address range registers must be setup correctly to ensure it has sufficient memory for the selected size.

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5.5.2.3 RL2_L2_STS Register

5.5.2.3.1 RL2_L2_STS Register (Offset = 8h) [reset = 0h]

The Status register displays the state of the RL2 module.

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Table 5-1128. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2008h
RL2_R5SS0_CORE1	5321 3008h
RL2_R5SS1_CORE0	5321 4008h
RL2_R5SS1_CORE1	5321 5008h

Figure 5-557. RL2_L2_STS Name Register

31	30	29	28	27	26	25	24
OK_TO_GO	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-1129. RL2_L2_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OK_TO_GO	R	0h	The ok_to_go status bit indicates the Tag/LRU Ram has been initialized and the cache is in an operable state.
30:0	RESERVED	NONE	0h	Reserved

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5.5.2.4 RL2_L2_LO Register

5.5.2.4.1 RL2_L2_LO Register (Offset = 10h) [reset = 0h]

The L2 Low address Least Significant word defines the least significant portion of the low cache address. The RL2 cache can cache a range of 1 to 16MB of cache as defined by L2_LO>=CachedRange<=L2_HI. This register is write protected when enable is set.

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Table 5-1130. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2010h
RL2_R5SS0_CORE1	5321 3010h
RL2_R5SS1_CORE0	5321 4010h
RL2_R5SS1_CORE1	5321 5010h

Figure 5-558. RL2_L2_LO Name Register

31	30	29	28	27	26	25	24
ADDRESS_LO_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS_LO_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS_LO_LSW					RESERVED		
R/W					NONE		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-1131. RL2_L2_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	ADDRESS_LO_LSW	R/W	0h	The address_lo_lsw defines the L2 low address[31:11] for the RL2 to cache. The remaining bits 10:0 are assumed to be zero.
10:0	RESERVED	NONE	0h	Reserved

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5.5.2.5 RL2_L2_HI Register

5.5.2.5.1 RL2_L2_HI Register (Offset = 18h) [reset = 0h]

The L2 High address Least Significant word defines the least significant portion of the high cache address. The RL2 cache can cache a range of 1 to 16MB of cache as defined by L2_LO>=CachedRange<=L2_HI. This register is write protected when enable is set.

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Table 5-1132. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2018h
RL2_R5SS0_CORE1	5321 3018h
RL2_R5SS1_CORE0	5321 4018h
RL2_R5SS1_CORE1	5321 5018h

Figure 5-559. RL2_L2_HI Name Register

31	30	29	28	27	26	25	24
ADDRESS_HI_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDRESS_HI_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDRESS_HI_LSW					RESERVED		
R/W					NONE		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-1133. RL2_L2_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	ADDRESS_HI_LSW	R/W	0h	The address_hi_lsw defines the high address[31:11] for the RL2 to cache. The remaining bits 10:0 are assumed to be ones.
10:0	RESERVED	NONE	0h	Reserved

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5.5.2.6 RL2_L2HC Register

5.5.2.6.1 RL2_L2HC Register (Offset = 78h) [reset = 0h]

The L2 HIT Counter register holds the number of L2 Hits to the Remote data storage memory.

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Table 5-1134. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2078h
RL2_R5SS0_CORE1	5321 3078h
RL2_R5SS1_CORE0	5321 4078h
RL2_R5SS1_CORE1	5321 5078h

Figure 5-560. RL2_L2HC Name Register

31	30	29	28	27	26	25	24
HIT							
R/W							
0h							
23	22	21	20	19	18	17	16
HIT							
R/W							
0h							
15	14	13	12	11	10	9	8
HIT							
R/W							
0h							
7	6	5	4	3	2	1	0
HIT							
R/W							
0h							

Table 5-1135. RL2_L2HC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HIT	R/W	0h	The hit Counts the number of hits to the L2 cache. Writing to this register will set the value written or restarting the cache will clear its contents. This field does not roll over, it will stop counting at all ones.

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5.5.2.7 RL2_L2MC Register

5.5.2.7.1 RL2_L2MC Register (Offset = 7Ch) [reset = 0h]

The L2 MISS Counter register holds the number of L2 Misses to the Remote data storage memory.

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Table 5-1136. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 207Ch
RL2_R5SS0_CORE1	5321 307Ch
RL2_R5SS1_CORE0	5321 407Ch
RL2_R5SS1_CORE1	5321 507Ch

Figure 5-561. RL2_L2MC Name Register

31	30	29	28	27	26	25	24
MISS							
R/W							
0h							
23	22	21	20	19	18	17	16
MISS							
R/W							
0h							
15	14	13	12	11	10	9	8
MISS							
R/W							
0h							
7	6	5	4	3	2	1	0
MISS							
R/W							
0h							

Table 5-1137. RL2_L2MC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	MISS	R/W	0h	The miss Counts the number of misses to the L2 cache. Writing to this register will set the value written or restarting the cache will clear its contents. This field does not roll over, it will stop counting at all ones.

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5.5.2.8 RL2_IRQSTATUS_RAW Register

5.5.2.8.1 RL2_IRQSTATUS_RAW Register (Offset = 80h) [reset = 0h]

The Interrupt Raw Status Register holds the raw status of the FLC/RL2 status/error interrupts.

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Table 5-1138. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2080h
RL2_R5SS0_CORE1	5321 3080h
RL2_R5SS1_CORE0	5321 4080h
RL2_R5SS1_CORE1	5321 5080h

Figure 5-562. RL2_IRQSTATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			FLC_DON	FLC_WRERR	FLC_RDERR	WR_HIT	WR_ERR
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 5-1139. RL2_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	FLC_DON	R/W1TS	0h	The flc_don bit indicates a FLC has completed the transfer to the FLC range. Write 1 to set the flc_don status for diagnostic purposes. Writing a 0 has no effect.
3	FLC_WRERR	R/W1TS	0h	The flc_wrerr bit indicates a write error from FLC remote range has occurred and the FLC is logically disabled while this bit is a '1'. Write 1 to set the flc_wrerr status for diagnostic purposes. Writing a 0 has no effect.
2	FLC_RDERR	R/W1TS	0h	The flc_rderr bit indicates a read error from FLC range has occurred and the FLC is logically disabled while this bit is a '1'. Write 1 to set the flc_rderr status for diagnostic purposes. Writing a 0 has no effect.
1	WR_HIT	R/W1TS	0h	The wr_hit bit indicates a write to the cacheable range has occurred potentially causing a coherency issue and the RL2 is logically disabled while this bit is a '1'. Write 1 to set the wr_hit status for diagnostic purposes. Writing a 0 has no effect.
0	WR_ERR	R/W1TS	0h	The wr_err bit indicates a write error has occurred to the remote cache data storage memory and the RL2 is logically disabled while this bit is a '1'. Write 1 to set the wr_err status for diagnostic purposes. Writing a 0 has no effect.

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5.5.2.9 RL2_IRQSTATUS_MSK Register

5.5.2.9.1 RL2_IRQSTATUS_MSK Register (Offset = 84h) [reset = 0h]

The Interrupt Masked Status Register holds the masked status for the FLC/RL2 status/error interrupts. Writing to this register will EOI the interrupt, that is if another interrupt is pending, a new pulse interrupt will be generated.

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Table 5-1140. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2084h
RL2_R5SS0_CORE1	5321 3084h
RL2_R5SS1_CORE0	5321 4084h
RL2_R5SS1_CORE1	5321 5084h

Figure 5-563. RL2_IRQSTATUS_MSK Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			FLC_DON	FLC_WRERR	FLC_RDERR	WR_HIT	WR_ERR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 5-1141. RL2_IRQSTATUS_MSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	FLC_DON	R/W1TC	0h	The flc_don bit indicates a FLC has completed the transfer to the FLC range. Write 1 to clear the flc_don status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.
3	FLC_WRERR	R/W1TC	0h	The flc_wrerr bit indicates a write error from FLC range has occurred and the FLC is logically disabled while this bit is a '1'. Write 1 to clear the flc_wrerr status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.
2	FLC_RDERR	R/W1TC	0h	The flc_rderr bit indicates a read error from FLC range has occurred and the FLC is logically disabled while this bit is a '1'. Write 1 to clear the flc_rderr status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.
1	WR_HIT	R/W1TC	0h	The wr_hit bit indicates a write to the cacheable range has occurred potentially causing a coherency issue and the RL2 is logically disabled while this bit is a '1'. Write 1 to clear the wr_hit status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.

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Table 5-1141. RL2_IRQSTATUS_MSK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WR_ERR	R/W1TC	0h	The wr_err bit indicates a write error has occurred to the remote cache data storage memory and the RL2 is logically disabled while this bit is a '1'. Write 1 to clear the wr_err status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect to this field.

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5.5.2.10 RL2_IRQENABLE_SET Register

5.5.2.10.1 RL2_IRQENABLE_SET Register (Offset = 88h) [reset = 0h]

The Interrupt Enable Set Register holds the interrupt enable status of the FLC/RL2 status/error interrupts.

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Table 5-1142. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2088h
RL2_R5SS0_CORE1	5321 3088h
RL2_R5SS1_CORE0	5321 4088h
RL2_R5SS1_CORE1	5321 5088h

Figure 5-564. RL2_IRQENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			EN_FLC_DON	EN_FLC_WRERR	EN_FLC_RDERR	EN_WR_HIT	EN_WR_ERR
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 5-1143. RL2_IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EN_FLC_DON	R/W1TS	0h	Interrupt Enable Set for en_flc_don status bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
3	EN_FLC_WRERR	R/W1TS	0h	Interrupt Enable Set for en_flc_wrerr error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
2	EN_FLC_RDERR	R/W1TS	0h	Interrupt Enable Set for en_flc_rderr error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
1	EN_WR_HIT	R/W1TS	0h	Interrupt Enable Set for wr_hit error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
0	EN_WR_ERR	R/W1TS	0h	Interrupt Enable Set for wr_err error bit. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

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5.5.2.11 RL2_IRQENABLE_CLR Register

5.5.2.11.1 RL2_IRQENABLE_CLR Register (Offset = 8Ch) [reset = 0h]

The Interrupt Enable Clear Register holds the interrupt enable status of the FLC/RL2 status/error interrupts.

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Table 5-1144. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 208Ch
RL2_R5SS0_CORE1	5321 308Ch
RL2_R5SS1_CORE0	5321 408Ch
RL2_R5SS1_CORE1	5321 508Ch

Figure 5-565. RL2_IRQENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			EN_FLC_DON	EN_FLC_WRERR	EN_FLC_RDERR	EN_WR_HIT	EN_WR_ERR
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 5-1145. RL2_IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	EN_FLC_DON	R/W1TC	0h	Interrupt Enable Clear for flc_don status bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
3	EN_FLC_WRERR	R/W1TC	0h	Interrupt Enable Clear for flc_wrerr error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
2	EN_FLC_RDERR	R/W1TC	0h	Interrupt Enable Clear for flc_rderr error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
1	EN_WR_HIT	R/W1TC	0h	Interrupt Enable Clear for wr_hit error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
0	EN_WR_ERR	R/W1TC	0h	Interrupt Enable Clear for wr_err error bit. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.

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5.5.2.12 RL2_FLC_CFG Register

5.5.2.12.1 RL2_FLC_CFG Register (Offset = 104h) [reset = 504h]

The FLC Config Register contains the configuration values for the FLC.

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Table 5-1146. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2104h
RL2_R5SS0_CORE1	5321 3104h
RL2_R5SS1_CORE0	5321 4104h
RL2_R5SS1_CORE1	5321 5104h

Figure 5-566. RL2_FLC_CFG Name Register

31	30	29	28	27	26	25	24
FIFO_BYPASS	RESERVED				FLC_EXCNT		
R/W	NONE				R/W		
0h	0h				0h		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ASMNUM							
R							
5h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RANGES							
R							
4h							

Table 5-1147. RL2_FLC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FIFO_BYPASS	R/W	0h	Setting this bit will cause the write to remote memory for a cache miss or FLC return to forces stalls on the read returns if any other data phase for a cache miss or FLC return is received. This can cause stalls on the write to force stalls on the read.
30:27	RESERVED	NONE	0h	Reserved
26:24	FLC_EXCNT	R/W	0h	The number of extra requests the FLC can send. The maximum value is 4 anything greater will default to 4. This value + 1 is the number of Reassembly Buffers used for FLC so if cache misses needed to be supported this value should be set to 4 or lower. The number of cache misses that will be allowed to be outstanding while FLC is running will be 5 - (FLC_EXCNT + 1).
23:16	RESERVED	NONE	0h	Reserved
15:8	ASMNUM	R	5h	Number of Reassembly Buffer supported
7:0	RANGES	R	4h	Number of FLC ranges supported

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5.5.2.13 RL2_FLC_STS Register

5.5.2.13.1 RL2_FLC_STS Register (Offset = 108h) [reset = 0h]

The FLC Status Register will indicate the state of the FLC completion.

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Table 5-1148. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2108h
RL2_R5SS0_CORE1	5321 3108h
RL2_R5SS1_CORE0	5321 4108h
RL2_R5SS1_CORE1	5321 5108h

Figure 5-567. RL2_FLC_STS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				CPYCMP			
NONE				R			
0h				0h			

Table 5-1149. RL2_FLC_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	CPYCMP	R	0h	The cpycmp indicates which FLC range is complete. Each bit index indicates the FLC range is complete.

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5.5.2.14 RL2_FLC_DBG0 Register

5.5.2.14.1 RL2_FLC_DBG0 Register (Offset = 110h) [reset = 0h]

The FLC Debug 0 Register holds the debug state of the FLC.

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Table 5-1150. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2110h
RL2_R5SS0_CORE1	5321 3110h
RL2_R5SS1_CORE0	5321 4110h
RL2_R5SS1_CORE1	5321 5110h

Figure 5-568. RL2_FLC_DBG0 Name Register

31	30	29	28	27	26	25	24
FLCIF	RESERVED				FLC_OUT_CNT		
R	NONE				R		
0h	0h				0h		
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CURFLC	
NONE						R	
0h						0h	

Table 5-1151. RL2_FLC_DBG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FLCIF	R	0h	The flcif indicates a FLC operation is in flight.
30:27	RESERVED	NONE	0h	Reserved
26:24	FLC_OUT_CNT	R	0h	The number of read requests the FLC operation has in flight.
23:2	RESERVED	NONE	0h	Reserved
1:0	CURFLC	R	0h	The curflc indicates which FLC range is in flight.

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5.5.2.15 RL2_FLC_DBG1 Register

5.5.2.15.1 RL2_FLC_DBG1 Register (Offset = 114h) [reset = 0h]

The FLC Debug 1 Register holds the debug address of the FLC.

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Table 5-1152. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2114h
RL2_R5SS0_CORE1	5321 3114h
RL2_R5SS1_CORE0	5321 4114h
RL2_R5SS1_CORE1	5321 5114h

Figure 5-569. RL2_FLC_DBG1 Name Register

31	30	29	28	27	26	25	24
FLCADR							
R							
0h							
23	22	21	20	19	18	17	16
FLCADR							
R							
0h							
15	14	13	12	11	10	9	8
FLCADR							
R							
0h							
7	6	5	4	3	2	1	0
FLCADR							
R							
0h							

Table 5-1153. RL2_FLC_DBG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FLCADR	R	0h	The flcadr indicates the next FLC address to be processed if still in flight. That is all addresses less than this address have been transferred. This address is used for FLC hit when the particular FLC range is in flight. That is FLC_LO>=FLCrange<flc_dbg1.flcadr would result in a hit. This address will match the last FLC transferred FLC_HI when no FLC ranges are in flight.

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5.5.2.16 RL2_RAT_CFG Register

5.5.2.16.1 RL2_RAT_CFG Register (Offset = 204h) [reset = 200004h]

The RAT Config Register contains the configuration values for the RAT.

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Table 5-1154. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2204h
RL2_R5SS0_CORE1	5321 3204h
RL2_R5SS1_CORE0	5321 4204h
RL2_R5SS1_CORE1	5321 5204h

Figure 5-570. RL2_RAT_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
ADDR_WIDTH							
R							
20h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
REGIONS							
R							
4h							

Table 5-1155. RL2_RAT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	ADDR_WIDTH	R	20h	Number of address bits
15:8	RESERVED	NONE	0h	Reserved
7:0	REGIONS	R	4h	Number of regions

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5.5.2.17 RL2_REM_ADR_J Register

5.5.2.17.1 RL2_REM_ADR_J Register (Offset = 20h) [reset = 0h]

The REMote 'n' Address Least Significant word defines the least significant portion of the Remote address for remote cache data storage memory 0. The RL2 cache use up to three remote cache data storage memory ranges to place the L2 data within. The length of these ranges must be greater or equal to the size specified. This register is write protected when enable is set.

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Table 5-1156. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2020h + formula
RL2_R5SS0_CORE1	5321 3020h + formula
RL2_R5SS1_CORE0	5321 4020h + formula
RL2_R5SS1_CORE1	5321 5020h + formula

Figure 5-571. RL2_REM_ADR_j Name Register

31	30	29	28	27	26	25	24
ADR_LSW							
R/W							
0h							
23	22	21	20	19	18	17	16
ADR_LSW							
R/W							
0h							
15	14	13	12	11	10	9	8
ADR_LSW					RESERVED		
R/W					NONE		
0h					0h		
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-1157. RL2_REM_ADR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	ADR_LSW	R/W	0h	The rem0_adr_lsw defines the LSW of the remote cache data storage memory address[31:11] range 'n' for the RL2 to use for the cache. The remaining bits 10:0 are assumed to be zero.
10:0	RESERVED	NONE	0h	Reserved

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5.5.2.18 RL2_REM_LEN_J Register

5.5.2.18.1 RL2_REM_LEN_J Register (Offset = 28h) [reset = 0h]

The Remote 'n' length defines the amount of remote cache data storage memory in 64 byte aligned quanta used starting from the REMote 'n' Address. The RL2 consumes remote cache data storage memory ranges in numeric order. Range 0 is consumed prior to range 1, etc. This register is write protected when enable is set.

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Table 5-1158. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2028h + formula
RL2_R5SS0_CORE1	5321 3028h + formula
RL2_R5SS1_CORE0	5321 4028h + formula
RL2_R5SS1_CORE1	5321 5028h + formula

Figure 5-572. RL2_REM_LEN_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED					LEN		
NONE					R/W		
0h					0h		
15	14	13	12	11	10	9	8
LEN							
R/W							
0h							
7	6	5	4	3	2	1	0
LEN		RESERVED					
R/W		NONE					
0h		0h					

Table 5-1159. RL2_REM_LEN_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:6	LEN	R/W	0h	The rem0_len field specifies the length of the remote cache data storage memory 'n' to use for the RL2 cache in 64 byte quanta, That is the number of bytes specified in the remote cache data storage memory range 'n' is (rem0_len X 64). Note: Any value greater than 4096 assumes 4096
5:0	RESERVED	NONE	0h	Reserved

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5.5.2.19 RL2_FLC_LO_J Register

5.5.2.19.1 RL2_FLC_LO_J Register (Offset = 120h) [reset = 0h]

The FLC Low 'n' address defines the FLC lo address for FLC range 0. The FLC range is defined by FLC_LO0>=FLCrange<FLC_HI0. This register is write protected when fenable0 is set.

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Table 5-1160. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2120h + formula
RL2_R5SS0_CORE1	5321 3120h + formula
RL2_R5SS1_CORE0	5321 4120h + formula
RL2_R5SS1_CORE1	5321 5120h + formula

Figure 5-573. RL2_FLC_LO_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">ADR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">ADR_LO</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">ADR_LO</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">NONE</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
</table>

Table 5-1161. RL2_FLC_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	ADR_LO	R/W	0h	The adr0_lo defines the FLC low address[31:12] for the FLC to copy. The remaining bits 11:0 are assumed to be zero.
11:0	RESERVED	NONE	0h	Reserved

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5.5.2.20 RL2_FLC_HI_J Register

5.5.2.20.1 RL2_FLC_HI_J Register (Offset = 128h) [reset = 0h]

The FLC High 'n' address defines the FLC high address for FLC range 0. The FLC range is defined by FLC_LO0>=FLCrange<FLC_HI0. This register is write protected when fenable0 is set.

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Table 5-1162. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2128h + formula
RL2_R5SS0_CORE1	5321 3128h + formula
RL2_R5SS1_CORE0	5321 4128h + formula
RL2_R5SS1_CORE1	5321 5128h + formula

Figure 5-574. RL2_FLC_HI_j Name Register

31	30	29	28	27	26	25	24
ADR_HI							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ADR_HI							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ADR_HI				RESERVED			
R/W				NONE			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 5-1163. RL2_FLC_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	ADR_HI	R/W	0h	The adr0_hi defines the FLC high address[31:12] for the FLC to copy. The remaining bits 11:0 are assumed to be ones.
11:0	RESERVED	NONE	0h	Reserved

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5.5.2.21 RL2_FLC_RA_J Register

5.5.2.21.1 RL2_FLC_RA_J Register (Offset = 130h) [reset = 0h]

The FLC Remote Address 'n' specifies the SRAM location base address the FLC will copy slow Flash data to the SRAM. That is the SRAM is acting like a block cacke for a slow device.

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Table 5-1164. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2130h + formula
RL2_R5SS0_CORE1	5321 3130h + formula
RL2_R5SS1_CORE0	5321 4130h + formula
RL2_R5SS1_CORE1	5321 5130h + formula

Figure 5-575. RL2_FLC_RA_j Name Register

31	30	29	28	27	26	25	24
RADR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RADR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RADR				RESERVED			
R/W				NONE			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
NONE							
0h							

Table 5-1165. RL2_FLC_RA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RADR	R/W	0h	The radr0 specifies the remote SRAM address for FLC data to be copied. The SRAM must be large enough for the specified range.
11:0	RESERVED	NONE	0h	Reserved

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5.5.2.22 RL2_FLC_CTL_J Register

5.5.2.22.1 RL2_FLC_CTL_J Register (Offset = 138h) [reset = 0h]

The FLC Control 'n' enables the given range FLC_LO0>=FLCrange<FLC_HI0 to be copied to the FLC_RA0 SRAM memory.

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Table 5-1166. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2138h + formula
RL2_R5SS0_CORE1	5321 3138h + formula
RL2_R5SS1_CORE0	5321 4138h + formula
RL2_R5SS1_CORE1	5321 5138h + formula

Figure 5-576. RL2_FLC_CTL_j Name Register

31	30	29	28	27	26	25	24
FENABLE	RESERVED		FCOPIED	RESERVED			
R/W	NONE		R/W	NONE			
0h	0h		0h	0h			
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-1167. RL2_FLC_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FENABLE	R/W	0h	The fenable0 enables the FLC_LO0>=FLCrange<FLC_HI0 to be copied. if the fenable0 is set to zero, the range is disabled and commands forwarded directly without change.
30:29	RESERVED	NONE	0h	Reserved
28	FCOPIED	R/W	0h	The fcopied0 bit indicates the FLC range has already been copied to the radr0 address so a transfer is not required. Setting this bit at the same cycle or prior to setting the fenable will prevent the FLC transfer but enable the mapping.
27:0	RESERVED	NONE	0h	Reserved

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5.5.2.23 RL2_RAT_CTL_J Register

5.5.2.23.1 RL2_RAT_CTL_J Register (Offset = 220h) [reset = 0h]

The Control for Region 0

Return to Summary Table

Table 5-1168. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2220h + formula
RL2_R5SS0_CORE1	5321 3220h + formula
RL2_R5SS1_CORE0	5321 4220h + formula
RL2_R5SS1_CORE1	5321 5220h + formula

Figure 5-577. RL2_RAT_CTL_j Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>REN</td><td colspan="7">RESERVED</td></tr>
<tr><td>R/W</td><td colspan="7">NONE</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">RESERVED</td></tr>
<tr><td colspan="8">NONE</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">SIZE</td></tr>
<tr><td colspan="2">NONE</td><td colspan="6">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">0h</td></tr>
</table>

Table 5-1169. RL2_RAT_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REN	R/W	0h	Enable for the Region
30:6	RESERVED	NONE	0h	Reserved
5:0	SIZE	R/W	0h	Size of the Region in Address Bits. 0-12 = 4K byte, 13 = 8KB, 14 = 16KB, 15 = 32KB, etc. up to 32-63 = 4GB.

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5.5.2.24 RL2_RAT_RBA_J Register

5.5.2.24.1 RL2_RAT_RBA_J Register (Offset = 224h) [reset = 0h]

The Base Address for Region 0. This is the source address for matching to a region.

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Table 5-1170. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2224h + formula
RL2_R5SS0_CORE1	5321 3224h + formula
RL2_R5SS1_CORE0	5321 4224h + formula
RL2_R5SS1_CORE1	5321 5224h + formula

Figure 5-578. RL2_RAT_RBA_j Name Register

31	30	29	28	27	26	25	24
BASE							
R/W							
0h							
23	22	21	20	19	18	17	16
BASE							
R/W							
0h							
15	14	13	12	11	10	9	8
BASE							
R/W							
0h							
7	6	5	4	3	2	1	0
BASE							
R/W							
0h							

Table 5-1171. RL2_RAT_RBA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	BASE	R/W	0h	Base Address for the Region. It must be aligned to the programmed size.

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5.5.2.25 RL2_RAT_RTA_J Register

5.5.2.25.1 RL2_RAT_RTA_J Register (Offset = 228h) [reset = 0h]

The Translated Address Bits for Region 0

Return to Summary Table

Table 5-1172. Instance Table

Instance Name	Physical Address
RL2_R5SS0_CORE0	5321 2228h + formula
RL2_R5SS0_CORE1	5321 3228h + formula
RL2_R5SS1_CORE0	5321 4228h + formula
RL2_R5SS1_CORE1	5321 5228h + formula

Figure 5-579. RL2_RAT_RTA_j Name Register

31	30	29	28	27	26	25	24
TRANS							
R/W							
0h							
23	22	21	20	19	18	17	16
TRANS							
R/W							
0h							
15	14	13	12	11	10	9	8
TRANS							
R/W							
0h							
7	6	5	4	3	2	1	0
TRANS							
R/W							
0h							

Table 5-1173. RL2_RAT_RTA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TRANS	R/W	0h	Translated Address Bits for the Region. It must be aligned to the programmed size.

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5.6 FSS_TIMEOUT_CFG

FSS_TIMEOUT_CFG

5.6.1 FSS_TIMEOUT_CFG Summaries

FSS_TIMEOUT_CFG Summaries

Table 5-1174. FSS_TIMEOUT_CFG Registers, Base Address=5340 0000h, Length=1024

Offset	Length	Register Name	FSS_TIMEOUT_CFG0 Physical Address
0h	32	FSS_TIMEOUT_CFG_PID	5340 0000h
4h	32	FSS_TIMEOUT_CFG_CFG	5340 0004h
8h	32	FSS_TIMEOUT_CFG_INFO	5340 0008h
Ch	32	FSS_TIMEOUT_CFG_ENABLE	5340 000Ch
10h	32	FSS_TIMEOUT_CFG_FLUSH	5340 0010h
14h	32	FSS_TIMEOUT_CFG_TIMEOUT	5340 0014h
18h	32	FSS_TIMEOUT_CFG_TIMER	5340 0018h
20h	32	FSS_TIMEOUT_CFG_ERR_RAW	5340 0020h
24h	32	FSS_TIMEOUT_CFG_ERR	5340 0024h
28h	32	FSS_TIMEOUT_CFG_ERR_MSK_SET	5340 0028h
2Ch	32	FSS_TIMEOUT_CFG_ERR_MSK_CLR	5340 002Ch
30h	32	FSS_TIMEOUT_CFG_ERR_TM_INFO	5340 0030h
34h	32	FSS_TIMEOUT_CFG_ERR_UN_INFO	5340 0034h
38h	32	FSS_TIMEOUT_CFG_ERR_VAL	5340 0038h
3Ch	32	FSS_TIMEOUT_CFG_ERR_TAG	5340 003Ch
40h	32	FSS_TIMEOUT_CFG_ERR_BYT	5340 0040h
44h	32	FSS_TIMEOUT_CFG_ERR_ADDR_U	5340 0044h
48h	32	FSS_TIMEOUT_CFG_ERR_ADDR_L	5340 0048h

5.6.2 FSS_TIMEOUT_CFG Registers

FSS_TIMEOUT_CFG Registers

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5.6.2.1 FSS_TIMEOUT_CFG_PID Register

5.6.2.1.1 FSS_TIMEOUT_CFG_PID Register (Offset = 0h) [reset = 66067100h]

The Revision Register contains the major and minor revisions for the module.

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Table 5-1175. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0000h

Figure 5-580. FSS_TIMEOUT_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R		R		R			
1h		2h		606h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R							
606h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTL					MAJOR		
R					R		
Eh					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINOR					
R		R					
0h		0h					

Table 5-1176. FSS_TIMEOUT_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme
29:28	BU	R	2h	Business Unit: 10 = Processors
27:16	FUNC	R	606h	Module ID
15:11	RTL	R	Eh	RTL revision. Will vary depending on release.
10:8	MAJOR	R	1h	Major revision
7:6	CUSTOM	R	0h	Custom
5:0	MINOR	R	0h	Minor revision

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5.6.2.2 FSS_TIMEOUT_CFG_CFG Register

5.6.2.2.1 FSS_TIMEOUT_CFG_CFG Register (Offset = 4h) [reset = 40004h]

The Configuration Register contains information about the configuration of the gasket.

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Table 5-1177. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0004h

Figure 5-581. FSS_TIMEOUT_CFG_CFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
NUM_WRITES							
R							
4h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NUM_READS							
R							
4h							

Table 5-1178. FSS_TIMEOUT_CFG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	NONE	0h	Reserved
23:16	NUM_WRITES	R	4h	Total Number of slots in the write scoreboard
15:8	RESERVED	NONE	0h	Reserved
7:0	NUM_READS	R	4h	Total Number of slots in the read scoreboard

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5.6.2.3 FSS_TIMEOUT_CFG_INFO Register

5.6.2.3.1 FSS_TIMEOUT_CFG_INFO Register (Offset = 8h) [reset = 0h]

The Info Register contains information about the current state of the gasket.

Return to Summary Table

Table 5-1179. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0008h

Figure 5-582. FSS_TIMEOUT_CFG_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							CUR_WRITES
NONE							R
0h							0h
23	22	21	20	19	18	17	16
CUR_WRITES							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							CUR_READS
NONE							R
0h							0h
7	6	5	4	3	2	1	0
CUR_READS							
R							
0h							

Table 5-1180. FSS_TIMEOUT_CFG_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24:16	CUR_WRITES	R	0h	Current number of occupied slots in the write scoreboard
15:9	RESERVED	NONE	0h	Reserved
8:0	CUR_READS	R	0h	Current number of occupied slots in the read scoreboard

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5.6.2.4 FSS_TIMEOUT_CFG_ENABLE Register

5.6.2.4.1 FSS_TIMEOUT_CFG_ENABLE Register (Offset = Ch) [reset = 0h]

The Enable Register contains the gasket enable.

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Table 5-1181. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 000Ch

Figure 5-583. FSS_TIMEOUT_CFG_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				EN			
NONE				R/W			
0h				0h			

Table 5-1182. FSS_TIMEOUT_CFG_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:0	EN	R/W	0h	Enable. 0 - Disabled, All other values - Enabled.

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5.6.2.5 FSS_TIMEOUT_CFG_FLUSH Register

5.6.2.5.1 FSS_TIMEOUT_CFG_FLUSH Register (Offset = 10h) [reset = 0h]

The Flush Register contains software flush control.

Return to Summary Table

Table 5-1183. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0010h

Figure 5-584. FSS_TIMEOUT_CFG_FLUSH Name Register

31	30	29	28	27	26	25	24
EXT_FL	RESERVED						
R	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				FL			
NONE				R/W			
0h				0h			

Table 5-1184. FSS_TIMEOUT_CFG_FLUSH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EXT_FL	R	0h	The value of external flush input
30:4	RESERVED	NONE	0h	Reserved
3:0	FL	R/W	0h	SW control and indicator for whether the gasket is in flush mode. 4'b1111 - Flush mode, All other values - Normal mode.

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5.6.2.6 FSS_TIMEOUT_CFG_TIMEOUT Register

5.6.2.6.1 FSS_TIMEOUT_CFG_TIMEOUT Register (Offset = 14h) [reset = 3FFFFFFFh]

The Timeout Value Register contains the timeout value for scoreboarded transactions.

Return to Summary Table

Table 5-1185. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0014h

Figure 5-585. FSS_TIMEOUT_CFG_TIMEOUT Name Register

31	30	29	28	27	26	25	24
RESERVED		TO					
NONE		R/W					
0h		3FFFFFFFh					
23	22	21	20	19	18	17	16
TO							
R/W							
3FFFFFFFh							
15	14	13	12	11	10	9	8
TO							
R/W							
3FFFFFFFh							
7	6	5	4	3	2	1	0
TO							
R/W							
3FFFFFFFh							

Table 5-1186. FSS_TIMEOUT_CFG_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED	NONE	0h	Reserved
29:0	TO	R/W	3FFFFFFFh	The number of cycles in each eon. Each transaction can be outstanding for 2-3 eons before it times out.

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5.6.2.7 FSS_TIMEOUT_CFG_TIMER Register

5.6.2.7.1 FSS_TIMEOUT_CFG_TIMER Register (Offset = 18h) [reset = 0h]

The Timer Register contains the current value for free-running timer.

Return to Summary Table

Table 5-1187. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0018h

Figure 5-586. FSS_TIMEOUT_CFG_TIMER Name Register

31	30	29	28	27	26	25	24
EON		CNTR					
R		R/WTC					
0h		0h					
23	22	21	20	19	18	17	16
CNTR							
R/WTC							
0h							
15	14	13	12	11	10	9	8
CNTR							
R/WTC							
0h							
7	6	5	4	3	2	1	0
CNTR							
R/WTC							
0h							

Table 5-1188. FSS_TIMEOUT_CFG_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	EON	R	0h	Current eon
29:0	CNTR	R/WTC	0h	Current value of the free-running timer. It increments once per clock cycle when the gasket is enabled.

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5.6.2.8 FSS_TIMEOUT_CFG_ERR_RAW Register

5.6.2.8.1 FSS_TIMEOUT_CFG_ERR_RAW Register (Offset = 20h) [reset = 0h]

This register contains the masked interrupt bits.

Return to Summary Table

Table 5-1189. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0020h

Figure 5-587. FSS_TIMEOUT_CFG_ERR_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMD	UNEXP	TIMEOUT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h

Table 5-1190. FSS_TIMEOUT_CFG_ERR_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	CMD	R/W1TS	0h	Raw Command Error Interrupt
1	UNEXP	R/W1TS	0h	Raw Unexpected Error Interrupt
0	TIMEOUT	R/W1TS	0h	Raw Timeout Error Interrupt

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5.6.2.9 FSS_TIMEOUT_CFG_ERR Register

5.6.2.9.1 FSS_TIMEOUT_CFG_ERR Register (Offset = 24h) [reset = 0h]

This register contains the masked interrupt bits.

Return to Summary Table

Table 5-1191. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0024h

Figure 5-588. FSS_TIMEOUT_CFG_ERR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMD	UNEXP	TIMEOUT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					0h	0h	0h

Table 5-1192. FSS_TIMEOUT_CFG_ERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	CMD	R/W1TC	0h	Masked Command Error Interrupt
1	UNEXP	R/W1TC	0h	Masked Unexpected Error Interrupt
0	TIMEOUT	R/W1TC	0h	Masked Timeout Error Interrupt

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5.6.2.10 FSS_TIMEOUT_CFG_ERR_MSK_SET Register

5.6.2.10.1 FSS_TIMEOUT_CFG_ERR_MSK_SET Register (Offset = 28h) [reset = 7h]

This register contains interrupt mask set bits.

Return to Summary Table

Table 5-1193. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0028h

Figure 5-589. FSS_TIMEOUT_CFG_ERR_MSK_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CMD	UNEXP	TIMEOUT
NONE					R/W1TS	R/W1TS	R/W1TS
0h					1h	1h	1h

Table 5-1194. FSS_TIMEOUT_CFG_ERR_MSK_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	CMD	R/W1TS	1h	Raw Command Error Interrupt Mask Set
1	UNEXP	R/W1TS	1h	Raw Unexpected Error Interrupt Mask Set
0	TIMEOUT	R/W1TS	1h	Raw Timeout Error Interrupt Mask Set

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5.6.2.11 FSS_TIMEOUT_CFG_ERR_MSK_CLR Register

5.6.2.11.1 FSS_TIMEOUT_CFG_ERR_MSK_CLR Register (Offset = 2Ch) [reset = 7h]

This register contains interrupt mask clear bits.

Return to Summary Table

Table 5-1195. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 002Ch

Figure 5-590. FSS_TIMEOUT_CFG_ERR_MSK_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED					CMD	UNEXP	TIMEOUT
NONE					R/W1TC	R/W1TC	R/W1TC
0h					1h	1h	1h

Table 5-1196. FSS_TIMEOUT_CFG_ERR_MSK_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	NONE	0h	Reserved
2	CMD	R/W1TC	1h	Raw Command Error Interrupt Mask Clear
1	UNEXP	R/W1TC	1h	Raw Unexpected Error Interrupt Mask Clear
0	TIMEOUT	R/W1TC	1h	Raw Timeout Error Interrupt Mask Clear

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5.6.2.12 FSS_TIMEOUT_CFG_ERR_TM_INFO Register

5.6.2.12.1 FSS_TIMEOUT_CFG_ERR_TM_INFO Register (Offset = 30h) [reset = 0h]

This register contains information about timeout interrupts.

Return to Summary Table

Table 5-1197. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0030h

Figure 5-591. FSS_TIMEOUT_CFG_ERR_TM_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CNT	
NONE						R/WTD	
0h						0h	

Table 5-1198. FSS_TIMEOUT_CFG_ERR_TM_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CNT	R/WTD	0h	This field contains information about how many transactions have timed out since the last one was serviced. Writing to this register decrements the contents by the value written. The value saturates at 3.

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5.6.2.13 FSS_TIMEOUT_CFG_ERR_UN_INFO Register

5.6.2.13.1 FSS_TIMEOUT_CFG_ERR_UN_INFO Register (Offset = 34h) [reset = 0h]

This register contains information about unexpected interrupts.

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Table 5-1199. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0034h

Figure 5-592. FSS_TIMEOUT_CFG_ERR_UN_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						CNT	
NONE						R/WTD	
0h						0h	

Table 5-1200. FSS_TIMEOUT_CFG_ERR_UN_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	CNT	R/WTD	0h	This field contains information about how many unexpected responses have been received since the last one was serviced. Writing to this register decrements the contents by the value written. The value saturates at 3.

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5.6.2.14 FSS_TIMEOUT_CFG_ERR_VAL Register

5.6.2.14.1 FSS_TIMEOUT_CFG_ERR_VAL Register (Offset = 38h) [reset = 0h]

This register contains information about transaction that caused the interrupt.

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Table 5-1201. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0038h

Figure 5-593. FSS_TIMEOUT_CFG_ERR_VAL Name Register

31	30	29	28	27	26	25	24
RESERVED				RID			
NONE				R			
0h				0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				OID			
NONE				R			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DIR	TYP	VAL
NONE					R	R	R
0h					0h	0h	0h

Table 5-1202. FSS_TIMEOUT_CFG_ERR_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	RID	R	0h	Route ID Indicator
15:12	RESERVED	NONE	0h	Reserved
11:8	OID	R	0h	Order ID Indicator
7:3	RESERVED	NONE	0h	Reserved
2	DIR	R	0h	Direction Indicator. 0-write. 1-read.
1	TYP	R	0h	Error Type Indicator. 0-transaction timeout. 1-unexpected response.
0	VAL	R	0h	Valid Indicator. If this field is a 1, then the contents of this and the below registers is considered valid: it contains the information about the transaction that was captured. If this field is 0 then this and the other listed registers are not valid.

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5.6.2.15 FSS_TIMEOUT_CFG_ERR_TAG Register

5.6.2.15.1 FSS_TIMEOUT_CFG_ERR_TAG Register (Offset = 3Ch) [reset = 0h]

This register contains information about transaction that caused the interrupt.

Return to Summary Table

Table 5-1203. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 003Ch

Figure 5-594. FSS_TIMEOUT_CFG_ERR_TAG Name Register

31	30	29	28	27	26	25	24
RESERVED				TAG			
NONE				R			
0h				0h			

23	22	21	20	19	18	17	16
TAG							
R							
0h							

15	14	13	12	11	10	9	8
RESERVED				CID			
NONE				R			
0h				0h			

7	6	5	4	3	2	1	0
CID							
R							
0h							

Table 5-1204. FSS_TIMEOUT_CFG_ERR_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED	NONE	0h	Reserved
27:16	TAG	R	0h	Command Tag Indicator consisting of replacement CID for timeout error, or SID/RID for unexpected response error.
15:12	RESERVED	NONE	0h	Reserved
11:0	CID	R	0h	Command ID Indicator. This is the original command id and is only valid on timeout error.

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5.6.2.16 FSS_TIMEOUT_CFG_ERR_BYT Register

5.6.2.16.1 FSS_TIMEOUT_CFG_ERR_BYT Register (Offset = 40h) [reset = 0h]

This register contains information about transaction that caused the interrupt.

Return to Summary Table

Table 5-1205. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0040h

Figure 5-595. FSS_TIMEOUT_CFG_ERR_BYT Name Register

31	30	29	28	27	26	25	24
RESERVED						CBYTECNT	
NONE						R	
0h						0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CBYTECNT							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED						OBYTECNT	
NONE						R	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OBYTECNT							
R							
0h							

Table 5-1206. FSS_TIMEOUT_CFG_ERR_BYT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED	NONE	0h	Reserved
25:16	CBYTECNT	R	0h	Current Bytecnt. For timeout error this is the number of bytes that were not returned.
15:10	RESERVED	NONE	0h	Reserved
9:0	OBYTECNT	R	0h	Original Bytecnt. This field represents the transaction cbytecnt of the original command.

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5.6.2.17 FSS_TIMEOUT_CFG_ERR_ADDR_U Register

5.6.2.17.1 FSS_TIMEOUT_CFG_ERR_ADDR_U Register (Offset = 44h) [reset = 0h]

This register contains information about transaction that caused the interrupt.

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Table 5-1207. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0044h

Figure 5-596. FSS_TIMEOUT_CFG_ERR_ADDR_U Name Register

31	30	29	28	27	26	25	24
ADDR							
R							
0h							
23	22	21	20	19	18	17	16
ADDR							
R							
0h							
15	14	13	12	11	10	9	8
ADDR							
R							
0h							
7	6	5	4	3	2	1	0
ADDR							
R							
0h							

Table 5-1208. FSS_TIMEOUT_CFG_ERR_ADDR_U Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR	R	0h	Upper bits of the address for the captured transaction. This is field is only valid for timeout error.

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5.6.2.18 FSS_TIMEOUT_CFG_ERR_ADDR_L Register

5.6.2.18.1 FSS_TIMEOUT_CFG_ERR_ADDR_L Register (Offset = 48h) [reset = 0h]

This register contains information about transaction that caused the interrupt.

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Table 5-1209. Instance Table

Instance Name	Physical Address
FSS_TIMEOUT_CFG0	5340 0048h

Figure 5-597. FSS_TIMEOUT_CFG_ERR_ADDR_L Name Register

31	30	29	28	27	26	25	24
ADDR							
R							
0h							
23	22	21	20	19	18	17	16
ADDR							
R							
0h							
15	14	13	12	11	10	9	8
ADDR							
R							
0h							
7	6	5	4	3	2	1	0
ADDR							
R							
0h							

Table 5-1210. FSS_TIMEOUT_CFG_ERR_ADDR_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR	R	0h	Lower bits of the address for the captured transaction. This is field is only valid for timeout error. If the address width is less than 32, then the bits above the address range will be read as 0.

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5.7 FSS

FSS

5.7.1 FSS Summaries

FSS Summaries

Table 5-1211. FSS_GENREGS Registers, Base Address=5380 0000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSS_GENREGS_REVISION	5380 0000h

Table 5-1212. FSS_FSAS_GENREGS Registers, Base Address=5380 1000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSS_FSAS_GENREGS_REVISION	5380 1000h
4h	32	FSS_FSAS_GENREGS_SYSCONFIG	5380 1004h
80h	32	FSS_FSAS_GENREGS_DP_ERR_INJ_CTRL	5380 1080h
10h	32	FSS_FSAS_GENREGS_IRQ_IRQ_EOI	5380 1010h + formula
14h	32	FSS_FSAS_GENREGS_IRQ_IRQ_STATUS_RAW	5380 1014h + formula
18h	32	FSS_FSAS_GENREGS_IRQ_IRQ_STATUS	5380 1018h + formula
1Ch	32	FSS_FSAS_GENREGS_IRQ_IRQ_ENABLE_SET	5380 101Ch + formula
20h	32	FSS_FSAS_GENREGS_IRQ_IRQ_ENABLE_CLR	5380 1020h + formula
30h	32	FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J	5380 1030h + formula
34h	32	FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J	5380 1034h + formula
70h	32	FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR	5380 1070h + formula
74h	32	FSS_FSAS_GENREGS_ERR_ECC_TYPE	5380 1074h + formula
78h	32	FSS_FSAS_GENREGS_ERR_WRT_TYPE	5380 1078h + formula

Table 5-1213. FSAS_OTFA_REGS Registers, Base Address=5380 2000h, Length=4096

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSAS_OTFA_REGS_REVID	5380 2000h
4h	32	FSAS_OTFA_REGS_SCFG	5380 2004h
8h	32	FSAS_OTFA_REGS_ISR	5380 2008h
Ch	32	FSAS_OTFA_REGS_IS	5380 200Ch
10h	32	FSAS_OTFA_REGS_IES	5380 2010h
14h	32	FSAS_OTFA_REGS_IEC	5380 2014h
18h	32	FSAS_OTFA_REGS_CCFG	5380 2018h
1Ch	32	FSAS_OTFA_REGS_CSTATUS	5380 201Ch
220h	32	FSAS_OTFA_REGS_IRQADDINFO0	5380 2220h
224h	32	FSAS_OTFA_REGS_IRQADDINFO1	5380 2224h
228h	32	FSAS_OTFA_REGS_MACCACHEINFO	5380 2228h
22Ch	32	FSAS_OTFA_REGS_RMWRMCNT	5380 222Ch
20h	32	FSAS_OTFA_REGS_RG_RGCFG_J	5380 2020h + formula
24h	32	FSAS_OTFA_REGS_RG_RGMACST_J	5380 2024h + formula
28h	32	FSAS_OTFA_REGS_RG_RGST_J	5380 2028h + formula
2Ch	32	FSAS_OTFA_REGS_RG_RGSI_J	5380 202Ch + formula
30h	32	FSAS_OTFA_REGS_RG_RKEYE_J_K	5380 2030h + formula
50h	32	FSAS_OTFA_REGS_RG_RKEYEP_J_K	5380 2050h + formula

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Table 5-1213. FSAS_OTFA_REGS Registers, Base Address=5380 2000h, Length=4096 (continued)

Offset	Length	Register Name	FSS0 Physical Address
70h	32	FSAS_OTFA_REGS_RG_RKEYA_J_K	5380 2070h + formula
80h	32	FSAS_OTFA_REGS_RG_RKEYAP_J_K	5380 2080h + formula
90h	32	FSAS_OTFA_REGS_RG_RIV_J_K	5380 2090h + formula

Table 5-1214. OSPI_CFG Registers, Base Address=5380 6000h, Length=512

Offset	Length	Register Name	FSS0 Physical Address
0h	32	OSPI_CFG_PID	5380 6000h
8h	32	OSPI_CFG_STAT	5380 6008h
20h	32	OSPI_CFG_EOI	5380 6020h

Table 5-1215. OSPI0_ECC_AGGR Registers, Base Address=5380 7000h, Length=1024

Offset	Length	Register Name	FSS0 Physical Address
0h	32	OSPI0_ECC_AGGR_REV	5380 7000h
8h	32	OSPI0_ECC_AGGR_VECTOR	5380 7008h
Ch	32	OSPI0_ECC_AGGR_STAT	5380 700Ch
10h	32	OSPI0_ECC_AGGR_RESERVED_SVBUS_J	5380 7010h + formula
3Ch	32	OSPI0_ECC_AGGR_SEC_EOI_REG	5380 703Ch
40h	32	OSPI0_ECC_AGGR_SEC_STATUS_REG0	5380 7040h
80h	32	OSPI0_ECC_AGGR_SEC_ENABLE_SET_REG0	5380 7080h
C0h	32	OSPI0_ECC_AGGR_SEC_ENABLE_CLR_REG0	5380 70C0h
13Ch	32	OSPI0_ECC_AGGR_DED_EOI_REG	5380 713Ch
140h	32	OSPI0_ECC_AGGR_DED_STATUS_REG0	5380 7140h
180h	32	OSPI0_ECC_AGGR_DED_ENABLE_SET_REG0	5380 7180h
1C0h	32	OSPI0_ECC_AGGR_DED_ENABLE_CLR_REG0	5380 71C0h
200h	32	OSPI0_ECC_AGGR_AGGR_ENABLE_SET	5380 7200h
204h	32	OSPI0_ECC_AGGR_AGGR_ENABLE_CLR	5380 7204h
208h	32	OSPI0_ECC_AGGR_AGGR_STATUS_SET	5380 7208h
20Ch	32	OSPI0_ECC_AGGR_AGGR_STATUS_CLR	5380 720Ch

Table 5-1216. OSPI_FLASH_CFG Registers, Base Address=5380 8000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	OSPI_FLASH_CFG_CONFIG_REG	5380 8000h
4h	32	OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG	5380 8004h
8h	32	OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG	5380 8008h
Ch	32	OSPI_FLASH_CFG_DEV_DELAY_REG	5380 800Ch
10h	32	OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG	5380 8010h
14h	32	OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG	5380 8014h
18h	32	OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG	5380 8018h
1Ch	32	OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG	5380 801Ch
24h	32	OSPI_FLASH_CFG_REMAP_ADDR_REG	5380 8024h
28h	32	OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG	5380 8028h
2Ch	32	OSPI_FLASH_CFG_SRAM_FILL_REG	5380 802Ch
30h	32	OSPI_FLASH_CFG_TX_THRESH_REG	5380 8030h
34h	32	OSPI_FLASH_CFG_RX_THRESH_REG	5380 8034h
38h	32	OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG	5380 8038h

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Table 5-1216. OSPI_FLASH_CFG Registers, Base Address=5380 8000h, Length=256 (continued)

Offset	Length	Register Name	FSS0 Physical Address
3Ch	32	OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG	5380 803Ch
40h	32	OSPI_FLASH_CFG_IRQ_STATUS_REG	5380 8040h
44h	32	OSPI_FLASH_CFG_IRQ_MASK_REG	5380 8044h
50h	32	OSPI_FLASH_CFG_LOWER_WR_PROT_REG	5380 8050h
54h	32	OSPI_FLASH_CFG_UPPER_WR_PROT_REG	5380 8054h
58h	32	OSPI_FLASH_CFG_WR_PROT_CTRL_REG	5380 8058h
60h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG	5380 8060h
64h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG	5380 8064h
68h	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG	5380 8068h
6Ch	32	OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG	5380 806Ch
70h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG	5380 8070h
74h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG	5380 8074h
78h	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG	5380 8078h
7Ch	32	OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG	5380 807Ch
80h	32	OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG	5380 8080h
8Ch	32	OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG	5380 808Ch
90h	32	OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG	5380 8090h
94h	32	OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG	5380 8094h
A0h	32	OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG	5380 80A0h
A4h	32	OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG	5380 80A4h
A8h	32	OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG	5380 80A8h
ACh	32	OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG	5380 80ACh
B0h	32	OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG	5380 80B0h
B4h	32	OSPI_FLASH_CFG_PHY_CONFIGURATION_REG	5380 80B4h
B8h	32	OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG	5380 80B8h
BCh	32	OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG	5380 80BCh
C0h	32	OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG	5380 80C0h
E0h	32	OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG	5380 80E0h
E4h	32	OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG	5380 80E4h
FCh	32	OSPI_FLASH_CFG_MODULE_ID_REG	5380 80FCh

Table 5-1217. FOTA_GENREGS Registers, Base Address=5380 B000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FOTA_GENREGS_FOTA_INIT	5380 B000h
4h	32	FOTA_GENREGS_FOTA_CTRL	5380 B004h
8h	32	FOTA_GENREGS_FOTA_ERR_INFO	5380 B008h
10h	32	FOTA_GENREGS_FOTA_GP0	5380 B010h
14h	32	FOTA_GENREGS_FOTA_GP1	5380 B014h
18h	32	FOTA_GENREGS_FOTA_ADDR	5380 B018h
1Ch	32	FOTA_GENREGS_FOTA_CNT	5380 B01Ch

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Table 5-1217. FOTA_GENREGS Registers, Base Address=5380 B000h, Length=256 (continued)

Offset	Length	Register Name	FSS0 Physical Address
20h	32	FOTA_GENREGS_STS_IRQ_IRQ_EOI	5380 B020h + formula
24h	32	FOTA_GENREGS_STS_IRQ_IRQ_STATUS_RAW	5380 B024h + formula
28h	32	FOTA_GENREGS_STS_IRQ_IRQ_STATUS	5380 B028h + formula
2Ch	32	FOTA_GENREGS_STS_IRQ_IRQ_ENABLE_SET	5380 B02Ch + formula
30h	32	FOTA_GENREGS_STS_IRQ_IRQ_ENABLE_CLR	5380 B030h + formula
40h	32	FOTA_GENREGS_ERR_STS_IRQ_IRQ_EOI	5380 B040h + formula
44h	32	FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS_RAW	5380 B044h + formula
48h	32	FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS	5380 B048h + formula
4Ch	32	FOTA_GENREGS_ERR_STS_IRQ_IRQ_ENABLE_SET	5380 B04Ch + formula
50h	32	FOTA_GENREGS_ERR_STS_IRQ_IRQ_ENABLE_CLR	5380 B050h + formula

Table 5-1218. PDMEM_GENREGS Registers, Base Address=5380 C000h, Length=2048

Offset	Length	Register Name	FSS0 Physical Address
0h	32	PDMEM_GENREGS_LOC_J	5380 C000h + formula

Table 5-1219. IMEM_GENREGS Registers, Base Address=5380 D000h, Length=256

Offset	Length	Register Name	FSS0 Physical Address
0h	32	IMEM_GENREGS_LOC_J	5380 D000h + formula

Table 5-1220. WBUF_GENREGS Registers, Base Address=5380 E000h, Length=512

Offset	Length	Register Name	FSS0 Physical Address
0h	32	WBUF_GENREGS_LOC_J	5380 E000h + formula

Table 5-1221. FSAS_ECC_AGGR Registers, Base Address=5380 F000h, Length=1024

Offset	Length	Register Name	FSS0 Physical Address
0h	32	FSAS_ECC_AGGR_REV	5380 F000h
8h	32	FSAS_ECC_AGGR_VECTOR	5380 F008h
Ch	32	FSAS_ECC_AGGR_STAT	5380 F00Ch
10h	32	FSAS_ECC_AGGR_RESERVED_SVBUS_J	5380 F010h + formula
3Ch	32	FSAS_ECC_AGGR_SEC_EOI_REG	5380 F03Ch
40h	32	FSAS_ECC_AGGR_SEC_STATUS_REG0	5380 F040h
80h	32	FSAS_ECC_AGGR_SEC_ENABLE_SET_REG0	5380 F080h
C0h	32	FSAS_ECC_AGGR_SEC_ENABLE_CLR_REG0	5380 F0C0h
13Ch	32	FSAS_ECC_AGGR_DED_EOI_REG	5380 F13Ch
140h	32	FSAS_ECC_AGGR_DED_STATUS_REG0	5380 F140h
180h	32	FSAS_ECC_AGGR_DED_ENABLE_SET_REG0	5380 F180h
1C0h	32	FSAS_ECC_AGGR_DED_ENABLE_CLR_REG0	5380 F1C0h
200h	32	FSAS_ECC_AGGR_AGGR_ENABLE_SET	5380 F200h
204h	32	FSAS_ECC_AGGR_AGGR_ENABLE_CLR	5380 F204h
208h	32	FSAS_ECC_AGGR_AGGR_STATUS_SET	5380 F208h
20Ch	32	FSAS_ECC_AGGR_AGGR_STATUS_CLR	5380 F20Ch

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Table 5-1222. DATA_REG0 Registers, Base Address=6000 0000h, Length=134217728

Offset	Length	Register Name	FSS0 Physical Address
0h	32	DATA_REG0_HPB_DATA_MEM_J	6000 0000h + formula

Table 5-1223. DATA_REG1 Registers, Base Address=8000 0000h, Length=134217728

Offset	Length	Register Name	FSS0 Physical Address
0h	32	DATA_REG1_HPB_DATA_MEM_J	8000 0000h + formula

Table 5-1224. DATA_REG3 Registers, Base Address=8800 0000h, Length=134217728

Offset	Length	Register Name	FSS0 Physical Address
0h	32	DATA_REG3_HPB_DATA_MEM_J	8800 0000h + formula

5.7.2 FSS Registers

FSS Registers

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5.7.2.1 FSS_GENREGS_REVISION Register

5.7.2.1.1 FSS_GENREGS_REVISION Register (Offset = 0h) [reset = 68502200h]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility.

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Table 5-1225. Instance Table

Instance Name	Physical Address
FSS0	5380 0000h

Figure 5-598. FSS_GENREGS_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
6850h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODID							
R							
6850h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
4h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 5-1226. FSS_GENREGS_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6850h	Module ID field
15:11	REVRTL	R	4h	RTL revision. Will vary depending on release.
10:8	REVMAJ	R	2h	Major revision
7:6	CUSTOM	R	0h	Custom
5:0	REVMIN	R	0h	Minor revision

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5.7.2.2 FSS_FSAS_GENREGS_REVISION Register

5.7.2.2.1 FSS_FSAS_GENREGS_REVISION Register (Offset = 0h) [reset = 68502200h]

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility.

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Table 5-1227. Instance Table

Instance Name	Physical Address
FSS0	5380 1000h

Figure 5-599. FSS_FSAS_GENREGS_REVISION Name Register

31	30	29	28	27	26	25	24
MODID							
R							
6850h							
23	22	21	20	19	18	17	16
MODID							
R							
6850h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
4h					2h		
7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 5-1228. FSS_FSAS_GENREGS_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	MODID	R	6850h	Module ID field
15:11	REVRTL	R	4h	RTL revision. Will vary depending on release.
10:8	REVMAJ	R	2h	Major revision
7:6	CUSTOM	R	0h	Custom
5:0	REVMIN	R	0h	Minor revision

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5.7.2.3 FSS_FSAS_GENREGS_SYSCONFIG Register

5.7.2.3.1 FSS_FSAS_GENREGS_SYSCONFIG Register (Offset = 4h) [reset = 5000h]

Controls various parameters of the cotroller state.

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Table 5-1229. Instance Table

Instance Name	Physical Address
FSS0	5380 1004h

Figure 5-600. FSS_FSAS_GENREGS_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED					HW_RW_DELAY_COUNT		
NONE					R/W		
0h					Ah		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HW_RW_DELAY_COUNT					HW_RW_DELAY_EN	DP_EN	OSPI_32B_DISABLE_MODE
R/W					R/W	R/W	R/W
Ah					0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DISXIP	OSPI_DDR_DISABLE_MODE	RESERVED		ECC_DISABLE_ADR	FSS_AES_EN_IPCFG	RESERVED	ECC_EN
R/W	R/W	NONE		R/W	R	NONE	R/W
0h	0h	0h		0h	0h	0h	0h

Table 5-1230. FSS_FSAS_GENREGS_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED	NONE	0h	Reserved
18:11	HW_RW_DELAY_COUNT	R/W	Ah	Delay for switching between reads and writes
10	HW_RW_DELAY_EN	R/W	0h	Enable delay when switching between reads and writes to avoid read-write collision for sensitive logic.
9	DP_EN	R/W	0h	0 Safety double pumping disabled. 1 Safety double pumping enabled
8	OSPI_32B_DISABLE_MODE	R/W	0h	0 OSPI 32bit mode enabled. 1 OSPI 32bit mode disabled
7	DISXIP	R/W	0h	This field is used to disable XIP prefetching. 0 XIP Prefetch Enabled. 1 XIP prefetch disabled Please note that this is referring to prefetching feature that is useful for linear accesses associated with XIP. This is NOT referring to XIP features implemented in flash Controller or memory device.
6	OSPI_DDR_DISABLE_MODE	R/W	0h	0 OSPI DDR mode enabled. 1 OSPI DDR mode disabled
5:4	RESERVED	NONE	0h	Reserved
3	ECC_DISABLE_ADR	R/W	0h	0 Block address within ECC calculation, 1 Block address not within ECC calculation
2	FSS_AES_EN_IPCFG	R	0h	1 select security, 0 disable security
1	RESERVED	NONE	0h	Reserved
0	ECC_EN	R/W	0h	0 ECC disabled. 1 ECC enabled

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5.7.2.4 FSS_FSAS_GENREGS_DP_ERR_INJ_CTRL Register

5.7.2.4.1 FSS_FSAS_GENREGS_DP_ERR_INJ_CTRL Register (Offset = 80h) [reset = 0h]

This register is used to setup double pumping error injection. Only one error injection enable field has to be set in this register at a given time. After error injection is enabled, a read must be issued to a valid flash address in order to trigger the error. Once triggered, the error will be reported using IRQ.STATUS register dp_cmd_err/dp_ret_err fields and corresponding interrupt fsas_ecc_intr_err_pend/fsas_ecc_intr_err_req will be generated if enabled.

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Table 5-1231. Instance Table

Instance Name	Physical Address
FSS0	5380 1080h

Figure 5-601. FSS_FSAS_GENREGS_DP_ERR_INJ_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BIT_SEL							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			RET_NFIRST_LAST	EN_DUPL_RET	EN_ORIG_RET	EN_DUPL_CMD	EN_ORIG_CMD
NONE			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 5-1232. FSS_FSAS_GENREGS_DP_ERR_INJ_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:8	BIT_SEL	R/W	0h	Bit select for injecting error on command or read return fields. For command error, only 0 through 47 are valid values for bit select. For read return error, only 0 through 166 are valid values for bit select.
7:5	RESERVED	NONE	0h	Reserved
4	RET_NFIRST_LAST	R/W	0h	1'b0 - Inject on first read return phase, 1'b1 - Inject on last read return phase
3	EN_DUPL_RET	R/W	0h	Enable error injection on duplicate read return fields.
2	EN_ORIG_RET	R/W	0h	Enable error injection on original read return fields.
1	EN_DUPL_CMD	R/W	0h	Enable error injection on duplicate command fields.
0	EN_ORIG_CMD	R/W	0h	Enable error injection on original command fields.

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5.7.2.5 FSS_FSAS_GENREGS_IRQ_IRQ_EOI Register

5.7.2.5.1 FSS_FSAS_GENREGS_IRQ_IRQ_EOI Register (Offset = 10h) [reset = 0h]

The End of Interrupt (EOI) Register allows the CPU to acknowledge completion of fsas_ecc_intr_err_req pulse interrupt. When this register is written to 1'b0, INTD logic used for converting fsas_ecc_intr_err_pend level interrupt to pulse will be re-armed. That is, if interrupt sources remain after writing this register to 1'b0, another pulse interrupt will be triggered by INTD. Conversely, if this register is not written to 1'b0 after fsas_ecc_intr_err_req pulse interrupt is received, then another pulse interrupt will not be received as INTD has not been re-armed. This register will be reset one cycle after it has been written to. Please note that the reason for writing 1'b0 is because there is only one interrupt (no interrupt aggregation) associated with this EOI and the INTD vector associated with this interrupt is 1'b0.

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Table 5-1233. Instance Table

Instance Name	Physical Address
FSS0	5380 1010h + formula

Figure 5-602. FSS_FSAS_GENREGS_IRQ_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_VECTOR
NONE							W
0h							0h

Table 5-1234. FSS_FSAS_GENREGS_IRQ_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	W	0h	Write 1'b0 to acknowledge fsas_ecc_intr_err_req pulse interrupt.

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5.7.2.6 FSS_FSAS_GENREGS_IRQ_IRQ_STATUS_RAW Register

5.7.2.6.1 FSS_FSAS_GENREGS_IRQ_IRQ_STATUS_RAW Register (Offset = 14h) [reset = 0h]

The IRQ_STATUS_RAW register allows the interrupt sources associated with each bit in this register to be manually set when writing a 1 to a specific bit. This register corresponds to fsas_ecc_intr_err_pend (level) and fsas_ecc_intr_err_req (pulse) interrupt outputs. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 5-1235. Instance Table

Instance Name	Physical Address
FSS0	5380 1014h + formula

Figure 5-603. FSS_FSAS_GENREGS_IRQ_IRQ_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DP_RET_ERROR	DP_CMD_ERROR	ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 5-1236. FSS_FSAS_GENREGS_IRQ_IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	DP_RET_ERROR	R/W1TS	0h	Safety double pumping read return error
3	DP_CMD_ERROR	R/W1TS	0h	Safety double pumping command error
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B
1	ECC_ERROR_2BIT	R/W1TS	0h	An ECC error occurred on 2 bits and was not correctable
0	ECC_ERROR_1BIT	R/W1TS	0h	An ECC error occurred on only 1 bit and was corrected

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5.7.2.7 FSS_FSAS_GENREGS_IRQ_IRQ_STATUS Register

5.7.2.7.1 FSS_FSAS_GENREGS_IRQ_IRQ_STATUS Register (Offset = 18h) [reset = 0h]

The IRQ_STATUS register allows the interrupt sources associated with each bit in this register to be manually cleared when writing a 1 to a specific bit. This register corresponds to fsas_ecc_intr_err_pend (level) and fsas_ecc_intr_err_req (pulse) interrupt outputs. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 5-1237. Instance Table

Instance Name	Physical Address
FSS0	5380 1018h + formula

Figure 5-604. FSS_FSAS_GENREGS_IRQ_IRQ_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DP_RET_ERROR	DP_CMD_ERROR	ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 5-1238. FSS_FSAS_GENREGS_IRQ_IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	DP_RET_ERROR	R/W1TC	0h	Safety double pumping read return error
3	DP_CMD_ERROR	R/W1TC	0h	Safety double pumping command error
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B
1	ECC_ERROR_2BIT	R/W1TC	0h	An ECC error on 2 bits. Not correctable
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. corrected

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5.7.2.8 FSS_FSAS_GENREGS_IRQ_IRQ_ENABLE_SET Register

5.7.2.8.1 FSS_FSAS_GENREGS_IRQ_IRQ_ENABLE_SET Register (Offset = 1Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the interrupt sources associated with each bit in this register to be manually enabled when writing a 1 to a specific bit. This register corresponds to fsas_ecc_intr_err_pend (level) and fsas_ecc_intr_err_req (pulse) interrupt outputs. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

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Table 5-1239. Instance Table

Instance Name	Physical Address
FSS0	5380 101Ch + formula

Figure 5-605. FSS_FSAS_GENREGS_IRQ_IRQ_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DP_RET_ERROR	DP_CMD_ERROR	ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE			R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h			0h	0h	0h	0h	0h

Table 5-1240. FSS_FSAS_GENREGS_IRQ_IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	DP_RET_ERROR	R/W1TS	0h	Safety double pumping read return error
3	DP_CMD_ERROR	R/W1TS	0h	Safety double pumping command error
2	ECC_WRITE_NONALIGN	R/W1TS	0h	Write is not aligned to 32B boundary or not a multiple of 32B
1	ECC_ERROR_2BIT	R/W1TS	0h	ECC error on 2 bits. Not correctable
0	ECC_ERROR_1BIT	R/W1TS	0h	ECC error on 1 bits. corrected

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5.7.2.9 FSS_FSAS_GENREGS_IRQ_IRQ_ENABLE_CLR Register

5.7.2.9.1 FSS_FSAS_GENREGS_IRQ_IRQ_ENABLE_CLR Register (Offset = 20h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the interrupt sources associated with each bit in this register to be manually disabled when writing a 1 to a specific bit. This register corresponds to fsas_ecc_intr_err_pend (level) and fsas_ecc_intr_err_req (pulse) interrupt outputs. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 5-1241. Instance Table

Instance Name	Physical Address
FSS0	5380 1020h + formula

Figure 5-606. FSS_FSAS_GENREGS_IRQ_IRQ_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			DP_RET_ERROR	DP_CMD_ERROR	ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h

Table 5-1242. FSS_FSAS_GENREGS_IRQ_IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	DP_RET_ERROR	R/W1TC	0h	Safety double pumping read return error
3	DP_CMD_ERROR	R/W1TC	0h	Safety double pumping command error
2	ECC_WRITE_NONALIGN	R/W1TC	0h	Write is not aligned to 32B boundary or not a multiple of 32B
1	ECC_ERROR_2BIT	R/W1TC	0h	ECC error on 2 bits. Not correctable
0	ECC_ERROR_1BIT	R/W1TC	0h	ECC error on 1 bits. corrected

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5.7.2.10 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J Register

5.7.2.10.1 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_J Register (Offset = 30h) [reset = 0h]

This defines the start of the ECC region in 4KBytes steps.

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Table 5-1243. Instance Table

Instance Name	Physical Address
FSS0	5380 1030h + formula

Figure 5-607. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START							
R/W							
0h							

Table 5-1244. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSTRT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START	R/W	0h	This defines the start of the ECC region in 4KBytes steps. Address start = {start[19:0], 0x000} 0x0 means the start is 0x0000_0000 0x1 means the start is 0x0000_1000 0xA means the start is 0x0000_A000 Note the offset + size should be <= 4GBytes, wrap around is not supported.

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5.7.2.11 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J Register

5.7.2.11.1 FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_J Register (Offset = 34h) [reset = 0h]

This defines the size of the ECC region in 4KBytes steps.

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Table 5-1245. Instance Table

Instance Name	Physical Address
FSS0	5380 1034h + formula

Figure 5-608. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_SIZE			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_SIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
R_SIZE							
R/W							
0h							

Table 5-1246. FSS_FSAS_GENREGS_ECC_REGCTRL_ECC_RGSIZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE	R/W	0h	This defines the size of the ECC region in 4KBytes steps 0x0 means the size is zero and disabled 0x1 means the size is 4KBytes 0xA means the size is 40KBytes 0xF_FFFF means the size is 4GBytes Note the offset + size should be <= 4GBytes, wrap around is not supported.

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5.7.2.12 FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register

5.7.2.12.1 FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register (Offset = 70h) [reset = 0h]

The ERR_ECC_BLOCK_ADR register holds the current top of stack ECC error block address, this is only valid when the ecc_err_valid is set

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Table 5-1247. Instance Table

Instance Name	Physical Address
FSS0	5380 1070h + formula

Figure 5-609. FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Name Register

31	30	29	28	27	26	25	24
ECC_ERROR_BLOCK_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
ECC_ERROR_BLOCK_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
ECC_ERROR_BLOCK_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
ECC_ERROR_BLOCK_ADDR			RESERVED				
R			NONE				
0h			0h				

Table 5-1248. FSS_FSAS_GENREGS_ERR_ECC_BLOCK_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	ECC_ERROR_BLOCK_ADDR	R	0h	ECC 32 byte aligned block address
4:0	RESERVED	NONE	0h	Reserved

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5.7.2.13 FSS_FSAS_GENREGS_ERR_ECC_TYPE Register

5.7.2.13.1 FSS_FSAS_GENREGS_ERR_ECC_TYPE Register (Offset = 74h) [reset = 0h]

The ERR_ECC_TYPE register holds the current top of stack ECC error info, this is only valid when the ecc_err_valid is set

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Table 5-1249. Instance Table

Instance Name	Physical Address
FSS0	5380 1074h + formula

Figure 5-610. FSS_FSAS_GENREGS_ERR_ECC_TYPE Name Register

31	30	29	28	27	26	25	24
ECC_ERR_VALID	RESERVED						
R/W1TC	NONE						
0h	0h						
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		ECC_ERR_ADR	ECC_ERR_MAC	ECC_ERR_DA1	ECC_ERR_DA0	ECC_ERR_DED	ECC_ERR_SEC
NONE		R	R	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 5-1250. FSS_FSAS_GENREGS_ERR_ECC_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_ERR_VALID	R/W1TC	0h	When set indicates that there is valid ECC error information available, Writing a one to this register will pop the top of the stack
30:6	RESERVED	NONE	0h	Reserved
5	ECC_ERR_ADR	R	0h	When set indicates that there was a single error detected within the address field. Bits 0 and 1 in this register indicate whether it is single or double error.
4	ECC_ERR_MAC	R	0h	When set indicates that there was a single error detected within the MAC field. Bits 0 and 1 in this register indicate whether it is single or double error.
3	ECC_ERR_DA1	R	0h	When set indicates that there was a single error detected within the High Data word, which is bits 127 through 64 of the data word. Bits 0 and 1 in this register indicate whether it is single or double error.
2	ECC_ERR_DA0	R	0h	When set indicates that there was a single error detected within the Low Data word, which is bits 63 through 0 of the data word. Bits 0 and 1 in this register indicate whether it is single or double error.
1	ECC_ERR_DED	R	0h	When set indicates that there was a double error detected for the block

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Table 5-1250. FSS_FSAS_GENREGS_ERR_ECC_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECC_ERR_SEC	R	0h	When set indicates that there was a single error detected for the block. The fields that had single error are reported by bits 2 through 5 in this register. It is possible that single error is reported in multiple fields since the ECCM inputs are partitioned into four partitions and ECC code is separate for each partition. It is also possible that none of the fields report single error even though ecc_err_sec bit is set. This can happen if single bit error occurred on the ECC code.

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5.7.2.14 FSS_FSAS_GENREGS_ERR_WRT_TYPE Register

5.7.2.14.1 FSS_FSAS_GENREGS_ERR_WRT_TYPE Register (Offset = 78h) [reset = 0h]

The ERR_WRT_TYPE register holds the current top of stack write error info. this is only valid when the wrt_err_valid is set

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Table 5-1251. Instance Table

Instance Name	Physical Address
FSS0	5380 1078h + formula

Figure 5-611. FSS_FSAS_GENREGS_ERR_WRT_TYPE Name Register

31	30	29	28	27	26	25	24
WRT_ERR_VALID	RESERVED						
R/W1TC	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRT_ERR_BEN	WRT_ERR_ADR	WRT_ERR_ROUTEID			
NONE		R	R	R			
0h		0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WRT_ERR_ROUTEID							
R							
0h							

Table 5-1252. FSS_FSAS_GENREGS_ERR_WRT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRT_ERR_VALID	R/W1TC	0h	When set indicates that there is valid write error information available, Writing a one to this register will pop the top of the stack
30:14	RESERVED	NONE	0h	Reserved
13	WRT_ERR_BEN	R	0h	When set indicates that there was a write error due to a non-contiguous byte enables or because write byte count was not 32-byte multiple. Please note that this bit will always be set when wrt_err_valid bit is set. There is no write error if byte count is 32-byte multiple and if byte-enables are all set.
12	WRT_ERR_ADR	R	0h	When set indicates that there was a write error due to a non-aligned address. Please note that this bit can only be set if address was 16-byte multiple but not 32-byte multiple. For example, an address of 0x10 or 0x30 for writes will cause this bit to get set.
11:0	WRT_ERR_ROUTEID	R	0h	Indicates the Route ID for the Master that caused the write error

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5.7.2.15 FSAS_OTFA_REGS_REVID Register

5.7.2.15.1 FSAS_OTFA_REGS_REVID Register (Offset = 0h) [reset = 47500101h]

This register defines the revision and functional ID.

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Table 5-1253. Instance Table

Instance Name	Physical Address
FSS0	5380 2000h

Figure 5-612. FSAS_OTFA_REGS_REVID Name Register

31	30	29	28	27	26	25	24
REVID							
R							
47500101h							
23	22	21	20	19	18	17	16
REVID							
R							
47500101h							
15	14	13	12	11	10	9	8
REVID							
R							
47500101h							
7	6	5	4	3	2	1	0
REVID							
R							
47500101h							

Table 5-1254. FSAS_OTFA_REGS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	REVID	R	47500101h	REVID

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5.7.2.16 FSAS_OTFA_REGS_SCFG Register

5.7.2.16.1 FSAS_OTFA_REGS_SCFG Register (Offset = 4h) [reset = 2h]

This register defines the power IDLE mode.

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Table 5-1255. Instance Table

Instance Name	Physical Address
FSS0	5380 2004h

Figure 5-613. FSAS_OTFA_REGS_SCFG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						IDLE_MODE	
NONE						R/W	
0h						2h	

Table 5-1256. FSAS_OTFA_REGS_SCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1:0	IDLE_MODE	R/W	2h	IDLE MODE. 0x0: Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements. Backup mode, for debug only. 0x1: No-idle mode: local target never enters idle state. Backup mode, for debug only. 0x2: Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wakeup events. 0x3: Reserved

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5.7.2.17 FSAS_OTFA_REGS_ISR Register

5.7.2.17.1 FSAS_OTFA_REGS_ISR Register (Offset = 8h) [reset = 0h]

Per-event raw interrupt status vector Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug and SW testing.

Return to Summary Table

Table 5-1257. Instance Table

Instance Name	Physical Address
FSS0	5380 2008h

Figure 5-614. FSAS_OTFA_REGS_ISR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 5-1258. FSAS_OTFA_REGS_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	Region MAC compare error event, Read MAC did not match the Write MAC. Write 0:No action Read 0:No event pending Read 1:Event pending Write 1:Set event (debug)
11:8	WRT_ERR	R/W	0h	Region write error event, write cmd issues when write is disabled Write 0:No action Read 0:No event pending Read 1:Event pending Write 1:Set event (debug)

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Table 5-1258. FSAS_OTFA_REGS_ISR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossed a start or end of a region. Write 0:No action Read 0:No event pending Read 1:Event pending Write 1:Set event (debug)
3:0	CTR_WKV	R/W	0h	AES CTR enabled region violated Wrt Once Per Wrt Key rule. Write 0:No action Read 0:No event pending Read 1:Event pending Write 1:Set event (debug)

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5.7.2.18 FSAS_OTFA_REGS_IS Register

5.7.2.18.1 FSAS_OTFA_REGS_IS Register (Offset = Ch) [reset = 0h]

Per-event "enabled" interrupt status vector. Enabled status isn't set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled).

Return to Summary Table

Table 5-1259. Instance Table

Instance Name	Physical Address
FSS0	5380 200Ch

Figure 5-615. FSAS_OTFA_REGS_IS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 5-1260. FSAS_OTFA_REGS_IS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	Region MAC compare error event, Read MAC did not match the Write MAC. Write 0:No action Read 0:No (enabled) event pending Read 1:Event pending Write 1:Clear event
11:8	WRT_ERR	R/W	0h	Region write error event, write cmd issues when write is disabled. Write 0:No action Read 0:No (enabled) event pending Read 1:Event pending Write 1:Clear event

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Table 5-1260. FSAS_OTFA_REGS_IS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossing a start or end of a region. Write 0:No action Read 0:No (enabled) event pending Read 1:Event pending Write 1:Clear event Note: a RMW transaction can make create 2 events , 1st do to the orginal over lap and then 2nd do to the new wrt cmd. Also, a RM and RMW can create event on the 2nd transaction do to the over lap do to the expansion of the transaction.
3:0	CTR_WKV	R/W	0h	AES CTR enabled region violated Wrt Once Per Wrt Key rule. Write 0:No action Read 0:No (enabled) event pending Read 1:Event pending Write 1:Clear event and reset counter

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5.7.2.19 FSAS_OTFA_REGS_IES Register

5.7.2.19.1 FSAS_OTFA_REGS_IES Register (Offset = 10h) [reset = 0h]

Per-event interrupt enable bit vector. Write 1 to set (enable interrupt). Readout equal to corresponding _CLR register.

Return to Summary Table

Table 5-1261. Instance Table

Instance Name	Physical Address
FSS0	5380 2010h

Figure 5-616. FSAS_OTFA_REGS_IES Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 5-1262. FSAS_OTFA_REGS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	Region MAC compare error event, Read MAC did not match the Write MAC. Write 0:No action Read 0:Interrupt disabled (masked) Read 1:Interrupt enabled Write 1:Enable interrupt
11:8	WRT_ERR	R/W	0h	Region write error event, write cmd issues when write is disabled. Write 0:No action Read 0:Interrupt disabled (masked) Read 1:Interrupt enabled Write 1:Enable interrupt

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Table 5-1262. FSAS_OTFA_REGS_IES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossing a start or end of a region. Write 0:No action Read 0:Interrupt disabled (masked) Read 1:Interrupt enabled Write 1:Enable interrupt
3:0	CTR_WKV	R/W	0h	AES CTR enabled region violated Wrt Once Per Wrt Key rule. Write 0:No action Read 0:Interrupt disabled (masked) Read 1:Interrupt enabled Write 1:Enable interrupt

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5.7.2.20 FSAS_OTFA_REGS_IEC Register

5.7.2.20.1 FSAS_OTFA_REGS_IEC Register (Offset = 14h) [reset = 0h]

Per-event interrupt enable bit vector. Write 1 to clear (disable interrupt). Readout equal to corresponding _SET register.

Return to Summary Table

Table 5-1263. Instance Table

Instance Name	Physical Address
FSS0	5380 2014h

Figure 5-617. FSAS_OTFA_REGS_IEC Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MAC_ERR				WRT_ERR			
R/W				R/W			
0h				0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REGION_BV				CTR_WKV			
R/W				R/W			
0h				0h			

Table 5-1264. FSAS_OTFA_REGS_IEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:12	MAC_ERR	R/W	0h	Region MAC compare error event, Read MAC did not match the Write MAC. Write 0:No action Read 0:Interrupt disabled (masked) Read 1:Interrupt enabled Write 1:Enable interrupt
11:8	WRT_ERR	R/W	0h	Region write error event, write cmd issues when write is disabled Write 0:No action Read 0:Interrupt disabled (masked) Read 1:Interrupt enabled Write 1:Disable interrupt

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Table 5-1264. FSAS_OTFA_REGS_IEC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	REGION_BV	R/W	0h	Region overflow boundary event caused by a burst transaction crossing a start or end of a region. Write 0:No action Read 0:Interrupt disabled (masked) Read 1:Interrupt enabled Write 1:Disable interrupt
3:0	CTR_WKV	R/W	0h	AES CTR enabled region violated Wrt Once Per Wrt Key rule. Write 0:No action Read 0:Interrupt disabled (masked) Read 1:Interrupt enabled Write 1:Disable interrupt

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5.7.2.21 FSAS_OTFA_REGS_CCFG Register

5.7.2.21.1 FSAS_OTFA_REGS_CCFG Register (Offset = 18h) [reset = 0h]

This register controls the enabling and the functionality of this AES core.

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Table 5-1265. Instance Table

Instance Name	Physical Address
FSS0	5380 2018h

Figure 5-618. FSAS_OTFA_REGS_CCFG Name Register

31	30	29	28	27	26	25	24
MASTER_EN_RD	RESERVED						
R/W	NONE						
0h	0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FE_PROC_EN	RESERVED		MAC_LSB_ALIGN_EN	MAC_SIZE		RSVD	OTFA_WAIT
R/W	NONE		R/W	R/W			R/W
0h	0h		0h	0h		0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	RSVD	CACHE_EVICT_MODE	KEY_SIZE	RSVD			
NONE		R/W	R/W				
0h	0h	0h	0h	0h			

Table 5-1266. FSAS_OTFA_REGS_CCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MASTER_EN_RD	R/W	0h	This register controls the enabling and the functionality of this IP. Write 0:Request to Disabled and enter into Bypass mode. Read 0:Disabled and enter into Bypass mode is active When Disabled, then Bypass mux is enabled which will directly connect the otfa_emif4d ocp hp target port to the ocp hp master port. The OTFA core clock is gated in this mode. Write 1:Request to Enabled mode Read 1:Enabled mode is active When Enabled, all functionality is enabled and bypass mux will be disabled. Note: The SW most follow the defined programming procedure from switching states. Disable -> Enable and Enable -> Disable. See programming model for more details on the procedures that the SW needs to follow. The hw_disable_ctrl input port driven by Efuse bit will disable the ability for SW to set MasterEnable. hw_disable_ctrl = 1, then MasterEnable will be forced to 0, SW WRT will have no effect, SW will always read back 0. hw_disable_ctrl = 0, then MasterEnable state can get controlled by SW. Note: Optimization MMR should not be changed when MasterEnable is 0, after the first Disable -> Enable phase

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Table 5-1266. FSAS_OTFA_REGS_CCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30:16	RESERVED	NONE	0h	Reserved
15	FE_PROC_EN	R/W	0h	This register allows the AES-CTR , GCM , GHASH modes to start the required AES jobs as soon as the RD CMD is passed through OTFA to help hide the AES op latency 0x0: Front End CMD AES start disable, only backend response , Legacy mode 0x1: Front End CMD AES start enabled, when enable only AES-CTR, GCM, and GHASH modes are supported
14:13	RESERVED	NONE	0h	Reserved
12	MAC_LSB_ALIGN_EN	R/W	0h	This register controls shift of mac data to always LSB independent of address. 0x0: Default mode 0x1: Set, for FSS use case, updated Opti flash.
11:10	MAC_SIZE	R/W	0h	This register defines the MAC size. 0x0: 4-bytes 0x1: 8-bytes 0x2: 12-bytes 0x3: 16-bytes.
8	OTFA_WAIT	R/W	0h	This register allows the ability to stop any new transactions from getting accepted and allow the current transactions to complete. Note: The otfa_emif has a one deep receive pipe stage, this will allow one new crypto cmd to get accepted before backpressure is asserted. Rules: Wait assertion can occur at any time. Wait de-assertion should only occur when CSTATUS.Busy is cleared SW needs to verify CSTATUS.Busy is cleared before it updates crypto region attributes. Non-Crypto transactions get accepted when Wait is asserted.
7	RESERVED	NONE	0h	Reserved
5	CACHE_EVICT_MODE	R/W	0h	cache evict mode
4	KEY_SIZE	R/W	0h	This register controls the key size used for all AES operations. 0x0: 128 Bit 0x1: 256 Bit

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5.7.2.22 FSAS_OTFA_REGS_CSTATUS Register

5.7.2.22.1 FSAS_OTFA_REGS_CSTATUS Register (Offset = 1Ch) [reset = 0h]

This is the status register which can be used to fine tune the AES core allocation to the Rd Pipe and Wrt Pipe along with a global activity status. Performance Counters which counts the number of events which causes high latency.

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Table 5-1267. Instance Table

Instance Name	Physical Address
FSS0	5380 201Ch

Figure 5-619. FSAS_OTFA_REGS_CSTATUS Name Register

31	30	29	28	27	26	25	24
BUSY	CRYPTO_BUSY	RD_STALL_EVENT_CNT					
R	R	R/W1TC					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_STALL_EVENT_CNT							
R/W1TC							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		WRT_STALL_EVENT_CNT					
NONE		R/W1TC					
0h		0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WRT_STALL_EVENT_CNT							
R/W1TC							
0h							

Table 5-1268. FSAS_OTFA_REGS_CSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BUSY	R	0h	0x0: No transactions are active, crypto or non-crypto. 0x1: One or more transactions are active, crypto or non-crypto SW needs to read 2 consecutive 0 with 100ns delay or more between samples to insure the pipe is fully empty
30	CRYPTO_BUSY	R	0h	0x0: No crypto transactions are active 0x1: One or more crypto transactions are active. SW needs to read 2 consecutive 0 with 100ns delay or more between samples to insure the pipe is fully empty
29:16	RD_STALL_EVENT_CNT	R/W1TC	0h	Read the number of Rd Pipe full events. The counter increments every clock.event that we have no more rd cores available for a new transaction. Saturates to 0x3FFF. Any Write to CSTATUS reset RdStallEventCnt and WrtStallEventCnt to 0x0.
15:14	RESERVED	NONE	0h	Reserved
13:0	WRT_STALL_EVENT_CNT	R/W1TC	0h	Read the number of Wrt Pipe full events. The counter increments every clock.event that we have no more wrt cores available for a new transaction. Saturates to 0x3FFF. Any Write to CSTATUS reset RdStallEventCnt and WrtStallEventCnt to 0x0.

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5.7.2.23 FSAS_OTFA_REGS_IRQADDINFO0 Register

5.7.2.23.1 FSAS_OTFA_REGS_IRQADDINFO0 Register (Offset = 220h) [reset = 0h]

IRQAdditionalInfo0 .

Return to Summary Table

Table 5-1269. Instance Table

Instance Name	Physical Address
FSS0	5380 2220h

Figure 5-620. FSAS_OTFA_REGS_IRQADDINFO0 Name Register

31	30	29	28	27	26	25	24
IRQ_MADDR							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_MADDR							
R							
0h							
15	14	13	12	11	10	9	8
IRQ_MADDR							
R							
0h							
7	6	5	4	3	2	1	0
IRQ_MADDR							
R							
0h							

Table 5-1270. FSAS_OTFA_REGS_IRQADDINFO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	IRQ_MADDR	R	0h	Master Address which caused the event. Note During MAC Error Events a new response can over write the data. Another method to debug is to enable error response , this can also be used to mark which transaction caused the error.

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5.7.2.24 FSAS_OTFA_REGS_IRQADDINFO1 Register

5.7.2.24.1 FSAS_OTFA_REGS_IRQADDINFO1 Register (Offset = 224h) [reset = 0h]

IRQAdditionalInfo1 .

Return to Summary Table

Table 5-1271. Instance Table

Instance Name	Physical Address
FSS0	5380 2224h

Figure 5-621. FSAS_OTFA_REGS_IRQADDINFO1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED						IRQ_MLEN	
NONE						R	
0h						0h	
15	14	13	12	11	10	9	8
IRQ_MLEN		IRQ_MSEQ			IRQ_MCMD		
R		R			R		
0h		0h			0h		
7	6	5	4	3	2	1	0
IRQ_MID							
R							
0h							

Table 5-1272. FSAS_OTFA_REGS_IRQADDINFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED	NONE	0h	Reserved
17:14	IRQ_MLEN	R	0h	Master OCP LENGTH which caused the event
13:11	IRQ_MSEQ	R	0h	Master OCP Seq which caused the event. Not avalible for MAC error events
10:8	IRQ_MCMD	R	0h	Master OCP CMD which caused the event. Note: During MAC Error Events a new response can over write the data. Another method to debug is to enable error response , this can also be used to mark which transaction caused the error.
7:0	IRQ_MID	R	0h	Master OCP ID which caused the event Note: During MAC Error Events a new response can over write the data. Another method to debug is to enable error response , this can also be used to mark which transaction caused the error.

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5.7.2.25 FSAS_OTFA_REGS_MACCACHEINFO Register

5.7.2.25.1 FSAS_OTFA_REGS_MACCACHEINFO Register (Offset = 228h) [reset = 0h]

MACCacheInfo .

Return to Summary Table

Table 5-1273. Instance Table

Instance Name	Physical Address
FSS0	5380 2228h

Figure 5-622. FSAS_OTFA_REGS_MACCACHEINFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CACHE_MISS_EVENT_CNT							
R							
0h							
7	6	5	4	3	2	1	0
CACHE_MISS_EVENT_CNT							
R							
0h							

Table 5-1274. FSAS_OTFA_REGS_MACCACHEINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CACHE_MISS_EVENT_CNT	R	0h	Counts the number of Cache Miss events. Saturates to 0xFFFF Any Write to reset to 0x0 Note that any Read Transaction that crosses a cache line will trigger a cache miss and 2 lines will be read. Also, any Write Transaction that crosses a cache line will mark both lines dirty.

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5.7.2.26 FSAS_OTFA_REGS_RMWRMCNT Register

5.7.2.26.1 FSAS_OTFA_REGS_RMWRMCNT Register (Offset = 22Ch) [reset = 0h]

RMWRMCnt .

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Table 5-1275. Instance Table

Instance Name	Physical Address
FSS0	5380 222Ch

Figure 5-623. FSAS_OTFA_REGS_RMWRMCNT Name Register

31	30	29	28	27	26	25	24
RM_EVENT_CNT							
R							
0h							
23	22	21	20	19	18	17	16
RM_EVENT_CNT							
R							
0h							
15	14	13	12	11	10	9	8
RMW_EVENT_CNT							
R							
0h							
7	6	5	4	3	2	1	0
RMW_EVENT_CNT							
R							
0h							

Table 5-1276. FSAS_OTFA_REGS_RMWRMCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RM_EVENT_CNT	R	0h	Counts the number of RM events. Saturates to 0xFFFF Any Write to RMWRMCNT will reset rm_event_cnt and rmw_event_cnt
15:0	RMW_EVENT_CNT	R	0h	Counts the number of RMW events. Saturates to 0xFFFF Any Write to RMWRMCNT will reset rm_event_cnt and rmw_event_cnt

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5.7.2.27 FSAS_OTFA_REGS_RG_RGCFG_J Register

5.7.2.27.1 FSAS_OTFA_REGS_RG_RGCFG_J Register (Offset = 20h) [reset = 0h]

RegionCfg

Return to Summary Table

Table 5-1277. Instance Table

Instance Name	Physical Address
FSS0	5380 2020h + formula

Figure 5-624. FSAS_OTFA_REGS_RG_RGCFG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			WRT_PROTECT	MAC_MODE		AES_MODE	
NONE			R/W	R/W		R/W	
0h			0h	0h		0h	

Table 5-1278. FSAS_OTFA_REGS_RG_RGCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RESERVED	NONE	0h	Reserved
4	WRT_PROTECT	R/W	0h	WRT protect
3:2	MAC_MODE	R/W	0h	MAC mode
1:0	AES_MODE	R/W	0h	AES mode

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5.7.2.28 FSAS_OTFA_REGS_RG_RGMACST_J Register

5.7.2.28.1 FSAS_OTFA_REGS_RG_RGMACST_J Register (Offset = 24h) [reset = 0h]

RegionMacStart

Return to Summary Table

Table 5-1279. Instance Table

Instance Name	Physical Address
FSS0	5380 2024h + formula

Figure 5-625. FSAS_OTFA_REGS_RG_RGMACST_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				M_START			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
M_START							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
M_START							
R/W							
0h							

Table 5-1280. FSAS_OTFA_REGS_RG_RGMACST_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	M_START	R/W	0h	This defines the start of the mac buffer in 4KBytes steps

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5.7.2.29 FSAS_OTFA_REGS_RG_RGST_J Register

5.7.2.29.1 FSAS_OTFA_REGS_RG_RGST_J Register (Offset = 28h) [reset = 0h]

RegionStart

Return to Summary Table

Table 5-1281. Instance Table

Instance Name	Physical Address
FSS0	5380 2028h + formula

Figure 5-626. FSAS_OTFA_REGS_RG_RGST_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				R_START			
NONE				R/W			
0h				0h			
15	14	13	12	11	10	9	8
R_START							
R/W							
0h							
7	6	5	4	3	2	1	0
R_START							
R/W							
0h							

Table 5-1282. FSAS_OTFA_REGS_RG_RGST_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_START	R/W	0h	This defines the start of the crypto region in 4KBytes steps

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5.7.2.30 FSAS_OTFA_REGS_RG_RGSI_J Register

5.7.2.30.1 FSAS_OTFA_REGS_RG_RGSI_J Register (Offset = 2Ch) [reset = 0h]

RegionSize

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Table 5-1283. Instance Table

Instance Name	Physical Address
FSS0	5380 202Ch + formula

Figure 5-627. FSAS_OTFA_REGS_RG_RGSI_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				R_SIZE			
NONE				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_SIZE							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_SIZE							
R/W							
0h							

Table 5-1284. FSAS_OTFA_REGS_RG_RGSI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED	NONE	0h	Reserved
19:0	R_SIZE	R/W	0h	This defines the size of the crypto region in 4KBytes steps

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5.7.2.31 FSAS_OTFA_REGS_RG_RKEYE_J_K Register

5.7.2.31.1 FSAS_OTFA_REGS_RG_RKEYE_J_K Register (Offset = 30h) [reset = 0h]

RegionKeyE

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Table 5-1285. Instance Table

Instance Name	Physical Address
FSS0	5380 2030h + formula

Figure 5-628. FSAS_OTFA_REGS_RG_RKEYE_j_k Name Register

31	30	29	28	27	26	25	24
R_KEY_E							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_E							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_E							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_E							
R/W							
0h							

Table 5-1286. FSAS_OTFA_REGS_RG_RKEYE_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_E	R/W	0h	Key E

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5.7.2.32 FSAS_OTFA_REGS_RG_RKEYEP_J_K Register

5.7.2.32.1 FSAS_OTFA_REGS_RG_RKEYEP_J_K Register (Offset = 50h) [reset = 0h]

RegionKeyEP

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Table 5-1287. Instance Table

Instance Name	Physical Address
FSS0	5380 2050h + formula

Figure 5-629. FSAS_OTFA_REGS_RG_RKEYEP_j_k Name Register

31	30	29	28	27	26	25	24
R_KEY_EP							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_EP							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_EP							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_EP							
R/W							
0h							

Table 5-1288. FSAS_OTFA_REGS_RG_RKEYEP_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_EP	R/W	0h	Key EP

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5.7.2.33 FSAS_OTFA_REGS_RG_RKEYA_J_K Register

5.7.2.33.1 FSAS_OTFA_REGS_RG_RKEYA_J_K Register (Offset = 70h) [reset = 0h]

RegionKeyA

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Table 5-1289. Instance Table

Instance Name	Physical Address
FSS0	5380 2070h + formula

Figure 5-630. FSAS_OTFA_REGS_RG_RKEYA_j_k Name Register

31	30	29	28	27	26	25	24
R_KEY_A							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_A							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_A							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_A							
R/W							
0h							

Table 5-1290. FSAS_OTFA_REGS_RG_RKEYA_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_A	R/W	0h	Key A

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5.7.2.34 FSAS_OTFA_REGS_RG_RKEYAP_J_K Register

5.7.2.34.1 FSAS_OTFA_REGS_RG_RKEYAP_J_K Register (Offset = 80h) [reset = 0h]

RegionKeyAP

Return to Summary Table

Table 5-1291. Instance Table

Instance Name	Physical Address
FSS0	5380 2080h + formula

Figure 5-631. FSAS_OTFA_REGS_RG_RKEYAP_j_k Name Register

31	30	29	28	27	26	25	24
R_KEY_AP							
R/W							
0h							
23	22	21	20	19	18	17	16
R_KEY_AP							
R/W							
0h							
15	14	13	12	11	10	9	8
R_KEY_AP							
R/W							
0h							
7	6	5	4	3	2	1	0
R_KEY_AP							
R/W							
0h							

Table 5-1292. FSAS_OTFA_REGS_RG_RKEYAP_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_KEY_AP	R/W	0h	Key AP

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5.7.2.35 FSAS_OTFA_REGS_RG_RIV_J_K Register

5.7.2.35.1 FSAS_OTFA_REGS_RG_RIV_J_K Register (Offset = 90h) [reset = 0h]

RegionIV

Return to Summary Table

Table 5-1293. Instance Table

Instance Name	Physical Address
FSS0	5380 2090h + formula

Figure 5-632. FSAS_OTFA_REGS_RG_RIV_j_k Name Register

31	30	29	28	27	26	25	24
R_IV							
R/W							
0h							
23	22	21	20	19	18	17	16
R_IV							
R/W							
0h							
15	14	13	12	11	10	9	8
R_IV							
R/W							
0h							
7	6	5	4	3	2	1	0
R_IV							
R/W							
0h							

Table 5-1294. FSAS_OTFA_REGS_RG_RIV_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	R_IV	R/W	0h	IV

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5.7.2.36 OSPI_CFG_PID Register

5.7.2.36.1 OSPI_CFG_PID Register (Offset = 0h) [reset = 68748100h]

The Revision Register contains the major and minor revisions for the module.

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Table 5-1295. Instance Table

Instance Name	Physical Address
FSS0	5380 6000h

Figure 5-633. OSPI_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		874h			
23	22	21	20	19	18	17	16
MODULE_ID							
R							
874h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
10h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		0h					

Table 5-1296. OSPI_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	PID register scheme
29:28	BU	R	2h	Business Unit: 10 = Processors
27:16	MODULE_ID	R	874h	Module ID
15:11	RTL	R	10h	RTL revision. Will vary depending on release.
10:8	MAJOR	R	1h	Major revision
7:6	CUSTOM	R	0h	Custom
5:0	MINOR	R	0h	Minor revision

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5.7.2.37 OSPI_CFG_STAT Register

5.7.2.37.1 OSPI_CFG_STAT Register (Offset = 8h) [reset = 0h]

The Status register provide general status bits for the ospi.

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Table 5-1297. Instance Table

Instance Name	Physical Address
FSS0	5380 6008h

Figure 5-634. OSPI_CFG_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_INIT_DONE	RESERVED
NONE						R	NONE
0h						0h	0h

Table 5-1298. OSPI_CFG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	MEM_INIT_DONE	R	0h	Bit indicates the memory initialization done status of the OSPI SRAM 1:Memory Intialization Done
0	RESERVED	NONE	0h	Reserved

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5.7.2.38 OSPI_CFG_EOI Register

5.7.2.38.1 OSPI_CFG_EOI Register (Offset = 20h) [reset = 0h]

End of Interrupt Register.

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Table 5-1299. Instance Table

Instance Name	Physical Address
FSS0	5380 6020h

Figure 5-635. OSPI_CFG_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOI							
W							
0h							

Table 5-1300. OSPI_CFG_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	EOI	W	0h	Write with bit position of targetted interrupt. (E.g. Ext TS is bit 0). Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt

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5.7.2.39 OSPI0_ECC_AGGR_REV Register

5.7.2.39.1 OSPI0_ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters.

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Table 5-1301. Instance Table

Instance Name	Physical Address
FSS0	5380 7000h

Figure 5-636. OSPI0_ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
7h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 5-1302. OSPI0_ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

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5.7.2.40 OSPI0_ECC_AGGR_VECTOR Register

5.7.2.40.1 OSPI0_ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register.

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Table 5-1303. Instance Table

Instance Name	Physical Address
FSS0	5380 7008h

Figure 5-637. OSPI0_ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 5-1304. OSPI0_ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

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5.7.2.41 OSPI0_ECC_AGGR_STAT Register

5.7.2.41.1 OSPI0_ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status.

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Table 5-1305. Instance Table

Instance Name	Physical Address
FSS0	5380 700Ch

Figure 5-638. OSPI0_ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1h							

Table 5-1306. OSPI0_ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

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5.7.2.42 OSPI0_ECC_AGGR_RESERVED_SVBUS_J Register

5.7.2.42.1 OSPI0_ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 5-1307. Instance Table

Instance Name	Physical Address
FSS0	5380 7010h + formula

Figure 5-639. OSPI0_ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 5-1308. OSPI0_ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

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5.7.2.43 OSPI0_ECC_AGGR_SEC_EOI_REG Register

5.7.2.43.1 OSPI0_ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

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Table 5-1309. Instance Table

Instance Name	Physical Address
FSS0	5380 703Ch

Figure 5-640. OSPI0_ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 5-1310. OSPI0_ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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5.7.2.44 OSPI0_ECC_AGGR_SEC_STATUS_REG0 Register

5.7.2.44.1 OSPI0_ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 5-1311. Instance Table

Instance Name	Physical Address
FSS0	5380 7040h

Figure 5-641. OSPI0_ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
NONE							R/W1TS
0h							0h

Table 5-1312. OSPI0_ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

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5.7.2.45 OSPI0_ECC_AGGR_SEC_ENABLE_SET_REG0 Register

5.7.2.45.1 OSPI0_ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 5-1313. Instance Table

Instance Name	Physical Address
FSS0	5380 7080h

Figure 5-642. OSPI0_ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 5-1314. OSPI0_ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

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5.7.2.46 OSPI0_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

5.7.2.46.1 OSPI0_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 5-1315. Instance Table

Instance Name	Physical Address
FSS0	5380 70C0h

Figure 5-643. OSPI0_ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 5-1316. OSPI0_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

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5.7.2.47 OSPI0_ECC_AGGR_DED_EOI_REG Register

5.7.2.47.1 OSPI0_ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

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Table 5-1317. Instance Table

Instance Name	Physical Address
FSS0	5380 713Ch

Figure 5-644. OSPI0_ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 5-1318. OSPI0_ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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5.7.2.48 OSPI0_ECC_AGGR_DED_STATUS_REG0 Register

5.7.2.48.1 OSPI0_ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 5-1319. Instance Table

Instance Name	Physical Address
FSS0	5380 7140h

Figure 5-645. OSPI0_ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
NONE							R/W1TS
0h							0h

Table 5-1320. OSPI0_ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_PEND	R/W1TS	0h	Interrupt Pending Status for sram_pend

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5.7.2.49 OSPI0_ECC_AGGR_DED_ENABLE_SET_REG0 Register

5.7.2.49.1 OSPI0_ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 5-1321. Instance Table

Instance Name	Physical Address
FSS0	5380 7180h

Figure 5-646. OSPI0_ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 5-1322. OSPI0_ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for sram_pend

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5.7.2.50 OSPI0_ECC_AGGR_DED_ENABLE_CLR_REG0 Register

5.7.2.50.1 OSPI0_ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 5-1323. Instance Table

Instance Name	Physical Address
FSS0	5380 71C0h

Figure 5-647. OSPI0_ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							SRAM_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 5-1324. OSPI0_ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for sram_pend

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5.7.2.51 OSPI0_ECC_AGGR_AGGR_ENABLE_SET Register

5.7.2.51.1 OSPI0_ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register.

Return to Summary Table

Table 5-1325. Instance Table

Instance Name	Physical Address
FSS0	5380 7200h

Figure 5-648. OSPI0_ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 5-1326. OSPI0_ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	Interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	Interrupt enable set for parity errors

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5.7.2.52 OSPI0_ECC_AGGR_AGGR_ENABLE_CLR Register

5.7.2.52.1 OSPI0_ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register.

Return to Summary Table

Table 5-1327. Instance Table

Instance Name	Physical Address
FSS0	5380 7204h

Figure 5-649. OSPI0_ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 5-1328. OSPI0_ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	Interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	Interrupt enable clear for parity errors

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5.7.2.53 OSPI0_ECC_AGGR_AGGR_STATUS_SET Register

5.7.2.53.1 OSPI0_ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register.

Return to Summary Table

Table 5-1329. Instance Table

Instance Name	Physical Address
FSS0	5380 7208h

Figure 5-650. OSPI0_ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 5-1330. OSPI0_ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	Interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	Interrupt status set for parity errors

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5.7.2.54 OSPI0_ECC_AGGR_AGGR_STATUS_CLR Register

5.7.2.54.1 OSPI0_ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register.

Return to Summary Table

Table 5-1331. Instance Table

Instance Name	Physical Address
FSS0	5380 720Ch

Figure 5-651. OSPI0_ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 5-1332. OSPI0_ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	Interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	Interrupt status clear for parity errors

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5.7.2.55 OSPI_FLASH_CFG_CONFIG_REG Register

5.7.2.55.1 OSPI_FLASH_CFG_CONFIG_REG Register (Offset = 0h) [reset = 80780081h]

This register contains basic configuration fields of the controller.

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Table 5-1333. Instance Table

Instance Name	Physical Address
FSS0	5380 8000h

Figure 5-652. OSPI_FLASH_CFG_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
IDLE_FLD	DUAL_BYTE_OPCODE_EN_FLD	CRC_ENABLE_FLD	CONFIG_RESV2_FLD			PIPELINE_PHY_FLD	ENABLE_DTR_PROTOCOL_FLD
R	R/W	R/W	R			R/W	R/W
1h	0h	0h	0h			0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ENABLE_AHB_DECODER_FLD	MSTR_BAUD_DIV_FLD				ENTER_XIP_MODE_IMM_FLD	ENTER_XIP_MODE_FLD	ENB_AHB_ADDR_REMAP_FLD
R/W	R/W				R/W	R/W	R/W
0h	Fh				0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ENB_DMA_IF_FLD	WR_PROT_FLASH_FLD	PERIPH_CS_LINES_FLD				PERIPH_SEL_DEC_FLD	ENB_LEGACY_IP_MODE_FLD
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ENB_DIR_ACC_CTLR_FLD	RESET_CFG_FLD	RESET_PIN_FLD	HOLD_PIN_FLD	PHY_MODE_ENABLE_FLD	SEL_CLK_PHASE_FLD	SEL_CLK_POL_FLD	ENB_SPI_FLD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	0h	0h	1h

Table 5-1334. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE_FLD	R	1h	Serial interface and low level SPI pipeline is IDLE: This is a STATUS read-only bit. Note this is a retimed signal, so there will be some inherent delay on the generation of this status signal.
30	DUAL_BYTE_OPCODE_EN_FLD	R/W	0h	Dual-byte Opcode Mode enable bit This bit is to be set in case the target Flash Device supports dual byte opcode [i.e. Macronix MX25]. It is applicable for Octal I/O Mode or Protocol only so should be set back to low if the device is configured to work in another SPI Mode. If enabled, the supplementing bytes are taken from Opcode Extension Register [Lower] and from Opcode Extension Register [Upper].
29	CRC_ENABLE_FLD	R/W	0h	CRC enable bit This bit is to be set in case the target Flash Device supports CRC [Macronix MX25]. It is applicable for Octal DDR Protocol only so should be set back to low if the device is configured to work in another SPI Mode.
28:26	CONFIG_RESV2_FLD	R	0h	Reserved
25	PIPELINE_PHY_FLD	R/W	0h	Pipeline PHY Mode enable: This bit is relevant only for configuration with PHY Module. It should be asserted to 1 between consecutive PHY pipeline reads transfers and de-asserted to 0 otherwise.
24	ENABLE_DTR_PROTOCOL_FLD	R/W	0h	Enable DTR Protocol: This bit should be set if device is configured to work in DTR protocol.

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Table 5-1334. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ENABLE_AHB_DECODER_FLD	R/W	0h	Enable AHB Decoder: Value 0 : Active target is selected based on Peripheral Chip Select Lines [bits [13:10]]. Value=1 Active target is selected based on actual AHB address [the partition for each device is calculated with respect to bits [28:21] of Device Size Configuration Register]
22:19	MSTR_BAUD_DIV_FLD	R/W	Fh	Master Mode Baud Rate Divisor: SPI baud rate = (master reference clock) baud_rate_divisor. Where BD is: 4b0000 = /2 4b0001 = /4 4b0010 = /6 4b0011 = /8 4b0100 = /10 4b0101 = /12 .. 4b1111 = /32 While the PHY Mode is enabled, clock from DLL is granted and consequently forwarded into external FLASH Device. Its frequency is equal to ref_clk i.e., value of /1 is used in PHY mode. Set this register up before enabling the Octal-SPI controller.
18	ENTER_XIP_MODE_IMM_FLD	R/W	0h	Enter XIP Mode immediately: Value 0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value 1 : Operate the device in XIP mode immediately Use this register when the external device wakes up in XIP mode [as per the contents of its non- volatile configuration register]. The controller will assume the next READ instruction will be passed to the device as an XIP instruction, and therefore will not require the READ opcode to be transferred. Note: To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only after the next READ instruction is executed. Software therefore should ensure that at least one READ instruction is requested after resetting this bit in order to be sure that XIP mode is exited.
17	ENTER_XIP_MODE_FLD	R/W	0h	Enter XIP Mode on next READ: Value 0 : If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. Value 1 : If XIP is disabled, then setting to ?1? will inform the controller that the device is ready to enter XIP on the next READ instruction. The controller will therefore send the appropriate command sequence, including mode bits to cause the device to enter XIP mode. Use this register after the controller has ensured the FLASH device has been configured to be ready to enter XIP mode. Note : To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only AFTER the next READ instruction is executed. Software should therefore ensure that at least one READ instruction is requested after resetting this bit before it can be sure XIP mode in the device is exited.
16	ENB_AHB_ADDR_REMAP_FLD	R/W	0h	Enable AHB Address Re-mapping: [Direct Access Mode Only] When set to 1, the incoming AHB address will be adapted and sent to the FLASH device as [address + N], where N is the value stored in the remap address register.
15	ENB_DMA_IF_FLD	R/W	0h	Enable DMA Peripheral Interface: Set to 1 to enable the DMA handshaking logic. When enabled the controller will trigger DMA transfer requests via the DMA peripheral interface. Set to 0 to disable
14	WR_PROT_FLASH_FLD	R/W	0h	Write Protect Flash Pin: Set to drive the Write Protect pin of the FLASH device. This is resynchronized to the generated memory clock as necessary.

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Table 5-1334. OSPI_FLASH_CFG_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:10	PERIPH_CS_LINES_FLD	R/W	0h	Peripheral Chip Select Lines: Peripheral chip select lines If pdec = 0, ss[3:0] are output thus: ss[3:0] n_ss_out[3:0] xxx0 1110xx01 1101x011 10110111 01111111 1111[no peripheral selected] else ss[3:0] directly drives n_ss_out[3:0]
9	PERIPH_SEL_DEC_FLD	R/W	0h	Peripheral select decode: 0 : only 1 of 4 selects n_ss_out[3:0] is active 1 : allow external 4-to-16 decode [n_ss_out = ss]
8	ENB_LEGACY_IP_MODE_FLD	R/W	0h	Legacy IP Mode Enable: 0 : Use Direct Access Controller/Indirect Access Controller 1 : legacy Mode is enabled. In this mode, any write to the controller via the AHB interface is serialized and sent to the FLASH device. Any valid AHB read will pop the internal RX-FIFO, retrieving data that was forwarded by the external FLASH device on the SPI lines,4,2 or 1 byte transfers are permitted and controlled via the HSIZE input.
7	ENB_DIR_ACC_CTLR_FLD	R/W	1h	Enable Direct Access Controller: 0 : disable the Direct Access Controller once current transfer of the data word [FF_W] is complete. 1 : enable the Direct Access Controller When the Direct Access Controller and Indirect Access Controller are both disabled, all AHB requested are completed with an error response.
6	RESET_CFG_FLD	R/W	0h	RESET pin configuration: 0 = RESET feature on DQ3 pin of the device 1 = RESET feature on dedicated pin of the device [controlling of 5th bit influences on reset_out output]
5	RESET_PIN_FLD	R/W	0h	Set to drive the RESET pin of the FLASH device and reset for de-activation of the RESET pin feature
4	HOLD_PIN_FLD	R/W	0h	Set to drive the HOLD pin of the FLASH device and reset for de-activation of the HOLD pin feature
3	PHY_MODE_ENABLE_FLD	R/W	0h	PHY mode enable: When enabled, the controller is informed that PHY Module is to be used for handling SPI transfers. This bit is relevant only for configuration with PHY Module.
2	SEL_CLK_PHASE_FLD	R/W	0h	Select Clock Phase: Selects whether the clock is in an active or inactive phase outside the SPI word. 0 : the SPI clock is active outside the word 1 : the SPI clock is inactive outside the word
1	SEL_CLK_POL_FLD	R/W	0h	Clock polarity outside SPI word: 0 : the SPI clock is quiescent low 1 : the SPI clock is quiescent high
0	ENB_SPI_FLD	R/W	1h	Octal-SPI Enable: 0 : disable the Octal-SPI, once current transfer of the data word [FF_W] is complete. 1 : enable the Octal-SPI, when spi_enable = 0, all output enables are inactive and all pins are set to input mode.

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5.7.2.56 OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register

5.7.2.56.1 OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register (Offset = 4h) [reset = 3h]

This register defines the configuration of Multiple-SPI READ instruction. This register should be setup while the controller is idle.

Return to Summary Table

Table 5-1335. Instance Table

Instance Name	Physical Address
FSS0	5380 8004h

Figure 5-653. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RD_INSTR_RESV5_FLD			DUMMY_RD_CLK_CYCLES_FLD				
R			R/W				
0h			0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_INSTR_RESV4_FLD			MODE_BIT_ENABLE_FLD	RD_INSTR_RESV3_FLD		DATA_XFER_TYPE_EXT_MODE_FLD	
R			R/W	R		R/W	
0h			0h	0h		0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_INSTR_RESV2_FLD		ADDR_XFER_TYPE_STD_MODE_FLD		RD_INSTR_RESV1_FLD	DDR_EN_FLD	INSTR_TYPE_FLD	
R		R/W		R	R/W	R/W	
0h		0h		0h	0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RD_OPCODE_NON_XIP_FLD							
R/W							
3h							

Table 5-1336. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RD_INSTR_RESV5_FLD	R	0h	Reserved
28:24	DUMMY_RD_CLK_CYCLES_FLD	R/W	0h	Dummy Read Clock Cycles: Number of dummy clock cycles required by device for read instruction.
23:21	RD_INSTR_RESV4_FLD	R	0h	Reserved
20	MODE_BIT_ENABLE_FLD	R/W	0h	Mode Bit Enable: Set this field to 1 to ensure that the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
19:18	RD_INSTR_RESV3_FLD	R	0h	Reserved
17:16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs.
15:14	RD_INSTR_RESV2_FLD	R	0h	Reserved

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Table 5-1336. OSPI_FLASH_CFG_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0]
11	RD_INSTR_RESV1_FLD	R	0h	Reserved
10	DDR_EN_FLD	R/W	0h	DDR Enable: This is to inform that opcode from rd_opcode_non_xip_fld is compliant with one of the DDR READ Commands
9:8	INSTR_TYPE_FLD	R/W	0h	Instruction Type: 0 : Use Standard SPI mode [instruction always shifted into the device on DQ0 only] 1 : Use DIO-SPI mode [Instructions, Address and Data always sent on DQ0 and DQ1] 2 : Use QIO-SPI mode [Instructions, Address and Data always sent on DQ0, DQ1, DQ2 and DQ3] 3 : Use Octal-IO-SPI mode [Instructions, Address and Data always sent on DQ[7:0]]
7:0	RD_OPCODE_NON_XIP_FLD	R/W	3h	Read Opcode in non-XIP mode: Read Opcode to use when not in XIP mode

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5.7.2.57 OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register

5.7.2.57.1 OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register (Offset = 8h) [reset = 2h]

This register defines the configuration of Multiple-SPI WRITE (Program Page) instruction. This register should be setup while the controller is idle.

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Table 5-1337. Instance Table

Instance Name	Physical Address
FSS0	5380 8008h

Figure 5-654. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">WR_INSTR_RESV4_FLD</td><td colspan="5">DUMMY_WR_CLK_CYCLES_FLD</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">WR_INSTR_RESV3_FLD</td><td colspan="2">DATA_XFER_TYPE_EXT_MODE_FLD</td></tr>
<tr><td colspan="6">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="6">0h</td><td colspan="2">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">WR_INSTR_RESV2_FLD</td><td colspan="2">ADDR_XFER_TYPE_STD_MODE_FLD</td><td colspan="3">WR_INSTR_RESV1_FLD</td><td>WEL_DIS_FLD</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R/W</td><td colspan="3">R</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="3">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">WR_OPCODE_FLD</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">2h</td></tr>
</table>

Table 5-1338. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	WR_INSTR_RESV4_FLD	R	0h	Reserved
28:24	DUMMY_WR_CLK_CYCLES_FLD	R/W	0h	Dummy Write Clock Cycles: Number of dummy clock cycles required by device for write instruction.
23:18	WR_INSTR_RESV3_FLD	R	0h	Reserved
17:16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes: 0 : SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1 : Used for Dual Input/Output instructions. For data transfers, DQ0 and DQ1 are used as both inputs and outputs. 2 : Used for Quad Input/Output instructions. For data transfers, DQ0,DQ1,DQ2 and DQ3 are used as both inputs and outputs. 3 : Used for Quad Input/Output instructions. For data transfers, DQ[7:0] are used as both inputs and outputs.
15:14	WR_INSTR_RESV2_FLD	R	0h	Reserved
13:12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes: 0 : Addresses can be shifted to the device on DQ0 only 1 : Addresses can be shifted to the device on DQ0 and DQ1 only 2 : Addresses can be shifted to the device on DQ0, DQ1, DQ2 and DQ3 3 : Addresses can be shifted to the device on DQ[7:0]
11:9	WR_INSTR_RESV1_FLD	R	0h	Reserved

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Table 5-1338. OSPI_FLASH_CFG_DEV_INSTR_WR_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	WEL_DIS_FLD	R/W	0h	WEL Disable: This is to turn off automatic issuing of WEL Command before write operation for DAC or INDAC
7:0	WR_OPCODE_FLD	R/W	2h	Write Opcode

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5.7.2.58 OSPI_FLASH_CFG_DEV_DELAY_REG Register

5.7.2.58.1 OSPI_FLASH_CFG_DEV_DELAY_REG Register (Offset = Ch) [reset = 0h]

Octal-SPI Device Delay Register: This register is used to introduce relative delays into the generation of the master output signals. All timings are defined in cycles of the SPI REFERENCE CLOCK/ext_clk, defined in this table as SPI master ref clock.

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Table 5-1339. Instance Table

Instance Name	Physical Address
FSS0	5380 800Ch

Figure 5-655. OSPI_FLASH_CFG_DEV_DELAY_REG Name Register

31	30	29	28	27	26	25	24
D_NSS_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
D_BTWN_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
D_AFTER_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
D_INIT_FLD							
R/W							
0h							

Table 5-1340. OSPI_FLASH_CFG_DEV_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	D_NSS_FLD	R/W	0h	Clock Delay for Chip Select Deassert: Delay in master reference clocks for the length that the master mode chip select outputs are de-asserted between transactions. The minimum delay is always SCLK period to ensure the chip select is never re-asserted within an SCLK period.
23:16	D_BTWN_FLD	R/W	0h	Clock Delay for Chip Select Deactivation: Delay in master reference clocks between one chip select being de-activated and the activation of another. This is used to ensure a quiet period between the selection of two different targets and requires the transmit FIFO to be empty.
15:8	D_AFTER_FLD	R/W	0h	Clock Delay for Last Transaction Bit: Delay in master reference clocks between last bit of current transaction and deasserting the device chip select [n_ss_out]. By default, the chip select will be deasserted on the cycle following the completion of the current transaction.
7:0	D_INIT_FLD	R/W	0h	Clock Delay with n_ss_out: Delay in master reference clocks between setting n_ss_out low and first bit transfer.

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5.7.2.59 OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register

5.7.2.59.1 OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register (Offset = 10h) [reset = 1h]

This register is used to adjust SPI transfer conditions in order to fetch and capture data reliably. This register should be setup while the controller is idle.

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Table 5-1341. Instance Table

Instance Name	Physical Address
FSS0	5380 8010h

Figure 5-656. OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RD_DATA_RESV3_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RD_DATA_RESV3_FLD</td><td colspan="4">DDR_READ_DELAY_FLD</td></tr>
<tr><td colspan="4">R</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="7">RD_DATA_RESV2_FLD</td><td>DQS_ENABLE_FLD</td></tr>
<tr><td colspan="7">R</td><td>R/W</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RD_DATA_RESV1_FLD</td><td>SAMPLE_EDGE_SEL_FLD</td><td colspan="4">DELAY_FLD</td><td>BYPASS_FLD</td></tr>
<tr><td colspan="2">R</td><td>R/W</td><td colspan="4">R/W</td><td>R/W</td></tr>
<tr><td colspan="2">0h</td><td>0h</td><td colspan="4">0h</td><td>1h</td></tr>
</table>

Table 5-1342. OSPI_FLASH_CFG_RD_DATA_CAPTURE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RD_DATA_RESV3_FLD	R	0h	Reserved
19:16	DDR_READ_DELAY_FLD	R/W	0h	DDR read delay: Delay the transmitted data by the programmed number of ref_clk cycles.This field is only relevant when DDR Read Command is executed. Otherwise can be ignored.
15:9	RD_DATA_RESV2_FLD	R	0h	Reserved
8	DQS_ENABLE_FLD	R/W	0h	DQS enable bit: If enabled, signal from DQS input is driven into RX DLL and is used for data capturing in PHY Mode rather than internally generated gated ref_clk..
7:6	RD_DATA_RESV1_FLD	R	0h	Reserved
5	SAMPLE_EDGE_SEL_FLD	R/W	0h	Sample edge selection: Choose edge on which data outputs from flash memory will be sampled
4:1	DELAY_FLD	R/W	0h	Read Delay: Delay the read data capturing logic by the programmed number of ref_clk cycles
0	BYPASS_FLD	R/W	1h	Bypass the adapted loopback clock circuit

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5.7.2.60 OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register

5.7.2.60.1 OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register (Offset = 14h) [reset = 101002h]

This register allows the user to define the memory organization of using Flash Devices. This register should be setup while the controller is idle.

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Table 5-1343. Instance Table

Instance Name	Physical Address
FSS0	5380 8014h

Figure 5-657. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
DEV_SIZE_RESV_FLD			MEM_SIZE_ON_CS3_FLD		MEM_SIZE_ON_CS2_FLD		MEM_SIZE_ON_CS1_FLD
R			R/W		R/W		R/W
0h			0h		0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MEM_SIZE_ON_CS1_FLD	MEM_SIZE_ON_CS0_FLD		BYTES_PER_SUBSECTOR_FLD				
R/W	R/W		R/W				
0h	0h		10h				
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BYTES_PER_DEVICE_PAGE_FLD							
R/W							
100h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BYTES_PER_DEVICE_PAGE_FLD				NUM_ADDR_BYTES_FLD			
R/W				R/W			
100h				2h			

Table 5-1344. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	DEV_SIZE_RESV_FLD	R	0h	Reserved
28:27	MEM_SIZE_ON_CS3_FLD	R/W	0h	Size of Flash Device connected to CS[3] pin: Value 00 : size of 512Mb. Value 01 : size of 1Gb. Value 10 : size of 2Gb. Value 11 : size of 4Gb.
26:25	MEM_SIZE_ON_CS2_FLD	R/W	0h	Size of Flash Device connected to CS[2] pin: Value 00 : size of 512Mb. Value 01 : size of 1Gb. Value 10 : size of 2Gb. Value 11 : size of 4Gb.
24:23	MEM_SIZE_ON_CS1_FLD	R/W	0h	Size of Flash Device connected to CS[1] pin: Value 00 : size of 512Mb. Value 01 : size of 1Gb. Value 10 : size of 2Gb. Value 11 : size of 4Gb.
22:21	MEM_SIZE_ON_CS0_FLD	R/W	0h	Size of Flash Device connected to CS[0] pin: Value 00 : size of 512Mb. Value 01 : size of 1Gb. Value 10 : size of 2Gb. Value 11 : size of 4Gb.

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Table 5-1344. OSPI_FLASH_CFG_DEV_SIZE_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20:16	BYTES_PER_SUBSECTOR_FLD	R/W	10h	Number of bytes per Block. This is required by the controller for performing the write protection logic. The number of bytes per block must be a power of 2 number.
15:4	BYTES_PER_DEVICE_PAGE_FLD	R/W	100h	Number of bytes per device page. This is required by the controller for performing FLASH writes up to and across page boundaries.
3:0	NUM_ADDR_BYTES_FLD	R/W	2h	Number of address bytes. A value of 0 indicates 1 byte.

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5.7.2.61 OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register

5.7.2.61.1 OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register (Offset = 18h) [reset = 80h]

This register allows the user to allocate the SRAM area for indirect writes and reads. N in this register is the SRAM depth, configured in the cdns_ospi_flash_ctrl_defs_default.v. The default value of N is 8 what assumes that external SRAM hard macro has 2**8=256 memory locations with fixed data size of 32 bits. This register should be setup while the controller is idle.

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Table 5-1345. Instance Table

Instance Name	Physical Address
FSS0	5380 8018h

Figure 5-658. OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Name Register

31	30	29	28	27	26	25	24
SRAM_PARTITION_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
SRAM_PARTITION_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
SRAM_PARTITION_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
80h							

Table 5-1346. OSPI_FLASH_CFG_SRAM_PARTITION_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	SRAM_PARTITION_RESV_FLD	R	0h	Reserved
7:0	ADDR_FLD	R/W	80h	Indirect Read Partition Size: Defines the size of the indirect read partition in the SRAM, in units of SRAM locations. By default, half of the SRAM is reserved for indirect read operation, and half for indirect write. The size of this register will scale with the depth of the SRAM.

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5.7.2.62 OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register

5.7.2.62.1 OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register (Offset = 1Ch) [reset = 0h]

This register allows the user to define the address distinguishing DAC access from triggered INDAC one. This register should be setup while the controller is idle.

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Table 5-1347. Instance Table

Instance Name	Physical Address
FSS0	5380 801Ch

Figure 5-659. OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 5-1348. OSPI_FLASH_CFG_IND_AHB_ADDR_TRIGGER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	This is the base address that will be used by the AHB controller. When the incoming AHB read access address matches a range of addresses from this trigger address to the trigger address + 15, then the AHB request will be completed by fetching data from the Indirect Controllers SRAM.

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5.7.2.63 OSPI_FLASH_CFG_REMAP_ADDR_REG Register

5.7.2.63.1 OSPI_FLASH_CFG_REMAP_ADDR_REG Register (Offset = 24h) [reset = 0h]

This register allows the user to define the address offset for DAC accesses. This register should be setup while the controller is idle.

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Table 5-1349. Instance Table

Instance Name	Physical Address
FSS0	5380 8024h

Figure 5-660. OSPI_FLASH_CFG_REMAP_ADDR_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 5-1350. OSPI_FLASH_CFG_REMAP_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	This register is used to remap an incoming AHB address to a different address used by the FLASH device.

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5.7.2.64 OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register

5.7.2.64.1 OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register (Offset = 28h) [reset = 200h]

This register allows the user to define the mode bits for corresponding Flash Device. It also provides configuration for CRC aware SPI transfers. This register should be setup while the controller is idle.

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Table 5-1351. Instance Table

Instance Name	Physical Address
FSS0	5380 8028h

Figure 5-661. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Name Register

31	30	29	28	27	26	25	24
RX_CRC_DATA_LOW_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_CRC_DATA_UP_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_OUT_ENABLE_FLD	MODE_BIT_RESV1_FLD				CHUNK_SIZE_FLD		
R/W	R				R/W		
0h	0h				2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MODE_FLD							
R/W							
0h							

Table 5-1352. OSPI_FLASH_CFG_MODE_BIT_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RX_CRC_DATA_LOW_FLD	R	0h	RX CRC data [lower] The first CRC byte returned after RX data chunk.
23:16	RX_CRC_DATA_UP_FLD	R	0h	RX CRC data [upper] The second CRC byte returned after RX data chunk.
15	CRC_OUT_ENABLE_FLD	R/W	0h	CRC# output enable bit When enabled, the controller expects the Flash Device to toggle CRC data on both SPI clock edges in CRC->CRC# sequence and calculates CRC compliance accordingly.
14:11	MODE_BIT_RESV1_FLD	R	0h	Reserved
10:8	CHUNK_SIZE_FLD	R/W	2h	It defines size of chunk after which CRC data is expected to show up on the SPI interface for write and read data transfers.
7:0	MODE_FLD	R/W	0h	These are the 8 mode bits that are sent to the device following the address bytes if mode bit transmission has been enabled.

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5.7.2.65 OSPI_FLASH_CFG_SRAM_FILL_REG Register

5.7.2.65.1 OSPI_FLASH_CFG_SRAM_FILL_REG Register (Offset = 2Ch) [reset = 0h]

This register keeps the values of current fill levels of both SRAM partitions.

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Table 5-1353. Instance Table

Instance Name	Physical Address
FSS0	5380 802Ch

Figure 5-662. OSPI_FLASH_CFG_SRAM_FILL_REG Name Register

31	30	29	28	27	26	25	24
SRAM_FILL_INDAC_WRITE_FLD							
R							
0h							
23	22	21	20	19	18	17	16
SRAM_FILL_INDAC_WRITE_FLD							
R							
0h							
15	14	13	12	11	10	9	8
SRAM_FILL_INDAC_READ_FLD							
R							
0h							
7	6	5	4	3	2	1	0
SRAM_FILL_INDAC_READ_FLD							
R							
0h							

Table 5-1354. OSPI_FLASH_CFG_SRAM_FILL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SRAM_FILL_INDAC_WRITE_FLD	R	0h	SRAM Fill Level [Indirect Write Partition]: Identifies the current fill level of the SRAM Indirect Write partition
15:0	SRAM_FILL_INDAC_READ_FLD	R	0h	SRAM Fill Level [Indirect Read Partition]: Identifies the current fill level of the SRAM Indirect Read partition

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5.7.2.66 OSPI_FLASH_CFG_TX_THRESH_REG Register

5.7.2.66.1 OSPI_FLASH_CFG_TX_THRESH_REG Register (Offset = 30h) [reset = 1h]

This register allows the user to define the TX FIFO level arousing the corresponding interrupt. This register should be setup while the controller is idle.

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Table 5-1355. Instance Table

Instance Name	Physical Address
FSS0	5380 8030h

Figure 5-663. OSPI_FLASH_CFG_TX_THRESH_REG Name Register

31	30	29	28	27	26	25	24
TX_THRESH_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
TX_THRESH_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
TX_THRESH_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
TX_THRESH_RESV_FLD			LEVEL_FLD				
R			R/W				
0h			1h				

Table 5-1356. OSPI_FLASH_CFG_TX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	TX_THRESH_RESV_FLD	R	0h	Reserved
4:0	LEVEL_FLD	R/W	1h	Defines the level at which the small TX FIFO not full interrupt is generated

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5.7.2.67 OSPI_FLASH_CFG_RX_THRESH_REG Register

5.7.2.67.1 OSPI_FLASH_CFG_RX_THRESH_REG Register (Offset = 34h) [reset = 1h]

This register allows the user to define the RX FIFO level arousing the corresponding interrupt. This register should be setup while the controller is idle.

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Table 5-1357. Instance Table

Instance Name	Physical Address
FSS0	5380 8034h

Figure 5-664. OSPI_FLASH_CFG_RX_THRESH_REG Name Register

31	30	29	28	27	26	25	24
RX_THRESH_RESV_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RX_THRESH_RESV_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RX_THRESH_RESV_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_THRESH_RESV_FLD			LEVEL_FLD				
R			R/W				
0h			1h				

Table 5-1358. OSPI_FLASH_CFG_RX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:5	RX_THRESH_RESV_FLD	R	0h	Reserved
4:0	LEVEL_FLD	R/W	1h	Defines the level at which the small RX FIFO not empty interrupt is generated

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5.7.2.68 OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register

5.7.2.68.1 OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register (Offset = 38h) [reset = 10005h]

This register defines how the controller will poll the device following a write transfer. By default it is set to poll bit 0 of the device STATUS register (using opcode 0x05), which is common across all devices to indicate WRITE IN PROGRESS (or WIP).

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Table 5-1359. Instance Table

Instance Name	Physical Address
FSS0	5380 8038h

Figure 5-665. OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Name Register

31	30	29	28	27	26	25	24
POLL_REP_DELAY_FLD							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
POLL_COUNT_FLD							
R/W							
1h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ENABLE_POLLING_EXP_FLD	DISABLE_POLLING_FLD	POLLING_POLARITY_FLD	WR_COMP_CTRL_RESV1_FLD		POLLING_BIT_INDEX_FLD		
R/W	R/W	R/W	R		R/W		
0h	0h	0h	0h		0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OPCODE_FLD							
R/W							
5h							

Table 5-1360. OSPI_FLASH_CFG_WRITE_COMPLETION_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	POLL_REP_DELAY_FLD	R/W	0h	Defines additional delay for maintain Chip Select de-asserted during auto-polling phase
23:16	POLL_COUNT_FLD	R/W	1h	Defines the number of times the controller should expect to see a true result from the polling in successive reads of the device register.
15	ENABLE_POLLING_EXP_FLD	R/W	0h	Set to '1' for enabling auto-polling expiration.
14	DISABLE_POLLING_FLD	R/W	0h	This switches off the automatic polling function
13	POLLING_POLARITY_FLD	R/W	0h	Defines the polling polarity. If '1', then the write transfer to the device will be complete if the polled bit is equal to '1'. If '0', then the write transfer to the device will be complete if the polled bit is equal to '0'.
12:11	WR_COMP_CTRL_RESV1_FLD	R	0h	Reserved
10:8	POLLING_BIT_INDEX_FLD	R/W	0h	Defines the bit index that should be polled. A value of 010 means that bit 2 of the returned data will be polled for.A value of 111 means that bit 7 of the returned data will be polled for.
7:0	OPCODE_FLD	R/W	5h	Defines the opcode that should be issued by the controller when it is automatically polling for device program completion. This command is issued followed all device write operations. By default, this will poll the standard device STATUS register using opcode 0x05

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5.7.2.69 OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register

5.7.2.69.1 OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register (Offset = 3Ch) [reset = FFFFFFFFh]

This register defines maximum number of poll cycles. If the expected value of the bit being polled is not gotten after number defined in this register, the auto-polling is done on the next phase.

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Table 5-1361. Instance Table

Instance Name	Physical Address
FSS0	5380 803Ch

Figure 5-666. OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Name Register

31	30	29	28	27	26	25	24
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NO_OF_POLLS_BEF_EXP_FLD							
R/W							
FFFFFFFFh							

Table 5-1362. OSPI_FLASH_CFG_NO_OF_POLLS_BEF_EXP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	NO_OF_POLLS_BEF_EXP_FLD	R/W	FFFFFFFFh	Number of polls cycles before expiration

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5.7.2.70 OSPI_FLASH_CFG_IRQ_STATUS_REG Register

5.7.2.70.1 OSPI_FLASH_CFG_IRQ_STATUS_REG Register (Offset = 40h) [reset = 0h]

Interrupt Status Register: The status fields in this register are set when the described event occurs and the interrupt is enabled in the mask register. When any of these bit fields are set, the interrupt output is asserted high. The fields are each cleared by writing a 1 to the field. Note that bit fields 6 thru 10 are only valid when legacy SPI mode is active.

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Table 5-1363. Instance Table

Instance Name	Physical Address
FSS0	5380 8040h

Figure 5-667. OSPI_FLASH_CFG_IRQ_STATUS_REG Name Register

31	30	29	28	27	26	25	24
IRQ_STAT_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IRQ_STAT_RESV_FLD				ECC_FAIL_FLD	TX_CRC_CHUNK_BRK_FLD	RX_CRC_DATA_VAL_FLD	RX_CRC_DATA_ERR_FLD
R				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
IRQ_STAT_RESV1_FLD	STIG_REQ_INT_FLD	POLL_EXP_INT_FLD	INDRD_SRAM_FULL_FLD	RX_FIFO_FULL_FLD	RX_FIFO_NOT_EMPTY_FLD	TX_FIFO_FULL_FLD	TX_FIFO_NOT_FULL_FLD
R	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RECV_OVERFLOW_FLD	INDIRECT_XFER_LEVEL_BREACH_FLD	ILLEGAL_ACCESS_DET_FLD	PROT_WR_ATTEMPT_FLD	INDIRECT_READ_REJECT_FLD	INDIRECT_OP_DONE_FLD	UNDERFLOW_DET_FLD	MODE_M_FAIL_FLD
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1364. OSPI_FLASH_CFG_IRQ_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	IRQ_STAT_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_FLD	R/W1TC	0h	ECC failure This interrupt informs the system that Flash Device reported ECC error.
18	TX_CRC_CHUNK_BRK_FLD	R/W1TC	0h	TX CRC chunk was broken This interrupt informs the system that program page SPI transfer was discontinued somewhere inside the chunk.
17	RX_CRC_DATA_VAL_FLD	R/W1TC	0h	RX CRC data valid New RX CRC data was captured from Flash Device
16	RX_CRC_DATA_ERR_FLD	R/W1TC	0h	RX CRC data error CRC data from Flash Device does not correspond to the one dynamically calculated by the controller.
15	IRQ_STAT_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_INT_FLD	R/W1TC	0h	The controller is ready for getting another STIG request.
13	POLL_EXP_INT_FLD	R/W1TC	0h	The maximum number of programmed polls cycles is expired
12	INDRD_SRAM_FULL_FLD	R/W1TC	0h	Indirect Read Partition overflow: Indirect Read Partition of SRAM is full and unable to immediately complete indirect operation

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Table 5-1364. OSPI_FLASH_CFG_IRQ_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RX_FIFO_FULL_FLD	R/W1TC	0h	Small RX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO is not full 1 : FIFO is full
10	RX_FIFO_NOT_EMPTY_FLD	R/W1TC	0h	Small RX FIFO not empty: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO has less than RX THRESHOLD entries, 1 : FIFO has >= THRESHOLD entries
9	TX_FIFO_FULL_FLD	R/W1TC	0h	Small TX FIFO full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO is not full, 1 : FIFO is full
8	TX_FIFO_NOT_FULL_FLD	R/W1TC	0h	Small TX FIFO not full: Current FIFO status can be ignored in non-SPI legacy mode 0 : FIFO has >= THRESHOLD entries, 1 : FIFO has less than THRESHOLD entries
7	RECV_OVERFLOW_FLD	R/W1TC	0h	Receive Overflow: This should only occur in Legacy SPI mode. Set if an attempt is made to push the RX FIFO when it is full. This bit is reset only by a system reset and cleared only when this register is read. If a new push to the RX FIFO occurs coincident with a register read this flag will remain set. 0 : no overflow has been detected. 1 : an overflow has occurred.
6	INDIRECT_XFER_LEVEL_BREACH_FLD	R/W1TC	0h	Indirect Transfer Watermark Level Breached
5	ILLEGAL_ACCESS_DET_FLD	R/W1TC	0h	Illegal AHB access has been detected. AHB wrapping bursts and the use of SPLIT/RETRY accesses will cause this error interrupt to trigger.
4	PROT_WR_ATTEMPT_FLD	R/W1TC	0h	Write to protected area was attempted and rejected.
3	INDIRECT_READ_REJECT_FLD	R/W1TC	0h	Indirect operation was requested but could not be accepted. Two indirect operations already in storage.
2	INDIRECT_OP_DONE_FLD	R/W1TC	0h	Indirect Operation Complete: Controller has completed last triggered indirect operation
1	UNDERFLOW_DET_FLD	R/W1TC	0h	Underflow Detected: 0 : no underflow has been detected 1 : underflow is detected and an attempt to transfer data is made when the small TX FIFO is empty. This may occur when AHB write data is being supplied too slowly to keep up with the requested write operation This bit is reset only by a system reset and cleared only when the register is read.
0	MODE_M_FAIL_FLD	R/W1TC	0h	Mode M Failure: Mode M failure indicates the voltage on pin n_ss_in is inconsistent with the SPI mode. Set =1 if n_ss_in is low in master mode [multi-master contention]. These conditions will clear the spi_enable bit and disable the SPI. This bit is reset only by a system reset and cleared only when this register is read. 0 : no mode fault has been detected 1 : a mode fault has occurred

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5.7.2.71 OSPI_FLASH_CFG_IRQ_MASK_REG Register

5.7.2.71.1 OSPI_FLASH_CFG_IRQ_MASK_REG Register (Offset = 44h) [reset = 0h]

Interrupt Mask: 0 : the interrupt for the corresponding interrupt status register bit is disabled.
1 : the interrupt for the corresponding interrupt status register bit is enabled.

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Table 5-1365. Instance Table

Instance Name	Physical Address
FSS0	5380 8044h

Figure 5-668. OSPI_FLASH_CFG_IRQ_MASK_REG Name Register

31	30	29	28	27	26	25	24
IRQ_MASK_RESV_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
IRQ_MASK_RESV_FLD				ECC_FAIL_MASK_FLD	TX_CRC_CHUNK_BRK_MASK_FLD	RX_CRC_DATA_VAL_MASK_FLD	RX_CRC_DATA_ERR_MASK_FLD
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
IRQ_MASK_RESV1_FLD	STIG_REQ_MASK_FLD	POLL_EXP_INT_MASK_FLD	INDRD_SRAM_FULL_MASK_FLD	RX_FIFO_FULL_MASK_FLD	RX_FIFO_NOT_EMPTY_MASK_FLD	TX_FIFO_FULL_MASK_FLD	TX_FIFO_NOT_FULL_MASK_FLD
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RECV_OVERFLOW_MASK_FLD	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	ILLEGAL_ACCESS_DET_MASK_FLD	PROT_WR_ATTEMPT_MASK_FLD	INDIRECT_READ_REJECT_MASK_FLD	INDIRECT_OP_DONE_MASK_FLD	UNDERFLOW_DET_MASK_FLD	MODE_M_FAIL_MASK_FLD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1366. OSPI_FLASH_CFG_IRQ_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	IRQ_MASK_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_MASK_FLD	R/W	0h	ECC failure Mask
18	TX_CRC_CHUNK_BRK_MASK_FLD	R/W	0h	TX CRC chunk was broken Mask
17	RX_CRC_DATA_VAL_MASK_FLD	R/W	0h	RX CRC data valid Mask
16	RX_CRC_DATA_ERR_MASK_FLD	R/W	0h	RX CRC data error Mask
15	IRQ_MASK_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_MASK_FLD	R/W	0h	STIG request completion Mask
13	POLL_EXP_INT_MASK_FLD	R/W	0h	Polling expiration detected Mask
12	INDRD_SRAM_FULL_MASK_FLD	R/W	0h	Indirect Read Partition overflow mask
11	RX_FIFO_FULL_MASK_FLD	R/W	0h	Small RX FIFO full Mask

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Table 5-1366. OSPI_FLASH_CFG_IRQ_MASK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX_FIFO_NOT_EMPTY_MASK_FLD	R/W	0h	Small RX FIFO not empty Mask
9	TX_FIFO_FULL_MASK_FLD	R/W	0h	Small TX FIFO full Mask
8	TX_FIFO_NOT_FULL_MASK_FLD	R/W	0h	Small TX FIFO not full Mask
7	RECV_OVERFLOW_MASK_FLD	R/W	0h	Receive Overflow Mask
6	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	R/W	0h	Transfer Watermark Breach Mask
5	ILLEGAL_ACCESS_DET_MASK_FLD	R/W	0h	Illegal Access Detected Mask
4	PROT_WR_ATTEMPT_MASK_FLD	R/W	0h	Protected Area Write Attempt Mask
3	INDIRECT_READ_REJECT_MASK_FLD	R/W	0h	Indirect Read Reject Mask
2	INDIRECT_OP_DONE_MASK_FLD	R/W	0h	Indirect Complete Mask
1	UNDERFLOW_DET_MASK_FLD	R/W	0h	Underflow Detected Mask
0	MODE_M_FAIL_MASK_FLD	R/W	0h	Mode M Failure Mask

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5.7.2.72 OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register

5.7.2.72.1 OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register (Offset = 50h) [reset = 0h]

This register allows the user to define lower boundary of the write protection area. This register should be setup while the controller is idle.

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Table 5-1367. Instance Table

Instance Name	Physical Address
FSS0	5380 8050h

Figure 5-669. OSPI_FLASH_CFG_LOWER_WR_PROT_REG Name Register

31	30	29	28	27	26	25	24
SUBSECTOR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
SUBSECTOR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
SUBSECTOR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
SUBSECTOR_FLD							
R/W							
0h							

Table 5-1368. OSPI_FLASH_CFG_LOWER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUBSECTOR_FLD	R/W	0h	The block number that defines the lower block in the range of blocks that is to be locked from Writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register.

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5.7.2.73 OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register

5.7.2.73.1 OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register (Offset = 54h) [reset = 0h]

Is register allows the user to define upper boundary of the write protection area. This register should be setup while the controller is idle.

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Table 5-1369. Instance Table

Instance Name	Physical Address
FSS0	5380 8054h

Figure 5-670. OSPI_FLASH_CFG_UPPER_WR_PROT_REG Name Register

31	30	29	28	27	26	25	24
SUBSECTOR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
SUBSECTOR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
SUBSECTOR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
SUBSECTOR_FLD							
R/W							
0h							

Table 5-1370. OSPI_FLASH_CFG_UPPER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SUBSECTOR_FLD	R/W	0h	The block number that defines the upper block in the range of blocks that is to be locked from Writing. The definition of a block in terms of number of bytes is programmable via the Device Size Configuration register.

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5.7.2.74 OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register

5.7.2.74.1 OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register (Offset = 58h) [reset = 0h]

This register allows the user to define the configuration of write protection settings. This register should be setup while the controller is idle.

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Table 5-1371. Instance Table

Instance Name	Physical Address
FSS0	5380 8058h

Figure 5-671. OSPI_FLASH_CFG_WR_PROT_CTRL_REG Name Register

31	30	29	28	27	26	25	24
WR_PROT_CTRL_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
WR_PROT_CTRL_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
WR_PROT_CTRL_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
WR_PROT_CTRL_RESV_FLD						ENB_FLD	INV_FLD
R						R/W	R/W
0h						0h	0h

Table 5-1372. OSPI_FLASH_CFG_WR_PROT_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	WR_PROT_CTRL_RESV_FLD	R	0h	Reserved
1	ENB_FLD	R/W	0h	Write Protection Enable Bit: When set to 1, any AHB write access with an address within the protection region defined in the lower and upper write protection registers is rejected. An AHB error response is generated and an interrupt source triggered. When set to 0, the protection region is disabled.
0	INV_FLD	R/W	0h	Write Protection Inversion Bit: When set to 1, the protection region defined in the lower and upper write protection registers is inverted meaning it is the region that the system is permitted to write to. When set to 0, the protection region defined in the lower and upper write protection registers is the region that the system is not permitted to write to.

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5.7.2.75 OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register

5.7.2.75.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register (Offset = 60h) [reset = 0h]

This register allows the user to control of the Indirect Read Transfer logic.

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Table 5-1373. Instance Table

Instance Name	Physical Address
FSS0	5380 8060h

Figure 5-672. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Name Register

31	30	29	28	27	26	25	24
INDIR_RD_XFER_RESV_FLD							
R							
0h							
23	22	21	20	19	18	17	16
INDIR_RD_XFER_RESV_FLD							
R							
0h							
15	14	13	12	11	10	9	8
INDIR_RD_XFER_RESV_FLD							
R							
0h							
7	6	5	4	3	2	1	0
NUM_IND_OPS_DONE_FLD		IND_OPS_DONE_STATUS_FLD	RD_QUEUED_FLD	SRAM_FULL_FLD	RD_STATUS_FLD	CANCEL_FLD	START_FLD
R		R/W1TC	R	R/W1TC	R	W	W
0h		0h	0h	0h	0h	0h	0h

Table 5-1374. OSPI_FLASH_CFG_INDIRECT_READ_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	INDIR_RD_XFER_RESV_FLD	R	0h	Reserved
7:6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field [bit 5]. It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1TC	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	RD_QUEUED_FLD	R	0h	Two indirect read operations have been queued
3	SRAM_FULL_FLD	R/W1TC	0h	SRAM Full: SRAM full and unable to immediately complete an indirect operation. Write a 1 to this field to clear it.; indirect operation [status]
2	RD_STATUS_FLD	R	0h	Indirect Read Status: Indirect read operation in progress [status]
1	CANCEL_FLD	W	0h	Cancel Indirect Read: Writing a 1 to this bit will cancel all ongoing indirect read operations.
0	START_FLD	W	0h	Start Indirect Read: Writing a 1 to this bit will trigger an indirect read operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect read operation.

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5.7.2.76 OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register

5.7.2.76.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register (Offset = 64h) [reset = 0h]

This register allows the user to define watermark level for Indirect read transfers. This register should be setup before an indirect read transfer is triggered.

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Table 5-1375. Instance Table

Instance Name	Physical Address
FSS0	5380 8064h

Figure 5-673. OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
LEVEL_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
LEVEL_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
LEVEL_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
LEVEL_FLD							
R/W							
0h							

Table 5-1376. OSPI_FLASH_CFG_INDIRECT_READ_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LEVEL_FLD	R/W	0h	Watermark Value: This represents the minimum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level passes the watermark, an interrupt is also generated. This field can be disabled by Writing a value of all zeroes.

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5.7.2.77 OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register

5.7.2.77.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register (Offset = 68h) [reset = 0h]

This register allows the user to define start address of indirect read transfer which is about to be triggered. This register should be setup before an indirect read transfer is triggered.

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Table 5-1377. Instance Table

Instance Name	Physical Address
FSS0	5380 8068h

Figure 5-674. OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 5-1378. OSPI_FLASH_CFG_INDIRECT_READ_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	This is the start address from which the indirect access will commence its READ operation.

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5.7.2.78 OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register

5.7.2.78.1 OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register (Offset = 6Ch) [reset = 0h]

This register allows the user to define number of bytes to be read of indirect read transfer which is about to be triggered. This register should be setup before an indirect read transfer is triggered.

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Table 5-1379. Instance Table

Instance Name	Physical Address
FSS0	5380 806Ch

Figure 5-675. OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 5-1380. OSPI_FLASH_CFG_INDIRECT_READ_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

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5.7.2.79 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register

5.7.2.79.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register (Offset = 70h) [reset = 0h]

This register allows the user to control of the Indirect Write Transfer logic.

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Table 5-1381. Instance Table

Instance Name	Physical Address
FSS0	5380 8070h

Figure 5-676. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Name Register

31	30	29	28	27	26	25	24
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INDIR_WR_XFER_RESV2_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_IND_OPS_DONE_FLD		IND_OPS_DONE_STATUS_FLD	WR_QUEUED_FLD	INDIR_WR_XFER_RESV1_FLD	WR_STATUS_FLD	CANCEL_FLD	START_FLD
R		R/W1TC	R	R	R	W	W
0h		0h	0h	0h	0h	0h	0h

Table 5-1382. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	INDIR_WR_XFER_RESV2_FLD	R	0h	Reserved
7:6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the indirect completion status field [bit 5]. It is incremented by hardware when an indirect operation has completed. Write a 1 to bit 5 of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1TC	0h	Indirect Completion Status: This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	WR_QUEUED_FLD	R	0h	Two indirect write operations have been queued
3	INDIR_WR_XFER_RESV1_FLD	R	0h	Reserved
2	WR_STATUS_FLD	R	0h	Indirect Write Status: Indirect write operation in progress [status]
1	CANCEL_FLD	W	0h	Cancel Indirect Write: Writing a 1 to this bit will cancel all ongoing indirect write operations.
0	START_FLD	W	0h	Start Indirect Write: Writing a 1 to this bit will trigger an indirect write operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect write operation.

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5.7.2.80 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register

5.7.2.80.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register (Offset = 74h) [reset = FFFFFFFFh]

This register allows the user to define watermark level for Indirect write transfers. This register should be setup before an indirect write transfer is triggered.

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Table 5-1383. Instance Table

Instance Name	Physical Address
FSS0	5380 8074h

Figure 5-677. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Name Register

31	30	29	28	27	26	25	24
LEVEL_FLD							
R/W							
FFFFFFFFh							
23	22	21	20	19	18	17	16
LEVEL_FLD							
R/W							
FFFFFFFFh							
15	14	13	12	11	10	9	8
LEVEL_FLD							
R/W							
FFFFFFFFh							
7	6	5	4	3	2	1	0
LEVEL_FLD							
R/W							
FFFFFFFFh							

Table 5-1384. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	LEVEL_FLD	R/W	FFFFFFFFh	Watermark Value: This represents the maximum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level falls below the watermark, an interrupt is also generated. This field can be disabled by Writing a value of all ones.

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5.7.2.81 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register

5.7.2.81.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register (Offset = 78h) [reset = 0h]

This register allows the user to define start address of indirect write transfer which is about to be triggered. This register should be setup before an indirect write transfer is triggered.

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Table 5-1385. Instance Table

Instance Name	Physical Address
FSS0	5380 8078h

Figure 5-678. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 5-1386. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	Start of Indirect Access: This is the start address from which the indirect access will commence its READ operation.

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5.7.2.82 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register

5.7.2.82.1 OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register (Offset = 7Ch) [reset = 0h]

This register allows the user to define number of bytes to be written of indirect read transfer which is about to be triggered. This register should be setup before an indirect read transfer is triggered.

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Table 5-1387. Instance Table

Instance Name	Physical Address
FSS0	5380 807Ch

Figure 5-679. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Name Register

31	30	29	28	27	26	25	24
VALUE_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
VALUE_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
VALUE_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
VALUE_FLD							
R/W							
0h							

Table 5-1388. OSPI_FLASH_CFG_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VALUE_FLD	R/W	0h	Indirect Number of Bytes: This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

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5.7.2.83 OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register

5.7.2.83.1 OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register (Offset = 80h) [reset = 4h]

This register allows the user to define the indirect trigger address range. If the configured range exceeds number of bytes programmed for particular indirect transfer, there is no need to detect indirect trigger address boundaries by software. This register should be setup before an indirect read transfer is triggered.

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Table 5-1389. Instance Table

Instance Name	Physical Address
FSS0	5380 8080h

Figure 5-680. OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Name Register

31	30	29	28	27	26	25	24
IND_RANGE_RESV1_FLD							
R							
0h							
23	22	21	20	19	18	17	16
IND_RANGE_RESV1_FLD							
R							
0h							
15	14	13	12	11	10	9	8
IND_RANGE_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
IND_RANGE_RESV1_FLD				IND_RANGE_WIDTH_FLD			
R				R/W			
0h				4h			

Table 5-1390. OSPI_FLASH_CFG_INDIRECT_TRIGGER_ADDR_RANGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	IND_RANGE_RESV1_FLD	R	0h	Reserved
3:0	IND_RANGE_WIDTH_FLD	R/W	4h	This is the address offset of Indirect Trigger Address Register.

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5.7.2.84 OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register

5.7.2.84.1 OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register (Offset = 8Ch) [reset = 0h]

This register controls the Memory Bank accesses. It also defines the number of bytes intended to get by STIG access configured to use the STIG Memory Bank.

Return to Summary Table

Table 5-1391. Instance Table

Instance Name	Physical Address
FSS0	5380 808Ch

Figure 5-681. OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">FLASH_COMMAND_CTRL_MEM_RESV1_FLD</td><td colspan="5">MEM_BANK_ADDR_FLD</td></tr>
<tr><td colspan="3">R</td><td colspan="5">R/W</td></tr>
<tr><td colspan="3">0h</td><td colspan="5">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">MEM_BANK_ADDR_FLD</td><td>FLASH_COMMAND_CTRL_MEM_RESV2_FLD</td><td colspan="3">NB_OF_STIG_READ_BYTES_FLD</td></tr>
<tr><td colspan="4">R/W</td><td>R</td><td colspan="3">R/W</td></tr>
<tr><td colspan="4">0h</td><td>0h</td><td colspan="3">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">MEM_BANK_READ_DATA_FLD</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">FLASH_COMMAND_CTRL_MEM_RESV3_FLD</td><td>MEM_BANK_REQ_IN_PROGRESS_FLD</td><td>TRIGGER_MEM_BANK_REQ_FLD</td></tr>
<tr><td colspan="6">R</td><td>R</td><td>W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-1392. OSPI_FLASH_CFG_FLASH_COMMAND_CTRL_MEM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	FLASH_COMMAND_CTRL_MEM_RESV1_FLD	R	0h	Reserved
28:20	MEM_BANK_ADDR_FLD	R/W	0h	The address of the Memory Bank which data will be read from.
19	FLASH_COMMAND_CTRL_MEM_RESV2_FLD	R	0h	Reserved
18:16	NB_OF_STIG_READ_BYTES_FLD	R/W	0h	It defines the number of read bytes for the extended STIG.
15:8	MEM_BANK_READ_DATA_FLD	R	0h	Last requested data from the STIG Memory Bank.
7:2	FLASH_COMMAND_CTRL_MEM_RESV3_FLD	R	0h	Reserved
1	MEM_BANK_REQ_IN_PROGRESS_FLD	R	0h	Memory Bank data request in progress.
0	TRIGGER_MEM_BANK_REQ_FLD	W	0h	Trigger the Memory Bank data request.

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5.7.2.85 OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register

5.7.2.85.1 OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register (Offset = 90h) [reset = 0h]

This register controls SPI transactions generated by STIG. It allows the user to define corresponding SPI frame to particular command, triggering the transfer and polling for its completion.

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Table 5-1393. Instance Table

Instance Name	Physical Address
FSS0	5380 8090h

Figure 5-682. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Name Register

31	30	29	28	27	26	25	24
CMD_OPCODE_FLD							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ENB_READ_DATA_FLD	NUM_RD_DATA_BYTES_FLD			ENB_COMD_ADDR_FLD	ENB_MODE_BIT_FLD	NUM_ADDR_BYTES_FLD	
R/W	R/W			R/W	R/W	R/W	
0h	0h			0h	0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ENB_WRITE_DATA_FLD	NUM_WR_DATA_BYTES_FLD			NUM_DUMMY_CYCLES_FLD			
R/W	R/W			R/W			
0h	0h			0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_DUMMY_CYCLES_FLD	FLASH_CMD_CTRL_RESV1_FLD				STIG_MEM_BANK_EN_FLD	CMD_EXEC_STATUS_FLD	CMD_EXEC_FLD
R/W	R				R/W	R	W
0h	0h				0h	0h	0h

Table 5-1394. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	CMD_OPCODE_FLD	R/W	0h	Command Opcode: The command opcode field should be setup before triggering the command. For example, 0x20 maps to SubSector Erase. Writing to the execute field [bit 0] of this register launches the command. NOTE : Using this approach to issue commands to the device will make use of the instruction type of the device instruction configuration register. If this field is set to 2'b00, then the command opcode, command address, command dummy bytes and command data will all be transferred in a serial fashion. If this field is set to 2'b01, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0 and DQ1 pins. If this field is set to 2'b10, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0, DQ1, DQ2 and DQ3 pins.
23	ENB_READ_DATA_FLD	R/W	0h	Read Data Enable: Set to 1 if the command specified in the command opcode field [bits 31:24] requires read data bytes to be received from the device.
22:20	NUM_RD_DATA_BYTES_FLD	R/W	0h	Number of Read Data Bytes: Up to 8 data bytes may be read using this command. Set to 0 for 1 byte and 7 for 8 bytes.
19	ENB_COMD_ADDR_FLD	R/W	0h	Command Address Enable: Set to 1 if the command specified in bits 31:24 requires an address. This should be setup before triggering the command via Writing a 1 to the execute field.

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Table 5-1394. OSPI_FLASH_CFG_FLASH_CMD_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	ENB_MODE_BIT_FLD	R/W	0h	Mode Bit Enable: Set to 1 to ensure the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
17:16	NUM_ADDR_BYTES_FLD	R/W	0h	Number of Address Bytes: Set to the number of address bytes required [the address itself is programmed in the FLASH COMMAND ADDRESS REGISTERS]. This should be setup before triggering the command via bit 0 of this register. 2'b00 : 1 address byte 2'b01 : 2 address bytes 2'b10 : 3 address bytes 2'b11 : 4 address bytes
15	ENB_WRITE_DATA_FLD	R/W	0h	Write Data Enable: Set to 1 if the command specified in the command opcode field requires write data bytes to be sent to the device.
14:12	NUM_WR_DATA_BYTES_FLD	R/W	0h	Number of Write Data Bytes: Up to 8 Data bytes may be written using this command Set to 0 for 1 byte, 7 for 8 bytes.
11:7	NUM_DUMMY_CYCLES_FLD	R/W	0h	Number of Dummy cycles: Set to the number of dummy cycles required. This should be setup before triggering the command via the execute field of this register.
6:3	FLASH_CMD_CTRL_RESV1_FLD	R	0h	Reserved
2	STIG_MEM_BANK_EN_FLD	R/W	0h	STIG Memory Bank enable bit.
1	CMD_EXEC_STATUS_FLD	R	0h	Command execution in progress.
0	CMD_EXEC_FLD	W	0h	Execute the command.

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5.7.2.86 OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register

5.7.2.86.1 OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register (Offset = 94h) [reset = 0h]

This register allows the user to define the address of the command using by the STIG controller. This register should be setup while the controller is idle.

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Table 5-1395. Instance Table

Instance Name	Physical Address
FSS0	5380 8094h

Figure 5-683. OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Name Register

31	30	29	28	27	26	25	24
ADDR_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
ADDR_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
ADDR_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
ADDR_FLD							
R/W							
0h							

Table 5-1396. OSPI_FLASH_CFG_FLASH_CMD_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADDR_FLD	R/W	0h	Command Address: This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the address used by the command specified in the opcode field [bits 31:24] of the Flash Command Control register.

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5.7.2.87 OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register

5.7.2.87.1 OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register (Offset = A0h) [reset = 0h]

This register keeps the last 4 bytes read by STIG SPI access.

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Table 5-1397. Instance Table

Instance Name	Physical Address
FSS0	5380 80A0h

Figure 5-684. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R							
0h							

Table 5-1398. OSPI_FLASH_CFG_FLASH_RD_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R	0h	This is the data that is returned by the flash device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

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5.7.2.88 OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register

5.7.2.88.1 OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register (Offset = A4h) [reset = 0h]

This register keeps the last but 4 bytes read by STIG SPI access. This register in conjunction with the Flash Command Read Data Register (Lower) enables the controller to keep 8 last bytes read from the Flash Device using STIG.

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Table 5-1399. Instance Table

Instance Name	Physical Address
FSS0	5380 80A4h

Figure 5-685. OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R							
0h							

Table 5-1400. OSPI_FLASH_CFG_FLASH_RD_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R	0h	This is the data that is returned by the FLASH device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

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5.7.2.89 OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register

5.7.2.89.1 OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register (Offset = A8h) [reset = 0h]

This register takes the first 4 bytes to be written by STIG.

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Table 5-1401. Instance Table

Instance Name	Physical Address
FSS0	5380 80A8h

Figure 5-686. OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R/W							
0h							

Table 5-1402. OSPI_FLASH_CFG_FLASH_WR_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R/W	0h	Command Write Data Lower Byte: This is the command write data lower byte. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register.

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5.7.2.90 OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register

5.7.2.90.1 OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register (Offset = ACh) [reset = 0h]

This register takes the bytes ranging from 5 to 8 to be written by STIG.

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Table 5-1403. Instance Table

Instance Name	Physical Address
FSS0	5380 80ACh

Figure 5-687. OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DATA_FLD							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA_FLD							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA_FLD							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA_FLD							
R/W							
0h							

Table 5-1404. OSPI_FLASH_CFG_FLASH_WR_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA_FLD	R/W	0h	Command Write Data Upper Byte: This is the command write data upper byte. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the Flash Command Control register.

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5.7.2.91 OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register

5.7.2.91.1 OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register (Offset = B0h) [reset = 0h]

This register provides auto-polling data. It acts as the extension for the Write Completion Control Register where full status is not available and any action can be taken only relying on the indication of single bit being polled for.

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Table 5-1405. Instance Table

Instance Name	Physical Address
FSS0	5380 80B0h

Figure 5-688. OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Name Register

31	30	29	28	27	26	25	24
DEVICE_STATUS_RSVD_FLD2							
R							
0h							
23	22	21	20	19	18	17	16
DEVICE_STATUS_RSVD_FLD2				DEVICE_STATUS_NB_DUMMY			
R				R/W			
0h				0h			
15	14	13	12	11	10	9	8
DEVICE_STATUS_RSVD_FLD1							DEVICE_STATUS_VALID_FLD
R							R
0h							0h
7	6	5	4	3	2	1	0
DEVICE_STATUS_FLD							
R							
0h							

Table 5-1406. OSPI_FLASH_CFG_POLLING_FLASH_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	DEVICE_STATUS_RSVD_FLD2	R	0h	Reserved
19:16	DEVICE_STATUS_NB_DUMMY	R/W	0h	Number of dummy cycles for auto-polling
15:9	DEVICE_STATUS_RSVD_FLD1	R	0h	Reserved
8	DEVICE_STATUS_VALID_FLD	R	0h	Device Status Valid: This should be set when value in bits from 7 to 0 is valid.
7:0	DEVICE_STATUS_FLD	R	0h	Defines actual Status Register of Device

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5.7.2.92 OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register

5.7.2.92.1 OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register (Offset = B4h) [reset = 40000000h]

PHY Configuration Register.

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Table 5-1407. Instance Table

Instance Name	Physical Address
FSS0	5380 80B4h

Figure 5-689. OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Name Register

31	30	29	28	27	26	25	24
PHY_CONFIG_RESYNC_FLD	PHY_CONFIG_RESET_FLD	PHY_CONFIG_RX_DLL_BYPASS_FLD	PHY_CONFIG_RESV2_FLD				
W	W	R/W	R				
0h	1h	0h	0h				
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_CONFIG_RESV2_FLD	PHY_CONFIG_TX_DLL_DELAY_FLD						
R	R/W						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_CONFIG_RESV1_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_CONFIG_RESV1_FLD	PHY_CONFIG_RX_DLL_DELAY_FLD						
R	R/W						
0h	0h						

Table 5-1408. OSPI_FLASH_CFG_PHY_CONFIGURATION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_CONFIG_RESYNC_FLD	W	0h	This bit is used for re-synchronisation delay lines to update them with values from TX DLL Delay and RX DLL Delay fields.
30	PHY_CONFIG_RESET_FLD	W	1h	DLL Reset bit: This bit is used for reset of Delay Lines by software.
29	PHY_CONFIG_RX_DLL_BYPASS_FLD	R/W	0h	RX DLL Bypass: This field determines id RX DLL is bypassed.
28:23	PHY_CONFIG_RESV2_FLD	R	0h	Reserved
22:16	PHY_CONFIG_TX_DLL_DELAY_FLD	R/W	0h	TX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and spi_clk.
15:7	PHY_CONFIG_RESV1_FLD	R	0h	Reserved
6:0	PHY_CONFIG_RX_DLL_DELAY_FLD	R/W	0h	RX DLL Delay: This field determines the number of delay elements to insert on data path between ref_clk and rx_dll_clk.

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5.7.2.93 OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register

5.7.2.93.1 OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register (Offset = B8h) [reset = 800000h]

PHY DLL Master Control Register.

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Table 5-1409. Instance Table

Instance Name	Physical Address
FSS0	5380 80B8h

Figure 5-690. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Name Register

31	30	29	28	27	26	25	24
PHY_MASTER_CONTROL_RESV3_FLD							PHY_MASTER_LOCK_MODE_FLD
R							R/W
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PHY_MASTER_BYPASS_MODE_FLD	PHY_MASTER_PHASE_DETECT_SELECTOR_FLD			PHY_MASTER_CONTROL_RESV2_FLD	PHY_MASTER_NB_INDICATIONS_FLD		
R/W	R/W			R	R/W		
1h	0h			0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PHY_MASTER_CONTROL_RESV1_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHY_MASTER_CONTROL_RESV1_FLD	PHY_MASTER_INITIAL_DELAY_FLD						
R	R/W						
0h	0h						

Table 5-1410. OSPI_FLASH_CFG_PHY_MASTER_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	PHY_MASTER_CONTROL_RESV3_FLD	R	0h	Reserved
24	PHY_MASTER_LOCK_MODE_FLD	R/W	0h	Determines if the master delay line locks on a full cycle or half cycle of delay.
23	PHY_MASTER_BYPASS_MODE_FLD	R/W	1h	Controls the bypass mode of the master and target DLLs.
22:20	PHY_MASTER_PHASE_DETECT_SELECTOR_FLD	R/W	0h	Selects the number of delay elements to be inserted between the phase detect flip-flops.
19	PHY_MASTER_CONTROL_RESV2_FLD	R	0h	Reserved
18:16	PHY_MASTER_NB_INDICATIONS_FLD	R/W	0h	Holds the number of consecutive increment or decrement indications.
15:7	PHY_MASTER_CONTROL_RESV1_FLD	R	0h	Reserved
6:0	PHY_MASTER_INITIAL_DELAY_FLD	R/W	0h	This value is the initial delay value for the DLL.

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5.7.2.94 OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register

5.7.2.94.1 OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register (Offset = BCh) [reset = 0h]

DLL Observable Register Lower.

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Table 5-1411. Instance Table

Instance Name	Physical Address
FSS0	5380 80BCh

Figure 5-691. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Name Register

31	30	29	28	27	26	25	24
DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD						
R	R						
0h	0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD					DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD		DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD
R					R		R
0h					0h		0h

Table 5-1412. OSPI_FLASH_CFG_DLL_OBSERVABLE_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD	R	0h	Holds the state of the cumulative dll_lock_inc register.
23:16	DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD	R	0h	Holds the state of the cumulative dll_lock_dec register.
15	DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	R	0h	This bit indicates that lock of loopback is done.
14:8	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD	R	0h	Reports the DLL encoder value from the master DLL to the target DLLs.
7:3	DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD	R	0h	Reports the number of increments or decrements required for the master DLL to complete the locking process.
2:1	DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD	R	0h	Defines the mode in which the DLL has achieved the lock.
0	DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD	R	0h	Indicates status of DLL.

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5.7.2.95 OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register

5.7.2.95.1 OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register (Offset = C0h) [reset = 0h]

DLL Observable Register Upper.

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Table 5-1413. Instance Table

Instance Name	Physical Address
FSS0	5380 80C0h

Figure 5-692. OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Name Register

31	30	29	28	27	26	25	24
DLL_OBSERVABLE_UPPER_RESV2_FLD							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DLL_OBSERVABLE_UPPER_RESV2_FLD	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD						
R	R						
0h	0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DLL_OBSERVABLE_UPPER_RESV1_FLD							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DLL_OBSERVABLE_UPPER_RESV1_FLD	DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT_FLD						
R	R						
0h	0h						

Table 5-1414. OSPI_FLASH_CFG_DLL_OBSERVABLE_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:23	DLL_OBSERVABLE_UPPER_RESV2_FLD	R	0h	Reserved
22:16	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD	R	0h	Holds the encoded value for the TX delay line for this slice.
15:7	DLL_OBSERVABLE_UPPER_RESV1_FLD	R	0h	Reserved
6:0	DLL_OBSERVABLE__UPPER_RX_DECODER_OUTPUT_FLD	R	0h	Holds the encoded value for the RX delay line for this slice.

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5.7.2.96 OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register

5.7.2.96.1 OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register (Offset = E0h) [reset = 13EDFA00h]

This register provides the supplementing opcodes for Dual Byte Opcode Mode activated by Octal-SPI Configuration Register bit[30].

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Table 5-1415. Instance Table

Instance Name	Physical Address
FSS0	5380 80E0h

Figure 5-693. OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Name Register

31	30	29	28	27	26	25	24
EXT_READ_OPCODE_FLD							
R/W							
13h							
23	22	21	20	19	18	17	16
EXT_WRITE_OPCODE_FLD							
R/W							
EDh							
15	14	13	12	11	10	9	8
EXT_POLL_OPCODE_FLD							
R/W							
FAh							
7	6	5	4	3	2	1	0
EXT_STIG_OPCODE_FLD							
R/W							
0h							

Table 5-1416. OSPI_FLASH_CFG_OPCODE_EXT_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	EXT_READ_OPCODE_FLD	R/W	13h	Supplement byte of any Read Opcode
23:16	EXT_WRITE_OPCODE_FLD	R/W	EDh	Supplement byte of any Write Opcode
15:8	EXT_POLL_OPCODE_FLD	R/W	FAh	Supplement byte of any Polling Opcode
7:0	EXT_STIG_OPCODE_FLD	R/W	0h	Supplement byte of any STIG Opcode

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5.7.2.97 OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register

5.7.2.97.1 OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register (Offset = E4h) [reset = 6F90000h]

This register provides the supplementing opcodes for Dual Byte Opcode Mode activated by Octal-SPI Configuration Register bit[30]. Additionaly, it allows the user to define the Write Enable Latch (WEL) command first byte opcode used for automatic WEL insertion before any AHB write access.

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Table 5-1417. Instance Table

Instance Name	Physical Address
FSS0	5380 80E4h

Figure 5-694. OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Name Register

31	30	29	28	27	26	25	24
WEL_OPCODE_FLD							
R/W							
6h							
23	22	21	20	19	18	17	16
EXT_WEL_OPCODE_FLD							
R/W							
F9h							
15	14	13	12	11	10	9	8
OPCODE_EXT_UPPER_RESV1_FLD							
R							
0h							
7	6	5	4	3	2	1	0
OPCODE_EXT_UPPER_RESV1_FLD							
R							
0h							

Table 5-1418. OSPI_FLASH_CFG_OPCODE_EXT_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	WEL_OPCODE_FLD	R/W	6h	First byte of any WEL Opcode
23:16	EXT_WEL_OPCODE_FLD	R/W	F9h	Supplement byte of any WEL Opcode
15:0	OPCODE_EXT_UPPER_RESV1_FLD	R	0h	Reserved

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5.7.2.98 OSPI_FLASH_CFG_MODULE_ID_REG Register

5.7.2.98.1 OSPI_FLASH_CFG_MODULE_ID_REG Register (Offset = FCh) [reset = 3000300h]

This register provides the IP release number and the configuration data.

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Table 5-1419. Instance Table

Instance Name	Physical Address
FSS0	5380 80FCh

Figure 5-695. OSPI_FLASH_CFG_MODULE_ID_REG Name Register

31	30	29	28	27	26	25	24
FIX_PATCH_FLD							
R							
3h							
23	22	21	20	19	18	17	16
MODULE_ID_FLD							
R							
3h							
15	14	13	12	11	10	9	8
MODULE_ID_FLD							
R							
3h							
7	6	5	4	3	2	1	0
MODULE_ID_RESV_FLD						CONF_FLD	
R						R	
0h						0h	

Table 5-1420. OSPI_FLASH_CFG_MODULE_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	FIX_PATCH_FLD	R	3h	Fix/path number related to revision described by 3 LSBs of this register
23:8	MODULE_ID_FLD	R	3h	Module/Revision ID number
7:2	MODULE_ID_RESV_FLD	R	0h	Reserved
1:0	CONF_FLD	R	0h	Configuration ID number: 0 : OCTAL + PHY Configuration 1 : OCTAL Configuration 2 : QUAD + PHY Configuration 3 : QUAD Configuration

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5.7.2.99 FOTA_GENREGS_FOTA_INIT Register

5.7.2.99.1 FOTA_GENREGS_FOTA_INIT Register (Offset = 0h) [reset = 15h]

This register is used to initialize FOTA logic including M8051EW MCU.

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Table 5-1421. Instance Table

Instance Name	Physical Address
FSS0	5380 B000h

Figure 5-696. FOTA_GENREGS_FOTA_INIT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		MCU_STALL_EN	FUNC_MODE	PDMEM_INIT_DONE	MEMACCESS	CLKDIS	RESET
NONE		R/W	R/W	R	R/W	R/W	R/W
0h		0h	1h	0h	1h	0h	1h

Table 5-1422. FOTA_GENREGS_FOTA_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	MCU_STALL_EN	R/W	0h	Reserved field. This field SHALL be retained at 0, which is the default value.
4	FUNC_MODE	R/W	1h	This bit is used for selection functional or debug mode. 1'b1 - M8051EW uses functional mode for regular operation. 1'b0 - M8051EW uses debug mode for debug using JTAG.
3	PDMEM_INIT_DONE	R	0h	This bit indicates that FOTA program/data memory RAM initialization is done. Until this bit is set, access to program/data memory should not be performed by software.
2	MEMACCESS	R/W	1h	This bit provides SOC CPU access to program/data memory and internal memory through FSS config interface when set. If clear, these M8051EW memories are not accessible through config interface and is fully under the control of M8051EW. Software has to ensure that M8051EW is in reset by setting bit 0 of this register when memaccess is set.
1	CLKDIS	R/W	0h	This bit holds M8051EW core clock gated when set to 1'b1. Clock to M8051EW is enabled at reset. SOC software sets this bit to put M8051EW and other FOTA logic in low power state when not used by enabling clock gating.
0	RESET	R/W	1h	This bit holds M8051EW core in reset when set to 1'b1. System firmware clears this bit after setting up program and data memories.

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5.7.2.100 FOTA_GENREGS_FOTA_CTRL Register

5.7.2.100.1 FOTA_GENREGS_FOTA_CTRL Register (Offset = 4h) [reset = 0h]

This register is used to start M8051EW firmware.

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Table 5-1423. Instance Table

Instance Name	Physical Address
FSS0	5380 B004h

Figure 5-697. FOTA_GENREGS_FOTA_CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							GO
NONE							R/W1TS
0h							0h

Table 5-1424. FOTA_GENREGS_FOTA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	GO	R/W1TS	0h	SOC CPU sets this bit to indicate to M8051EW firmware that it can start the next FOTA page write. Once go is set, SOC software has to ensure that it is set again only after receiving an interrupt (completion or error) from M8051EW. If this requirement is not followed, it could result in M8051EW firmware repeating the FOTA write erroneously. A write to this register causes an indirect write to ESFR space for M8051EW. Firmware polls until ESFR GO bit is set and then starts the FOTA write sequence. This bit is cleared by hardware when the MCU has acknowledged GO through a write to the GO_ACK ESFR bit.

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5.7.2.101 FOTA_GENREGS_FOTA_ERR_INFO Register

5.7.2.101.1 FOTA_GENREGS_FOTA_ERR_INFO Register (Offset = 8h) [reset = 0h]

This register contains information from FOTA logic used when servicing fsas_fota_stat_err_pend/ fsas_fota_stat_err_req interrupt. This information is used in conjunction with FOTA interrupt status register ERR_STS_IRQ_STATUS_RAW. Software is expected to clear the fields in this register as it is not auto cleared by hardware.

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Table 5-1425. Instance Table

Instance Name	Physical Address
FSS0	5380 B008h

Figure 5-698. FOTA_GENREGS_FOTA_ERR_INFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MCU_ERR_CODE
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
MCU_ERR_CODE				DAT_ERR_SSTATUS			DAT_ERR_RSTATUS
R/W				R/W			R/W
0h				0h			0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DAT_ERR_RSTATUS		CFG_ERR_SSTATUS			CFG_ERR_RSTATUS		
R/W		R/W			R/W		
0h		0h			0h		

Table 5-1426. FOTA_GENREGS_FOTA_ERR_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16:12	MCU_ERR_CODE	R/W	0h	This field contains error code reported by M8051EW firmware when ERR_STS_IRQ_STATUS_RAW.mcu_err is set. Error codes are software defined. Example encoding: 5'd0 - Flash error encountered during auto status polling, 5'd1 - Auto polling timeout error as status read from flash did not occur within expected time, 5'd2 - FOTA write timeout error where auto polling by M8051EW has indicated that flash write is still in progress after auto polling expiry time programmed in firmware, 5'd3 to 5'd31 - Reserved for future use.
11:9	DAT_ERR_SSTATUS	R/W	0h	This field contains read error status code when ERR_STS_IRQ_STATUS_RAW.dat_read_err interrupt flag is set
8:6	DAT_ERR_RSTATUS	R/W	0h	This field contains read error status code when ERR_STS_IRQ_STATUS_RAW.dat_read_err interrupt flag is set
5:3	CFG_ERR_SSTATUS	R/W	0h	This field contains read error status code when ERR_STS_IRQ_STATUS_RAW.cfg_read_err interrupt flag is set
2:0	CFG_ERR_RSTATUS	R/W	0h	This field contains read error status code when ERR_STS_IRQ_STATUS_RAW.cfg_read_err interrupt flag is set

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5.7.2.102 FOTA_GENREGS_FOTA_GP0 Register

5.7.2.102.1 FOTA_GENREGS_FOTA_GP0 Register (Offset = 10h) [reset = 0h]

FOTA general purpose 0 register. SOC CPU can write to this register to pass information to M8051EW firmware through ESFR space.

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Table 5-1427. Instance Table

Instance Name	Physical Address
FSS0	5380 B010h

Figure 5-699. FOTA_GENREGS_FOTA_GP0 Name Register

31	30	29	28	27	26	25	24
VAL3							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL2							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL1							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL0							
R/W							
0h							

Table 5-1428. FOTA_GENREGS_FOTA_GP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	VAL3	R/W	0h	General purpose 0 register val3.
23:16	VAL2	R/W	0h	General purpose 0 register val2.
15:8	VAL1	R/W	0h	General purpose 0 register val1.
7:0	VAL0	R/W	0h	General purpose 0 register val0.

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5.7.2.103 FOTA_GENREGS_FOTA_GP1 Register

5.7.2.103.1 FOTA_GENREGS_FOTA_GP1 Register (Offset = 14h) [reset = 0h]

FOTA general purpose 1 register. M8051EW can write to this register to pass information to SOC CPU through ESFR space. Interpretation for this register is software defined and can be made context dependent if required.

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Table 5-1429. Instance Table

Instance Name	Physical Address
FSS0	5380 B014h

Figure 5-700. FOTA_GENREGS_FOTA_GP1 Name Register

31	30	29	28	27	26	25	24
VAL3							
R							
0h							
23	22	21	20	19	18	17	16
VAL2							
R							
0h							
15	14	13	12	11	10	9	8
VAL1							
R							
0h							
7	6	5	4	3	2	1	0
VAL0							
R							
0h							

Table 5-1430. FOTA_GENREGS_FOTA_GP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	VAL3	R	0h	General purpose 1 register val3.
23:16	VAL2	R	0h	General purpose 1 register val2.
15:8	VAL1	R	0h	General purpose 1 register val1.
7:0	VAL0	R	0h	General purpose 1 register val0.

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5.7.2.104 FOTA_GENREGS_FOTA_ADDR Register

5.7.2.104.1 FOTA_GENREGS_FOTA_ADDR Register (Offset = 18h) [reset = 0h]

FOTA operation write address register. SOC can write to this register to preload address for FOTA write instead of having 8051 firmware to setup address. Writing this register causes an indirect write to MCU_DAT_ADDR0-MCU_DAT_ADDR3 ESFR registers that are used by the VBUSM initiator as address for the FOTA write operation. Preloading these ESFR registers through this register removes the burden from 8051 firmware and reduces 8051 code size.

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Table 5-1431. Instance Table

Instance Name	Physical Address
FSS0	5380 B018h

Figure 5-701. FOTA_GENREGS_FOTA_ADDR Name Register

31	30	29	28	27	26	25	24
VAL3							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL2							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL1							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL0							
R/W							
0h							

Table 5-1432. FOTA_GENREGS_FOTA_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	VAL3	R/W	0h	FOTA write address bits 31:24
23:16	VAL2	R/W	0h	FOTA write address bits 23:16
15:8	VAL1	R/W	0h	FOTA write address bits 15:8
7:0	VAL0	R/W	0h	FOTA write address bits 7:0

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5.7.2.105 FOTA_GENREGS_FOTA_CNT Register

5.7.2.105.1 FOTA_GENREGS_FOTA_CNT Register (Offset = 1Ch) [reset = 0h]

FOTA operation write byte count. SOC can write to this register to preload byte count based on the page size of the flash memory used. Writing this register causes an indirect write to MCU_DAT_CNT0-MCU_DAT_CNT1 ESFR registers that are used by the VBUSM initiator as the overall byte count for the FOTA write operation. VBUSM initiator performs the required number of 32-byte writes to match this overall byte count. Preloading these ESFR registers through this register removes the burden from 8051 firmware and reduces 8051 code size.

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Table 5-1433. Instance Table

Instance Name	Physical Address
FSS0	5380 B01Ch

Figure 5-702. FOTA_GENREGS_FOTA_CNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						VAL1	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
VAL0							
R/W							
0h							

Table 5-1434. FOTA_GENREGS_FOTA_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9:8	VAL1	R/W	0h	FOTA write byte count bits 9:8
7:0	VAL0	R/W	0h	FOTA write byte count bits 7:0

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5.7.2.106 FOTA_GENREGS_STS_IRQ_IRQ_EOI Register

5.7.2.106.1 FOTA_GENREGS_STS_IRQ_IRQ_EOI Register (Offset = 20h) [reset = 0h]

The End of Interrupt (EOI) Register allows the CPU to acknowledge completion of fsas_fota_stat_intr_req pulse interrupt. When this register is written to 1'b0, INTD logic used for converting fsas_ecc_intr_err_pend level interrupt to pulse will be re-armed. That is, if interrupt sources remain after writing this register to 1'b0, another pulse interrupt will be triggered by INTD. Conversely, if this register is not written to 1'b0 after fsas_fota_stat_intr_req pulse interrupt is received, then another pulse interrupt will not be received as INTD has not been re-armed. This register will be reset one cycle after it has been written to. Please note that the reason for writing 1'b0 is because there is only one interrupt (no interrupt aggregation) associated with this EOI and the INTD vector associated with this interrupt is 1'b0.

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Table 5-1435. Instance Table

Instance Name	Physical Address
FSS0	5380 B020h + formula

Figure 5-703. FOTA_GENREGS_STS_IRQ_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
NONE							W
0h							0h

Table 5-1436. FOTA_GENREGS_STS_IRQ_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	W	0h	Write 1'b0 to acknowledge fsas_fota_stat_intr_req pulse interrupt.

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5.7.2.107 FOTA_GENREGS_STS_IRQ_IRQ_STATUS_RAW Register

5.7.2.107.1 FOTA_GENREGS_STS_IRQ_IRQ_STATUS_RAW Register (Offset = 24h) [reset = 0h]

The IRQ_STATUS_RAW register allows the interrupt sources to be manually set when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_intr_pend/fsas_fota_stat_intr_req interrupt output. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

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Table 5-1437. Instance Table

Instance Name	Physical Address
FSS0	5380 B024h + formula

Figure 5-704. FOTA_GENREGS_STS_IRQ_IRQ_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FOTA_DONE
NONE							R/W1TS
0h							0h

Table 5-1438. FOTA_GENREGS_STS_IRQ_IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FOTA_DONE	R/W1TS	0h	FOTA done raw status flag

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5.7.2.108 FOTA_GENREGS_STS_IRQ_IRQ_STATUS Register

5.7.2.108.1 FOTA_GENREGS_STS_IRQ_IRQ_STATUS Register (Offset = 28h) [reset = 0h]

The IRQ_STATUS register allows the interrupt sources to be manually cleared when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_intr_pend/fsas_fota_stat_intr_req interrupt output. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

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Table 5-1439. Instance Table

Instance Name	Physical Address
FSS0	5380 B028h + formula

Figure 5-705. FOTA_GENREGS_STS_IRQ_IRQ_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FOTA_DONE
NONE							R/W1TC
0h							0h

Table 5-1440. FOTA_GENREGS_STS_IRQ_IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FOTA_DONE	R/W1TC	0h	FOTA done status flag

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5.7.2.109 FOTA_GENREGS_STS_IRQ_IRQ_ENABLE_SET Register

5.7.2.109.1 FOTA_GENREGS_STS_IRQ_IRQ_ENABLE_SET Register (Offset = 2Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the interrupt sources to be manually enabled when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_intr_pend/fsas_fota_stat_intr_req interrupt output. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

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Table 5-1441. Instance Table

Instance Name	Physical Address
FSS0	5380 B02Ch + formula

Figure 5-706. FOTA_GENREGS_STS_IRQ_IRQ_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FOTA_DONE
NONE							R/W1TS
0h							0h

Table 5-1442. FOTA_GENREGS_STS_IRQ_IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FOTA_DONE	R/W1TS	0h	FOTA done enable set

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5.7.2.110 FOTA_GENREGS_STS_IRQ_IRQ_ENABLE_CLR Register

5.7.2.110.1 FOTA_GENREGS_STS_IRQ_IRQ_ENABLE_CLR Register (Offset = 30h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the interrupt sources to be manually disabled when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_intr_pend/fsas_fota_stat_intr_req interrupt output. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

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Table 5-1443. Instance Table

Instance Name	Physical Address
FSS0	5380 B030h + formula

Figure 5-707. FOTA_GENREGS_STS_IRQ_IRQ_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							FOTA_DONE
NONE							R/W1TC
0h							0h

Table 5-1444. FOTA_GENREGS_STS_IRQ_IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	FOTA_DONE	R/W1TC	0h	FOTA done enable clear

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5.7.2.111 FOTA_GENREGS_ERR_STS_IRQ_IRQ_EOI Register

5.7.2.111.1 FOTA_GENREGS_ERR_STS_IRQ_IRQ_EOI Register (Offset = 40h) [reset = 0h]

The End of Interrupt (EOI) Register allows the CPU to acknowledge completion of fsas_fota_stat_err_req pulse interrupt. When this register is written to 1'b0, INTD logic used for converting fsas_ecc_intr_err_pend level interrupt to pulse will be re-armed. That is, if interrupt sources remain after writing this register to 1'b0, another pulse interrupt will be triggered by INTD. Conversely, if this register is not written to 1'b0 after fsas_fota_stat_err_req pulse interrupt is received, then another pulse interrupt will not be received as INTD has not been re-armed. This register will be reset one cycle after it has been written to. Please note that the reason for writing 1'b0 is because there is only one interrupt (no interrupt aggregation) associated with this EOI and the INTD vector associated with this interrupt is 1'b0.

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Table 5-1445. Instance Table

Instance Name	Physical Address
FSS0	5380 B040h + formula

Figure 5-708. FOTA_GENREGS_ERR_STS_IRQ_IRQ_EOI Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
NONE							W
0h							0h

Table 5-1446. FOTA_GENREGS_ERR_STS_IRQ_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_VECTOR	W	0h	Write 1'b0 to acknowledge fsas_fota_stat_err_req pulse interrupt.

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5.7.2.112 FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS_RAW Register

5.7.2.112.1 FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS_RAW Register (Offset = 44h) [reset = 0h]

The IRQ_STATUS_RAW register allows the interrupt sources to be manually set when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_err_pend/fsas_fota_stat_err_req interrupt output. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

Return to Summary Table

Table 5-1447. Instance Table

Instance Name	Physical Address
FSS0	5380 B044h + formula

Figure 5-709. FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS_RAW Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	MCU_ERR	DAT_WRITE_ERR	DAT_READ_ERR	CFG_WRITE_ERR	CFG_READ_ERR	RESERVED	
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	NONE	
0h	0h	0h	0h	0h	0h	0h	

Table 5-1448. FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	MCU_ERR	R/W1TS	0h	MCU error raw status flag. This is used to communicate error conditions encountered by 8051 firmware to SOC CPU. Error code is captured in FOTA_ERR_INFO.mcu_err_code field. If 8051 firmware runs into any error conditions, it sets the FOTA_ERR_STAT.mcu_err ESFR bit to 1'b1 and writes the corresponding error code into FOTA_ERR_STAT.mcu_err_code field. This causes an indirect writes to STATUS_RAW.mcu_err MMR and FOTA_ERR_INFO.mcu_err_code MMR. M8051EW firmware defines the error codes that result in this error. Please refer to FOTA_ERR_INFO.mcu_err_code MMR description for suggested encoding.
5	DAT_WRITE_ERR	R/W1TS	0h	Data interface write status error raw status flag. This error flag gets set when M8051EW performs a data write and error status is returned. The CBA error status code received is stored in FOTA_ERR_INFO.dat_err_sstatus register.
4	DAT_READ_ERR	R/W1TS	0h	Data interface read status error raw status flag. This error flag gets set when M8051EW performs a data read and error status is returned. The CBA error status code received is stored in FOTA_ERR_INFO.dat_err_rstatus register.

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Table 5-1448. FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CFG_WRITE_ERR	R/W1TS	0h	Config interface write status error raw status flag. This error flag gets set when M8051EW performs a configuration write and error status is returned. The CBA error status code received is stored in FOTA_ERR_INFO.cfg_err_sstatus register.
2	CFG_READ_ERR	R/W1TS	0h	Config interface read status error raw status flag. This error flag gets set when M8051EW performs a configuration read and error status is returned. The CBA error status code received is stored in FOTA_ERR_INFO.cfg_err_rstatus register.
1:0	RESERVED	NONE	0h	Reserved

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5.7.2.113 FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS Register

5.7.2.113.1 FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS Register (Offset = 48h) [reset = 0h]

The IRQ_STATUS register allows the interrupt sources to be manually cleared when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_err_pend/fsas_fota_stat_err_req interrupt output. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

Return to Summary Table

Table 5-1449. Instance Table

Instance Name	Physical Address
FSS0	5380 B048h + formula

Figure 5-710. FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MCU_ERR	DAT_WRITE_ERR	DAT_READ_ERR	CFG_WRITE_ERR	CFG_READ_ERR	RESERVED	
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE	
0h	0h	0h	0h	0h	0h	0h	

Table 5-1450. FOTA_GENREGS_ERR_STS_IRQ_IRQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	MCU_ERR	R/W1TC	0h	MCU error status flag
5	DAT_WRITE_ERR	R/W1TC	0h	Data interface write status error status flag
4	DAT_READ_ERR	R/W1TC	0h	Data interface read status error status flag
3	CFG_WRITE_ERR	R/W1TC	0h	Config interface write status error status flag
2	CFG_READ_ERR	R/W1TC	0h	Config interface read status error status flag
1:0	RESERVED	NONE	0h	Reserved

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5.7.2.114 FOTA_GENREGS_ERR_STS_IRQ_IRQ_ENABLE_SET Register

5.7.2.114.1 FOTA_GENREGS_ERR_STS_IRQ_IRQ_ENABLE_SET Register (Offset = 4Ch) [reset = 0h]

The IRQ_ENABLE_SET register allows the interrupt sources to be manually enabled when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_err_pend/fsas_fota_stat_err_req interrupt output. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

Return to Summary Table

Table 5-1451. Instance Table

Instance Name	Physical Address
FSS0	5380 B04Ch + formula

Figure 5-711. FOTA_GENREGS_ERR_STS_IRQ_IRQ_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MCU_ERR	DAT_WRITE_ERR	DAT_READ_ERR	CFG_WRITE_ERR	CFG_READ_ERR	RESERVED	
NONE	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	NONE	
0h	0h	0h	0h	0h	0h	0h	

Table 5-1452. FOTA_GENREGS_ERR_STS_IRQ_IRQ_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	MCU_ERR	R/W1TS	0h	MCU error enable set
5	DAT_WRITE_ERR	R/W1TS	0h	Data interface write status error enable set
4	DAT_READ_ERR	R/W1TS	0h	Data interface read status error enable set
3	CFG_WRITE_ERR	R/W1TS	0h	Config interface write status error enable set
2	CFG_READ_ERR	R/W1TS	0h	Config interface read status error enable set
1:0	RESERVED	NONE	0h	Reserved

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5.7.2.115 FOTA_GENREGS_ERR_STS_IRQ_IRQ_ENABLE_CLR Register

5.7.2.115.1 FOTA_GENREGS_ERR_STS_IRQ_IRQ_ENABLE_CLR Register (Offset = 50h) [reset = 0h]

The IRQ_ENABLE_CLR register allows the interrupt sources to be manually disabled when writing a 1 to a specific bit. This register corresponds to fsas_fota_stat_err_pend/fsas_fota_stat_err_req interrupt output. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

Return to Summary Table

Table 5-1453. Instance Table

Instance Name	Physical Address
FSS0	5380 B050h + formula

Figure 5-712. FOTA_GENREGS_ERR_STS_IRQ_IRQ_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED	MCU_ERR	DAT_WRITE_ERR	DAT_READ_ERR	CFG_WRITE_ERR	CFG_READ_ERR	RESERVED	
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE	
0h	0h	0h	0h	0h	0h	0h	

Table 5-1454. FOTA_GENREGS_ERR_STS_IRQ_IRQ_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	NONE	0h	Reserved
6	MCU_ERR	R/W1TC	0h	MCU error enable clear
5	DAT_WRITE_ERR	R/W1TC	0h	Data interface write status error enable clear
4	DAT_READ_ERR	R/W1TC	0h	Data interface read status error enable clear
3	CFG_WRITE_ERR	R/W1TC	0h	Config interface write status error enable clear
2	CFG_READ_ERR	R/W1TC	0h	Config interface read status error enable clear
1:0	RESERVED	NONE	0h	Reserved

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5.7.2.116 PDMEM_GENREGS_LOC_J Register

5.7.2.116.1 PDMEM_GENREGS_LOC_J Register (Offset = 0h) [reset = 0h]

M8051EW program and external data memory array.

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Table 5-1455. Instance Table

Instance Name	Physical Address
FSS0	5380 C000h + formula

Figure 5-713. PDMEM_GENREGS_LOC_j Name Register

31	30	29	28	27	26	25	24
VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL							
R/W							
0h							

Table 5-1456. PDMEM_GENREGS_LOC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R/W	0h	Value of element in program and external data memory

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5.7.2.117 IMEM_GENREGS_LOC_J Register

5.7.2.117.1 IMEM_GENREGS_LOC_J Register (Offset = 0h) [reset = 0h]

M8051EW Internal Data Memory array.

Return to Summary Table

Table 5-1457. Instance Table

Instance Name	Physical Address
FSS0	5380 D000h + formula

Figure 5-714. IMEM_GENREGS_LOC_j Name Register

31	30	29	28	27	26	25	24
VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL							
R/W							
0h							

Table 5-1458. IMEM_GENREGS_LOC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R/W	0h	Value of element in internal data memory

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5.7.2.118 WBUF_GENREGS_LOC_J Register

5.7.2.118.1 WBUF_GENREGS_LOC_J Register (Offset = 0h) [reset = 0h]

FOTA write buffer array.

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Table 5-1459. Instance Table

Instance Name	Physical Address
FSS0	5380 E000h + formula

Figure 5-715. WBUF_GENREGS_LOC_j Name Register

31	30	29	28	27	26	25	24
VAL							
R/W							
0h							
23	22	21	20	19	18	17	16
VAL							
R/W							
0h							
15	14	13	12	11	10	9	8
VAL							
R/W							
0h							
7	6	5	4	3	2	1	0
VAL							
R/W							
0h							

Table 5-1460. WBUF_GENREGS_LOC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	VAL	R/W	0h	Value of element in FOTA write buffer

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5.7.2.119 FSAS_ECC_AGGR_REV Register

5.7.2.119.1 FSAS_ECC_AGGR_REV Register (Offset = 0h) [reset = 66A03A01h]

Revision parameters.

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Table 5-1461. Instance Table

Instance Name	Physical Address
FSS0	5380 F000h

Figure 5-716. FSAS_ECC_AGGR_REV Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			

23	22	21	20	19	18	17	16
MODULE_ID							
R							
6A0h							

15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
7h					2h		

7	6	5	4	3	2	1	0
CUSTOM		REVMIN					
R		R					
0h		1h					

Table 5-1462. FSAS_ECC_AGGR_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	7h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	1h	Minor version

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5.7.2.120 FSAS_ECC_AGGR_VECTOR Register

5.7.2.120.1 FSAS_ECC_AGGR_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register.

Return to Summary Table

Table 5-1463. Instance Table

Instance Name	Physical Address
FSS0	5380 F008h

Figure 5-717. FSAS_ECC_AGGR_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R/W1TC
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 5-1464. FSAS_ECC_AGGR_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

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5.7.2.121 FSAS_ECC_AGGR_STAT Register

5.7.2.121.1 FSAS_ECC_AGGR_STAT Register (Offset = Ch) [reset = 1h]

Misc Status.

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Table 5-1465. Instance Table

Instance Name	Physical Address
FSS0	5380 F00Ch

Figure 5-718. FSAS_ECC_AGGR_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED					NUM_RAMS		
NONE					R		
0h					1h		
7	6	5	4	3	2	1	0
NUM_RAMS							
R							
1h							

Table 5-1466. FSAS_ECC_AGGR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	1h	Indicates the number of RAMS serviced by the ECC aggregator

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5.7.2.122 FSAS_ECC_AGGR_RESERVED_SVBUS_J Register

5.7.2.122.1 FSAS_ECC_AGGR_RESERVED_SVBUS_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

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Table 5-1467. Instance Table

Instance Name	Physical Address
FSS0	5380 F010h + formula

Figure 5-719. FSAS_ECC_AGGR_RESERVED_SVBUS_j Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 5-1468. FSAS_ECC_AGGR_RESERVED_SVBUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Serial VBUS register data

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5.7.2.123 FSAS_ECC_AGGR_SEC_EOI_REG Register

5.7.2.123.1 FSAS_ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

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Table 5-1469. Instance Table

Instance Name	Physical Address
FSS0	5380 F03Ch

Figure 5-720. FSAS_ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 5-1470. FSAS_ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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5.7.2.124 FSAS_ECC_AGGR_SEC_STATUS_REG0 Register

5.7.2.124.1 FSAS_ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 5-1471. Instance Table

Instance Name	Physical Address
FSS0	5380 F040h

Figure 5-721. FSAS_ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_PEND
NONE							R/W1TS
0h							0h

Table 5-1472. FSAS_ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

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5.7.2.125 FSAS_ECC_AGGR_SEC_ENABLE_SET_REG0 Register

5.7.2.125.1 FSAS_ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 5-1473. Instance Table

Instance Name	Physical Address
FSS0	5380 F080h

Figure 5-722. FSAS_ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 5-1474. FSAS_ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

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5.7.2.126 FSAS_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

5.7.2.126.1 FSAS_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

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Table 5-1475. Instance Table

Instance Name	Physical Address
FSS0	5380 F0C0h

Figure 5-723. FSAS_ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 5-1476. FSAS_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

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5.7.2.127 FSAS_ECC_AGGR_DED_EOI_REG Register

5.7.2.127.1 FSAS_ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

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Table 5-1477. Instance Table

Instance Name	Physical Address
FSS0	5380 F13Ch

Figure 5-724. FSAS_ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 5-1478. FSAS_ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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5.7.2.128 FSAS_ECC_AGGR_DED_STATUS_REG0 Register

5.7.2.128.1 FSAS_ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

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Table 5-1479. Instance Table

Instance Name	Physical Address
FSS0	5380 F140h

Figure 5-725. FSAS_ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							RAMECC_PEND
NONE							R/W1TS
0h							0h

Table 5-1480. FSAS_ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc_pend

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5.7.2.129 FSAS_ECC_AGGR_DED_ENABLE_SET_REG0 Register

5.7.2.129.1 FSAS_ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 5-1481. Instance Table

Instance Name	Physical Address
FSS0	5380 F180h

Figure 5-726. FSAS_ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_SET
NONE							R/W1TS
0h							0h

Table 5-1482. FSAS_ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc_pend

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5.7.2.130 FSAS_ECC_AGGR_DED_ENABLE_CLR_REG0 Register

5.7.2.130.1 FSAS_ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 5-1483. Instance Table

Instance Name	Physical Address
FSS0	5380 F1C0h

Figure 5-727. FSAS_ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_CLR
NONE							R/W1TC
0h							0h

Table 5-1484. FSAS_ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc_pend

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5.7.2.131 FSAS_ECC_AGGR_AGGR_ENABLE_SET Register

5.7.2.131.1 FSAS_ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register.

Return to Summary Table

Table 5-1485. Instance Table

Instance Name	Physical Address
FSS0	5380 F200h

Figure 5-728. FSAS_ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 5-1486. FSAS_ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	Interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	Interrupt enable set for parity errors

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5.7.2.132 FSAS_ECC_AGGR_AGGR_ENABLE_CLR Register

5.7.2.132.1 FSAS_ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register.

Return to Summary Table

Table 5-1487. Instance Table

Instance Name	Physical Address
FSS0	5380 F204h

Figure 5-729. FSAS_ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 5-1488. FSAS_ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	Interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	Interrupt enable clear for parity errors

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5.7.2.133 FSAS_ECC_AGGR_AGGR_STATUS_SET Register

5.7.2.133.1 FSAS_ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register.

Return to Summary Table

Table 5-1489. Instance Table

Instance Name	Physical Address
FSS0	5380 F208h

Figure 5-730. FSAS_ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 5-1490. FSAS_ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	Interrupt status set for svbus timeout errors
1:0	PARITY	R/WI	0h	Interrupt status set for parity errors

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5.7.2.134 FSAS_ECC_AGGR_AGGR_STATUS_CLR Register

5.7.2.134.1 FSAS_ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register.

Return to Summary Table

Table 5-1491. Instance Table

Instance Name	Physical Address
FSS0	5380 F20Ch

Figure 5-731. FSAS_ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 5-1492. FSAS_ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	Interrupt status clear for svbus timeout errors
1:0	PARITY	R/WD	0h	Interrupt status clear for parity errors

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5.7.2.135 DATA_REG0_HPB_DATA_MEM_J Register

5.7.2.135.1 DATA_REG0_HPB_DATA_MEM_J Register (Offset = 0h) [reset = 0h]

FSAS data region0.

Return to Summary Table

Table 5-1493. Instance Table

Instance Name	Physical Address
FSS0	6000 0000h + formula

Figure 5-732. DATA_REG0_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 5-1494. DATA_REG0_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region0

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5.7.2.136 DATA_REG1_HPB_DATA_MEM_J Register

5.7.2.136.1 DATA_REG1_HPB_DATA_MEM_J Register (Offset = 0h) [reset = 0h]

FSAS boot data region1.

Return to Summary Table

Table 5-1495. Instance Table

Instance Name	Physical Address
FSS0	8000 0000h + formula

Figure 5-733. DATA_REG1_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 5-1496. DATA_REG1_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region1

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5.7.2.137 DATA_REG3_HPB_DATA_MEM_J Register

5.7.2.137.1 DATA_REG3_HPB_DATA_MEM_J Register (Offset = 0h) [reset = 0h]

FSAS bypass data region3.

Return to Summary Table

Table 5-1497. Instance Table

Instance Name	Physical Address
FSS0	8800 0000h + formula

Figure 5-734. DATA_REG3_HPB_DATA_MEM_j Name Register

31	30	29	28	27	26	25	24
HPB_DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
HPB_DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
HPB_DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
HPB_DATA							
R/W							
0h							

Table 5-1498. DATA_REG3_HPB_DATA_MEM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	HPB_DATA	R/W	0h	FSAS data region1

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5.8 GPIO

GPIO

5.8.1 GPIO Summaries

GPIO Summaries

Table 5-1499. GPIO Registers, Base Address=5200 0000h, Length=256

Offset	Length	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	GPIO2 Physical Address
0h	32	GPIO_PID	5200 0000h	5200 1000h	5200 2000h
4h	32	GPIO_PCR	5200 0004h	5200 1004h	5200 2004h
8h	32	GPIO_BINTEN	5200 0008h	5200 1008h	5200 2008h
10h	32	GPIO_DIR01	5200 0010h	5200 1010h	5200 2010h
14h	32	GPIO_OUT_DATA01	5200 0014h	5200 1014h	5200 2014h
18h	32	GPIO_SET_DATA01	5200 0018h	5200 1018h	5200 2018h
1Ch	32	GPIO_CLR_DATA01	5200 001Ch	5200 101Ch	5200 201Ch
20h	32	GPIO_IN_DATA01	5200 0020h	5200 1020h	5200 2020h
24h	32	GPIO_SET_RIS_TRIG01	5200 0024h	5200 1024h	5200 2024h
28h	32	GPIO_CLR_RIS_TRIG01	5200 0028h	5200 1028h	5200 2028h
2Ch	32	GPIO_SET_FAL_TRIG01	5200 002Ch	5200 102Ch	5200 202Ch
30h	32	GPIO_CLR_FAL_TRIG01	5200 0030h	5200 1030h	5200 2030h
34h	32	GPIO_INTSTAT01	5200 0034h	5200 1034h	5200 2034h
38h	32	GPIO_DIR23	5200 0038h	5200 1038h	5200 2038h
3Ch	32	GPIO_OUT_DATA23	5200 003Ch	5200 103Ch	5200 203Ch
40h	32	GPIO_SET_DATA23	5200 0040h	5200 1040h	5200 2040h
44h	32	GPIO_CLR_DATA23	5200 0044h	5200 1044h	5200 2044h
48h	32	GPIO_IN_DATA23	5200 0048h	5200 1048h	5200 2048h
4Ch	32	GPIO_SET_RIS_TRIG23	5200 004Ch	5200 104Ch	5200 204Ch
50h	32	GPIO_CLR_RIS_TRIG23	5200 0050h	5200 1050h	5200 2050h
54h	32	GPIO_SET_FAL_TRIG23	5200 0054h	5200 1054h	5200 2054h
58h	32	GPIO_CLR_FAL_TRIG23	5200 0058h	5200 1058h	5200 2058h
5Ch	32	GPIO_INTSTAT23	5200 005Ch	5200 105Ch	5200 205Ch
60h	32	GPIO_DIR45	5200 0060h	5200 1060h	5200 2060h
64h	32	GPIO_OUT_DATA45	5200 0064h	5200 1064h	5200 2064h
68h	32	GPIO_SET_DATA45	5200 0068h	5200 1068h	5200 2068h
6Ch	32	GPIO_CLR_DATA45	5200 006Ch	5200 106Ch	5200 206Ch
70h	32	GPIO_IN_DATA45	5200 0070h	5200 1070h	5200 2070h
74h	32	GPIO_SET_RIS_TRIG45	5200 0074h	5200 1074h	5200 2074h
78h	32	GPIO_CLR_RIS_TRIG45	5200 0078h	5200 1078h	5200 2078h
7Ch	32	GPIO_SET_FAL_TRIG45	5200 007Ch	5200 107Ch	5200 207Ch
80h	32	GPIO_CLR_FAL_TRIG45	5200 0080h	5200 1080h	5200 2080h
84h	32	GPIO_INTSTAT45	5200 0084h	5200 1084h	5200 2084h
88h	32	GPIO_DIR67	5200 0088h	5200 1088h	5200 2088h
8Ch	32	GPIO_OUT_DATA67	5200 008Ch	5200 108Ch	5200 208Ch
90h	32	GPIO_SET_DATA67	5200 0090h	5200 1090h	5200 2090h
94h	32	GPIO_CLR_DATA67	5200 0094h	5200 1094h	5200 2094h
98h	32	GPIO_IN_DATA67	5200 0098h	5200 1098h	5200 2098h
9Ch	32	GPIO_SET_RIS_TRIG67	5200 009Ch	5200 109Ch	5200 209Ch
A0h	32	GPIO_CLR_RIS_TRIG67	5200 00A0h	5200 10A0h	5200 20A0h

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Table 5-1499. GPIO Registers, Base Address=5200 0000h, Length=256 (continued)

Offset	Length	Register Name	GPIO0 Physical Address	GPIO1 Physical Address	GPIO2 Physical Address
A4h	32	GPIO_SET_FAL_TRIG67	5200 00A4h	5200 10A4h	5200 20A4h
A8h	32	GPIO_CLR_FAL_TRIG67	5200 00A8h	5200 10A8h	5200 20A8h
ACh	32	GPIO_INTSTAT67	5200 00ACh	5200 10ACh	5200 20ACh
B0h	32	GPIO_DIR8	5200 00B0h	5200 10B0h	5200 20B0h
B4h	32	GPIO_OUT_DATA8	5200 00B4h	5200 10B4h	5200 20B4h
B8h	32	GPIO_SET_DATA8	5200 00B8h	5200 10B8h	5200 20B8h
BCh	32	GPIO_CLR_DATA8	5200 00BCh	5200 10BCh	5200 20BCh
C0h	32	GPIO_IN_DATA8	5200 00C0h	5200 10C0h	5200 20C0h
C4h	32	GPIO_SET_RIS_TRIG8	5200 00C4h	5200 10C4h	5200 20C4h
C8h	32	GPIO_CLR_RIS_TRIG8	5200 00C8h	5200 10C8h	5200 20C8h
CCh	32	GPIO_SET_FAL_TRIG8	5200 00CCh	5200 10CCh	5200 20CCh
D0h	32	GPIO_CLR_FAL_TRIG8	5200 00D0h	5200 10D0h	5200 20D0h
D4h	32	GPIO_INTSTAT8	5200 00D4h	5200 10D4h	5200 20D4h

Table 5-1500. GPIO Registers, Base Address=5200 0000h, Length=256

Offset	Length	Register Name	GPIO3 Physical Address
0h	32	GPIO_PID	5200 3000h
4h	32	GPIO_PCR	5200 3004h
8h	32	GPIO_BINTEN	5200 3008h
10h	32	GPIO_DIR01	5200 3010h
14h	32	GPIO_OUT_DATA01	5200 3014h
18h	32	GPIO_SET_DATA01	5200 3018h
1Ch	32	GPIO_CLR_DATA01	5200 301Ch
20h	32	GPIO_IN_DATA01	5200 3020h
24h	32	GPIO_SET_RIS_TRIG01	5200 3024h
28h	32	GPIO_CLR_RIS_TRIG01	5200 3028h
2Ch	32	GPIO_SET_FAL_TRIG01	5200 302Ch
30h	32	GPIO_CLR_FAL_TRIG01	5200 3030h
34h	32	GPIO_INTSTAT01	5200 3034h
38h	32	GPIO_DIR23	5200 3038h
3Ch	32	GPIO_OUT_DATA23	5200 303Ch
40h	32	GPIO_SET_DATA23	5200 3040h
44h	32	GPIO_CLR_DATA23	5200 3044h
48h	32	GPIO_IN_DATA23	5200 3048h
4Ch	32	GPIO_SET_RIS_TRIG23	5200 304Ch
50h	32	GPIO_CLR_RIS_TRIG23	5200 3050h
54h	32	GPIO_SET_FAL_TRIG23	5200 3054h
58h	32	GPIO_CLR_FAL_TRIG23	5200 3058h
5Ch	32	GPIO_INTSTAT23	5200 305Ch
60h	32	GPIO_DIR45	5200 3060h
64h	32	GPIO_OUT_DATA45	5200 3064h
68h	32	GPIO_SET_DATA45	5200 3068h
6Ch	32	GPIO_CLR_DATA45	5200 306Ch
70h	32	GPIO_IN_DATA45	5200 3070h
74h	32	GPIO_SET_RIS_TRIG45	5200 3074h
78h	32	GPIO_CLR_RIS_TRIG45	5200 3078h

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Table 5-1500. GPIO Registers, Base Address=5200 0000h, Length=256 (continued)

Offset	Length	Register Name	GPIO3 Physical Address
7Ch	32	GPIO_SET_FAL_TRIG45	5200 307Ch
80h	32	GPIO_CLR_FAL_TRIG45	5200 3080h
84h	32	GPIO_INTSTAT45	5200 3084h
88h	32	GPIO_DIR67	5200 3088h
8Ch	32	GPIO_OUT_DATA67	5200 308Ch
90h	32	GPIO_SET_DATA67	5200 3090h
94h	32	GPIO_CLR_DATA67	5200 3094h
98h	32	GPIO_IN_DATA67	5200 3098h
9Ch	32	GPIO_SET_RIS_TRIG67	5200 309Ch
A0h	32	GPIO_CLR_RIS_TRIG67	5200 30A0h
A4h	32	GPIO_SET_FAL_TRIG67	5200 30A4h
A8h	32	GPIO_CLR_FAL_TRIG67	5200 30A8h
ACh	32	GPIO_INTSTAT67	5200 30ACh
B0h	32	GPIO_DIR8	5200 30B0h
B4h	32	GPIO_OUT_DATA8	5200 30B4h
B8h	32	GPIO_SET_DATA8	5200 30B8h
BCh	32	GPIO_CLR_DATA8	5200 30BCh
C0h	32	GPIO_IN_DATA8	5200 30C0h
C4h	32	GPIO_SET_RIS_TRIG8	5200 30C4h
C8h	32	GPIO_CLR_RIS_TRIG8	5200 30C8h
CCh	32	GPIO_SET_FAL_TRIG8	5200 30CCh
D0h	32	GPIO_CLR_FAL_TRIG8	5200 30D0h
D4h	32	GPIO_INTSTAT8	5200 30D4h

5.8.2 GPIO Registers

GPIO Registers

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5.8.2.1 GPIO_PID Register

5.8.2.1.1 GPIO_PID Register (Offset = 0h) [reset = 44832905h]

GPIO Periperal ID Register.

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Table 5-1501. Instance Table

Instance Name	Physical Address
GPIO0	5200 0000h
GPIO1	5200 1000h
GPIO2	5200 2000h
GPIO3	5200 3000h

Figure 5-735. GPIO_PID Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">RESERVED</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">0h</td><td colspan="4">483h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">483h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RTL</td><td colspan="3">MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">5h</td><td colspan="3">1h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">5h</td></tr>
</table>

Table 5-1502. GPIO_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Current scheme
29:28	RESERVED	R	0h	RESERVED
27:16	FUNC	R	483h	Function code assigned to TCP3
15:11	RTL	R	5h	RTL Version R code
10:8	MAJOR	R	1h	Major revision X code
7:6	CUSTOM	R	0h	Custom version code
5:0	MINOR	R	5h	Minor revision Y code

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5.8.2.2 GPIO_PCR Register

5.8.2.2.1 GPIO_PCR Register (Offset = 4h) [reset = 1h]

Peripheral Control Register.

Return to Summary Table

Table 5-1503. Instance Table

Instance Name	Physical Address
GPIO0	5200 0004h
GPIO1	5200 1004h
GPIO2	5200 2004h
GPIO3	5200 3004h

Figure 5-736. GPIO_PCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						R	R
0h						0h	1h

Table 5-1504. GPIO_PCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT	R	0h	Used in conjunction with FREE bit to determine the emulation suspend mode.
0	FREE	R	1h	For GPIO, the FREE bit is fixed at 1, which means GPIO runs free in emulation suspend.

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5.8.2.3 GPIO_BINTEN Register

5.8.2.3.1 GPIO_BINTEN Register (Offset = 8h) [reset = 0h]

Bit Interrupt Enable Register.

Return to Summary Table

Table 5-1505. Instance Table

Instance Name	Physical Address
GPIO0	5200 0008h
GPIO1	5200 1008h
GPIO2	5200 2008h
GPIO3	5200 3008h

Figure 5-737. GPIO_BINTEN Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
EN							
R/W							
0h							
7	6	5	4	3	2	1	0
EN							
R/W							
0h							

Table 5-1506. GPIO_BINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	EN	R/W	0h	Per bank interrupt enable. 0 = disable, 1 = enable.

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5.8.2.4 GPIO_DIR01 Register

5.8.2.4.1 GPIO_DIR01 Register (Offset = 10h) [reset = FFFFFFFFh]

Direction Register.

Return to Summary Table

Table 5-1507. Instance Table

Instance Name	Physical Address
GPIO0	5200 0010h
GPIO1	5200 1010h
GPIO2	5200 2010h
GPIO3	5200 3010h

Figure 5-738. GPIO_DIR01 Name Register

31	30	29	28	27	26	25	24
DIR1							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR1							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR0							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR0							
R/W							
FFFFh							

Table 5-1508. GPIO_DIR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR1	R/W	FFFFh	Direction of GPIO bank 1 bits, 0 = output, 1 = input.
15:0	DIR0	R/W	FFFFh	Direction of GPIO bank 0 bits, 0 = output, 1 = input.

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5.8.2.5 GPIO_OUT_DATA01 Register

5.8.2.5.1 GPIO_OUT_DATA01 Register (Offset = 14h) [reset = 0h]

Output Drive State Register.

Return to Summary Table

Table 5-1509. Instance Table

Instance Name	Physical Address
GPIO0	5200 0014h
GPIO1	5200 1014h
GPIO2	5200 2014h
GPIO3	5200 3014h

Figure 5-739. GPIO_OUT_DATA01 Name Register

31	30	29	28	27	26	25	24
OUT1							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT1							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT0							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT0							
R/W							
0h							

Table 5-1510. GPIO_OUT_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT1	R/W	0h	Output drive state of GPIO bank 1 bits, does not effect operation when it is configured as input. Reading it returns the output drive state.
15:0	OUT0	R/W	0h	Output drive state of GPIO bank 0 bits, does not effect operation when it is configured as input. Reading it returns the output drive state.

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5.8.2.6 GPIO_SET_DATA01 Register

5.8.2.6.1 GPIO_SET_DATA01 Register (Offset = 18h) [reset = 0h]

Set Output Drive State Register.

Return to Summary Table

Table 5-1511. Instance Table

Instance Name	Physical Address
GPIO0	5200 0018h
GPIO1	5200 1018h
GPIO2	5200 2018h
GPIO3	5200 3018h

Figure 5-740. GPIO_SET_DATA01 Name Register

31	30	29	28	27	26	25	24
SET1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET0							
R/W1TS							
0h							

Table 5-1512. GPIO_SET_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET1	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 1 bits. Reading it returns the output drive state.
15:0	SET0	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 0 bits. Reading it returns the output drive state.

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5.8.2.7 GPIO_CLR_DATA01 Register

5.8.2.7.1 GPIO_CLR_DATA01 Register (Offset = 1Ch) [reset = 0h]

Clear Output Drive State Register.

Return to Summary Table

Table 5-1513. Instance Table

Instance Name	Physical Address
GPIO0	5200 001Ch
GPIO1	5200 101Ch
GPIO2	5200 201Ch
GPIO3	5200 301Ch

Figure 5-741. GPIO_CLR_DATA01 Name Register

31	30	29	28	27	26	25	24
CLR1							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR1							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR0							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR0							
R/W1TC							
0h							

Table 5-1514. GPIO_CLR_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR1	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15:0	CLR0	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

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5.8.2.8 GPIO_IN_DATA01 Register

5.8.2.8.1 GPIO_IN_DATA01 Register (Offset = 20h) [reset = 0h]

Bank Status Register.

Return to Summary Table

Table 5-1515. Instance Table

Instance Name	Physical Address
GPIO0	5200 0020h
GPIO1	5200 1020h
GPIO2	5200 2020h
GPIO3	5200 3020h

Figure 5-742. GPIO_IN_DATA01 Name Register

31	30	29	28	27	26	25	24
IN1							
R							
0h							
23	22	21	20	19	18	17	16
IN1							
R							
0h							
15	14	13	12	11	10	9	8
IN0							
R							
0h							
7	6	5	4	3	2	1	0
IN0							
R							
0h							

Table 5-1516. GPIO_IN_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN1	R	0h	Status of GPIO bank 1 bits.
15:0	IN0	R	0h	Status of GPIO bank 0 bits.

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5.8.2.9 GPIO_SET_RIS_TRIG01 Register

5.8.2.9.1 GPIO_SET_RIS_TRIG01 Register (Offset = 24h) [reset = 0h]

Set Rising Edge Detection Register.

Return to Summary Table

Table 5-1517. Instance Table

Instance Name	Physical Address
GPIO0	5200 0024h
GPIO1	5200 1024h
GPIO2	5200 2024h
GPIO3	5200 3024h

Figure 5-743. GPIO_SET_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24
SETRIS1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS0							
R/W1TS							
0h							

Table 5-1518. GPIO_SET_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS1	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 1 bits.
15:0	SETRIS0	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 0 bits.

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5.8.2.10 GPIO_CLR_RIS_TRIG01 Register

5.8.2.10.1 GPIO_CLR_RIS_TRIG01 Register (Offset = 28h) [reset = 0h]

Clear Rising Edge Detection Register.

Return to Summary Table

Table 5-1519. Instance Table

Instance Name	Physical Address
GPIO0	5200 0028h
GPIO1	5200 1028h
GPIO2	5200 2028h
GPIO3	5200 3028h

Figure 5-744. GPIO_CLR_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24
CLRRIS1							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS1							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS0							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS0							
R/W1TC							
0h							

Table 5-1520. GPIO_CLR_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS1	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 1 bits.
15:0	CLRRIS0	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 0 bits.

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5.8.2.11 GPIO_SET_FAL_TRIG01 Register

5.8.2.11.1 GPIO_SET_FAL_TRIG01 Register (Offset = 2Ch) [reset = 0h]

Set Falling Edge Detection Register.

Return to Summary Table

Table 5-1521. Instance Table

Instance Name	Physical Address
GPIO0	5200 002Ch
GPIO1	5200 102Ch
GPIO2	5200 202Ch
GPIO3	5200 302Ch

Figure 5-745. GPIO_SET_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24
SETFAL1							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL1							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL0							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL0							
R/W1TS							
0h							

Table 5-1522. GPIO_SET_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL1	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 1 bits.
15:0	SETFAL0	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 0 bits.

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5.8.2.12 GPIO_CLR_FAL_TRIG01 Register

5.8.2.12.1 GPIO_CLR_FAL_TRIG01 Register (Offset = 30h) [reset = 0h]

Clear Falling Edge Detection Register.

Return to Summary Table

Table 5-1523. Instance Table

Instance Name	Physical Address
GPIO0	5200 0030h
GPIO1	5200 1030h
GPIO2	5200 2030h
GPIO3	5200 3030h

Figure 5-746. GPIO_CLR_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24
CLRFAL1							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL1							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL0							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL0							
R/W1TC							
0h							

Table 5-1524. GPIO_CLR_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL1	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 1 bits.
15:0	CLRFAL0	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 0 bits.

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5.8.2.13 GPIO_INTSTAT01 Register

5.8.2.13.1 GPIO_INTSTAT01 Register (Offset = 34h) [reset = 0h]

Bank Interrupt Status Register.

Return to Summary Table

Table 5-1525. Instance Table

Instance Name	Physical Address
GPIO0	5200 0034h
GPIO1	5200 1034h
GPIO2	5200 2034h
GPIO3	5200 3034h

Figure 5-747. GPIO_INTSTAT01 Name Register

31	30	29	28	27	26	25	24
STAT1							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT1							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT0							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT0							
R/W1TC							
0h							

Table 5-1526. GPIO_INTSTAT01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT1	R/W1TC	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15:0	STAT0	R/W1TC	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

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5.8.2.14 GPIO_DIR23 Register

5.8.2.14.1 GPIO_DIR23 Register (Offset = 38h) [reset = FFFFFFFFh]

Direction Register.

Return to Summary Table

Table 5-1527. Instance Table

Instance Name	Physical Address
GPIO0	5200 0038h
GPIO1	5200 1038h
GPIO2	5200 2038h
GPIO3	5200 3038h

Figure 5-748. GPIO_DIR23 Name Register

31	30	29	28	27	26	25	24
DIR3							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR3							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR2							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR2							
R/W							
FFFFh							

Table 5-1528. GPIO_DIR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR3	R/W	FFFFh	Direction of GPIO bank 3 bits, 0 = output, 1 = input.
15:0	DIR2	R/W	FFFFh	Direction of GPIO bank 2 bits, 0 = output, 1 = input.

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5.8.2.15 GPIO_OUT_DATA23 Register

5.8.2.15.1 GPIO_OUT_DATA23 Register (Offset = 3Ch) [reset = 0h]

Output Drive State Register.

Return to Summary Table

Table 5-1529. Instance Table

Instance Name	Physical Address
GPIO0	5200 003Ch
GPIO1	5200 103Ch
GPIO2	5200 203Ch
GPIO3	5200 303Ch

Figure 5-749. GPIO_OUT_DATA23 Name Register

31	30	29	28	27	26	25	24
OUT3							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT3							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT2							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT2							
R/W							
0h							

Table 5-1530. GPIO_OUT_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT3	R/W	0h	Output drive state of GPIO bank 3 bits, does not effect operation when it is configured as input. Reading it returns the output drive state.
15:0	OUT2	R/W	0h	Output drive state of GPIO bank 2 bits, does not effect operation when it is configured as input. Reading it returns the output drive state.

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5.8.2.16 GPIO_SET_DATA23 Register

5.8.2.16.1 GPIO_SET_DATA23 Register (Offset = 40h) [reset = 0h]

Set Output Drive State Register.

Return to Summary Table

Table 5-1531. Instance Table

Instance Name	Physical Address
GPIO0	5200 0040h
GPIO1	5200 1040h
GPIO2	5200 2040h
GPIO3	5200 3040h

Figure 5-750. GPIO_SET_DATA23 Name Register

31	30	29	28	27	26	25	24
SET3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET2							
R/W1TS							
0h							

Table 5-1532. GPIO_SET_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET3	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 3 bits. Reading it returns the output drive state.
15:0	SET2	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 2 bits. Reading it returns the output drive state.

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5.8.2.17 GPIO_CLR_DATA23 Register

5.8.2.17.1 GPIO_CLR_DATA23 Register (Offset = 44h) [reset = 0h]

Clear Output Drive State Register.

Return to Summary Table

Table 5-1533. Instance Table

Instance Name	Physical Address
GPIO0	5200 0044h
GPIO1	5200 1044h
GPIO2	5200 2044h
GPIO3	5200 3044h

Figure 5-751. GPIO_CLR_DATA23 Name Register

31	30	29	28	27	26	25	24
CLR3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR2							
R/W1TC							
0h							

Table 5-1534. GPIO_CLR_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR3	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15:0	CLR2	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

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5.8.2.18 GPIO_IN_DATA23 Register

5.8.2.18.1 GPIO_IN_DATA23 Register (Offset = 48h) [reset = 0h]

Bank Status Register.

Return to Summary Table

Table 5-1535. Instance Table

Instance Name	Physical Address
GPIO0	5200 0048h
GPIO1	5200 1048h
GPIO2	5200 2048h
GPIO3	5200 3048h

Figure 5-752. GPIO_IN_DATA23 Name Register

31	30	29	28	27	26	25	24
IN3							
R							
0h							
23	22	21	20	19	18	17	16
IN3							
R							
0h							
15	14	13	12	11	10	9	8
IN2							
R							
0h							
7	6	5	4	3	2	1	0
IN2							
R							
0h							

Table 5-1536. GPIO_IN_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN3	R	0h	Status of GPIO bank 3 bits.
15:0	IN2	R	0h	Status of GPIO bank 2 bits.

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5.8.2.19 GPIO_SET_RIS_TRIG23 Register

5.8.2.19.1 GPIO_SET_RIS_TRIG23 Register (Offset = 4Ch) [reset = 0h]

Set Rising Edge Detection Register.

Return to Summary Table

Table 5-1537. Instance Table

Instance Name	Physical Address
GPIO0	5200 004Ch
GPIO1	5200 104Ch
GPIO2	5200 204Ch
GPIO3	5200 304Ch

Figure 5-753. GPIO_SET_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24
SETRIS3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS2							
R/W1TS							
0h							

Table 5-1538. GPIO_SET_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS3	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 3 bits.
15:0	SETRIS2	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 2 bits.

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5.8.2.20 GPIO_CLR_RIS_TRIG23 Register

5.8.2.20.1 GPIO_CLR_RIS_TRIG23 Register (Offset = 50h) [reset = 0h]

Clear Rising Edge Detection Register.

Return to Summary Table

Table 5-1539. Instance Table

Instance Name	Physical Address
GPIO0	5200 0050h
GPIO1	5200 1050h
GPIO2	5200 2050h
GPIO3	5200 3050h

Figure 5-754. GPIO_CLR_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24
CLRRIS3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS2							
R/W1TC							
0h							

Table 5-1540. GPIO_CLR_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS3	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 3 bits.
15:0	CLRRIS2	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 2 bits.

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5.8.2.21 GPIO_SET_FAL_TRIG23 Register

5.8.2.21.1 GPIO_SET_FAL_TRIG23 Register (Offset = 54h) [reset = 0h]

Set Falling Edge Detection Register.

Return to Summary Table

Table 5-1541. Instance Table

Instance Name	Physical Address
GPIO0	5200 0054h
GPIO1	5200 1054h
GPIO2	5200 2054h
GPIO3	5200 3054h

Figure 5-755. GPIO_SET_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24
SETFAL3							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL3							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL2							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL2							
R/W1TS							
0h							

Table 5-1542. GPIO_SET_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL3	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 3 bits.
15:0	SETFAL2	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 2 bits.

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5.8.2.22 GPIO_CLR_FAL_TRIG23 Register

5.8.2.22.1 GPIO_CLR_FAL_TRIG23 Register (Offset = 58h) [reset = 0h]

Clear Falling Edge Detection Register.

Return to Summary Table

Table 5-1543. Instance Table

Instance Name	Physical Address
GPIO0	5200 0058h
GPIO1	5200 1058h
GPIO2	5200 2058h
GPIO3	5200 3058h

Figure 5-756. GPIO_CLR_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24
CLRFAL3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL2							
R/W1TC							
0h							

Table 5-1544. GPIO_CLR_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL3	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 3 bits.
15:0	CLRFAL2	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 2 bits.

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5.8.2.23 GPIO_INTSTAT23 Register

5.8.2.23.1 GPIO_INTSTAT23 Register (Offset = 5Ch) [reset = 0h]

Bank Interrupt Status Register.

Return to Summary Table

Table 5-1545. Instance Table

Instance Name	Physical Address
GPIO0	5200 005Ch
GPIO1	5200 105Ch
GPIO2	5200 205Ch
GPIO3	5200 305Ch

Figure 5-757. GPIO_INTSTAT23 Name Register

31	30	29	28	27	26	25	24
STAT3							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT3							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT2							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT2							
R/W1TC							
0h							

Table 5-1546. GPIO_INTSTAT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT3	R/W1TC	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15:0	STAT2	R/W1TC	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

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5.8.2.24 GPIO_DIR45 Register

5.8.2.24.1 GPIO_DIR45 Register (Offset = 60h) [reset = FFFFFFFFh]

Direction Register.

Return to Summary Table

Table 5-1547. Instance Table

Instance Name	Physical Address
GPIO0	5200 0060h
GPIO1	5200 1060h
GPIO2	5200 2060h
GPIO3	5200 3060h

Figure 5-758. GPIO_DIR45 Name Register

31	30	29	28	27	26	25	24
DIR5							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR5							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR4							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR4							
R/W							
FFFFh							

Table 5-1548. GPIO_DIR45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR5	R/W	FFFFh	Direction of GPIO bank 5 bits, 0 = output, 1 = input.
15:0	DIR4	R/W	FFFFh	Direction of GPIO bank 4 bits, 0 = output, 1 = input.

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5.8.2.25 GPIO_OUT_DATA45 Register

5.8.2.25.1 GPIO_OUT_DATA45 Register (Offset = 64h) [reset = 0h]

Output Drive State Register.

Return to Summary Table

Table 5-1549. Instance Table

Instance Name	Physical Address
GPIO0	5200 0064h
GPIO1	5200 1064h
GPIO2	5200 2064h
GPIO3	5200 3064h

Figure 5-759. GPIO_OUT_DATA45 Name Register

31	30	29	28	27	26	25	24
OUT5							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT5							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT4							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT4							
R/W							
0h							

Table 5-1550. GPIO_OUT_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT5	R/W	0h	Output drive state of GPIO bank 5 bits, does not effect operation when it is configured as input. Reading it returns the output drive state.
15:0	OUT4	R/W	0h	Output drive state of GPIO bank 4 bits, does not effect operation when it is configured as input. Reading it returns the output drive state.

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5.8.2.26 GPIO_SET_DATA45 Register

5.8.2.26.1 GPIO_SET_DATA45 Register (Offset = 68h) [reset = 0h]

Set Output Drive State Register.

Return to Summary Table

Table 5-1551. Instance Table

Instance Name	Physical Address
GPIO0	5200 0068h
GPIO1	5200 1068h
GPIO2	5200 2068h
GPIO3	5200 3068h

Figure 5-760. GPIO_SET_DATA45 Name Register

31	30	29	28	27	26	25	24
SET5							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET5							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET4							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET4							
R/W1TS							
0h							

Table 5-1552. GPIO_SET_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET5	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 5 bits. Reading it returns the output drive state.
15:0	SET4	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 4 bits. Reading it returns the output drive state.

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5.8.2.27 GPIO_CLR_DATA45 Register

5.8.2.27.1 GPIO_CLR_DATA45 Register (Offset = 6Ch) [reset = 0h]

Clear Output Drive State Register.

Return to Summary Table

Table 5-1553. Instance Table

Instance Name	Physical Address
GPIO0	5200 006Ch
GPIO1	5200 106Ch
GPIO2	5200 206Ch
GPIO3	5200 306Ch

Figure 5-761. GPIO_CLR_DATA45 Name Register

31	30	29	28	27	26	25	24
CLR5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR4							
R/W1TC							
0h							

Table 5-1554. GPIO_CLR_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR5	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15:0	CLR4	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

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5.8.2.28 GPIO_IN_DATA45 Register

5.8.2.28.1 GPIO_IN_DATA45 Register (Offset = 70h) [reset = 0h]

Bank Status Register.

Return to Summary Table

Table 5-1555. Instance Table

Instance Name	Physical Address
GPIO0	5200 0070h
GPIO1	5200 1070h
GPIO2	5200 2070h
GPIO3	5200 3070h

Figure 5-762. GPIO_IN_DATA45 Name Register

31	30	29	28	27	26	25	24
IN5							
R							
0h							
23	22	21	20	19	18	17	16
IN5							
R							
0h							
15	14	13	12	11	10	9	8
IN4							
R							
0h							
7	6	5	4	3	2	1	0
IN4							
R							
0h							

Table 5-1556. GPIO_IN_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN5	R	0h	Status of GPIO bank 5 bits.
15:0	IN4	R	0h	Status of GPIO bank 4 bits.

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5.8.2.29 GPIO_SET_RIS_TRIG45 Register

5.8.2.29.1 GPIO_SET_RIS_TRIG45 Register (Offset = 74h) [reset = 0h]

Set Rising Edge Detection Register.

Return to Summary Table

Table 5-1557. Instance Table

Instance Name	Physical Address
GPIO0	5200 0074h
GPIO1	5200 1074h
GPIO2	5200 2074h
GPIO3	5200 3074h

Figure 5-763. GPIO_SET_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24
SETRIS5							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS5							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS4							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS4							
R/W1TS							
0h							

Table 5-1558. GPIO_SET_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS5	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 5 bits.
15:0	SETRIS4	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 4 bits.

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5.8.2.30 GPIO_CLR_RIS_TRIG45 Register

5.8.2.30.1 GPIO_CLR_RIS_TRIG45 Register (Offset = 78h) [reset = 0h]

Clear Rising Edge Detection Register.

Return to Summary Table

Table 5-1559. Instance Table

Instance Name	Physical Address
GPIO0	5200 0078h
GPIO1	5200 1078h
GPIO2	5200 2078h
GPIO3	5200 3078h

Figure 5-764. GPIO_CLR_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24
CLRRIS5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS4							
R/W1TC							
0h							

Table 5-1560. GPIO_CLR_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS5	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 5 bits.
15:0	CLRRIS4	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 4 bits.

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5.8.2.31 GPIO_SET_FAL_TRIG45 Register

5.8.2.31.1 GPIO_SET_FAL_TRIG45 Register (Offset = 7Ch) [reset = 0h]

Set Falling Edge Detection Register.

Return to Summary Table

Table 5-1561. Instance Table

Instance Name	Physical Address
GPIO0	5200 007Ch
GPIO1	5200 107Ch
GPIO2	5200 207Ch
GPIO3	5200 307Ch

Figure 5-765. GPIO_SET_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24
SETFAL5							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL5							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL4							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL4							
R/W1TS							
0h							

Table 5-1562. GPIO_SET_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL5	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 5 bits.
15:0	SETFAL4	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 4 bits.

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5.8.2.32 GPIO_CLR_FAL_TRIG45 Register

5.8.2.32.1 GPIO_CLR_FAL_TRIG45 Register (Offset = 80h) [reset = 0h]

Clear Falling Edge Detection Register.

Return to Summary Table

Table 5-1563. Instance Table

Instance Name	Physical Address
GPIO0	5200 0080h
GPIO1	5200 1080h
GPIO2	5200 2080h
GPIO3	5200 3080h

Figure 5-766. GPIO_CLR_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24
CLRFAL5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL4							
R/W1TC							
0h							

Table 5-1564. GPIO_CLR_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL5	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 5 bits.
15:0	CLRFAL4	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 4 bits.

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5.8.2.33 GPIO_INTSTAT45 Register

5.8.2.33.1 GPIO_INTSTAT45 Register (Offset = 84h) [reset = 0h]

Bank Interrupt Status Register.

Return to Summary Table

Table 5-1565. Instance Table

Instance Name	Physical Address
GPIO0	5200 0084h
GPIO1	5200 1084h
GPIO2	5200 2084h
GPIO3	5200 3084h

Figure 5-767. GPIO_INTSTAT45 Name Register

31	30	29	28	27	26	25	24
STAT5							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT5							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT4							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT4							
R/W1TC							
0h							

Table 5-1566. GPIO_INTSTAT45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT5	R/W1TC	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15:0	STAT4	R/W1TC	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

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5.8.2.34 GPIO_DIR67 Register

5.8.2.34.1 GPIO_DIR67 Register (Offset = 88h) [reset = FFFFFFFFh]

Direction Register.

Return to Summary Table

Table 5-1567. Instance Table

Instance Name	Physical Address
GPIO0	5200 0088h
GPIO1	5200 1088h
GPIO2	5200 2088h
GPIO3	5200 3088h

Figure 5-768. GPIO_DIR67 Name Register

31	30	29	28	27	26	25	24
DIR7							
R/W							
FFFFh							
23	22	21	20	19	18	17	16
DIR7							
R/W							
FFFFh							
15	14	13	12	11	10	9	8
DIR6							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR6							
R/W							
FFFFh							

Table 5-1568. GPIO_DIR67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	DIR7	R/W	FFFFh	Direction of GPIO bank 7 bits, 0 = output, 1 = input.
15:0	DIR6	R/W	FFFFh	Direction of GPIO bank 6 bits, 0 = output, 1 = input.

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5.8.2.35 GPIO_OUT_DATA67 Register

5.8.2.35.1 GPIO_OUT_DATA67 Register (Offset = 8Ch) [reset = 0h]

Output Drive State Register.

Return to Summary Table

Table 5-1569. Instance Table

Instance Name	Physical Address
GPIO0	5200 008Ch
GPIO1	5200 108Ch
GPIO2	5200 208Ch
GPIO3	5200 308Ch

Figure 5-769. GPIO_OUT_DATA67 Name Register

31	30	29	28	27	26	25	24
OUT7							
R/W							
0h							
23	22	21	20	19	18	17	16
OUT7							
R/W							
0h							
15	14	13	12	11	10	9	8
OUT6							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT6							
R/W							
0h							

Table 5-1570. GPIO_OUT_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	OUT7	R/W	0h	Output drive state of GPIO bank 7 bits, does not effect operation when it is configured as input. Reading it returns the output drive state.
15:0	OUT6	R/W	0h	Output drive state of GPIO bank 6 bits, does not effect operation when it is configured as input. Reading it returns the output drive state.

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5.8.2.36 GPIO_SET_DATA67 Register

5.8.2.36.1 GPIO_SET_DATA67 Register (Offset = 90h) [reset = 0h]

Set Output Drive State Register.

Return to Summary Table

Table 5-1571. Instance Table

Instance Name	Physical Address
GPIO0	5200 0090h
GPIO1	5200 1090h
GPIO2	5200 2090h
GPIO3	5200 3090h

Figure 5-770. GPIO_SET_DATA67 Name Register

31	30	29	28	27	26	25	24
SET7							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SET7							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SET6							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET6							
R/W1TS							
0h							

Table 5-1572. GPIO_SET_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SET7	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 7 bits. Reading it returns the output drive state.
15:0	SET6	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 6 bits. Reading it returns the output drive state.

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5.8.2.37 GPIO_CLR_DATA67 Register

5.8.2.37.1 GPIO_CLR_DATA67 Register (Offset = 94h) [reset = 0h]

Clear Output Drive State Register.

Return to Summary Table

Table 5-1573. Instance Table

Instance Name	Physical Address
GPIO0	5200 0094h
GPIO1	5200 1094h
GPIO2	5200 2094h
GPIO3	5200 3094h

Figure 5-771. GPIO_CLR_DATA67 Name Register

31	30	29	28	27	26	25	24
CLR7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLR7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLR6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR6							
R/W1TC							
0h							

Table 5-1574. GPIO_CLR_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLR7	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15:0	CLR6	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

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5.8.2.38 GPIO_IN_DATA67 Register

5.8.2.38.1 GPIO_IN_DATA67 Register (Offset = 98h) [reset = 0h]

Bank Status Register.

Return to Summary Table

Table 5-1575. Instance Table

Instance Name	Physical Address
GPIO0	5200 0098h
GPIO1	5200 1098h
GPIO2	5200 2098h
GPIO3	5200 3098h

Figure 5-772. GPIO_IN_DATA67 Name Register

31	30	29	28	27	26	25	24
IN7							
R							
0h							
23	22	21	20	19	18	17	16
IN7							
R							
0h							
15	14	13	12	11	10	9	8
IN6							
R							
0h							
7	6	5	4	3	2	1	0
IN6							
R							
0h							

Table 5-1576. GPIO_IN_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	IN7	R	0h	Status of GPIO bank 7 bits.
15:0	IN6	R	0h	Status of GPIO bank 6 bits.

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5.8.2.39 GPIO_SET_RIS_TRIG67 Register

5.8.2.39.1 GPIO_SET_RIS_TRIG67 Register (Offset = 9Ch) [reset = 0h]

Set Rising Edge Detection Register.

Return to Summary Table

Table 5-1577. Instance Table

Instance Name	Physical Address
GPIO0	5200 009Ch
GPIO1	5200 109Ch
GPIO2	5200 209Ch
GPIO3	5200 309Ch

Figure 5-773. GPIO_SET_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24
SETRIS7							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETRIS7							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETRIS6							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS6							
R/W1TS							
0h							

Table 5-1578. GPIO_SET_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETRIS7	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 7 bits.
15:0	SETRIS6	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 6 bits.

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5.8.2.40 GPIO_CLR_RIS_TRIG67 Register

5.8.2.40.1 GPIO_CLR_RIS_TRIG67 Register (Offset = A0h) [reset = 0h]

Clear Rising Edge Detection Register.

Return to Summary Table

Table 5-1579. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A0h
GPIO1	5200 10A0h
GPIO2	5200 20A0h
GPIO3	5200 30A0h

Figure 5-774. GPIO_CLR_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24
CLRRIS7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRRIS7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRRIS6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS6							
R/W1TC							
0h							

Table 5-1580. GPIO_CLR_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRRIS7	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 7 bits.
15:0	CLRRIS6	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 6 bits.

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5.8.2.41 GPIO_SET_FAL_TRIG67 Register

5.8.2.41.1 GPIO_SET_FAL_TRIG67 Register (Offset = A4h) [reset = 0h]

Set Falling Edge Detection Register.

Return to Summary Table

Table 5-1581. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A4h
GPIO1	5200 10A4h
GPIO2	5200 20A4h
GPIO3	5200 30A4h

Figure 5-775. GPIO_SET_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24
SETFAL7							
R/W1TS							
0h							
23	22	21	20	19	18	17	16
SETFAL7							
R/W1TS							
0h							
15	14	13	12	11	10	9	8
SETFAL6							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL6							
R/W1TS							
0h							

Table 5-1582. GPIO_SET_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	SETFAL7	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 7 bits.
15:0	SETFAL6	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 6 bits.

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5.8.2.42 GPIO_CLR_FAL_TRIG67 Register

5.8.2.42.1 GPIO_CLR_FAL_TRIG67 Register (Offset = A8h) [reset = 0h]

Clear Falling Edge Detection Register.

Return to Summary Table

Table 5-1583. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A8h
GPIO1	5200 10A8h
GPIO2	5200 20A8h
GPIO3	5200 30A8h

Figure 5-776. GPIO_CLR_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24
CLRFAL7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
CLRFAL7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
CLRFAL6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL6							
R/W1TC							
0h							

Table 5-1584. GPIO_CLR_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	CLRFAL7	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 7 bits.
15:0	CLRFAL6	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 6 bits.

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5.8.2.43 GPIO_INTSTAT67 Register

5.8.2.43.1 GPIO_INTSTAT67 Register (Offset = ACh) [reset = 0h]

Bank Interrupt Status Register.

Return to Summary Table

Table 5-1585. Instance Table

Instance Name	Physical Address
GPIO0	5200 00ACh
GPIO1	5200 10ACh
GPIO2	5200 20ACh
GPIO3	5200 30ACh

Figure 5-777. GPIO_INTSTAT67 Name Register

31	30	29	28	27	26	25	24
STAT7							
R/W1TC							
0h							
23	22	21	20	19	18	17	16
STAT7							
R/W1TC							
0h							
15	14	13	12	11	10	9	8
STAT6							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT6							
R/W1TC							
0h							

Table 5-1586. GPIO_INTSTAT67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	STAT7	R/W1TC	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15:0	STAT6	R/W1TC	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

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5.8.2.44 GPIO_DIR8 Register

5.8.2.44.1 GPIO_DIR8 Register (Offset = B0h) [reset = FFFFFFFFh]

Direction Register.

Return to Summary Table

Table 5-1587. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B0h
GPIO1	5200 10B0h
GPIO2	5200 20B0h
GPIO3	5200 30B0h

Figure 5-778. GPIO_DIR8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
FFFFh							
23	22	21	20	19	18	17	16
RESERVED							
R							
FFFFh							
15	14	13	12	11	10	9	8
DIR8							
R/W							
FFFFh							
7	6	5	4	3	2	1	0
DIR8							
R/W							
FFFFh							

Table 5-1588. GPIO_DIR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	FFFFh	RESERVED
15:0	DIR8	R/W	FFFFh	Direction of GPIO bank 8 bits, 0 = output, 1 = input.

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5.8.2.45 GPIO_OUT_DATA8 Register

5.8.2.45.1 GPIO_OUT_DATA8 Register (Offset = B4h) [reset = 0h]

Output Drive State Register.

Return to Summary Table

Table 5-1589. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B4h
GPIO1	5200 10B4h
GPIO2	5200 20B4h
GPIO3	5200 30B4h

Figure 5-779. GPIO_OUT_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
OUT8							
R/W							
0h							
7	6	5	4	3	2	1	0
OUT8							
R/W							
0h							

Table 5-1590. GPIO_OUT_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	OUT8	R/W	0h	Output drive state of GPIO bank 8 bits, does not effect operation when it is configured as input. Reading it returns the output drive state.

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5.8.2.46 GPIO_SET_DATA8 Register

5.8.2.46.1 GPIO_SET_DATA8 Register (Offset = B8h) [reset = 0h]

Set Output Drive State Register.

Return to Summary Table

Table 5-1591. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B8h
GPIO1	5200 10B8h
GPIO2	5200 20B8h
GPIO3	5200 30B8h

Figure 5-780. GPIO_SET_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
SET8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SET8							
R/W1TS							
0h							

Table 5-1592. GPIO_SET_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	SET8	R/W1TS	0h	Writing 1 sets the output drive state of GPIO bank 8 bits. Reading it returns the output drive state.

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5.8.2.47 GPIO_CLR_DATA8 Register

5.8.2.47.1 GPIO_CLR_DATA8 Register (Offset = BCh) [reset = 0h]

Clear Output Drive State Register.

Return to Summary Table

Table 5-1593. Instance Table

Instance Name	Physical Address
GPIO0	5200 00BCh
GPIO1	5200 10BCh
GPIO2	5200 20BCh
GPIO3	5200 30BCh

Figure 5-781. GPIO_CLR_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
CLR8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLR8							
R/W1TC							
0h							

Table 5-1594. GPIO_CLR_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	CLR8	R/W1TC	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

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5.8.2.48 GPIO_IN_DATA8 Register

5.8.2.48.1 GPIO_IN_DATA8 Register (Offset = C0h) [reset = 0h]

Bank Status Register.

Return to Summary Table

Table 5-1595. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C0h
GPIO1	5200 10C0h
GPIO2	5200 20C0h
GPIO3	5200 30C0h

Figure 5-782. GPIO_IN_DATA8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
IN8							
R							
0h							
7	6	5	4	3	2	1	0
IN8							
R							
0h							

Table 5-1596. GPIO_IN_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	IN8	R	0h	Status of GPIO bank 8 bits.

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5.8.2.49 GPIO_SET_RIS_TRIG8 Register

5.8.2.49.1 GPIO_SET_RIS_TRIG8 Register (Offset = C4h) [reset = 0h]

Set Rising Edge Detection Register.

Return to Summary Table

Table 5-1597. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C4h
GPIO1	5200 10C4h
GPIO2	5200 20C4h
GPIO3	5200 30C4h

Figure 5-783. GPIO_SET_RIS_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SETRIS8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETRIS8							
R/W1TS							
0h							

Table 5-1598. GPIO_SET_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SETRIS8	R/W1TS	0h	Writing 1 enables rising edge detection for GPIO bank 8 bits.

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5.8.2.50 GPIO_CLR_RIS_TRIG8 Register

5.8.2.50.1 GPIO_CLR_RIS_TRIG8 Register (Offset = C8h) [reset = 0h]

Clear Rising Edge Detection Register.

Return to Summary Table

Table 5-1599. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C8h
GPIO1	5200 10C8h
GPIO2	5200 20C8h
GPIO3	5200 30C8h

Figure 5-784. GPIO_CLR_RIS_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLRRIS8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRRIS8							
R/W1TC							
0h							

Table 5-1600. GPIO_CLR_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLRRIS8	R/W1TC	0h	Writing 1 clears rising edge detection for GPIO bank 8 bits.

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5.8.2.51 GPIO_SET_FAL_TRIG8 Register

5.8.2.51.1 GPIO_SET_FAL_TRIG8 Register (Offset = CCh) [reset = 0h]

Set Falling Edge Detection Register.

Return to Summary Table

Table 5-1601. Instance Table

Instance Name	Physical Address
GPIO0	5200 00CCh
GPIO1	5200 10CCh
GPIO2	5200 20CCh
GPIO3	5200 30CCh

Figure 5-785. GPIO_SET_FAL_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
SETFAL8							
R/W1TS							
0h							
7	6	5	4	3	2	1	0
SETFAL8							
R/W1TS							
0h							

Table 5-1602. GPIO_SET_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	SETFAL8	R/W1TS	0h	Writing 1 enables falling edge detection for for GPIO bank 8 bits.

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5.8.2.52 GPIO_CLR_FAL_TRIG8 Register

5.8.2.52.1 GPIO_CLR_FAL_TRIG8 Register (Offset = D0h) [reset = 0h]

Clear Falling Edge Detection Register.

Return to Summary Table

Table 5-1603. Instance Table

Instance Name	Physical Address
GPIO0	5200 00D0h
GPIO1	5200 10D0h
GPIO2	5200 20D0h
GPIO3	5200 30D0h

Figure 5-786. GPIO_CLR_FAL_TRIG8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
CLRFAL8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
CLRFAL8							
R/W1TC							
0h							

Table 5-1604. GPIO_CLR_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	NONE	0h	Reserved
15:0	CLRFAL8	R/W1TC	0h	Writing 1 clears falling edge detection for for GPIO bank 8 bits.

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5.8.2.53 GPIO_INTSTAT8 Register

5.8.2.53.1 GPIO_INTSTAT8 Register (Offset = D4h) [reset = 0h]

Bank Interrupt Status Register.

Return to Summary Table

Table 5-1605. Instance Table

Instance Name	Physical Address
GPIO0	5200 00D4h
GPIO1	5200 10D4h
GPIO2	5200 20D4h
GPIO3	5200 30D4h

Figure 5-787. GPIO_INTSTAT8 Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
STAT8							
R/W1TC							
0h							
7	6	5	4	3	2	1	0
STAT8							
R/W1TC							
0h							

Table 5-1606. GPIO_INTSTAT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	RESERVED
15:0	STAT8	R/W1TC	0h	Status of GPIO bank 8 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

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5.9 GPIO_XBAR_INTR

GPIO_XBAR_INTR

5.9.1 GPIO_XBAR_INTR Summaries

GPIO_XBAR_INTR Summaries

Table 5-1607. GPIO_XBAR_INTR Registers, Base Address=52E0 2000h, Length=1024

Offset	Length	Register Name	GPIO_XBAR_INTR Physical Address
0h	32	GPIO_XBAR_INTR_PID	52E0 2000h
4h	32	GPIO_XBAR_INTR_MUXCNTL_J	52E0 2004h + formula

5.9.2 GPIO_XBAR_INTR Registers

GPIO_XBAR_INTR Registers

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5.9.2.1 GPIO_XBAR_INTR_PID Register

5.9.2.1.1 GPIO_XBAR_INTR_PID Register (Offset = 0h) [reset = 66948100h]

Identification register.

Return to Summary Table

Table 5-1608. Instance Table

Instance Name	Physical Address
GPIO_XBAR_INTR	52E0 2000h

Figure 5-788. GPIO_XBAR_INTR_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	22	21	20	19	18	17	16
FUNCTION							
R							
694h							
15	14	13	12	11	10	9	8
RTLVER					MAJREV		
R					R		
10h					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINREV					
R		R					
0h		0h					

Table 5-1609. GPIO_XBAR_INTR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	FUNCTION	R	694h	function
15:11	RTLVER	R	10h	Rtl version
10:8	MAJREV	R	1h	major version
7:6	CUSTOM	R	0h	custom id
5:0	MINREV	R	0h	minor version

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5.9.2.2 GPIO_XBAR_INTR_MUXCNTL_J Register

5.9.2.2.1 GPIO_XBAR_INTR_MUXCNTL_J Register (Offset = 4h) [reset = 0h]

Interrupt mux control register.

Return to Summary Table

Table 5-1610. Instance Table

Instance Name	Physical Address
GPIO_XBAR_INTR	52E0 2004h + formula

Figure 5-789. GPIO_XBAR_INTR_MUXCNTL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							INT_ENABLE
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MUX_CNTL							
R/W							
0h							

Table 5-1611. GPIO_XBAR_INTR_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	Interrupt *j* Output Enable.
15:8	RESERVED	NONE	0h	Reserved
7:0	MUX_CNTL	R/W	0h	Mux Control for Interrupt *j*.

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5.10 I2C

I2C

5.10.1 I2C Summaries

I2C Summaries

Table 5-1612. I2C Registers, Base Address=5250 0000h, Length=128

Offset	Length	Register Name	I2C0 Physical Address	I2C1 Physical Address	I2C2 Physical Address
0h	32	I2C_ICOAR	5250 0000h	5250 1000h	5250 2000h
4h	32	I2C_ICIMR	5250 0004h	5250 1004h	5250 2004h
8h	32	I2C_ICSTR	5250 0008h	5250 1008h	5250 2008h
Ch	32	I2C_ICCLKL	5250 000Ch	5250 100Ch	5250 200Ch
10h	32	I2C_ICCLKH	5250 0010h	5250 1010h	5250 2010h
14h	32	I2C_ICCNT	5250 0014h	5250 1014h	5250 2014h
18h	32	I2C_ICDRR	5250 0018h	5250 1018h	5250 2018h
1Ch	32	I2C_ICSAR	5250 001Ch	5250 101Ch	5250 201Ch
20h	32	I2C_ICDXR	5250 0020h	5250 1020h	5250 2020h
24h	32	I2C_ICMDR	5250 0024h	5250 1024h	5250 2024h
28h	32	I2C_ICIVR	5250 0028h	5250 1028h	5250 2028h
2Ch	32	I2C_ICEMDR	5250 002Ch	5250 102Ch	5250 202Ch
30h	32	I2C_ICPSC	5250 0030h	5250 1030h	5250 2030h
34h	32	I2C_ICPID1	5250 0034h	5250 1034h	5250 2034h
38h	32	I2C_ICPID2	5250 0038h	5250 1038h	5250 2038h
3Ch	32	I2C_ICDMAC	5250 003Ch	5250 103Ch	5250 203Ch
48h	32	I2C_ICPFUNC	5250 0048h	5250 1048h	5250 2048h
4Ch	32	I2C_ICPDIR	5250 004Ch	5250 104Ch	5250 204Ch
50h	32	I2C_ICPDIN	5250 0050h	5250 1050h	5250 2050h
54h	32	I2C_ICPDOUT	5250 0054h	5250 1054h	5250 2054h
58h	32	I2C_ICPDSET	5250 0058h	5250 1058h	5250 2058h
5Ch	32	I2C_ICPDCLR	5250 005Ch	5250 105Ch	5250 205Ch
60h	32	I2C_ICPDRV	5250 0060h	5250 1060h	5250 2060h

Table 5-1613. I2C Registers, Base Address=5250 0000h, Length=128

Offset	Length	Register Name	I2C3 Physical Address
0h	32	I2C_ICOAR	5250 3000h
4h	32	I2C_ICIMR	5250 3004h
8h	32	I2C_ICSTR	5250 3008h
Ch	32	I2C_ICCLKL	5250 300Ch
10h	32	I2C_ICCLKH	5250 3010h
14h	32	I2C_ICCNT	5250 3014h
18h	32	I2C_ICDRR	5250 3018h
1Ch	32	I2C_ICSAR	5250 301Ch
20h	32	I2C_ICDXR	5250 3020h
24h	32	I2C_ICMDR	5250 3024h
28h	32	I2C_ICIVR	5250 3028h
2Ch	32	I2C_ICEMDR	5250 302Ch
30h	32	I2C_ICPSC	5250 3030h

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Table 5-1613. I2C Registers, Base Address=5250 0000h, Length=128 (continued)

Offset	Length	Register Name	I2C3 Physical Address
34h	32	I2C_ICPID1	5250 3034h
38h	32	I2C_ICPID2	5250 3038h
3Ch	32	I2C_ICDMAC	5250 303Ch
48h	32	I2C_ICPFUNC	5250 3048h
4Ch	32	I2C_ICPDIR	5250 304Ch
50h	32	I2C_ICPDIN	5250 3050h
54h	32	I2C_ICPDOUT	5250 3054h
58h	32	I2C_ICPDSET	5250 3058h
5Ch	32	I2C_ICPDCLR	5250 305Ch
60h	32	I2C_ICPDRV	5250 3060h

5.10.2 I2C Registers

I2C Registers

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5.10.2.1 I2C_ICOAR Register

5.10.2.1.1 I2C_ICOAR Register (Offset = 0h) [reset = 0h]

I2C Own Address register

Return to Summary Table

Table 5-1614. Instance Table

Instance Name	Physical Address
I2C0	5250 0000h
I2C1	5250 1000h
I2C2	5250 2000h
I2C3	5250 3000h

Figure 5-790. I2C_ICOAR Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU						A9_A0	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
A9_A0							
R/W							
0h							

Table 5-1615. I2C_ICOAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	NU	R/W	0h	Reserved
9:0	A9_A0	R/W	0h	Own address. Use in both 7- and 10-bit address mode. Note that usercan program the I2C own address to any value as long as it does notconflict with other components in the system.

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5.10.2.2 I2C_ICIMR Register

5.10.2.2.1 I2C_ICIMR Register (Offset = 4h) [reset = 0h]

I2C Interrupt Mask/Status register

Return to Summary Table

Table 5-1616. Instance Table

Instance Name	Physical Address
I2C0	5250 0004h
I2C1	5250 1004h
I2C2	5250 2004h
I2C3	5250 3004h

Figure 5-791. I2C_ICIMR Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
NU	AAS	SCD	ICXRDY	ICRRDY	ARDY	NACK	AL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1617. I2C_ICIMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	NU	R/W	0h	Reserved
6	AAS	R/W	0h	Address As Target interrupt mask bit. Setting a"1" to this bit unmasks the Address As Target interrupt. Setting a"0" to this bit masks the Address As Target interrupt.
5	SCD	R/W	0h	Stop Condition Detection mask bit. Setting a"1" to this bit unmasks the Stop Condition Detection interrupt. Setting a "0" to this bit masks the Stop Condition Detection interrupt.
4	ICXRDY	R/W	0h	Transmit Data Ready interrupt mask bit. Setting a"1" to this bit unmasks the Transmit Data Ready interrupt. Setting a"0" to this bit masks the Transmit Data Ready interrupt.
3	ICRRDY	R/W	0h	Receive Data Ready interrupt mask bit. Setting a"1" to this bit unmasks the Receive Data Ready interrupt. Setting a"0" to this bit masks the Receive Data Ready interrupt.
2	ARDY	R/W	0h	Register access ready interrupt mask bit. Setting a"1" to this bit unmasks the Register access ready interrupt. Setting a"0" to this bit masks the Register access ready interrupt.
1	NACK	R/W	0h	No Acknowledgement interrupt mask bit. Setting a"1" to this bit unmasks the No Acknowledgement interrupt. Setting a"0" to this bit masks the No Acknowledgement interrupt.

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Table 5-1617. I2C_ICIMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AL	R/W	0h	Arbitration Lost interrupt mask bit. Setting a"1" to this bit unmasks the Arbitration Lost interrupt. Setting a"0" to this bit masks the Arbitration Lost interrupt.

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5.10.2.3 I2C_ICSTR Register

5.10.2.3.1 I2C_ICSTR Register (Offset = 8h) [reset = 0h]

I2C Interrupt Status register

Return to Summary Table

Table 5-1618. Instance Table

Instance Name	Physical Address
I2C0	5250 0008h
I2C1	5250 1008h
I2C2	5250 2008h
I2C3	5250 3008h

Figure 5-792. I2C_ICSTR Name Register

31	30	29	28	27	26	25	24
NU2							
NU2							
0h							
23	22	21	20	19	18	17	16
NU2							
NU2							
0h							
15	14	13	12	11	10	9	8
NU2	SDIR	NACKSNT	BB	RSFULL	XSMT	AAS	AD0
NU2	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
NU1		SCD	ICXRDY	ICRRDY	ARDY	NACK	AL
NU1		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 5-1619. I2C_ICSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:15	NU2	NU2	0h	Reserved
14	SDIR	R/W	0h	Target Direction. This bit is clear to '0' indicating the I2C is a master transmitter/receiver or a target receiver. This bit is also clear by STOP condition or START condition. It is set to '1' when the I2C target is a transmitter. In DLB mode [which the configuration should be master-transmitter target-receiver] this bit is clear to '0'. Writing a"1" to this bit to clear it.
13	NACKSNT	R/W	0h	A No Acknowledge is sent due to NACKMOD is set to a"1". NACKSNT 0:A No Acknowledge is not sent. NACKSNT 1:A No Acknowledge is sent. Writing a"1" to this bit to clear it.
12	BB	R/W	0h	Bus Busy. This bit indicates the state of the serial bus. BB 0:The bus is free. BB 1:The bus is occupied. On reception of a"start" condition the device sets BB to 1. This bit is also set if the I2C detects SCL low state. BB is clear to 0 after reception of a"stop" condition. BB is kept to"0" regardless SCL state when the I2C is in reset [IRS_=0]. If the IRS_ is set to"1" during transaction between other I2C devices the BB bit is set at the first falling edge of SCL or START condition. - [RW]

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Table 5-1619. I2C_ICSTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RSFULL	R/W	0h	Receive shift full. This bit indicates whether the receiver has experienced overrun. Overrun occurs when the receive shift register [ICRSR] is full and ICDRR has not been read since the ICRSR-to-ICDRR transfer. The FSM is holding for ICDRR read access. RSFULL is clear when Reading the ICDRR. RSFULL is set to"1" when the I2C has recognized an overrun. The contents of ICDRR are NOT lost in this case. In repeat mode since double buffer [ICRSR and ICDRR] behaves like a single buffer RSFULL is set to"1" every time the data is received. RSFULL is clear as a result of Reading the ICDRR. - [RW]
10	XSMT	R/W	0h	Transmit shift empty not. This bit indicates whether the transmitter has experienced underflow. Underflow occurs when the transmit shift register [ICXSR] is empty and ICDXR has not been loaded. The FSM is holding for ICDXR write access. XSMT_ is cleared when underflow has occurred. XSMT_ is set to"1" as a result of Writing to ICDXR. In repeat mode if the I2C in master transmitter mode is holding transfer with XSMT_=0 [i.e. waiting for further action] and the STT or STP bit is set XSMT_ is set to"1" by hardware.
9	AAS	R/W	0h	Address As Target. This bit is set to 1 by the device when it has recognized its own target address or an address of all [8] zeros. The AAS bit is reset by stop condition or detection of any address byte that does not match ICOAR. - [RW]
8	AD0	R/W	0h	Address Zero Status: This bit is set to 1 by device if it detects the address of all [8] zeros [i.e. general call]. The AD0 bit is reset to 0 [default value] when a"start" or"stop" condition is detected. - [RW]
7:6	NU1	NU1	0h	Reserved
5	SCD	R/W	0h	Stop Condition Detection bit SCD is set when the I2C sends or receives STOP condition. This bit is cleared by Reading ICIVR [as 110] or Writing '1' to itself.
4	ICXRDY	R/W	0h	Transmit Data Ready interrupt flag bit. ICXRDY is set to"1" is generated when the transmitted data has been copied from ICDXR to the transmit-shift register [ICXSR]. ICRXDY is clear to"0" when the ICDXR is written. This bit can also be polled by the CPU to write a new transmitted data into the ICDXR. Write '1' to this bit will set it and DXR Write will clear it.
3	ICRRDY	R/W	0h	Receive Data Ready interrupt flag bit. ICRRDY is set to"1" when the received data has been copied from ICRSR into the ICDRR. ICRRDY is cleared to"0" when the ICDRR is read. This bit can also be polled by the CPU to read the received data in the ICDRR. Write '1' or DRR Read will clear it.
2	ARDY	R/W	0h	Register-access-ready interrupt flag bit. ARDY is generated by the hardware if the I2C is in the master mode when the previously programmed data and command has been performed and status bit has been updated. This flag is used by the CPU to let it knows that the I2C registers are ready to be accessed again. When RM=0 ARDY is set when the internal data count is passed 0 if STP register bit has not been set. When RM=1 ARDY is set at each byte end. If the I2C is in FDF mode[FDF=1] ARDY is set just after Start condition. This bit is automatically cleared by hardware when Writing data to ICDXR in transmit mode Reading data from ICDRR in receive mode or setting STT or STP bit. Write '1' will clear it.
1	NACK	R/W	0h	No-Acknowledgement interrupt flag bit. The No Acknowledge flag bit is set when the hardware in "master" mode detects no acknowledge has been received. This bit is NOT set by no-acknowledgement after Start byte Write '1' or Read the ICIVR [as 010] will clear it.
0	AL	R/W	0h	Arbitration-Lost interrupt flag bit. The Arbitration Lost flag bit is set to 1 when the device in the "master" mode senses it has lost an arbitration when two or more transmitters start a transmission almost simultaneously or when the I2C attempts to start a transfer while BB [bus busy] is 1. When this is set to 1 due to arbitration lost the MST/STT/STP bits are clear the I2C becomes a target. Write '1' or Read the ICIVR [as 001] will clear it.

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5.10.2.4 I2C_ICCLKL Register

5.10.2.4.1 I2C_ICCLKL Register (Offset = Ch) [reset = 0h]

I2C Clock Divider Low register

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Table 5-1620. Instance Table

Instance Name	Physical Address
I2C0	5250 000Ch
I2C1	5250 100Ch
I2C2	5250 200Ch
I2C3	5250 300Ch

Figure 5-793. I2C_ICCLKL Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
ICCL15_ICCL0							
R/W							
0h							
7	6	5	4	3	2	1	0
ICCL15_ICCL0							
R/W							
0h							

Table 5-1621. I2C_ICCLKL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU	R/W	0h	Reserved
15:0	ICCL15_ICCL0	R/W	0h	Low time I 2 C SCL Clock Division Factor. They are used to divide down the master clock to create the SCL low time transition frequency. This register must be configured while the I2C is still in reset [IRS_=0].

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5.10.2.5 I2C_ICCLKH Register

5.10.2.5.1 I2C_ICCLKH Register (Offset = 10h) [reset = 0h]

I2C Clock Divider High register

Return to Summary Table

Table 5-1622. Instance Table

Instance Name	Physical Address
I2C0	5250 0010h
I2C1	5250 1010h
I2C2	5250 2010h
I2C3	5250 3010h

Figure 5-794. I2C_ICCLKH Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
ICCH15_ICCLH0							
R/W							
0h							
7	6	5	4	3	2	1	0
ICCH15_ICCLH0							
R/W							
0h							

Table 5-1623. I2C_ICCLKH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU	R/W	0h	Reserved
15:0	ICCH15_ICCLH0	R/W	0h	High time I 2 C SCL Clock Division Factor. They are used to divide down the master clock to create the SCL high time transition frequency. This register must be configured while the I2C is still in reset [IRS_=0].

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5.10.2.6 I2C_ICCNT Register

5.10.2.6.1 I2C_ICCNT Register (Offset = 14h) [reset = 0h]

I2C Data Count register

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Table 5-1624. Instance Table

Instance Name	Physical Address
I2C0	5250 0014h
I2C1	5250 1014h
I2C2	5250 2014h
I2C3	5250 3014h

Figure 5-795. I2C_ICCNT Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
ICDC15_ICDC0							
R/W							
0h							
7	6	5	4	3	2	1	0
ICDC15_ICDC0							
R/W							
0h							

Table 5-1625. I2C_ICCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU	R/W	0h	Reserved
15:0	ICDC15_ICDC0	R/W	0h	Data count. This data count register is used to generate a Stop condition if a Stop condition is specified [STP=1]. . ICCNT=1 data count is 1 ::: ::: ICCNT=0FFFFh data count is 65535 ICCNT=0data counter is 65536 Note that ICCNT is a don"t care when RM is set to 1.

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5.10.2.7 I2C_ICDRR Register

5.10.2.7.1 I2C_ICDRR Register (Offset = 18h) [reset = 0h]

I2C Data Receive register

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Table 5-1626. Instance Table

Instance Name	Physical Address
I2C0	5250 0018h
I2C1	5250 1018h
I2C2	5250 2018h
I2C3	5250 3018h

Figure 5-796. I2C_ICDRR Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
D7_D0							
R/W							
0h							

Table 5-1627. I2C_ICDRR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	NU	R/W	0h	Reserved
7:0	D7_D0	R/W	0h	Receive data

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5.10.2.8 I2C_ICSAR Register

5.10.2.8.1 I2C_ICSAR Register (Offset = 1Ch) [reset = 0h]

I2C Slave Address register

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Table 5-1628. Instance Table

Instance Name	Physical Address
I2C0	5250 001Ch
I2C1	5250 101Ch
I2C2	5250 201Ch
I2C3	5250 301Ch

Figure 5-797. I2C_ICSAR Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU						A9_A0	
R/W						R/W	
0h						0h	
7	6	5	4	3	2	1	0
A9_A0							
R/W							
0h							

Table 5-1629. I2C_ICSAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	NU	R/W	0h	Reserved
9:0	A9_A0	R/W	0h	Target address. Use in both 7- and 10-bit address mode.

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5.10.2.9 I2C_ICDXR Register

5.10.2.9.1 I2C_ICDXR Register (Offset = 20h) [reset = 0h]

I2C Data Transmit register

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Table 5-1630. Instance Table

Instance Name	Physical Address
I2C0	5250 0020h
I2C1	5250 1020h
I2C2	5250 2020h
I2C3	5250 3020h

Figure 5-798. I2C_ICDXR Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
D7_D0							
R/W							
0h							

Table 5-1631. I2C_ICDXR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	NU	R/W	0h	Reserved
7:0	D7_D0	R/W	0h	Transmit data

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5.10.2.10 I2C_ICMDR Register

5.10.2.10.1 I2C_ICMDR Register (Offset = 24h) [reset = 0h]

I2C Mode register

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Table 5-1632. Instance Table

Instance Name	Physical Address
I2C0	5250 0024h
I2C1	5250 1024h
I2C2	5250 2024h
I2C3	5250 3024h

Figure 5-799. I2C_ICMDR Name Register

31	30	29	28	27	26	25	24
NU2							
NU2							
0h							
23	22	21	20	19	18	17	16
NU2							
NU2							
0h							
15	14	13	12	11	10	9	8
NACKMOD	FREE	STT	NU1	STP	MST	TRX	XA
R/W	R/W	R/W	NU1	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RM	DLB	IRS	STB	FDF	BC2_BC1_BC0		
R/W	R/W	R/W	R/W	R/W	R/W		
0h	0h	0h	0h	0h	0h		

Table 5-1633. I2C_ICMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU2	NU2	0h	Reserved
15	NACKMOD	R/W	0h	No Acknowledge [NACK] mode. This bit is used to send an Acknowledge [ACK] or a No Acknowledge [NACK] to the transmitter. This bit is only applicable when the I2C is in receiver mode. In master receiver mode when the internal data count counter decrements to zero the I2C sends a NACK. The master receiver I2C finishes a transfer when it sends a NACK. The I2C ignores ICCNT when NACKMOD is '1'. The NACKMOD bit should be set before the rising edge of the last data bit [bit 8] if a NACK must be sent and this bit is cleared once a NACK has been sent. NACKMOD=0 the I2C sends an ACK to the transmitter during the acknowledge cycle. NACKMOD=1 the I2C sends a NACK to the transmitter during the acknowledge cycle.
14	FREE	R/W	0h	Free Running. This bit is used to determine the state of the I2C when a breakpoint is encountered in the HLL debugger. FREE 0:[default] Stops immediately if SCL is low and keep driving SCL low whether I2C is master transmitter/receiver. If SCL is high I2C waits until SCL becomes low and then stops. If the I2C is a target it will stop when the transmission/receiving completes. FREE 1:The I2C runs free.

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Table 5-1633. I2C_ICMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	STT	R/W	0h	Start Condition [Master only mode]. This bit can be set to a"1" by the CPU to generate a Start condition. In master mode when setting Start to"1" generates a Start condition. It is reset to "0" by the hardware after the Start condition has been generated. The Start/Stop bits can be configured to generate different transfer formats. Note that the STT and STP can be used to terminate the repeat mode. ____ STT___STP____Conditions_______________Bus Activities _1_____0________Start___________________S-A-D _0_____1________Stop____________________P _1_____1________Start-Stop [ICCNT= n]______S-A-D..[n]..D-P _1_____0________Start [ICCNT= n]__________S-A-D..[n]..D ____
12	NU1	NU1	0h	Reserved for IDLEEN [IDLE Enable on 5509. - [RW]
11	STP	R/W	0h	Stop Condition [Master mode only]. This bit can be set to a"1" by the CPU to generate a Stop condition. It is reset to "0" by the hardware after the Stop condition has been generated. The Stop condition is generated when ICCNT passes 0 when the I2C is in non-repeat mode[RM=0].
10	MST	R/W	0h	Master. MST 0:The I 2 C peripheral is in the"target" mode and clock is received from the"master" device. MST 1:The I 2 C peripheral is in the"master" mode and it generates the clock. This bit is clear when the transfer completed.
9	TRX	R/W	0h	Transmitter. TRX 0:The I 2 C is in the"receiver" mode and data on data line SDA is shifted into the data register ICDRR. TRX 1:The I 2 C is in the"transmitter" mode and the data in ICDXR is shifted out on data line SDA. The operating modes [not in FDF mode] are defined as follows. In FDF mode TRX must be configured even if the I2C is in target mode because there is no address/direction byte in FDF mode. __________________________ MST___TRX___Operating Modes _0______x_____"target receiver" _0______x_____"target transmitter" _1______0_____"master receiver" _1______1_____"master transmitter" __________________________
8	XA	R/W	0h	Expanded Address. XA 0:[default] 7-bit address mode [normal address mode]. XA 1:10-bit address mode [expanded address mode] Please note that XA needs to be configured even if the I2C is in target mode.
7	RM	R/W	0h	Repeat Mode. This bit is set to a"1" by the CPU to put the I2C in the repeat mode. In this mode data is continuously transmitted out of the ICDXR until the STP bit is set to"1" regardless of ICCNT value. This bit is don"t care if the I2C is configured in target mode. ____ __ RM___STT___STP___Conditions_____Bus Activities_______Mode _0_____0_____0_______Idle___________None___________NA _0_____0_____1_______Stop____________P____________NA _0_____1_____0_____[Re]Start_______S-A-D..[n]..D____Repeat n _0_____1_____1_____[Re]Start-Stop___S-A-D..[n]..D-P__Repeat n _1_____0_____0_______Idle___________none___________NA _1_____0_____1_______Stop____________P ___________NA _1_____1_____0_____[Re]Start_______S-A-D-D- D.._____Continuous _1_____1_____1_____Reserved________None___________NA ____ __

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Table 5-1633. I2C_ICMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	DLB	R/W	0h	Digital Loop Back [in master transmit mode only]. This bit is set to a"1" by the CPU to put the I2C in the loop back mode. In this mode data transmitted out of the ICDXR will be received in the ICDRR after [[CPU freq/I2C freq]8] CPU cycles via an internal path. The address of the ICOAR is output on SDA.
5	IRS	R/W	0h	I2C Reset Not. This can be set to a"0" by the CPU to put the I2C in reset or to a"1" to take the I2C out of reset. When this bit is reset to 0 all status bits in ICSTR and ICIVR are set to default values. Note that if this bit is reset during a transfer it can cause the I2C bus hang [SDA and SCL are tri-stated].
4	STB	R/W	0h	Start Byte [Master only mode]. The Start Byte mode bit is set to 1 by the CPU to configure the I2C in Start byte mode the I2C sends "00000001" regardless ICSAR value. Refer to the Philip I2C spec for more details.
3	FDF	R/W	0h	Free Data Format. This bit can be set to"1" by the CPU to configure the I2C in Free Data Format mode. ____ FDF___MST___TRX______Operating mode _0______0_____ x____Target in non FDF mode _0______1_____0____Master receive in non FDF mode _0______1_____1____Master transmit in non FDF mode _1______0_____0____Target receiver in FDF mode _1______0_____1____Target transmitter in FDF mode _1______1_____0____Master receiver in FDF mode _1______1_____1____Master transmitter in FDF mode ____
2:0	BC2_BC1_BC0	R/W	0h	Bit Count : Bit Count 2, Bit Count 1 and Bit Count 0 define the number of bits starting from the lsb [excluding the acknowledge bit] of the next byte which are yet to be received or transmitted. ______________________________________ BC2_BC1_BC0__Bits/byte in FDF__Bits/byte w/ ACK _0___0___1_____NA [reserved]____ NA [reserved] _0___1___0________2______________3_______ _0___1___1________3______________4_______ _1___0___0________4______________5_______ _1___0___1________5______________6_______ _1___1___0________6______________7_______ _1___1___1________7______________8_______ _0___0___0________8______________9_______ ______________________________________

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5.10.2.11 I2C_ICIVR Register

5.10.2.11.1 I2C_ICIVR Register (Offset = 28h) [reset = 0h]

I2C Interrupt Vector register

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Table 5-1634. Instance Table

Instance Name	Physical Address
I2C0	5250 0028h
I2C1	5250 1028h
I2C2	5250 2028h
I2C3	5250 3028h

Figure 5-800. I2C_ICIVR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">NU2</td></tr>
<tr><td colspan="8">NU2</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">NU2</td></tr>
<tr><td colspan="8">NU2</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">NU2</td><td colspan="4">TESTMD</td></tr>
<tr><td colspan="4">NU2</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="5">NU1</td><td colspan="3">INTCODE</td></tr>
<tr><td colspan="5">NU1</td><td colspan="3">R/W</td></tr>
<tr><td colspan="5">0h</td><td colspan="3">0h</td></tr>
</table>

Table 5-1635. I2C_ICIVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	NU2	NU2	0h	Reserved.
11:8	TESTMD	R/W	0h	Reserved for internal testing.
7:3	NU1	NU1	0h	Reserved.

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Table 5-1635. I2C_ICIVR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	INTCODE	R/W	0h	Interrupt code. The binary-coded-interrupt vector indicates which interrupt has occurred. Reading the ICIVR clears the interrupt code except ARDY[011] RRDY[100] and XRDY[101]. Interrupt code for ARDY RRDY and XRDY is cleared when ARDY ICRRDY and ICXRDY bits in the ICSTR is cleared to default value respectively. If other interrupts are pending a new interrupt is generated. If there are more than one interrupt flag Reading the ICIVR clears the highest priority interrupt code. Reading the ICIVR also clears corresponding status bit in the ICSTR except ARDY ICRRDY ICXRDY and AAS. Note that users must read [clear] the ICIVR before doing another start otherwise the ICIVR could contain incorrect [old interrupt flags] value. ____ Interrupt Code____________Interrupt Occurred__________ _000_[default]_________________None _001_[highest priority]____Arbitration Lost interrupt _010__________________No Acknowledgement interrupt _011__________________Register Access Ready interrupt _100__________________Receive Data Ready interrupt _101__________________Transmit Data Ready interrupt _110__________________Stop Condition Detection _111_[lowest priority]_____Address As Target - [RW] ____

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5.10.2.12 I2C_ICEMDR Register

5.10.2.12.1 I2C_ICEMDR Register (Offset = 2Ch) [reset = 0h]

I2C Extended Mode register

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Table 5-1636. Instance Table

Instance Name	Physical Address
I2C0	5250 002Ch
I2C1	5250 102Ch
I2C2	5250 202Ch
I2C3	5250 302Ch

Figure 5-801. I2C_ICEMDR Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
NU						IGNACK	BCM
R/W						R/W	R/W
0h						0h	0h

Table 5-1637. I2C_ICEMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU	R/W	0h	Reserved. - [RW]
1	IGNACK	R/W	0h	Ignore NACK mode IGNACK=0 The master transmitter will operate normally discontinue the data transfer and set the ARDY and NACK status bits when a NACK signal is received from the target. IGNACK=1 The master transmitter will ignore a NACK received from the target.
0	BCM	R/W	0h	Backward Compatibility Mode. This bit affects the I2C interrupt behavior. Refer to appendix A for details.

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5.10.2.13 I2C_ICPSC Register

5.10.2.13.1 I2C_ICPSC Register (Offset = 30h) [reset = 0h]

I2C Prescaler register

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Table 5-1638. Instance Table

Instance Name	Physical Address
I2C0	5250 0030h
I2C1	5250 1030h
I2C2	5250 2030h
I2C3	5250 3030h

Figure 5-802. I2C_ICPSC Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
NU							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NU							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IPSC7_IPSC0							
R/W							
0h							

Table 5-1639. I2C_ICPSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	NU	R/W	0h	Reserved.
7:0	IPSC7_IPSC0	R/W	0h	8-bit prescaler to divide the system clock down to 4/8/12Mhz clock and used by the I2C module. This register must be initialized while the I2C is still in reset [IRS_=0]. The value takes effect on the rising edge of IRS_.

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5.10.2.14 I2C_ICPID1 Register

5.10.2.14.1 I2C_ICPID1 Register (Offset = 34h) [reset = 0h]

I2C Peripheral ID register 1

Return to Summary Table

Table 5-1640. Instance Table

Instance Name	Physical Address
I2C0	5250 0034h
I2C1	5250 1034h
I2C2	5250 2034h
I2C3	5250 3034h

Figure 5-803. I2C_ICPID1 Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
CLASS							
R/W							
0h							
7	6	5	4	3	2	1	0
REVISION							
R/W							
0h							

Table 5-1641. I2C_ICPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NU	R/W	0h	Reserved.
15:8	CLASS	R/W	0h	Identifies the class of peripheral. This value should be 0x01 - [RW]
7:0	REVISION	R/W	0h	Identifies the revision level of the I2C. This value should be incremented each time the design is revised. - [RW]

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5.10.2.15 I2C_ICPID2 Register

5.10.2.15.1 I2C_ICPID2 Register (Offset = 38h) [reset = 0h]

I2C Peripheral ID register 2

Return to Summary Table

Table 5-1642. Instance Table

Instance Name	Physical Address
I2C0	5250 0038h
I2C1	5250 1038h
I2C2	5250 2038h
I2C3	5250 3038h

Figure 5-804. I2C_ICPID2 Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
TYPE							
R/W							
0h							

Table 5-1643. I2C_ICPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	NU	R/W	0h	Reserved.
7:0	TYPE	R/W	0h	Identifies the type of peripheral. This value should be 0x05 - [RW]

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5.10.2.16 I2C_ICDMAC Register

5.10.2.16.1 I2C_ICDMAC Register (Offset = 3Ch) [reset = 0h]

I2C DMA Control Register

Return to Summary Table

Table 5-1644. Instance Table

Instance Name	Physical Address
I2C0	5250 003Ch
I2C1	5250 103Ch
I2C2	5250 203Ch
I2C3	5250 303Ch

Figure 5-805. I2C_ICDMAC Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
NU						TXDMAEN	RXDMAEN
R/W						R/W	R/W
0h						0h	0h

Table 5-1645. I2C_ICDMAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU	R/W	0h	Reserved. - [RW]
1	TXDMAEN	R/W	0h	Transmit DMA enable. This bit controls the receive DMA event pin to the system. When this bit is 1 the DMA event is enabled and ICTEVT_POR pin is asserted when the DMA transfer is required. When this bit is 0 the ICTEVT_POR pin is never asserted. RXDMAEN 0:DMA transmit event is disabled. RXDMAEN 1:DMA transmit event is enabled. [Default]
0	RXDMAEN	R/W	0h	Receive DMA enable. This bit controls the receive DMA event pin to the system. When this bit is 1 the DMA event is enabled and ICREVT_POR pin is asserted when the DMA transfer is required. When this bit is 0 the ICREVT_POR pin is never asserted. RXDMAEN 0:DMA receive event is disabled. RXDMAEN 1:DMA receive event is enabled. [Default]

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5.10.2.17 I2C_ICPFUNC Register

5.10.2.17.1 I2C_ICPFUNC Register (Offset = 48h) [reset = 0h]

I2C Pin Function register

Return to Summary Table

Table 5-1646. Instance Table

Instance Name	Physical Address
I2C0	5250 0048h
I2C1	5250 1048h
I2C2	5250 2048h
I2C3	5250 3048h

Figure 5-806. I2C_ICPFUNC Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
NU							PFUNC0
R/W							R/W
0h							0h

Table 5-1647. I2C_ICPFUNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	NU	R/W	0h	Reserved.
0	PFUNC0	R/W	0h	Controls the function of the I2C SCL and SDA pins. 0 = Pins function as SCL and SDA 1 = Pins functions as GPIO Note: No hardware protection is required to disable I2C function when the PFUNC[0] and IRS_ bits are both set to one. When PFUNC[0] is"1" [GPIO mode] the sub-module which controls the I2C function receives the value"1" for SCL and SDA. IRS_ can be set to"1" regardless of PFUNC[0] and the I2C function works whenever the IRS_ bit is"1". The user is expected to hold I2C in reset via IRS_ bit when changing to/from GPIO mode via the PFUNC[0] bit.

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5.10.2.18 I2C_ICPDIR Register

5.10.2.18.1 I2C_ICPDIR Register (Offset = 4Ch) [reset = 0h]

I2C Pin Direction register

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Table 5-1648. Instance Table

Instance Name	Physical Address
I2C0	5250 004Ch
I2C1	5250 104Ch
I2C2	5250 204Ch
I2C3	5250 304Ch

Figure 5-807. I2C_ICPDIR Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">NU</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">NU</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">NU</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">NU</td><td>PDIR1</td><td>PDIR0</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-1649. I2C_ICPDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU	R/W	0h	Reserved
1	PDIR1	R/W	0h	Controls the direction of the I2C SDA pin when configured as GPIO. 0 = SDA pin functions as input 1 = SDA pin functions as output
0	PDIR0	R/W	0h	Controls the direction of the I2C SCL pin when configured as GPIO. 0 = SCL pin functions as input 1 = SCL pin functions as output

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5.10.2.19 I2C_ICPDIN Register

5.10.2.19.1 I2C_ICPDIN Register (Offset = 50h) [reset = 0h]

I2C Pin Data In register

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Table 5-1650. Instance Table

Instance Name	Physical Address
I2C0	5250 0050h
I2C1	5250 1050h
I2C2	5250 2050h
I2C3	5250 3050h

Figure 5-808. I2C_ICPDIN Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
NU						PDIN1	PDIN0
R/W						R/W	R/W
0h						0h	0h

Table 5-1651. I2C_ICPDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU	R/W	0h	Reserved
1	PDIN1	R/W	0h	Indicates the logic level present on the SDA pin. Reads: 0 = Logic low present at SDA pin regardless of PFUNC setting. 1 = Logic high present at SDA pin regardless of PFUNC setting. Writes: Writes have no effect. - [RW]
0	PDIN0	R/W	0h	Indicates the logic level present on the SCL pin. Reads: 0 = Logic low present at SCL pin regardless of PFUNC setting. 1 = Logic high present at SCL pin regardless of PFUNC setting. Writes: Writes have no effect - [RW]

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5.10.2.20 I2C_ICPDOUT Register

5.10.2.20.1 I2C_ICPDOUT Register (Offset = 54h) [reset = 0h]

I2C Pin Data Out register

Return to Summary Table

Table 5-1652. Instance Table

Instance Name	Physical Address
I2C0	5250 0054h
I2C1	5250 1054h
I2C2	5250 2054h
I2C3	5250 3054h

Figure 5-809. I2C_ICPDOUT Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
NU						PDOUT1	PDOUT0
R/W						R/W	R/W
0h						0h	0h

Table 5-1653. I2C_ICPDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU	R/W	0h	Reserved
1	PDOUT1	R/W	0h	Controls the level driven on the SDA pin when configured as GPIO output. Reads: Reads return register values not GPIO pin levels. Writes: 0 = SDA pin driven low 1 = SDA pin driven high. Note: If SDA is connected to an open-drain buffer at the chiplevel the I2C cannot drive SDA to high.
0	PDOUT0	R/W	0h	Controls the level driven on the SCL pin when configured as GPIO output. Reads: Reads return register values not GPIO pin levels. Writes: 0 = SCL pin driven low 1 = SCL pin driven high Note: If SCL is connected to an open-drain buffer at the chiplevel the I2C cannot drive SCL to high.

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5.10.2.21 I2C_ICPDSET Register

5.10.2.21.1 I2C_ICPDSET Register (Offset = 58h) [reset = 0h]

I2C Pin Data Set register

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Table 5-1654. Instance Table

Instance Name	Physical Address
I2C0	5250 0058h
I2C1	5250 1058h
I2C2	5250 2058h
I2C3	5250 3058h

Figure 5-810. I2C_ICPDSET Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
NU						PDSET1	PDSET0
R/W						R/W	R/W
0h						0h	0h

Table 5-1655. I2C_ICPDSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU	R/W	0h	Reserved
1	PDSET1	R/W	0h	Used to set PDOUT[1] bit which corresponds to the SDA GPIO pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[1] bit is set to logic high.
0	PDSET0	R/W	0h	Used to set PDOUT[0] bit which corresponds to the SCL GPIO pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[0] bit is set to logic high.

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5.10.2.22 I2C_ICPDCLR Register

5.10.2.22.1 I2C_ICPDCLR Register (Offset = 5Ch) [reset = 0h]

I2C Pin Data Clear register

Return to Summary Table

Table 5-1656. Instance Table

Instance Name	Physical Address
I2C0	5250 005Ch
I2C1	5250 105Ch
I2C2	5250 205Ch
I2C3	5250 305Ch

Figure 5-811. I2C_ICPDCLR Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
NU						PDCLR1	PDCLR0
R/W						R/W	R/W
0h						0h	0h

Table 5-1657. I2C_ICPDCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU	R/W	0h	Reserved
1	PDCLR1	R/W	0h	Used to clear PDOUT[1] bit which corresponds to the SDA pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[1] bit is cleared to logic low.
0	PDCLR0	R/W	0h	Used to clear PDOUT[0] bit which corresponds to the SCL pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[0] bit is cleared to logic low.

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5.10.2.23 I2C_ICPDRV Register

5.10.2.23.1 I2C_ICPDRV Register (Offset = 60h) [reset = 0h]

I2C Pin Driver Mode Register

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Table 5-1658. Instance Table

Instance Name	Physical Address
I2C0	5250 0060h
I2C1	5250 1060h
I2C2	5250 2060h
I2C3	5250 3060h

Figure 5-812. I2C_ICPDRV Name Register

31	30	29	28	27	26	25	24
NU							
R/W							
0h							
23	22	21	20	19	18	17	16
NU							
R/W							
0h							
15	14	13	12	11	10	9	8
NU							
R/W							
0h							
7	6	5	4	3	2	1	0
NU						PDRV1	PDRV0
R/W						R/W	R/W
0h						0h	0h

Table 5-1659. I2C_ICPDRV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	NU	R/W	0h	Reserved
1	PDRV1	R/W	0h	Used to select driver mode of output buffer for SDA pin. 0 = I2C mode. 1 = GPIO mode. Note: Value of this register is reflected on the PDRV_SDA_POR port. Actual function depends on I/O buffer and chip implementation.
0	PDRV0	R/W	0h	Used to select driver mode of output buffer for SCL pin. 0 = I2C mode. 1 = GPIO mode. Note: Value of this register is reflected on the PDRV_SCL_POR port. Actual function depends on I/O buffer and chip implementation.

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5.11 LIN

LIN

5.11.1 LIN Summaries

LIN Summaries

Table 5-1660. LIN Registers, Base Address=5240 0000h, Length=256

Offset	Length	Register Name	LIN0 Physical Address	LIN1 Physical Address	LIN2 Physical Address
0h	32	LIN_SCIGCR0	5240 0000h	5240 1000h	5240 2000h
4h	32	LIN_SCIGCR1	5240 0004h	5240 1004h	5240 2004h
8h	32	LIN_SCIGCR2	5240 0008h	5240 1008h	5240 2008h
Ch	32	LIN_SCISETINT	5240 000Ch	5240 100Ch	5240 200Ch
10h	32	LIN_SCICLEARINT	5240 0010h	5240 1010h	5240 2010h
14h	32	LIN_SCISETINTLVL	5240 0014h	5240 1014h	5240 2014h
18h	32	LIN_SCICLEARINTLVL	5240 0018h	5240 1018h	5240 2018h
1Ch	32	LIN_SCIFLR	5240 001Ch	5240 101Ch	5240 201Ch
20h	32	LIN_SCIINTVECT0	5240 0020h	5240 1020h	5240 2020h
24h	32	LIN_SCIINTVECT1	5240 0024h	5240 1024h	5240 2024h
28h	32	LIN_SCIFORMAT	5240 0028h	5240 1028h	5240 2028h
2Ch	32	LIN_BRSR	5240 002Ch	5240 102Ch	5240 202Ch
30h	32	LIN_SCIED	5240 0030h	5240 1030h	5240 2030h
34h	32	LIN_SCIRD	5240 0034h	5240 1034h	5240 2034h
38h	32	LIN_SCITD	5240 0038h	5240 1038h	5240 2038h
3Ch	32	LIN_SCIPIO0	5240 003Ch	5240 103Ch	5240 203Ch
40h	32	LIN_SCIPIO1	5240 0040h	5240 1040h	5240 2040h
44h	32	LIN_SCIPIO2	5240 0044h	5240 1044h	5240 2044h
48h	32	LIN_SCIPIO3	5240 0048h	5240 1048h	5240 2048h
4Ch	32	LIN_SCIPIO4	5240 004Ch	5240 104Ch	5240 204Ch
50h	32	LIN_SCIPIO5	5240 0050h	5240 1050h	5240 2050h
54h	32	LIN_SCIPIO6	5240 0054h	5240 1054h	5240 2054h
58h	32	LIN_SCIPIO7	5240 0058h	5240 1058h	5240 2058h
5Ch	32	LIN_SCIPIO8	5240 005Ch	5240 105Ch	5240 205Ch
60h	32	LIN_LINCOMP	5240 0060h	5240 1060h	5240 2060h
64h	32	LIN_LINRD0	5240 0064h	5240 1064h	5240 2064h
68h	32	LIN_LINRD1	5240 0068h	5240 1068h	5240 2068h
6Ch	32	LIN_LINMASK	5240 006Ch	5240 106Ch	5240 206Ch
70h	32	LIN_LINID	5240 0070h	5240 1070h	5240 2070h
74h	32	LIN_LINTD0	5240 0074h	5240 1074h	5240 2074h
78h	32	LIN_LINTD1	5240 0078h	5240 1078h	5240 2078h
7Ch	32	LIN_MBRSR	5240 007Ch	5240 107Ch	5240 207Ch
80h	32	LIN_RESERVED_1_J	5240 0080h + formula	5240 1080h + formula	5240 2080h + formula
90h	32	LIN_IODFTCTRL	5240 0090h	5240 1090h	5240 2090h
94h	32	LIN_RESERVED_2_J	5240 0094h + formula	5240 1094h + formula	5240 2094h + formula
E0h	32	LIN_LIN_GLB_INT_EN	5240 00E0h	5240 10E0h	5240 20E0h
E4h	32	LIN_LIN_GLB_INT_FLG	5240 00E4h	5240 10E4h	5240 20E4h
E8h	32	LIN_LIN_GLB_INT_CLR	5240 00E8h	5240 10E8h	5240 20E8h

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Table 5-1661. LIN Registers, Base Address=5240 0000h, Length=256

Offset	Length	Register Name	LIN3 Physical Address	LIN4 Physical Address
0h	32	LIN_SCIGCR0	5240 3000h	5240 4000h
4h	32	LIN_SCIGCR1	5240 3004h	5240 4004h
8h	32	LIN_SCIGCR2	5240 3008h	5240 4008h
Ch	32	LIN_SCISETINT	5240 300Ch	5240 400Ch
10h	32	LIN_SCICLEARINT	5240 3010h	5240 4010h
14h	32	LIN_SCISETINTLVL	5240 3014h	5240 4014h
18h	32	LIN_SCICLEARINTLVL	5240 3018h	5240 4018h
1Ch	32	LIN_SCIFLR	5240 301Ch	5240 401Ch
20h	32	LIN_SCIINTVECT0	5240 3020h	5240 4020h
24h	32	LIN_SCIINTVECT1	5240 3024h	5240 4024h
28h	32	LIN_SCIFORMAT	5240 3028h	5240 4028h
2Ch	32	LIN_BRSR	5240 302Ch	5240 402Ch
30h	32	LIN_SCIED	5240 3030h	5240 4030h
34h	32	LIN_SCIRD	5240 3034h	5240 4034h
38h	32	LIN_SCITD	5240 3038h	5240 4038h
3Ch	32	LIN_SCIPIO0	5240 303Ch	5240 403Ch
40h	32	LIN_SCIPIO1	5240 3040h	5240 4040h
44h	32	LIN_SCIPIO2	5240 3044h	5240 4044h
48h	32	LIN_SCIPIO3	5240 3048h	5240 4048h
4Ch	32	LIN_SCIPIO4	5240 304Ch	5240 404Ch
50h	32	LIN_SCIPIO5	5240 3050h	5240 4050h
54h	32	LIN_SCIPIO6	5240 3054h	5240 4054h
58h	32	LIN_SCIPIO7	5240 3058h	5240 4058h
5Ch	32	LIN_SCIPIO8	5240 305Ch	5240 405Ch
60h	32	LIN_LINCOMP	5240 3060h	5240 4060h
64h	32	LIN_LINRD0	5240 3064h	5240 4064h
68h	32	LIN_LINRD1	5240 3068h	5240 4068h
6Ch	32	LIN_LINMASK	5240 306Ch	5240 406Ch
70h	32	LIN_LINID	5240 3070h	5240 4070h
74h	32	LIN_LINTD0	5240 3074h	5240 4074h
78h	32	LIN_LINTD1	5240 3078h	5240 4078h
7Ch	32	LIN_MBRSR	5240 307Ch	5240 407Ch
80h	32	LIN_RESERVED_1_J	5240 3080h + formula	5240 4080h + formula
90h	32	LIN_IODFTCTRL	5240 3090h	5240 4090h
94h	32	LIN_RESERVED_2_J	5240 3094h + formula	5240 4094h + formula
E0h	32	LIN_LIN_GLB_INT_EN	5240 30E0h	5240 40E0h
E4h	32	LIN_LIN_GLB_INT_FLG	5240 30E4h	5240 40E4h
E8h	32	LIN_LIN_GLB_INT_CLR	5240 30E8h	5240 40E8h

5.11.2 LIN Registers

LIN Registers

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5.11.2.1 LIN_SCIGCR0 Register

5.11.2.1.1 LIN_SCIGCR0 Register (Offset = 0h) [reset = 0h]

The SCIGCR0 register defines the module reset.

Return to Summary Table

Table 5-1662. Instance Table

Instance Name	Physical Address
LIN0	5240 0000h
LIN1	5240 1000h
LIN2	5240 2000h
LIN3	5240 3000h
LIN4	5240 4000h

Figure 5-813. LIN_SCIGCR0 Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							RESET
R							R/W
0h							0h

Table 5-1663. LIN_SCIGCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:1	RESERVED_1	R	0h	Reserved
0	RESET	R/W	0h	This bit resets the SCI/LIN module. This bit is effective in LIN or SCI-compatible mode.. This bit affects the reset state of the SCI/LIN module. 0 `SCI/LIN module is in held in reset.` 1 `SCI/LIN module is out of reset.`

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5.11.2.2 LIN_SCIGCR1 Register

5.11.2.2.1 LIN_SCIGCR1 Register (Offset = 4h) [reset = 0h]

The SCIGCR1 register defines the frame format, protocol, and communication mode used by the SCI.

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Table 5-1664. Instance Table

Instance Name	Physical Address
LIN0	5240 0004h
LIN1	5240 1004h
LIN2	5240 2004h
LIN3	5240 3004h
LIN4	5240 4004h

Figure 5-814. LIN_SCIGCR1 Name Register

31	30	29	28	27	26	25	24
RESERVED_3						TXENA	RXENA
R						R/W	R/W
0h						0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2						CONT	LOOPBACK
R						R/W	R/W
0h						0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1		STOPEXTFRAME	HGENCTRL	CTYPE	MBUFMODE	ADAPT	SLEEP
R		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SWNRST	LINMODE	CLK_MASTER	STOP	PARITY	PARITYENA	TIMINGMODE	COMMMODE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1665. LIN_SCIGCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED_3	R	0h	Reserved
25	TXENA	R/W	0h	Transmit enable. This bit is effective in LIN and SCI modes. Data is transferred from SCITD or the TDy [with y=0, 1,...7] buffers in LIN mode to the SCITXSHF shift out register only when the TXENA bit is set. Note: Data written to SCITD or the transmit multi-buffer before TXENA is set is not transmitted. If TXENA is cleared while transmission is ongoing, the data previously written to SCITD is sent [including the checksum byte in LIN mode]. 0 `Disable transfers from SCITD or TDy to SCITXSHF` 1 `Enable transfers of data from SCITD or TDy to SCITXSHF`

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Table 5-1665. LIN_SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	RXENA	R/W	0h	Receive enable. This bit is effective in LIN or SCI-compatible mode. RXENA allows or prevents the transfer of data from SCIRXSHF to SCIRD or the receive multibuffers. Note: Clearing RXENA stops received characters from being transferred into the receive buffer or multi-buffers, prevents the RX status flags [see Table 7] from being updated by receive data, and inhibits both receive and error interrupts. However, the shift register continues to assemble data regardless of the state of RXENA. Note: If RXENA is cleared before the time the reception of a frame is complete, the data from the frame is not transferred into the receive buffer. Note: If RXENA is set before the time the reception of a frame is complete, the data from the frame is transferred into the receive buffer. If RXENA is set while SCIRXSHF is in the process of assembling a frame, the status flags are not guaranteed to be accurate for that frame. To ensure that the status flags correctly reflect what was detected on the bus during a particular frame, RXENA should be set before the detection of that frame 0 Prevents the receiver from transferring data from the shift buffer to the receive buffer or multi-buffers 1 Allows the receiver to transfer data from the shift buffer to the receive buffer or multi-buffers
23:18	RESERVED_2	R	0h	Reserved
17	CONT	R/W	0h	Continue on suspend. This bit has an effect only when a program is being debugged with an emulator, and it determines how the SCI/LIN operates when the program is suspended. This bit affects the LIN counters. When this bit is set, the counters are not stopped during debug. When this bit is cleared, the counters are stopped during debug. 0 When debug mode is entered, the SCI/LIN state machine is frozen. Transmissions and LIN counters are halted and resume when debug mode is exited. 1 When debug mode is entered, the SCI/LIN continues to operate until the current transmit and receive functions are complete.
16	LOOPBACK	R/W	0h	Loopback bit. This bit is effective in LIN or SCI-compatible mode. The self-checking option for the SCI/LIN can be selected with this bit. If the LINTX and LINRX pins are configured with SCI/LIN functionality, then the LINTX pin is internally connected to the LINRX pin. Externally, during loop back operation, the LINTX pin outputs a high value and the LINRX pin is in a high-impedance state. If this bit value is changed while the SCI/LIN is transmitting or receiving data, errors may result. 0 Loopback mode is disabled. 1 Loopback mode is enabled.
15:14	RESERVED_1	R	0h	Reserved
13	STOPEXTFRAME	R/W	0h	Stop extended frame communication. This bit is effective in LIN mode only. This bit can be written only during extended frame communication. When the extended frame communication is stopped, this bit is cleared automatically. 0 No effect 1 Extended frame communication will be stopped, once current frame transmission/reception is completed.

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Table 5-1665. LIN_SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	HGENCTRL	R/W	0h	HGEN control bit. This bit is effective in LIN mode only. This bit controls the type of mask filtering comparison. 0 ID filtering using ID-Byte. RECEIVEDID and IDBYTE fields in the LINID register are used for detecting a match (using TX/RXMASK values). Mask of 0xFF in LINMASK register will result in NO match. 1 ID filtering using ID-SlaveTask byte (Recommended). RECEIVEDID and IDSLAVETASKBYTE fields in the LINID register are used for detecting a match (using TX/RXMASK values). Mask of 0xFF in LINMASK register will result in ALWAYS match
11	CTYPE	R/W	0h	Checksum type. This bit is effective in LIN mode only. This bit controls the type of checksum to be used: classic or enhanced. 0 Classic checksum is used. This checksum is compatible with LIN 1.3 slave nodes. The classic checksum contains the modulo-256 sum with carry over all data bytes. Frames sent with Identifier 60 (0x3C) to 63 (0x3F) must allways use the classic checksum. 1 Enhanced checksum is used. The enhanced checksum is compatible with LIN 2.0 and newer slave nodes. The enhanced checksum contains the modulo-256 sum with carry over all data bytes AND the protected Identifier.
10	MBUFMODE	R/W	0h	Multibuffer mode. This bit is effective in LIN or SCI-compatible mode. This bit controls receive/transmit buffer usage, that is, whether the RX/TX multibuffers are used or a single register, RD0/TD0, is used. 0 The multi-buffer mode is disabled. 1 The multi-buffer mode is enabled.
9	ADAPT	R/W	0h	Adapt mode enable. This mode is effective in LIN mode only. This bit has an effect during the detection of the Sync Field. There are two LIN protocol bit rate modes that could be enabled with this bit according to the Node capability file definition: automatic or select. Software and network configuration will decide which of the previous two modes. When this bit is cleared, the LIN 2.0 protocol fixed bit rate should be used. If the ADAPT bit is set, a LIN target node detecting the baudrate will compare it to the prescalers in BRSR register and update it if they are different. The BRSR register will be updated with the new value. If this bit is not set there will be no adjustment to the BRSR register. This field is writable in LIN mode only. 0 Automatic baudrate adjustment is disabled. 1 Automatic baudrate adjustment is enabled.

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Table 5-1665. LIN_SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SLEEP	R/W	0h	SCI sleep. SCI compatibility mode only. In a multiprocessor configuration, this bit controls the receive sleep function. Clearing this bit brings the SCI out of sleep mode. The receiver still operates when the SLEEP bit is set; however, RXRDY is updated and SCIRD is loaded with new data only when an address frame is detected. The remaining receiver status flags are updated and an error interrupt is requested if the corresponding interrupt enable bit is set, regardless of the value of the SLEEP bit. In this way, if an error is detected on the receive data line while the SCI is asleep, software can promptly deal with the error condition. The SLEEP bit is not automatically cleared when an address byte is detected. This field is writable in SCI mode only. 0 Sleep mode is disabled. 1 Sleep mode is enabled.
7	SWNRST	R/W	0h	Software reset [active low]. This bit is effective in LIN or SCI-compatible mode. The SCI/LIN should only be configured while SWnRST = 0. Only the following configuration bits can be changed in runtime [i.e., while SWnRESET = 1]: - STOP EXT Frame [SCIGCR1[13]] - CC bit [SCIGCR2[17]] - SC bit [SCIGCR2[16]] 0 The SCI/LIN is in its reset state; no data will be transmitted or received. Writing a 0 to this bit intializes the SCI/LIN state machines and operating flags. All affected logic is held in the reset state until a 1 is written to this bit. 1 The SCI/LIN is in its ready state; transmission and reception can occur. After this bit is set to 1, the configuration of the module should not change.
6	LINMODE	R/W	0h	LIN mode This bit controls the mode of operation of the module. 0 LIN mode is disabled; SCI compatibility mode is enabled. 1 LIN mode is enabled; SCI compatibility mode is disabled.
5	CLK_MASTER	R/W	0h	SCI internal clock enable or LIN Master/Target configuration. In the SCI mode, this bit enables the clock to the SCI module. In LIN mode, this bit determines whether a LIN node is a target or master. 0 SCI-compatible mode: Reserved. LIN mode: The module is in slave mode. 1 SCI-compatible mode: Enable clock to the SCI module. LIN mode: The node is in master mode.
4	STOP	R/W	0h	SCI number of stop bits. This bit is effective in SCI-compatible mode only. Note: The receiver checks for only one stop bit. However in idle-line mode, the receiver waits until the end of the second stop bit [if STOP = 1] to begin checking for an idle period. This field is writable in SCI mode only. 0 One stop bit is used. 1 Two stop bits are used.

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Table 5-1665. LIN_SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PARITY	R/W	0h	SCI parity odd/even selection. This bit is effective in SCI-compatible mode only. If the PARITY ENA bit [SCIGCR1.2] is set, PARITY designates odd or even parity. The parity bit is calculated based on the data bits in each frame and the address bit [in address-bit mode]. The start and stop fields in the frame are not included in the parity calculation. This field is writable in SCI mode only. 0 Odd parity is used. The SCI transmits and expects to receive a value in the parity bit that makes odd the total number of bits in the frame with the value of 1. 1 Even parity is used. The SCI transmits and expects to receive a value in the parity bit that makes even the total number of bits in the frame with the value of 1.
2	PARITYENA	R/W	0h	Parity enable. Enables or disables the parity function. 0 SCI-compatible mode: Parity disabled; no parity bit is generated during transmission or is expected during reception. LIN mode: ID-parity verification is disabled. 1 SCI compatible mode: Parity enabled. A parity bit is generated during transmission and is expected during reception. LIN mode: ID-parity verification is enabled.
1	TIMINGMODE	R/W	0h	SCI timing mode bit. This bit is effective in SCI-compatible mode only. It must be set to 1 when the SCI mode is used. This bit configures the SCI for asynchronous operation. 0 Reserved. 1 Must be set to 1 when module is configured for SCI operation
0	COMMMODE	R/W	0h	SCI/LIN communication mode bit. In compatibility mode, it selects the SCI communication mode. In LIN mode it selects length control option for ID-field bits ID4 and ID5. 0 SCI-compatible mode: Idle-line mode is used. LIN mode: ID4 and ID5 are not used for length control. 1 SCI-compatible mode: Address-bit mode is used. LIN mode: ID4 and ID5 are used for length control.

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5.11.2.3 LIN_SCIGCR2 Register

5.11.2.3.1 LIN_SCIGCR2 Register (Offset = 8h) [reset = 0h]

The SCIGCR2 register is used to send or compare a checksum byte during extended frames, to generate a wakeup and for low-power mode control of the LIN module.

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Table 5-1666. Instance Table

Instance Name	Physical Address
LIN0	5240 0008h
LIN1	5240 1008h
LIN2	5240 2008h
LIN3	5240 3008h
LIN4	5240 4008h

Figure 5-815. LIN_SCIGCR2 Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_3						CC	SC
R						R/W	R/W
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED_2							GENWU
R							R/W
0h							0h
7	6	5	4	3	2	1	0
RESERVED_1							POWERDOWN
R							R/W
0h							0h

Table 5-1667. LIN_SCIGCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_3	R	0h	Reserved

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Table 5-1667. LIN_SCIGCR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CC	R/W	0h	Compare Checksum. This mode is effective in LIN mode only. This bit is used by the receiver for extended frames to trigger a checksum compare. The user will initiate this transaction by Writing a one to this bit. In non multibuffer mode, once the CC bit is set, the checksum will be compared on the byte that is currently being received, expected to be the checkbyte. During Multi-buffer mode, following are the scenarios associated with the CC bit : - If CC bit is set during the reception of the data, then the byte that is received after the reception of the programmed no. of data bytes indicated by SCIFORMAT[18:16], is treated as a checksum byte. - If CC bit is set during the IDLE period [i.e. during inter-frame space], then the next immediate byte will be treated as a checksum byte. A CE will immediatly be flagged if there is a checksum error. This bit is automatically cleared once the checksum is successfully compared. 0 No effect 1 Compare checksum on expected checkbyte
16	SC	R/W	0h	Send Checksum This mode is effective in LIN mode only. This bit is used by the transmitter with extended frames to send a checkbyte. In non multibuffer mode the checkbyte will be sent after the current byte transmission. In multibuffer mode the checkbyte will be sent after the last byte count, indicated by the SCIFORMAT[18:16]]. This field is writable in LIN mode only. 0 No checkbyte will be sent. 1 A checkbyte will be sent. This bit will automatically get cleared after the checkbyte is transmitted. The checksum will not be sent if this bit is set before transmitting the very first byte, that is, during interframe space.
15:9	RESERVED_2	R	0h	Reserved
8	GENWU	R/W	0h	Generate wakeup signal. This bit controls the generation of a wakeup signal, by transmitting the TDO buffer value. This bit is cleared on reception of a valid sync break. 0 No effect 1 Transmit TDO for wakeup. This bit will be cleared on a SWnRST (SCIGCR1.7)
7:1	RESERVED_1	R	0h	Reserved
0	POWERDOWN	R/W	0h	Power down. This bit is effective in LIN or SCI-compatible mode. When the powerdown bit is set, the SCI/LIN module attempts to enter local low-power mode. If the POWERDOWN bit is set while the receiver is actively receiving data and the wakeup interrupt is disabled, then the SCI/LIN will delay low-power mode from being entered until completion of reception. In LIN mode the user may set the POWERDOWN bit on Sleep Command reception or on idle bus detection [more than 4 seconds, i.e. 80,000 cycles at 20kHz] 0 Normal operation 1 Request local low-power mode

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5.11.2.4 LIN_SCISETINT Register

5.11.2.4.1 LIN_SCISETINT Register (Offset = Ch) [reset = 0h]

The SCISETINT register is used to enable the various interrupts available in the LIN module.

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Table 5-1668. Instance Table

Instance Name	Physical Address
LIN0	5240 000Ch
LIN1	5240 100Ch
LIN2	5240 200Ch
LIN3	5240 300Ch
LIN4	5240 400Ch

Figure 5-816. LIN_SCISETINT Name Register

31	30	29	28	27	26	25	24
SETBEINT	SETPBEINT	SETCEINT	SETISFEINT	SETNREINT	SETFEINT	SETOEINT	SETPEINT
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_5					SET_RX_DMA_ALL	SET_RX_DMA	SET_TX_DMA
R					R/W1TS	R/W1TS	R/W1TS
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_4		SETIDINT	RESERVED_3			SETRXINT	SETTXINT
R		R/W1TS	R			R/W1TS	R/W1TS
0h		0h	0h			0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETTOA3WUSINT	SETTOAWUSINT	RESERVED_2	SETTIMEOUTINT	RESERVED_1		SETWAKEUPINT	SETBRKDTINT
R/W1TS	R/W1TS	R	R/W1TS	R		R/W1TS	R/W1TS
0h	0h	0h	0h	0h		0h	0h

Table 5-1669. LIN_SCISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SETBEINT	R/W1TS	0h	Set bit error interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is a bit error. This field is writable in LIN mode only. `0` `Interrupt is disabled. Writing a 0 to this bit has no effect.` `1` `Interrupt is enabled.`
30	SETPBEINT	R/W1TS	0h	Set physical bus error interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when a physical bus error occurs. This field is writable in LIN mode only. `0` `Interrupt is disabled. Writing a 0 to this bit has no effect.` `1` `Interrupt is enabled.`

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Table 5-1669. LIN_SCISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	SETCEINT	R/W1TS	0h	Set checksum-error Interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is a checksum error. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
28	SETISFEINT	R/W1TS	0h	Set inconsistent-sync-field-error interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is an inconsistent sync field error. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
27	SETNREINT	R/W1TS	0h	Set no-response-error interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when a no-response error occurs. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
26	SETFEINT	R/W1TS	0h	Set framing-error interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when a framing error occurs. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
25	SETOEINT	R/W1TS	0h	Set overrun-error interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when an overrun error occurs. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
24	SETPEINT	R/W1TS	0h	Set parity interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when a parity error occurs. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
23:19	RESERVED_5	R	0h	Reserved
18	SET_RX_DMA_ALL	R/W1TS	0h	Set receiver DMA for Address & Data frames. This bit is effective in LIN or SCI-compatible mode. To enable RX DMA request for address and data frames this bit must be set. If it is cleared, RX interrupt request is generated for address frames and DMA requests are generated for data frames. 0 Receiver DMA request is disabled for address frames (RX interrupt request is enabled for address frames). Writing a 0 to this bit has no effect. 1 Receiver DMA request is enabled for address and data frames

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Table 5-1669. LIN_SCISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	SET_RX_DMA	R/W1TS	0h	Set receiver DMA. This bit is effective in LIN or SCI-compatible mode. To enable DMA requests for the receiver this bit must be set. If it is cleared, interrupt requests are generated depending on SETRXINT. 0 Receiver DMA request is disabled. Writing a 0 to this bit has no effect. 1 Receiver DMA request is enabled.
16	SET_TX_DMA	R/W1TS	0h	Set transmit DMA. This bit is effective in LIN or SCI-compatible mode. To enable DMA requests for the transmitter, this bit must be set. If it is cleared, interrupt requests are generated depending on SETTXINT. 0 Transmit DMA request is disabled. Writing a 0 to this bit has no effect. 1 Transmit DMA request is enabled
15:14	RESERVED_4	R	0h	Reserved
13	SETIDINT	R/W1TS	0h	Set Identification interrupt. This bit is effective in LIN mode only. This bit is set to enable interrupt once a valid matching identifier is received. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
12:10	RESERVED_3	R	0h	Reserved
9	SETRXINT	R/W1TS	0h	Set Receiver interrupt. Setting this bit enables the SCI/LIN to generate a receive interrupt after a frame has been completely received and the data is being transferred from SCIRXSHF to SCIRD. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
8	SETTXINT	R/W1TS	0h	Set Transmitter interrupt. Setting this bit enables the SCI/LIN to generate a transmit interrupt as data is being transferred from SCITD to SCITXSHF and the TXRDY bit is being set. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
7	SETTOA3WUSINT	R/W1TS	0h	Set Timeout After 3 Wakeup Signals interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when there is a timeout after 3 wakeup signals have been sent. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
6	SETTOAWUSINT	R/W1TS	0h	Set Timeout After Wakeup Signal interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when there is a timeout after one wakeup signal has been sent. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled.
5	RESERVED_2	R	0h	Reserved

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Table 5-1669. LIN_SCISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SETTIMEOUTINT	R/W1TS	0h	Set timeout interrupt. This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when no LIN bus activity [bus idle] occurs for at least 4 seconds. This field is writable in LIN mode only. 0 `Interrupt is disabled. Writing a 0 to this bit has no effect.` 1 `Interrupt is enabled.`
3:2	RESERVED_1	R	0h	Reserved
1	SETWAKEUPINT	R/W1TS	0h	Set wake-up interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN to generate a wake-up interrupt and thereby exit low-power mode. The wake-up interrupt is asserted on falling edge of the wake-up pulse. If enabled, the wake-up interrupt is asserted when local low-power mode is requested while the receiver is busy or if a low level is detected on the SCIRX pin during low-power mode. Wake-up interrupt is not asserted upon a wakeup pulse if the module is not in power down mode. 0 `Interrupt is disabled. Writing a 0 to this bit has no effect.` 1 `Interrupt is enabled.`
0	SETBRKDTINT	R/W1TS	0h	Set break-detect interrupt. This bit is effective in SCI-compatible mode only. Setting this bit enables the SCI/LIN to generate an interrupt if a break condition is detected on the LINRX pin. This field is writable in SCI mode only. 0 `Interrupt is disabled. Writing a 0 to this bit has no effect.` 1 `Interrupt is enabled.`

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5.11.2.5 LIN_SCICLEARINT Register

5.11.2.5.1 LIN_SCICLEARINT Register (Offset = 10h) [reset = 0h]

The SCICLEARINT register is used to disable the enabled interrupts without accessing the SCISETINT register.

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Table 5-1670. Instance Table

Instance Name	Physical Address
LIN0	5240 0010h
LIN1	5240 1010h
LIN2	5240 2010h
LIN3	5240 3010h
LIN4	5240 4010h

Figure 5-817. LIN_SCICLEARINT Name Register

31	30	29	28	27	26	25	24
CLRBEINT	CLRPBEINT	CLRCEINT	CLRISFEINT	CLRNREINT	CLRFEINT	CLROEINT	CLRPEINT
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_6					RESERVED_5	SETRXDMA	CLRTXDMA
R					R	R/W1TC	R/W1TC
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_4		CLRIDINT	RESERVED_3			CLRRXINT	CLRTXINT
R		R/W1TC	R			R/W1TC	R/W1TC
0h		0h	0h			0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLRTOA3WUSINT	CLRTOAWUSINT	RESERVED_2	CLRTIMEOUTINT	RESERVED_1		CLRWAKEUPINT	CLRBRKDTINT
R/W1TC	R/W1TC	R	R/W1TC	R		R/W1TC	R/W1TC
0h	0h	0h	0h	0h		0h	0h

Table 5-1671. LIN_SCICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLRBEINT	R/W1TC	0h	Clear Bit Error Interrupt. This bit is effective in LIN mode only. Setting this bit disables the bit error interrupt. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
30	CLRPBEINT	R/W1TC	0h	Clear Physical Bus Error Interrupt. This bit is effective in LIN mode only. Setting this bit disables the physical-bus error interrupt. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.

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Table 5-1671. LIN_SCICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	CLRCEINT	R/W1TC	0h	Clear checksum-error Interrupt. This bit is effective in LIN mode only. Setting this bit disables the checksum-error interrupt. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
28	CLRISFEINT	R/W1TC	0h	Clear Inconsistent-Sync-Field-Error Interrupt. This bit is effective in LIN mode only. Setting this bit disables the ISFE interrupt. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
27	CLRNREINT	R/W1TC	0h	Clear No-Reponse-Error Interrupt. This bit is effective in LIN mode only. Setting this bit disables the no-response error interrupt. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
26	CLRFEINT	R/W1TC	0h	Clear Framing-Error Interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables framing-error interrupt. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
25	CLROEINT	R/W1TC	0h	Clear Overrun-Error Interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the overrun interrupt. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
24	CLRPEINT	R/W1TC	0h	Clear Parity Interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the parity error interrupt. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
23:19	RESERVED_6	R	0h	Reserved
18	RESERVED_5	R	0h	Reserved
17	SETRXDMA	R/W1TC	0h	Clear receiver DMA. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the receive DMA request. 0 Receiver DMA request is disabled. Writing a 0 to this bit has no effect. 1 Receiver DMA request is enabled. Writing a 1 to this bit will disable the DMA request and clear this bit.

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Table 5-1671. LIN_SCICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CLRTXDMA	R/W1TC	0h	Clear transmit DMA. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the transmit DMA request. 0 Transmit DMA request is disabled. Writing a 0 to this bit has no effect. 1 Transmit DMA request is enabled. Writing a 1 to this bit will disable the DMA request and clear this bit.
15:14	RESERVED_4	R	0h	Reserved
13	CLRIDINT	R/W1TC	0h	Clear Identifier interrupt. This bit is effective in LIN mode only. Setting this bit disables the ID interrupt. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
12:10	RESERVED_3	R	0h	Reserved
9	CLRRXINT	R/W1TC	0h	Clear Receiver interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the receiver interrupt. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
8	CLRTXINT	R/W1TC	0h	Clear Transmitter interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the transmitter interrupt. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
7	CLRTOA3WUSINT	R/W1TC	0h	Clear Timeout After 3 Wakeup Signals interrupt. This bit is effective in LIN mode only. Setting this bit disables the timeout after 3 wakeup signals interrupt. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
6	CLRTOAWUSINT	R/W1TC	0h	Clear Timeout After Wakeup Signal interrupt. This bit is effective in LIN mode only. Setting this bit disables the timeout after one wakeup signal interrupt. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
5	RESERVED_2	R	0h	Reserved
4	CLRTIMEOUTINT	R/W1TC	0h	Clear Timeout interrupt. This bit is effective in LIN mode only. Setting this bit disables the timeout [LIN bus idle] interrupt. This field is writable in LIN mode only. 0 Interrupt is disabled. Writing a 0 to this bit has no effect. 1 Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.

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Table 5-1671. LIN_SCICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	RESERVED_1	R	0h	Reserved
1	CLRWAKEUPINT	R/W1TC	0h	Clear Wake-up interrupt. This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the wake-up interrupt. 0 `Interrupt is disabled. Writing a 0 to this bit has no effect.` 1 `Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.`
0	CLRBRKDTINT	R/W1TC	0h	Clear Break-detect interrupt. This bit is effective in SCI-compatible mode only. Setting this bit disables the Break-detect interrupt. This field is writable in SCI mode only. 0 `Interrupt is disabled. Writing a 0 to this bit has no effect.` 1 `Interrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.`

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5.11.2.6 LIN_SCISETINTLVL Register

5.11.2.6.1 LIN_SCISETINTLVL Register (Offset = 14h) [reset = 0h]

The SCISETINTLVL register is used to map individual interrupt sources to the INT1 interrupt line.

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Table 5-1672. Instance Table

Instance Name	Physical Address
LIN0	5240 0014h
LIN1	5240 1014h
LIN2	5240 2014h
LIN3	5240 3014h
LIN4	5240 4014h

Figure 5-818. LIN_SCISETINTLVL Name Register

31	30	29	28	27	26	25	24
SETBEINTLVL	SETPBEINTLVL	SETCEINTLVL	SETISFEINTLVL	SETNREINTLVL	SETFEINTLVL	SETOEINTLVL	SETPEINTLVL
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_7					RESERVED_6	RESERVED_5	
R					R	R	
0h					0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_4		SETIDINTLVL	RESERVED_3			SETRXINTOVO	SETTXINTLVL
R		R/W1TS	R			R/W1TS	R/W1TS
0h		0h	0h			0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETTOA3WUSINTLVL	SETTOAWUSINTLVL	RESERVED_2	SETTIMEOUTINTLVL	RESERVED_1		SETWAKEUPINTLVL	SETBRKDTINTLVL
R/W1TS	R/W1TS	R	R/W1TS	R		R/W1TS	R/W1TS
0h	0h	0h	0h	0h		0h	0h

Table 5-1673. LIN_SCISETINTLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SETBEINTLVL	R/W1TS	0h	Set Bit Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Bit Error interrupt level to the INT1 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
30	SETPBEINTLVL	R/W1TS	0h	Set Physical Bus Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Physical Bus Error interrupt level to the INT1 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
29	SETCEINTLVL	R/W1TS	0h	Set Checksum-error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Checksum-error interrupt level to the INT1 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.

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Table 5-1673. LIN_SCISETINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	SETISFEINTLVL	R/W1TS	0h	Set Inconsistent-Sync-Field-Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Inconsistent-Sync-Field-Error interrupt level to the INT1 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
27	SETNREINTLVL	R/W1TS	0h	Set No-Reponse-Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the No-Response-Error interrupt level to the INT1 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
26	SETFEINTLVL	R/W1TS	0h	Set Framing-Error interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Framing-Error interrupt level to the INT1 line. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
25	SETOEINTLVL	R/W1TS	0h	Set Overrun-Error Interrupt Level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Overrun-Error interrupt level to the INT1 line. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
24	SETPEINTLVL	R/W1TS	0h	Set Parity Error interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Parity error interrupt level to the INT1 line. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
23:19	RESERVED_7	R	0h	Reserved
18	RESERVED_6	R	0h	Reserved
17:16	RESERVED_5	R	0h	Reserved
15:14	RESERVED_4	R	0h	Reserved
13	SETIDINTLVL	R/W1TS	0h	Set ID interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the ID interrupt level to the INT1 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
12:10	RESERVED_3	R	0h	Reserved
9	SETRXINTOVO	R/W1TS	0h	Set Receiver interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the receiver interrupt level to the INT1 line. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
8	SETTXINTLVL	R/W1TS	0h	Set Transmitter interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the transmitter interrupt level to the INT1 line. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
7	SETTOA3WUSINTLVL	R/W1TS	0h	Set Timeout After 3 Wakeup Signals interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the timeout after 3 wakeup signals interrupt level to the INT1 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.

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Table 5-1673. LIN_SCISETINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SETTOAWUSINTLVL	R/W1TS	0h	Set Timeout After Wakeup Signal interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the the timeout after wakeup interrupt level to the INT1 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
5	RESERVED_2	R	0h	Reserved
4	SETTIMEOUTINTLVL	R/W1TS	0h	Set Timeout interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the timeout interrupt level to the INT1 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
3:2	RESERVED_1	R	0h	Reserved
1	SETWAKEUPINTLVL	R/W1TS	0h	Set Wake-up interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Wake-up interrupt level to the INT1 line. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.
0	SETBRKDTINTLVL	R/W1TS	0h	Set Break-detect interrupt level. This bit is effective in SCI-compatible mode only. Writing to this bit maps the Break-detect interrupt level to the INT1 line. This field is writable in SCI mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line.

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5.11.2.7 LIN_SCICLEARINTLVL Register

5.11.2.7.1 LIN_SCICLEARINTLVL Register (Offset = 18h) [reset = 0h]

The SCICLEARINTLVL register is used to map individual interrupt sources to the INT0 line.

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Table 5-1674. Instance Table

Instance Name	Physical Address
LIN0	5240 0018h
LIN1	5240 1018h
LIN2	5240 2018h
LIN3	5240 3018h
LIN4	5240 4018h

Figure 5-819. LIN_SCICLEARINTLVL Name Register

31	30	29	28	27	26	25	24
CLRBEINTLVL	CLRPBEINTLVL	CLRCEINTLVL	CLRISFEINTLVL	CLRNREINTLVL	CLRFEINTLVL	CLROEINTLVL	CLRPEINTLVL
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_7					RESERVED_6	RESERVED_5	
R					R	R	
0h					0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_4		CLRIDINTLVL	RESERVED_3			CLRRXINTLVL	CLRTXINTLVL
R		R/W1TC	R			R/W1TC	R/W1TC
0h		0h	0h			0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLRTOA3WUSINTLVL	CLRTOAWUSINTLVL	RESERVED_2	CLRTIMEOUTINTLVL	RESERVED_1		CLRWAKEUPINTLVL	CLRBRKDTINTLVL
R/W1TC	R/W1TC	R	R/W1TC	R		R/W1TC	R/W1TC
0h	0h	0h	0h	0h		0h	0h

Table 5-1675. LIN_SCICLEARINTLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLRBEINTLVL	R/W1TC	0h	Clear Bit Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Bit Error interrupt level to the INT0 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
30	CLRPBEINTLVL	R/W1TC	0h	Clear Physical Bus Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Physical Bus Error interrupt level to the INT0 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.

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Table 5-1675. LIN_SCICLEARINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	CLRCEINTLVL	R/W1TC	0h	Clear Checksum-error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Checksum-error interrupt level to the INT0 line. This field is writable in LIN mode only. 0 `Interrupt level mapped to INT0 line.` 1 `Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.`
28	CLRISFEINTLVL	R/W1TC	0h	Clear Inconsistent-Sync-Field-Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the Inconsistent-Sync-Field-Error interrupt level to the INT0 line. This field is writable in LIN mode only. 0 `Interrupt level mapped to INT0 line.` 1 `Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.`
27	CLRNREINTLVL	R/W1TC	0h	Clear No-Reponse-Error interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the No-Response-Error interrupt level to the INT0 line. This field is writable in LIN mode only. 0 `Interrupt level mapped to INT0 line.` 1 `Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.`
26	CLRFEINTLVL	R/W1TC	0h	Clear Framing-Error interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Framing-Error interrupt level to the INT0 line. 0 `Interrupt level mapped to INT0 line.` 1 `Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.`
25	CLROEINTLVL	R/W1TC	0h	Clear Overrun-Error Interrupt Level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Overrun-Error interrupt level to the INT0 line. 0 `Interrupt level mapped to INT0 line.` 1 `Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.`
24	CLRPEINTLVL	R/W1TC	0h	Clear Parity Error interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Parity Error interrupt level to the INT0 line. 0 `Interrupt level mapped to INT0 line.` 1 `Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.`
23:19	RESERVED_7	R	0h	Reserved
18	RESERVED_6	R	0h	Reserved
17:16	RESERVED_5	R	0h	Reserved
15:14	RESERVED_4	R	0h	Reserved
13	CLRIDINTLVL	R/W1TC	0h	Clear ID interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the ID interrupt level to the INT0 line. This field is writable in LIN mode only. 0 `Interrupt level mapped to INT0 line.` 1 `Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.`
12:10	RESERVED_3	R	0h	Reserved

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Table 5-1675. LIN_SCICLEARINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CLRRXINTLVL	R/W1TC	0h	Clear Receiver interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the receiver interrupt level to the INT0 line. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
8	CLRTXINTLVL	R/W1TC	0h	Clear Transmitter interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the transmitter interrupt level to the INT0 line. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
7	CLRTOA3WUSINTLVL	R/W1TC	0h	Clear Timeout After 3 Wakeup Signals interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the timeout after 3 wakeup signals interrupt level to the INT0 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
6	CLRTOAWUSINTLVL	R/W1TC	0h	Clear Timeout After Wakeup Signal interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the the timeout after wakeup interrupt level to the INT0 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
5	RESERVED_2	R	0h	Reserved
4	CLRTIMEOUTINTLVL	R/W1TC	0h	Clear Timeout interrupt level. This bit is effective in LIN mode only. Writing to this bit maps the timeout interrupt level to the INT0 line. This field is writable in LIN mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
3:2	RESERVED_1	R	0h	Reserved
1	CLRWAKEUPINTLVL	R/W1TC	0h	Clear Wake-up interrupt level. This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Wake-up interrupt level to the INT0 line. 0 Interrupt level mapped to INT0 line. Writing a 0 to this bit has no effect. 1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
0	CLRBRKDTINTLVL	R/W1TC	0h	Clear Break-detect interrupt level. This bit is effective in SCI-compatible mode only. Writing to this bit maps the Break-detect interrupt level to the INT0 line. This field is writable in SCI mode only. 0 Interrupt level mapped to INT0 line. 1 Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.

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5.11.2.8 LIN_SCIFLR Register

5.11.2.8.1 LIN_SCIFLR Register (Offset = 1Ch) [reset = 904h]

The SCIFLR register indicates the current status of the various interrupt sources of the LIN module.

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Table 5-1676. Instance Table

Instance Name	Physical Address
LIN0	5240 001Ch
LIN1	5240 101Ch
LIN2	5240 201Ch
LIN3	5240 301Ch
LIN4	5240 401Ch

Figure 5-820. LIN_SCIFLR Name Register

31	30	29	28	27	26	25	24
BE	PBE	CE	ISFE	NRE	FE	OE	PE
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2	IDRXFLAG	IDTXFLAG	RXWAKE	TXEMPTY	TXWAKE	RXRDY	TXRDY
R	R/W1TC	R/W1TC	R	R	R/W	R/W1TC	R
0h	0h	0h	0h	1h	0h	0h	1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TOA3WUS	TOAWUS	RESERVED_1	TIMEOUT	BUSY	IDLE	WAKEUP	BRKDT
R/W1TC	R/W1TC	R	R/W1TC	R	R	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	1h	0h	0h

Table 5-1677. LIN_SCIFLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BE	R/W1TC	0h	Bit Error Flag. This bit is effective in LIN mode only. This bit is set when there has been a bit error. This is detected by the bit monitor in the internal bit monitor. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new sync break This field is writable in LIN mode only. 0 No bit error detected. 1 Bit error detected.

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Table 5-1677. LIN_SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	PBE	R/W1TC	0h	Physical Bus Error Flag. This bit is effective in LIN mode only. This bit is set when there has been a physical bus error. This is detected by the bit monitor in TED. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new sync break Note: thie PBE will ony be flagged if no sync break can be generated. [because of a bus shortage to VBAT] or if no sync break delimeter can be generated [because of a bus shortage to GND]. This field is writable in LIN mode only. 0 No physiscal bus error detected. 1 Physical bus error detected.
29	CE	R/W1TC	0h	Checksum Error Flag. This bit is effective in LIN mode only. This bit is set when there is checksum error detected by a receiving node. The type of checksum to be used depends on the SCIGCR1.CTYPE bit. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new sync break This field is writable in LIN mode only. 0 No Checksum error detected. 1 Checksum error detected.
28	ISFE	R/W1TC	0h	Inconsistent Sync Field Error Flag. This bit is effective in LIN mode only. This bit is set when there has been an inconsistent Sync Field error detected by the synchronizer during header reception. See the "Header Reception and Adaptive Baudrate" section for more information. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new sync break This field is writable in LIN mode only. 0 No Inconsistent Sync Field error detected. 1 Inconsistent Sync Field error detected.
27	NRE	R/W1TC	0h	No-Response Error Flag. This bit is effective in LIN mode only. This bit is set when there is no response to a master's header completed within TFRAME_MAX. This timeout period is applied for message frames of unknown length [identifiers 0 to 61]. This error is detected by the synchronizer of the module. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new sync break This field is writable in LIN mode only. 0 No No-Response error detected. 1 No-Response error detected.

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Table 5-1677. LIN_SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	FE	R/W1TC	0h	Framing error flag. This bit is effective in LIN or SCI-compatible mode. This bit is set when an expected stop bit is not found. In SCI compatible mode, only the first stop bit is checked. The missing stop bit indicates that synchronization with the start bit has been lost and that the character is incorrectly framed. Detection of a framing error causes the SCI to generate an error interrupt if the RXERR INT ENA bit is set. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit - Reception of a new character [SCI-compatible mode], or frame [LIN mode] In multibuffer mode the frame is defined in the SCIFORMAT register. 0 No framing error detected. 1 Framing error detected.
25	OE	R/W1TC	0h	Overrun error flag. This bit is effective in LIN or SCI-compatible mode. This bit is set when the transfer of data from SCIRXSHF to SCIRD overwrites unread data already in SCIRD or the RDy buffers. Detection of an overrun error causes the LIN to generate an error interrupt if the SET OE INT bit is one. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit 0 No overrun error detected. 1 Overrun error detected.
24	PE	R/W1TC	0h	Parity error flag. This bit is effective in LIN or SCI-compatible mode. This bit is set when a parity error is detected in the received data. In SCI address-bit mode, the parity is calculated on the data and address bit fields of the received frame. In idle-line mode, only the data is used to calculate parity. An error is generated when a character is received with a mismatch between the number of 1s and its parity bit. For more information on parity checking, see the "SCI Global Control Register [SCIGCR1]" description. If the parity function is disabled [that is, SCIGCR1.2 = 0], the PE flag is disabled and read as 0. Detection of a parity error causes the LIN to generate an error interrupt if the SET PE INT bit = 1. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Reception of a new charcter [SCI-compatible mode] or frame [LIN mode] - Writing a 1 to this bit 0 No parity error or parity disabled. 1 Parity error detected.
23:16	RESERVED_3	R	0h	Reserved
15	RESERVED_2	R	0h	Reserved

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Table 5-1677. LIN_SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	IDRXFLAG	R/W1TC	0h	Identifier On Receive Flag. This bit is effective in LIN mode only. This flag is set once an identifier is received with an RX match and no ID-parity error. See the "Message Filtering and Validation" section for more details. When this flag is set it indicates that a new valid identifier has been received on an RX match. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Reading the LINID register - Writing a 1 to this bit This field is writable in LIN mode only. 0 No valid ID received. 1 Valid ID RX received in LINID[23:16] on RX match.
13	IDTXFLAG	R/W1TC	0h	Identifier On Transmit Flag. This bit is effective in LIN mode only. This flag is set once an identifier is received with a TX match and no ID-parity error. See the "Message Filtering and Validation" section for more details. When this flag is set it indicates that a new valid identifier has been received on a TX match. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - RESET bit [SCIGCR0.0] - Setting SWnRESET - System reset - Reading the LINID register - Writing a 1 to this bit This field is writable in LIN mode only. 0 No valid ID received. 1 Valid ID received in LINID[23:16] on TX match.
12	RXWAKE	R	0h	Receiver wakeup detect flag. This bit is effective in SCI-compatible mode only. The SCI sets this bit to indicate that the data currently in SCIRD is an address. This bit is cleared by: - RESET bit - Setting the SWnRESET bit [SCIGCR1.7] - System reset - Receipt of a data frame This bit is writable in SCI mode only. 0 The data in SCIRD is not an address. 1 The data in SCIRD is an address. See [1] Section 3.4.4, Sleep Mode for Multiprocessor Communication, on page 16 for more information on using the RXWAKE bit with sleep mode.

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Table 5-1677. LIN_SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TXEMPTY	R	1h	Transmitter Empty flag. The value of this flag indicates the contents of the transmitter's buffer register[s] [SCITD/TDy] and shift register [SCITXSHF]. In multibuffer mode, this flag indicates the value of the TDx registers and shift register [SCITXSHF]. In non multibuffer mode, this flag indicates the value of LINTD0 [byte] and shift register [SCITXSHF]. This bit is set by: - RESET bit [SCIGCR0.0] - Setting the SWnRESET bit [SCIGCR1.7] - System reset. Note: This bit does not cause an interrupt request. 0 Compatible mode or LIN with no multibuffer: Transmitter buffer or shift register (or both) are loaded with data. In LIN mode using multibuffer mode: Multibuffer or shift register (or all) are loaded with data. 1 Compatible mode or LIN with no multibuffer: Transmitter buffer and shift registers are both empty. In LIN mode using multibuffer mode: Multibuffer and shift registers are all empty.
10	TXWAKE	R/W	0h	SCI transmitter wakeup method select. This bit is effective in SCI-compatible mode only. The TXWAKE bit controls whether the data in SCITD should be sent as an address or data frame using multiprocessor communication format. This bit is set to 1 or 0 by software before a byte is written to SCITD and is cleared by the SCI when data is transferred from SCITD to SCITXSHF or by a system reset. TXWAKE is not cleared by the SWnRESET bit [SCIGCR1.7]. 0 Address-bit mode: Frame to be transmitted will be data (address bit = 0). Idle-line mode: Frame to be transmitted will be data. 1 Address-bit mode: Frame to be transmitted will be an address (address bit=1). Idle-line mode: Following frame to be transmitted will be an address (writing a 1 to this bit followed by writing dummy data to the SCITD will result in a idle period of 11 bit periods before the next frame is transmitted).

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Table 5-1677. LIN_SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RXRDY	R/W1TC	0h	Receiver ready flag. In SCI compatibility mode, the receiver sets this bit to indicate that the SCIRD contains new data and is ready to be read by the CPU. In LIN mode, RXRDY is set once a valid frame is received in multibuffer mode, a valid frame being a message frame received with no errors. In non multibuffer mode RXRDY is set for each received byte and will be set for the last byte of the frame if there are no errors. The SCI/LIN generates a receive interrupt when RXRDY flag bit is set if the interrupt-enable bit is set [SCISETINT.9]. RXRDY is cleared by: - RESET bit [SCIGCR0.0] - Setting the SWnRESET - System reset - Writing a 1 to this bit - Reading SCIRD in while in SCI compatibility mode - Reading last data byte RDy of the response in LIN mode Note: The RXRDY flag cannot be cleared by Reading the corresponding interrupt offset in the SCIINTVECT0/1 register. 0 No new data in SCIRD/RDy. 1 New data ready to be read from SCIRD.
8	TXRDY	R	1h	Transmitter buffer register ready flag. When set, this bit indicates that the transmit buffer[s] register [SCITD in compatibility mode and LINTD0, LINTD1 in MBUF mode] is/are ready to get another character from a CPU write. In SCI compatibility mode, Writing data to SCITD automatically clears this bit. In LIN mode, this bit is cleared once byte 0 [TD0] is written to LINTD0. This bit is set after the data of the TX buffer are shifted into the SCITXSHF register. This event can trigger a transmit DMA event if the DMA enable bit is set. This bit is set to 1 by: - RESET bit [SCIGCR0.0] - Setting the SWnRESET [SCIGCR1.7] - System reset Note: The TXRDY flag cannot be cleared by Reading the corresponding interrupt offset in the SCIINTVECT0/1 register. Note: The transmit interrupt request can be eliminated until the next series of data is written into the transmit buffers LINTD0 and LINTD1, by disaLINg the corresponding interrupt via the SCICLEARINT register or by disaLINg the transmitter via the TXENA bit [SCIGCR1.25=0]. 0 Compatible mode: SCITD is full. LIN mode: The multibuffers are full. 1 Compatible mode: SCITD is ready to receive the next character. LIN mode: The multibuffers are ready to receive the next character(s).
7	TOA3WUS	R/W1TC	0h	Timeout After 3 Wakeup Signals flag. This bit is effective in LIN mode only. This flag is set if there is no Sync Break received after 3 wakeup signals and a period of 1.5 seconds have passed. Such expiration time is used before issuing another round of wakeup signals. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit This field is writable in LIN mode only. 0 No timeout after 3 wakeup signals. 1 Timeout after 3 wakeup signals and 1.5s time.

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Table 5-1677. LIN_SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TOAWUS	R/W1TC	0h	Timeout After Wakeup Signal flag. This bit is effective in LIN mode only. This bit is set if there is no Sync Break received after a wakeup signal has been sent. A minimum of 150 ms expiration time is used before issuing another wakeup signal. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit This field is writable in LIN mode only. 0 No timeout after one wakeup signal (150 ms). 1 Timeout after one wakeup signal.
5	RESERVED_1	R	0h	Reserved
4	TIMEOUT	R/W1TC	0h	LIN Bus IDLE timeout flag. This bit is effective in LIN mode only. This bit is set if there is no LIN bus activity for at least 4 seconds. LIN bus activity being a transition from recessive to dominant. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit This field is writable in LIN mode only. 0 No bus idle detected. 1 LIN bus idle detected.
3	BUSY	R	0h	Bus BUSY flag. This bit is effective in LIN mode and SCI-compatible mode. This bit indicates whether the receiver is in the process of receiving a frame. As soon as the receiver detects the beginning of a start bit, the BUSY bit is set to 1. When the reception of a frame is complete, the BUSY bit is cleared. If SET WAKEUP INT is set and power down is requested while this bit is set, the SCI/LIN automatically prevents low-power mode from being entered and generates wakeup interrupt. The BUSY bit is controlled directly by the SCI receiver but can be cleared by: - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset. 0 Receiver is not currently receiving a frame. 1 Receiver is currently receiving a frame.
2	IDLE	R	1h	SCI receiver in idle state. This bit is effective in SCI-compatible mode only. While this bit is set, the SCI looks for an idle period to resynchronize itself with the bit stream. The receiver does not receive any data while the bit is set. The bus must be idle for 11 bit periods to clear this bit. The SCI enters this state: - After a system reset - Setting the SWnRESET bit [SCIGCR1.7] - After coming out of power down This bit is writable in SCI mode only. 0 Idle period detected, the SCI is ready to receive. 1 Idle period not detected, the SCI will not receive any data.

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Table 5-1677. LIN_SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	WAKEUP	R/W1TC	0h	Wake-up flag. This bit is effective in LIN mode only. This bit is set by the SCI/LIN when receiver or transmitter activity has taken the module out of power-down mode. An interrupt is generated if the SET WAKEUP INT bit [SCISETINT.1] is set. This bit is cleared by: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register. - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - Writing a 1 to this bit. This field is writable in LIN mode only. 0 Do not wake up from power-down mode. 1 Wake up from power-down mode.
0	BRKDT	R/W1TC	0h	SCI break-detect flag. This bit is effective in SCI-compatible mode only. This bit is set when the SCI detects a break condition on the LINRX pin. A break condition occurs when the LINRX pin remains continuously low for at least 10 bits after a missing first stop bit, that is, after a framing error. Detection of a break condition causes the SCI to generate an error interrupt if the BRKDT INT ENA bit is set. The BRKDT bit is cleared by the following: - Reading the corresponding interrupt offset in the SCIINTVECT0/1 register. - Setting the SWnRESET bit [SCIGCR1.7] - RESET bit [SCIGCR0.0] - System reset - By Writing a 1 to this bit. This bit is writable in SCI mode only. 0 No break condition detected. 1 Break condition detected.

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5.11.2.9 LIN_SCIINTVECT0 Register

5.11.2.9.1 LIN_SCIINTVECT0 Register (Offset = 20h) [reset = 0h]

The SCIINTVECT0 register indicates the offset for the INT0 interrupt line.

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Table 5-1678. Instance Table

Instance Name	Physical Address
LIN0	5240 0020h
LIN1	5240 1020h
LIN2	5240 2020h
LIN3	5240 3020h
LIN4	5240 4020h

Figure 5-821. LIN_SCIINTVECT0 Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			INTVECT0				
R			R				
0h			0h				

Table 5-1679. LIN_SCIINTVECT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:5	RESERVED_1	R	0h	Reserved
4:0	INTVECT0	R	0h	Interrupt vector offset for INT0. This register indicates the offset for interrupt line INT0. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read. Note: The flags for the receive [SCIFLR.9] and the transmit [SCIFLR.8] interrupts cannot be cleared by Reading the corresponding offset vector in this register [see detailed description in SCIFLR register].

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5.11.2.10 LIN_SCIINTVECT1 Register

5.11.2.10.1 LIN_SCIINTVECT1 Register (Offset = 24h) [reset = 0h]

The SCIINTVECT1 register indicates the offset for the INT1 interrupt line.

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Table 5-1680. Instance Table

Instance Name	Physical Address
LIN0	5240 0024h
LIN1	5240 1024h
LIN2	5240 2024h
LIN3	5240 3024h
LIN4	5240 4024h

Figure 5-822. LIN_SCIINTVECT1 Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1			INTVECT1				
R			R				
0h			0h				

Table 5-1681. LIN_SCIINTVECT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Reserved
15:5	RESERVED_1	R	0h	Reserved
4:0	INTVECT1	R	0h	Interrupt vector offset for INT1. This register indicates the offset for interrupt line INT1. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read. Note: The flags for the receive [SCIFLR.9] and the transmit [SCIFLR.8] interrupts cannot be cleared by Reading the corresponding offset vector in this register [see detailed description in SCIFLR register].

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5.11.2.11 LIN_SCIFORMAT Register

5.11.2.11.1 LIN_SCIFORMAT Register (Offset = 28h) [reset = 0h]

The SCIFORMAT register is used to set up the character and frame lengths.

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Table 5-1682. Instance Table

Instance Name	Physical Address
LIN0	5240 0028h
LIN1	5240 1028h
LIN2	5240 2028h
LIN3	5240 3028h
LIN4	5240 4028h

Figure 5-823. LIN_SCIFORMAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2					LENGTH		
R					R/W		
0h					0h		
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1					CHAR		
R					R/W		
0h					0h		

Table 5-1683. LIN_SCIFORMAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED_2	R	0h	Reserved
18:16	LENGTH	R/W	0h	Frame length control bits. In LIN mode, these bits indicate the number of bytes in the response field from 1 to 8 bytes. In buffered SCI mode, these bits indicate the number of characters. When these bits are used to indicate LIN response length [SCIGCR1[0] = 1], then when there is an ID RX match, this value should be updated with the expected length of the response. In buffered SCI mode, these bits indicate the number of characters with SCIFORMAT[2:0] bits per character. i.e. these bits indicate the transmitter/receiver format for the number of characters: 1 to 8. There can be up to eight characters with eight bits each. 0 The response field has 1 bytes/characters. 1 The response field has 2 bytes/characters. 2 The response field has 3 bytes/characters. 3 The response field has 4 bytes/characters. 4 The response field has 5 bytes/characters. 5 The response field has 6 bytes/characters. 6 The response field has 7 bytes/characters. 7 The response field has 8 bytes/characters.
15:3	RESERVED_1	R	0h	Reserved

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Table 5-1683. LIN_SCIFORMAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	CHAR	R/W	0h	Character length control bits. These bits are effective in SCI compatible mode only. These bits set the SCI character length from 1 to 8 bits. Note: In compatibility mode or buffered SCI mode, when data of fewer than eight bits in length is received, it is left justified in SCIRD/RDy and padded with trailing zeros. Data read from the SCIRD should be shifted by software to make the received data right justified. Note: Data written to the SCITD should be right justified but does not need to be padded with leading zeros. These bits are witable in SCI mode only. 0 The character is 1 bits long. 1 The character is 2 bits long. 2 The character is 3 bits long. 3 The character is 4 bits long. 4 The character is 5 bits long. 5 The character is 6 bits long. 6 The character is 7 bits long. 7 The character is 8 bits long.

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5.11.2.12 LIN_BRSR Register

5.11.2.12.1 LIN_BRSR Register (Offset = 2Ch) [reset = 0h]

The BRSR register is used to configure the baud rate of the LIN module.

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Table 5-1684. Instance Table

Instance Name	Physical Address
LIN0	5240 002Ch
LIN1	5240 102Ch
LIN2	5240 202Ch
LIN3	5240 302Ch
LIN4	5240 402Ch

Figure 5-824. LIN_BRSR Name Register

31	30	29	28	27	26	25	24
RESERVED_1	U			M			
R	R/W			R/W			
0h	0h			0h			
23	22	21	20	19	18	17	16
SCI_LIN_PSH							
R/W							
0h							
15	14	13	12	11	10	9	8
SCI_LIN_PSL							
R/W							
0h							
7	6	5	4	3	2	1	0
SCI_LIN_PSL							
R/W							
0h							

Table 5-1685. LIN_BRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_1	R	0h	Reserved
30:28	U	R/W	0h	Superfractional Divider Selection. [U] These bits are an additional fractional part for the baudrate specification. These bits allow a super fine tuning of the fractional baudrate with 7 more intermediate values for each of the M fractional divider values. See the Superfractional Divider section for more details.
27:24	M	R/W	0h	SCI/LIN 4-bit Fractional Divider Selection. [M] These bits are effective in LIN or SCI asynchronous mode. These bits are used to select a baud rate for the SCI/LIN module, and they are a fractional part for the baud rate specification. The M divider allows fine-tuning of the baud rate over the P prescaler with 15 additional intermediate values for each of the P integer values.

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Table 5-1685. LIN_BRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:16	SCI_LIN_PSH	R/W	0h	PRESCALER P [High Bits]. SCI/LIN 24-bit Integer Prescaler Selection. These bits are used to select a baudrate for the SCI/LIN module. These bits are effective in LIN mode and SCI compatible mode. The SCI/LIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudate selection.
15:0	SCI_LIN_PSL	R/W	0h	PRESCALER P [Low Bits]. SCI/LIN 24-bit Integer Prescaler Selection. These bits are used to select a baudrate for the SCI/LIN module. These bits are effective in LIN mode and SCI compatible mode. The SCI/LIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudate selection.

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5.11.2.13 LIN_SCIED Register

5.11.2.13.1 LIN_SCIED Register (Offset = 30h) [reset = 0h]

The SCIED register is a duplicate copy of SCIRD register that has no effect on the RXRDY flag for use with an emulator.

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Table 5-1686. Instance Table

Instance Name	Physical Address
LIN0	5240 0030h
LIN1	5240 1030h
LIN2	5240 2030h
LIN3	5240 3030h
LIN4	5240 4030h

Figure 5-825. LIN_SCIED Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
ED							
R							
0h							

Table 5-1687. LIN_SCIED Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_1	R	0h	Reserved
7:0	ED	R	0h	Receiver Emulation Data. This bit is effective in SCI-compatible mode only. Reading SCIED[7-0] does not clear the RXRDY flag. This register should be used only by an emulator that must continually read the data buffer without affecting the RXRDY flag.

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5.11.2.14 LIN_SCIRD Register

5.11.2.14.1 LIN_SCIRD Register (Offset = 34h) [reset = 0h]

The SCIRD register is where received data is stored and can be read from.

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Table 5-1688. Instance Table

Instance Name	Physical Address
LIN0	5240 0034h
LIN1	5240 1034h
LIN2	5240 2034h
LIN3	5240 3034h
LIN4	5240 4034h

Figure 5-826. LIN_SCIRD Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RD							
R							
0h							

Table 5-1689. LIN_SCIRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_1	R	0h	Reserved
7:0	RD	R	0h	Received Data. This bit is effective in SCI-compatible mode only. When a frame has been completely received, the data in the frame is transferred from the receiver shift register SCIRXSHF to this register. As this transfer occurs, the RXRDY flag is set and a receive interrupt is generated if RX INT ENA [SCISETINT0.9] is set. When the data is read from SCIRD, the RXRDY flag is automatically cleared. When the SCI receives data that is fewer than eight bits in length, it loads the data into this register in a left justified format padded with trailing zeros. Therefore, your software should perform a logical shift on the data by the correct number of positions to make it right justified.

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5.11.2.15 LIN_SCITD Register

5.11.2.15.1 LIN_SCITD Register (Offset = 38h) [reset = 0h]

The SCITD register is where data to be transmitted is written to by application software.

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Table 5-1690. Instance Table

Instance Name	Physical Address
LIN0	5240 0038h
LIN1	5240 1038h
LIN2	5240 2038h
LIN3	5240 3038h
LIN4	5240 4038h

Figure 5-827. LIN_SCITD Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
TD							
R/W							
0h							

Table 5-1691. LIN_SCITD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_1	R	0h	Reserved
7:0	TD	R/W	0h	Transmit data This bit is effective in SCI-compatible mode only. Data to be transmitted is written to this register. The transfer of data from this register to the transmit shift register SCITXSHF sets the TXRDY flag [SCIFLR.23], which indicates that SCITD is ready to be loaded with another byte of data. Note: If TX INT ENA [SCISETINT.8] is set, this data transfer also causes an interrupt. Note: Data written to the SCIRD register that is fewer than eight bits long must be right justified, but it does not need to be padded with leading zeros.

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5.11.2.16 LIN_SCIPIO0 Register

5.11.2.16.1 LIN_SCIPIO0 Register (Offset = 3Ch) [reset = 0h]

The SCIPIO0 register is used to enable the LINTX and LINRX pins.

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Table 5-1692. Instance Table

Instance Name	Physical Address
LIN0	5240 003Ch
LIN1	5240 103Ch
LIN2	5240 203Ch
LIN3	5240 303Ch
LIN4	5240 403Ch

Figure 5-828. LIN_SCIPIO0 Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2					TXFUNC	RXFUNC	RESERVED_1
R					R/W	R/W	R
0h					0h	0h	0h

Table 5-1693. LIN_SCIPIO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXFUNC	R/W	0h	Transmit pin function. This bit is effective in LIN or SCI mode. This bit defines the function of LINTX pin. 0 `LINTX pin is disabled.` 1 `LINTX pin is enabled.`
1	RXFUNC	R/W	0h	Receive pin function. This bit is effective in LIN or SCI mode. This bit defines the function of the LINRX pin. 0 `LINRX pin is disabled.` 1 `LINRX pin is enabled.`
0	RESERVED_1	R	0h	Reserved

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5.11.2.17 LIN_SCIPIO1 Register

5.11.2.17.1 LIN_SCIPIO1 Register (Offset = 40h) [reset = 0h]

Pin control Register 1

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Table 5-1694. Instance Table

Instance Name	Physical Address
LIN0	5240 0040h
LIN1	5240 1040h
LIN2	5240 2040h
LIN3	5240 3040h
LIN4	5240 4040h

Figure 5-829. LIN_SCIPIO1 Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2					TXDIR	RXDIR	RESERVED_1
R					R/W	R/W	R
0h					0h	0h	0h

Table 5-1695. LIN_SCIPIO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXDIR	R/W	0h	Transmit pin direction. This bit is effective in LIN or SCI mode. This bit determines the data direction on the LINTX pin if it is configured with general-purpose I/O functionality [TX FUNC = 0]. 0:general purpose input pin. 1:general-purpose output pin
1	RXDIR	R/W	0h	Receive pin direction. This bit is effective in LIN or SCI mode. This bit determines the data direction on the LINRX pin if it is configured with general-purpose I/O functionality [RX FUNC = 0]. 0:general purpose input pin. 1:general-purpose output pin
0	RESERVED_1	R	0h	Reserved

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5.11.2.18 LIN_SCIPIO2 Register

5.11.2.18.1 LIN_SCIPIO2 Register (Offset = 44h) [reset = 0h]

The SCIPIO2 register indicates the current status of the LINTX and LINRX pins.

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Table 5-1696. Instance Table

Instance Name	Physical Address
LIN0	5240 0044h
LIN1	5240 1044h
LIN2	5240 2044h
LIN3	5240 3044h
LIN4	5240 4044h

Figure 5-830. LIN_SCIPIO2 Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2					TXIN	RXIN	RESERVED_1
R					R	R	R
0h					0h	0h	0h

Table 5-1697. LIN_SCIPIO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXIN	R	0h	Transmit data in. This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the LINTX pin.
1	RXIN	R	0h	Receive data in. This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the LINRX pin.
0	RESERVED_1	R	0h	Reserved

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5.11.2.19 LIN_SCIPIO3 Register

5.11.2.19.1 LIN_SCIPIO3 Register (Offset = 48h) [reset = 0h]

Pin control Register 3

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Table 5-1698. Instance Table

Instance Name	Physical Address
LIN0	5240 0048h
LIN1	5240 1048h
LIN2	5240 2048h
LIN3	5240 3048h
LIN4	5240 4048h

Figure 5-831. LIN_SCIPIO3 Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2					TXOUT	RXOUT	RESERVED_1
R					R/W	R/W	R
0h					0h	0h	0h

Table 5-1699. LIN_SCIPIO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXOUT	R/W	0h	Transmit pin out. This bit is effective in LIN or SCI mode. This pin specifies the logic to be output on pin LINTX.
1	RXOUT	R/W	0h	Receive pin out. This bit is effective in LIN or SCI mode. This pin specifies the logic to be output on pin LINRX.
0	RESERVED_1	R	0h	Reserved

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5.11.2.20 LIN_SCIPIO4 Register

5.11.2.20.1 LIN_SCIPIO4 Register (Offset = 4Ch) [reset = 0h]

Pin control Register 4

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Table 5-1700. Instance Table

Instance Name	Physical Address
LIN0	5240 004Ch
LIN1	5240 104Ch
LIN2	5240 204Ch
LIN3	5240 304Ch
LIN4	5240 404Ch

Figure 5-832. LIN_SCIPIO4 Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2					TXSET	RXSET	RESERVED_1
R					R/W1TS	R/W1TS	R
0h					0h	0h	0h

Table 5-1701. LIN_SCIPIO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXSET	R/W1TS	0h	Transmit pin set. This bit is effective in LIN or SCI mode. This bit sets the logic to be output on pin LINTX.
1	RXSET	R/W1TS	0h	Receive pin set. This bit is effective in LIN or SCI mode. This bit sets the logic to be output on pin LINRX.
0	RESERVED_1	R	0h	Reserved

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5.11.2.21 LIN_SCIPIO5 Register

5.11.2.21.1 LIN_SCIPIO5 Register (Offset = 50h) [reset = 0h]

Pin control Register 5

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Table 5-1702. Instance Table

Instance Name	Physical Address
LIN0	5240 0050h
LIN1	5240 1050h
LIN2	5240 2050h
LIN3	5240 3050h
LIN4	5240 4050h

Figure 5-833. LIN_SCIPIO5 Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2					TXCLR	RXCLR	RESERVED_1
R					R/W1TC	R/W1TC	R
0h					0h	0h	0h

Table 5-1703. LIN_SCIPIO5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXCLR	R/W1TC	0h	Transmit pin clear. This bit is effective in LIN or SCI mode. This bit clears the logic to be output on pin LINTX.
1	RXCLR	R/W1TC	0h	Receive pin clear. This bit is effective in LIN or SCI mode. This bit clears the logic to be output on pin LINRX.
0	RESERVED_1	R	0h	Reserved

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5.11.2.22 LIN_SCIPIO6 Register

5.11.2.22.1 LIN_SCIPIO6 Register (Offset = 54h) [reset = 0h]

Pin control Register 6

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Table 5-1704. Instance Table

Instance Name	Physical Address
LIN0	5240 0054h
LIN1	5240 1054h
LIN2	5240 2054h
LIN3	5240 3054h
LIN4	5240 4054h

Figure 5-834. LIN_SCIPIO6 Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2					TXPDR	RXPDR	RESERVED_1
R					R/W	R/W	R
0h					0h	0h	0h

Table 5-1705. LIN_SCIPIO6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXPDR	R/W	0h	Transmit pin open drain enable. This bit is effective in LIN or SCI mode. This bit enables open-drain capability in the output pin LINTX.
1	RXPDR	R/W	0h	Receive pin open drain enable. This bit is effective in LIN or SCI mode. This bit enables open-drain capability in the output pin LINRX.
0	RESERVED_1	R	0h	Reserved

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5.11.2.23 LIN_SCIPIO7 Register

5.11.2.23.1 LIN_SCIPIO7 Register (Offset = 58h) [reset = 0h]

Pin control Register 7

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Table 5-1706. Instance Table

Instance Name	Physical Address
LIN0	5240 0058h
LIN1	5240 1058h
LIN2	5240 2058h
LIN3	5240 3058h
LIN4	5240 4058h

Figure 5-835. LIN_SCIPIO7 Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2					TXPD	RXPD	RESERVED_1
R					R/W	R/W	R
0h					0h	0h	0h

Table 5-1707. LIN_SCIPIO7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXPD	R/W	0h	Transmit pin pull control disable. This bit is effective in LIN or SCI mode. This bit disables pull control capability on the input pin LINTX.
1	RXPD	R/W	0h	Receive pin pull control disable. This bit is effective in LIN or SCI mode. This bit disables pull control capability on the input pin LINRX.
0	RESERVED_1	R	0h	Reserved

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5.11.2.24 LIN_SCIPIO8 Register

5.11.2.24.1 LIN_SCIPIO8 Register (Offset = 5Ch) [reset = 7h]

Pin control Register 8

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Table 5-1708. Instance Table

Instance Name	Physical Address
LIN0	5240 005Ch
LIN1	5240 105Ch
LIN2	5240 205Ch
LIN3	5240 305Ch
LIN4	5240 405Ch

Figure 5-836. LIN_SCIPIO8 Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_3							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2					TXPSL	RXPSL	RESERVED_1
R					R/W	R/W	R
0h					1h	1h	1h

Table 5-1709. LIN_SCIPIO8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:3	RESERVED_2	R	0h	Reserved
2	TXPSL	R/W	1h	TX pin pull select. This bit is effective in LIN or SCI mode. This bit selects pull type in the input pin LINTX.
1	RXPSL	R/W	1h	RX pin pull select. This bit is effective in LIN or SCI mode. This bit selects pull type in the input pin LINRX.
0	RESERVED_1	R	1h	Reserved

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5.11.2.25 LIN_LINCOMP Register

5.11.2.25.1 LIN_LINCOMP Register (Offset = 60h) [reset = 0h]

The LINCOMPARE register is used to configure the sync delimeter and sync break extension.

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Table 5-1710. Instance Table

Instance Name	Physical Address
LIN0	5240 0060h
LIN1	5240 1060h
LIN2	5240 2060h
LIN3	5240 3060h
LIN4	5240 4060h

Figure 5-837. LIN_LINCOMP Name Register

31	30	29	28	27	26	25	24
RESERVED_3							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_3							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2						SDEL	
R						R/W	
0h						0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1					SBREAK		
R					R/W		
0h					0h		

Table 5-1711. LIN_LINCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_3	R	0h	Reserved
15:10	RESERVED_2	R	0h	Reserved
9:8	SDEL	R/W	0h	2-bit Sync Delimiter compare. These bits are effective in LIN mode only. These bits are used to configure the number of Tbit for the sync delimiter in the sync field. The time delay calculation for the synchronization delimiter is: TSDEL = [SDEL + 1]Tbit These bits are writable in LIN mode only. 0 The sync delimiter has 1 Tbit. 1 The sync delimiter has 2 Tbit. 2 The sync delimiter has 3 Tbit. 3 The sync delimiter has 4 Tbit.
7:3	RESERVED_1	R	0h	Reserved

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Table 5-1711. LIN_LINCOMP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	SBREAK	R/W	0h	3-bit Sync Break extend. LIN mode only. These bits are used to configure the number of Tbits for the sync break to extend the minimum 13 Tbit in the Sync Field to a maximum of 20 Tbit. The time delay calculation for the sync break is: TSYNBRK = 13Tbit + SBREAK x Tbit These bits are writable in LIN mode only. 0 The sync break has no additional Tbit. 1 The sync break has 1 additional Tbit. 2 The sync break has 2 additional Tbit. 3 The sync break has 3 additional Tbit. 4 The sync break has 4 additional Tbit. 5 The sync break has 5 additional Tbit. 6 The sync break has 6 additional Tbit. 7 The sync break has 7 additional Tbit.

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5.11.2.26 LIN_LINRD0 Register

5.11.2.26.1 LIN_LINRD0 Register (Offset = 64h) [reset = 0h]

The LINRD0 register contains the lower 4 bytes of the received LIN frame data.

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Table 5-1712. Instance Table

Instance Name	Physical Address
LIN0	5240 0064h
LIN1	5240 1064h
LIN2	5240 2064h
LIN3	5240 3064h
LIN4	5240 4064h

Figure 5-838. LIN_LINRD0 Name Register

31	30	29	28	27	26	25	24
RD0							
R							
0h							
23	22	21	20	19	18	17	16
RD1							
R							
0h							
15	14	13	12	11	10	9	8
RD2							
R							
0h							
7	6	5	4	3	2	1	0
RD3							
R							
0h							

Table 5-1713. LIN_LINRD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RD0	R	0h	8-bit Receive Buffer 0 Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received. A read of this byte clears the RXDY byte. Note: RD<x-1> is equivalent to Data byte <x> of the LIN frame.
23:16	RD1	R	0h	8-bit Receive Buffer 1. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
15:8	RD2	R	0h	8-bit Receive Buffer 2. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
7:0	RD3	R	0h	8-bit Receive Buffer 3. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

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5.11.2.27 LIN_LINRD1 Register

5.11.2.27.1 LIN_LINRD1 Register (Offset = 68h) [reset = 0h]

The LINRD1 regsiter contains the upper 4 bytes of the received LIN frame data.

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Table 5-1714. Instance Table

Instance Name	Physical Address
LIN0	5240 0068h
LIN1	5240 1068h
LIN2	5240 2068h
LIN3	5240 3068h
LIN4	5240 4068h

Figure 5-839. LIN_LINRD1 Name Register

31	30	29	28	27	26	25	24
RD4							
R							
0h							
23	22	21	20	19	18	17	16
RD5							
R							
0h							
15	14	13	12	11	10	9	8
RD6							
R							
0h							
7	6	5	4	3	2	1	0
RD7							
R							
0h							

Table 5-1715. LIN_LINRD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RD4	R	0h	8-bit Receive Buffer 4 Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
23:16	RD5	R	0h	8-bit Receive Buffer 5. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
15:8	RD6	R	0h	8-bit Receive Buffer 6. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
7:0	RD7	R	0h	8-bit Receive Buffer 7. Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

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5.11.2.28 LIN_LINMASK Register

5.11.2.28.1 LIN_LINMASK Register (Offset = 6Ch) [reset = 0h]

The LINMASK register is used to configure the masks used for filtering incoming ID messages for receive and transmit frames.

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Table 5-1716. Instance Table

Instance Name	Physical Address
LIN0	5240 006Ch
LIN1	5240 106Ch
LIN2	5240 206Ch
LIN3	5240 306Ch
LIN4	5240 406Ch

Figure 5-840. LIN_LINMASK Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RXIDMASK							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
TXIDMASK							
R/W							
0h							

Table 5-1717. LIN_LINMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_2	R	0h	Reserved
23:16	RXIDMASK	R/W	0h	Receive ID mask. This field is effective in LIN mode only.This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID witht the RX ID mask will set the ID RX flag and trigger and ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that that bit is filtered and therefore not used in the compare. When HGENCTRL is set to 1, this field must be set to 0xFF.
15:8	RESERVED_1	R	0h	Reserved
7:0	TXIDMASK	R/W	0h	Transmit ID mask. This field is effective in LIN mode only. This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID with the TX ID Mask will set the ID TX flag and trigger an ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that bit is filtered and therefore not used for the compare. When HGENCTRL is set to 1, this field must be set to 0xFF.

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5.11.2.29 LIN_LINID Register

5.11.2.29.1 LIN_LINID Register (Offset = 70h) [reset = 0h]

The LINID register contains the identification fields for LIN communication.
NOTE: For software compatibility with future LIN modules, the HGEN CTRL bit must be set to 1, the RX ID MASK field must be set to FFh, and the TX ID MASK field must be set to FFh.

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Table 5-1718. Instance Table

Instance Name	Physical Address
LIN0	5240 0070h
LIN1	5240 1070h
LIN2	5240 2070h
LIN3	5240 3070h
LIN4	5240 4070h

Figure 5-841. LIN_LINID Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RECEIVEDID							
R							
0h							
15	14	13	12	11	10	9	8
IDSLAVETASKBYTE							
R/W							
0h							
7	6	5	4	3	2	1	0
IDBYTE							
R/W							
0h							

Table 5-1719. LIN_LINID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED_1	R	0h	Reserved
23:16	RECEIVEDID	R	0h	Received ID. This bit is effective in LIN mode only. This byte contains the current message identifier. During header reception the received ID is copied from the SCIRXSHF register to this byte if there is no ID-parity error and there has been an RX/TX match. Note: If a framing error [FE] is detected during ID reception, the received ID will also not be copied to the LINID register.
15:8	IDSLAVETASKBYTE	R/W	0h	ID Target Task byte. This field is effective in LIN mode only. This byte contains the identifier to which the received ID of an incoming header will be compared in order to decide whether a RX response, a TX response, or no action needs to be done by the LIN node. These bits are writable in LIN mode only.

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Table 5-1719. LIN_LINID Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	IDBYTE	R/W	0h	ID byte. This field is effective in LIN mode only. This byte is the LIN mode message ID. On a master node, a write to this register by the CPU initiates a header transmission. For a target task, this byte is used for message filtering when HGENCTRL [SCIGCR1.12] is '0'. These bits are writable in LIN mode only.

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5.11.2.30 LIN_LINTD0 Register

5.11.2.30.1 LIN_LINTD0 Register (Offset = 74h) [reset = 0h]

The LINTD0 register contains the lower 4 bytes of the data to be transmitted.
NOTE: TD<x-1> is equivalent to Data byte <x> of the LIN frame.

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Table 5-1720. Instance Table

Instance Name	Physical Address
LIN0	5240 0074h
LIN1	5240 1074h
LIN2	5240 2074h
LIN3	5240 3074h
LIN4	5240 4074h

Figure 5-842. LIN_LINTD0 Name Register

31	30	29	28	27	26	25	24
TD0							
R/W							
0h							
23	22	21	20	19	18	17	16
TD1							
R/W							
0h							
15	14	13	12	11	10	9	8
TD2							
R/W							
0h							
7	6	5	4	3	2	1	0
TD3							
R/W							
0h							

Table 5-1721. LIN_LINTD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TD0	R/W	0h	8-bit Transmit Buffer 0. Byte 0 to be transmitted is written into this register and then copied to SCITXSHF for transmission. Once byte 0 is written in TDO buffer, transmission will be initiated.
23:16	TD1	R/W	0h	8-bit Transmit Buffer 3. Byte 1 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
15:8	TD2	R/W	0h	8-bit Transmit Buffer 2. Byte 2 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
7:0	TD3	R/W	0h	8-bit Transmit Buffer 3. Byte 3 to be transmitted is written into this register and then copied to SCITXSHF for transmission.

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5.11.2.31 LIN_LINTD1 Register

5.11.2.31.1 LIN_LINTD1 Register (Offset = 78h) [reset = 0h]

The LINTD1 register contains the upper 4 bytes of the data to be transmitted.
NOTE: TD<x-1> is equivalent to Data byte <x> of the LIN frame.

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Table 5-1722. Instance Table

Instance Name	Physical Address
LIN0	5240 0078h
LIN1	5240 1078h
LIN2	5240 2078h
LIN3	5240 3078h
LIN4	5240 4078h

Figure 5-843. LIN_LINTD1 Name Register

31	30	29	28	27	26	25	24
TD4							
R/W							
0h							
23	22	21	20	19	18	17	16
TD5							
R/W							
0h							
15	14	13	12	11	10	9	8
TD6							
R/W							
0h							
7	6	5	4	3	2	1	0
TD7							
R/W							
0h							

Table 5-1723. LIN_LINTD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	TD4	R/W	0h	8-bit Transmit Buffer 4. Byte4 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
23:16	TD5	R/W	0h	8-bit Transmit Buffer 5. Byte 5 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
15:8	TD6	R/W	0h	8-bit Transmit Buffer 6. Byte 6 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
7:0	TD7	R/W	0h	8-bit Transmit Buffer 7. Byte 7 to be transmitted is written into this register and then copied to SCITXSHF for transmission.

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5.11.2.32 LIN_MBRSR Register

5.11.2.32.1 LIN_MBRSR Register (Offset = 7Ch) [reset = DACh]

The MBRSR register is used to configure the expected maximum baud rate of the LIN network.

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Table 5-1724. Instance Table

Instance Name	Physical Address
LIN0	5240 007Ch
LIN1	5240 107Ch
LIN2	5240 207Ch
LIN3	5240 307Ch
LIN4	5240 407Ch

Figure 5-844. LIN_MBRSR Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1			MBR				
R			R/W				
0h			DACh				
7	6	5	4	3	2	1	0
MBR							
R/W							
DACh							

Table 5-1725. LIN_MBRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED_1	R	0h	Reserved
12:0	MBR	R/W	DACh	Maximum Baud Rate Prescaler. This field is effective in LIN mode only. This 13-bit prescaler is used during the synchronization phase [see the "Header Reception and Adaptive Baudrate" section] of a target module if the ADAPT bit is set. In this way, a SCI/LIN target using an automatic or select bit rate modes detects any LIN bus legal rate automatically. The MBR value should be programmed to allow a maximum baud rate that is not more than 10% above the expected operating baud rate in the LIN network. Otherwise a s 0x00 data byte could mistakenly be detected as sync break. The default value is for a 70MHz LINCLK [0xDAC]. This MBR prescaler is used by the wake-up and idle time counters for a constant expiration time relative to a 20kHz rate.

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5.11.2.33 LIN_RESERVED_1_J Register

5.11.2.33.1 LIN_RESERVED_1_J Register (Offset = 80h) [reset = 0h]

tbd.

Return to Summary Table

Table 5-1726. Instance Table

Instance Name	Physical Address
LIN0	5240 0080h + formula
LIN1	5240 1080h + formula
LIN2	5240 2080h + formula
LIN3	5240 3080h + formula
LIN4	5240 4080h + formula

Figure 5-845. LIN_RESERVED_1_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-1727. LIN_RESERVED_1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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5.11.2.34 LIN_IODFTCTRL Register

5.11.2.34.1 LIN_IODFTCTRL Register (Offset = 90h) [reset = 500h]

The IODFTCTRL register is used to emulate various error and test conditions.

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Table 5-1728. Instance Table

Instance Name	Physical Address
LIN0	5240 0090h
LIN1	5240 1090h
LIN2	5240 2090h
LIN3	5240 3090h
LIN4	5240 4090h

Figure 5-846. LIN_IODFTCTRL Name Register

31	30	29	28	27	26	25	24
BERRENA	PBERRENA	CERRENA	ISFERRENA	RESERVED_4	FERRENA	PERRENA	BRKDTERRENA
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED_3			PINSAMPLEMASK		TXSHIFT		
R/W			R/W		R/W		
0h			0h		0h		
15	14	13	12	11	10	9	8
RESERVED_2				IODFTENA			
R				R/W			
0h				5h			
7	6	5	4	3	2	1	0
RESERVED_1						LPBENA	RXPENA
R						R/W	R/W
0h						0h	0h

Table 5-1729. LIN_IODFTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BERRENA	R/W	0h	Bit Errror Enable bit. This bit is effective in LIN mode only. This bit is used to create a Bit error. When this bit is set, the bit received is ORed with 1 and passed to the Bit monitor circuitry.
30	PBERRENA	R/W	0h	Physical Bus Error Enable bit. This bit is effective in LIN mode only. This bit is used to create a Physical Bus Error. When this bit is set, the bit received during Sync Break field transmission is ORed with 1 and passed to the Bit monitor circuitry
29	CERRENA	R/W	0h	Checksum Error Enable bit. This bit is effective in LIN mode only. This bit is used to create a checksum error. When this bit is set, the polarity of the CTYPE [checksum type] in the receive checksum calculator is changed so that a checksum error is generated.
28	ISFERRENA	R/W	0h	Inconsistent Sync Field Error Enable bit. This bit is effective in LIN mode only. This bit is used to create an ISF error. When this bit is set, the bit widths in the sync field are varied so that the ISF check fails and the error flag is set.
27	RESERVED_4	R	0h	Reserved

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Table 5-1729. LIN_IODFTCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	FERRENA	R/W	0h	This bit is used to create a Frame Error. This bit is effective in SCI-compatible mode only. When this bit is set, the stop bit received is ANDed with '0' and passed to the stop bit check circuitry.
25	PERRENA	R/W	0h	Compatible Mode only This bit is effective in SCI-compatible mode only. This bit is used to create a Parity Error. When this bit is set, in compatible mode, the parity bit received is toggled so that a parity error occurs.
24	BRKDTERRENA	R/W	0h	Compatible Mode only This bit is effective in SCI-compatible mode only. This bit is used to create BRKDT error [SCI mode only]. When this bit is set, the stop bit of the frame is ANDed with '0' and passed to the RSM so that a frame error occurs. Then the RX Pin is forced to continuous low for 10 Tbits so that a BRKDT error occurs.
23:21	RESERVED_3	R/W	0h	Reserved
20:19	PINSAMPLEMASK	R/W	0h	Pin sample mask. These bits define the sample number at which the TX Pin value that is being transmitted will be inverted to verify the receive pin samples correctly with the majority detection circuitry. Note: During IODFT mode testing for the pin sample mask, the prescalar P must be programmed to be greater than 2. 0 No Mask 1 Invert the TX Pin value at TBIT_CENTER 2 Invert the TX Pin value at TBIT_CENTER + SCLK 3 Invert the TX Pin value at TBIT_CENTER + 2 SCLK
18:16	TXSHIFT	R/W	0h	Transmit shift. These bits define the delay by which the value on LINTX is delayed so that the value on LINRX is asynchronous. [Not applicable to Start Bit] 0 No Delay 1 Delay by 1 SCLK 2 Delay by 2 SCLK 3 Delay by 3 SCLK 4 Delay by 4 SCLK 5 Delay by 5 SCLK 6 Delay by 6 SCLK 7 Delay by 7 SCLK
15:12	RESERVED_2	R	0h	Reserved
11:8	IODFTENA	R/W	5h	IO DFT Enable Key This field is used to enable the IODFT mode of the SCI/LIN module for testing. 0 IODFT is disabled 1 IODFT is disabled 2 IODFT is disabled 3 IODFT is disabled 4 IODFT is disabled 5 IODFT is disabled 6 IODFT is disabled 7 IODFT is disabled 8 IODFT is disabled 9 IODFT is disabled 10 IODFT is enabled 11 IODFT is disabled 12 IODFT is disabled 13 IODFT is disabled 14 IODFT is disabled 15 IODFT is disabled
7:2	RESERVED_1	R	0h	Reserved

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Table 5-1729. LIN_IODFTCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LPBENA	R/W	0h	Module loopback enable. In analog loopback mode the complete communication path through the I/Os can be tested, whereas in digital loopback mode the I/O buffers are excluded from this path. 0 Digital loopback is enabled. 1 Analog loopback is enabled in module I/O DFT mode (when IODFTENA = 1010)
0	RXPENA	R/W	0h	Module Analog loopback through receive pin enable. This bit defines whether the I/O buffers for the transmit or the receive pin are included in the communication path in analog loopback mode only. 0 Analog loopback through the transmit pin is enabled. 1 Analog loopback through the receive pin is enabled.

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5.11.2.35 LIN_RESERVED_2_J Register

5.11.2.35.1 LIN_RESERVED_2_J Register (Offset = 94h) [reset = 0h]

tbd.

Return to Summary Table

Table 5-1730. Instance Table

Instance Name	Physical Address
LIN0	5240 0094h + formula
LIN1	5240 1094h + formula
LIN2	5240 2094h + formula
LIN3	5240 3094h + formula
LIN4	5240 4094h + formula

Figure 5-847. LIN_RESERVED_2_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							
NONE							
0h							

Table 5-1731. LIN_RESERVED_2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	NONE	0h	Reserved

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5.11.2.36 LIN_LIN_GLB_INT_EN Register

5.11.2.36.1 LIN_LIN_GLB_INT_EN Register (Offset = E0h) [reset = 0h]

The LIN_GLB_INT_EN register is used to enable the INT0 and INT1 interrupt lines to propagate to the PIE block.

Return to Summary Table

Table 5-1732. Instance Table

Instance Name	Physical Address
LIN0	5240 00E0h
LIN1	5240 10E0h
LIN2	5240 20E0h
LIN3	5240 30E0h
LIN4	5240 40E0h

Figure 5-848. LIN_LIN_GLB_INT_EN Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						GLBINT1_EN	GLBINT0_EN
R						R/W	R/W
0h						0h	0h

Table 5-1733. LIN_LIN_GLB_INT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_1	R	0h	Reserved
1	GLBINT1_EN	R/W	0h	Global Interrupt Enable for LIN INT1. This bit determines whether the INT1 interrupt line generates an interrupt to the PIE or not 0 `LIN INT1 line does not generate an interrupt to the PIE.` 1 `LIN INT1 line generates an interrupt to the PIE if an enabled interrupt condition occurs.`
0	GLBINT0_EN	R/W	0h	Global Interrupt Enable for LIN INT0. This bit determines whether the INT0 interrupt line generates an interrupt to the PIE or not. 0 `LIN INT0 line does not generate an interrupt to the PIE.` 1 `LIN INT0 line generates an interrupt to the PIE if an enabled interrupt condition occurs.`

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5.11.2.37 LIN_LIN_GLB_INT_FLG Register

5.11.2.37.1 LIN_LIN_GLB_INT_FLG Register (Offset = E4h) [reset = 0h]

The LIN_GLB_INT_FLG register contains the current status of the INT0 and INT1 flags.

Return to Summary Table

Table 5-1734. Instance Table

Instance Name	Physical Address
LIN0	5240 00E4h
LIN1	5240 10E4h
LIN2	5240 20E4h
LIN3	5240 30E4h
LIN4	5240 40E4h

Figure 5-849. LIN_LIN_GLB_INT_FLG Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_1						INT1_FLG	INT0_FLG
R						R	R
0h						0h	0h

Table 5-1735. LIN_LIN_GLB_INT_FLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_1	R	0h	Reserved
1	INT1_FLG	R	0h	Global Interrupt Flag for LIN INT1. This bit indicates if an interrupt was generated to the PIE due to an enabled interrupt on the INT1 interrupt line. Refer to the LIN Interrupt Status Register for the condition that generated the interrupt. This bit can be cleared by Writing a 1 to the corresponding bit in the LIN_GLB_INT_CLR register. 0 No interrupt is active on the INT1 line. 1 An interrupt was generated due to an enabled interrupt on the INT1 interrupt line.

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Table 5-1735. LIN_LIN_GLB_INT_FLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT0_FLG	R	0h	Global Interrupt Flag for LIN INT0. This bit indicates if an interrupt was generated to the PIE due to an enabled interrupt on the INT0 interrupt line. Refer to the LIN Interrupt Status Register for the condition that generated the interrupt. This bit can be cleared by Writing a 1 to the corresponding bit in the LIN_GLB_INT_CLR register. 0 No interrupt is active on the INT0 line. 1 An interrupt was generated due to an enabled interrupt on the INT0 interrupt line.

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5.11.2.38 LIN_LIN_GLB_INT_CLR Register

5.11.2.38.1 LIN_LIN_GLB_INT_CLR Register (Offset = E8h) [reset = 0h]

The LIN_GLB_INT_CLR register is used to clear the interrupt flags in LIN_GLB_INT_FLG register.

Return to Summary Table

Table 5-1736. Instance Table

Instance Name	Physical Address
LIN0	5240 00E8h
LIN1	5240 10E8h
LIN2	5240 20E8h
LIN3	5240 30E8h
LIN4	5240 40E8h

Figure 5-850. LIN_LIN_GLB_INT_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED_1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_1						INT1_FLG_CLR	INT0_FLG_CLR
R						R/W1TC	R/W1TC
0h						0h	0h

Table 5-1737. LIN_LIN_GLB_INT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED_1	R	0h	Reserved
1	INT1_FLG_CLR	R/W1TC	0h	Global Interrupt flag clear for LIN INT1. This bit is used to clear the corresponding bit in the LIN_GLB_INT_FLG register. Write 1 to clear the INT1_FLG bit. Writing 0 has no effect.
0	INT0_FLG_CLR	R/W1TC	0h	Global Interrupt flag clear for LIN INT0. This bit is used to clear the corresponding bit in the LIN_GLB_INT_FLG register. Write 1 to clear the INT0_FLG bit. Writing 0 has no effect.

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5.12 MCRC

MCRC

5.12.1 MCRC Summaries

MCRC Summaries

Table 5-1738. MSS_MCRC Registers, Base Address=3500 0000h, Length=1024

Offset	Length	Register Name	MCRC0 Physical Address
0h	32	MSS_MCRC_CRC_CTRL0	3500 0000h
8h	32	MSS_MCRC_CRC_CTRL1	3500 0008h
10h	32	MSS_MCRC_CRC_CTRL2	3500 0010h
18h	32	MSS_MCRC_CRC_INTS	3500 0018h
20h	32	MSS_MCRC_CRC_INTR	3500 0020h
28h	32	MSS_MCRC_CRC_STATUS_REG	3500 0028h
30h	32	MSS_MCRC_CRC_INT_OFFSET_REG	3500 0030h
38h	32	MSS_MCRC_CRC_BUSY	3500 0038h
40h	32	MSS_MCRC_CRC_PCOUNT_REG1	3500 0040h
44h	32	MSS_MCRC_CRC_SCOUNT_REG1	3500 0044h
48h	32	MSS_MCRC_CRC_CURSEC_REG1	3500 0048h
4Ch	32	MSS_MCRC_CRC_WDTOPLD1	3500 004Ch
50h	32	MSS_MCRC_CRC_BCTOPLD1	3500 0050h
60h	32	MSS_MCRC_PSA_SIGREGL1	3500 0060h
64h	32	MSS_MCRC_PSA_SIGREGH1	3500 0064h
68h	32	MSS_MCRC_CRC_REGL1	3500 0068h
6Ch	32	MSS_MCRC_CRC_REGH1	3500 006Ch
70h	32	MSS_MCRC_PSA_SECSIGREGL1	3500 0070h
74h	32	MSS_MCRC_PSA_SECSIGREGH1	3500 0074h
78h	32	MSS_MCRC_RAW_DATAREGL1	3500 0078h
7Ch	32	MSS_MCRC_RAW_DATAREGH1	3500 007Ch
80h	32	MSS_MCRC_CRC_PCOUNT_REG2	3500 0080h
84h	32	MSS_MCRC_CRC_SCOUNT_REG2	3500 0084h
88h	32	MSS_MCRC_CRC_CURSEC_REG2	3500 0088h
8Ch	32	MSS_MCRC_CRC_WDTOPLD2	3500 008Ch
90h	32	MSS_MCRC_CRC_BCTOPLD2	3500 0090h
A0h	32	MSS_MCRC_PSA_SIGREGL2	3500 00A0h
A4h	32	MSS_MCRC_PSA_SIGREGH2	3500 00A4h
A8h	32	MSS_MCRC_CRC_REGL2	3500 00A8h
ACh	32	MSS_MCRC_CRC_REGH2	3500 00ACh
B0h	32	MSS_MCRC_PSA_SECSIGREGL2	3500 00B0h
B4h	32	MSS_MCRC_PSA_SECSIGREGH2	3500 00B4h
B8h	32	MSS_MCRC_RAW_DATAREGL2	3500 00B8h
BCh	32	MSS_MCRC_RAW_DATAREGH2	3500 00BCh
C0h	32	MSS_MCRC_CRC_PCOUNT_REG3	3500 00C0h
C4h	32	MSS_MCRC_CRC_SCOUNT_REG3	3500 00C4h
C8h	32	MSS_MCRC_CRC_CURSEC_REG3	3500 00C8h
CCh	32	MSS_MCRC_CRC_WDTOPLD3	3500 00CCh
D0h	32	MSS_MCRC_CRC_BCTOPLD3	3500 00D0h
E0h	32	MSS_MCRC_PSA_SIGREGL3	3500 00E0h

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Table 5-1738. MSS_MCRC Registers, Base Address=3500 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCRC0 Physical Address
E4h	32	MSS_MCRC_PSA_SIGREGH3	3500 00E4h
E8h	32	MSS_MCRC_CRC_REGL3	3500 00E8h
ECh	32	MSS_MCRC_CRC_REGH3	3500 00ECh
F0h	32	MSS_MCRC_PSA_SECSIGREGL3	3500 00F0h
F4h	32	MSS_MCRC_PSA_SECSIGREGH3	3500 00F4h
F8h	32	MSS_MCRC_RAW_DATAREGL3	3500 00F8h
FCh	32	MSS_MCRC_RAW_DATAREGH3	3500 00FCh
100h	32	MSS_MCRC_CRC_PCOUNT_REG4	3500 0100h
104h	32	MSS_MCRC_CRC_SCOUNT_REG4	3500 0104h
108h	32	MSS_MCRC_CRC_CURSEC_REG4	3500 0108h
10Ch	32	MSS_MCRC_CRC_WDTOPLD4	3500 010Ch
110h	32	MSS_MCRC_CRC_BCTOPLD4	3500 0110h
120h	32	MSS_MCRC_PSA_SIGREGL4	3500 0120h
124h	32	MSS_MCRC_PSA_SIGREGH4	3500 0124h
128h	32	MSS_MCRC_CRC_REGL4	3500 0128h
12Ch	32	MSS_MCRC_CRC_REGH4	3500 012Ch
130h	32	MSS_MCRC_PSA_SECSIGREGL4	3500 0130h
134h	32	MSS_MCRC_PSA_SECSIGREGH4	3500 0134h
138h	32	MSS_MCRC_RAW_DATAREGL4	3500 0138h
13Ch	32	MSS_MCRC_RAW_DATAREGH4	3500 013Ch
140h	32	MSS_MCRC_MCRC_BUS_SEL	3500 0140h

5.12.2 MCRC Registers

MCRC Registers

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5.12.2.1 MSS_MCRC_CRC_CTRL0 Register

5.12.2.1.1 MSS_MCRC_CRC_CTRL0 Register (Offset = 0h) [reset = 0h]

Contains sw reset control bit to reset PSA.

Return to Summary Table

Table 5-1739. Instance Table

Instance Name	Physical Address
MCRC0	3500 0000h

Figure 5-851. MSS_MCRC_CRC_CTRL0 Name Register

31	30	29	28	27	26	25	24
CH4_CRC_SEL2	CH4_BYTE_SWAP	CH4_BIT_SWAP	CH4_CRC_SEL		CH4_DW_SEL		CH4_PSA_SWREST
R/W	R/W	R/W	R/W		R/W		R/W
0h	0h	0h	0h		0h		0h
23	22	21	20	19	18	17	16
CH3_CRC_SEL2	CH3_BYTE_SWAP	CH3_BIT_SWAP	CH3_CRC_SEL		CH3_DW_SEL		CH3_PSA_SWREST
R/W	R/W	R/W	R/W		R/W		R/W
0h	0h	0h	0h		0h		0h
15	14	13	12	11	10	9	8
CH2_CRC_SEL2	CH2_BYTE_SWAP	CH2_BIT_SWAP	CH2_CRC_SEL		CH2_DW_SEL		CH2_PSA_SWREST
R/W	R/W	R/W	R/W		R/W		R/W
0h	0h	0h	0h		0h		0h
7	6	5	4	3	2	1	0
CH1_CRC_SEL2	CH1_BYTE_SWAP	CH1_BIT_SWAP	CH1_CRC_SEL		CH1_DW_SEL		CH1_PSA_SWREST
R/W	R/W	R/W	R/W		R/W		R/W
0h	0h	0h	0h		0h		0h

Table 5-1740. MSS_MCRC_CRC_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CH4_CRC_SEL2	R/W	0h	Refer "CH4_DW_SEL" field description
30	CH4_BYTE_SWAP	R/W	0h	BYTE SWAP Enable across Data Size 0 Byte Swap Disabled 1 Byte Swap enabled.
29	CH4_BIT_SWAP	R/W	0h	msb/lsb SWAPPING 0 msb [most significant bit First] 1 lsb [least significant bit First]
28:27	CH4_CRC_SEL	R/W	0h	CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]} 000 CRC-64 001 - CRC-16 010 CRC-32 100 - VDA CAN, SAE-J1850 CRC-8 101 - H2F, Autosar 4.0 110 - CASTAGNOLI, iSCSI 111 / 011 - E2E Profile 4
26:25	CH4_DW_SEL	R/W	0h	CRC Data Size select. 000 64 bit Data Size 001 - 16 bit Data Size 010 32 Bit Data Size

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Table 5-1740. MSS_MCRC_CRC_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CH4_PSA_SWREST	R/W	0h	Channel 4 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by Writing a 0. 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
23	CH3_CRC_SEL2	R/W	0h	Refer "CH3_DW_SEL" field description
22	CH3_BYTE_SWAP	R/W	0h	BYTE SWAP Enable across Data Size 0 Byte Swap Disabled 1 Byte Swap enabled.
21	CH3_BIT_SWAP	R/W	0h	msb/lsb SWAPPING 0 msb [most significant bit First] 1 lsb [least significant bit First]
20:19	CH3_CRC_SEL	R/W	0h	CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]} 000 CRC-64 001 - CRC-16 010 CRC-32 100 - VDA CAN, SAE-J1850 CRC-8 101 - H2F, Autosar 4.0 110 - CASTAGNOLI, iSCSI 111 / 011 - E2E Profile 4
18:17	CH3_DW_SEL	R/W	0h	CRC Data Size select. 000 64 bit Data Size 001 - 16 bit Data Size 010 32 Bit Data Size
16	CH3_PSA_SWREST	R/W	0h	Channel 3 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by Writing a 0. 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
15	CH2_CRC_SEL2	R/W	0h	Refer "CH2_DW_SEL" field description
14	CH2_BYTE_SWAP	R/W	0h	BYTE SWAP Enable across Data Size 0 Byte Swap Disabled 1 Byte Swap enabled.
13	CH2_BIT_SWAP	R/W	0h	msb/lsb SWAPPING 0 msb [most significant bit First] 1 lsb [least significant bit First]
12:11	CH2_CRC_SEL	R/W	0h	CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]} 000 CRC-64 001 - CRC-16 010 CRC-32 100 - VDA CAN, SAE-J1850 CRC-8 101 - H2F, Autosar 4.0 110 - CASTAGNOLI, iSCSI 111 / 011 - E2E Profile 4
10:9	CH2_DW_SEL	R/W	0h	CRC Data Size select. 000 64 bit Data Size 001 - 16 bit Data Size 010 32 Bit Data Size
8	CH2_PSA_SWREST	R/W	0h	Channel 2 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by Writing a 0. 0 = PSA Signature Register not reset 1 = PSA Signature Register reset
7	CH1_CRC_SEL2	R/W	0h	Refer "CH1_DW_SEL" field description
6	CH1_BYTE_SWAP	R/W	0h	BYTE SWAP Enable across Data Size 0 Byte Swap Disabled 1 Byte Swap enabled.

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Table 5-1740. MSS_MCRC_CRC_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CH1_BIT_SWAP	R/W	0h	msb/lsb SWAPPING 0 msb [most significant bit First] 1 lsb [least significant bit First]
4:3	CH1_CRC_SEL	R/W	0h	CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]} 000 CRC-64 001 - CRC-16 010 CRC-32 100 - VDA CAN, SAE-J1850 CRC-8 101 - H2F, Autosar 4.0 110 - CASTAGNOLI, iSCSI 111 / 011 - E2E Profile 4
2:1	CH1_DW_SEL	R/W	0h	CRC Data Size select. 000 64 bit Data Size 001 - 16 bit Data Size 010 32 Bit Data Size
0	CH1_PSA_SWREST	R/W	0h	Channel 1 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by Writing a 0. 0 = PSA Signature Register not reset 1 = PSA Signature Register reset

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5.12.2.2 MSS_MCRC_CRC_CTRL1 Register

5.12.2.2.1 MSS_MCRC_CRC_CTRL1 Register (Offset = 8h) [reset = 0h]

Contains power down control bit.

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Table 5-1741. Instance Table

Instance Name	Physical Address
MCRC0	3500 0008h

Figure 5-852. MSS_MCRC_CRC_CTRL1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1							PWDN
R							R/W
0h							0h

Table 5-1742. MSS_MCRC_CRC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED1	R	0h	
0	PWDN	R/W	0h	Power Down. When set, MCRC moduleMCRC Module is put in power down mode. 0 = MCRC is not in power down mode 1 = MCRC is in power down mode

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5.12.2.3 MSS_MCRC_CRC_CTRL2 Register

5.12.2.3.1 MSS_MCRC_CRC_CTRL2 Register (Offset = 10h) [reset = 0h]

Contains channel mode, data trace enable control bits.

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Table 5-1743. Instance Table

Instance Name	Physical Address
MCRC0	3500 0010h

Figure 5-853. MSS_MCRC_CRC_CTRL2 Name Register

31	30	29	28	27	26	25	24
RESERVED5						CH4_MODE	
R						R/W	
0h						0h	
23	22	21	20	19	18	17	16
RESERVED4						CH3_MODE	
R						R/W	
0h						0h	
15	14	13	12	11	10	9	8
RESERVED3						CH2_MODE	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED2			CH1_TRACEEN	RESERVED1		CH1_MODE	
R			R/W	R		R/W	
0h			0h	0h		0h	

Table 5-1744. MSS_MCRC_CRC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:26	RESERVED5	R	0h	
25:24	CH4_MODE	R/W	0h	Channel 4 Mode: 0 0 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register 0 1 = AUTO mode 1 0 = reserved 1 1 = Full-CPU mode
23:18	RESERVED4	R	0h	
17:16	CH3_MODE	R/W	0h	Channel 3 Mode: 0 0 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register 0 1 = AUTO mode 1 0 = reserved 1 1 = Full-CPU mode
15:10	RESERVED3	R	0h	

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Table 5-1744. MSS_MCRC_CRC_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:8	CH2_MODE	R/W	0h	Channel 2 Mode: 0 0 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register 0 1 = AUTO mode 1 0 = reserved 1 1 = Full-CPU mode
7:5	RESERVED2	R	0h	
4	CH1_TRACEEN	R/W	0h	Channel 1 Data Trace Enable. When set, the channel is put into data trace mode. The channel snoops on the CPU VBUSM, ITCM, DTCM buses for any read transaction. Any read data on these buses is compressed by the PSA Signature Register. When suspend is on, the PSA Signature Register does not compress any read data on these buses. 0 = Data Trace disable 1 = Data Trace enable
3:2	RESERVED1	R	0h	
1:0	CH1_MODE	R/W	0h	Channel 1 Mode: 0 0 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register 0 1 = AUTO mode 1 0 = reserved 1 1 = Full-CPU mode

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5.12.2.4 MSS_MCRC_CRC_INTS Register

5.12.2.4.1 MSS_MCRC_CRC_INTS Register (Offset = 18h) [reset = 0h]

CRC interrupt enable register. Write one to a bit to enable a interrupt.

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Table 5-1745. Instance Table

Instance Name	Physical Address
MCRC0	3500 0018h

Figure 5-854. MSS_MCRC_CRC_INTS Name Register

31	30	29	28	27	26	25	24
RESERVED5			CH4_TIMEOUTENS	CH4_UNDERENS	CH4_OVERENS	CH4_CRCFAILENS	RESERVED4
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED4			CH3_TIMEOUTENS	CH3_UNDERENS	CH3_OVERENS	CH3_CRCFAILENS	RESERVED3
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED3			CH2_TIMEOUTENS	CH2_UNDERENS	CH2_OVERENS	CH2_CRCFAILENS	RESERVED2
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED2			CH1_TIMEOUTENS	CH1_UNDERENS	CH1_OVERENS	CH1_CRCFAILENS	RESERVED1
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h

Table 5-1746. MSS_MCRC_CRC_INTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED5	R	0h	
28	CH4_TIMEOUTENS	R/W	0h	Channel 4 Timeout Interrupt Enable Bit. Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
27	CH4_UNDERENS	R/W	0h	Channel 4 Underrun Interrupt Enable Bit. Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable

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Table 5-1746. MSS_MCRC_CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	CH4_OVERENS	R/W	0h	Channel 4 Overrun Interrupt Enable Bit. Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
25	CH4_CRCFAILENS	R/W	0h	Channel 4 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
24:21	RESERVED4	R	0h	
20	CH3_TIMEOUTENS	R/W	0h	Channel 3 Timeout Interrupt Enable Bit. Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
19	CH3_UNDERENS	R/W	0h	Channel 3 Underrun Interrupt Enable Bit. Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
18	CH3_OVERENS	R/W	0h	Channel 3 Overrun Interrupt Enable Bit. Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
17	CH3_CRCFAILENS	R/W	0h	Channel 3 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
16:13	RESERVED3	R	0h	

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Table 5-1746. MSS_MCRC_CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CH2_TIMEOUTENS	R/W	0h	Channel 2 Timeout Interrupt Enable Bit. Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
11	CH2_UNDERENS	R/W	0h	Channel 2 Underrun Interrupt Enable Bit. Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
10	CH2_OVERENS	R/W	0h	Channel 2 Overrun Interrupt Enable Bit. Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable
9	CH2_CRCFAILENS	R/W	0h	Channel 2 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
8:5	RESERVED2	R	0h	
4	CH1_TIMEOUTENS	R/W	0h	Channel 1 Timeout Interrupt Enable Bit. Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable
3	CH1_UNDERENS	R/W	0h	Channel 1 Underrun Interrupt Enable Bit. Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable
2	CH1_OVERENS	R/W	0h	Channel 1 Overrun Interrupt Enable Bit. Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable

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Table 5-1746. MSS_MCRC_CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CH1_CRCFAILENS	R/W	0h	Channel 1 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable
0	RESERVED1	R	0h	

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5.12.2.5 MSS_MCRC_CRC_INTR Register

5.12.2.5.1 MSS_MCRC_CRC_INTR Register (Offset = 20h) [reset = 0h]

CRC interrupt disable register. Write one to a bit to disable a interrupt.

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Table 5-1747. Instance Table

Instance Name	Physical Address
MCRC0	3500 0020h

Figure 5-855. MSS_MCRC_CRC_INTR Name Register

31	30	29	28	27	26	25	24
RESERVED5			CH4_TIMEOUTENR	CH4_UNDERENR	CH4_OVERENR	CH4_CRCFAILENR	RESERVED4
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED4			CH3_TIMEOUTENR	CH3_UNDERENR	CH3_OVERENR	CH3_CRCFAILENR	RESERVED3
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED3			CH2_TIMEOUTENR	CH2_UNDERENR	CH2_OVERENR	CH2_CRCFAILENR	RESERVED2
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2			CH1_TIMEOUTENR	CH1_UNDERENR	CH1_OVERENR	CH1_CRCFAILENR	RESERVED1
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h

Table 5-1748. MSS_MCRC_CRC_INTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED5	R	0h	
28	CH4_TIMEOUTENR	R/W	0h	Channel 4 Timeout Interrupt Disable Bit. Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt disable
27	CH4_UNDERENR	R/W	0h	Channel 4 Underrun Interrupt Disable Bit. Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt disable

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Table 5-1748. MSS_MCRC_CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	CH4_OVERENR	R/W	0h	Channel 4 Overrun Interrupt Disable Bit. Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt disable
25	CH4_CRCFAILENR	R/W	0h	Channel 4 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt disable
24:21	RESERVED4	R	0h	
20	CH3_TIMEOUTENR	R/W	0h	Channel 3 Timeout Interrupt Disable Bit. Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt disable
19	CH3_UNDERENR	R/W	0h	Channel 3 Underrun Interrupt Disable Bit. Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt disable
18	CH3_OVERENR	R/W	0h	Channel 3 Overrun Interrupt Disable Bit. Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt disable
17	CH3_CRCFAILENR	R/W	0h	Channel 3 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt disable
16:13	RESERVED3	R	0h	

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Table 5-1748. MSS_MCRC_CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CH2_TIMEOUTENR	R/W	0h	Channel 2 Timeout Interrupt Disable Bit. Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt disable
11	CH2_UNDERENR	R/W	0h	Channel 2 Underrun Interrupt Disable Bit. Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt disable
10	CH2_OVERENR	R/W	0h	Channel 2 Overrun Interrupt Disable Bit. Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt disable
9	CH2_CRCFAILENR	R/W	0h	Channel 2 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt disable
8:5	RESERVED2	R	0h	
4	CH1_TIMEOUTENR	R/W	0h	Channel 1 Timeout Interrupt Disable Bit. Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt disable
3	CH1_UNDERENR	R/W	0h	Channel 1 Underrun Interrupt Disable Bit. Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt disable

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Table 5-1748. MSS_MCRC_CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CH1_OVERENR	R/W	0h	Channel 1 Overrun Interrupt Disable Bit. Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt disable
1	CH1_CRCFAILENR	R/W	0h	Channel 1 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt disable
0	RESERVED1	R	0h	

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5.12.2.6 MSS_MCRC_CRC_STATUS_REG Register

5.12.2.6.1 MSS_MCRC_CRC_STATUS_REG Register (Offset = 28h) [reset = 0h]

CRC interrupt status register. Contains interrupt flags for different types of interrupt.

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Table 5-1749. Instance Table

Instance Name	Physical Address
MCRC0	3500 0028h

Figure 5-856. MSS_MCRC_CRC_STATUS_REG Name Register

31	30	29	28	27	26	25	24
RESERVED5			CH4_TIMEOUT	CH4_UNDER	CH4_OVER	CH4_CRCFAIL	RESERVED4
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED4			CH3_TIMEOUT	CH3_UNDER	CH3_OVER	CH3_CRCFAIL	RESERVED3
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED3			CH2_TIMEOUT	CH2_UNDER	CH2_OVER	CH2_CRCFAIL	RESERVED2
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED2			CH1_TIMEOUT	CH1_UNDER	CH1_OVER	CH1_CRCFAIL	RESERVED1
R			R/W	R/W	R/W	R/W	R
0h			0h	0h	0h	0h	0h

Table 5-1750. MSS_MCRC_CRC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED5	R	0h	
28	CH4_TIMEOUT	R/W	0h	Channel 4 CRC Timeout Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
27	CH4_UNDER	R/W	0h	Channel 4 CRC Underrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
26	CH4_OVER	R/W	0h	Channel 4 CRC Overrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
25	CH4_CRCFAIL	R/W	0h	Channel 4 CRC Compare Fail Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
24:21	RESERVED4	R	0h	

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Table 5-1750. MSS_MCRC_CRC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	CH3_TIMEOUT	R/W	0h	Channel 3 CRC Timeout Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
19	CH3_UNDER	R/W	0h	Channel 3 CRC Underrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
18	CH3_OVER	R/W	0h	Channel 3 CRC Overrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
17	CH3_CRCFAIL	R/W	0h	Channel 3 CRC Compare Fail Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
16:13	RESERVED3	R	0h	
12	CH2_TIMEOUT	R/W	0h	Channel 2 CRC Timeout Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
11	CH2_UNDER	R/W	0h	Channel 2 CRC Underrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
10	CH2_OVER	R/W	0h	Channel 2 CRC Overrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
9	CH2_CRCFAIL	R/W	0h	Channel 2 CRC Compare Fail Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active
8:5	RESERVED2	R	0h	
4	CH1_TIMEOUT	R/W	0h	Channel 1 CRC Timeout Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active
3	CH1_UNDER	R/W	0h	Channel 1 CRC Underrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active
2	CH1_OVER	R/W	0h	Channel 1 CRC Overrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active
1	CH1_CRCFAIL	R/W	0h	Channel 1 CRC Compare Fail Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active

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Table 5-1750. MSS_MCRC_CRC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED1	R	0h	

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5.12.2.7 MSS_MCRC_CRC_INT_OFFSET_REG Register

5.12.2.7.1 MSS_MCRC_CRC_INT_OFFSET_REG Register (Offset = 30h) [reset = 0h]

Register indicates highest priority pending interrupt vector address.

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Table 5-1751. Instance Table

Instance Name	Physical Address
MCRC0	3500 0030h

Figure 5-857. MSS_MCRC_CRC_INT_OFFSET_REG Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
OFSTREG							
R/W							
0h							

Table 5-1752. MSS_MCRC_CRC_INT_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:0	OFSTREG	R/W	0h	CRC Interrupt Offset. This register indicates the highest priority pending interrupt vector address. Reading the offset register auto-matically clear the respective interrupt flag.

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5.12.2.8 MSS_MCRC_CRC_BUSY Register

5.12.2.8.1 MSS_MCRC_CRC_BUSY Register (Offset = 38h) [reset = 0h]

Register indicates CRC busy flag for each channel.

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Table 5-1753. Instance Table

Instance Name	Physical Address
MCRC0	3500 0038h

Figure 5-858. MSS_MCRC_CRC_BUSY Name Register

31	30	29	28	27	26	25	24
RESERVED4							CH4_BUSY
R							R
0h							0h
23	22	21	20	19	18	17	16
RESERVED3							CH3_BUSY
R							R
0h							0h
15	14	13	12	11	10	9	8
RESERVED2							CH2_BUSY
R							R
0h							0h
7	6	5	4	3	2	1	0
RESERVED1							CH1_BUSY
R							R
0h							0h

Table 5-1754. MSS_MCRC_CRC_BUSY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED4	R	0h	
24	CH4_BUSY	R	0h	Ch4_BUSY. During AUTO mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
23:17	RESERVED3	R	0h	
16	CH3_BUSY	R	0h	Ch3_BUSY. During AUTO mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
15:9	RESERVED2	R	0h	
8	CH2_BUSY	R	0h	Ch2_BUSY. During AUTO mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.
7:1	RESERVED1	R	0h	
0	CH1_BUSY	R	0h	CH1_BUSY. During AUTO mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed.

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5.12.2.9 MSS_MCRC_CRC_PCOUNT_REG1 Register

5.12.2.9.1 MSS_MCRC_CRC_PCOUNT_REG1 Register (Offset = 40h) [reset = 0h]

Channel 1 preload register for the pattern count.

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Table 5-1755. Instance Table

Instance Name	Physical Address
MCRC0	3500 0040h

Figure 5-859. MSS_MCRC_CRC_PCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1				CRC_PAT_COUNT1			
R				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CRC_PAT_COUNT1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_PAT_COUNT1							
R/W							
0h							

Table 5-1756. MSS_MCRC_CRC_PCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	
19:0	CRC_PAT_COUNT1	R/W	0h	Channel 1 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

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5.12.2.10 MSS_MCRC_CRC_SCOUNT_REG1 Register

5.12.2.10.1 MSS_MCRC_CRC_SCOUNT_REG1 Register (Offset = 44h) [reset = 0h]

Channel 1 preload register for the sector count.

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Table 5-1757. Instance Table

Instance Name	Physical Address
MCRC0	3500 0044h

Figure 5-860. MSS_MCRC_CRC_SCOUNT_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
CRC_SEC_COUNT1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_SEC_COUNT1							
R/W							
0h							

Table 5-1758. MSS_MCRC_CRC_SCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	
15:0	CRC_SEC_COUNT1	R/W	0h	Channel 1 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

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5.12.2.11 MSS_MCRC_CRC_CURSEC_REG1 Register

5.12.2.11.1 MSS_MCRC_CRC_CURSEC_REG1 Register (Offset = 48h) [reset = 0h]

Channel 1 current sector register contains the sector number which causes CRC failure.

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Table 5-1759. Instance Table

Instance Name	Physical Address
MCRC0	3500 0048h

Figure 5-861. MSS_MCRC_CRC_CURSEC_REG1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_CURSEC1							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_CURSEC1							
R/W							
0h							

Table 5-1760. MSS_MCRC_CRC_CURSEC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	
15:0	CRC_CURSEC1	R/W	0h	Channel 1 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.

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5.12.2.12 MSS_MCRC_CRC_WDTOPLD1 Register

5.12.2.12.1 MSS_MCRC_CRC_WDTOPLD1 Register (Offset = 4Ch) [reset = 0h]

Channel 1 timeout pre-load value to check if within a given time DMA initiates a block transfer.

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Table 5-1761. Instance Table

Instance Name	Physical Address
MCRC0	3500 004Ch

Figure 5-862. MSS_MCRC_CRC_WDTOPLD1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
CRC_WDTOPLD1							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_WDTOPLD1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_WDTOPLD1							
R/W							
0h							

Table 5-1762. MSS_MCRC_CRC_WDTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	
23:0	CRC_WDTOPLD1	R/W	0h	Channel 1 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

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5.12.2.13 MSS_MCRC_CRC_BCTOPLD1 Register

5.12.2.13.1 MSS_MCRC_CRC_BCTOPLD1 Register (Offset = 50h) [reset = 0h]

Channel 1 timeout pre-load value to check if one block of patterns are compressed with a given time.

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Table 5-1763. Instance Table

Instance Name	Physical Address
MCRC0	3500 0050h

Figure 5-863. MSS_MCRC_CRC_BCTOPLD1 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD1							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD1							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD1							
R/W							
0h							

Table 5-1764. MSS_MCRC_CRC_BCTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	
23:0	CRC_BCTOPLD1	R/W	0h	Channel 1 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated.

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5.12.2.14 MSS_MCRC_PSA_SIGREGL1 Register

5.12.2.14.1 MSS_MCRC_PSA_SIGREGL1 Register (Offset = 60h) [reset = 0h]

Channel 1 PSA signature low register.

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Table 5-1765. Instance Table

Instance Name	Physical Address
MCRC0	3500 0060h

Figure 5-864. MSS_MCRC_PSA_SIGREGL1 Name Register

31	30	29	28	27	26	25	24
PSASIG1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG1_31_0							
R/W							
0h							

Table 5-1766. MSS_MCRC_PSA_SIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG1_31_0	R/W	0h	Channel 1 PSA Signature Low Register. This register contains the value stored at PSASIG1[31:0] register.

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5.12.2.15 MSS_MCRC_PSA_SIGREGH1 Register

5.12.2.15.1 MSS_MCRC_PSA_SIGREGH1 Register (Offset = 64h) [reset = 0h]

Channel 1 PSA signature high register.

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Table 5-1767. Instance Table

Instance Name	Physical Address
MCRC0	3500 0064h

Figure 5-865. MSS_MCRC_PSA_SIGREGH1 Name Register

31	30	29	28	27	26	25	24
PSA_SIG1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSA_SIG1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSA_SIG1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSA_SIG1_63_32							
R/W							
0h							

Table 5-1768. MSS_MCRC_PSA_SIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSA_SIG1_63_32	R/W	0h	Channel 1 PSA Signature High Register. This register contains the value stored at PSASIG1[63:32] register.

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5.12.2.16 MSS_MCRC_CRC_REGL1 Register

5.12.2.16.1 MSS_MCRC_CRC_REGL1 Register (Offset = 68h) [reset = 0h]

Channel 1 CRC value low register.

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Table 5-1769. Instance Table

Instance Name	Physical Address
MCRC0	3500 0068h

Figure 5-866. MSS_MCRC_CRC_REGL1 Name Register

31	30	29	28	27	26	25	24
CRC1_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC1_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC1_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC1_31_0							
R/W							
0h							

Table 5-1770. MSS_MCRC_CRC_REGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC1_31_0	R/W	0h	Channel 1 CRC Value Low Register. This register contains the current known good signature value stored at CRC1[31:0] register.

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5.12.2.17 MSS_MCRC_CRC_REGH1 Register

5.12.2.17.1 MSS_MCRC_CRC_REGH1 Register (Offset = 6Ch) [reset = 0h]

Channel 1 CRC value high register.

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Table 5-1771. Instance Table

Instance Name	Physical Address
MCRC0	3500 006Ch

Figure 5-867. MSS_MCRC_CRC_REGH1 Name Register

31	30	29	28	27	26	25	24
CRC1_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC1_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC1_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC1_63_32							
R/W							
0h							

Table 5-1772. MSS_MCRC_CRC_REGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC1_63_32	R/W	0h	Channel 1 CRC Value High Register. This register contains the current known good signature value stored at CRC1[63:32] register.

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5.12.2.18 MSS_MCRC_PSA_SECSIGREGL1 Register

5.12.2.18.1 MSS_MCRC_PSA_SECSIGREGL1 Register (Offset = 70h) [reset = 0h]

Channel 1 PSA sector signature low regis-ter.

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Table 5-1773. Instance Table

Instance Name	Physical Address
MCRC0	3500 0070h

Figure 5-868. MSS_MCRC_PSA_SECSIGREGL1 Name Register

31	30	29	28	27	26	25	24
PSASECSIG1_31_0							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG1_31_0							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG1_31_0							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG1_31_0							
R							
0h							

Table 5-1774. MSS_MCRC_PSA_SECSIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG1_31_0	R	0h	Channel 1 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG1[31:0] register.

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5.12.2.19 MSS_MCRC_PSA_SECSIGREGH1 Register

5.12.2.19.1 MSS_MCRC_PSA_SECSIGREGH1 Register (Offset = 74h) [reset = 0h]

Channel 1 PSA sector signature high regis-ter.

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Table 5-1775. Instance Table

Instance Name	Physical Address
MCRC0	3500 0074h

Figure 5-869. MSS_MCRC_PSA_SECSIGREGH1 Name Register

31	30	29	28	27	26	25	24
PSASECSIG1_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG1_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG1_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG1_63_32							
R							
0h							

Table 5-1776. MSS_MCRC_PSA_SECSIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG1_63_32	R	0h	Channel 1 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG1[63:32] register.

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5.12.2.20 MSS_MCRC_RAW_DATAREGL1 Register

5.12.2.20.1 MSS_MCRC_RAW_DATAREGL1 Register (Offset = 78h) [reset = 0h]

Channel 1 un-compressed raw data low register.

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Table 5-1777. Instance Table

Instance Name	Physical Address
MCRC0	3500 0078h

Figure 5-870. MSS_MCRC_RAW_DATAREGL1 Name Register

31	30	29	28	27	26	25	24
RAW_DATA1_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA1_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA1_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA1_31_0							
R							
0h							

Table 5-1778. MSS_MCRC_RAW_DATAREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA1_31_0	R	0h	Channel 1 Raw Data Low Register. This register contains bit 31:0 of the un-compressed raw data.

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5.12.2.21 MSS_MCRC_RAW_DATAREGH1 Register

5.12.2.21.1 MSS_MCRC_RAW_DATAREGH1 Register (Offset = 7Ch) [reset = 0h]

Channel 1 un-compressed raw data high register.

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Table 5-1779. Instance Table

Instance Name	Physical Address
MCRC0	3500 007Ch

Figure 5-871. MSS_MCRC_RAW_DATAREGH1 Name Register

31	30	29	28	27	26	25	24
RAW_DATA1_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA1_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA1_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA1_63_32							
R							
0h							

Table 5-1780. MSS_MCRC_RAW_DATAREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA1_63_32	R	0h	Channel 1 Raw Data High Register. This register contains bit 63:32 of the un-compressed raw data.

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5.12.2.22 MSS_MCRC_CRC_PCOUNT_REG2 Register

5.12.2.22.1 MSS_MCRC_CRC_PCOUNT_REG2 Register (Offset = 80h) [reset = 0h]

Channel 2 preload register for the pattern count.

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Table 5-1781. Instance Table

Instance Name	Physical Address
MCRC0	3500 0080h

Figure 5-872. MSS_MCRC_CRC_PCOUNT_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1				CRC_PAT_COUNT2			
R				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_PAT_COUNT2							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_PAT_COUNT2							
R/W							
0h							

Table 5-1782. MSS_MCRC_CRC_PCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	
19:0	CRC_PAT_COUNT2	R/W	0h	Channel 2 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

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5.12.2.23 MSS_MCRC_CRC_SCOUNT_REG2 Register

5.12.2.23.1 MSS_MCRC_CRC_SCOUNT_REG2 Register (Offset = 84h) [reset = 0h]

Channel 2 preload register for the sector count.

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Table 5-1783. Instance Table

Instance Name	Physical Address
MCRC0	3500 0084h

Figure 5-873. MSS_MCRC_CRC_SCOUNT_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
CRC_SEC_COUNT2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_SEC_COUNT2							
R/W							
0h							

Table 5-1784. MSS_MCRC_CRC_SCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	
15:0	CRC_SEC_COUNT2	R/W	0h	Channel 2 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

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5.12.2.24 MSS_MCRC_CRC_CURSEC_REG2 Register

5.12.2.24.1 MSS_MCRC_CRC_CURSEC_REG2 Register (Offset = 88h) [reset = 0h]

Channel 2 current sector register contains the sector number which causes CRC fail-ure.

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Table 5-1785. Instance Table

Instance Name	Physical Address
MCRC0	3500 0088h

Figure 5-874. MSS_MCRC_CRC_CURSEC_REG2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC2							
R/W							
0h							

Table 5-1786. MSS_MCRC_CRC_CURSEC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	
15:0	CRC_CURSEC2	R/W	0h	Channel 2 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erro-neous sector number.

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5.12.2.25 MSS_MCRC_CRC_WDTOPLD2 Register

5.12.2.25.1 MSS_MCRC_CRC_WDTOPLD2 Register (Offset = 8Ch) [reset = 0h]

Channel 2 timeout pre-load value to check if within a given time DMA initiates a block transfer.

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Table 5-1787. Instance Table

Instance Name	Physical Address
MCRC0	3500 008Ch

Figure 5-875. MSS_MCRC_CRC_WDTOPLD2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
CRC_WDTOPLD2							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_WDTOPLD2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_WDTOPLD2							
R/W							
0h							

Table 5-1788. MSS_MCRC_CRC_WDTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	
23:0	CRC_WDTOPLD2	R/W	0h	Channel 2 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

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5.12.2.26 MSS_MCRC_CRC_BCTOPLD2 Register

5.12.2.26.1 MSS_MCRC_CRC_BCTOPLD2 Register (Offset = 90h) [reset = 0h]

Channel 2 timeout pre-load value to check if one block of patterns are compressed with a given time.

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Table 5-1789. Instance Table

Instance Name	Physical Address
MCRC0	3500 0090h

Figure 5-876. MSS_MCRC_CRC_BCTOPLD2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD2							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD2							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD2							
R/W							
0h							

Table 5-1790. MSS_MCRC_CRC_BCTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	
23:0	CRC_BCTOPLD2	R/W	0h	Channel 2 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated.

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5.12.2.27 MSS_MCRC_PSA_SIGREGL2 Register

5.12.2.27.1 MSS_MCRC_PSA_SIGREGL2 Register (Offset = A0h) [reset = 0h]

Channel 2 PSA signature low register.

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Table 5-1791. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A0h

Figure 5-877. MSS_MCRC_PSA_SIGREGL2 Name Register

31	30	29	28	27	26	25	24
PSASIG2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG2_31_0							
R/W							
0h							

Table 5-1792. MSS_MCRC_PSA_SIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG2_31_0	R/W	0h	Channel 2 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register.

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5.12.2.28 MSS_MCRC_PSA_SIGREGH2 Register

5.12.2.28.1 MSS_MCRC_PSA_SIGREGH2 Register (Offset = A4h) [reset = 0h]

Channel 2 PSA signature high register.

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Table 5-1793. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A4h

Figure 5-878. MSS_MCRC_PSA_SIGREGH2 Name Register

31	30	29	28	27	26	25	24
PSA_SIG2_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSA_SIG2_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSA_SIG2_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSA_SIG2_63_32							
R/W							
0h							

Table 5-1794. MSS_MCRC_PSA_SIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSA_SIG2_63_32	R/W	0h	Channel 2 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register.

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5.12.2.29 MSS_MCRC_CRC_REGL2 Register

5.12.2.29.1 MSS_MCRC_CRC_REGL2 Register (Offset = A8h) [reset = 0h]

Channel 2 CRC value low register.

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Table 5-1795. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A8h

Figure 5-879. MSS_MCRC_CRC_REGL2 Name Register

31	30	29	28	27	26	25	24
CRC2_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC2_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC2_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC2_31_0							
R/W							
0h							

Table 5-1796. MSS_MCRC_CRC_REGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC2_31_0	R/W	0h	Channel 2 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] register.

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5.12.2.30 MSS_MCRC_CRC_REGH2 Register

5.12.2.30.1 MSS_MCRC_CRC_REGH2 Register (Offset = ACh) [reset = 0h]

Channel 2 CRC value high register.

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Table 5-1797. Instance Table

Instance Name	Physical Address
MCRC0	3500 00ACh

Figure 5-880. MSS_MCRC_CRC_REGH2 Name Register

31	30	29	28	27	26	25	24
CRC2_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC2_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC2_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC2_63_32							
R/W							
0h							

Table 5-1798. MSS_MCRC_CRC_REGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC2_63_32	R/W	0h	Channel 2 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register.

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5.12.2.31 MSS_MCRC_PSA_SECSIGREGL2 Register

5.12.2.31.1 MSS_MCRC_PSA_SECSIGREGL2 Register (Offset = B0h) [reset = 0h]

Channel 2 PSA sector signature low regis-ter.

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Table 5-1799. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B0h

Figure 5-881. MSS_MCRC_PSA_SECSIGREGL2 Name Register

31	30	29	28	27	26	25	24
PSASECSIG2_31_0							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG2_31_0							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG2_31_0							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG2_31_0							
R							
0h							

Table 5-1800. MSS_MCRC_PSA_SECSIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG2_31_0	R	0h	Channel 2 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register.

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5.12.2.32 MSS_MCRC_PSA_SECSIGREGH2 Register

5.12.2.32.1 MSS_MCRC_PSA_SECSIGREGH2 Register (Offset = B4h) [reset = 0h]

Channel 2 PSA sector signature high regis-ter.

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Table 5-1801. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B4h

Figure 5-882. MSS_MCRC_PSA_SECSIGREGH2 Name Register

31	30	29	28	27	26	25	24
PSASECSIG2_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG2_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG2_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG2_63_32							
R							
0h							

Table 5-1802. MSS_MCRC_PSA_SECSIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG2_63_32	R	0h	Channel 2 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register.

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5.12.2.33 MSS_MCRC_RAW_DATAREGL2 Register

5.12.2.33.1 MSS_MCRC_RAW_DATAREGL2 Register (Offset = B8h) [reset = 0h]

Channel 2 un-compressed raw data low register.

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Table 5-1803. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B8h

Figure 5-883. MSS_MCRC_RAW_DATAREGL2 Name Register

31	30	29	28	27	26	25	24
RAW_DATA2_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA2_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA2_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA2_31_0							
R							
0h							

Table 5-1804. MSS_MCRC_RAW_DATAREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA2_31_0	R	0h	Channel 2 Raw Data Low Register. This register contains bit 31:0 of the un-compressed raw data.

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5.12.2.34 MSS_MCRC_RAW_DATAREGH2 Register

5.12.2.34.1 MSS_MCRC_RAW_DATAREGH2 Register (Offset = BCh) [reset = 0h]

Channel 2 un-compressed raw data high Register.

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Table 5-1805. Instance Table

Instance Name	Physical Address
MCRC0	3500 00BCh

Figure 5-884. MSS_MCRC_RAW_DATAREGH2 Name Register

31	30	29	28	27	26	25	24
RAW_DATA2_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA2_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA2_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA2_63_32							
R							
0h							

Table 5-1806. MSS_MCRC_RAW_DATAREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA2_63_32	R	0h	Channel 2 Raw Data High Register. This register contains bit 63:32 of the un-compressed raw data.

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5.12.2.35 MSS_MCRC_CRC_PCOUNT_REG3 Register

5.12.2.35.1 MSS_MCRC_CRC_PCOUNT_REG3 Register (Offset = C0h) [reset = 0h]

Channel 3 preload register for the pattern count.

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Table 5-1807. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C0h

Figure 5-885. MSS_MCRC_CRC_PCOUNT_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1				CRC_PAT_COUNT3			
R				R/W			
0h				0h			
15	14	13	12	11	10	9	8
CRC_PAT_COUNT3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_PAT_COUNT3							
R/W							
0h							

Table 5-1808. MSS_MCRC_CRC_PCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	
19:0	CRC_PAT_COUNT3	R/W	0h	Channel 3 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

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5.12.2.36 MSS_MCRC_CRC_SCOUNT_REG3 Register

5.12.2.36.1 MSS_MCRC_CRC_SCOUNT_REG3 Register (Offset = C4h) [reset = 0h]

Channel 3 preload register for the sector count.

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Table 5-1809. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C4h

Figure 5-886. MSS_MCRC_CRC_SCOUNT_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_SEC_COUNT3							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_SEC_COUNT3							
R/W							
0h							

Table 5-1810. MSS_MCRC_CRC_SCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	
15:0	CRC_SEC_COUNT3	R/W	0h	Channel 3 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

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5.12.2.37 MSS_MCRC_CRC_CURSEC_REG3 Register

5.12.2.37.1 MSS_MCRC_CRC_CURSEC_REG3 Register (Offset = C8h) [reset = 0h]

Channel 3 current sector register contains the sector number which causes CRC fail-ure.

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Table 5-1811. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C8h

Figure 5-887. MSS_MCRC_CRC_CURSEC_REG3 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC3							
R/W							
0h							

Table 5-1812. MSS_MCRC_CRC_CURSEC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	
15:0	CRC_CURSEC3	R/W	0h	Channel 3 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erro-neous sector number.

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5.12.2.38 MSS_MCRC_CRC_WDTOPLD3 Register

5.12.2.38.1 MSS_MCRC_CRC_WDTOPLD3 Register (Offset = CCh) [reset = 0h]

Channel 3 timeout pre-load value to check if within a given time DMA initiates a block transfer.

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Table 5-1813. Instance Table

Instance Name	Physical Address
MCRC0	3500 00CCh

Figure 5-888. MSS_MCRC_CRC_WDTOPLD3 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
CRC_WDTOPLD3							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_WDTOPLD3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_WDTOPLD3							
R/W							
0h							

Table 5-1814. MSS_MCRC_CRC_WDTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	
23:0	CRC_WDTOPLD3	R/W	0h	Channel 3 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

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5.12.2.39 MSS_MCRC_CRC_BCTOPLD3 Register

5.12.2.39.1 MSS_MCRC_CRC_BCTOPLD3 Register (Offset = D0h) [reset = 0h]

Channel 3 timeout pre-load value to check if one block of patterns are compressed with a given time.

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Table 5-1815. Instance Table

Instance Name	Physical Address
MCRC0	3500 00D0h

Figure 5-889. MSS_MCRC_CRC_BCTOPLD3 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
CRC_BCTOPLD3							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_BCTOPLD3							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_BCTOPLD3							
R/W							
0h							

Table 5-1816. MSS_MCRC_CRC_BCTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	
23:0	CRC_BCTOPLD3	R/W	0h	Channel 3 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated.

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5.12.2.40 MSS_MCRC_PSA_SIGREGL3 Register

5.12.2.40.1 MSS_MCRC_PSA_SIGREGL3 Register (Offset = E0h) [reset = 0h]

Channel 3 PSA signature low register.

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Table 5-1817. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E0h

Figure 5-890. MSS_MCRC_PSA_SIGREGL3 Name Register

31	30	29	28	27	26	25	24
PSASIG3_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG3_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG3_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG3_31_0							
R/W							
0h							

Table 5-1818. MSS_MCRC_PSA_SIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG3_31_0	R/W	0h	Channel 3 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register.

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5.12.2.41 MSS_MCRC_PSA_SIGREGH3 Register

5.12.2.41.1 MSS_MCRC_PSA_SIGREGH3 Register (Offset = E4h) [reset = 0h]

Channel 3 PSA signature high register.

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Table 5-1819. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E4h

Figure 5-891. MSS_MCRC_PSA_SIGREGH3 Name Register

31	30	29	28	27	26	25	24
PSA_SIG3_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
PSA_SIG3_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
PSA_SIG3_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
PSA_SIG3_63_32							
R/W							
0h							

Table 5-1820. MSS_MCRC_PSA_SIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSA_SIG3_63_32	R/W	0h	Channel 3 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register.

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5.12.2.42 MSS_MCRC_CRC_REGL3 Register

5.12.2.42.1 MSS_MCRC_CRC_REGL3 Register (Offset = E8h) [reset = 0h]

Channel 3 CRC value low register.

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Table 5-1821. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E8h

Figure 5-892. MSS_MCRC_CRC_REGL3 Name Register

31	30	29	28	27	26	25	24
CRC3_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC3_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC3_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC3_31_0							
R/W							
0h							

Table 5-1822. MSS_MCRC_CRC_REGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC3_31_0	R/W	0h	Channel 3 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] register.

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5.12.2.43 MSS_MCRC_CRC_REGH3 Register

5.12.2.43.1 MSS_MCRC_CRC_REGH3 Register (Offset = ECh) [reset = 0h]

Channel 3 CRC value high register.

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Table 5-1823. Instance Table

Instance Name	Physical Address
MCRC0	3500 00ECh

Figure 5-893. MSS_MCRC_CRC_REGH3 Name Register

31	30	29	28	27	26	25	24
CRC3_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC3_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC3_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC3_63_32							
R/W							
0h							

Table 5-1824. MSS_MCRC_CRC_REGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC3_63_32	R/W	0h	Channel 3 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register.

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5.12.2.44 MSS_MCRC_PSA_SECSIGREGL3 Register

5.12.2.44.1 MSS_MCRC_PSA_SECSIGREGL3 Register (Offset = F0h) [reset = 0h]

Channel 3 PSA sector signature low regis-ter.

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Table 5-1825. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F0h

Figure 5-894. MSS_MCRC_PSA_SECSIGREGL3 Name Register

31	30	29	28	27	26	25	24
PSASECSIG3_31_0							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG3_31_0							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG3_31_0							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG3_31_0							
R							
0h							

Table 5-1826. MSS_MCRC_PSA_SECSIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG3_31_0	R	0h	Channel 3 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register.

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5.12.2.45 MSS_MCRC_PSA_SECSIGREGH3 Register

5.12.2.45.1 MSS_MCRC_PSA_SECSIGREGH3 Register (Offset = F4h) [reset = 0h]

Channel 3 PSA sector signature high regis-ter.

Return to Summary Table

Table 5-1827. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F4h

Figure 5-895. MSS_MCRC_PSA_SECSIGREGH3 Name Register

31	30	29	28	27	26	25	24
PSASECSIG3_63_32							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PSASECSIG3_63_32							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PSASECSIG3_63_32							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PSASECSIG3_63_32							
R							
0h							

Table 5-1828. MSS_MCRC_PSA_SECSIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG3_63_32	R	0h	Channel 3 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register.

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5.12.2.46 MSS_MCRC_RAW_DATAREGL3 Register

5.12.2.46.1 MSS_MCRC_RAW_DATAREGL3 Register (Offset = F8h) [reset = 0h]

Channel 3 un-compressed raw data low register.

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Table 5-1829. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F8h

Figure 5-896. MSS_MCRC_RAW_DATAREGL3 Name Register

31	30	29	28	27	26	25	24
RAW_DATA3_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA3_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA3_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA3_31_0							
R							
0h							

Table 5-1830. MSS_MCRC_RAW_DATAREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA3_31_0	R	0h	Channel 3 Raw Data Low Register. This register contains bit 31:0 of the un-compressed raw data.

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5.12.2.47 MSS_MCRC_RAW_DATAREGH3 Register

5.12.2.47.1 MSS_MCRC_RAW_DATAREGH3 Register (Offset = FCh) [reset = 0h]

Channel 3 un-compressed raw data high Register.

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Table 5-1831. Instance Table

Instance Name	Physical Address
MCRC0	3500 00FCh

Figure 5-897. MSS_MCRC_RAW_DATAREGH3 Name Register

31	30	29	28	27	26	25	24
RAW_DATA3_63_32							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RAW_DATA3_63_32							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RAW_DATA3_63_32							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAW_DATA3_63_32							
R							
0h							

Table 5-1832. MSS_MCRC_RAW_DATAREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA3_63_32	R	0h	Channel 3 Raw Data High Register. This register contains bit 63:32 of the un-compressed raw data.

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5.12.2.48 MSS_MCRC_CRC_PCOUNT_REG4 Register

5.12.2.48.1 MSS_MCRC_CRC_PCOUNT_REG4 Register (Offset = 100h) [reset = 0h]

Channel 4 preload register for the pattern count.

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Table 5-1833. Instance Table

Instance Name	Physical Address
MCRC0	3500 0100h

Figure 5-898. MSS_MCRC_CRC_PCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1				CRC_PAT_COUNT4			
R				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_PAT_COUNT4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_PAT_COUNT4							
R/W							
0h							

Table 5-1834. MSS_MCRC_CRC_PCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED1	R	0h	
19:0	CRC_PAT_COUNT4	R/W	0h	Channel 4 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed.

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5.12.2.49 MSS_MCRC_CRC_SCOUNT_REG4 Register

5.12.2.49.1 MSS_MCRC_CRC_SCOUNT_REG4 Register (Offset = 104h) [reset = 0h]

Channel 4 preload register for the sector count.

Return to Summary Table

Table 5-1835. Instance Table

Instance Name	Physical Address
MCRC0	3500 0104h

Figure 5-899. MSS_MCRC_CRC_SCOUNT_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
CRC_SEC_COUNT4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_SEC_COUNT4							
R/W							
0h							

Table 5-1836. MSS_MCRC_CRC_SCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	
15:0	CRC_SEC_COUNT4	R/W	0h	Channel 4 Sector Counter Preload Register. This register contains the number of sectors in one block of memory.

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5.12.2.50 MSS_MCRC_CRC_CURSEC_REG4 Register

5.12.2.50.1 MSS_MCRC_CRC_CURSEC_REG4 Register (Offset = 108h) [reset = 0h]

Channel 4 current sector register contains the sector number which causes CRC fail-ure.

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Table 5-1837. Instance Table

Instance Name	Physical Address
MCRC0	3500 0108h

Figure 5-900. MSS_MCRC_CRC_CURSEC_REG4 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
CRC_CURSEC4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_CURSEC4							
R/W							
0h							

Table 5-1838. MSS_MCRC_CRC_CURSEC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED1	R	0h	
15:0	CRC_CURSEC4	R/W	0h	Channel 4 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erro-neous sector number.

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5.12.2.51 MSS_MCRC_CRC_WDTOPLD4 Register

5.12.2.51.1 MSS_MCRC_CRC_WDTOPLD4 Register (Offset = 10Ch) [reset = 0h]

Channel 4 timeout pre-load value to check if within a given time DMA initiates a block transfer.

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Table 5-1839. Instance Table

Instance Name	Physical Address
MCRC0	3500 010Ch

Figure 5-901. MSS_MCRC_CRC_WDTOPLD4 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
CRC_WDTOPLD4							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC_WDTOPLD4							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC_WDTOPLD4							
R/W							
0h							

Table 5-1840. MSS_MCRC_CRC_WDTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	
23:0	CRC_WDTOPLD4	R/W	0h	Channel 4 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns.

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5.12.2.52 MSS_MCRC_CRC_BCTOPLD4 Register

5.12.2.52.1 MSS_MCRC_CRC_BCTOPLD4 Register (Offset = 110h) [reset = 0h]

Channel 4 timeout pre-load value to check if one block of patterns are compressed with a given time.

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Table 5-1841. Instance Table

Instance Name	Physical Address
MCRC0	3500 0110h

Figure 5-902. MSS_MCRC_CRC_BCTOPLD4 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CRC_BCTOPLD4							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CRC_BCTOPLD4							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CRC_BCTOPLD4							
R/W							
0h							

Table 5-1842. MSS_MCRC_CRC_BCTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED1	R	0h	
23:0	CRC_BCTOPLD4	R/W	0h	Channel 4 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated.

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5.12.2.53 MSS_MCRC_PSA_SIGREGL4 Register

5.12.2.53.1 MSS_MCRC_PSA_SIGREGL4 Register (Offset = 120h) [reset = 0h]

Channel 4 PSA signature low register.

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Table 5-1843. Instance Table

Instance Name	Physical Address
MCRC0	3500 0120h

Figure 5-903. MSS_MCRC_PSA_SIGREGL4 Name Register

31	30	29	28	27	26	25	24
PSASIG4_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
PSASIG4_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
PSASIG4_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
PSASIG4_31_0							
R/W							
0h							

Table 5-1844. MSS_MCRC_PSA_SIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASIG4_31_0	R/W	0h	Channel 4 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register.

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5.12.2.54 MSS_MCRC_PSA_SIGREGH4 Register

5.12.2.54.1 MSS_MCRC_PSA_SIGREGH4 Register (Offset = 124h) [reset = 0h]

Channel 4 PSA signature high register.

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Table 5-1845. Instance Table

Instance Name	Physical Address
MCRC0	3500 0124h

Figure 5-904. MSS_MCRC_PSA_SIGREGH4 Name Register

31	30	29	28	27	26	25	24
PSA_SIG4_63_32							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PSA_SIG4_63_32							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PSA_SIG4_63_32							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PSA_SIG4_63_32							
R/W							
0h							

Table 5-1846. MSS_MCRC_PSA_SIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSA_SIG4_63_32	R/W	0h	Channel 4 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register.

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5.12.2.55 MSS_MCRC_CRC_REGL4 Register

5.12.2.55.1 MSS_MCRC_CRC_REGL4 Register (Offset = 128h) [reset = 0h]

Channel 4 CRC value low register.

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Table 5-1847. Instance Table

Instance Name	Physical Address
MCRC0	3500 0128h

Figure 5-905. MSS_MCRC_CRC_REGL4 Name Register

31	30	29	28	27	26	25	24
CRC4_31_0							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC4_31_0							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC4_31_0							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC4_31_0							
R/W							
0h							

Table 5-1848. MSS_MCRC_CRC_REGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC4_31_0	R/W	0h	Channel 4 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] register.

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5.12.2.56 MSS_MCRC_CRC_REGH4 Register

5.12.2.56.1 MSS_MCRC_CRC_REGH4 Register (Offset = 12Ch) [reset = 0h]

Channel 4 CRC value high register.

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Table 5-1849. Instance Table

Instance Name	Physical Address
MCRC0	3500 012Ch

Figure 5-906. MSS_MCRC_CRC_REGH4 Name Register

31	30	29	28	27	26	25	24
CRC4_63_32							
R/W							
0h							
23	22	21	20	19	18	17	16
CRC4_63_32							
R/W							
0h							
15	14	13	12	11	10	9	8
CRC4_63_32							
R/W							
0h							
7	6	5	4	3	2	1	0
CRC4_63_32							
R/W							
0h							

Table 5-1850. MSS_MCRC_CRC_REGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CRC4_63_32	R/W	0h	Channel 4 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register.

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5.12.2.57 MSS_MCRC_PSA_SECSIGREGL4 Register

5.12.2.57.1 MSS_MCRC_PSA_SECSIGREGL4 Register (Offset = 130h) [reset = 0h]

Channel 4 PSA sector signature low regis-ter.

Return to Summary Table

Table 5-1851. Instance Table

Instance Name	Physical Address
MCRC0	3500 0130h

Figure 5-907. MSS_MCRC_PSA_SECSIGREGL4 Name Register

31	30	29	28	27	26	25	24
PSASECSIG4_31_0							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG4_31_0							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG4_31_0							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG4_31_0							
R							
0h							

Table 5-1852. MSS_MCRC_PSA_SECSIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG4_31_0	R	0h	Channel 4 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register.

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5.12.2.58 MSS_MCRC_PSA_SECSIGREGH4 Register

5.12.2.58.1 MSS_MCRC_PSA_SECSIGREGH4 Register (Offset = 134h) [reset = 0h]

Channel 4 PSA sector signature high regis-ter.

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Table 5-1853. Instance Table

Instance Name	Physical Address
MCRC0	3500 0134h

Figure 5-908. MSS_MCRC_PSA_SECSIGREGH4 Name Register

31	30	29	28	27	26	25	24
PSASECSIG4_63_32							
R							
0h							
23	22	21	20	19	18	17	16
PSASECSIG4_63_32							
R							
0h							
15	14	13	12	11	10	9	8
PSASECSIG4_63_32							
R							
0h							
7	6	5	4	3	2	1	0
PSASECSIG4_63_32							
R							
0h							

Table 5-1854. MSS_MCRC_PSA_SECSIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	PSASECSIG4_63_32	R	0h	Channel 4 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register.

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5.12.2.59 MSS_MCRC_RAW_DATAREGL4 Register

5.12.2.59.1 MSS_MCRC_RAW_DATAREGL4 Register (Offset = 138h) [reset = 0h]

Channel 4 un-compressed raw data low register.

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Table 5-1855. Instance Table

Instance Name	Physical Address
MCRC0	3500 0138h

Figure 5-909. MSS_MCRC_RAW_DATAREGL4 Name Register

31	30	29	28	27	26	25	24
RAW_DATA4_31_0							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA4_31_0							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA4_31_0							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA4_31_0							
R							
0h							

Table 5-1856. MSS_MCRC_RAW_DATAREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA4_31_0	R	0h	Channel 4 Raw Data Low Register. This register contains bit 31:0 of the un-compressed raw data.

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5.12.2.60 MSS_MCRC_RAW_DATAREGH4 Register

5.12.2.60.1 MSS_MCRC_RAW_DATAREGH4 Register (Offset = 13Ch) [reset = 0h]

Channel 4 un-compressed raw data high Register.

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Table 5-1857. Instance Table

Instance Name	Physical Address
MCRC0	3500 013Ch

Figure 5-910. MSS_MCRC_RAW_DATAREGH4 Name Register

31	30	29	28	27	26	25	24
RAW_DATA4_63_32							
R							
0h							
23	22	21	20	19	18	17	16
RAW_DATA4_63_32							
R							
0h							
15	14	13	12	11	10	9	8
RAW_DATA4_63_32							
R							
0h							
7	6	5	4	3	2	1	0
RAW_DATA4_63_32							
R							
0h							

Table 5-1858. MSS_MCRC_RAW_DATAREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RAW_DATA4_63_32	R	0h	Channel 4 Raw Data High Register. This register contains bit 63:32 of the un-compressed raw data.

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5.12.2.61 MSS_MCRC_MCRC_BUS_SEL Register

5.12.2.61.1 MSS_MCRC_MCRC_BUS_SEL Register (Offset = 140h) [reset = 7h]

Disables either or all tracing of data buses.

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Table 5-1859. Instance Table

Instance Name	Physical Address
MCRC0	3500 0140h

Figure 5-911. MSS_MCRC_MCRC_BUS_SEL Name Register

31	30	29	28	27	26	25	24
NU67							
R							
0h							
23	22	21	20	19	18	17	16
NU67							
R							
0h							
15	14	13	12	11	10	9	8
NU67							
R							
0h							
7	6	5	4	3	2	1	0
NU67					MEN	DTCMEN	ITCMEN
R					R/W	R/W	R/W
0h					1h	1h	1h

Table 5-1860. MSS_MCRC_MCRC_BUS_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	NU67	R	0h	Reserved
2	MEN	R/W	1h	MEn. Enable/disables the tracing of VBUSM 0:Tracing of VBUSM master bus has been disabled 1:Tracing of VBUSM master bus has been enabled
1	DTCMEN	R/W	1h	DTCMEn. Enable/disables the tracing of data TCM 0:Tracing of DTCM_ODD and DTCM_EVEN buses have been disabled 1:Tracing of DTCM_ODD and DTCM_EVEN buses have been enabled
0	ITCMEN	R/W	1h	ITCMEn. Enable/disables the tracing of instruction TCM 0:Tracing of ITCM bus has been disabled 1:Tracing of ITCM bus has been enabled

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5.13 MCSPI

MCSPI

5.13.1 MCSPI Summaries

MCSPI Summaries

Table 5-1861. MCSPI Registers, Base Address=5220 0000h, Length=1024

Offset	Length	Register Name	MCSPI0 Physical Address	MCSPI1 Physical Address	MCSPI2 Physical Address
0h	32	MCSPI_HL_REV	5220 0000h	5220 1000h	5220 2000h
4h	32	MCSPI_HL_HWINFO	5220 0004h	5220 1004h	5220 2004h
10h	32	MCSPI_HL_SYSCONFIG	5220 0010h	5220 1010h	5220 2010h
100h	32	MCSPI_REVISION	5220 0100h	5220 1100h	5220 2100h
110h	32	MCSPI_SYSCONFIG	5220 0110h	5220 1110h	5220 2110h
114h	32	MCSPI_SYSSTATUS	5220 0114h	5220 1114h	5220 2114h
118h	32	MCSPI_IRQSTATUS	5220 0118h	5220 1118h	5220 2118h
11Ch	32	MCSPI_IRQENABLE	5220 011Ch	5220 111Ch	5220 211Ch
120h	32	MCSPI_WAKEUPENABLE	5220 0120h	5220 1120h	5220 2120h
124h	32	MCSPI_SYST	5220 0124h	5220 1124h	5220 2124h
128h	32	MCSPI_MODULCTRL	5220 0128h	5220 1128h	5220 2128h
12Ch	32	MCSPI_CH0CONF	5220 012Ch	5220 112Ch	5220 212Ch
130h	32	MCSPI_CH0STAT	5220 0130h	5220 1130h	5220 2130h
134h	32	MCSPI_CH0CTRL	5220 0134h	5220 1134h	5220 2134h
138h	32	MCSPI_TX0	5220 0138h	5220 1138h	5220 2138h
13Ch	32	MCSPI_RX0	5220 013Ch	5220 113Ch	5220 213Ch
140h	32	MCSPI_CH1CONF	5220 0140h	5220 1140h	5220 2140h
144h	32	MCSPI_CH1STAT	5220 0144h	5220 1144h	5220 2144h
148h	32	MCSPI_CH1CTRL	5220 0148h	5220 1148h	5220 2148h
14Ch	32	MCSPI_TX1	5220 014Ch	5220 114Ch	5220 214Ch
150h	32	MCSPI_RX1	5220 0150h	5220 1150h	5220 2150h
154h	32	MCSPI_CH2CONF	5220 0154h	5220 1154h	5220 2154h
158h	32	MCSPI_CH2STAT	5220 0158h	5220 1158h	5220 2158h
15Ch	32	MCSPI_CH2CTRL	5220 015Ch	5220 115Ch	5220 215Ch
160h	32	MCSPI_TX2	5220 0160h	5220 1160h	5220 2160h
164h	32	MCSPI_RX2	5220 0164h	5220 1164h	5220 2164h
168h	32	MCSPI_CH3CONF	5220 0168h	5220 1168h	5220 2168h
16Ch	32	MCSPI_CH3STAT	5220 016Ch	5220 116Ch	5220 216Ch
170h	32	MCSPI_CH3CTRL	5220 0170h	5220 1170h	5220 2170h
174h	32	MCSPI_TX3	5220 0174h	5220 1174h	5220 2174h
178h	32	MCSPI_RX3	5220 0178h	5220 1178h	5220 2178h
17Ch	32	MCSPI_XFERLEVEL	5220 017Ch	5220 117Ch	5220 217Ch
180h	32	MCSPI_DAFTX	5220 0180h	5220 1180h	5220 2180h
1A0h	32	MCSPI_DAFRX	5220 01A0h	5220 11A0h	5220 21A0h

Table 5-1862. MCSPI Registers, Base Address=5220 0000h, Length=1024

Offset	Length	Register Name	MCSPI3 Physical Address	MCSPI4 Physical Address	MCSPI5 Physical Address
0h	32	MCSPI_HL_REV	5220 3000h	5220 4000h	5220 5000h

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Table 5-1862. MCSPI Registers, Base Address=5220 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCSPI3 Physical Address	MCSPI4 Physical Address	MCSPI5 Physical Address
4h	32	MCSPI_HL_HWINFO	5220 3004h	5220 4004h	5220 5004h
10h	32	MCSPI_HL_SYSCONFIG	5220 3010h	5220 4010h	5220 5010h
100h	32	MCSPI_REVISION	5220 3100h	5220 4100h	5220 5100h
110h	32	MCSPI_SYSCONFIG	5220 3110h	5220 4110h	5220 5110h
114h	32	MCSPI_SYSSTATUS	5220 3114h	5220 4114h	5220 5114h
118h	32	MCSPI_IRQSTATUS	5220 3118h	5220 4118h	5220 5118h
11Ch	32	MCSPI_IRQENABLE	5220 311Ch	5220 411Ch	5220 511Ch
120h	32	MCSPI_WAKEUPENABLE	5220 3120h	5220 4120h	5220 5120h
124h	32	MCSPI_SYST	5220 3124h	5220 4124h	5220 5124h
128h	32	MCSPI_MODULCTRL	5220 3128h	5220 4128h	5220 5128h
12Ch	32	MCSPI_CH0CONF	5220 312Ch	5220 412Ch	5220 512Ch
130h	32	MCSPI_CH0STAT	5220 3130h	5220 4130h	5220 5130h
134h	32	MCSPI_CH0CTRL	5220 3134h	5220 4134h	5220 5134h
138h	32	MCSPI_TX0	5220 3138h	5220 4138h	5220 5138h
13Ch	32	MCSPI_RX0	5220 313Ch	5220 413Ch	5220 513Ch
140h	32	MCSPI_CH1CONF	5220 3140h	5220 4140h	5220 5140h
144h	32	MCSPI_CH1STAT	5220 3144h	5220 4144h	5220 5144h
148h	32	MCSPI_CH1CTRL	5220 3148h	5220 4148h	5220 5148h
14Ch	32	MCSPI_TX1	5220 314Ch	5220 414Ch	5220 514Ch
150h	32	MCSPI_RX1	5220 3150h	5220 4150h	5220 5150h
154h	32	MCSPI_CH2CONF	5220 3154h	5220 4154h	5220 5154h
158h	32	MCSPI_CH2STAT	5220 3158h	5220 4158h	5220 5158h
15Ch	32	MCSPI_CH2CTRL	5220 315Ch	5220 415Ch	5220 515Ch
160h	32	MCSPI_TX2	5220 3160h	5220 4160h	5220 5160h
164h	32	MCSPI_RX2	5220 3164h	5220 4164h	5220 5164h
168h	32	MCSPI_CH3CONF	5220 3168h	5220 4168h	5220 5168h
16Ch	32	MCSPI_CH3STAT	5220 316Ch	5220 416Ch	5220 516Ch
170h	32	MCSPI_CH3CTRL	5220 3170h	5220 4170h	5220 5170h
174h	32	MCSPI_TX3	5220 3174h	5220 4174h	5220 5174h
178h	32	MCSPI_RX3	5220 3178h	5220 4178h	5220 5178h
17Ch	32	MCSPI_XFERLEVEL	5220 317Ch	5220 417Ch	5220 517Ch
180h	32	MCSPI_DAFTX	5220 3180h	5220 4180h	5220 5180h
1A0h	32	MCSPI_DAFRX	5220 31A0h	5220 41A0h	5220 51A0h

Table 5-1863. MCSPI Registers, Base Address=5220 0000h, Length=1024

Offset	Length	Register Name	MCSPI6 Physical Address	MCSPI7 Physical Address
0h	32	MCSPI_HL_REV	5220 6000h	5220 7000h
4h	32	MCSPI_HL_HWINFO	5220 6004h	5220 7004h
10h	32	MCSPI_HL_SYSCONFIG	5220 6010h	5220 7010h
100h	32	MCSPI_REVISION	5220 6100h	5220 7100h
110h	32	MCSPI_SYSCONFIG	5220 6110h	5220 7110h
114h	32	MCSPI_SYSSTATUS	5220 6114h	5220 7114h
118h	32	MCSPI_IRQSTATUS	5220 6118h	5220 7118h
11Ch	32	MCSPI_IRQENABLE	5220 611Ch	5220 711Ch
120h	32	MCSPI_WAKEUPENABLE	5220 6120h	5220 7120h
124h	32	MCSPI_SYST	5220 6124h	5220 7124h

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Table 5-1863. MCSPI Registers, Base Address=5220 0000h, Length=1024 (continued)

Offset	Length	Register Name	MCSPI6 Physical Address	MCSPI7 Physical Address
128h	32	MCSPI_MODULCTRL	5220 6128h	5220 7128h
12Ch	32	MCSPI_CH0CONF	5220 612Ch	5220 712Ch
130h	32	MCSPI_CH0STAT	5220 6130h	5220 7130h
134h	32	MCSPI_CH0CTRL	5220 6134h	5220 7134h
138h	32	MCSPI_TX0	5220 6138h	5220 7138h
13Ch	32	MCSPI_RX0	5220 613Ch	5220 713Ch
140h	32	MCSPI_CH1CONF	5220 6140h	5220 7140h
144h	32	MCSPI_CH1STAT	5220 6144h	5220 7144h
148h	32	MCSPI_CH1CTRL	5220 6148h	5220 7148h
14Ch	32	MCSPI_TX1	5220 614Ch	5220 714Ch
150h	32	MCSPI_RX1	5220 6150h	5220 7150h
154h	32	MCSPI_CH2CONF	5220 6154h	5220 7154h
158h	32	MCSPI_CH2STAT	5220 6158h	5220 7158h
15Ch	32	MCSPI_CH2CTRL	5220 615Ch	5220 715Ch
160h	32	MCSPI_TX2	5220 6160h	5220 7160h
164h	32	MCSPI_RX2	5220 6164h	5220 7164h
168h	32	MCSPI_CH3CONF	5220 6168h	5220 7168h
16Ch	32	MCSPI_CH3STAT	5220 616Ch	5220 716Ch
170h	32	MCSPI_CH3CTRL	5220 6170h	5220 7170h
174h	32	MCSPI_TX3	5220 6174h	5220 7174h
178h	32	MCSPI_RX3	5220 6178h	5220 7178h
17Ch	32	MCSPI_XFERLEVEL	5220 617Ch	5220 717Ch
180h	32	MCSPI_DAFTX	5220 6180h	5220 7180h
1A0h	32	MCSPI_DAFRX	5220 61A0h	5220 71A0h

5.13.2 MCSPI Registers

MCSPI Registers

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5.13.2.1 MCSPI_HL_REV Register

5.13.2.1.1 MCSPI_HL_REV Register (Offset = 0h) [reset = 40301A0Bh]

IP Revision Identifier (X.Y.R)
Used by software to track features, bugs, and compatibility.

Return to Summary Table

Table 5-1864. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0000h
MCSPI1	5220 1000h
MCSPI2	5220 2000h
MCSPI3	5220 3000h
MCSPI4	5220 4000h
MCSPI5	5220 5000h
MCSPI6	5220 6000h
MCSPI7	5220 7000h

Figure 5-912. MCSPI_HL_REV Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="2">SCHEME</td><td colspan="2">RSVD</td><td colspan="4">FUNC</td></tr>
<tr><td colspan="2">R</td><td colspan="2">R</td><td colspan="4">R</td></tr>
<tr><td colspan="2">1h</td><td colspan="2">0h</td><td colspan="4">30h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">FUNC</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">30h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">R_RTL</td><td colspan="3">X_MAJOR</td></tr>
<tr><td colspan="5">R</td><td colspan="3">R</td></tr>
<tr><td colspan="5">3h</td><td colspan="3">2h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CUSTOM</td><td colspan="6">Y_MINOR</td></tr>
<tr><td colspan="2">R</td><td colspan="6">R</td></tr>
<tr><td colspan="2">0h</td><td colspan="6">Bh</td></tr>
</table>

Table 5-1865. MCSPI_HL_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish between old scheme and current
29:28	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
27:16	FUNC	R	30h	Function indicates a software compatible module family If there is no level of software compatibility a new Func number [and hence REVISION] should be assigned
15:11	R_RTL	R	3h	RTL Version [R], maintained by IP design owner RTL follows a numbering such as XYRZ which are explained in this table R changes ONLY when: [1] PDS uploads occur which may have been due to spec changes [2] Bug fixes occur [3] Resets to '0' when X or Y changes Design team has an internal 'Z' [customer invisible] number which increments on every drop that happens due to DV and RTL updates Z resets to 0 when R increments

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Table 5-1865. MCSPI_HL_REV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10:8	X_MAJOR	R	2h	Major Revision [X], maintained by IP specification owner X changes ONLY when: [1] There is a major feature addition An example would be adding Master Mode to Utopia Level2 The Func field [or Class/ Type in old PID format] will remain the same X does NOT change due to: [1] Bug fixes [2] Change in feature parameters
7:6	CUSTOM	R	0h	Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers
5:0	Y_MINOR	R	Bh	Minor Revision [Y], maintained by IP specification owner Y changes ONLY when: [1] Features are scaled [up or down] Flexibility exists in that this feature scalability may either be represented in the Y change or a specific register in the IP that indicates which features are exactly available [2] When feature creeps from Is-Not list to Is list But this may not be the case once it sees silicon; in which case X will change Y does NOT change due to: [1] Bug fixes [2] Typos or clarifications [3] major functional/feature change/addition/ deletion Instead these changes may be reflected via R, S, X as applicable Spec owner maintains a customer-invisible number 'S' which changes due to: [1] Typos/clarifications [2] Bug documentation Note that this bug is not due to a spec change but due to implementation Nevertheless, the spec tracks the IP bugs An RTL release [say for silicon PG11] that occurs due to bug fix should document the corresponding spec number [XYS] in its release notes

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5.13.2.2 MCSPI_HL_HWINFO Register

5.13.2.2.1 MCSPI_HL_HWINFO Register (Offset = 4h) [reset = 9h]

Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.

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Table 5-1866. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0004h
MCSPI1	5220 1004h
MCSPI2	5220 2004h
MCSPI3	5220 3004h
MCSPI4	5220 4004h
MCSPI5	5220 5004h
MCSPI6	5220 6004h
MCSPI7	5220 7004h

Figure 5-913. MCSPI_HL_HWINFO Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD	RETMODE	FFNBYTE					USEFIFO
R	R	R					R
0h	0h	4h					1h

Table 5-1867. MCSPI_HL_HWINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
6	RETMODE	R	0h	This bit field indicates whether the retention mode is supported using the pin PIRFFRET `0 Retention mode disabled` `1 Retention mode enabled`
5:1	FFNBYTE	R	4h	FIFO number of byte generic parameter This register defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account `1 FIFO 16 bytes depth` `2 FIFO 32 bytes depth` `4 FIFO 64 bytes depth` `8 FIFO 128 bytes depth` `10 FIFO 256 bytes depth`

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Table 5-1867. MCSPI_HL_HWINFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	USEFIFO	R	1h	Use of a FIFO enable: This bit field indicates if a FIFO is integrated within controller design with its management 0 FIFO not implemented in design 1 FIFO and its management implemented in design with depth defined by FFNBYTE generic

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5.13.2.3 MCSPI_HL_SYSCONFIG Register

5.13.2.3.1 MCSPI_HL_SYSCONFIG Register (Offset = 10h) [reset = 8h]

Clock management configuration.

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Table 5-1868. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0010h
MCSPI1	5220 1010h
MCSPI2	5220 2010h
MCSPI3	5220 3010h
MCSPI4	5220 4010h
MCSPI5	5220 5010h
MCSPI6	5220 6010h
MCSPI7	5220 7010h

Figure 5-914. MCSPI_HL_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RSVD							
R							
0h							
23	22	21	20	19	18	17	16
RSVD							
R							
0h							
15	14	13	12	11	10	9	8
RSVD							
R							
0h							
7	6	5	4	3	2	1	0
RSVD				IDLEMODE		FREEEMU	SOFTRESET
R				R/W		R/W	R/W
0h				2h		0h	0h

Table 5-1869. MCSPI_HL_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RSVD	R	0h	Reserved
3:2	IDLEMODE	R/W	2h	Configuration of the local target state management mode By definition, target can handle read/write transaction as long as it is out of IDLE state 0 `Force-idle mode: local target's IDLE state follows (acknowledges) the system's clock stop requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only.` 1 `No-idle mode: local target never enters IDLE state. Backup mode, for debug only.` 2 `Smart-idle mode: local target's IDLE state eventually follows (acknowledges) the system's clock stop requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events.`

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Table 5-1869. MCSPI_HL_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	FREEEMU	R/W	0h	Sensitivity to emulation [debug] suspend input signal 0 IP module is sensitive to emulation suspend. 1 IP module is not sensitive to emulation suspend.
0	SOFTRESET	R/W	0h	Software reset [Optional] 0 Read 0 - Reset done, no pending action 0 Write 0 - No Action 1 Read 1 - Reset(software or other) ongoing 1 Write 1 - Initiate software reset

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5.13.2.4 MCSPI_REVISION Register

5.13.2.4.1 MCSPI_REVISION Register (Offset = 100h) [reset = 2Bh]

This register contains the hard coded RTL revision number.

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Table 5-1870. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0100h
MCSPI1	5220 1100h
MCSPI2	5220 2100h
MCSPI3	5220 3100h
MCSPI4	5220 4100h
MCSPI5	5220 5100h
MCSPI6	5220 6100h
MCSPI7	5220 7100h

Figure 5-915. MCSPI_REVISION Name Register

31	30	29	28	27	26	25	24
RESERVED_13							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_13							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_13							
R							
0h							
7	6	5	4	3	2	1	0
REV							
R							
2Bh							

Table 5-1871. MCSPI_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_13	R	0h	Reads returns 0
7:0	REV	R	2Bh	IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 10, 0x21 for 21

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5.13.2.5 MCSPI_SYSCONFIG Register

5.13.2.5.1 MCSPI_SYSCONFIG Register (Offset = 110h) [reset = 15h]

This register allows controlling various parameters of the OCP interface.

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Table 5-1872. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0110h
MCSPI1	5220 1110h
MCSPI2	5220 2110h
MCSPI3	5220 3110h
MCSPI4	5220 4110h
MCSPI5	5220 5110h
MCSPI6	5220 6110h
MCSPI7	5220 7110h

Figure 5-916. MCSPI_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED_14							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_14							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_14						CLOCKACTIVITY	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
RESERVED_15			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R			R/W		R/W	R/W	R/W
0h			2h		1h	0h	1h

Table 5-1873. MCSPI_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED_14	R	0h	Reads returns 0
9:8	CLOCKACTIVITY	R/W	0h	Clocks activity during wake up mode period 0 Interface and functional clocks may be switched off. 1 Interface clock is maintained. Functional clock may be switched off. 2 Functional clock is maintained. Interface clock may be switched off. 3 Interface and functional clocks are maintained.
7:5	RESERVED_15	R	0h	Reads returns 0

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Table 5-1873. MCSPI_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	SIDLEMODE	R/W	2h	Power management 0 If an IDLE request is detected, the MCSPI acknowledges it unconditionally and goes in inactive mode. Interrupt, DMA requests and wake-up lines are unconditionally deasserted and the module wake-up capability is deactivated even if the MCSPI_SYSCONFIG[2] ENAWAKEUP bit is set. 1 If an IDLE request is detected, the request is ignored and the module does not switch to wake-up mode, and keeps on behaving normally. 2 If an IDLE request is detected, the module will switch to wake-up mode based on its internal activity, and the wake-up capability can be used if the bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set. 3 Reserved - do not use.
2	ENAWAKEUP	R/W	1h	WakeUp feature control 0 Wake-up capability is disabled. 1 Wake-up capability is enabled.
1	SOFTRESET	R/W	0h	Software reset During reads it always returns 0 0 (write) Normal mode 1 (write) Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware.
0	AUTOIDLE	R/W	1h	Internal OCP Clock gating strategy 0 Interface clock is free-running. 1 Automatic interface clock gating strategy is applied, based on the configuration interface activity.

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5.13.2.6 MCSPI_SYSSTATUS Register

5.13.2.6.1 MCSPI_SYSSTATUS Register (Offset = 114h) [reset = 1h]

This register provides status information about the module excluding the interrupt status information .

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Table 5-1874. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0114h
MCSPI1	5220 1114h
MCSPI2	5220 2114h
MCSPI3	5220 3114h
MCSPI4	5220 4114h
MCSPI5	5220 5114h
MCSPI6	5220 6114h
MCSPI7	5220 7114h

Figure 5-917. MCSPI_SYSSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_16							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_16							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_16							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_16							RESETDONE
R							R
0h							1h

Table 5-1875. MCSPI_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_16	R	0h	Reserved for module specific status information Read returns 0
0	RESETDONE	R	1h	Internal Reset Monitoring `0 Internal module reset is ongoing` `1 Reset completed`

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5.13.2.7 MCSPI_IRQSTATUS Register

5.13.2.7.1 MCSPI_IRQSTATUS Register (Offset = 118h) [reset = 0h]

The interrupt status regroups all the status of the module internal events that can generate an interrupt .

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Table 5-1876. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0118h
MCSPI1	5220 1118h
MCSPI2	5220 2118h
MCSPI3	5220 3118h
MCSPI4	5220 4118h
MCSPI5	5220 5118h
MCSPI6	5220 6118h
MCSPI7	5220 7118h

Figure 5-918. MCSPI_IRQSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED_8							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_8						EOW	WKS
R						R/W1TS	R/W1TS
0h						0h	0h
15	14	13	12	11	10	9	8
RESERVED_7	RX3_FULL	TX3_UNDERFLOW	TX3_EMPTY	RESERVED_9	RX2_FULL	TX2_UNDERFLOW	TX2_EMPTY
R	R/W1TS	R/W1TS	R/W1TS	R	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED_10	RX1_FULL	TX1_UNDERFLOW	TX1_EMPTY	RX0_OVERFLOW	RX0_FULL	TX0_UNDERFLOW	TX0_EMPTY
R	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1877. MCSPI_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_8	R	0h	Reads returns 0
17	EOW	R/W1TS	0h	End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of SPI word defined by MCSPI_XFERLEVEL[WCNT] 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
16	WKS	R/W1TS	0h	Wake Up event in target mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset

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Table 5-1877. MCSPI_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RESERVED_7	R	0h	Reads returns 0
14	RX3_FULL	R/W1TS	0h	Receiver register is full or almost full Only when Channel 3 is enabled 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
13	TX3_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Only when Channel 3 is enabled The transmitter register is empty [not updated by Host or DMA with new data] before its time slot assignment Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
12	TX3_EMPTY	R/W1TS	0h	Transmitter register is empty or almost empty Note: Enabling the channel automatically rises this event 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
11	RESERVED_9	R	0h	Reads returns 0
10	RX2_FULL	R/W1TS	0h	Receiver register full or almost full Channel 2 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
9	TX2_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 2 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
8	TX2_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 2 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
7	RESERVED_10	R	0h	Reads returns 0
6	RX1_FULL	R/W1TS	0h	Receiver register full or almost full Channel 1 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
5	TX1_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 1 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
4	TX1_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 1 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
3	RX0_OVERFLOW	R/W1TS	0h	Receiver register overflow [target mode only] Channel 0 0 Event status bit unchanged 1 Event is pending

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Table 5-1877. MCSPI_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RX0_FULL	R/W1TS	0h	Receiver register full or almost full Channel 0 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
1	TX0_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 0 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset
0	TX0_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 0 0 Read 0 - Event false 0 Write 0 - Event status bit Unchanged 1 Read 1 - Event is Pending 1 Write 1 - Event status bit is reset

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5.13.2.8 MCSPI_IRQENABLE Register

5.13.2.8.1 MCSPI_IRQENABLE Register (Offset = 11Ch) [reset = 0h]

This register allows to enable/disable the module internal sources of interrupt, on an event-by-event basis.

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Table 5-1878. Instance Table

Instance Name	Physical Address
MCSPI0	5220 011Ch
MCSPI1	5220 111Ch
MCSPI2	5220 211Ch
MCSPI3	5220 311Ch
MCSPI4	5220 411Ch
MCSPI5	5220 511Ch
MCSPI6	5220 611Ch
MCSPI7	5220 711Ch

Figure 5-919. MCSPI_IRQENABLE Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED_5</td></tr>
<tr><td colspan="8">R</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="6">RESERVED_5</td><td>EOW_ENABLE</td><td>WKE</td></tr>
<tr><td colspan="6">R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED_4</td><td>RX3_FULL_ENABLE</td><td>TX3_UNDERFLOW_ENABLE</td><td>TX3_EMPTY_ENABLE</td><td>RESERVED_6</td><td>RX2_FULL_ENABLE</td><td>TX2_UNDERFLOW_ENABLE</td><td>TX2_EMPTY_ENABLE</td></tr>
<tr><td>R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED_3</td><td>RX1_FULL_ENABLE</td><td>TX1_UNDERFLOW_ENABLE</td><td>TX1_EMPTY_ENABLE</td><td>RX0_OVERFLOW_ENABLE</td><td>RX0_FULL_ENABLE</td><td>TX0_UNDERFLOW_ENABLE</td><td>TX0_EMPTY_ENABLE</td></tr>
<tr><td>R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-1879. MCSPI_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:18	RESERVED_5	R	0h	Reads return 0
17	EOW_ENABLE	R/W	0h	End of Word count Interrupt Enable 0 Interrupt disabled 1 Interrupt enabled
16	WKE	R/W	0h	Wake Up event interrupt Enable in target mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] 0 Interrupt disabled 1 Interrupt enabled
15	RESERVED_4	R	0h	Reads returns 0
14	RX3_FULL_ENABLE	R/W	0h	Receiver register full or almost full Interrupt Enable Ch 3 0 Interrupt disabled 1 Interrupt enabled

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Table 5-1879. MCSPI_IRQENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TX3_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 3 0 Interrupt disabled 1 Interrupt enabled
12	TX3_EMPTY_ENABLE	R/W	0h	Transmitter register empty or almost empty Interrupt Enable Ch3 0 Interrupt disabled 1 Interrupt enabled
11	RESERVED_6	R	0h	Reads return 0
10	RX2_FULL_ENABLE	R/W	0h	Receiver register full or almost full Interrupt Enable Ch 2 0 Interrupt disabled 1 Interrupt enabled
9	TX2_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 2 0 Interrupt disabled 1 Interrupt enabled
8	TX2_EMPTY_ENABLE	R/W	0h	Transmitter register empty or almost empty Interrupt Enable Ch 2 0 Interrupt disabled 1 Interrupt enabled
7	RESERVED_3	R	0h	Reads return 0
6	RX1_FULL_ENABLE	R/W	0h	Receiver register full or almost full Interrupt Enable Ch 1 0 Interrupt disabled 1 Interrupt enabled
5	TX1_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 1 0 Interrupt disabled 1 Interrupt enabled
4	TX1_EMPTY_ENABLE	R/W	0h	Transmitter register empty or almost empty Interrupt Enable Ch 1 0 Interrupt disabled 1 Interrupt enabled
3	RX0_OVERFLOW_ENABLE	R/W	0h	Receiver register Overflow Interrupt Enable Ch 0 0 Interrupt disabled 1 Interrupt enabled
2	RX0_FULL_ENABLE	R/W	0h	Receiver register full or almost full Interrupt Enable Ch 0 0 Interrupt disabled 1 Interrupt enabled
1	TX0_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 0 0 Interrupt disabled 1 Interrupt enabled
0	TX0_EMPTY_ENABLE	R/W	0h	Transmitter register empty or almost empty Interrupt Enable Ch 0 0 Interrupt disabled 1 Interrupt enabled

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5.13.2.9 MCSPI_WAKEUPENABLE Register

5.13.2.9.1 MCSPI_WAKEUPENABLE Register (Offset = 120h) [reset = 0h]

The wakeup enable register allows to enable/disable the module internal sources of wakeup on event-by-event basis.

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Table 5-1880. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0120h
MCSPI1	5220 1120h
MCSPI2	5220 2120h
MCSPI3	5220 3120h
MCSPI4	5220 4120h
MCSPI5	5220 5120h
MCSPI6	5220 6120h
MCSPI7	5220 7120h

Figure 5-920. MCSPI_WAKEUPENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED_18							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_18							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_18							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_18							WKEN
R							R/W
0h							0h

Table 5-1881. MCSPI_WAKEUPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED_18	R	0h	Reads returns 0
0	WKEN	R/W	0h	WakeUp functionality in target mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV] 0 The event is not allowed to wake-up the system, even if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUPis set. 1 The event is allowed to wake-up the system if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set.

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5.13.2.10 MCSPI_SYST Register

5.13.2.10.1 MCSPI_SYST Register (Offset = 124h) [reset = 0h]

This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device IO pads, when the module is configured in system test (SYSTEST) mode.

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Table 5-1882. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0124h
MCSPI1	5220 1124h
MCSPI2	5220 2124h
MCSPI3	5220 3124h
MCSPI4	5220 4124h
MCSPI5	5220 5124h
MCSPI6	5220 6124h
MCSPI7	5220 7124h

Figure 5-921. MCSPI_SYST Name Register

31	30	29	28	27	26	25	24
RESERVED_17							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_17							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_17				SSB	SPIENDIR	SPIDATDIR1	SPIDATDIR0
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
WAKD	SPICLK	SPIDAT_1	SPIDAT_0	SPIEN_3	SPIEN_2	SPIEN_1	SPIEN_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1883. MCSPI_SYST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED_17	R	0h	Reads returns 0
11	SSB	R/W	0h	Set status bit 0 No action. Writing 0 does not clear already set status bits. This bit must be cleared before trying to clear a status bit of the MCSPI_IRQSTATUS register. 1 Force to 1 all status bits of MCSPI_IRQSTATUS register. Writing 1 into this bit sets to 1 all status bits in the MCSPI_IRQSTATUS register.
10	SPIENDIR	R/W	0h	Set the direction of the SPIEN[3:0] lines and SPICLK line 0 Output (as in controller mode) 1 Input (as in peripheral mode)

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Table 5-1883. MCSPI_SYST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SPIDATDIR1	R/W	0h	Set the direction of the SPIDAT[1] 0 Output 1 Input
8	SPIDATDIR0	R/W	0h	Set the direction of the SPIDAT[0] 0 Output 1 Input
7	WAKD	R/W	0h	SWAKEUP output [signal data value of internal signal to system] The signal is driven high or low according to the value written into this register bit 0 The pin is driven low. 1 The pin is driven high.
6	SPICLK	R/W	0h	SPICLK line [signal data value] If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the CLKSPI line [high or low], and a write into this bit has no effect If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the CLKSPI line is driven high or low according to the value written into this register
5	SPIDAT_1	R/W	0h	SPIDAT[1] line [signal data value] If MCSPI_SYST[SPIDATDIR1] = 0 [output mode direction], the SPIDAT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR1] = 1 [input mode direction], this bit returns the value on the SPIDAT[1] line [high or low], and a write into this bit has no effect
4	SPIDAT_0	R/W	0h	SPIDAT[0] line [signal data value] If MCSPI_SYST[SPIDATDIR0] = 0 [output mode direction], the SPIDAT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR0] = 1 [input mode direction], this bit returns the value on the SPIDAT[0] line [high or low], and a write into this bit has no effect
3	SPIEN_3	R/W	0h	SPIEN[3] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[3] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[3] line [high or low], and a write into this bit has no effect
2	SPIEN_2	R/W	0h	SPIEN[2] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[2] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[2] line [high or low], and a write into this bit has no effect
1	SPIEN_1	R/W	0h	SPIEN[1] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[1] line [high or low], and a write into this bit has no effect
0	SPIEN_0	R/W	0h	SPIEN[0] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[0] line [high or low], and a write into this bit has no effect

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5.13.2.11 MCSPI_MODULCTRL Register

5.13.2.11.1 MCSPI_MODULCTRL Register (Offset = 128h) [reset = 4h]

This register is dedicated to the configuration of the serial port interface.

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Table 5-1884. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0128h
MCSPI1	5220 1128h
MCSPI2	5220 2128h
MCSPI3	5220 3128h
MCSPI4	5220 4128h
MCSPI5	5220 5128h
MCSPI6	5220 6128h
MCSPI7	5220 7128h

Figure 5-922. MCSPI_MODULCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_11							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_11							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_11							FDAA
R							R/W
0h							0h
7	6	5	4	3	2	1	0
MOA	INITDLY			SYSTEM_TEST	MS	PIN34	SINGLE
R/W	R/W			R/W	R/W	R/W	R/W
0h	0h			0h	1h	0h	0h

Table 5-1885. MCSPI_MODULCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED_11	R	0h	Reads returns 0
8	FDAA	R/W	0h	FIFO DMA Address 256-bit aligned This register is used when a FIFO is managed by the module and DMA connected to the controller provides only 256 bit aligned address If this bit is set the enabled channel which uses the FIFO has its datas managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX[i] and MCSPI_RX[i] registers 0 `FIFO data managed by MCSPI_TX(i) and MCSPI_RX(i) registers.` 1 `FIFO data managed by MCSPI_DAFTX and MCSPI_DAFRX registers.`

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Table 5-1885. MCSPI_MODULCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	MOA	R/W	0h	Multiple word ocp access: This register can only be used when a channel is enabled using a FIFO It allows the system to perform multiple SPI word access for a single 32-bit OCP word access This is possible for WL < 16 0 Multiple word access disabled 1 Multiple word access enabled with FIFO
6:4	INITDLY	R/W	0h	Initial spi delay for first transfer: This register is an option only available in SINGLE master mode, The controller waits for a delay to transmit the first spi word after channel enabled and corresponding TX register filled This Delay is based on SPI output frequency clock, No clock output provided to the boundary and chip select is not active in 4 pin mode within this period 0 No delay for first MCSPI transfer. 1 The controller wait 4 MCSPI bus clock 2 The controller wait 8 MCSPI bus clock 3 The controller wait 16 MCSPI bus clock 4 The controller wait 32 MCSPI bus clock
3	SYSTEM_TEST	R/W	0h	Enables the system test mode 0 Functional mode 1 System test mode (SYSTEST)
2	MS	R/W	1h	Master/ Target 0 Controller - The module generates the SPICLK and SPIEN[3:0]. 1 Peripheral - The module receives the SPICLK and SPIEN[3:0].
1	PIN34	R/W	0h	Pin mode selection: This register is used to configure the SPI pin mode, in master or target mode If asserted the controller only use SIMO,SOMI and SPICLK clock pin for spi transfers 0 SPIEN is used as a chip-select. 1 SPIEN is not used. In this mode all related options to chip-select have no meaning.
0	SINGLE	R/W	0h	Single channel / Multi Channel [master mode only] 0 More than one channel will be used in controller mode. 1 Only one channel will be used in controller mode. This bit must be set in Force SPIEN[i] mode.

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5.13.2.12 MCSPI_CH0CONF Register

5.13.2.12.1 MCSPI_CH0CONF Register (Offset = 12Ch) [reset = 60000h]

This register is dedicated to the configuration of the channel 0

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Table 5-1886. Instance Table

Instance Name	Physical Address
MCSPI0	5220 012Ch
MCSPI1	5220 112Ch
MCSPI2	5220 212Ch
MCSPI3	5220 312Ch
MCSPI4	5220 412Ch
MCSPI5	5220 512Ch
MCSPI6	5220 612Ch
MCSPI7	5220 712Ch

Figure 5-923. MCSPI_CH0CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS0		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
R/W	R/W		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 5-1887. MCSPI_CH0CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	Read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.

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Table 5-1887. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.
26:25	TCS0	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	SPIENSLV	R/W	0h	Channel 0 only and target mode only: SPI target select signal detection Reserved bits for other cases 0 Detection enabled only on SPIEN[0] 1 Detection enabled only on SPIEN[1] 2 Detection enabled only on SPIEN[2] 3 Detection enabled only on SPIEN[3]
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0[6] EPOL=0, and drives it high when MCSPI_CHCONF_0[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0[6] EPOL=0, and drives it low when MCSPI_CHCONF_0[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])

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Table 5-1887. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 `DMA read request disabled` 1 `DMA read request enabled`
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 `DMA write request disabled` 1 `DMA write request enabled`
13:12	TRM	R/W	0h	Transmit/Receive modes 0 `Transmit-and-receive mode` 1 `Receive-only mode` 2 `Transmit-only mode` 3 `Reserved`

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Table 5-1887. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:7	WL	R/W	0h	SPI word length 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: The SPI word is 4-bits long 0x4: The SPI word is 5-bits long 0x5: The SPI word is 6-bits long 0x6: The SPI word is 7-bits long 0x7: The SPI word is 8-bits long 0x8: The SPI word is 9-bits long 0x9: The SPI word is 10-bits long 0xA: The SPI word is 11-bits long 0xB: The SPI word is 12-bits long 0xC: The SPI word is 13-bits long 0xD: The SPI word is 14-bits long 0xE: The SPI word is 15-bits long 0xF: The SPI word is 16-bits long 0x10: The SPI word is 17-bits long 0x11: The SPI word is 18-bits long 0x12: The SPI word is 19-bits long 0x13: The SPI word is 20-bits long 0x14: The SPI word is 21-bits long 0x15: The SPI word is 22-bits long 0x16: The SPI word is 23-bits long 0x17: The SPI word is 24-bits long 0x18: The SPI word is 25-bits long 0x19: The SPI word is 26-bits long 0x1A: The SPI word is 27-bits long 0x1B: The SPI word is 28-bits long 0x1C: The SPI word is 29-bits long 0x1D: The SPI word is 30-bits long 0x1E: The SPI word is 31-bits long 0x1F: The SPI word is 32-bits long 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long

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Table 5-1887. MCSPI_CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0. 0x0: 1 0x1: 2 0x2: 4 0x3: 8 0x4: 16 0x5: 32 0x6: 64 0x7: 128 0x8: 256 0x9: 512 0xA: 1024 0xB: 2048 0xC: 4096 0xD: 8192 0xE: 16384 0xF: 32768 0 1 1 2 2 4 3 8 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

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5.13.2.13 MCSPI_CH0STAT Register

5.13.2.13.1 MCSPI_CH0STAT Register (Offset = 130h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 0

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Table 5-1888. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0130h
MCSPI1	5220 1130h
MCSPI2	5220 2130h
MCSPI3	5220 3130h
MCSPI4	5220 4130h
MCSPI5	5220 5130h
MCSPI6	5220 6130h
MCSPI7	5220 7130h

Figure 5-924. MCSPI_CH0STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1889. MCSPI_CH0STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel 0 FIFO Receive Buffer Full Status 0 FIFO receive buffer is not full 1 FIFO receive buffer is full
5	RXFFE	R	0h	Channel 0 FIFO Receive Buffer Empty Status 0 FIFO receive buffer is not empty 1 FIFO receive buffer is empty
4	TXFFF	R	0h	Channel 0 FIFO Transmit Buffer Full Status 0 FIFO transmit buffer is not full 1 FIFO transmit buffer is full
3	TXFFE	R	0h	Channel 0 FIFO Transmit Buffer Empty Status 0 FIFO transmit buffer is not empty 1 FIFO transmit buffer is empty

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Table 5-1889. MCSPI_CH0STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel 0 End of transfer Status The definitions of beginning and end of transfer vary with master versus target and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1 This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel 0 Transmitter Register Status 0 Register is full. 1 Register is empty.
0	RXS	R	0h	Channel 0 Receiver Register Status 0 Register is empty. 1 Register is full.

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5.13.2.14 MCSPI_CH0CTRL Register

5.13.2.14.1 MCSPI_CH0CTRL Register (Offset = 134h) [reset = 0h]

This register is dedicated to enable the channel 0

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Table 5-1890. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0134h
MCSPI1	5220 1134h
MCSPI2	5220 2134h
MCSPI3	5220 3134h
MCSPI4	5220 4134h
MCSPI5	5220 5134h
MCSPI6	5220 6134h
MCSPI7	5220 7134h

Figure 5-925. MCSPI_CH0CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
EXTCLK							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							EN
R							R/W
0h							0h

Table 5-1891. MCSPI_CH0CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096clock divider ratio. 0x0: Clock ratio is CLKD + 1 0x1: Clock ratio is CLKD + 1 + 16 0xFF: Clock ratio is CLKD + 1 + 4080 `0      Clock ratio is CLKD + 1.` `1      Clock ratio is CLKD + 1 + 16.` `FF     Clock ratio is CLKD + 1 + 4080.`
7:1	RESERVED_1	R	0h	Read returns 0

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Table 5-1891. MCSPI_CH0CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

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5.13.2.15 MCSPI_TX0 Register

5.13.2.15.1 MCSPI_TX0 Register (Offset = 138h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 5-1892. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0138h
MCSPI1	5220 1138h
MCSPI2	5220 2138h
MCSPI3	5220 3138h
MCSPI4	5220 4138h
MCSPI5	5220 5138h
MCSPI6	5220 6138h
MCSPI7	5220 7138h

Figure 5-926. MCSPI_TX0 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 5-1893. MCSPI_TX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 0 Data to transmit

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5.13.2.16 MCSPI_RX0 Register

5.13.2.16.1 MCSPI_RX0 Register (Offset = 13Ch) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 5-1894. Instance Table

Instance Name	Physical Address
MCSPI0	5220 013Ch
MCSPI1	5220 113Ch
MCSPI2	5220 213Ch
MCSPI3	5220 313Ch
MCSPI4	5220 413Ch
MCSPI5	5220 513Ch
MCSPI6	5220 613Ch
MCSPI7	5220 713Ch

Figure 5-927. MCSPI_RX0 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 5-1895. MCSPI_RX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 0 Received Data

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5.13.2.17 MCSPI_CH1CONF Register

5.13.2.17.1 MCSPI_CH1CONF Register (Offset = 140h) [reset = 60000h]

This register is dedicated to the configuration of the channel 1

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Table 5-1896. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0140h
MCSPI1	5220 1140h
MCSPI2	5220 2140h
MCSPI3	5220 3140h
MCSPI4	5220 4140h
MCSPI5	5220 5140h
MCSPI6	5220 6140h
MCSPI7	5220 7140h

Figure 5-928. MCSPI_CH1CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS1		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 5-1897. MCSPI_CH1CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	Read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.

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Table 5-1897. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.
26:25	TCS1	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	RESERVED_1	R	0h	Read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_1[6] EPOL=0, and drives it high when MCSPI_CHCONF_1[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_1[6] EPOL=0, and drives it low when MCSPI_CHCONF_1[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 DMA read request disabled 1 DMA read request enabled

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Table 5-1897. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 DMA write request disabled 1 DMA write request enabled
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

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Table 5-1897. MCSPI_CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 1 2 2 4 3 8 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

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5.13.2.18 MCSPI_CH1STAT Register

5.13.2.18.1 MCSPI_CH1STAT Register (Offset = 144h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 1

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Table 5-1898. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0144h
MCSPI1	5220 1144h
MCSPI2	5220 2144h
MCSPI3	5220 3144h
MCSPI4	5220 4144h
MCSPI5	5220 5144h
MCSPI6	5220 6144h
MCSPI7	5220 7144h

Figure 5-929. MCSPI_CH1STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_2							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_2							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1899. MCSPI_CH1STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel 1 FIFO Receive Buffer Full Status 0 FIFO receive buffer is not full 1 FIFO receive buffer is full
5	RXFFE	R	0h	Channel 1 FIFO Receive Buffer Empty Status 0 FIFO receive buffer is not empty 1 FIFO receive buffer is empty
4	TXFFF	R	0h	Channel 1 FIFO Transmit Buffer Full Status 0 FIFO transmit buffer is not full 1 FIFO transmit buffer is full
3	TXFFE	R	0h	Channel 1 FIFO Transmit Buffer Empty Status 0 FIFO transmit buffer is not empty 1 FIFO transmit buffer is empty

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Table 5-1899. MCSPI_CH1STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel 1 End of transfer Status The definitions of beginning and end of transfer vary with master versus target and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1 This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel 1 Transmitter Register Status 0 Register is full. 1 Register is empty.
0	RXS	R	0h	Channel 1 Receiver Register Status 0 Register is empty. 1 Register is full.

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5.13.2.19 MCSPI_CH1CTRL Register

5.13.2.19.1 MCSPI_CH1CTRL Register (Offset = 148h) [reset = 0h]

This register is dedicated to enable the channel 1

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Table 5-1900. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0148h
MCSPI1	5220 1148h
MCSPI2	5220 2148h
MCSPI3	5220 3148h
MCSPI4	5220 4148h
MCSPI5	5220 5148h
MCSPI6	5220 6148h
MCSPI7	5220 7148h

Figure 5-930. MCSPI_CH1CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
EXTCLK							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							EN
R							R/W
0h							0h

Table 5-1901. MCSPI_CH1CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096clock divider ratio `0      Clock ratio is CLKD + 1.` `1      Clock ratio is CLKD + 1 + 16.` `FF     Clock ratio is CLKD + 1 + 4080.`
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable `0      Channel i is not active.` `1      Channel i is active.`

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5.13.2.20 MCSPI_TX1 Register

5.13.2.20.1 MCSPI_TX1 Register (Offset = 14Ch) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 5-1902. Instance Table

Instance Name	Physical Address
MCSPI0	5220 014Ch
MCSPI1	5220 114Ch
MCSPI2	5220 214Ch
MCSPI3	5220 314Ch
MCSPI4	5220 414Ch
MCSPI5	5220 514Ch
MCSPI6	5220 614Ch
MCSPI7	5220 714Ch

Figure 5-931. MCSPI_TX1 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 5-1903. MCSPI_TX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 1 Data to transmit

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5.13.2.21 MCSPI_RX1 Register

5.13.2.21.1 MCSPI_RX1 Register (Offset = 150h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

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Table 5-1904. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0150h
MCSPI1	5220 1150h
MCSPI2	5220 2150h
MCSPI3	5220 3150h
MCSPI4	5220 4150h
MCSPI5	5220 5150h
MCSPI6	5220 6150h
MCSPI7	5220 7150h

Figure 5-932. MCSPI_RX1 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 5-1905. MCSPI_RX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 1 Received Data

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5.13.2.22 MCSPI_CH2CONF Register

5.13.2.22.1 MCSPI_CH2CONF Register (Offset = 154h) [reset = 60000h]

This register is dedicated to the configuration of the channel 2

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Table 5-1906. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0154h
MCSPI1	5220 1154h
MCSPI2	5220 2154h
MCSPI3	5220 3154h
MCSPI4	5220 4154h
MCSPI5	5220 5154h
MCSPI6	5220 6154h
MCSPI7	5220 7154h

Figure 5-933. MCSPI_CH2CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS2		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 5-1907. MCSPI_CH2CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	Read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.

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Table 5-1907. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.
26:25	TCS2	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	RESERVED_1	R	0h	Read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_2[6] EPOL=0, and drives it high when MCSPI_CHCONF_2[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_2[6] EPOL=0, and drives it low when MCSPI_CHCONF_2[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 DMA read request disabled 1 DMA read request enabled

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Table 5-1907. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 DMA write request disabled 1 DMA write request enabled
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

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Table 5-1907. MCSPI_CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 1 2 2 4 3 8 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

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5.13.2.23 MCSPI_CH2STAT Register

5.13.2.23.1 MCSPI_CH2STAT Register (Offset = 158h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 2

Return to Summary Table

Table 5-1908. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0158h
MCSPI1	5220 1158h
MCSPI2	5220 2158h
MCSPI3	5220 3158h
MCSPI4	5220 4158h
MCSPI5	5220 5158h
MCSPI6	5220 6158h
MCSPI7	5220 7158h

Figure 5-934. MCSPI_CH2STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1909. MCSPI_CH2STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel 2 FIFO Receive Buffer Full Status 0 FIFO receive buffer is not full 1 FIFO receive buffer is full
5	RXFFE	R	0h	Channel 2 FIFO Receive Buffer Empty Status 0 FIFO receive buffer is not empty 1 FIFO receive buffer is empty
4	TXFFF	R	0h	Channel 2 FIFO Transmit Buffer Full Status 0 FIFO transmit buffer is not full 1 FIFO transmit buffer is full
3	TXFFE	R	0h	Channel 2 FIFO Transmit Buffer Empty Status 0 FIFO transmit buffer is not empty 1 FIFO transmit buffer is empty

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Table 5-1909. MCSPI_CH2STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel 2 End of transfer Status The definitions of beginning and end of transfer vary with master versus target and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1 This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel 2 Transmitter Register Status 0 Register is full. 1 Register is empty.
0	RXS	R	0h	Channel 2 Receiver Register Status 0 Register is empty. 1 Register is full.

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5.13.2.24 MCSPI_CH2CTRL Register

5.13.2.24.1 MCSPI_CH2CTRL Register (Offset = 15Ch) [reset = 0h]

This register is dedicated to enable the channel 2

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Table 5-1910. Instance Table

Instance Name	Physical Address
MCSPI0	5220 015Ch
MCSPI1	5220 115Ch
MCSPI2	5220 215Ch
MCSPI3	5220 315Ch
MCSPI4	5220 415Ch
MCSPI5	5220 515Ch
MCSPI6	5220 615Ch
MCSPI7	5220 715Ch

Figure 5-935. MCSPI_CH2CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
EXTCLK							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							EN
R							R/W
0h							0h

Table 5-1911. MCSPI_CH2CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

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5.13.2.25 MCSPI_TX2 Register

5.13.2.25.1 MCSPI_TX2 Register (Offset = 160h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

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Table 5-1912. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0160h
MCSPI1	5220 1160h
MCSPI2	5220 2160h
MCSPI3	5220 3160h
MCSPI4	5220 4160h
MCSPI5	5220 5160h
MCSPI6	5220 6160h
MCSPI7	5220 7160h

Figure 5-936. MCSPI_TX2 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 5-1913. MCSPI_TX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 2 Data to transmit

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5.13.2.26 MCSPI_RX2 Register

5.13.2.26.1 MCSPI_RX2 Register (Offset = 164h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

Return to Summary Table

Table 5-1914. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0164h
MCSPI1	5220 1164h
MCSPI2	5220 2164h
MCSPI3	5220 3164h
MCSPI4	5220 4164h
MCSPI5	5220 5164h
MCSPI6	5220 6164h
MCSPI7	5220 7164h

Figure 5-937. MCSPI_RX2 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 5-1915. MCSPI_RX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 2 Received Data

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5.13.2.27 MCSPI_CH3CONF Register

5.13.2.27.1 MCSPI_CH3CONF Register (Offset = 168h) [reset = 60000h]

This register is dedicated to the configuration of the channel 3

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Table 5-1916. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0168h
MCSPI1	5220 1168h
MCSPI2	5220 2168h
MCSPI3	5220 3168h
MCSPI4	5220 4168h
MCSPI5	5220 5168h
MCSPI6	5220 6168h
MCSPI7	5220 7168h

Figure 5-938. MCSPI_CH3CONF Name Register

31	30	29	28	27	26	25	24
RESERVED_0		CLKG	FFER	FFEW	TCS3		SBPOL
R		R/W	R/W	R/W	R/W		R/W
0h		0h	0h	0h	0h		0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SBE	RESERVED_1		FORCE	TURBO	IS	DPE1	DPE0
R/W	R		R/W	R/W	R/W	R/W	R/W
0h	0h		0h	0h	1h	1h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DMAR	DMAW	TRM		WL			
R/W	R/W	R/W		R/W			
0h	0h	0h		0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
WL	EPOL	CLKD				POL	PHA
R/W	R/W	R/W				R/W	R/W
0h	0h	0h				0h	0h

Table 5-1917. MCSPI_CH3CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED_0	R	0h	Read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values 0 Clock granularity of power of 2 1 One clock cycle granularity
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set 0 The buffer is not used to receive data. 1 The buffer is used to receive data.

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Table 5-1917. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set 0 The buffer is not used to transmit data. 1 The buffer is used to transmit data.
26:25	TCS3	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock 0 0.5 clock cycle 1 1.5 clock cycles 2 2.5 clock cycles 3 3.5 clock cycles
24	SBPOL	R/W	0h	Start bit polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
23	SBE	R/W	0h	Start bit enable for SPI transfer 0 Default MCSPI transfer length as specified by WL bit field 1 Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22:21	RESERVED_1	R	0h	Read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only] 0 Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_3[6] EPOL=0, and drives it high when MCSPI_CHCONF_3[6] EPOL=1. 1 Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_3[6] EPOL=0, and drives it low when MCSPI_CHCONF_3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0 Turbo is deactivated (recommended for single MCSPI word transfer). 1 Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0 Data line 0 (SPIDAT[0]) selected for reception 1 Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]] 0 Data line 1 (SPIDAT[1]) selected for transmission 1 No transmission on Data Line1 (SPIDAT[1])
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]] 0 Data Line0 (SPIDAT[0]) selected for transmission 1 No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel 0 DMA read request disabled 1 DMA read request enabled

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Table 5-1917. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel 0 DMA write request disabled 1 DMA write request enabled
13:12	TRM	R/W	0h	Transmit/Receive modes 0 Transmit-and-receive mode 1 Receive-only mode 2 Transmit-only mode 3 Reserved
11:7	WL	R/W	0h	SPI word length 0 Reserved 1 Reserved 2 Reserved 3 The MCSPI word is 4 bits long 4 The MCSPI word is 5 bits long 5 The MCSPI word is 6 bits long 6 The MCSPI word is 7 bits long 7 The MCSPI word is 8 bits long 8 The MCSPI word is 9 bits long 9 The MCSPI word is 10 bits long A The MCSPI word is 11 bits long B The MCSPI word is 12 bits long C The MCSPI word is 13 bits long D The MCSPI word is 14 bits long E The MCSPI word is 15 bits long F The MCSPI word is 16 bits long 10 The MCSPI word is 17 bits long 11 The MCSPI word is 18 bits long 12 The MCSPI word is 19 bits long 13 The MCSPI word is 20 bits long 14 The MCSPI word is 21 bits long 15 The MCSPI word is 22 bits long 16 The MCSPI word is 23 bits long 17 The MCSPI word is 24 bits long 18 The MCSPI word is 25 bits long 19 The MCSPI word is 26 bits long 1A The MCSPI word is 27 bits long 1B The MCSPI word is 28 bits long 1C The MCSPI word is 29 bits long 1D The MCSPI word is 30 bits long 1E The MCSPI word is 31 bits long 1F The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state

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Table 5-1917. MCSPI_CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0 0 1 1 2 2 4 3 8 4 16 5 32 6 64 7 128 8 256 9 512 A 1024 B 2048 C 4096 D 8192 E 16384 F 32768
1	POL	R/W	0h	SPICLK polarity 0 SPICLK is held low during the INACTIVE state 1 SPICLK is held high during the INACTIVE state
0	PHA	R/W	0h	SPICLK phase 0 Data are latched on odd-numbered edges of SPICLK. 1 Data are latched on even-numbered edges of SPICLK.

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5.13.2.28 MCSPI_CH3STAT Register

5.13.2.28.1 MCSPI_CH3STAT Register (Offset = 16Ch) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 3

Return to Summary Table

Table 5-1918. Instance Table

Instance Name	Physical Address
MCSPI0	5220 016Ch
MCSPI1	5220 116Ch
MCSPI2	5220 216Ch
MCSPI3	5220 316Ch
MCSPI4	5220 416Ch
MCSPI5	5220 516Ch
MCSPI6	5220 616Ch
MCSPI7	5220 716Ch

Figure 5-939. MCSPI_CH3STAT Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED_2	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1919. MCSPI_CH3STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED_2	R	0h	Read returns 0
6	RXFFF	R	0h	Channel 3 FIFO Receive Buffer Full Status `0 FIFO receive buffer is not full` `1 FIFO receive buffer is full`
5	RXFFE	R	0h	Channel 3 FIFO Receive Buffer Empty Status `0 FIFO receive buffer is not empty` `1 FIFO receive buffer is empty`
4	TXFFF	R	0h	Channel 3 FIFO Transmit Buffer Full Status `0 FIFO transmit buffer is not full` `1 FIFO transmit buffer is full`
3	TXFFE	R	0h	Channel 3 FIFO Transmit Buffer Empty Status `0 FIFO transmit buffer is not empty` `1 FIFO transmit buffer is empty`

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Table 5-1919. MCSPI_CH3STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EOT	R	0h	Channel 3 End of transfer Status The definitions of beginning and end of transfer vary with master versus target and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details 0 This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1 This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel 3 Transmitter Register Status 0 Register is full. 1 Register is empty.
0	RXS	R	0h	Channel 3 Receiver Register Status 0 Register is empty. 1 Register is full.

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5.13.2.29 MCSPI_CH3CTRL Register

5.13.2.29.1 MCSPI_CH3CTRL Register (Offset = 170h) [reset = 0h]

This register is dedicated to enable the channel 3

Return to Summary Table

Table 5-1920. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0170h
MCSPI1	5220 1170h
MCSPI2	5220 2170h
MCSPI3	5220 3170h
MCSPI4	5220 4170h
MCSPI5	5220 5170h
MCSPI6	5220 6170h
MCSPI7	5220 7170h

Figure 5-940. MCSPI_CH3CTRL Name Register

31	30	29	28	27	26	25	24
RESERVED_2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_2							
R							
0h							
15	14	13	12	11	10	9	8
EXTCLK							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED_1							EN
R							R/W
0h							0h

Table 5-1921. MCSPI_CH3CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED_2	R	0h	Read returns 0
15:8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096clock divider ratio 0 Clock ratio is CLKD + 1. 1 Clock ratio is CLKD + 1 + 16. FF Clock ratio is CLKD + 1 + 4080.
7:1	RESERVED_1	R	0h	Read returns 0
0	EN	R/W	0h	Channel Enable 0 Channel i is not active. 1 Channel i is active.

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5.13.2.30 MCSPI_TX3 Register

5.13.2.30.1 MCSPI_TX3 Register (Offset = 174h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

Return to Summary Table

Table 5-1922. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0174h
MCSPI1	5220 1174h
MCSPI2	5220 2174h
MCSPI3	5220 3174h
MCSPI4	5220 4174h
MCSPI5	5220 5174h
MCSPI6	5220 6174h
MCSPI7	5220 7174h

Figure 5-941. MCSPI_TX3 Name Register

31	30	29	28	27	26	25	24
TDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
TDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
TDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
TDATA							
R/W							
0h							

Table 5-1923. MCSPI_TX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TDATA	R/W	0h	Channel 3 Data to transmit

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5.13.2.31 MCSPI_RX3 Register

5.13.2.31.1 MCSPI_RX3 Register (Offset = 178h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

Return to Summary Table

Table 5-1924. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0178h
MCSPI1	5220 1178h
MCSPI2	5220 2178h
MCSPI3	5220 3178h
MCSPI4	5220 4178h
MCSPI5	5220 5178h
MCSPI6	5220 6178h
MCSPI7	5220 7178h

Figure 5-942. MCSPI_RX3 Name Register

31	30	29	28	27	26	25	24
RDATA							
R							
0h							
23	22	21	20	19	18	17	16
RDATA							
R							
0h							
15	14	13	12	11	10	9	8
RDATA							
R							
0h							
7	6	5	4	3	2	1	0
RDATA							
R							
0h							

Table 5-1925. MCSPI_RX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RDATA	R	0h	Channel 3 Received Data

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5.13.2.32 MCSPI_XFERLEVEL Register

5.13.2.32.1 MCSPI_XFERLEVEL Register (Offset = 17Ch) [reset = 0h]

This register provides transfer levels needed while using FIFO buffer during transfer.

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Table 5-1926. Instance Table

Instance Name	Physical Address
MCSPI0	5220 017Ch
MCSPI1	5220 117Ch
MCSPI2	5220 217Ch
MCSPI3	5220 317Ch
MCSPI4	5220 417Ch
MCSPI5	5220 517Ch
MCSPI6	5220 617Ch
MCSPI7	5220 717Ch

Figure 5-943. MCSPI_XFERLEVEL Name Register

31	30	29	28	27	26	25	24
WCNT							
R/W							
0h							
23	22	21	20	19	18	17	16
WCNT							
R/W							
0h							
15	14	13	12	11	10	9	8
AFL							
R/W							
0h							
7	6	5	4	3	2	1	0
AEL							
R/W							
0h							

Table 5-1927. MCSPI_XFERLEVEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	WCNT	R/W	0h	Spi word counterThis register holds the programmable value of number of SPI word to be transferred on channel which is using the FIFO bufferWhen transfer had started, a read back in this register returns the current SPI word transfer index. 0x0: Counter not used 0x1: One spi word . . 0xFFFE: 65534 spi word 0xFFFF: 65535 spi word 0 Counter not used 1 One word FFFE 65534 MCSPI word FFFF 65535 MCSPI word

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Table 5-1927. MCSPI_XFERLEVEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	AFL	R/W	0h	Buffer Almost Full This register holds the programmable almost full level value used to determine almost full buffer condition If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_MODULCTRL[AFL] must be set with n-1The size of this register is defined by the generic parameter FFNBYTE. 0x0: One byte 0x1: 2 bytes . . 0xFF: 256 bytes 0 1 byte 1 2 bytes FE 255bytes FF 256bytes
7:0	AEL	R/W	0h	Buffer Almost EmptyThis register holds the programmable almost empty level value used to determine almost empty buffer condition If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_MODULCTRL[AEL] must be set with n-1. 0x0: One byte 0x1: 2 bytes . . 0xFF: 256 bytes 0 1 byte 1 2 bytes FE 255 bytes FF 256bytes

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5.13.2.33 MCSPI_DAFTX Register

5.13.2.33.1 MCSPI_DAFTX Register (Offset = 180h) [reset = 0h]

This register contains the SPI words to transmit on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_TX(i) register corresponding to the channel which have its FIFO enabled.

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Table 5-1928. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0180h
MCSPI1	5220 1180h
MCSPI2	5220 2180h
MCSPI3	5220 3180h
MCSPI4	5220 4180h
MCSPI5	5220 5180h
MCSPI6	5220 6180h
MCSPI7	5220 7180h

Figure 5-944. MCSPI_DAFTX Name Register

31	30	29	28	27	26	25	24
DAFTDATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DAFTDATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DAFTDATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DAFTDATA							
R/W							
0h							

Table 5-1929. MCSPI_DAFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAFTDATA	R/W	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

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5.13.2.34 MCSPI_DAFRX Register

5.13.2.34.1 MCSPI_DAFRX Register (Offset = 1A0h) [reset = 0h]

This register contains the SPI words to received on the serial link when FIFO used and DMA address is aligned on 256 bit.This register is an image of one of MCSPI_RX(i) register corresponding to the channel which have its FIFO enabled.

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Table 5-1930. Instance Table

Instance Name	Physical Address
MCSPI0	5220 01A0h
MCSPI1	5220 11A0h
MCSPI2	5220 21A0h
MCSPI3	5220 31A0h
MCSPI4	5220 41A0h
MCSPI5	5220 51A0h
MCSPI6	5220 61A0h
MCSPI7	5220 71A0h

Figure 5-945. MCSPI_DAFRX Name Register

31	30	29	28	27	26	25	24
DAFRDATA							
R							
0h							
23	22	21	20	19	18	17	16
DAFRDATA							
R							
0h							
15	14	13	12	11	10	9	8
DAFRDATA							
R							
0h							
7	6	5	4	3	2	1	0
DAFRDATA							
R							
0h							

Table 5-1931. MCSPI_DAFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DAFRDATA	R	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

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5.14 MMCSD

MMCSD

5.14.1 MMCSD Summaries

MMCSD Summaries

Table 5-1932. MMC Registers, Base Address=4830 0000h, Length=8192

Offset	Length	Register Name	MMCSD0 Physical Address
4h	32	MMC_HL_HWINFO	4830 0004h
10h	32	MMC_HL_SYSCONFIG	4830 0010h
114h	32	MMC_SYSSTATUS	4830 0114h
124h	32	MMC_CSRE	4830 0124h
128h	32	MMC_SYSTEST	4830 0128h
12Ch	32	MMC_CON	4830 012Ch
130h	32	MMC_PWCNT	4830 0130h
134h	32	MMC_DLL	4830 0134h
200h	32	MMC_SDMASA	4830 0200h
204h	32	MMC_BLK	4830 0204h
208h	32	MMC_ARG	4830 0208h
20Ch	32	MMC_CMD	4830 020Ch
210h	32	MMC_RSP10	4830 0210h
214h	32	MMC_RSP32	4830 0214h
218h	32	MMC_RSP54	4830 0218h
21Ch	32	MMC_RSP76	4830 021Ch
220h	32	MMC_DATA	4830 0220h
224h	32	MMC_PSTATE	4830 0224h
228h	32	MMC_HCTL	4830 0228h
22Ch	32	MMC_SYSCTL	4830 022Ch
230h	32	MMC_STAT	4830 0230h
234h	32	MMC_IE	4830 0234h
238h	32	MMC_ISE	4830 0238h
23Ch	32	MMC_AC12	4830 023Ch
240h	32	MMC_CAPA	4830 0240h
244h	32	MMC_CAPA2	4830 0244h
248h	32	MMC_CUR_CAPA	4830 0248h
250h	32	MMC_FE	4830 0250h
254h	32	MMC_ADMAES	4830 0254h
258h	32	MMC_ADMASAL	4830 0258h
260h	32	MMC_PVINITSD	4830 0260h
264h	32	MMC_PVHSSDR12	4830 0264h
268h	32	MMC_PVSDR25SDR50	4830 0268h
26Ch	32	MMC_PVSDR104DDR50	4830 026Ch
2FCh	32	MMC_REV	4830 02FCh

5.14.2 MMCSD Registers

MMCSD Registers

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5.14.2.1 MMC_HL_HWINFO Register

5.14.2.1.1 MMC_HL_HWINFO Register (Offset = 4h) [reset = 8h]

Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.

Return to Summary Table

Table 5-1933. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0004h

Figure 5-946. MMC_HL_HWINFO Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	RETMODE	MEM_SIZE				MERGE_MEM	MADMA_EN
R	R	R				R	R
0h	0h	2h				0h	0h

Table 5-1934. MMC_HL_HWINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:7	RESERVED	R	0h	
6	RETMODE	R	0h	Retention Mode generic parameter This bit field indicates whether the retention mode is supported using the pin PIRFFRET. 0 Retention mode disabled 1 Retention mode enabled
5:2	MEM_SIZE	R	2h	Memory size for FIFO buffer: 1 Memory of 512 bytes, max block length is 512 bytes 2 Memory of 1024 bytes, max block length is 1024 bytes 4 Memory of 2048 bytes, max block length is 2048 bytes 8 Memory of 4096 bytes, max block length is 2048 bytes
1	MERGE_MEM	R	0h	Memory merged for FIFO buffer: This register defines the configuration of FIFO buffer architecture. If the bit is set STA and DFT shall support clock multiplexing and balancing. 0 2 memories instantiated, one per data transfer direction. 1 A single memory is used with multiplexed addresses, data and clocks.

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Table 5-1934. MMC_HL_HWINFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MADMA_EN	R	0h	Master DMA enabled generic parameter: This register defines the configuration of the controller to know if it supports the master DMA management called ADMA. 0 No Master DMA (ADMA) management supported 1 Controller supports ADMA

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5.14.2.2 MMC_HL_SYSCONFIG Register

5.14.2.2.1 MMC_HL_SYSCONFIG Register (Offset = 10h) [reset = 28h]

Clock Management Configuration Register.

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Table 5-1935. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0010h

Figure 5-947. MMC_HL_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED		STANDBYMODE		IDLEMODE		FREEEMU	SOFTRESET
R		R/W		R/W		R/W	R/W
0h		2h		2h		0h	0h

Table 5-1936. MMC_HL_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	R	0h	
5:4	STANDBYMODE	R/W	2h	Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state. 0 `Force-standby mode: local initiator is unconditionally placed in standby state.Backup mode, for debug only.` 1 `No-standby mode: local initiator is unconditionally placed out of standby state.Backup mode, for debug only.` 2 `Smart-standby mode: local initiator standby status depends on local conditions, i.e. the module's functional requirement from the initiator.IP module shall not generate (initiator-related) wakeup events.` 3 `Smart-Standby wakeup-capable mode: local initiator standby status depends on local conditions, i.e. the module's functional requirement from the initiator. IP module may generate (master-related) wakeup events when in standby state.Mode is only relevant if the appropriate IP module "mwakeup" output is implemented.`

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Table 5-1936. MMC_HL_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:2	IDLEMODE	R/W	2h	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0 Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements.Backup mode, for debug only. 1 No-idle mode: local target never enters idle state.Backup mode, for debug only. 2 Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements.IP module shall not generate (IRQ- or DMA-request-related) wakeup events. 3 Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements.IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state.Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) implemented.
1	FREEEMU	R/W	0h	Sensitivity to emulation [debug] suspend input signal. Functionality NOT implemented in MMCSD. 0 IP module is sensitive to emulation suspend 1 IP module is not sensitive to emulation suspend
0	SOFTRESET	R/W	0h	Software reset. [Optional] 0 No action 0 Reset done, no pending action 1 Reset (software or other) ongoing 1 Initiate software reset

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5.14.2.3 MMC_SYSSTATUS Register

5.14.2.3.1 MMC_SYSSTATUS Register (Offset = 114h) [reset = 0h]

System Status Register
This register provides status information about the module excluding the interrupt status information.

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Table 5-1937. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0114h

Figure 5-948. MMC_SYSSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R							R
0h							0h

Table 5-1938. MMC_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	
0	RESETDONE	R	0h	Internal Reset Monitoring Note: the debounce clock , the system clock [OCP] and the functional clock shall be provided to the MMC/SD/SDIO host controller to allow the internal reset monitoring. 0 Internal module reset is on-going 1 Reset completed.

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5.14.2.4 MMC_CSRE Register

5.14.2.4.1 MMC_CSRE Register (Offset = 124h) [reset = 0h]

Card Status Response Error
This register enables the host controller to detect card status errors of response type R1, R1b for all cards and of R5, R5b and R6 response for cards types SD or SDIO.
When a bit MMCHS_CSRE[i] is set to 1, if the corresponding bit at the same position in the response MMCHS_RSP0[i] is set to 1, the host controller indicates a card error (MMCHS_STAT[CERR]) interrupt status to avoid the host driver reading the response register (MMCHS_RSP0).
Note: No automatic card error detection for autoCMD12 is implemented; the host system has to check autoCMD12 response register (MMCHS_RESP76) for possible card errors.

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Table 5-1939. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0124h

Figure 5-949. MMC_CSRE Name Register

31	30	29	28	27	26	25	24
CSRE							
R/W							
0h							
23	22	21	20	19	18	17	16
CSRE							
R/W							
0h							
15	14	13	12	11	10	9	8
CSRE							
R/W							
0h							
7	6	5	4	3	2	1	0
CSRE							
R/W							
0h							

Table 5-1940. MMC_CSRE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CSRE	R/W	0h	Card status response error

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5.14.2.5 MMC_SYSTEST Register

5.14.2.5.1 MMC_SYSTEST Register (Offset = 128h) [reset = 0h]

System Test Register
This register is used to control the signals that connect to I/O pins when the module is configured in system test (SYSTEST) mode for boundary connectivity verification.
Note: In SYSTEST mode, a write into MMCHS_CMD register will not start a transfer. The buffer behaves as a stack accessible only by the local host (push and pop operations). In this mode, the Transfer Block Size (MMCHS_BLK[BLEN]) and the Blocks count for current transfer (MMCHS_BLK[NBLK]) are needed to generate a Buffer write ready interrupt (MMCHS_STAT[BWR]) or a Buffer read ready interrupt (MMCHS_STAT[BRR]) and DMA requests if enabled.

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Table 5-1941. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0128h

Figure 5-950. MMC_SYSTEST Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							OBI
R							R
0h							0h
15	14	13	12	11	10	9	8
SDCD	SDWP	WAKD	SSB	D7D	D6D	D5D	D4D
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
D3D	D2D	D1D	D0D	DDIR	CDAT	CDIR	MCKD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1942. MMC_SYSTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	R	0h	
16	OBI	R	0h	Out-Of-Band Interrupt [OBI] data value 0 The Out-of-Band Interrupt pin is driven low. 1 The Out-of-Band Interrupt pin is driven high.
15	SDCD	R	0h	Card detect input signal [SDCD] data value 0 The card detect pin is driven low. 1 The card detect pin is driven high.
14	SDWP	R	0h	Write protect input signal [SDWP] data value 0 The write protect pin SDWP is driven low. 1 The write protect pin SDWP is driven high.

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Table 5-1942. MMC_SYSTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	WAKD	R/W	0h	Wake request output signal data value 0 The pin SWAKEUP is driven low. 0 No action. Returns 0. 1 The pin SWAKEUP is driven high. 1 No action. Returns 1.
12	SSB	R/W	0h	Set status bit This bit must be cleared prior attempting to clear a status bit of the interrupt status register [MMCSD_STAT]. 0 Clear this SSB bitfield. Writing 0 does not clear already set status bits; 0 No action. Returns 0. 1 No action. Returns 1. 1 Force to 1 all status bits of the interrupt status register (MMCHS_STAT) only if the corresponding bitfield in the Interrupt signal enable register (MMCHS_ISE) is set.
11	D7D	R/W	0h	DAT7 input/output signal data value 0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT7 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT7 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0 1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT7 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT7 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1
10	D6D	R/W	0h	DAT6 input/output signal data value 0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT6 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT6 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0 1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT6 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT6 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1
9	D5D	R/W	0h	DAT5 input/output signal data value 0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT5 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT5 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0 1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT5 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT5 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1

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Table 5-1942. MMC_SYSTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	D4D	R/W	0h	DAT4 input/output signal data value 0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT4 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT4 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0 1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT4 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT4 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1
7	D3D	R/W	0h	DAT3 input/output signal data value 0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT3 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT3 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0 1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT3 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT3 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1
6	D2D	R/W	0h	DAT2 input/output signal data value 0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT2 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT2 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0 1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT2 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT2 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1
5	D1D	R/W	0h	DAT1 input/output signal data value 0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT1 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT1 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0 1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT1 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT1 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1

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Table 5-1942. MMC_SYSTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	D0D	R/W	0h	DAT0 input/output signal data value 0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT0 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0 0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT0 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT0 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect. 1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT0 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1
3	DDIR	R/W	0h	Control of the DAT[7:0] pins direction. 0 The DAT lines are outputs (host to card) 0 No action. Returns 0. 1 The DAT lines are inputs (card to host) 1 No action. Returns 1.
2	CDAT	R/W	0h	CMD input/output signal data value 0 If SYSTEST[CDIR] = 0 (output mode direction), the CMD line is driven low. If SYSTEST[CDIR] = 1 (input mode direction), no effect. 0 If SYSTEST[CDIR] = 1 (input mode direction), returns the value on the CMD line (low). If SYSTEST[CDIR] = 0 (output mode direction), returns 0 1 If SYSTEST[CDIR] = 0 (output mode direction), the CMD line is driven high. If SYSTEST[CDIR] = 1 (input mode direction), no effect. 1 If SYSTEST[CDIR] = 1 (input mode direction), returns the value on the CMD line (high) If SYSTEST[CDIR] = 0 (output mode direction), returns 1
1	CDIR	R/W	0h	Control of the CMD pin direction. 0 The CMD line is an output (host to card) 0 No action. Returns 0. 1 The CMD line is an input (card to host) 1 No action. Returns 1.
0	MCKD	R/W	0h	MMC clock output signal data value 0 The output clock is driven low. 0 No action. Returns 0. 1 The output clock is driven high. 1 No action. Returns 1.

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5.14.2.6 MMC_CON Register

5.14.2.6.1 MMC_CON Register (Offset = 12Ch) [reset = 600h]

Configuration Register
This register is used:
- to select the functional mode or the SYSTEST mode for any card.
- to send an initialization sequence to any card.
- to enable the detection on DAT[1] of a card interrupt for SDIO cards only.
and also to configure :
- specific data and command transfers for MMC cards only.
- the parameters related to the card detect and write protect input signals.

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Table 5-1943. Instance Table

Instance Name	Physical Address
MMCSD0	4830 012Ch

Figure 5-951. MMC_CON Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED		SDMA_LNE	DMA_MNS	DDR	BOOT_CF0	BOOT_ACK	CLKEXTFREE
R		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
PADEN	OBIE	OBIP	CEATA	CTPL	DVAL		WPP
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	3h		0h
7	6	5	4	3	2	1	0
CDP	MIT	DW8	MODE	STR	HR	INIT	OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1944. MMC_CON Register Field Descriptions

Bit	Field	Type	Reset	Description
31:22	RESERVED	R	0h	
21	SDMA_LNE	R/W	0h	Target DMA Level/Edge Request: The waveform of the DMA request can be configured either edge sensitive with early de-assertion on first access to MMCSD_DATA register or late de-assertion, request remains active until last allowed data written into MMCSD_DATA. 0 `Slave DMA edge sensitive, Early DMA de-assertion` 1 `Slave DMA level sensitive, Late DMA de-assertion`

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Table 5-1944. MMC_CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DMA_MNS	R/W	0h	DMA Master or Target selection: When this bit is set and the controller is configured to use the DMA, Ocp master interface is used to get datas from system using ADMA2 procedure [direct access to the memory].This option is only available if generic parameter MADMA_EN is asserted to '1'. 0 The controller is slave on data transfers with system. 1 The controller is master on data exchange with system, controller must be configured as using DMA.
19	DDR	R/W	0h	Dual Data Rate mode: When this register is set, the controller uses both clock edge to emit or receive data. Odd bytes are transmitted on falling edges and even bytes are transmitted on rise edges. It only applies on Data bytes and CRC, Start, end bits and CRC status are kept full cycle. This bit field is only meaningful and active for even clock divider ratio of MMCSD_SYSCTL[CLKD], it is insensitive to MMCSD_HCTL[HSPE] setting. 0 Standard mode : data are transmitted on a single edge depending on MMCHS_HCTRL[HSPE]. 1 Data Bytes and CRC are transmitted on both edge.
18	BOOT_CF0	R/W	0h	Boot status supported: This register is set when the CMD line need to be forced to '0' for a boot sequence. CMD line is driven to '0' after Writing in MMCSD_CMD. The line is released when this bit field is de-asserted and abort data transfer in case of a pending transaction. 0 CMD line is released when it was previously forced to '0' by a boot sequence. 0 CMD line not forced 1 CMD line forced to '0' is enabled and will be active after writing into MMCHS_CMD 1 CMD line forced to '0' is enabled
17	BOOT_ACK	R/W	0h	Book acknowledge received: When this bit is set the controller should receive a boot status on DAT0 line after next command issued. If no status is received a data timeout will be generated. 0 No acknowledge to be received 1 A boot status will be received on DAT0 line after issuing a command.
16	CLKEXTFREE	R/W	0h	External clock free running: This register is used to maintain card clock out of transfer transaction to enable target module for example to generate a synchronous interrupt on DAT[1]. The Clock will be maintain only if MMCSD_SYSCTL[CEN] is set. 0 External card clock is cut off outside active transaction period. 1 External card clock is maintain even out of active transaction period only if MMCHS_SYSCTL[CEN] is set.
15	PADEN	R/W	0h	Control Power for MMC Lines: This register is only useful when MMC PADs contain power saving mechanism to minimize its leakage power. It works as a GPIO that directly control the ACTIVE pin of PADs. Excepted for DAT[1], the signal is also combine outside the module with the dedicated power control MMCSD_CON[CTPL] bit. 0 ADPIDLE module pin is not forced, it is automatically generated by the MMC fsms. 1 ADPIDLE module pin is forced to active state.

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Table 5-1944. MMC_CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	OBIE	R/W	0h	Out-of-Band Interrupt Enable MMC cards only: This bit enables the detection of Out-of-Band Interrupt on MMCOBI input pin. The usage of the Out-of-Band signal [OBI] is optional and depends on the system integration. 0 Out-of-Band interrupt detection disabled 1 Out-of-Band interrupt detection enabled
13	OBIP	R/W	0h	Out-of-Band Interrupt Polarity MMC cards only: This bit selects the active level of the out-of-band interrupt coming from MMC cards. The usage of the Out-of-Band signal [OBI] is optional and depends on the system integration. 0 Active high level 1 Active low level
12	CEATA	R/W	0h	CE-ATA control mode MMC cards compliant with CE-ATA:By default, this bit is set to 0. It is use to indicate that next commands are considered as specific CE-ATA commands that potentially use 'command completion' features. 0 Standard MMC/SD/SDIO mode. 1 CE-ATA mode next commands are considered as CE-ATA commands.
11	CTPL	R/W	0h	Control Power for DAT[1] line MMC and SD cards: By default, this bit is set to 0 and the host controller automatically disables all the input buffers outside of a transaction to minimize the leakage current. SDIO cards: When this bit is set to 1, the host controller automatically disables all the input buffers except the buffer of DAT[1] outside of a transaction in order to detect asynchronous card interrupt on DAT[1] line and minimize the leakage current of the buffers. 0 Disable all the input buffers outside of a transaction. 1 Disable all the input buffers except the buffer of DAT[1] outside of a transaction.
10:9	DVAL	R/W	3h	Debounce filter value All cards This register is used to define a debounce period to filter the card detect input signal [SDCD]. The usage of the card detect input signal [SDCD] is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0 33 us debounce period 1 231 us debounce period 2 1 ms debounce period 3 8,4 ms debounce period
8	WPP	R/W	0h	Write protect polarity For SD and SDIO cards only This bit selects the active level of the write protect input signal [SDWP]. The usage of the write protect input signal [SDWP] is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0 Active high level 1 Active low level

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Table 5-1944. MMC_CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CDP	R/W	0h	Card detect polarity All cards This bit selects the active level of the card detect input signal [SDCD]. The usage of the card detect input signal [SDCD] is optional and depends on the system integration and the type of the connector housing that accommodates the card. 0 Active low level 1 Active high level
6	MIT	R/W	0h	MMC interrupt command Only for MMC cards. This bit must be set to 1, when the next write access to the command register [MMCSD_CMD] is for Writing a MMC interrupt command [CMD40] requiring the command timeout detection to be disabled for the command response. 0 Command timeout enabled 1 Command timeout disabled
5	DW8	R/W	0h	8-bit mode MMC select For SD/SDIO cards, this bit must be set to 0. For MMC card, this bit must be set following a valid SWITCH command [CMD6] with the correct value and extend CSD index written in the argument. Prior to this command, the MMC card configuration register [CSD and EXT_CSD] must be verified for compliancy with MMC standard specification 4.x [see section 3.6]. 0 1-bit or 4-bit Data width (DAT[0] used, MMC, SD cards) 1 8-bit Data width (DAT[7:0] used, MMC cards)
4	MODE	R/W	0h	Mode select All cards These bits select between Functional mode and SYSTEST mode. 0 Functional mode. Transfers to the MMC/SD/SDIO cards follow the card protocol. MMC clock is enabled. MMC/SD transfers are operated under the control of the CMD register. 1 SYSTEST mode The signal pins are configured as general-purpose input/output and the 1024-byte buffer is configured as a stack memory accessible only by the local host or system DMA. The pins retain their default type (input, output or in-out). SYSTEST mode is operated under the control of the SYSTEST register.
3	STR	R/W	0h	Stream command Only for MMC cards. This bit must be set to 1 only for the stream data transfers [read or write] of the adtc commands. Stream read is a class 1 command [CMD11: READ_DAT_UNTIL_STOP]. Stream write is a class 3 command [CMD20: WRITE_DAT_UNTIL_STOP]. 0 Block oriented data transfer 1 Stream oriented data transfer

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Table 5-1944. MMC_CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	HR	R/W	0h	Broadcast host response Only for MMC cards. This register is used to force the host to generate a 48-bit response for bc command type. It can be used to terminate the interrupt mode by generating a CMD40 response by the core [see section 4.3, "Interrupt Mode", in the MMC [1] specification]. In order to have the host response to be generated in open drain mode, the register MMCSD_CON[OD] must be set to 1. When MMCSD_CON[CEATA] is set to 1 and MMCSD_ARG set to 0x00000000 when Writing 0x00000000 into MMCSD_CMD register, the host controller performs a 'command completion signal disable' token i.e. CMD line held to '0' during 47 cycles followed by a 1. 0 The host does not generate a 48-bit response instead of a command. 1 The host generates a 48-bit response instead of a command or a command completion signal disable token.
1	INIT	R/W	0h	Send initialization stream All cards. When this bit is set to 1, and the card is idle, an initialization sequence is sent to the card. An initialization sequence consists of setting the CMD line to 1 during 80 clock cycles. The initialization sequence is mandatory - but it is not required to do it through this bit - this bit makes it easier. Clock divider [MMCSD_SYSCTL[CLKD]] should be set to ensure that 80 clock periods are greater than 1ms. [see section 9.3, "Power-Up", in the MMC card specification [1], or section 6.4 in the SD card specification [2]]. Note: in this mode, there is no command sent to the card and no response is expected 0 The host does not send an initialization sequence. 1 The host sends an initialization sequence.
0	OD	R/W	0h	Card open drain mode. Only for MMC cards. This bit must be set to 1 for MMC card commands 1, 2, 3 and 40, and if the MMC card bus is operating in open-drain mode during the response phase to the command sent. Typically, during card identification mode when the card is either in idle, ready or ident state. It is also necessary to set this bit to 1, for a broadcast host response [see Broadcast host response register MMCSD_CON[HR]] 0 No Open Drain 1 Open Drain or Broadcast host response

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5.14.2.7 MMC_PWCNT Register

5.14.2.7.1 MMC_PWCNT Register (Offset = 130h) [reset = 0h]

Power Counter Register
This register is used to program a mmc counter to delay command transfers after activating the PAD power, this value depends on PAD characteristics and voltage.

Return to Summary Table

Table 5-1945. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0130h

Figure 5-952. MMC_PWCNT Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
PWRCNT							
R/W							
0h							
7	6	5	4	3	2	1	0
PWRCNT							
R/W							
0h							

Table 5-1946. MMC_PWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED	R	0h	
15:0	PWRCNT	R/W	0h	Power counter register. This register is used to introduce a delay between the PAD ACTIVE pin assertion and the command issued. 0 No additional delay added 1 TCF delay (card clock period) 2 TCF x 2 delay (card clock period) 65534 TCF x 65534 delay (card clock period) 65535 TCF x 65535 delay (card clock period)

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5.14.2.8 MMC_DLL Register

5.14.2.8.1 MMC_DLL Register (Offset = 134h) [reset = 80000000h]

DLL control and status register
This register is used for tuning procedure required for SDR104 speed mode.
It gives visibility and control on the DLL.

Return to Summary Table

Table 5-1947. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0134h

Figure 5-953. MMC_DLL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td>DLL_SOFT_RESET</td><td>LOCK_TIMER</td><td colspan="6">MAX_LOCK_DIFF</td></tr>
<tr><td>R/W</td><td>R/W</td><td colspan="6">R/W</td></tr>
<tr><td>1h</td><td>0h</td><td colspan="6">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="2">MAX_LOCK_DIFF</td><td colspan="2">FORCE_SR_F</td><td colspan="4">FORCE_SR_C</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">FORCE_SR_C</td><td>FORCE_VALUE</td><td colspan="4">SLAVE_RATIO</td></tr>
<tr><td colspan="3">R/W</td><td>R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="4">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">SLAVE_RATIO</td><td colspan="2">RESERVED</td><td>DLL_UNLOCK_CLEAR</td><td>DLL_UNLOCK_STICKY</td><td>DLL_CALIB</td><td>DLL_LOCK</td></tr>
<tr><td colspan="2">R/W</td><td colspan="2">R</td><td>R/W</td><td>R</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="2">0h</td><td colspan="2">0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-1948. MMC_DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DLL_SOFT_RESET	R/W	1h	Soft reset for DLL, active HIGH. 0 Reset completed. 0 No action. 1 Reset is in progress 1 Issue soft reset
30	LOCK_TIMER	R/W	0h	Timer for the dll_lock signal to be asserted after reset. 0 1024 cycles (equivalent to DLL fast mode lock) 1 66560 cycles
29:22	MAX_LOCK_DIFF	R/W	0h	Maximum number of taps that the master DLLs clock period measurement can deviate without resulting in the master DLL losing lock.
21:20	FORCE_SR_F	R/W	0h	Forced fine delay value.
19:13	FORCE_SR_C	R/W	0h	Forced coarse delay value
12	FORCE_VALUE	R/W	0h	Put forced values to target DLL, ignoring master DLL output and ratio value. 0 Do not put force value 1 Put force value.

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Table 5-1948. MMC_DLL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:6	SLAVE_RATIO	R/W	0h	Fraction of a clock cycle for the shift to be implemented, in units of 256ths of a clock cycle. 0 0 degree delay 2 45 degrees delay 4 90 degrees delay 6 135 degrees delay 8 180 degrees delay 10 225 degrees delay 12 270 degrees delay 14 315 degrees delay 16 Full clock delay 63 4 clocks delay
5:4	RESERVED	R	0h	
3	DLL_UNLOCK_CLEAR	R/W	0h	Clears the phy_reg_status_mdll_unlock_sticky flags of the DLL. 0 No effect. 1 Clears the flag.
2	DLL_UNLOCK_STICKY	R	0h	Asserted when any single period measurement exceeds MAX_LOCK_DIFF.
1	DLL_CALIB	R/W	0h	Enables Target DLL to update new delay values. 0 Disabled 1 Enabled
0	DLL_LOCK	R	0h	Master DLL lock status. 0 DLL is not locked 1 DLL is locked

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5.14.2.9 MMC_SDMASA Register

5.14.2.9.1 MMC_SDMASA Register (Offset = 200h) [reset = 0h]

SDMA System Address / Argument 2 Register.

Return to Summary Table

Table 5-1949. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0200h

Figure 5-954. MMC_SDMASA Name Register

31	30	29	28	27	26	25	24
SDMA_ARG2							
R/W							
0h							
23	22	21	20	19	18	17	16
SDMA_ARG2							
R/W							
0h							
15	14	13	12	11	10	9	8
SDMA_ARG2							
R/W							
0h							
7	6	5	4	3	2	1	0
SDMA_ARG2							
R/W							
0h							

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Table 5-1950. MMC_SDMASA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	SDMA_ARG2	R/W	0h	SDMA System Address / Argument 2 This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23. [1] SDMA System Address This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing [i.e., after a transaction has stopped]. Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register 003h is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register. [2] Argument 2 This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23. If Auto CMD23 is used with ADMA, the full 32-bit block count value can be used. If Auto CMD23 is used without AMDA, the available block count value is limited by the Block Count register. 65535 blocks is the maximum value in this case.

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5.14.2.10 MMC_BLK Register

5.14.2.10.1 MMC_BLK Register (Offset = 204h) [reset = 0h]

Transfer Length Configuration Register
MMCHS_BLK[BLEN] is the block size register.
MMCHS_BLK[NBLK] is the block count register.
This register shall be used for any card.

Return to Summary Table

Table 5-1951. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0204h

Figure 5-955. MMC_BLK Name Register

31	30	29	28	27	26	25	24
NBLK							
R/W							
0h							
23	22	21	20	19	18	17	16
NBLK							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED				BLEN			
R				R/W			
0h				0h			
7	6	5	4	3	2	1	0
BLEN							
R/W							
0h							

Table 5-1952. MMC_BLK Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	NBLK	R/W	0h	Blocks count for current transfer This register is enabled when Block count Enable [MMCSD_CMD[BCE]] is set to 1 and is valid only for multiple block transfers. Setting the block count to 0 results no data blocks being transferred. Note: The host controller decrements the block count after each block transfer and stops when the count reaches zero. This register can be accessed only if no transaction is executing [i.e, after a transaction has stopped]. Read operations during transfers may return an invalid value and write operation will be ignored. In suspend context, the number of blocks yet to be transferred can be determined by Reading this register. When restoring transfer context prior to issuing a Resume command, The local host shall restore the previously saved block count. 0 Stop count 1 1 block 2 2 blocks 65535 65535 blocks
15:12	RESERVED	R	0h	

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Table 5-1952. MMC_BLK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	BLEN	R/W	0h	Transfer Block Size. This register specifies the block size for block data transfers. Read operations during transfers may return an invalid value, and write operations are ignored. When a CMD12 command is issued to stop the transfer, a read of the BLEN field after transfer completion [MMCSD_STAT[TC] set to 1] will not return the true byte number of data length while the stop occurs but the value written in this register before transfer is launched. 0 No data transfer 1 1 byte block length 2 2 bytes block length 3 3 bytes block length 511 511 bytes block length 512 512 bytes block length 2047 2047 bytes block length 2048 2048 bytes block length

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5.14.2.11 MMC_ARG Register

5.14.2.11.1 MMC_ARG Register (Offset = 208h) [reset = 0h]

Command Argument Register
This register contains command argument specified as bit 39-8 of Command-Format
These registers must be initialized prior to sending the command itself to the card (write action into the register MMCHS_CMD register). Only exception is for a command index specifying stuff bits in arguments, making a write unnecessary.

Return to Summary Table

Table 5-1953. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0208h

Figure 5-956. MMC_ARG Name Register

31	30	29	28	27	26	25	24
ARG							
R/W							
0h							
23	22	21	20	19	18	17	16
ARG							
R/W							
0h							
15	14	13	12	11	10	9	8
ARG							
R/W							
0h							
7	6	5	4	3	2	1	0
ARG							
R/W							
0h							

Table 5-1954. MMC_ARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ARG	R/W	0h	Command argument bits [31:0]

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5.14.2.12 MMC_CMD Register

5.14.2.12.1 MMC_CMD Register (Offset = 20Ch) [reset = 0h]

Command and Transfer Mode Register
MMCHS_CMD[31:16] = the command register
MMCHS_CMD[15:0] = the transfer mode.
This register configures the data and command transfers. A write into the most significant byte send the command. A write into MMCHS_CMD[15:0] registers during data transfer has no effect.
This register shall be used for any card.
Note: In SYSTEST mode, a write into MMCHS_CMD register will not start a transfer.

Return to Summary Table

Table 5-1955. Instance Table

Instance Name	Physical Address
MMCSD0	4830 020Ch

Figure 5-957. MMC_CMD Name Register

31	30	29	28	27	26	25	24
RESERVED2		INDX					
R		R/W					
0h		0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CMD_TYPE		DP	CICE	CCCE	RESERVED1	RSP_TYPE	
R/W		R/W	R/W	R/W	R	R/W	
0h		0h	0h	0h	0h	0h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		MSBS	DDIR	ACEN		BCE	DE
R		R/W	R/W	R/W		R/W	R/W
0h		0h	0h	0h		0h	0h

Table 5-1956. MMC_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED2	R	0h	

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Table 5-1956. MMC_CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29:24	INDX	R/W	0h	Command index Binary encoded value from 0 to 63 specifying the command number send to card 0 CMD0 or ACMD0 1 CMD1 or ACMD1 2 CMD2 or ACMD2 3 CMD3 or ACMD3 4 CMD4 or ACMD4 5 CMD5 or ACMD5 6 CMD6 or ACMD6 7 CMD7 or ACMD7 8 CMD8 or ACMD8 9 CMD9 or ACMD9 10 CMD10 or ACMD10 11 CMD11 or ACMD11 12 CMD12 or ACMD12 13 CMD13 or ACMD13 14 CMD14 or ACMD14 15 CMD15 or ACMD15 16 CMD16 or ACMD16 17 CMD17 or ACMD17 18 CMD18 or ACMD18 19 CMD19 or ACMD19 20 CMD20 or ACMD20 21 CMD21 or ACMD21 22 CMD22 or ACMD22 23 CMD23 or ACMD23 24 CMD24 or ACMD24 25 CMD25 or ACMD25 26 CMD26 or ACMD26 27 CMD27 or ACMD27 28 CMD28 or ACMD28 29 CMD29 or ACMD29 30 CMD30 or ACMD30 31 CMD31 or ACMD31 32 CMD32 or ACMD32 33 CMD33 or ACMD33 34 CMD34 or ACMD34 35 CMD35 or ACMD35 36 CMD36 or ACMD36 37 CMD37 or ACMD37 38 CMD38 or ACMD38 39 CMD39 or ACMD39 40 CMD40 or ACMD40 41 CMD41 or ACMD41 42 CMD42 or ACMD42 43 CMD43 or ACMD43 44 CMD44 or ACMD44 45 CMD45 or ACMD45 46 CMD46 or ACMD46 47 CMD47 or ACMD47 48 CMD48 or ACMD48 49 CMD49 or ACMD49 50 CMD50 or ACMD50 51 CMD51 or ACMD51 52 CMD52 or ACMD52 53 CMD53 or ACMD53 54 CMD54 or ACMD54 55 CMD55 or ACMD55 56 CMD56 or ACMD56 57 CMD57 or ACMD57 58 CMD58 or ACMD58 59 CMD59 or ACMD59 60 CMD60 or ACMD60 61 CMD61 or ACMD61 62 CMD62 or ACMD62 63 CMD63 or ACMD63

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Table 5-1956. MMC_CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23:22	CMD_TYPE	R/W	0h	Command type This register specifies three types of special command: Suspend, Resume and Abort. These bits shall be set to 00bfor all other commands. 0 Others Commands 1 CMD52 for writing "Bus Suspend" in CCCR 2 CMD52 for writing "Function Select" in CCCR 3 Abort command CMD12, CMD52 for writing " I/O Abort" in CCCR
21	DP	R/W	0h	Data present select This register indicates that data is present and DAT line shall be used. It must be set to 0 in the following conditions: - command using only CMD line - command with no data transfer but using busy signal on DAT[0] - Resume command 0 Command with no data transfer 1 Command with data transfer
20	CICE	R/W	0h	Command Index check enable This bit must be set to 1 to enable index check on command response to compare the index field in the response against the index of the command. If the index is not the same in the response as in the command, it is reported as a command index error [MMCSD_STAT[CIE] set to1] Note: The register CICE cannot be configured for an Auto CMD12, then index check is automatically checked when this command is issued. 0 Index check disable 1 Index check enable
19	CCCE	R/W	0h	Command CRC check enable This bit must be set to 1 to enable CRC7 check on command response to protect the response against transmission errors on the bus. If an error is detected, it is reported as a command CRC error [MMCSD_STAT[CCRC] set to 1]. Note: The register CCCE cannot be configured for an Auto CMD12, and then CRC check is automatically checked when this command is issued. 0 CRC7 check disable 1 CRC7 check enable
18	RESERVED1	R	0h	
17:16	RSP_TYPE	R/W	0h	Response type This bits defines the response type of the command 0 No response 1 Response Length 136 bits 2 Response Length 48 bits 3 Response Length 48 bits with busy after response
15:6	RESERVED	R	0h	
5	MSBS	R/W	0h	Multi/Single block select This bit must be set to 1 for data transfer in case of multi block command. For any others command this bit shall be set to 0. 0 Single block. If this bit is 0, it is not necessary to set the register MMCHS_BLK[NBLK]. 1 Multi block. When Block Count is disabled (MMCHS_CMD[BCE] is set to 0) in Multiple block transfers (MMCHS_CMD[MSBS] is set to 1), the module can perform infinite transfer.

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Table 5-1956. MMC_CMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DDIR	R/W	0h	Data transfer Direction Select This bit defines either data transfer will be a read or a write. 0 Data Write (host to card) 1 Data Read (card to host)
3:2	ACEN	R/W	0h	Auto CMD Enable - SD card only. This field determines use of auto command functions. There are two methods to stop Multiple-block read and write operation [1] Auto CMD12 Enable When this field is set to 01b the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the Auto CMD Error Status register. The Host Driver shall not set this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. [2] Auto CMD23 Enable When this bit field is set to 10b the Host Controller issues a CMD23 automatically before issuing a command specified in the Command Register. The Host Controller Version 3.00 and later shall support this function. The following conditions are required to use the Auto CMD23. Auto CMD23 Supported [Host Controller Version is 3.00 or later] A memory card that supports CMD23 [SCR[33]=1] If DMA is used, it shall be ADMA. Only when CMD18 or CMD25 is issued [Note, the Host Controller does not check command index.] Auto CMD23 can be used with or without ADMA. By Writing the Command register, the Host Controller issues a CMD23 first and then issues a command specified by the Command Index in Command register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the Auto CMD Error Status register. 32-bit block count value for CMD23 is set to SDMA System Address / Argument 2 register. 0 Auto Command Disabled 1 Auto CMD12 enable or CCS detection enabled. 2 Auto CMD23 Enable 3 Reserved
1	BCE	R/W	0h	Block Count Enable Multiple block transfers only. This bit is used to enable the block count register [MMCSD_BLK[NBLK]]. When Block Count is disabled [MMCSD_CMD[BCE] is set to 0] in Multiple block transfers [MMCSD_CMD[MSBS] is set to 1], the module can perform infinite transfer. 0 Block count disabled for infinite transfer. 1 Block count enabled for multiple block transfer with known number of blocks
0	DE	R/W	0h	DMA Enable This bit is used to enable DMA mode for host data access. 0 DMA mode disable 1 DMA mode enable

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5.14.2.13 MMC_RSP10 Register

5.14.2.13.1 MMC_RSP10 Register (Offset = 210h) [reset = 0h]

Command Response[31:0] Register
This 32-bit register holds bits positions [31:0] of command response type R1/R1b/R2/R3/R4/R5/R5b/R6.

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Table 5-1957. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0210h

Figure 5-958. MMC_RSP10 Name Register

31	30	29	28	27	26	25	24
RSP1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RSP1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RSP0							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSP0							
R							
0h							

Table 5-1958. MMC_RSP10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSP1	R	0h	Command Response [31:16]
15:0	RSP0	R	0h	Command Response [15:0]

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5.14.2.14 MMC_RSP32 Register

5.14.2.14.1 MMC_RSP32 Register (Offset = 214h) [reset = 0h]

Command Response[63:32] Register
This 32-bit register holds bits positions [63:32] of command response type R2.

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Table 5-1959. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0214h

Figure 5-959. MMC_RSP32 Name Register

31	30	29	28	27	26	25	24
RSP3							
R							
0h							
23	22	21	20	19	18	17	16
RSP3							
R							
0h							
15	14	13	12	11	10	9	8
RSP2							
R							
0h							
7	6	5	4	3	2	1	0
RSP2							
R							
0h							

Table 5-1960. MMC_RSP32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSP3	R	0h	Command Response [63:48]
15:0	RSP2	R	0h	Command Response [47:32]

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5.14.2.15 MMC_RSP54 Register

5.14.2.15.1 MMC_RSP54 Register (Offset = 218h) [reset = 0h]

Command Response[95:64] Register
This 32-bit register holds bits positions [95:64] of command response type R2.

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Table 5-1961. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0218h

Figure 5-960. MMC_RSP54 Name Register

31	30	29	28	27	26	25	24
RSP5							
R							
0h							
23	22	21	20	19	18	17	16
RSP5							
R							
0h							
15	14	13	12	11	10	9	8
RSP4							
R							
0h							
7	6	5	4	3	2	1	0
RSP4							
R							
0h							

Table 5-1962. MMC_RSP54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSP5	R	0h	Command Response [95:80]
15:0	RSP4	R	0h	Command Response [79:64]

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5.14.2.16 MMC_RSP76 Register

5.14.2.16.1 MMC_RSP76 Register (Offset = 21Ch) [reset = 0h]

Command Response[127:96] Register
This 32-bit register holds bits positions [127:96] of command response type R1(Auto CMD23)/R1b(Auto CMD12)/R2.

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Table 5-1963. Instance Table

Instance Name	Physical Address
MMCSD0	4830 021Ch

Figure 5-961. MMC_RSP76 Name Register

31	30	29	28	27	26	25	24
RSP7							
R							
0h							
23	22	21	20	19	18	17	16
RSP7							
R							
0h							
15	14	13	12	11	10	9	8
RSP6							
R							
0h							
7	6	5	4	3	2	1	0
RSP6							
R							
0h							

Table 5-1964. MMC_RSP76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RSP7	R	0h	Command Response [127:112]
15:0	RSP6	R	0h	Command Response [111:96]

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5.14.2.17 MMC_DATA Register

5.14.2.17.1 MMC_DATA Register (Offset = 220h) [reset = 0h]

Data Register
This register is the 32-bit entry point of the buffer for read or write data transfers.
The buffer size is 32bits x256(1024 bytes). Bytes within a word are stored and read in little endian format. This buffer can be used as two 512 byte buffers to transfer data efficiently without reducing the throughput.
Sequential and contiguous access is necessary to increment the pointer correctly. Random or skipped access is not allowed. In little endian, if the local host accesses this register byte-wise or 16bit-wise, the least significant byte (bits [7:0]) must always be written/read first. The update of the buffer address is done on the most significant byte write for full 32-bit DATA register or on the most significant byte of the last word of block transfer.
Example 1: Byte or 16-bit access
Mbyteen[3:0]=0001 (1-byte) => Mbyteen[3:0]=0010 (1-byte) => Mbyteen[3:0]=1100 (2-bytes) OK
Mbyteen[3:0]=0001 (1-byte) => Mbyteen[3:0]=0010 (1-byte) => Mbyteen[3:0]=0100 (1-byte) OK
Mbyteen[3:0]=0001 (1-byte) => Mbyteen[3:0]=0010 (1-byte) => Mbyteen[3:0]=1000 (1-byte) Bad .

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Table 5-1965. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0220h

Figure 5-962. MMC_DATA Name Register

31	30	29	28	27	26	25	24
DATA							
R/W							
0h							
23	22	21	20	19	18	17	16
DATA							
R/W							
0h							
15	14	13	12	11	10	9	8
DATA							
R/W							
0h							
7	6	5	4	3	2	1	0
DATA							
R/W							
0h							

Table 5-1966. MMC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DATA	R/W	0h	Data Register [31:0] In functional mode [MMCSD_CON[MODE] set to the default value 0] , A read access to this register is allowed only when the buffer read enable status is set to 1 [MMCSD_PSTATE[BRE]], otherwise a bad access [MMCSD_STAT[BADA]] is signaled. A write access to this register is allowed only when the buffer write enable status is set to 1[MMCSD_STATE[BWE]], otherwise a bad access [MMCSD_STAT[BADA]] is signaled and the data is not written.

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5.14.2.18 MMC_PSTATE Register

5.14.2.18.1 MMC_PSTATE Register (Offset = 224h) [reset = 40000h]

Present State Register
The Host can get status of the Host Controller from this 32-bit read only register.

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Table 5-1967. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0224h

Figure 5-963. MMC_PSTATE Name Register

31	30	29	28	27	26	25	24
RESERVED2							CLEV
R							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DLEV				WP	CDPL	CSS	CINS
R				R	R	R	R
0h				0h	1h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1				BRE	BWE	RTA	WTA
R				R	R	R	R
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				RTR	DLA	DATI	CMDI
R				R	R	R	R
0h				0h	0h	0h	0h

Table 5-1968. MMC_PSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED2	R	0h	
24	CLEV	R	0h	CMD line signal level This status is used to check the CMD line level to recover from errors, and for debugging. The value of this register after reset depends on the CMD line level at that time. 0 The CMD line level is 0. 1 The CMD line level is 1.
23:20	DLEV	R	0h	DAT[3:0] line signal level DAT[3] => bit 23 DAT[2] => bit 22 DAT[1] => bit 21 DAT[0] => bit 20 This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. The value of these registers after reset depends on the DAT lines level at that time.

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Table 5-1968. MMC_PSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	WP	R	0h	Write protect switch pin level For SDIO cards only. This bit reflects the write protect input pin [SDWP] level. The value of this register after reset depends on the protect input pin [SDWP] level at that time. 0 If MMCHS_CON[WPP] is set to 0 (default), the card is write protected, otherwise the card is not protected. 1 If MMCHS_CON[WPP] is set to 0 (default), the card is not write protected, otherwise the card is protected.
18	CDPL	R	1h	Card detect pin level This bit reflects the inverse value of the card detect input pin [SDCD], debouncing is not performed on this bit and bit is valid only when Card State Stable [MMCSD_PSTAE[CSS]] is set to 1. Use of this bit is limited to testing since it must be debounced y software. The value of this register after reset depends on the card detect input pin [SDCD] level at that time. 0 The value of the card detect input pin (SDCD) is 1 1 The value of the card detect input pin (SDCD) is 0
17	CSS	R	0h	Card State Stable This bit is used for testing. It is set to 1 only when Card Detect Pin Level is stable [MMCSD_PSTATE[CDPL]]. Debouncing is performed on the card detect input pin [SDCD] to detect card stability. This bit is not affected by a software reset. 0 Reset or Debouncing 1 No card or card inserted
16	CINS	R	0h	Card inserted This bit is the debounced value of the card detect input pin [SDCD]. An inactive to active transition of the card detect input pin [SDCD] will generate a card insertion interrupt [MMCSD_STAT[CINS]]. A active to inactive transition of the card detect input pin [SDCD] will generate a card removal interrupt [MMCSD_STAT[REM]]. This bit is not affected by a software reset. 0 If MMCHS_CON[CDP] is set to 1, no card is detected. The card may have been removed from the card slot. If MMCHS_CON[CDP] is set to 0, the card has been inserted. 1 If MMCHS_CON[CDP] is set to 1, the card has been inserted from the card slot. If MMCHS_CON[CDP] is set to 0 no card is detected. The card may have been removed from the card slot.
15:12	RESERVED1	R	0h	
11	BRE	R	0h	Buffer read enable This bit is used for non-DMA read transfers. It indicates that a complete block specified by MMCSD_BLK[BLEN] has been written in the buffer and is ready to be read. It is set to 0 when the entire block is read from the buffer. It is set to 1 when a block data is ready in the buffer and generates the Buffer read ready status of interrupt [MMCSD_STAT[BRR]]. 0 Read BLEN bytes disable 1 Read BLEN bytes enable. Readable data exists in the buffer.

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Table 5-1968. MMC_PSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	BWE	R	0h	Buffer Write enable This status is used for non-DMA write transfers. It indicates if space is available for write data. 0 There is no room left in the buffer to write BLEN bytes of data. 1 There is enough space in the buffer to write BLEN bytes of data.
9	RTA	R	0h	Read transfer active This status is used for detecting completion of a read transfer. It is set to 1 after the end bit of read command or by activating a continue request [MMCSD_HCTL[CR]] following a stop at block gap request. This bit is set to 0 when all data have been read by the local host after last block or after a stop at block gap request. 0 No valid data on the DAT lines. 1 read data transfer on going.
8	WTA	R	0h	Write transfer active This status indicates a write transfer active. It is set to 1 after the end bit of write command or by activating a continue request [MMCSD_HCTL[CR]] following a stop at block gap request. This bit is set to 0 when CRC status has been received after last block or after a stop at block gap request. 0 No valid data on the DAT lines. 1 Write data transfer on going.
7:4	RESERVED	R	0h	
3	RTR	R	0h	Re-Tuning Request Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to Normal Interrupt Status registers for more detail. This bit isn't set to 1 if Sampling Clock Select in the Host Control 2 register is set to 0 [using fixed sampling clock]. Refer to Re-Tuning Modes in the Capabilities register for more detail. 0 Fixed or well tuned sampling clock 1 Sampling clock needs re-tuning
2	DLA	R	0h	DAT line active This status bit indicates whether one of the DAT line is in use. In the case of read transactions [card to host]: This bit is set to 1 after the end bit of read command or by activating continue request MMCSD_HCTL[CR]. This bit is set to 0 when the host controller received the end bit of the last data block or at the beginning of the read wait mode. In the case of write transactions [host to card]: This bit is set to 1 after the end bit of write command or by activating continue request MMCSD_HCTL[CR]. This bit is set to 0 on the end of busy event for the last block; host controller must wait 8 clock cycles with line not busy to really consider not "busy state" or after the busy block as a result of a stop at gap request. 0 DAT Line inactive 1 DAT Line active

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Table 5-1968. MMC_PSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DATI	R	0h	Command inhibit[DAT] This status bit is generated if either DAT line is active [MMCSD_PSTATE[DLA]] or Read transfer is active [MMCSD_PSTATE[RTA]] or when a command with busy is issued. This bit prevents the local host to issue a command. A change of this bit from 1 to 0 generates a transfer complete interrupt [MMCSD_STAT[TC]]. 0 Issuing of command using the DAT lines is allowed 1 Issuing of command using DAT lines is not allowed
0	CMDI	R	0h	Command inhibit[CMD] This status bit indicates that the CMD line is in use. This bit is set to 0 when the most significant byte is written into the command register. This bit is not set when Auto CMD12 is transmitted. This bit is set to 0 in either the following cases: - After the end bit of the command response, excepted if there is a command conflict error [MMCSD_STAT[CCRC] or MMCSD_STAT[CEB] set to 1] or a Auto CMD12 is not executed [MMCSD_AC12[ACNE]]. - After the end bit of the command without response [MMCSD_CMD[RSP_TYPE] set to "00"] In case of a command data error is detected [MMCSD_STAT[CTO] set to 1], this register is not automatically cleared. 0 Issuing of command using CMD line is allowed 1 Issuing of command using CMD line is not allowed

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5.14.2.19 MMC_HCTL Register

5.14.2.19.1 MMC_HCTL Register (Offset = 228h) [reset = 0h]

Host Control Register
This register defines the host controls to set power, wakeup and transfer parameters.
MMCHS_HCTL[31:24] = Wakeup control
MMCHS_HCTL[23:16] = Block gap control
MMCHS_HCTL[15:8] = Power control
MMCHS_HCTL[7:0] = Host control.

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Table 5-1969. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0228h

Figure 5-964. MMC_HCTL Name Register

31	30	29	28	27	26	25	24
RESERVED3				OBWE	REM	INS	IWE
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
23	22	21	20	19	18	17	16
RESERVED2				IBG	RWC	CR	SBGR
R				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED1				SDVS			SDBP
R				R/W			R/W
0h				0h			0h
7	6	5	4	3	2	1	0
CDSS	CDTL	RESERVED	DMAS		HSPE	DTW	LED
R/W	R/W	R	R/W		R/W	R/W	R
0h	0h	0h	0h		0h	0h	0h

Table 5-1970. MMC_HCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED3	R	0h	
27	OBWE	R/W	0h	Wakeup event enable for 'Out-of-Band' Interrupt. This bit enables wakeup events for 'Out-of-Band' assertion. Wakeup is generated if the wakeup feature is enabled [MMCSD_SYSCONFIG[ENAWAKEUP]]. The write to this register is ignored when MMCSD_CON[OBIE] is not set. 0 Disable wakeup on 'Out-of-Band' Interrupt 1 Enable wakeup on 'Out-of-Band' Interrupt
26	REM	R/W	0h	Wakeup event enable on SD card removal This bit enables wakeup events for card removal assertion. Wakeup is generated if the wakeup feature is enabled [MMCSD_SYSCONFIG[ENAWAKEUP]]. 0 Disable wakeup on card removal 1 Enable wakeup on card removal

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Table 5-1970. MMC_HCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	INS	R/W	0h	Wakeup event enable on SD card insertion This bit enables wakeup events for card insertion assertion. Wakeup is generated if the wakeup feature is enabled [MMCSD_SYSCONFIG[ENAWAKEUP]]. 0 Disable wakeup on card insertion 1 Enable wakeup on card insertion
24	IWE	R/W	0h	Wakeup event enable on SD card interrupt This bit enables wakeup events for card interrupt assertion. Wakeup is generated if the wakeup feature is enabled [MMCSD_SYSCONFIG[ENAWAKEUP]]. 0 Disable wakeup on card interrupt 1 Enable wakeup on card interrupt
23:20	RESERVED2	R	0h	
19	IBG	R/W	0h	Interrupt block at gap This bit is valid only in 4-bit mode of SDIO card to enable interrupt detection in the interrupt cycle at block gap for a multiple block transfer. For MMC cards and for SD card this bit should be set to 0. 0 Disable interrupt detection at the block gap in 4-bit mode 1 Enable interrupt detection at the block gap in 4-bit mode
18	RWC	R/W	0h	Read wait control The read wait function is optional only for SDIO cards. If the card supports read wait, this bit must be enabled, then requesting a stop at block gap [MMCSD_HCTL[SBGR]] generates a read wait period after the current end of block. Be careful, if read wait is not supported it may cause a conflict on DAT line. 0 Disable Read Wait Control. Suspend/Resume cannot be supported. 1 Enable Read Wait Control
17	CR	R/W	0h	Continue request This bit is used to restart a transaction that was stopped by requesting a stop at block gap [MMCSD_HCTL[SBGR]]. Set this bit to 1 restarts the transfer. The bit is automatically set to 0 by the host controller when transfer has restarted i.e DAT line is active [MMCSD_PSTATE[DLA]] or transferring data [MMCSD_PSTATE[WTA]]. The Stop at block gap request must be disabled [MMCSD_HCTL[SBGR]=0] before setting this bit. 0 No affect 1 transfer restart
16	SBGR	R/W	0h	Stop at block gap request This bit is used to stop executing a transaction at the next block gap. The transfer can restart with a continue request [MMHS_HCTL[CR]] or during a suspend/resume sequence. In case of read transfer, the card must support read wait control. In case of write transfer, the host driver shall set this bit after all block data written. Until the transfer completion [MMCSD_STAT[TC] set to 1], the host driver shall leave this bit set to 1. If this bit is set, the local host shall not write to the data register [MMCSD_DATA]. 0 Transfer mode 1 Stop at block gap
15:12	RESERVED1	R	0h	

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Table 5-1970. MMC_HCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:9	SDVS	R/W	0h	SD bus voltage select All cards. The host driver should set to these bits to select the voltage level for the card according to the voltage supported by the system [MMCSD_CAPA[VS18,VS30,VS33]] before starting a transfer. 5 1.8V (Typical) 6 3.0V (Typical) 7 3.3V (Typical)
8	SDBP	R/W	0h	SD bus power Before setting this bit, the host driver shall select the SD bus voltage [MMCSD_HCTL[SDVS]]. If the host controller detects the No card state, this bit is automatically set to 0. If the module is power off, a write in the command register [MMCSD_CMD] will not start the transfer. A write to this bit has no effect if the selected SD bus voltage MMCSD_HCTL[SDVS] is not supported according to capability register [MMCSD_CAPA[VS*]]. 0 Power off 1 Power on
7	CDSS	R/W	0h	Card Detect Signal Selection This bit selects source for the card detection.When the source for the card detection is switched, the interrupt should be disabled during the switching period by clearing the Interrupt Status/Signal Enable register in order to mask unexpected interrupt being caused by the glitch. The Interrupt Status/Signal Enable should be disabled during over the period of debouncing. 0 SDCD# is selected (for normal use) 1 The Card Detect Test Level is selected (for test purpose)
6	CDTL	R/W	0h	Card Detect Test Level: This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. 0 No Card 1 Card Inserted
5	RESERVED	R	0h	
4:3	DMAS	R/W	0h	DMA Select Mode: One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. Use of selected DMA is determined by DMA Enable of the Transfer Mode register. This register is only meaningful when MADMA_EN is set to 1. When MADMA_EN is set to 0 the bit field is read only and returned value is 0. 0 Reserved 1 Reserved 2 32-bit Address ADMA2 is selected 3 Reserved
2	HSPE	R/W	0h	High Speed Enable: Before setting this bit, the Host Driver shall check the High Speed Support in the Capabilities register. If this bit is set to 0 [default], the Host Controller outputs CMD line and DAT lines at the falling edge of the SD Clock. If this bit is set to 1, the Host Controller outputs CMD line and DAT lines at the rising edge of the SD Clock.This bit shall not be set when dual data rate mode is activated in MMCSD_CON[DDR]. 0 Normal speed mode 1 High speed mode

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Table 5-1970. MMC_HCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DTW	R/W	0h	Data transfer width For MMC card, this bit must be set following a valid SWITCH command [CMD6] with the correct value and extend CSD index written in the argument. Prior to this command, the MMC card configuration register [CSD and EXT_CSD] must be verified for compliance with MMC standard specification 4.x [see section 3.6]. This register has no effect when the MMC 8-bit mode is selected [register MMCSD_CON[DW8] set to1], For SD/SDIO cards, this bit must be set following a valid SET_BUS_WIDTH command [ACMD6] with the value written in bit 1 of the argument. Prior to this command, the SD card configuration register [SCR] must be verified for the supported bus width by the SD card. 0 1-bit Data width (DAT[0] used) 1 4-bit Data width (DAT[3:0] used)
0	LED	R	0h	Reserved bit. LED control feature is not supported This bit is initialized to zero, and writes to it are ignored.

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5.14.2.20 MMC_SYSCTL Register

5.14.2.20.1 MMC_SYSCTL Register (Offset = 22Ch) [reset = 0h]

SD System Control Register
This register defines the system controls to set software resets, clock frequency management and data timeout.
MMCHS_SYSCTL[31:24] = Software resets
MMCHS_SYSCTL[23:16] = Timeout control
MMCHS_SYSCTL[15:0] = Clock control.

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Table 5-1971. Instance Table

Instance Name	Physical Address
MMCSD0	4830 022Ch

Figure 5-965. MMC_SYSCTL Name Register

31	30	29	28	27	26	25	24
RESERVED2					SRD	SRC	SRA
R					R/W	R/W	R/W
0h					0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1				DTO			
R				R/W			
0h				0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKD							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CLKD		CGS	RESERVED		CEN	ICS	ICE
R/W		R	R		R/W	R	R/W
0h		0h	0h		0h	0h	0h

Table 5-1972. MMC_SYSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:27	RESERVED2	R	0h	
26	SRD	R/W	0h	Software reset for DAT line This bit is set to 1 for reset and released to 0 when completed. DAT finite state machine in both clock domain are also reset. Here below are the registers cleared by MMCSD_SYSCTL[SRD]: - MMCSD_DATA - MMCSD_PSTATE: BRE, BWE, RTA, WTA, DLA and DATI - MMCSD_HCTL: SBGR and CR - MMCSD_STAT: BRR, BWR, BGE and TC OCP and MMC buffer data management is reinitialized. 0 Reset completed 1 Software reset for DAT line
25	SRC	R/W	0h	Software reset for CMD line This bit is set to 1 for reset and released to 0 when completed. CMD finite state machine in both clock domain are also reset. Here below the registers cleared by MMCSD_SYSCTL[SRC]: - MMCSD_PSTATE: CMDI - MMCSD_STAT: CC OCP and MMC command status management is reinitialized. 0 Reset completed 1 Software reset for CMD line

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Table 5-1972. MMC_SYSCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	SRA	R/W	0h	Software reset for all This bit is set to 1 for reset , and released to 0 when completed. This reset affects the entire host controller except for the card detection circuit and capabilities registers. 0 Reset completed 1 Software reset for all the design
23:20	RESERVED1	R	0h	
19:16	DTO	R/W	0h	Data timeout counter value and busy timeout. This value determines the interval by which DAT lines timeouts are detected. The host driver needs to set this bitfield based on - the maximum read access time [NAC] [Refer to the SD Specification Part1 Physical Layer], - the data read access time values [TAAC and NSAC] in the card specific data register [CSD] of the card, - the timeout clock base frequency [MMCSD_CAPA[TCF]]. If the card does not respond within the specified number of cycles, a data timeout error occurs [MMCSD_STA[DTO]]. The MMCSD_SYSCTL[DTO] register is also used to check busy duration, to generate busy timeout for commands with busy response or for busy programming during a write command. Timeout on CRC status is generated if no CRC token is present after a block write. 0 TCF x 2^13 1 TCF x 2^14 14 TCF x 2^27 15 Reserved
15:6	CLKD	R/W	0h	Clock frequency select These bits define the ratio between a reference clock frequency [system dependant] and the output clock frequency on the CLK pin of either the memory card [MMC, SD or SDIO]. 0 Clock Ref bypass 1 Clock Ref bypass 2 Clock Ref / 2 3 Clock Ref / 3 1023 Clock Ref / 1023
5	CGS	R	0h	Clock Generator Select - For SD cards Host Controller Version 3.00 supports this bit. This bit is used to select the clock generator mode in SDCLK Frequency Select. If the Programmable Clock Mode is supported [non-zero value is set to Clock Multiplier in the Capabilities register], this bit attribute is RW, and if not supported, this bit attribute is RO and zero is read. This bit depends on the setting of Preset Value Enable in the Host Control 2 register. If the Preset Value Enable = 0, this bit is set by Host Driver. If the Preset Value Enable = 1, this bit is automatically set to a value specified in one of Preset Value registers.
4:3	RESERVED	R	0h	
2	CEN	R/W	0h	Clock enable This bit controls if the clock is provided to the card or not. 0 The clock is not provided to the card . Clock frequency can be changed . 1 The clock is provided to the card and can be automatically gated when MMCHS_SYSCONFIG[AUTOIDLE] is set to 1 (default value) . The host driver shall wait to set this bit to 1 until the Internal clock is stable (MMCHS_SYSCTL[ICS]).

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Table 5-1972. MMC_SYSCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ICS	R	0h	Internal clock stable [status] This bit indicates either the internal clock is stable or not. 0 The internal clock is not stable. 1 The internal clock is stable after enabling the clock (MMCHS_SYSCTL[ICE]) or after changing the clock ratio (MMCHS_SYSCTL[CLKD]).
0	ICE	R/W	0h	Internal clock enable This register controls the internal clock activity. In very low power state, the internal clock is stopped. Note: The activity of the debounce clock [used for wakeup events] and the OCP clock [used for reads and writes to the module register map] are not affected by this register. 0 The internal clock is stopped (very low power state). 1 The internal clock oscillates and can be automatically gated when MMCHS_SYSCONFIG[AUTOIDLE] is set to 1 (default value) .

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5.14.2.21 MMC_STAT Register

5.14.2.21.1 MMC_STAT Register (Offset = 230h) [reset = 0h]

Interrupt Status Register
The interrupt status regroups all the status of the module internal events that can generate an interrupt.
MMCHS_STAT[31:16] = Error Interrupt Status
MMCHS_STAT[15:0] = Normal Interrupt Status.

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Table 5-1973. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0230h

Figure 5-966. MMC_STAT Name Register

31	30	29	28	27	26	25	24
RESERVED3		BADA	CERR	RESERVED2	TE	ADMAE	ACE
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	22	21	20	19	18	17	16
CLE	DEB	DCRC	DTO	CIE	CEB	CCRC	CTO
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
ERRI	RESERVED				BSR	OBI	CIRQ
R	R				R/W	R/W	R
0h	0h				0h	0h	0h
7	6	5	4	3	2	1	0
CREM	CINS	BRR	BWR	DMA	BGE	TC	CC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1974. MMC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED3	R	0h	
29	BADA	R/W	0h	Bad access to data space This bit is set automatically to indicate a bad access to buffer when not allowed: -This bit is set during a read access to the data register [MMCSD_DATA] while buffer reads are not allowed [MMCSD_PSTATE[BRE] =0] -This bit is set during a write access to the data register [MMCSD_DATA] while buffer writes are not allowed [MMCSD_STATE[BWE] =0] 0 No Interrupt. 0 Status bit unchanged 1 Bad Access 1 Status is cleared

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Table 5-1974. MMC_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	CERR	R/W	0h	Card error This bit is set automatically when there is at least one error in a response of type R1, R1b, R6, R5 or R5b. Only bits referenced as type E[error] in status field in the response can set a card status error. An error bit in the response is flagged only if corresponding bit in card status response error MMCSD_CSRE in set. There is no card error detection for autoCMD12 command. The host driver shall read MMCSD_RSP76 register to detect error bits in the command response. 0 No Error 0 Status bit unchanged 1 Card error 1 Status is cleared
27	RESERVED2	R	0h	
26	TE	R/W	0h	Tuning Error This bit is set when an unrecoverable error is detected in a tuning circuit except during tuning procedure [Occurrence of an error during tuning procedure is indicated by Sampling Select]. By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning. To reset tuning circuit, Sampling Clock shall be set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Tuning Error, the Host Driver should discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from tuning circuit error. The bit is set if the lock is lost [but not during the tuning process] or if the lock counter expires without the lock being asserted. If the latter happens, the SW can decide to ignore the interrupt and wait some more for the lock to be set. 0 No Error 1 Error
25	ADMAE	R/W	0h	ADMA Error: This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register.In addition, the Host Controller generates this interrupt when it detects invalid descriptor data [Valid=0] at the ST_FDS state. ADMA Error State in the ADMA Error Status indicates that an error occurs in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor. 0 No Interrupt. 0 Status bit unchanged 1 ADMA error 1 Status is cleared
24	ACE	R/W	0h	Auto CMD error Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1. In case of Auto CMD12, this bit is set to 1, not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error. 0 No Error. 0 Status bit unchanged 1 Auto CMD error 1 Status is cleared
23	CLE	R	0h	Reserved. Current limit error is not supported. These bits are initialized to zero, and writes to them are ignored.

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Table 5-1974. MMC_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	DEB	R/W	0h	Data End Bit error This bit is set automatically when detecting a 0 at the end bit position of read data on DAT line or at the end position of the CRC status in write mode. 0 No Error 0 Status bit unchanged 1 Data end bit error 1 Status is cleared
21	DCRC	R/W	0h	Data CRC Error This bit is set automatically when there is a CRC16 error in the data phase response following a block read command or if there is a 3-bit CRC status different of a position "010" token during a block write command. 0 No Error. 0 Status bit unchanged 1 Data CRC error 1 Status is cleared
20	DTO	R/W	0h	Data timeout error This bit is set automatically according to the following conditions: - busy timeout for R1b, R5b response type - busy timeout after write CRC status - write CRC status timeout - read data timeout 0 No error. 0 Status bit unchanged 1 Time out 1 Status is cleared
19	CIE	R/W	0h	Command index error This bit is set automatically when response index differs from corresponding command index previously emitted. It depends on the enable in MMCSD_CMD[CICE] register. 0 No error. 0 Status bit unchanged 1 Command index error 1 Status is cleared
18	CEB	R/W	0h	Command end bit error This bit is set automatically when detecting a 0 at the end bit position of a command response. 0 No error. 0 Status bit unchanged 1 Command end bit error 1 Status is cleared
17	CCRC	R/W	0h	Command CRC Error This bit is set automatically when there is a CRC7 error in the command response depending on the enable in MMCSD_CMD[CCCE] register. 0 No Error. 0 Status bit unchanged 1 Command CRC error 1 Status is cleared
16	CTO	R/W	0h	Command Timeout Error This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command. For commands that reply within 5 clock cycles - the timeout is still detected at 64 clock cycles. 0 No error 0 Status bit unchanged 1 Time Out 1 Status is cleared

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Table 5-1974. MMC_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ERRI	R	0h	Error Interrupt If any of the bits in the Error Interrupt Status register [MMCSD_STAT[24:15]] are set, then this bit is set to 1. Therefore the host driver can efficiently test for an error by checking this bit first. Writes to this bit are ignored. 0 No Interrupt. 1 Error interrupt event(s) occurred
14:11	RESERVED	R	0h	
10	BSR	R/W	0h	Boot status received interrupt This bit is set automatically when MMCSD_CON[BOOT] is set 0x1 or 0x2 and a boot status is received on DAT[0] line. This interrupt is only useful for MMC card. 0 No Interrupt. 0 Status bit unchanged 1 Boot status received interrupt. 1 Status is cleared
9	OBI	R/W	0h	Out-Of-Band interrupt This bit is set automatically when MMCSD_CON[OBIE] is set and an Out-of-Band interrupt occurs on OBI pin. The interrupt detection depends on polarity controlled by MMCSD_CON[OBIP]. This interrupt is only useful for MMC card. The Out-of-Band interrupt signal is a system specific feature for future use, this signal is not required for existing specification implementation. 0 No Out-Of-Band interrupt. 0 Status bit unchanged 1 Interrupt Out-Of-Band occurs 1 Status is cleared
8	CIRQ	R	0h	Card interrupt This bit is only used for SD and SDIO and CE-ATA cards. In 1-bit mode, interrupt source is asynchronous [can be a source of asynchronous wakeup]. In 4-bit mode, interrupt source is sampled during the interrupt cycle. In CE-ATA mode, interrupt source is detected when the card drives CMD line to zero during one cycle after data transmission end.All modes above are fully exclusive. The controller interrupt must be clear by setting MMCSD_IE[CIRQ] to 0, then the host driver must start the interrupt service with card [clearing card interrupt status] to remove card interrupt source. Otherwise the Controller interrupt will be reasserted as soon as MMCSD_IE[CIRQ] is set to 1. Writes to this bit are ignored. 0 No card interrupt 1 Generate card interrupt
7	CREM	R/W	0h	Card removal This bit is set automatically when MMCSD_PSTATE[CINS] changes from 1 to 0. A clear of this bit doesn't effect Card inserted present state [MMCSD_PSTATE[CINS]]. 0 Card state stable or Debouncing 0 Status bit unchanged 1 Card removed 1 Status is cleared

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Table 5-1974. MMC_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CINS	R/W	0h	Card insertion This bit is set automatically when MMCSD_PSTATE[CINS] changes from 0 to 1. A clear of this bit doesn't effect Card inserted present state [MMCSD_PSTATE[CINS]]. 0 Card state stable or debouncing 0 Status bit unchanged 1 Card inserted 1 Status is cleared
5	BRR	R/W	0h	Buffer read ready This bit is set automatically during a read operation to the card [see class 2 - block oriented read commands] when one block specified by MMCSD_BLK[BLEN] is completely written in the buffer. It indicates that the memory card has filled out the buffer and that the local host needs to empty the buffer by Reading it. Note: If the DMA receive-mode is enabled, this bit is never set; instead a DMA receive request to the main DMA controller of the system is generated. 0 Not Ready to read buffer 0 Status bit unchanged 1 Ready to read buffer 1 Status is cleared
4	BWR	R/W	0h	Buffer write ready This bit is set automatically during a write operation to the card [see class 4 - block oriented write command] when the host can write a complete block as specified by MMCSD_BLK[BLEN]. It indicates that the memory card has emptied one block from the buffer and that the local host is able to write one block of data into the buffer. Note: If the DMA transmit mode is enabled, this bit is never set; instead, a DMA transmit request to the main DMA controller of the system is generated. 0 Not Ready to write buffer 0 Status bit unchanged 1 Ready to write buffer 1 Status is cleared
3	DMA	R/W	0h	DMA interrupt : This status is set when an interrupt is required in the ADMA instruction and after the data transfer completion. 0 Dma interrupt detected 0 Status bit unchanged 1 No dma interrupt 1 Status is cleared
2	BGE	R/W	0h	Block gap event When a stop at block gap is requested [MMCSD_HCTL[SBGR]], this bit is automatically set when transaction is stopped at the block gap during a read or write operation. This event does not occur when the stop at block gap is requested on the last block. In read mode, a 1-to-0 transition of the DAT Line active status [MMCSD_PSTATE[DLA]] between data blocks generates a Block gap event interrupt. 0 No block gap event 0 Status bit unchanged 1 Transaction stopped at block gap 1 Status is cleared

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Table 5-1974. MMC_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TC	R/W	0h	Transfer completed This bit is always set when a read/write transfer is completed or between two blocks when the transfer is stopped due to a stop at block gap request [MMCSD_HCTL[SBGR]]. In Read mode: This bit is automatically set on completion of a read transfer [MMCSD_PSTATE[RTA]]. In write mode: This bit is set automatically on completion of the DAT line use [MMCSD_PSTATE[DLA]]. 0 No transfer complete 0 Status bit unchanged 1 Data transfer complete 1 Status is cleared
0	CC	R/W	0h	Command complete This bit is set when a 1-to-0 transition occurs in the register command inhibit [MMCSD_PSTATE[CMDI]] If the command is a type for which no response is expected, then the command complete interrupt is generated at the end of the command. A command timeout error [MMCSD_STAT[CTO]] has higher priority than command complete [MMCSD_STAT[CC]]. If a response is expected but none is received, then a command timeout error is detected and signaled instead of the command complete interrupt. 0 No Command complete 0 Status bit unchanged 1 Command complete 1 Status is cleared

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5.14.2.22 MMC_IE Register

5.14.2.22.1 MMC_IE Register (Offset = 234h) [reset = 0h]

Interrupt Status Enable Register
This register allows to enable/disable the module to set status bits, on an event-by-event basis.
MMCHS_IE[31:16] = Error Interrupt Status Enable
MMCHS_IE[15:0] = Normal Interrupt Status Enable.

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Table 5-1975. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0234h

Figure 5-967. MMC_IE Name Register

31	30	29	28	27	26	25	24
RESERVED3		BADA_ENABLE	CERR_ENABLE	RESERVED2	TE_ENABLE	ADMAE_ENABLE	ACE_ENABLE
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLE	DEB_ENABLE	DCRC_ENABLE	DTO_ENABLE	CIE_ENABLE	CEB_ENABLE	CCRC_ENABLE	CTO_ENABLE
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NULL	RESERVED				BSR_ENABLE	OBI_ENABLE	CIRQ_ENABLE
R	R				R/W	R/W	R/W
0h	0h				0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CREM_ENABLE	CINS_ENABLE	BRR_ENABLE	BWR_ENABLE	DMA_ENABLE	BGE_ENABLE	TC_ENABLE	CC_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1976. MMC_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED3	R	0h	
29	BADA_ENABLE	R/W	0h	Bad access to data space Status Enable 0 Masked 1 Enabled
28	CERR_ENABLE	R/W	0h	Card Error Status Enable 0 Masked 1 Enabled
27	RESERVED2	R	0h	
26	TE_ENABLE	R/W	0h	Tuning Error Status Enable 0 Masked 1 Enabled
25	ADMAE_ENABLE	R/W	0h	ADMA Error Status Enable 0 Masked 1 Enabled

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Table 5-1976. MMC_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	ACE_ENABLE	R/W	0h	Auto CMD Error Status Enable 0 Masked 1 Enabled
23	CLE	R	0h	Reserved bit. Current limit error is not supported. These bits are initialized to zero, and writes to them are ignored.
22	DEB_ENABLE	R/W	0h	Data End Bit Error Status Enable 0 Masked 1 Enabled
21	DCRC_ENABLE	R/W	0h	Data CRC Error Status Enable 0 Masked 1 Enabled
20	DTO_ENABLE	R/W	0h	Data Timeout Error Status Enable 0 The data timeout detection is deactivated. The host controller provides the clock to the card until the card sends the data or the transfer is aborted. 1 The data timeout detection is enabled.
19	CIE_ENABLE	R/W	0h	Command Index Error Status Enable 0 Masked 1 Enabled
18	CEB_ENABLE	R/W	0h	Command End Bit Error Status Enable 0 Masked 1 Enabled
17	CCRC_ENABLE	R/W	0h	Command CRC Error Status Enable 0 Masked 1 Enabled
16	CTO_ENABLE	R/W	0h	Command Timeout Error Status Enable 0 Masked 1 Enabled
15	NULL	R	0h	Fixed to 0 The host driver shall control error interrupts using the Error Interrupt Signal Enable register. Writes to this bit are ignored
14:11	RESERVED	R	0h	
10	BSR_ENABLE	R/W	0h	Boot Status Enable A write to this register when MMCSD_CON[BOOT_ACK] is set to 0x0 is ignored. 0 Masked 1 Enabled
9	OBI_ENABLE	R/W	0h	Out-of-Band Status Enable A write to this register when MMCSD_CON[OBIE] is set to '0' is ignored. 0 Masked 1 Enabled
8	CIRQ_ENABLE	R/W	0h	Card Status Enable A clear of this bit also clears the corresponding status bit. During 1-bit mode, if the interrupt routine doesn't remove the source of a card interrupt in the SDIO card, the status bit is reasserted when this bit is set to 1. 0 Masked 1 Enabled
7	CREM_ENABLE	R/W	0h	Card Removal Status Enable 0 Masked 1 Enabled

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Table 5-1976. MMC_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CINS_ENABLE	R/W	0h	Card Insertion Status Enable 0 Masked 1 Enabled
5	BRR_ENABLE	R/W	0h	Buffer Read Ready Status Enable 0 Masked 1 Enabled
4	BWR_ENABLE	R/W	0h	Buffer Write Ready Status Enable 0 Masked 1 Enabled
3	DMA_ENABLE	R/W	0h	DMA Status Enable 0 Masked 1 Enabled
2	BGE_ENABLE	R/W	0h	Block Gap Event Status Enable 0 Masked 1 Enabled
1	TC_ENABLE	R/W	0h	Transfer Complete Status Enable 0 Masked 1 Enabled
0	CC_ENABLE	R/W	0h	Command Complete Status Enable 0 Masked 1 Enabled

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5.14.2.23 MMC_ISE Register

5.14.2.23.1 MMC_ISE Register (Offset = 238h) [reset = 0h]

Interrupt Signal Enable Register
This register allows to enable/disable the module internal sources of status, on an event-by-event basis.
MMCHS_ISE[31:16] = Error Interrupt Signal Enable
MMCHS_ISE[15:0] = Normal Interrupt Signal Enable.

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Table 5-1977. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0238h

Figure 5-968. MMC_ISE Name Register

31	30	29	28	27	26	25	24
RESERVED3		BADA_SIGEN	CERR_SIGEN	RESERVED2	TE_SIGEN	ADMAE_SIGEN	ACE_SIGEN
R		R/W	R/W	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CLE	DEB_SIGEN	DCRC_SIGEN	DTO_SIGEN	CIE_SIGEN	CEB_SIGEN	CCRC_SIGEN	CTO_SIGEN
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
NULL	RESERVED				BSR_SIGEN	OBI_SIGEN	CIRQ_SIGEN
R	R				R/W	R/W	R/W
0h	0h				0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CREM_SIGEN	CINS_SIGEN	BRR_SIGEN	BWR_SIGEN	DMA_SIGEN	BGE_SIGEN	TC_SIGEN	CC_SIGEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1978. MMC_ISE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED3	R	0h	
29	BADA_SIGEN	R/W	0h	Bad access to data space Signal Enable 0 `Masked` 1 `Enabled`
28	CERR_SIGEN	R/W	0h	Card Error Interrupt Signal Enable 0 `Masked` 1 `Enabled`
27	RESERVED2	R	0h	
26	TE_SIGEN	R/W	0h	Tuning Error Signal Enable 0 `Masked` 1 `Enabled`
25	ADMAE_SIGEN	R/W	0h	ADMA Error Signal Enable 0 `Masked` 1 `Enabled`
24	ACE_SIGEN	R/W	0h	Auto CMD Error Signal Enable 0 `Masked` 1 `Enabled`

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Table 5-1978. MMC_ISE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	CLE	R	0h	Reserved bit. Current limit error is not supported. These bits are initialized to zero, and writes to them are ignored.
22	DEB_SIGEN	R/W	0h	Data End Bit Error Signal Enable 0 Masked 1 Enabled
21	DCRC_SIGEN	R/W	0h	Data CRC Error Signal Enable 0 Masked 1 Enabled
20	DTO_SIGEN	R/W	0h	Data Timeout Error Signal Enable 0 Masked 1 Enabled
19	CIE_SIGEN	R/W	0h	Command Index Error Signal Enable 0 Masked 1 Enabled
18	CEB_SIGEN	R/W	0h	Command End Bit Error Signal Enable 0 Masked 1 Enabled
17	CCRC_SIGEN	R/W	0h	Command CRC Error Signal Enable 0 Masked 1 Enabled
16	CTO_SIGEN	R/W	0h	Command timeout Error Signal Enable 0 Masked 1 Enabled
15	NULL	R	0h	Fixed to 0 The host driver shall control error interrupts using the Error Interrupt Signal Enable register. Writes to this bit are ignored
14:11	RESERVED	R	0h	
10	BSR_SIGEN	R/W	0h	Boot Status Signal Enable A write to this register when MMCSD_CON[BOOT_ACK] is set to 0x0 is ignored. 0 Masked 1 Enabled
9	OBI_SIGEN	R/W	0h	Out-Of-Band Interrupt Signal Enable A write to this register when MMCSD_CON[OBIE] is set to '0' is ignored. 0 Masked 1 Enabled
8	CIRQ_SIGEN	R/W	0h	Card Interrupt Signal Enable 0 Masked 1 Enabled
7	CREM_SIGEN	R/W	0h	Card Removal Signal Enable 0 Masked 1 Enabled
6	CINS_SIGEN	R/W	0h	Card Insertion Signal Enable 0 Masked 1 Enabled
5	BRR_SIGEN	R/W	0h	Buffer Read Ready Signal Enable 0 Masked 1 Enabled

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Table 5-1978. MMC_ISE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	BWR_SIGEN	R/W	0h	Buffer Write Ready Signal Enable 0 Masked 1 Enabled
3	DMA_SIGEN	R/W	0h	DMA Interrupt Signal Enable 0 Masked 1 Enabled
2	BGE_SIGEN	R/W	0h	Black Gap Event Signal Enable 0 Masked 1 Enabled
1	TC_SIGEN	R/W	0h	Transfer Completed Status Enable 0 Masked 1 Enabled
0	CC_SIGEN	R/W	0h	Command Complete Status Enable 0 Masked 1 Enabled

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5.14.2.24 MMC_AC12 Register

5.14.2.24.1 MMC_AC12 Register (Offset = 23Ch) [reset = 0h]

Host Control 2 Register and Auto CMD Error Status Register
This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD23. The Host driver can determine what kind of Auto CMD12 / CMD23 errors occur by this register. Auto CMD23 errors are indicated in bit 04-01.This register is valid only when the Auto CMD Error is set.

Return to Summary Table

Table 5-1979. Instance Table

Instance Name	Physical Address
MMCSD0	4830 023Ch

Figure 5-969. MMC_AC12 Name Register

31	30	29	28	27	26	25	24
PV_ENABLE	AI_ENABLE	RESERVED2					
R/W	R/W	R					
0h	0h	0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SCLK_SEL	ET	DS_SEL		V1V8_SIGEN	UHSMS		
R/W	R/W	R/W		R/W	R/W		
0h	0h	0h		0h	0h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CNI	RESERVED		ACIE	ACEB	ACCE	ACTO	ACNE
R	R		R	R	R	R	R
0h	0h		0h	0h	0h	0h	0h

Table 5-1980. MMC_AC12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PV_ENABLE	R/W	0h	Preset Value Enable Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set, automatic SDCLK frequency generation and driver strength selection is performed without considering system specific conditions. This bit enables the functions defined in the Preset Value registers. If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers. 0 `SDCLK and Driver Strength are controlled by Host Driver.` 1 `Automatic Selection by Preset Value are Enabled.`

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Table 5-1980. MMC_AC12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	AI_ENABLE	R/W	0h	Asynchronous Interrupt Enable This bit can be set to 1 if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode [and zero is set to Interrupt Pin Select in the Shared Bus Control register]. If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver the Card Interrupt to the host when it is asserted by the Card. 0 Disabled 1 Enabled
29:24	RESERVED2	R	0h	
23	SCLK_SEL	R/W	0h	Sampling Clock Select Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is set by tuning procedure and valid after the completion of tuning [when Execute Tuning is cleared]. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Writing 1 to this bit is meaningless and ignored. A tuning circuit is reset by Writing to 0. This bit can be cleared with setting Execute Tuning. Once the tuning circuit is reset, it will take time to complete tuning sequence. Therefore, Host Driver should keep this bit to 1 to perform re-tuning sequence to compete re-tuning sequence in a short time. Change of this bit is not allowed while the Host Controller is receiving response or a read data block. 0 Fixed clock is used to sample data 1 Tuned clock is used to sample data
22	ET	R/W	0h	Execute Tuning This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by Writing 0. This is Read-Write with automatic clear register 0 Not Tuned or Tuning Completed 1 Execute Tuning
21:20	DS_SEL	R/W	0h	Driver Strength Select Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the Capabilities register. This bit depends on setting of Preset Value Enable. If Preset Value Enable = 0, this field is set by Host Driver. If Preset Value Enable = 1, this field is automatically set by a value specified in the one of Preset Value registers. 0 Driver Type B is selected (Default) 1 Driver Type A is selected 2 Driver Type C is selected 3 Driver Type D is selected
19	V1V8_SIGEN	R/W	0h	1.8V Signaling Enable This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V. 1.8V regulator output shall be stable within 5ms. Host Controller clears this bit if switching to 1.8V signaling fails. Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V. 3.3V regulator output shall be stable within 5ms. Host Driver can set this bit to 1 when Host Controller supports 1.8V signaling [One of support bits is set to 1:SDR50, SDR104 or DDR50 in the Capabilities register] and the card or device supports UHS-I [S18A=1. Refer to Bus Signal Voltage Switch Sequence in the Physical Layer Specification Version 3.0x]. 0 3.3V Signaling 1 1.8V Signaling

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Table 5-1980. MMC_AC12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18:16	UHSMS	R/W	0h	UHS Mode Select This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1. If Preset Value Enable in the Host Control 2 register is set to 1, Host Controller sets SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again. When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more detail. 0 SDR12 1 SDR25 2 SDR50 3 SDR104 4 DDR50 5 Reserved 6 Reserved 7 Reserved
15:8	RESERVED1	R	0h	
7	CNI	R	0h	Command Not Issued By Auto CMD12 Error Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 Error [D04-D01] in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. 0 Not error 1 Command not issued
6:5	RESERVED	R	0h	
4	ACIE	R	0h	Auto CMD Index Error This bit is set if the Command Index error occurs in response to a command. 0 No error 1 Error
3	ACEB	R	0h	Auto CMD End Bit Error This bit is set when detecting that the end bit of command response is 0. 0 No error 1 End bit Error Generated
2	ACCE	R	0h	Auto CMD CRC Error This bit is set when detecting a CRC error in the command response. 0 No error 1 CRC Error Generated
1	ACTO	R	0h	Auto CMD Timeout Error This bit is set if no response is returned within 64 SDCLK cycles from the end bit of command. If this bit is set to1, the other error status bits [D04-D02] are meaningless. 0 No error 1 Auto CMD Time Out

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Table 5-1980. MMC_AC12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ACNE	R	0h	Auto CMD12 Not Executed If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the Host Controller cannot issue Auto CMD12 to stop memory multiple block data transfer due to some error. If this bit is set to 1, other error status bits [D04-D01] are meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. 0 Auto CMD12 Executed 1 Auto CMD12 Not Executed

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5.14.2.25 MMC_CAPA Register

5.14.2.25.1 MMC_CAPA Register (Offset = 240h) [reset = E10080h]

Capabilities Register
This register lists the capabilities of the MMC/SD/SDIO host controller.

Return to Summary Table

Table 5-1981. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0240h

Figure 5-970. MMC_CAPA Name Register

31	30	29	28	27	26	25	24
RESERVED4		AIS	BIT64	RESERVED3	VS18	VS30	VS33
R		R	R	R	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SRS	DS	HSS	RESERVED2	AD2S	RESERVED1	MBL	
R	R	R	R	R	R	R	
1h	1h	1h	0h	0h	0h	1h	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BCF							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TCU	RESERVED	TCF					
R	R	R					
1h	0h	0h					

Table 5-1982. MMC_CAPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED4	R	0h	
29	AIS	R	0h	Asynchronous Interrupt Support Refer to SDIO Specification Version 3.00 about asynchronous interrupt. `0 Asynchronous Interrupt Not Supported` `1 Asynchronous Interrupt Supported`
28	BIT64	R	0h	64 Bit System Bus Support Setting 1 to this bit indicates that the Host Controller supports 64-bit address descriptor mode and is connected to 64-bit address system bus. `0 32 bit System bus address` `1 64 bit System bus address`
27	RESERVED3	R	0h	
26	VS18	R/W	0h	Voltage support 1.8V Initialization of this register [via a write access to this register] depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset [via RESETN signal] `0 1.8V Not supported` `0 1.8V Not Supported` `1 1.8V Supported` `1 1.8V Supported`

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Table 5-1982. MMC_CAPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	VS30	R/W	0h	Voltage support 3.0V Initialization of this register [via a write access to this register] depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset [via RESETN signal] 0 3.0V Not supported 0 3.0V Not Supported 1 3.0V Supported 1 3.0V Supported
24	VS33	R/W	0h	Voltage support 3.3V Initialization of this register [via a write access to this register] depends on the system capabilities. The host driver shall not modify this register after the initilaization. This register is only reinitialized by a hard reset [via RESETN signal] 0 3.3V Not supported 0 3.3V Not Supported 1 3.3V Supported 1 3.3V Supported
23	SRS	R	1h	Suspend/Resume support [SDIO cards only] This bit indicates whether the host controller supports Suspend/ Resume functionality. 0 The Host controller does not Suspend/Resume functionality. 1 The Host controller supports Suspend/Resume functionality.
22	DS	R	1h	DMA support This bit indicates that the Host Controller is able to use DMA to transfer data between system memory and the Host Controller directly. 0 DMA Not Supported 1 DMA Supported
21	HSS	R	1h	High speed support This bit indicates that the host controller supports high speed operations and can supply an up-to maximum card frequency. 0 High Speed Not Supported 1 High Speed Supported
20	RESERVED2	R	0h	
19	AD2S	R	0h	ADMA2 Support This bit indicates whether the Host Controller is capable of using ADMA2. It depends on setting of generic parameter MADMA_EN 0 ADMA2 not Supported 1 ADMA2 Supported
18	RESERVED1	R	0h	
17:16	MBL	R	1h	Maximum block length This value indicates the maximum block size that the host driver can read and write to the buffer in the host controller. This value depends on definition of generic parameter with a max value of 2048bytes. The host controller supports 512 bytes and 1024bytes block transfers. 0 512 bytes 1 1024 bytes 2 2048 bytes

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Table 5-1982. MMC_CAPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	BCF	R	0h	Base Clock Frequency For SD Clock This value indicates the base [maximum] clock frequency for the SD Clock. 8-bit Base Clock Frequency This mode is supported by the Host Controller Version 3.00. Unit values are 1MHz. The supported clock range is 10MHz to 255MHz. FFh : 255MHz .... : .... 02h: 2MHz 01h: 1MHz 00h: Get information via another method If the real frequency is 16.5MHz, the lager value shall be set 00010001b [17MHz] because the Host Driver use this value to calculate the clock divider value [Refer to the SDCLK Frequency Select in the Clock Control register.] and it shall not exceed upper limit of the SD Clock frequency. If these bits are all 0, the Host System has to get information via another method. 0 The value indicating the base (maximum) frequency for the output clock provided to the card is system dependent and is not available in this register. Get the information via another method.
7	TCU	R	1h	Timeout clock unit This bit shows the unit of base clock frequency used to detect Data Timeout Error [MMCSD_STAT[DTO]]. 0 KHz 1 MHz
6	RESERVED	R	0h	
5:0	TCF	R	0h	Timeout clock frequency The timeout clock frequency is used to detect Data Timeout Error [MMCSD_STAT[DTO]]. 0 The timeout clock frequency depends on the frequency of the clock provided to the card. The value of the timeout clock frequency is not available in this register.

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5.14.2.26 MMC_CAPA2 Register

5.14.2.26.1 MMC_CAPA2 Register (Offset = 244h) [reset = 0h]

Capabilities 2 Register
This register provides the Host Driver with information specific to the Host Controller implementation. The Host Controller may implement these values as fixed or loaded from flash memory during power on initialization. Refer to Software Reset For All in the Software Reset register for loading from flash memory and completion timing control.

Return to Summary Table

Table 5-1983. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0244h

Figure 5-971. MMC_CAPA2 Name Register

31	30	29	28	27	26	25	24
RESERVED3							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CM							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTM		TSDR50	RESERVED2	TCRT			
R		R	R	R			
0h		0h	0h	0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED1	DTD	DTC	DTA	RESERVED	DDR50	SDR104	SDR50
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-1984. MMC_CAPA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED3	R	0h	
23:16	CM	R	0h	Clock Multiplier This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 00hmeans that Host Controller does not support programmable clock generator. 00h: Clock Multiplier is Not Supported 01h: Clock Multiplier M = 2 02h: Clock Multiplier M = 3 .... : .... FFh : Clock Multiplier M = 256

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Table 5-1984. MMC_CAPA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	RTM	R	0h	Re-Tuning Modes This field selects re-tuning method and limits the maximum data length. Bit47-46 Re-Tuning Mode Re-Tuning Method Data Length There are two re-tuning timings: Re-Tuning Request controlled by the Host Controller and expiration of a Re-Tuning Timer controlled by the Host Driver. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue. The maximum data length per read/write command is restricted so that re-tuning procedures can be inserted during data transfers. [1] Re-Tuning Mode 1 The host controller does not have any internal logic to detect when the re-tuning needs to be performed. In this case, the Host Driver should maintain all re-tuning timings by using a Re-Tuning Timer. To enable inserting the re-tuning procedure during data transfers, the data length per read/write command shall be limited up to 4MB. [2] Re-Tuning Mode 2 The host controller has the capability to indicate the re-tuning timing by Re-Tuning Request during data transfers. Then the data length per read/write command shall be limited up to 4MB. During non data transfer, re-tuning timing is determined by either Re-Tuning Request or Re-Tuning Timer. If Re-Tuning Request is used, Re-Tuning Timer should be disabled. [3] Re-Tuning Mode 3 The host controller has the capability to take care of the re-tuning during data transfer [Auto Re-Tuning]. Re-Tuning Request shall not be generated during data transfers and there is no limitation to data length per read/write command. During non data transfer, re-tuning timing is determined by either Re-Tuning Request or Re-Tuning Timer. If Re-Tuning Request is used, Re-Tuning Timer should be disabled. Re-Tuning Timer Control Example for Re-Tuning Mode 1 The initial value of re-tuning timer is provided by Timer Count for Re-Tuning field in this register. The timer starts counting by loading the initial value. When the timer expires, the Host Driver marks an expiration flag. On receiving a command request, the Host driver checks the expiration flag. If the expiration flag is set, then the Host Driver should perform the re-tuning procedure before issuing a command. If the expiration flag is not set, then the Host Driver issues a command without performing the re-tuning procedure. Every time the re-tuning procedure is performed, the timer loads the new initial value and the expiration flag is cleared. Re-Tuning Timer Control Example for Re-Tuning Mode 2 and Mode 3 The timer control is almost the same as Re-Tuning Mode 1 except the timer loads the new initial value after data transfer [when receiving Transfer Complete]. In case of Mode 3, Timer Count for Re-Tuning is set either smaller value: Tuning effective time after re-tuning procedure or after data transfer. If a Host System goes into power down mode, the Host Driver should stop the re-tuning timer and set the expiration flag to 1 when the Host System resumes from power down mode. 0 Timer - Max data length 4MB 1 Timer and Re-Tuning Request - Max data length 4MB 2 Auto Re-Tuning (for transfer) - Timer and Re-Tuning Request 3 Reserved
13	TSDR50	R	0h	Use Tuning for SDR50 If this bit is set to 1, this Host Controller requires tuning to operate SDR50. [Tuning is always required to operate SDR104.] 0 SDR50 does not require tuning. 1 SDR50 requires tuning.
12	RESERVED2	R	0h	

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Table 5-1984. MMC_CAPA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:8	TCRT	R	0h	Timer Count for Re-Tuning This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 0 disables Re-Tuning Timer. 0 Re-Tuning Timer disabled 1 1 second 2 2 seconds 3 4 seconds 4 8 seconds 5 16 seconds 6 32 seconds 7 64 seconds 8 128 seconds 9 256 seconds 10 512 seconds 11 1024 seconds 12 Reserved 13 Reserved 14 Reserved 15 Get information from other source
7	RESERVED1	R	0h	
6	DTD	R	0h	Driver Type D Support This bit indicates support of Driver Type D for 1.8 Signaling. 0 Driver Type D is Not Supported. 1 Driver Type D is Supported
5	DTC	R	0h	Driver Type C Support This bit indicates support of Driver Type C for 1.8 Signaling. 0 Driver Type C is Not Supported. 1 Driver Type C is Supported.
4	DTA	R	0h	Driver Type A Support This bit indicates support of Driver Type A for 1.8 Signaling. 0 Driver Type A is Not Supported. 1 Driver Type A is Supported.
3	RESERVED	R	0h	
2	DDR50	R	0h	DDR50 Support 0 DDR50 is Not Supported. 1 DDR50 is Supported.
1	SDR104	R	0h	SDR104 Support SDR104 requires tuning. 0 SDR104 is Not Supported. 1 SDR104 is Supported.
0	SDR50	R	0h	SDR50 Support If SDR104 is supported, this bit shall be set to 1. Bit 13 indicates whether SDR50 requires tuning or not. 0 SDR50 is Not Supported. 1 SDR50 is Supported.

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5.14.2.27 MMC_CUR_CAPA Register

5.14.2.27.1 MMC_CUR_CAPA Register (Offset = 248h) [reset = 0h]

Maximum Current Capabilities Register
This register indicates the maximum current capability for each voltage. The value is meaningful if the voltage support is set in the capabilities register (MMCHS_CAPA).
Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initilaization.
This register is only reinitialized by a hard reset (via RESETN signal).

Return to Summary Table

Table 5-1985. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0248h

Figure 5-972. MMC_CUR_CAPA Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
CUR_1V8							
R/W							
0h							
15	14	13	12	11	10	9	8
CUR_3V0							
R/W							
0h							
7	6	5	4	3	2	1	0
CUR_3V3							
R/W							
0h							

Table 5-1986. MMC_CUR_CAPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RESERVED	R	0h	
23:16	CUR_1V8	R/W	0h	Maximum current for 1.8V 0 `The maximum current capability for this voltage is not available. Feature not implemented.`
15:8	CUR_3V0	R/W	0h	Maximum current for 3.0V 0 `The maximum current capability for this voltage is not available. Feature not implemented.`
7:0	CUR_3V3	R/W	0h	Maximum current for 3.3V 0 `The maximum current capability for this voltage is not available. Feature not implemented.`

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5.14.2.28 MMC_FE Register

5.14.2.28.1 MMC_FE Register (Offset = 250h) [reset = 0h]

Force Event Register for Auto CMD Error Status and Error Interrupt status
The Force Event Register is not a physically implemented register. Rather, it is an address at which the Auto CMD Error Status Register can be written.
Writing 1 : set each bit of the Auto CMD Error Status Register
Writing 0 : no effect
Rather, it is an address at which the Error Interrupt Status register can be written. The effect of a write to this address will be reflected in the Error Interrupt Status Register if the corresponding bit of the Error Interrupt Status Enable Register is set.
Writing 1 : set each bit of the Error Interrupt Status Register
Writing 0 : no effect
Note: By setting this register, the Error Interrupt can be set in the Error Interrupt Status register. In order to generate interrupt signal, both the Error Interrupt Status Enable and Error Interrupt Signal Enable shall be set.

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Table 5-1987. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0250h

Figure 5-973. MMC_FE Name Register

31	30	29	28	27	26	25	24
RESERVED3		FE_BADA	FE_CERR	RESERVED2		FE_ADMAE	FE_ACE
		W	W			W	W
0h		0h	0h	0h		0h	0h
23	22	21	20	19	18	17	16
FE_CLE	FE_DEB	FE_DCRC	FE_DTO	FE_CIE	FE_CEB	FE_CCRC	FE_CTO
	W	W	W	W	W	W	W
0h	0h	0h	0h	0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED1							
0h							
7	6	5	4	3	2	1	0
FE_CNI	RESERVED		FE_ACIE	FE_ACEB	FE_ACCE	FE_ACTO	FE_ACNE
W			W	W	W	W	W
0h	0h		0h	0h	0h	0h	0h

Table 5-1988. MMC_FE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	RESERVED3		0h	
29	FE_BADA	W	0h	Force Event Bad access to data space. 0 `No effect, No Interrupt.` 1 `Interrupt Forced`
28	FE_CERR	W	0h	Force Event Card error. 0 `No effect, No Interrupt.` 1 `Interrupt Forced`
27:26	RESERVED2		0h	
25	FE_ADMAE	W	0h	Force Event ADMA Error. 0 `No effect, No Interrupt.` 1 `Interrupt Forced`

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Table 5-1988. MMC_FE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	FE_ACE	W	0h	Force Event for Auto CMD Error 0 No effect, No Interrupt. 1 Interrupt Forced
23	FE_CLE		0h	Reserved. Current limit error is not supported. These bits are initialized to zero, and writes to them are ignored.
22	FE_DEB	W	0h	Force Event Data End Bit error. 0 No effect, No Interrupt. 1 Interrupt Forced
21	FE_DCRC	W	0h	Force Event Data CRC Error. 0 No effect, No Interrupt. 1 Interrupt Forced
20	FE_DTO	W	0h	Force Event Data Timeout Error. 0 No effect, No Interrupt. 1 Interrupt Forced
19	FE_CIE	W	0h	Force Event Command Index Error. 0 No effect, No Interrupt. 1 Interrupt Forced
18	FE_CEB	W	0h	Force Event Command End Bit Error. 0 No effect, No Interrupt. 1 Interrupt Forced
17	FE_CCRC	W	0h	Force Event Command CRC Error. 0 No effect, No Interrupt. 1 Interrupt Forced
16	FE_CTO	W	0h	Command Timeout Error This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command. For commands that reply within 5 clock cycles - the timeout is still detected at 64 clock cycles. 0 Status bit unchanged 1 Status is cleared
15:8	RESERVED1		0h	
7	FE_CNI	W	0h	Force Event Command not issue by Auto CMD12 error 0 No effect, No Interrupt. 1 Interrupt Forced
6:5	RESERVED		0h	
4	FE_ACIE	W	0h	Force Event for Auto CMD Index Error 0 No effect, No Interrupt. 1 Interrupt Forced
3	FE_ACEB	W	0h	Force Event Auto CMD End Bit Error 0 No effect, No Interrupt. 1 Interrupt Forced
2	FE_ACCE	W	0h	Force Event Auto CMD CRC Error 0 No effect, No Interrupt. 1 Interrupt Forced
1	FE_ACTO	W	0h	Force Event Auto CMD Timeout Error 0 No effect, No Interrupt. 1 Interrupt Forced
0	FE_ACNE	W	0h	Force Event Auto CMD12 Not Executed 0 No effect, No Interrupt. 1 Interrupt Forced

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5.14.2.29 MMC_ADMAES Register

5.14.2.29.1 MMC_ADMAES Register (Offset = 254h) [reset = 0h]

ADMA Error Status Register
When ADMA Error Interrupt is occurred, the ADMA Error States field in this register holds the ADMA state and the ADMA System Address Register holds the address around the error descriptor. For recovering the error, the Host Driver requires the ADMA state to identify the error descriptor address as follows:
ST_STOP: Previous location set in the ADMA System Address register is the error descriptor address
ST_FDS: Current location set in the ADMA System Address register is the error descriptor address
ST_CADR: This sate is never set because do not generate ADMA error in this state.
ST_TFR: Previous location set in the ADMA System Address register is the error descriptor address
In case of write operation, the Host Driver should use ACMD22 to get the number of written block rather than using this information, since unwritten data may exist in the Host Controller. The Host Controller generates the ADMA Error Interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. In this case, ADMA Error State indicates that an error occurs at ST_FDS state. The Host Driver may find that the Valid bit is not set in the error descriptor.

Return to Summary Table

Table 5-1989. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0254h

Figure 5-974. MMC_ADMAES Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					LME	AES	
R					R/W	R/W	
0h					0h	0h	

Table 5-1990. MMC_ADMAES Register Field Descriptions

Bit	Field	Type	Reset	Description
31:3	RESERVED	R	0h	
2	LME	R/W	0h	ADMA Length Mismatch Error: [1] While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. [2] Total data length can not be divided by the block length. 0 No Error 1 Error

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Table 5-1990. MMC_ADMAES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	AES	R/W	0h	ADMA Error State his field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. 0 ST_STOP (Stop DMA)Contents of SYS_SDR register 1 ST_STOP (Stop DMA)Points the error descriptor 2 Never set this state(Not used) 3 ST_TFR (Transfer Data)Points the next of the error descriptor

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5.14.2.30 MMC_ADMASAL Register

5.14.2.30.1 MMC_ADMASAL Register (Offset = 258h) [reset = 0h]

ADMA System address Low bits.

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Table 5-1991. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0258h

Figure 5-975. MMC_ADMASAL Name Register

31	30	29	28	27	26	25	24
ADMA_A32B							
R/W							
0h							
23	22	21	20	19	18	17	16
ADMA_A32B							
R/W							
0h							
15	14	13	12	11	10	9	8
ADMA_A32B							
R/W							
0h							
7	6	5	4	3	2	1	0
ADMA_A32B							
R/W							
0h							

Table 5-1992. MMC_ADMASAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ADMA_A32B	R/W	0h	ADMA System address 32 bits.This register holds byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32-bit of this register. At the start of ADMA, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold valid Descriptor address depending on the ADMA state. The Host Driver shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. ADMA2 ignores lower 2-bit of this register and assumes it to be 00b

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5.14.2.31 MMC_PVINITSD Register

5.14.2.31.1 MMC_PVINITSD Register (Offset = 260h) [reset = 0h]

Preset Value for Initialization and Default Speed modes.

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Table 5-1993. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0260h

Figure 5-976. MMC_PVINITSD Name Register

31	30	29	28	27	26	25	24
DSDS_SEL		RESERVED1			DSCLKGEN_SEL	DSSDCLK_SEL	
R		R			R	R	
0h		0h			0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DSSDCLK_SEL							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
INITDS_SEL		RESERVED			INITCLKGEN_SEL	INITSDCLK_SEL	
R		R			R	R	
0h		0h			0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INITSDCLK_SEL							
R							
0h							

Table 5-1994. MMC_PVINITSD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	DSDS_SEL	R	0h	Driver Strength Select Value - Default Speed mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 0 Driver Type B is Selected. 1 Driver Type A is Selected. 2 Driver Type C is Selected. 3 Driver Type D is Selected.
29:27	RESERVED1	R	0h	
26	DSCLKGEN_SEL	R	0h	Clock Generator Select Value - Default Speed mode This bit is effective when Host Controller supports programmable clock generator. 0 Host Controller Ver2.00 Compatible Clock Generator. 1 Programmable Clock Generator.
25:16	DSSDCLK_SEL	R	0h	SDCLK Frequency Select Value - Default Speed mode 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

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Table 5-1994. MMC_PVINITSD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	INITDS_SEL	R	0h	Driver Strength Select Value - Initialization mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 0 Driver Type B is Selected 1 Driver Type A is Selected 2 Driver Type C is Selected 3 Driver Type D is Selected
13:11	RESERVED	R	0h	
10	INITCLKGEN_SEL	R	0h	Clock Generator Select Value - Initialization mode This bit is effective when Host Controller supports programmable clock generator. 0 Host Controller Ver2.00 Compatible Clock Generator. 1 Programmable Clock Generator.
9:0	INITSDCLK_SEL	R	0h	SDCLK Frequency Select Value - Initialization mode 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

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5.14.2.32 MMC_PVHSSDR12 Register

5.14.2.32.1 MMC_PVHSSDR12 Register (Offset = 264h) [reset = 0h]

Preset Value for High Speed and SDR12 speed modes.

Return to Summary Table

Table 5-1995. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0264h

Figure 5-977. MMC_PVHSSDR12 Name Register

31	30	29	28	27	26	25	24
SDR12DS_SEL		RESERVED1			SDR12CLKGEN_SEL	SDR12SDCLK_SEL	
R		R			R	R	
0h		0h			0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SDR12SDCLK_SEL							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
HSDS_SEL		RESERVED			HSCLKGEN_SEL	HSSDCLK_SEL	
R		R			R	R	
0h		0h			0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HSSDCLK_SEL							
R							
0h							

Table 5-1996. MMC_PVHSSDR12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SDR12DS_SEL	R	0h	Driver Strength Select Value - SDR12 mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 0 Driver Type B is Selected. 1 Driver Type A is Selected. 2 Driver Type C is Selected. 3 Driver Type D is Selected.
29:27	RESERVED1	R	0h	
26	SDR12CLKGEN_SEL	R	0h	Clock Generator Select Value - SDR12 mode This bit is effective when Host Controller supports programmable clock generator. 0 Host Controller Ver2.00 Compatible Clock Generato. 1 Programmable Clock Generator.
25:16	SDR12SDCLK_SEL	R	0h	SDCLK Frequency Select Value - SDR12 mode 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

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Table 5-1996. MMC_PVHSSDR12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	HSDS_SEL	R	0h	Driver Strength Select Value - High Speed mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 0 Driver Type B is Selected. 1 Driver Type A is Selected. 2 Driver Type C is Selected. 3 Driver Type D is Selected.
13:11	RESERVED	R	0h	
10	HSCLKGEN_SEL	R	0h	Clock Generator Select Value - High Speed mode This bit is effective when Host Controller supports programmable clock generator. 0 Host Controller Ver2.00 Compatible Clock Generator. 1 Programmable Clock Generator.
9:0	HSSDCLK_SEL	R	0h	SDCLK Frequency Select Value - High Speed mode 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

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5.14.2.33 MMC_PVSDR25SDR50 Register

5.14.2.33.1 MMC_PVSDR25SDR50 Register (Offset = 268h) [reset = 0h]

Preset Value for SDR25 and SDR50 speed modes.

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Table 5-1997. Instance Table

Instance Name	Physical Address
MMCSD0	4830 0268h

Figure 5-978. MMC_PVSDR25SDR50 Name Register

31	30	29	28	27	26	25	24
SDR50DS_SEL		RESERVED1			SDR50CLKGEN_SEL	SDR50SDCLK_SEL	
R		R			R	R	
0h		0h			0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SDR50SDCLK_SEL							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SDR25DS_SEL		RESERVED			SDR25CLKGEN_SEL	SDR25SDCLK_SEL	
R		R			R	R	
0h		0h			0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDR25SDCLK_SEL							
R							
0h							

Table 5-1998. MMC_PVSDR25SDR50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SDR50DS_SEL	R	0h	Driver Strength Select Value - SDR50 mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 0 `Driver Type B is Selected.` 1 `Driver Type A is Selected.` 2 `Driver Type C is Selected.` 3 `Driver Type D is Selected.`
29:27	RESERVED1	R	0h	
26	SDR50CLKGEN_SEL	R	0h	Clock Generator Select Value - SDR50 mode This bit is effective when Host Controller supports programmable clock generator. 0 `Host Controller Ver2.00 Compatible Clock Generator.` 1 `Programmable Clock Generator.`
25:16	SDR50SDCLK_SEL	R	0h	SDCLK Frequency Select Value - SDR50 mode 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

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Table 5-1998. MMC_PVSDR25SDR50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SDR25DS_SEL	R	0h	Driver Strength Select Value - SDR25 mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 0 Driver Type B is Selected. 1 Driver Type A is Selected. 2 Driver Type C is Selected. 3 Driver Type D is Selected.
13:11	RESERVED	R	0h	
10	SDR25CLKGEN_SEL	R	0h	Clock Generator Select Value - SDR25 mode This bit is effective when Host Controller supports programmable clock generator. 0 Host Controller Ver2.00 Compatible Clock Generator. 1 Programmable Clock Generato.
9:0	SDR25SDCLK_SEL	R	0h	SDCLK Frequency Select Value - SDR25 mode 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

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5.14.2.34 MMC_PVSDR104DDR50 Register

5.14.2.34.1 MMC_PVSDR104DDR50 Register (Offset = 26Ch) [reset = 0h]

Preset Value for SDR104 and DDR50 speed modes.

Return to Summary Table

Table 5-1999. Instance Table

Instance Name	Physical Address
MMCSD0	4830 026Ch

Figure 5-979. MMC_PVSDR104DDR50 Name Register

31	30	29	28	27	26	25	24
DDR50DS_SEL		RESERVED1			DDR50CLKGEN_SEL	DDR50SDCLK_SEL	
R		R			R	R	
0h		0h			0h	0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DDR50SDCLK_SEL							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SDR104DS_SEL		RESERVED			SDR104CLKGEN_SEL	SDR104SDCLK_SEL	
R		R			R	R	
0h		0h			0h	0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SDR104SDCLK_SEL							
R							
0h							

Table 5-2000. MMC_PVSDR104DDR50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	DDR50DS_SEL	R	0h	Driver Strength Select Value - DDR50 mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 0 Driver Type B is Selected. 1 Driver Type A is Selected. 2 Driver Type C is Selected. 3 Driver Type D is Selected.
29:27	RESERVED1	R	0h	
26	DDR50CLKGEN_SEL	R	0h	Clock Generator Select Value - DDR50 mode This bit is effective when Host Controller supports programmable clock generator. 0 Host Controller Ver2.00 Compatible Clock Generator 1 Programmable Clock Generator
25:16	DDR50SDCLK_SEL	R	0h	SDCLK Frequency Select Value - DDR50 mode 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

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Table 5-2000. MMC_PVSDR104DDR50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:14	SDR104DS_SEL	R	0h	Driver Strength Select Value - SDR104 mode Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 0 Driver Type B is Selected. 1 Driver Type A is Selected. 2 Driver Type C is Selected. 3 Driver Type D is Selected.
13:11	RESERVED	R	0h	
10	SDR104CLKGEN_SEL	R	0h	Clock Generator Select Value - SDR104 mode This bit is effective when Host Controller supports programmable clock generator. 0 Host Controller Ver2.00 Compatible Clock Generator. 1 Programmable Clock Generator.
9:0	SDR104SDCLK_SEL	R	0h	SDCLK Frequency Select Value - SDR104 mode 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

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5.14.2.35 MMC_REV Register

5.14.2.35.1 MMC_REV Register (Offset = 2FCh) [reset = 31010000h]

Versions Register
This register contains the hard coded RTL vendor revision number, the version number of SD specification compliancy and a slot status bit.
MMCHS_REV[31:16] = Host controller version
MMCHS_REV[15:0] = Slot Interrupt Status.

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Table 5-2001. Instance Table

Instance Name	Physical Address
MMCSD0	4830 02FCh

Figure 5-980. MMC_REV Name Register

31	30	29	28	27	26	25	24
VREV							
R							
31h							
23	22	21	20	19	18	17	16
SREV							
R							
1h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							SIS
R							R
0h							0h

Table 5-2002. MMC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	VREV	R	31h	Vendor Version Number: IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 1.0 0x21 for 2.1
23:16	SREV	R	1h	Specification Version Number This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version. 0 SD Host Specification Version 1.00. 1 SD Host Specification Version 2.00 - Including the feature of the ADMA and Test Register. 2 SD Host Specification Version 3.00. 3 Reserved
15:1	RESERVED	R	0h	

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Table 5-2002. MMC_REV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SIS	R	0h	Slot Interrupt Status This status bit indicates the inverted state of interrupt signal for the module. By a power on reset or by setting a software reset for all [MMCSD_HCTL[SRA]], the interrupt signal shall be de-asserted and this status shall read 0.

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5.15 MPU_4

MPU_4

5.15.1 MPU_4 Summaries

MPU_4 Summaries

Table 5-2003. MPU_4 Registers, Base Address=4026 0000h, Length=1024

Offset	Length	Register Name	MPU_FSS_CONFIG Physical Address	MPU_R5SS0_CONFIG Physical Address	MPU_R5SS1_CONFIG Physical Address
0h	32	MPU_4_REVISION	4026 0000h	4028 0000h	402A 0000h
10h	32	MPU_4_INTERRUPT_RAW_STATUS_SET	4026 0010h	4028 0010h	402A 0010h
14h	32	MPU_4_INTERRUPT_ENABLED_STATUS_CLEAR	4026 0014h	4028 0014h	402A 0014h
18h	32	MPU_4_INTERRUPT_ENABLE	4026 0018h	4028 0018h	402A 0018h
1Ch	32	MPU_4_INTERRUPT_ENABLE_CLEAR	4026 001Ch	4028 001Ch	402A 001Ch
200h	32	MPU_4_PROGRAMMABLE_1_START_ADDRESS	4026 0200h	4028 0200h	402A 0200h
204h	32	MPU_4_PROGRAMMABLE_1_END_ADDRESS	4026 0204h	4028 0204h	402A 0204h
208h	32	MPU_4_PROGRAMMABLE_1_MPPA	4026 0208h	4028 0208h	402A 0208h
210h	32	MPU_4_PROGRAMMABLE_2_START_ADDRESS	4026 0210h	4028 0210h	402A 0210h
214h	32	MPU_4_PROGRAMMABLE_2_END_ADDRESS	4026 0214h	4028 0214h	402A 0214h
218h	32	MPU_4_PROGRAMMABLE_2_MPPA	4026 0218h	4028 0218h	402A 0218h
220h	32	MPU_4_PROGRAMMABLE_3_START_ADDRESS	4026 0220h	4028 0220h	402A 0220h
224h	32	MPU_4_PROGRAMMABLE_3_END_ADDRESS	4026 0224h	4028 0224h	402A 0224h
228h	32	MPU_4_PROGRAMMABLE_3_MPPA	4026 0228h	4028 0228h	402A 0228h
230h	32	MPU_4_PROGRAMMABLE_4_START_ADDRESS	4026 0230h	4028 0230h	402A 0230h
234h	32	MPU_4_PROGRAMMABLE_4_END_ADDRESS	4026 0234h	4028 0234h	402A 0234h
238h	32	MPU_4_PROGRAMMABLE_4_MPPA	4026 0238h	4028 0238h	402A 0238h
300h	32	MPU_4_FAULT_ADDRESS	4026 0300h	4028 0300h	402A 0300h
304h	32	MPU_4_FAULT_STATUS	4026 0304h	4028 0304h	402A 0304h
308h	32	MPU_4_FAULT_CLEAR	4026 0308h	4028 0308h	402A 0308h

5.15.2 MPU_4 Registers

MPU_4 Registers

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5.15.2.1 MPU_4_REVISION Register

5.15.2.1.1 MPU_4_REVISION Register (Offset = 0h) [reset = 4E815101h]

Revision.

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Table 5-2004. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0000h
MPU_R5SS0_CONFIG	4028 0000h
MPU_R5SS1_CONFIG	402A 0000h

Figure 5-981. MPU_4_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		MODID			
R		R		R			
1h		0h		E81h			
23	22	21	20	19	18	17	16
MODID							
R							
E81h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
Ah					1h		
7	6	5	4	3	2	1	0
REVCUSTOM		REVMIN					
R		R					
0h		1h					

Table 5-2005. MPU_4_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme.
29:28	RESERVED	R	0h	Always read a s0. Writes have no affect.
27:16	MODID	R	E81h	Module ID field.
15:11	REVRTL	R	Ah	RTL revision.Will vary depending on release.
10:8	REVMAJ	R	1h	Major revision.
7:6	REVCUSTOM	R	0h	Custom revision.
5:0	REVMIN	R	1h	Minor revision.

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5.15.2.2 MPU_4_INTERRUPT_RAW_STATUS_SET Register

5.15.2.2.1 MPU_4_INTERRUPT_RAW_STATUS_SET Register (Offset = 10h) [reset = 0h]

Interrupt Raw Status/Set.

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Table 5-2006. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0010h
MPU_R5SS0_CONFIG	4028 0010h
MPU_R5SS1_CONFIG	402A 0010h

Figure 5-982. MPU_4_INTERRUPT_RAW_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						ADDR_ERR	PROT_ERR
R						R/W1TS	R/W1TS
0h						0h	0h

Table 5-2007. MPU_4_INTERRUPT_RAW_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read.Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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5.15.2.3 MPU_4_INTERRUPT_ENABLED_STATUS_CLEAR Register

5.15.2.3.1 MPU_4_INTERRUPT_ENABLED_STATUS_CLEAR Register (Offset = 14h) [reset = 0h]

Interrupt Enabled Status/Clear.

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Table 5-2008. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0014h
MPU_R5SS0_CONFIG	4028 0014h
MPU_R5SS1_CONFIG	402A 0014h

Figure 5-983. MPU_4_INTERRUPT_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						ENABLED_ADDR_ERR	ENABLED_PROT_ERR
R						R/W0TC	R/W0TC
0h						0h	0h

Table 5-2009. MPU_4_INTERRUPT_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ENABLED_ADDR_ERR	R/W0TC	0h	Addressing violation error. Enabled status is read.Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	R/W0TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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5.15.2.4 MPU_4_INTERRUPT_ENABLE Register

5.15.2.4.1 MPU_4_INTERRUPT_ENABLE Register (Offset = 18h) [reset = 0h]

Interrupt Enable.

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Table 5-2010. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0018h
MPU_R5SS0_CONFIG	4028 0018h
MPU_R5SS1_CONFIG	402A 0018h

Figure 5-984. MPU_4_INTERRUPT_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						ADDR_ERR_EN	PROT_ERR_EN
R						R/W1TS	R/W1TS
0h						0h	0h

Table 5-2011. MPU_4_INTERRUPT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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5.15.2.5 MPU_4_INTERRUPT_ENABLE_CLEAR Register

5.15.2.5.1 MPU_4_INTERRUPT_ENABLE_CLEAR Register (Offset = 1Ch) [reset = 0h]

Interrupt Enable Clear.

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Table 5-2012. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 001Ch
MPU_R5SS0_CONFIG	4028 001Ch
MPU_R5SS1_CONFIG	402A 001Ch

Figure 5-985. MPU_4_INTERRUPT_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
R						R/W0TC	R/W0TC
0h						0h	0h

Table 5-2013. MPU_4_INTERRUPT_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ADDR_ERR_EN_CLR	R/W0TC	0h	Addressing violation error enable. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	R/W0TC	0h	Protection violation error enable. Write a 1 to clear the enable. Writing a 0 has no effect.

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5.15.2.6 MPU_4_PROGRAMMABLE_1_START_ADDRESS Register

5.15.2.6.1 MPU_4_PROGRAMMABLE_1_START_ADDRESS Register (Offset = 200h) [reset = 0h]

Programmable_1_Start_Address.

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Table 5-2014. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0200h
MPU_R5SS0_CONFIG	4028 0200h
MPU_R5SS1_CONFIG	402A 0200h

Figure 5-986. MPU_4_PROGRAMMABLE_1_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2015. MPU_4_PROGRAMMABLE_1_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.15.2.7 MPU_4_PROGRAMMABLE_1_END_ADDRESS Register

5.15.2.7.1 MPU_4_PROGRAMMABLE_1_END_ADDRESS Register (Offset = 204h) [reset = 0h]

Programmable_1_End_Address.

Return to Summary Table

Table 5-2016. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0204h
MPU_R5SS0_CONFIG	4028 0204h
MPU_R5SS1_CONFIG	402A 0204h

Figure 5-987. MPU_4_PROGRAMMABLE_1_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2017. MPU_4_PROGRAMMABLE_1_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.15.2.8 MPU_4_PROGRAMMABLE_1_MPPA Register

5.15.2.8.1 MPU_4_PROGRAMMABLE_1_MPPA Register (Offset = 208h) [reset = 0h]

Programmable_1_MPPA.

Return to Summary Table

Table 5-2018. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0208h
MPU_R5SS0_CONFIG	4028 0208h
MPU_R5SS1_CONFIG	402A 0208h

Figure 5-988. MPU_4_PROGRAMMABLE_1_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2019. MPU_4_PROGRAMMABLE_1_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0.
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.

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Table 5-2019. MPU_4_PROGRAMMABLE_1_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.15.2.9 MPU_4_PROGRAMMABLE_2_START_ADDRESS Register

5.15.2.9.1 MPU_4_PROGRAMMABLE_2_START_ADDRESS Register (Offset = 210h) [reset = 0h]

Programmable_2_Start_Address.

Return to Summary Table

Table 5-2020. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0210h
MPU_R5SS0_CONFIG	4028 0210h
MPU_R5SS1_CONFIG	402A 0210h

Figure 5-989. MPU_4_PROGRAMMABLE_2_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2021. MPU_4_PROGRAMMABLE_2_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.15.2.10 MPU_4_PROGRAMMABLE_2_END_ADDRESS Register

5.15.2.10.1 MPU_4_PROGRAMMABLE_2_END_ADDRESS Register (Offset = 214h) [reset = 0h]

Programmable_2_End_Address.

Return to Summary Table

Table 5-2022. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0214h
MPU_R5SS0_CONFIG	4028 0214h
MPU_R5SS1_CONFIG	402A 0214h

Figure 5-990. MPU_4_PROGRAMMABLE_2_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2023. MPU_4_PROGRAMMABLE_2_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.15.2.11 MPU_4_PROGRAMMABLE_2_MPPA Register

5.15.2.11.1 MPU_4_PROGRAMMABLE_2_MPPA Register (Offset = 218h) [reset = 0h]

Programmable_2_MPPA.

Return to Summary Table

Table 5-2024. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0218h
MPU_R5SS0_CONFIG	4028 0218h
MPU_R5SS1_CONFIG	402A 0218h

Figure 5-991. MPU_4_PROGRAMMABLE_2_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	22	21	20	19	18	17	16
AID15_0							
R/W							
0h							
15	14	13	12	11	10	9	8
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	6	5	4	3	2	1	0
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2025. MPU_4_PROGRAMMABLE_2_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.

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Table 5-2025. MPU_4_PROGRAMMABLE_2_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.15.2.12 MPU_4_PROGRAMMABLE_3_START_ADDRESS Register

5.15.2.12.1 MPU_4_PROGRAMMABLE_3_START_ADDRESS Register (Offset = 220h) [reset = 0h]

Programmable_3_Start_Address.

Return to Summary Table

Table 5-2026. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0220h
MPU_R5SS0_CONFIG	4028 0220h
MPU_R5SS1_CONFIG	402A 0220h

Figure 5-992. MPU_4_PROGRAMMABLE_3_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2027. MPU_4_PROGRAMMABLE_3_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.15.2.13 MPU_4_PROGRAMMABLE_3_END_ADDRESS Register

5.15.2.13.1 MPU_4_PROGRAMMABLE_3_END_ADDRESS Register (Offset = 224h) [reset = 0h]

Programmable_3_End_Address.

Return to Summary Table

Table 5-2028. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0224h
MPU_R5SS0_CONFIG	4028 0224h
MPU_R5SS1_CONFIG	402A 0224h

Figure 5-993. MPU_4_PROGRAMMABLE_3_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDR							
R/W							
0h							

Table 5-2029. MPU_4_PROGRAMMABLE_3_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.15.2.14 MPU_4_PROGRAMMABLE_3_MPPA Register

5.15.2.14.1 MPU_4_PROGRAMMABLE_3_MPPA Register (Offset = 228h) [reset = 0h]

Programmable_3_MPPA.

Return to Summary Table

Table 5-2030. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0228h
MPU_R5SS0_CONFIG	4028 0228h
MPU_R5SS1_CONFIG	402A 0228h

Figure 5-994. MPU_4_PROGRAMMABLE_3_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	22	21	20	19	18	17	16
AID15_0							
R/W							
0h							
15	14	13	12	11	10	9	8
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	6	5	4	3	2	1	0
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2031. MPU_4_PROGRAMMABLE_3_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.

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Table 5-2031. MPU_4_PROGRAMMABLE_3_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.15.2.15 MPU_4_PROGRAMMABLE_4_START_ADDRESS Register

5.15.2.15.1 MPU_4_PROGRAMMABLE_4_START_ADDRESS Register (Offset = 230h) [reset = 0h]

Programmable_4_Start_Address.

Return to Summary Table

Table 5-2032. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0230h
MPU_R5SS0_CONFIG	4028 0230h
MPU_R5SS1_CONFIG	402A 0230h

Figure 5-995. MPU_4_PROGRAMMABLE_4_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2033. MPU_4_PROGRAMMABLE_4_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.15.2.16 MPU_4_PROGRAMMABLE_4_END_ADDRESS Register

5.15.2.16.1 MPU_4_PROGRAMMABLE_4_END_ADDRESS Register (Offset = 234h) [reset = 0h]

Programmable_4_End_Address.

Return to Summary Table

Table 5-2034. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0234h
MPU_R5SS0_CONFIG	4028 0234h
MPU_R5SS1_CONFIG	402A 0234h

Figure 5-996. MPU_4_PROGRAMMABLE_4_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2035. MPU_4_PROGRAMMABLE_4_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.15.2.17 MPU_4_PROGRAMMABLE_4_MPPA Register

5.15.2.17.1 MPU_4_PROGRAMMABLE_4_MPPA Register (Offset = 238h) [reset = 0h]

Programmable_4_MPPA.

Return to Summary Table

Table 5-2036. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0238h
MPU_R5SS0_CONFIG	4028 0238h
MPU_R5SS1_CONFIG	402A 0238h

Figure 5-997. MPU_4_PROGRAMMABLE_4_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2037. MPU_4_PROGRAMMABLE_4_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.

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Table 5-2037. MPU_4_PROGRAMMABLE_4_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.15.2.18 MPU_4_FAULT_ADDRESS Register

5.15.2.18.1 MPU_4_FAULT_ADDRESS Register (Offset = 300h) [reset = 0h]

Fault_Address.

Return to Summary Table

Table 5-2038. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0300h
MPU_R5SS0_CONFIG	4028 0300h
MPU_R5SS1_CONFIG	402A 0300h

Figure 5-998. MPU_4_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 5-2039. MPU_4_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault address.

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5.15.2.19 MPU_4_FAULT_STATUS Register

5.15.2.19.1 MPU_4_FAULT_STATUS Register (Offset = 304h) [reset = 0h]

Fault Status.

Return to Summary Table

Table 5-2040. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0304h
MPU_R5SS0_CONFIG	4028 0304h
MPU_R5SS1_CONFIG	402A 0304h

Figure 5-999. MPU_4_FAULT_STATUS Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MSTID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRIVID				RESERVED1
R			R				R
0h			0h				0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	RESERVED2	FAULT_TYPE					
R	R	R					
0h	0h	0h					

Table 5-2041. MPU_4_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ID	R	0h	Transfer ID
23:16	MSTID	R	0h	Initiator ID.
15:13	RESERVED	R	0h	Always read as 0.
12:9	PRIVID	R	0h	Privilege ID.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R	0h	Non-secure access.
6	RESERVED2	R	0h	Always read as 0.
5:0	FAULT_TYPE	R	0h	Fault type. 100000 = supervisor read fault 010000 = supervisor write fault 001000 = supervisor execute fault 000100 = user read fault 000010 = user write fault 000001 = user execute fault 111111 = relaxed cache linefill fault 010010 = relaxed cache writeback fault 000000 = no fault

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5.15.2.20 MPU_4_FAULT_CLEAR Register

5.15.2.20.1 MPU_4_FAULT_CLEAR Register (Offset = 308h) [reset = 0h]

Fault Clear.

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Table 5-2042. Instance Table

Instance Name	Physical Address
MPU_FSS_CONFIG	4026 0308h
MPU_R5SS0_CONFIG	4028 0308h
MPU_R5SS1_CONFIG	402A 0308h

Figure 5-1000. MPU_4_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
R							W
0h							0h

Table 5-2043. MPU_4_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Always read as 0.
0	FAULT_CLR	W	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

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5.16 MPU_8

MPU_8

5.16.1 MPU_8 Summaries

MPU_8 Summaries

Table 5-2044. MPU_8 Registers, Base Address=4012 0000h, Length=1024

Offset	Length	Register Name	MPU_DTHE Physical Address	MPU_FSS_DATA Physical Address	MPU_HSM Physical Address
0h	32	MPU_8_REVISION	4012 0000h	4016 0000h	4024 0000h
10h	32	MPU_8_INTERRUPT_RAW_STATUS_SET	4012 0010h	4016 0010h	4024 0010h
14h	32	MPU_8_INTERRUPT_ENABLED_STATUS_CLEAR	4012 0014h	4016 0014h	4024 0014h
18h	32	MPU_8_INTERRUPT_ENABLE	4012 0018h	4016 0018h	4024 0018h
1Ch	32	MPU_8_INTERRUPT_ENABLE_CLEAR	4012 001Ch	4016 001Ch	4024 001Ch
200h	32	MPU_8_PROGRAMMABLE_1_START_ADDRESS	4012 0200h	4016 0200h	4024 0200h
204h	32	MPU_8_PROGRAMMABLE_1_END_ADDRESS	4012 0204h	4016 0204h	4024 0204h
208h	32	MPU_8_PROGRAMMABLE_1_MPPA	4012 0208h	4016 0208h	4024 0208h
210h	32	MPU_8_PROGRAMMABLE_2_START_ADDRESS	4012 0210h	4016 0210h	4024 0210h
214h	32	MPU_8_PROGRAMMABLE_2_END_ADDRESS	4012 0214h	4016 0214h	4024 0214h
218h	32	MPU_8_PROGRAMMABLE_2_MPPA	4012 0218h	4016 0218h	4024 0218h
220h	32	MPU_8_PROGRAMMABLE_3_START_ADDRESS	4012 0220h	4016 0220h	4024 0220h
224h	32	MPU_8_PROGRAMMABLE_3_END_ADDRESS	4012 0224h	4016 0224h	4024 0224h
228h	32	MPU_8_PROGRAMMABLE_3_MPPA	4012 0228h	4016 0228h	4024 0228h
230h	32	MPU_8_PROGRAMMABLE_4_START_ADDRESS	4012 0230h	4016 0230h	4024 0230h
234h	32	MPU_8_PROGRAMMABLE_4_END_ADDRESS	4012 0234h	4016 0234h	4024 0234h
238h	32	MPU_8_PROGRAMMABLE_4_MPPA	4012 0238h	4016 0238h	4024 0238h
240h	32	MPU_8_PROGRAMMABLE_5_START_ADDRESS	4012 0240h	4016 0240h	4024 0240h
244h	32	MPU_8_PROGRAMMABLE_5_END_ADDRESS	4012 0244h	4016 0244h	4024 0244h
248h	32	MPU_8_PROGRAMMABLE_5_MPPA	4012 0248h	4016 0248h	4024 0248h
250h	32	MPU_8_PROGRAMMABLE_6_START_ADDRESS	4012 0250h	4016 0250h	4024 0250h
254h	32	MPU_8_PROGRAMMABLE_6_END_ADDRESS	4012 0254h	4016 0254h	4024 0254h
258h	32	MPU_8_PROGRAMMABLE_6_MPPA	4012 0258h	4016 0258h	4024 0258h
260h	32	MPU_8_PROGRAMMABLE_7_START_ADDRESS	4012 0260h	4016 0260h	4024 0260h

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Table 5-2044. MPU_8 Registers, Base Address=4012 0000h, Length=1024 (continued)

Offset	Length	Register Name	MPU_DTHE Physical Address	MPU_FSS_DATA Physical Address	MPU_HSM Physical Address
264h	32	MPU_8_PROGRAMMABLE_7_END_ADDRESS	4012 0264h	4016 0264h	4024 0264h
268h	32	MPU_8_PROGRAMMABLE_7_MPPA	4012 0268h	4016 0268h	4024 0268h
270h	32	MPU_8_PROGRAMMABLE_8_START_ADDRESS	4012 0270h	4016 0270h	4024 0270h
274h	32	MPU_8_PROGRAMMABLE_8_END_ADDRESS	4012 0274h	4016 0274h	4024 0274h
278h	32	MPU_8_PROGRAMMABLE_8_MPPA	4012 0278h	4016 0278h	4024 0278h
300h	32	MPU_8_FAULT_ADDRESS	4012 0300h	4016 0300h	4024 0300h
304h	32	MPU_8_FAULT_STATUS	4012 0304h	4016 0304h	4024 0304h
308h	32	MPU_8_FAULT_CLEAR	4012 0308h	4016 0308h	4024 0308h

Table 5-2045. MPU_8 Registers, Base Address=4012 0000h, Length=1024

Offset	Length	Register Name	MPU_L2OCRAM_BANK0 Physical Address	MPU_L2OCRAM_BANK1 Physical Address	MPU_L2OCRAM_BANK2 Physical Address
0h	32	MPU_8_REVISION	4002 0000h	4004 0000h	4006 0000h
10h	32	MPU_8_INTERRUPT_RAW_STATUS_SET	4002 0010h	4004 0010h	4006 0010h
14h	32	MPU_8_INTERRUPT_ENABLED_STATUS_CLEAR	4002 0014h	4004 0014h	4006 0014h
18h	32	MPU_8_INTERRUPT_ENABLE	4002 0018h	4004 0018h	4006 0018h
1Ch	32	MPU_8_INTERRUPT_ENABLE_CLEAR	4002 001Ch	4004 001Ch	4006 001Ch
200h	32	MPU_8_PROGRAMMABLE_1_START_ADDRESS	4002 0200h	4004 0200h	4006 0200h
204h	32	MPU_8_PROGRAMMABLE_1_END_ADDRESS	4002 0204h	4004 0204h	4006 0204h
208h	32	MPU_8_PROGRAMMABLE_1_MPPA	4002 0208h	4004 0208h	4006 0208h
210h	32	MPU_8_PROGRAMMABLE_2_START_ADDRESS	4002 0210h	4004 0210h	4006 0210h
214h	32	MPU_8_PROGRAMMABLE_2_END_ADDRESS	4002 0214h	4004 0214h	4006 0214h
218h	32	MPU_8_PROGRAMMABLE_2_MPPA	4002 0218h	4004 0218h	4006 0218h
220h	32	MPU_8_PROGRAMMABLE_3_START_ADDRESS	4002 0220h	4004 0220h	4006 0220h
224h	32	MPU_8_PROGRAMMABLE_3_END_ADDRESS	4002 0224h	4004 0224h	4006 0224h
228h	32	MPU_8_PROGRAMMABLE_3_MPPA	4002 0228h	4004 0228h	4006 0228h
230h	32	MPU_8_PROGRAMMABLE_4_START_ADDRESS	4002 0230h	4004 0230h	4006 0230h
234h	32	MPU_8_PROGRAMMABLE_4_END_ADDRESS	4002 0234h	4004 0234h	4006 0234h
238h	32	MPU_8_PROGRAMMABLE_4_MPPA	4002 0238h	4004 0238h	4006 0238h
240h	32	MPU_8_PROGRAMMABLE_5_START_ADDRESS	4002 0240h	4004 0240h	4006 0240h
244h	32	MPU_8_PROGRAMMABLE_5_END_ADDRESS	4002 0244h	4004 0244h	4006 0244h

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Table 5-2045. MPU_8 Registers, Base Address=4012 0000h, Length=1024 (continued)

Offset	Length	Register Name	MPU_L2OCRAM_BANK0 Physical Address	MPU_L2OCRAM_BANK1 Physical Address	MPU_L2OCRAM_BANK2 Physical Address
248h	32	MPU_8_PROGRAMMABLE_5_MPPA	4002 0248h	4004 0248h	4006 0248h
250h	32	MPU_8_PROGRAMMABLE_6_START_ADDRESS	4002 0250h	4004 0250h	4006 0250h
254h	32	MPU_8_PROGRAMMABLE_6_END_ADDRESS	4002 0254h	4004 0254h	4006 0254h
258h	32	MPU_8_PROGRAMMABLE_6_MPPA	4002 0258h	4004 0258h	4006 0258h
260h	32	MPU_8_PROGRAMMABLE_7_START_ADDRESS	4002 0260h	4004 0260h	4006 0260h
264h	32	MPU_8_PROGRAMMABLE_7_END_ADDRESS	4002 0264h	4004 0264h	4006 0264h
268h	32	MPU_8_PROGRAMMABLE_7_MPPA	4002 0268h	4004 0268h	4006 0268h
270h	32	MPU_8_PROGRAMMABLE_8_START_ADDRESS	4002 0270h	4004 0270h	4006 0270h
274h	32	MPU_8_PROGRAMMABLE_8_END_ADDRESS	4002 0274h	4004 0274h	4006 0274h
278h	32	MPU_8_PROGRAMMABLE_8_MPPA	4002 0278h	4004 0278h	4006 0278h
300h	32	MPU_8_FAULT_ADDRESS	4002 0300h	4004 0300h	4006 0300h
304h	32	MPU_8_FAULT_STATUS	4002 0304h	4004 0304h	4006 0304h
308h	32	MPU_8_FAULT_CLEAR	4002 0308h	4004 0308h	4006 0308h

Table 5-2046. MPU_8 Registers, Base Address=4012 0000h, Length=1024

Offset	Length	Register Name	MPU_L2OCRAM_BANK3 Physical Address	MPU_L2OCRAM_BANK4 Physical Address	MPU_L2OCRAM_BANK5 Physical Address
0h	32	MPU_8_REVISION	4008 0000h	402C 0000h	402E 0000h
10h	32	MPU_8_INTERRUPT_RAW_STATUS_SET	4008 0010h	402C 0010h	402E 0010h
14h	32	MPU_8_INTERRUPT_ENABLED_STATUS_CLEAR	4008 0014h	402C 0014h	402E 0014h
18h	32	MPU_8_INTERRUPT_ENABLE	4008 0018h	402C 0018h	402E 0018h
1Ch	32	MPU_8_INTERRUPT_ENABLE_CLEAR	4008 001Ch	402C 001Ch	402E 001Ch
200h	32	MPU_8_PROGRAMMABLE_1_START_ADDRESS	4008 0200h	402C 0200h	402E 0200h
204h	32	MPU_8_PROGRAMMABLE_1_END_ADDRESS	4008 0204h	402C 0204h	402E 0204h
208h	32	MPU_8_PROGRAMMABLE_1_MPPA	4008 0208h	402C 0208h	402E 0208h
210h	32	MPU_8_PROGRAMMABLE_2_START_ADDRESS	4008 0210h	402C 0210h	402E 0210h
214h	32	MPU_8_PROGRAMMABLE_2_END_ADDRESS	4008 0214h	402C 0214h	402E 0214h
218h	32	MPU_8_PROGRAMMABLE_2_MPPA	4008 0218h	402C 0218h	402E 0218h
220h	32	MPU_8_PROGRAMMABLE_3_START_ADDRESS	4008 0220h	402C 0220h	402E 0220h
224h	32	MPU_8_PROGRAMMABLE_3_END_ADDRESS	4008 0224h	402C 0224h	402E 0224h
228h	32	MPU_8_PROGRAMMABLE_3_MPPA	4008 0228h	402C 0228h	402E 0228h

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Table 5-2046. MPU_8 Registers, Base Address=4012 0000h, Length=1024 (continued)

Offset	Length	Register Name	MPU_L2OCRAM_BANK3 Physical Address	MPU_L2OCRAM_BANK4 Physical Address	MPU_L2OCRAM_BANK5 Physical Address
230h	32	MPU_8_PROGRAMMABLE_4_START_ADDRESS	4008 0230h	402C 0230h	402E 0230h
234h	32	MPU_8_PROGRAMMABLE_4_END_ADDRESS	4008 0234h	402C 0234h	402E 0234h
238h	32	MPU_8_PROGRAMMABLE_4_MPPA	4008 0238h	402C 0238h	402E 0238h
240h	32	MPU_8_PROGRAMMABLE_5_START_ADDRESS	4008 0240h	402C 0240h	402E 0240h
244h	32	MPU_8_PROGRAMMABLE_5_END_ADDRESS	4008 0244h	402C 0244h	402E 0244h
248h	32	MPU_8_PROGRAMMABLE_5_MPPA	4008 0248h	402C 0248h	402E 0248h
250h	32	MPU_8_PROGRAMMABLE_6_START_ADDRESS	4008 0250h	402C 0250h	402E 0250h
254h	32	MPU_8_PROGRAMMABLE_6_END_ADDRESS	4008 0254h	402C 0254h	402E 0254h
258h	32	MPU_8_PROGRAMMABLE_6_MPPA	4008 0258h	402C 0258h	402E 0258h
260h	32	MPU_8_PROGRAMMABLE_7_START_ADDRESS	4008 0260h	402C 0260h	402E 0260h
264h	32	MPU_8_PROGRAMMABLE_7_END_ADDRESS	4008 0264h	402C 0264h	402E 0264h
268h	32	MPU_8_PROGRAMMABLE_7_MPPA	4008 0268h	402C 0268h	402E 0268h
270h	32	MPU_8_PROGRAMMABLE_8_START_ADDRESS	4008 0270h	402C 0270h	402E 0270h
274h	32	MPU_8_PROGRAMMABLE_8_END_ADDRESS	4008 0274h	402C 0274h	402E 0274h
278h	32	MPU_8_PROGRAMMABLE_8_MPPA	4008 0278h	402C 0278h	402E 0278h
300h	32	MPU_8_FAULT_ADDRESS	4008 0300h	402C 0300h	402E 0300h
304h	32	MPU_8_FAULT_STATUS	4008 0304h	402C 0304h	402E 0304h
308h	32	MPU_8_FAULT_CLEAR	4008 0308h	402C 0308h	402E 0308h

Table 5-2047. MPU_8 Registers, Base Address=4012 0000h, Length=1024

Offset	Length	Register Name	MPU_MBOX_SRAM Physical Address	MPU_R5SS0_CORE0_AXIS Physical Address	MPU_R5SS0_CORE1_AXIS Physical Address
0h	32	MPU_8_REVISION	4014 0000h	400A 0000h	400C 0000h
10h	32	MPU_8_INTERRUPT_RAW_STATUS_SET	4014 0010h	400A 0010h	400C 0010h
14h	32	MPU_8_INTERRUPT_ENABLED_STATUS_CLEAR	4014 0014h	400A 0014h	400C 0014h
18h	32	MPU_8_INTERRUPT_ENABLE	4014 0018h	400A 0018h	400C 0018h
1Ch	32	MPU_8_INTERRUPT_ENABLE_CLEAR	4014 001Ch	400A 001Ch	400C 001Ch
200h	32	MPU_8_PROGRAMMABLE_1_START_ADDRESS	4014 0200h	400A 0200h	400C 0200h
204h	32	MPU_8_PROGRAMMABLE_1_END_ADDRESS	4014 0204h	400A 0204h	400C 0204h
208h	32	MPU_8_PROGRAMMABLE_1_MPPA	4014 0208h	400A 0208h	400C 0208h
210h	32	MPU_8_PROGRAMMABLE_2_START_ADDRESS	4014 0210h	400A 0210h	400C 0210h

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Table 5-2047. MPU_8 Registers, Base Address=4012 0000h, Length=1024 (continued)

Offset	Length	Register Name	MPU_MBOX_SRAM Physical Address	MPU_R5SS0_CORE0_AXIS Physical Address	MPU_R5SS0_CORE1_AXIS Physical Address
214h	32	MPU_8_PROGRAMMABLE_2_END_ADDRESS	4014 0214h	400A 0214h	400C 0214h
218h	32	MPU_8_PROGRAMMABLE_2_MPPA	4014 0218h	400A 0218h	400C 0218h
220h	32	MPU_8_PROGRAMMABLE_3_START_ADDRESS	4014 0220h	400A 0220h	400C 0220h
224h	32	MPU_8_PROGRAMMABLE_3_END_ADDRESS	4014 0224h	400A 0224h	400C 0224h
228h	32	MPU_8_PROGRAMMABLE_3_MPPA	4014 0228h	400A 0228h	400C 0228h
230h	32	MPU_8_PROGRAMMABLE_4_START_ADDRESS	4014 0230h	400A 0230h	400C 0230h
234h	32	MPU_8_PROGRAMMABLE_4_END_ADDRESS	4014 0234h	400A 0234h	400C 0234h
238h	32	MPU_8_PROGRAMMABLE_4_MPPA	4014 0238h	400A 0238h	400C 0238h
240h	32	MPU_8_PROGRAMMABLE_5_START_ADDRESS	4014 0240h	400A 0240h	400C 0240h
244h	32	MPU_8_PROGRAMMABLE_5_END_ADDRESS	4014 0244h	400A 0244h	400C 0244h
248h	32	MPU_8_PROGRAMMABLE_5_MPPA	4014 0248h	400A 0248h	400C 0248h
250h	32	MPU_8_PROGRAMMABLE_6_START_ADDRESS	4014 0250h	400A 0250h	400C 0250h
254h	32	MPU_8_PROGRAMMABLE_6_END_ADDRESS	4014 0254h	400A 0254h	400C 0254h
258h	32	MPU_8_PROGRAMMABLE_6_MPPA	4014 0258h	400A 0258h	400C 0258h
260h	32	MPU_8_PROGRAMMABLE_7_START_ADDRESS	4014 0260h	400A 0260h	400C 0260h
264h	32	MPU_8_PROGRAMMABLE_7_END_ADDRESS	4014 0264h	400A 0264h	400C 0264h
268h	32	MPU_8_PROGRAMMABLE_7_MPPA	4014 0268h	400A 0268h	400C 0268h
270h	32	MPU_8_PROGRAMMABLE_8_START_ADDRESS	4014 0270h	400A 0270h	400C 0270h
274h	32	MPU_8_PROGRAMMABLE_8_END_ADDRESS	4014 0274h	400A 0274h	400C 0274h
278h	32	MPU_8_PROGRAMMABLE_8_MPPA	4014 0278h	400A 0278h	400C 0278h
300h	32	MPU_8_FAULT_ADDRESS	4014 0300h	400A 0300h	400C 0300h
304h	32	MPU_8_FAULT_STATUS	4014 0304h	400A 0304h	400C 0304h
308h	32	MPU_8_FAULT_CLEAR	4014 0308h	400A 0308h	400C 0308h

Table 5-2048. MPU_8 Registers, Base Address=4012 0000h, Length=1024

Offset	Length	Register Name	MPU_R5SS1_CORE0_AXIS Physical Address	MPU_R5SS1_CORE1_AXIS Physical Address
0h	32	MPU_8_REVISION	400E 0000h	4010 0000h
10h	32	MPU_8_INTERRUPT_RAW_STATUS_SET	400E 0010h	4010 0010h
14h	32	MPU_8_INTERRUPT_ENABLED_STATUS_CLEAR	400E 0014h	4010 0014h
18h	32	MPU_8_INTERRUPT_ENABLE	400E 0018h	4010 0018h

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Table 5-2048. MPU_8 Registers, Base Address=4012 0000h, Length=1024 (continued)

Offset	Length	Register Name	MPU_R5SS1_CORE0_AXIS Physical Address	MPU_R5SS1_CORE1_AXIS Physical Address
1Ch	32	MPU_8_INTERRUPT_ENABLE_CLEAR	400E 001Ch	4010 001Ch
200h	32	MPU_8_PROGRAMMABLE_1_START_ADDRESS	400E 0200h	4010 0200h
204h	32	MPU_8_PROGRAMMABLE_1_END_ADDRESS	400E 0204h	4010 0204h
208h	32	MPU_8_PROGRAMMABLE_1_MPPA	400E 0208h	4010 0208h
210h	32	MPU_8_PROGRAMMABLE_2_START_ADDRESS	400E 0210h	4010 0210h
214h	32	MPU_8_PROGRAMMABLE_2_END_ADDRESS	400E 0214h	4010 0214h
218h	32	MPU_8_PROGRAMMABLE_2_MPPA	400E 0218h	4010 0218h
220h	32	MPU_8_PROGRAMMABLE_3_START_ADDRESS	400E 0220h	4010 0220h
224h	32	MPU_8_PROGRAMMABLE_3_END_ADDRESS	400E 0224h	4010 0224h
228h	32	MPU_8_PROGRAMMABLE_3_MPPA	400E 0228h	4010 0228h
230h	32	MPU_8_PROGRAMMABLE_4_START_ADDRESS	400E 0230h	4010 0230h
234h	32	MPU_8_PROGRAMMABLE_4_END_ADDRESS	400E 0234h	4010 0234h
238h	32	MPU_8_PROGRAMMABLE_4_MPPA	400E 0238h	4010 0238h
240h	32	MPU_8_PROGRAMMABLE_5_START_ADDRESS	400E 0240h	4010 0240h
244h	32	MPU_8_PROGRAMMABLE_5_END_ADDRESS	400E 0244h	4010 0244h
248h	32	MPU_8_PROGRAMMABLE_5_MPPA	400E 0248h	4010 0248h
250h	32	MPU_8_PROGRAMMABLE_6_START_ADDRESS	400E 0250h	4010 0250h
254h	32	MPU_8_PROGRAMMABLE_6_END_ADDRESS	400E 0254h	4010 0254h
258h	32	MPU_8_PROGRAMMABLE_6_MPPA	400E 0258h	4010 0258h
260h	32	MPU_8_PROGRAMMABLE_7_START_ADDRESS	400E 0260h	4010 0260h
264h	32	MPU_8_PROGRAMMABLE_7_END_ADDRESS	400E 0264h	4010 0264h
268h	32	MPU_8_PROGRAMMABLE_7_MPPA	400E 0268h	4010 0268h
270h	32	MPU_8_PROGRAMMABLE_8_START_ADDRESS	400E 0270h	4010 0270h
274h	32	MPU_8_PROGRAMMABLE_8_END_ADDRESS	400E 0274h	4010 0274h
278h	32	MPU_8_PROGRAMMABLE_8_MPPA	400E 0278h	4010 0278h
300h	32	MPU_8_FAULT_ADDRESS	400E 0300h	4010 0300h
304h	32	MPU_8_FAULT_STATUS	400E 0304h	4010 0304h
308h	32	MPU_8_FAULT_CLEAR	400E 0308h	4010 0308h

5.16.2 MPU_8 Registers

MPU_8 Registers

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5.16.2.1 MPU_8_REVISION Register

5.16.2.1.1 MPU_8_REVISION Register (Offset = 0h) [reset = 4E815101h]

Revision.

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Table 5-2049. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0000h
MPU_FSS_DATA	4016 0000h
MPU_HSM	4024 0000h
MPU_L2OCRAM_BANK0	4002 0000h
MPU_L2OCRAM_BANK1	4004 0000h
MPU_L2OCRAM_BANK2	4006 0000h
MPU_L2OCRAM_BANK3	4008 0000h
MPU_L2OCRAM_BANK4	402C 0000h
MPU_L2OCRAM_BANK5	402E 0000h
MPU_MBOX_SRAM	4014 0000h
MPU_R5SS0_CORE0_AXIS	400A 0000h
MPU_R5SS0_CORE1_AXIS	400C 0000h
MPU_R5SS1_CORE0_AXIS	400E 0000h
MPU_R5SS1_CORE1_AXIS	4010 0000h

Figure 5-1001. MPU_8_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		MODID			
R		R		R			
1h		0h		E81h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODID							
R							
E81h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
Ah					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REVCUSTOM		REVMIN					
R		R					
0h		1h					

Table 5-2050. MPU_8_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme.
29:28	RESERVED	R	0h	Always read a s0. Writes have no affect.
27:16	MODID	R	E81h	Module ID field.
15:11	REVRTL	R	Ah	RTL revision.Will vary depending on release.
10:8	REVMAJ	R	1h	Major revision.
7:6	REVCUSTOM	R	0h	Custom revision.

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Table 5-2050. MPU_8_REVISION Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	REVMIN	R	1h	Minor revision.

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5.16.2.2 MPU_8_INTERRUPT_RAW_STATUS_SET Register

5.16.2.2.1 MPU_8_INTERRUPT_RAW_STATUS_SET Register (Offset = 10h) [reset = 0h]

Interrupt_Raw_Status_Set.

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Table 5-2051. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0010h
MPU_FSS_DATA	4016 0010h
MPU_HSM	4024 0010h
MPU_L2OCRAM_BANK0	4002 0010h
MPU_L2OCRAM_BANK1	4004 0010h
MPU_L2OCRAM_BANK2	4006 0010h
MPU_L2OCRAM_BANK3	4008 0010h
MPU_L2OCRAM_BANK4	402C 0010h
MPU_L2OCRAM_BANK5	402E 0010h
MPU_MBOX_SRAM	4014 0010h
MPU_R5SS0_CORE0_AXIS	400A 0010h
MPU_R5SS0_CORE1_AXIS	400C 0010h
MPU_R5SS1_CORE0_AXIS	400E 0010h
MPU_R5SS1_CORE1_AXIS	4010 0010h

Figure 5-1002. MPU_8_INTERRUPT_RAW_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						ADDR_ERR	PROT_ERR
R						R/W1TS	R/W1TS
0h						0h	0h

Table 5-2052. MPU_8_INTERRUPT_RAW_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read.Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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5.16.2.3 MPU_8_INTERRUPT_ENABLED_STATUS_CLEAR Register

5.16.2.3.1 MPU_8_INTERRUPT_ENABLED_STATUS_CLEAR Register (Offset = 14h) [reset = 0h]

Interrupt_Enabled_Status_Clear.

Return to Summary Table

Table 5-2053. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0014h
MPU_FSS_DATA	4016 0014h
MPU_HSM	4024 0014h
MPU_L2OCRAM_BANK0	4002 0014h
MPU_L2OCRAM_BANK1	4004 0014h
MPU_L2OCRAM_BANK2	4006 0014h
MPU_L2OCRAM_BANK3	4008 0014h
MPU_L2OCRAM_BANK4	402C 0014h
MPU_L2OCRAM_BANK5	402E 0014h
MPU_MBOX_SRAM	4014 0014h
MPU_R5SS0_CORE0_AXIS	400A 0014h
MPU_R5SS0_CORE1_AXIS	400C 0014h
MPU_R5SS1_CORE0_AXIS	400E 0014h
MPU_R5SS1_CORE1_AXIS	4010 0014h

Figure 5-1003. MPU_8_INTERRUPT_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						ENABLED_ADDR_ERR	ENABLED_PROT_ERR
R						R/W0TC	R/W0TC
0h						0h	0h

Table 5-2054. MPU_8_INTERRUPT_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ENABLED_ADDR_ERR	R/W0TC	0h	Addressing violation error. Enabled status is read.Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	R/W0TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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5.16.2.4 MPU_8_INTERRUPT_ENABLE Register

5.16.2.4.1 MPU_8_INTERRUPT_ENABLE Register (Offset = 18h) [reset = 0h]

Interrupt_Enable.

Return to Summary Table

Table 5-2055. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0018h
MPU_FSS_DATA	4016 0018h
MPU_HSM	4024 0018h
MPU_L2OCRAM_BANK0	4002 0018h
MPU_L2OCRAM_BANK1	4004 0018h
MPU_L2OCRAM_BANK2	4006 0018h
MPU_L2OCRAM_BANK3	4008 0018h
MPU_L2OCRAM_BANK4	402C 0018h
MPU_L2OCRAM_BANK5	402E 0018h
MPU_MBOX_SRAM	4014 0018h
MPU_R5SS0_CORE0_AXIS	400A 0018h
MPU_R5SS0_CORE1_AXIS	400C 0018h
MPU_R5SS1_CORE0_AXIS	400E 0018h
MPU_R5SS1_CORE1_AXIS	4010 0018h

Figure 5-1004. MPU_8_INTERRUPT_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						ADDR_ERR_EN	PROT_ERR_EN
R						R/W1TS	R/W1TS
0h						0h	0h

Table 5-2056. MPU_8_INTERRUPT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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5.16.2.5 MPU_8_INTERRUPT_ENABLE_CLEAR Register

5.16.2.5.1 MPU_8_INTERRUPT_ENABLE_CLEAR Register (Offset = 1Ch) [reset = 0h]

Interrupt_Enable_Clear.

Return to Summary Table

Table 5-2057. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 001Ch
MPU_FSS_DATA	4016 001Ch
MPU_HSM	4024 001Ch
MPU_L2OCRAM_BANK0	4002 001Ch
MPU_L2OCRAM_BANK1	4004 001Ch
MPU_L2OCRAM_BANK2	4006 001Ch
MPU_L2OCRAM_BANK3	4008 001Ch
MPU_L2OCRAM_BANK4	402C 001Ch
MPU_L2OCRAM_BANK5	402E 001Ch
MPU_MBOX_SRAM	4014 001Ch
MPU_R5SS0_CORE0_AXIS	400A 001Ch
MPU_R5SS0_CORE1_AXIS	400C 001Ch
MPU_R5SS1_CORE0_AXIS	400E 001Ch
MPU_R5SS1_CORE1_AXIS	4010 001Ch

Figure 5-1005. MPU_8_INTERRUPT_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
R						R/W0TC	R/W0TC
0h						0h	0h

Table 5-2058. MPU_8_INTERRUPT_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ADDR_ERR_EN_CLR	R/W0TC	0h	Addressing violation error enable. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	R/W0TC	0h	Protection violation error enable. Write a 1 to clear the enable. Writing a 0 has no effect.

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5.16.2.6 MPU_8_PROGRAMMABLE_1_START_ADDRESS Register

5.16.2.6.1 MPU_8_PROGRAMMABLE_1_START_ADDRESS Register (Offset = 200h) [reset = 0h]

Programmable_1_Start_Address.

Return to Summary Table

Table 5-2059. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0200h
MPU_FSS_DATA	4016 0200h
MPU_HSM	4024 0200h
MPU_L2OCRAM_BANK0	4002 0200h
MPU_L2OCRAM_BANK1	4004 0200h
MPU_L2OCRAM_BANK2	4006 0200h
MPU_L2OCRAM_BANK3	4008 0200h
MPU_L2OCRAM_BANK4	402C 0200h
MPU_L2OCRAM_BANK5	402E 0200h
MPU_MBOX_SRAM	4014 0200h
MPU_R5SS0_CORE0_AXIS	400A 0200h
MPU_R5SS0_CORE1_AXIS	400C 0200h
MPU_R5SS1_CORE0_AXIS	400E 0200h
MPU_R5SS1_CORE1_AXIS	4010 0200h

Figure 5-1006. MPU_8_PROGRAMMABLE_1_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2060. MPU_8_PROGRAMMABLE_1_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.16.2.7 MPU_8_PROGRAMMABLE_1_END_ADDRESS Register

5.16.2.7.1 MPU_8_PROGRAMMABLE_1_END_ADDRESS Register (Offset = 204h) [reset = 0h]

Programmable_1_End_Address.

Return to Summary Table

Table 5-2061. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0204h
MPU_FSS_DATA	4016 0204h
MPU_HSM	4024 0204h
MPU_L2OCRAM_BANK0	4002 0204h
MPU_L2OCRAM_BANK1	4004 0204h
MPU_L2OCRAM_BANK2	4006 0204h
MPU_L2OCRAM_BANK3	4008 0204h
MPU_L2OCRAM_BANK4	402C 0204h
MPU_L2OCRAM_BANK5	402E 0204h
MPU_MBOX_SRAM	4014 0204h
MPU_R5SS0_CORE0_AXIS	400A 0204h
MPU_R5SS0_CORE1_AXIS	400C 0204h
MPU_R5SS1_CORE0_AXIS	400E 0204h
MPU_R5SS1_CORE1_AXIS	4010 0204h

Figure 5-1007. MPU_8_PROGRAMMABLE_1_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2062. MPU_8_PROGRAMMABLE_1_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.16.2.8 MPU_8_PROGRAMMABLE_1_MPPA Register

5.16.2.8.1 MPU_8_PROGRAMMABLE_1_MPPA Register (Offset = 208h) [reset = 0h]

Programmable_1_MPPA.

Return to Summary Table

Table 5-2063. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0208h
MPU_FSS_DATA	4016 0208h
MPU_HSM	4024 0208h
MPU_L2OCRAM_BANK0	4002 0208h
MPU_L2OCRAM_BANK1	4004 0208h
MPU_L2OCRAM_BANK2	4006 0208h
MPU_L2OCRAM_BANK3	4008 0208h
MPU_L2OCRAM_BANK4	402C 0208h
MPU_L2OCRAM_BANK5	402E 0208h
MPU_MBOX_SRAM	4014 0208h
MPU_R5SS0_CORE0_AXIS	400A 0208h
MPU_R5SS0_CORE1_AXIS	400C 0208h
MPU_R5SS1_CORE0_AXIS	400E 0208h
MPU_R5SS1_CORE1_AXIS	4010 0208h

Figure 5-1008. MPU_8_PROGRAMMABLE_1_MPPA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED3</td><td>LOCK</td><td colspan="2">RESERVED2</td><td colspan="2">AID15_0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="2">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">AID15_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">AID15_0</td><td>AIDX</td><td>RESERVED1</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>NS</td><td>EMU</td><td>SR</td><td>SW</td><td>SX</td><td>UR</td><td>UW</td><td>UX</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-2064. MPU_8_PROGRAMMABLE_1_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.

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Table 5-2064. MPU_8_PROGRAMMABLE_1_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.16.2.9 MPU_8_PROGRAMMABLE_2_START_ADDRESS Register

5.16.2.9.1 MPU_8_PROGRAMMABLE_2_START_ADDRESS Register (Offset = 210h) [reset = 0h]

Programmable_2_Start_Address.

Return to Summary Table

Table 5-2065. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0210h
MPU_FSS_DATA	4016 0210h
MPU_HSM	4024 0210h
MPU_L2OCRAM_BANK0	4002 0210h
MPU_L2OCRAM_BANK1	4004 0210h
MPU_L2OCRAM_BANK2	4006 0210h
MPU_L2OCRAM_BANK3	4008 0210h
MPU_L2OCRAM_BANK4	402C 0210h
MPU_L2OCRAM_BANK5	402E 0210h
MPU_MBOX_SRAM	4014 0210h
MPU_R5SS0_CORE0_AXIS	400A 0210h
MPU_R5SS0_CORE1_AXIS	400C 0210h
MPU_R5SS1_CORE0_AXIS	400E 0210h
MPU_R5SS1_CORE1_AXIS	4010 0210h

Figure 5-1009. MPU_8_PROGRAMMABLE_2_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2066. MPU_8_PROGRAMMABLE_2_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.16.2.10 MPU_8_PROGRAMMABLE_2_END_ADDRESS Register

5.16.2.10.1 MPU_8_PROGRAMMABLE_2_END_ADDRESS Register (Offset = 214h) [reset = 0h]

Programmable_2_End_Address.

Return to Summary Table

Table 5-2067. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0214h
MPU_FSS_DATA	4016 0214h
MPU_HSM	4024 0214h
MPU_L2OCRAM_BANK0	4002 0214h
MPU_L2OCRAM_BANK1	4004 0214h
MPU_L2OCRAM_BANK2	4006 0214h
MPU_L2OCRAM_BANK3	4008 0214h
MPU_L2OCRAM_BANK4	402C 0214h
MPU_L2OCRAM_BANK5	402E 0214h
MPU_MBOX_SRAM	4014 0214h
MPU_R5SS0_CORE0_AXIS	400A 0214h
MPU_R5SS0_CORE1_AXIS	400C 0214h
MPU_R5SS1_CORE0_AXIS	400E 0214h
MPU_R5SS1_CORE1_AXIS	4010 0214h

Figure 5-1010. MPU_8_PROGRAMMABLE_2_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDR							
R/W							
0h							

Table 5-2068. MPU_8_PROGRAMMABLE_2_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.16.2.11 MPU_8_PROGRAMMABLE_2_MPPA Register

5.16.2.11.1 MPU_8_PROGRAMMABLE_2_MPPA Register (Offset = 218h) [reset = 0h]

Programmable_2_MPPA.

Return to Summary Table

Table 5-2069. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0218h
MPU_FSS_DATA	4016 0218h
MPU_HSM	4024 0218h
MPU_L2OCRAM_BANK0	4002 0218h
MPU_L2OCRAM_BANK1	4004 0218h
MPU_L2OCRAM_BANK2	4006 0218h
MPU_L2OCRAM_BANK3	4008 0218h
MPU_L2OCRAM_BANK4	402C 0218h
MPU_L2OCRAM_BANK5	402E 0218h
MPU_MBOX_SRAM	4014 0218h
MPU_R5SS0_CORE0_AXIS	400A 0218h
MPU_R5SS0_CORE1_AXIS	400C 0218h
MPU_R5SS1_CORE0_AXIS	400E 0218h
MPU_R5SS1_CORE1_AXIS	4010 0218h

Figure 5-1011. MPU_8_PROGRAMMABLE_2_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2070. MPU_8_PROGRAMMABLE_2_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.

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Table 5-2070. MPU_8_PROGRAMMABLE_2_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.16.2.12 MPU_8_PROGRAMMABLE_3_START_ADDRESS Register

5.16.2.12.1 MPU_8_PROGRAMMABLE_3_START_ADDRESS Register (Offset = 220h) [reset = 0h]

Programmable_3_Start_Address.

Return to Summary Table

Table 5-2071. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0220h
MPU_FSS_DATA	4016 0220h
MPU_HSM	4024 0220h
MPU_L2OCRAM_BANK0	4002 0220h
MPU_L2OCRAM_BANK1	4004 0220h
MPU_L2OCRAM_BANK2	4006 0220h
MPU_L2OCRAM_BANK3	4008 0220h
MPU_L2OCRAM_BANK4	402C 0220h
MPU_L2OCRAM_BANK5	402E 0220h
MPU_MBOX_SRAM	4014 0220h
MPU_R5SS0_CORE0_AXIS	400A 0220h
MPU_R5SS0_CORE1_AXIS	400C 0220h
MPU_R5SS1_CORE0_AXIS	400E 0220h
MPU_R5SS1_CORE1_AXIS	4010 0220h

Figure 5-1012. MPU_8_PROGRAMMABLE_3_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2072. MPU_8_PROGRAMMABLE_3_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.16.2.13 MPU_8_PROGRAMMABLE_3_END_ADDRESS Register

5.16.2.13.1 MPU_8_PROGRAMMABLE_3_END_ADDRESS Register (Offset = 224h) [reset = 0h]

Programmable_3_End_Address.

Return to Summary Table

Table 5-2073. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0224h
MPU_FSS_DATA	4016 0224h
MPU_HSM	4024 0224h
MPU_L2OCRAM_BANK0	4002 0224h
MPU_L2OCRAM_BANK1	4004 0224h
MPU_L2OCRAM_BANK2	4006 0224h
MPU_L2OCRAM_BANK3	4008 0224h
MPU_L2OCRAM_BANK4	402C 0224h
MPU_L2OCRAM_BANK5	402E 0224h
MPU_MBOX_SRAM	4014 0224h
MPU_R5SS0_CORE0_AXIS	400A 0224h
MPU_R5SS0_CORE1_AXIS	400C 0224h
MPU_R5SS1_CORE0_AXIS	400E 0224h
MPU_R5SS1_CORE1_AXIS	4010 0224h

Figure 5-1013. MPU_8_PROGRAMMABLE_3_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2074. MPU_8_PROGRAMMABLE_3_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.16.2.14 MPU_8_PROGRAMMABLE_3_MPPA Register

5.16.2.14.1 MPU_8_PROGRAMMABLE_3_MPPA Register (Offset = 228h) [reset = 0h]

Programmable_3_MPPA.

Return to Summary Table

Table 5-2075. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0228h
MPU_FSS_DATA	4016 0228h
MPU_HSM	4024 0228h
MPU_L2OCRAM_BANK0	4002 0228h
MPU_L2OCRAM_BANK1	4004 0228h
MPU_L2OCRAM_BANK2	4006 0228h
MPU_L2OCRAM_BANK3	4008 0228h
MPU_L2OCRAM_BANK4	402C 0228h
MPU_L2OCRAM_BANK5	402E 0228h
MPU_MBOX_SRAM	4014 0228h
MPU_R5SS0_CORE0_AXIS	400A 0228h
MPU_R5SS0_CORE1_AXIS	400C 0228h
MPU_R5SS1_CORE0_AXIS	400E 0228h
MPU_R5SS1_CORE1_AXIS	4010 0228h

Figure 5-1014. MPU_8_PROGRAMMABLE_3_MPPA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED3</td><td>LOCK</td><td colspan="2">RESERVED2</td><td colspan="2">AID15_0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="2">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">AID15_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">AID15_0</td><td>AIDX</td><td>RESERVED1</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>NS</td><td>EMU</td><td>SR</td><td>SW</td><td>SX</td><td>UR</td><td>UW</td><td>UX</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-2076. MPU_8_PROGRAMMABLE_3_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.

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Table 5-2076. MPU_8_PROGRAMMABLE_3_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.16.2.15 MPU_8_PROGRAMMABLE_4_START_ADDRESS Register

5.16.2.15.1 MPU_8_PROGRAMMABLE_4_START_ADDRESS Register (Offset = 230h) [reset = 0h]

Programmable_4_Start_Address.

Return to Summary Table

Table 5-2077. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0230h
MPU_FSS_DATA	4016 0230h
MPU_HSM	4024 0230h
MPU_L2OCRAM_BANK0	4002 0230h
MPU_L2OCRAM_BANK1	4004 0230h
MPU_L2OCRAM_BANK2	4006 0230h
MPU_L2OCRAM_BANK3	4008 0230h
MPU_L2OCRAM_BANK4	402C 0230h
MPU_L2OCRAM_BANK5	402E 0230h
MPU_MBOX_SRAM	4014 0230h
MPU_R5SS0_CORE0_AXIS	400A 0230h
MPU_R5SS0_CORE1_AXIS	400C 0230h
MPU_R5SS1_CORE0_AXIS	400E 0230h
MPU_R5SS1_CORE1_AXIS	4010 0230h

Figure 5-1015. MPU_8_PROGRAMMABLE_4_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2078. MPU_8_PROGRAMMABLE_4_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.16.2.16 MPU_8_PROGRAMMABLE_4_END_ADDRESS Register

5.16.2.16.1 MPU_8_PROGRAMMABLE_4_END_ADDRESS Register (Offset = 234h) [reset = 0h]

Programmable_4_End_Address.

Return to Summary Table

Table 5-2079. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0234h
MPU_FSS_DATA	4016 0234h
MPU_HSM	4024 0234h
MPU_L2OCRAM_BANK0	4002 0234h
MPU_L2OCRAM_BANK1	4004 0234h
MPU_L2OCRAM_BANK2	4006 0234h
MPU_L2OCRAM_BANK3	4008 0234h
MPU_L2OCRAM_BANK4	402C 0234h
MPU_L2OCRAM_BANK5	402E 0234h
MPU_MBOX_SRAM	4014 0234h
MPU_R5SS0_CORE0_AXIS	400A 0234h
MPU_R5SS0_CORE1_AXIS	400C 0234h
MPU_R5SS1_CORE0_AXIS	400E 0234h
MPU_R5SS1_CORE1_AXIS	4010 0234h

Figure 5-1016. MPU_8_PROGRAMMABLE_4_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2080. MPU_8_PROGRAMMABLE_4_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.16.2.17 MPU_8_PROGRAMMABLE_4_MPPA Register

5.16.2.17.1 MPU_8_PROGRAMMABLE_4_MPPA Register (Offset = 238h) [reset = 0h]

Programmable_4_MPPA.

Return to Summary Table

Table 5-2081. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0238h
MPU_FSS_DATA	4016 0238h
MPU_HSM	4024 0238h
MPU_L2OCRAM_BANK0	4002 0238h
MPU_L2OCRAM_BANK1	4004 0238h
MPU_L2OCRAM_BANK2	4006 0238h
MPU_L2OCRAM_BANK3	4008 0238h
MPU_L2OCRAM_BANK4	402C 0238h
MPU_L2OCRAM_BANK5	402E 0238h
MPU_MBOX_SRAM	4014 0238h
MPU_R5SS0_CORE0_AXIS	400A 0238h
MPU_R5SS0_CORE1_AXIS	400C 0238h
MPU_R5SS1_CORE0_AXIS	400E 0238h
MPU_R5SS1_CORE1_AXIS	4010 0238h

Figure 5-1017. MPU_8_PROGRAMMABLE_4_MPPA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED3</td><td>LOCK</td><td colspan="2">RESERVED2</td><td colspan="2">AID15_0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="2">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">AID15_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">AID15_0</td><td>AIDX</td><td>RESERVED1</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>NS</td><td>EMU</td><td>SR</td><td>SW</td><td>SX</td><td>UR</td><td>UW</td><td>UX</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-2082. MPU_8_PROGRAMMABLE_4_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will reset clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.

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Table 5-2082. MPU_8_PROGRAMMABLE_4_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.16.2.18 MPU_8_PROGRAMMABLE_5_START_ADDRESS Register

5.16.2.18.1 MPU_8_PROGRAMMABLE_5_START_ADDRESS Register (Offset = 240h) [reset = 0h]

Programmable_5_Start_Address.

Return to Summary Table

Table 5-2083. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0240h
MPU_FSS_DATA	4016 0240h
MPU_HSM	4024 0240h
MPU_L2OCRAM_BANK0	4002 0240h
MPU_L2OCRAM_BANK1	4004 0240h
MPU_L2OCRAM_BANK2	4006 0240h
MPU_L2OCRAM_BANK3	4008 0240h
MPU_L2OCRAM_BANK4	402C 0240h
MPU_L2OCRAM_BANK5	402E 0240h
MPU_MBOX_SRAM	4014 0240h
MPU_R5SS0_CORE0_AXIS	400A 0240h
MPU_R5SS0_CORE1_AXIS	400C 0240h
MPU_R5SS1_CORE0_AXIS	400E 0240h
MPU_R5SS1_CORE1_AXIS	4010 0240h

Figure 5-1018. MPU_8_PROGRAMMABLE_5_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2084. MPU_8_PROGRAMMABLE_5_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.16.2.19 MPU_8_PROGRAMMABLE_5_END_ADDRESS Register

5.16.2.19.1 MPU_8_PROGRAMMABLE_5_END_ADDRESS Register (Offset = 244h) [reset = 0h]

Programmable_5_End_Address.

Return to Summary Table

Table 5-2085. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0244h
MPU_FSS_DATA	4016 0244h
MPU_HSM	4024 0244h
MPU_L2OCRAM_BANK0	4002 0244h
MPU_L2OCRAM_BANK1	4004 0244h
MPU_L2OCRAM_BANK2	4006 0244h
MPU_L2OCRAM_BANK3	4008 0244h
MPU_L2OCRAM_BANK4	402C 0244h
MPU_L2OCRAM_BANK5	402E 0244h
MPU_MBOX_SRAM	4014 0244h
MPU_R5SS0_CORE0_AXIS	400A 0244h
MPU_R5SS0_CORE1_AXIS	400C 0244h
MPU_R5SS1_CORE0_AXIS	400E 0244h
MPU_R5SS1_CORE1_AXIS	4010 0244h

Figure 5-1019. MPU_8_PROGRAMMABLE_5_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2086. MPU_8_PROGRAMMABLE_5_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.16.2.20 MPU_8_PROGRAMMABLE_5_MPPA Register

5.16.2.20.1 MPU_8_PROGRAMMABLE_5_MPPA Register (Offset = 248h) [reset = 0h]

Programmable_5_MPPA.

Return to Summary Table

Table 5-2087. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0248h
MPU_FSS_DATA	4016 0248h
MPU_HSM	4024 0248h
MPU_L2OCRAM_BANK0	4002 0248h
MPU_L2OCRAM_BANK1	4004 0248h
MPU_L2OCRAM_BANK2	4006 0248h
MPU_L2OCRAM_BANK3	4008 0248h
MPU_L2OCRAM_BANK4	402C 0248h
MPU_L2OCRAM_BANK5	402E 0248h
MPU_MBOX_SRAM	4014 0248h
MPU_R5SS0_CORE0_AXIS	400A 0248h
MPU_R5SS0_CORE1_AXIS	400C 0248h
MPU_R5SS1_CORE0_AXIS	400E 0248h
MPU_R5SS1_CORE1_AXIS	4010 0248h

Figure 5-1020. MPU_8_PROGRAMMABLE_5_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2088. MPU_8_PROGRAMMABLE_5_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.

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Table 5-2088. MPU_8_PROGRAMMABLE_5_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.16.2.21 MPU_8_PROGRAMMABLE_6_START_ADDRESS Register

5.16.2.21.1 MPU_8_PROGRAMMABLE_6_START_ADDRESS Register (Offset = 250h) [reset = 0h]

Programmable_6_Start_Address.

Return to Summary Table

Table 5-2089. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0250h
MPU_FSS_DATA	4016 0250h
MPU_HSM	4024 0250h
MPU_L2OCRAM_BANK0	4002 0250h
MPU_L2OCRAM_BANK1	4004 0250h
MPU_L2OCRAM_BANK2	4006 0250h
MPU_L2OCRAM_BANK3	4008 0250h
MPU_L2OCRAM_BANK4	402C 0250h
MPU_L2OCRAM_BANK5	402E 0250h
MPU_MBOX_SRAM	4014 0250h
MPU_R5SS0_CORE0_AXIS	400A 0250h
MPU_R5SS0_CORE1_AXIS	400C 0250h
MPU_R5SS1_CORE0_AXIS	400E 0250h
MPU_R5SS1_CORE1_AXIS	4010 0250h

Figure 5-1021. MPU_8_PROGRAMMABLE_6_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2090. MPU_8_PROGRAMMABLE_6_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.16.2.22 MPU_8_PROGRAMMABLE_6_END_ADDRESS Register

5.16.2.22.1 MPU_8_PROGRAMMABLE_6_END_ADDRESS Register (Offset = 254h) [reset = 0h]

Programmable_6_End_Address.

Return to Summary Table

Table 5-2091. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0254h
MPU_FSS_DATA	4016 0254h
MPU_HSM	4024 0254h
MPU_L2OCRAM_BANK0	4002 0254h
MPU_L2OCRAM_BANK1	4004 0254h
MPU_L2OCRAM_BANK2	4006 0254h
MPU_L2OCRAM_BANK3	4008 0254h
MPU_L2OCRAM_BANK4	402C 0254h
MPU_L2OCRAM_BANK5	402E 0254h
MPU_MBOX_SRAM	4014 0254h
MPU_R5SS0_CORE0_AXIS	400A 0254h
MPU_R5SS0_CORE1_AXIS	400C 0254h
MPU_R5SS1_CORE0_AXIS	400E 0254h
MPU_R5SS1_CORE1_AXIS	4010 0254h

Figure 5-1022. MPU_8_PROGRAMMABLE_6_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2092. MPU_8_PROGRAMMABLE_6_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.16.2.23 MPU_8_PROGRAMMABLE_6_MPPA Register

5.16.2.23.1 MPU_8_PROGRAMMABLE_6_MPPA Register (Offset = 258h) [reset = 0h]

Programmable_6_MPPA.

Return to Summary Table

Table 5-2093. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0258h
MPU_FSS_DATA	4016 0258h
MPU_HSM	4024 0258h
MPU_L2OCRAM_BANK0	4002 0258h
MPU_L2OCRAM_BANK1	4004 0258h
MPU_L2OCRAM_BANK2	4006 0258h
MPU_L2OCRAM_BANK3	4008 0258h
MPU_L2OCRAM_BANK4	402C 0258h
MPU_L2OCRAM_BANK5	402E 0258h
MPU_MBOX_SRAM	4014 0258h
MPU_R5SS0_CORE0_AXIS	400A 0258h
MPU_R5SS0_CORE1_AXIS	400C 0258h
MPU_R5SS1_CORE0_AXIS	400E 0258h
MPU_R5SS1_CORE1_AXIS	4010 0258h

Figure 5-1023. MPU_8_PROGRAMMABLE_6_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2094. MPU_8_PROGRAMMABLE_6_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.

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Table 5-2094. MPU_8_PROGRAMMABLE_6_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.16.2.24 MPU_8_PROGRAMMABLE_7_START_ADDRESS Register

5.16.2.24.1 MPU_8_PROGRAMMABLE_7_START_ADDRESS Register (Offset = 260h) [reset = 0h]

Programmable_7_Start_Address.

Return to Summary Table

Table 5-2095. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0260h
MPU_FSS_DATA	4016 0260h
MPU_HSM	4024 0260h
MPU_L2OCRAM_BANK0	4002 0260h
MPU_L2OCRAM_BANK1	4004 0260h
MPU_L2OCRAM_BANK2	4006 0260h
MPU_L2OCRAM_BANK3	4008 0260h
MPU_L2OCRAM_BANK4	402C 0260h
MPU_L2OCRAM_BANK5	402E 0260h
MPU_MBOX_SRAM	4014 0260h
MPU_R5SS0_CORE0_AXIS	400A 0260h
MPU_R5SS0_CORE1_AXIS	400C 0260h
MPU_R5SS1_CORE0_AXIS	400E 0260h
MPU_R5SS1_CORE1_AXIS	4010 0260h

Figure 5-1024. MPU_8_PROGRAMMABLE_7_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2096. MPU_8_PROGRAMMABLE_7_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.16.2.25 MPU_8_PROGRAMMABLE_7_END_ADDRESS Register

5.16.2.25.1 MPU_8_PROGRAMMABLE_7_END_ADDRESS Register (Offset = 264h) [reset = 0h]

Programmable_7_End_Address.

Return to Summary Table

Table 5-2097. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0264h
MPU_FSS_DATA	4016 0264h
MPU_HSM	4024 0264h
MPU_L2OCRAM_BANK0	4002 0264h
MPU_L2OCRAM_BANK1	4004 0264h
MPU_L2OCRAM_BANK2	4006 0264h
MPU_L2OCRAM_BANK3	4008 0264h
MPU_L2OCRAM_BANK4	402C 0264h
MPU_L2OCRAM_BANK5	402E 0264h
MPU_MBOX_SRAM	4014 0264h
MPU_R5SS0_CORE0_AXIS	400A 0264h
MPU_R5SS0_CORE1_AXIS	400C 0264h
MPU_R5SS1_CORE0_AXIS	400E 0264h
MPU_R5SS1_CORE1_AXIS	4010 0264h

Figure 5-1025. MPU_8_PROGRAMMABLE_7_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2098. MPU_8_PROGRAMMABLE_7_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.16.2.26 MPU_8_PROGRAMMABLE_7_MPPA Register

5.16.2.26.1 MPU_8_PROGRAMMABLE_7_MPPA Register (Offset = 268h) [reset = 0h]

Programmable_7_MPPA.

Return to Summary Table

Table 5-2099. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0268h
MPU_FSS_DATA	4016 0268h
MPU_HSM	4024 0268h
MPU_L2OCRAM_BANK0	4002 0268h
MPU_L2OCRAM_BANK1	4004 0268h
MPU_L2OCRAM_BANK2	4006 0268h
MPU_L2OCRAM_BANK3	4008 0268h
MPU_L2OCRAM_BANK4	402C 0268h
MPU_L2OCRAM_BANK5	402E 0268h
MPU_MBOX_SRAM	4014 0268h
MPU_R5SS0_CORE0_AXIS	400A 0268h
MPU_R5SS0_CORE1_AXIS	400C 0268h
MPU_R5SS1_CORE0_AXIS	400E 0268h
MPU_R5SS1_CORE1_AXIS	4010 0268h

Figure 5-1026. MPU_8_PROGRAMMABLE_7_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2100. MPU_8_PROGRAMMABLE_7_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.

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Table 5-2100. MPU_8_PROGRAMMABLE_7_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.16.2.27 MPU_8_PROGRAMMABLE_8_START_ADDRESS Register

5.16.2.27.1 MPU_8_PROGRAMMABLE_8_START_ADDRESS Register (Offset = 270h) [reset = 0h]

Programmable_8_Start_Address.

Return to Summary Table

Table 5-2101. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0270h
MPU_FSS_DATA	4016 0270h
MPU_HSM	4024 0270h
MPU_L2OCRAM_BANK0	4002 0270h
MPU_L2OCRAM_BANK1	4004 0270h
MPU_L2OCRAM_BANK2	4006 0270h
MPU_L2OCRAM_BANK3	4008 0270h
MPU_L2OCRAM_BANK4	402C 0270h
MPU_L2OCRAM_BANK5	402E 0270h
MPU_MBOX_SRAM	4014 0270h
MPU_R5SS0_CORE0_AXIS	400A 0270h
MPU_R5SS0_CORE1_AXIS	400C 0270h
MPU_R5SS1_CORE0_AXIS	400E 0270h
MPU_R5SS1_CORE1_AXIS	4010 0270h

Figure 5-1027. MPU_8_PROGRAMMABLE_8_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2102. MPU_8_PROGRAMMABLE_8_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.16.2.28 MPU_8_PROGRAMMABLE_8_END_ADDRESS Register

5.16.2.28.1 MPU_8_PROGRAMMABLE_8_END_ADDRESS Register (Offset = 274h) [reset = 0h]

Programmable_8_End_Address.

Return to Summary Table

Table 5-2103. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0274h
MPU_FSS_DATA	4016 0274h
MPU_HSM	4024 0274h
MPU_L2OCRAM_BANK0	4002 0274h
MPU_L2OCRAM_BANK1	4004 0274h
MPU_L2OCRAM_BANK2	4006 0274h
MPU_L2OCRAM_BANK3	4008 0274h
MPU_L2OCRAM_BANK4	402C 0274h
MPU_L2OCRAM_BANK5	402E 0274h
MPU_MBOX_SRAM	4014 0274h
MPU_R5SS0_CORE0_AXIS	400A 0274h
MPU_R5SS0_CORE1_AXIS	400C 0274h
MPU_R5SS1_CORE0_AXIS	400E 0274h
MPU_R5SS1_CORE1_AXIS	4010 0274h

Figure 5-1028. MPU_8_PROGRAMMABLE_8_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDR							
R/W							
0h							

Table 5-2104. MPU_8_PROGRAMMABLE_8_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.16.2.29 MPU_8_PROGRAMMABLE_8_MPPA Register

5.16.2.29.1 MPU_8_PROGRAMMABLE_8_MPPA Register (Offset = 278h) [reset = 0h]

Programmable_8_MPPA.

Return to Summary Table

Table 5-2105. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0278h
MPU_FSS_DATA	4016 0278h
MPU_HSM	4024 0278h
MPU_L2OCRAM_BANK0	4002 0278h
MPU_L2OCRAM_BANK1	4004 0278h
MPU_L2OCRAM_BANK2	4006 0278h
MPU_L2OCRAM_BANK3	4008 0278h
MPU_L2OCRAM_BANK4	402C 0278h
MPU_L2OCRAM_BANK5	402E 0278h
MPU_MBOX_SRAM	4014 0278h
MPU_R5SS0_CORE0_AXIS	400A 0278h
MPU_R5SS0_CORE1_AXIS	400C 0278h
MPU_R5SS1_CORE0_AXIS	400E 0278h
MPU_R5SS1_CORE1_AXIS	4010 0278h

Figure 5-1029. MPU_8_PROGRAMMABLE_8_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2106. MPU_8_PROGRAMMABLE_8_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.

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Table 5-2106. MPU_8_PROGRAMMABLE_8_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.16.2.30 MPU_8_FAULT_ADDRESS Register

5.16.2.30.1 MPU_8_FAULT_ADDRESS Register (Offset = 300h) [reset = 0h]

Fault_Address.

Return to Summary Table

Table 5-2107. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0300h
MPU_FSS_DATA	4016 0300h
MPU_HSM	4024 0300h
MPU_L2OCRAM_BANK0	4002 0300h
MPU_L2OCRAM_BANK1	4004 0300h
MPU_L2OCRAM_BANK2	4006 0300h
MPU_L2OCRAM_BANK3	4008 0300h
MPU_L2OCRAM_BANK4	402C 0300h
MPU_L2OCRAM_BANK5	402E 0300h
MPU_MBOX_SRAM	4014 0300h
MPU_R5SS0_CORE0_AXIS	400A 0300h
MPU_R5SS0_CORE1_AXIS	400C 0300h
MPU_R5SS1_CORE0_AXIS	400E 0300h
MPU_R5SS1_CORE1_AXIS	4010 0300h

Figure 5-1030. MPU_8_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 5-2108. MPU_8_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault_address.

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5.16.2.31 MPU_8_FAULT_STATUS Register

5.16.2.31.1 MPU_8_FAULT_STATUS Register (Offset = 304h) [reset = 0h]

Fault_Status.

Return to Summary Table

Table 5-2109. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0304h
MPU_FSS_DATA	4016 0304h
MPU_HSM	4024 0304h
MPU_L2OCRAM_BANK0	4002 0304h
MPU_L2OCRAM_BANK1	4004 0304h
MPU_L2OCRAM_BANK2	4006 0304h
MPU_L2OCRAM_BANK3	4008 0304h
MPU_L2OCRAM_BANK4	402C 0304h
MPU_L2OCRAM_BANK5	402E 0304h
MPU_MBOX_SRAM	4014 0304h
MPU_R5SS0_CORE0_AXIS	400A 0304h
MPU_R5SS0_CORE1_AXIS	400C 0304h
MPU_R5SS1_CORE0_AXIS	400E 0304h
MPU_R5SS1_CORE1_AXIS	4010 0304h

Figure 5-1031. MPU_8_FAULT_STATUS Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	22	21	20	19	18	17	16
MSTID							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED			PRIVID				RESERVED1
R			R				R
0h			0h				0h
7	6	5	4	3	2	1	0
NS	RESERVED2	FAULT_TYPE					
R	R	R					
0h	0h	0h					

Table 5-2110. MPU_8_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ID	R	0h	Transfer ID
23:16	MSTID	R	0h	Master ID.
15:13	RESERVED	R	0h	Always read as 0.
12:9	PRIVID	R	0h	Privilege ID.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R	0h	Non-secure access.
6	RESERVED2	R	0h	Always read as 0.

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Table 5-2110. MPU_8_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	FAULT_TYPE	R	0h	Fault_type. 100000 = supervisor read fault 010000 = supervisor write fault 001000 = supervisor execute fault 000100 = user read fault 000010 = user write fault 000001 = user execute fault 111111 = relaxed cache linefill fault 010010 = relaxed cache writeback fault 000000 = no fault

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5.16.2.32 MPU_8_FAULT_CLEAR Register

5.16.2.32.1 MPU_8_FAULT_CLEAR Register (Offset = 308h) [reset = 0h]

Fault_Clear.

Return to Summary Table

Table 5-2111. Instance Table

Instance Name	Physical Address
MPU_DTHE	4012 0308h
MPU_FSS_DATA	4016 0308h
MPU_HSM	4024 0308h
MPU_L2OCRAM_BANK0	4002 0308h
MPU_L2OCRAM_BANK1	4004 0308h
MPU_L2OCRAM_BANK2	4006 0308h
MPU_L2OCRAM_BANK3	4008 0308h
MPU_L2OCRAM_BANK4	402C 0308h
MPU_L2OCRAM_BANK5	402E 0308h
MPU_MBOX_SRAM	4014 0308h
MPU_R5SS0_CORE0_AXIS	400A 0308h
MPU_R5SS0_CORE1_AXIS	400C 0308h
MPU_R5SS1_CORE0_AXIS	400E 0308h
MPU_R5SS1_CORE1_AXIS	4010 0308h

Figure 5-1032. MPU_8_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							FAULT_CLR
R							W
0h							0h

Table 5-2112. MPU_8_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Always read as 0.
0	FAULT_CLR	W	0h	Fault_clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

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5.17 MPU_16

MPU_16

5.17.1 MPU_16 Summaries

MPU_16 Summaries

Table 5-2113. MPU_16 Registers, Base Address=401C 0000h, Length=1024

Offset	Length	Register Name	MPU_R5SS0_CORE0_AHB Physical Address	MPU_R5SS0_CORE1_AHB Physical Address	MPU_R5SS1_CORE0_AHB Physical Address
0h	32	MPU_16_REVISION	401C 0000h	401E 0000h	4020 0000h
10h	32	MPU_16_INTERRUPT_RAW_STATUS_SET	401C 0010h	401E 0010h	4020 0010h
14h	32	MPU_16_INTERRUPT_ENABLED_STATUS_CLEAR	401C 0014h	401E 0014h	4020 0014h
18h	32	MPU_16_INTERRUPT_ENABLE	401C 0018h	401E 0018h	4020 0018h
1Ch	32	MPU_16_INTERRUPT_ENABLE_CLEAR	401C 001Ch	401E 001Ch	4020 001Ch
200h	32	MPU_16_PROGRAMMABLE_1_START_ADDRESS	401C 0200h	401E 0200h	4020 0200h
204h	32	MPU_16_PROGRAMMABLE_1_END_ADDRESS	401C 0204h	401E 0204h	4020 0204h
208h	32	MPU_16_PROGRAMMABLE_1_MPPA	401C 0208h	401E 0208h	4020 0208h
210h	32	MPU_16_PROGRAMMABLE_2_START_ADDRESS	401C 0210h	401E 0210h	4020 0210h
214h	32	MPU_16_PROGRAMMABLE_2_END_ADDRESS	401C 0214h	401E 0214h	4020 0214h
218h	32	MPU_16_PROGRAMMABLE_2_MPPA	401C 0218h	401E 0218h	4020 0218h
220h	32	MPU_16_PROGRAMMABLE_3_START_ADDRESS	401C 0220h	401E 0220h	4020 0220h
224h	32	MPU_16_PROGRAMMABLE_3_END_ADDRESS	401C 0224h	401E 0224h	4020 0224h
228h	32	MPU_16_PROGRAMMABLE_3_MPPA	401C 0228h	401E 0228h	4020 0228h
230h	32	MPU_16_PROGRAMMABLE_4_START_ADDRESS	401C 0230h	401E 0230h	4020 0230h
234h	32	MPU_16_PROGRAMMABLE_4_END_ADDRESS	401C 0234h	401E 0234h	4020 0234h
238h	32	MPU_16_PROGRAMMABLE_4_MPPA	401C 0238h	401E 0238h	4020 0238h
240h	32	MPU_16_PROGRAMMABLE_5_START_ADDRESS	401C 0240h	401E 0240h	4020 0240h
244h	32	MPU_16_PROGRAMMABLE_5_END_ADDRESS	401C 0244h	401E 0244h	4020 0244h
248h	32	MPU_16_PROGRAMMABLE_5_MPPA	401C 0248h	401E 0248h	4020 0248h
250h	32	MPU_16_PROGRAMMABLE_6_START_ADDRESS	401C 0250h	401E 0250h	4020 0250h
254h	32	MPU_16_PROGRAMMABLE_6_END_ADDRESS	401C 0254h	401E 0254h	4020 0254h
258h	32	MPU_16_PROGRAMMABLE_6_MPPA	401C 0258h	401E 0258h	4020 0258h
260h	32	MPU_16_PROGRAMMABLE_7_START_ADDRESS	401C 0260h	401E 0260h	4020 0260h

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Table 5-2113. MPU_16 Registers, Base Address=401C 0000h, Length=1024 (continued)

Offset	Length	Register Name	MPU_R5SS0_CORE0_AHB Physical Address	MPU_R5SS0_CORE1_AHB Physical Address	MPU_R5SS1_CORE0_AHB Physical Address
264h	32	MPU_16_PROGRAMMABLE_7_END_ADDRESS	401C 0264h	401E 0264h	4020 0264h
268h	32	MPU_16_PROGRAMMABLE_7_MPPA	401C 0268h	401E 0268h	4020 0268h
270h	32	MPU_16_PROGRAMMABLE_8_START_ADDRESS	401C 0270h	401E 0270h	4020 0270h
274h	32	MPU_16_PROGRAMMABLE_8_END_ADDRESS	401C 0274h	401E 0274h	4020 0274h
278h	32	MPU_16_PROGRAMMABLE_8_MPPA	401C 0278h	401E 0278h	4020 0278h
280h	32	MPU_16_PROGRAMMABLE_9_START_ADDRESS	401C 0280h	401E 0280h	4020 0280h
284h	32	MPU_16_PROGRAMMABLE_9_END_ADDRESS	401C 0284h	401E 0284h	4020 0284h
288h	32	MPU_16_PROGRAMMABLE_9_MPPA	401C 0288h	401E 0288h	4020 0288h
290h	32	MPU_16_PROGRAMMABLE_10_START_ADDRESS	401C 0290h	401E 0290h	4020 0290h
294h	32	MPU_16_PROGRAMMABLE_10_END_ADDRESS	401C 0294h	401E 0294h	4020 0294h
298h	32	MPU_16_PROGRAMMABLE_10_MPPA	401C 0298h	401E 0298h	4020 0298h
2A0h	32	MPU_16_PROGRAMMABLE_11_START_ADDRESS	401C 02A0h	401E 02A0h	4020 02A0h
2A4h	32	MPU_16_PROGRAMMABLE_11_END_ADDRESS	401C 02A4h	401E 02A4h	4020 02A4h
2A8h	32	MPU_16_PROGRAMMABLE_11_MPPA	401C 02A8h	401E 02A8h	4020 02A8h
2B0h	32	MPU_16_PROGRAMMABLE_12_START_ADDRESS	401C 02B0h	401E 02B0h	4020 02B0h
2B4h	32	MPU_16_PROGRAMMABLE_12_END_ADDRESS	401C 02B4h	401E 02B4h	4020 02B4h
2B8h	32	MPU_16_PROGRAMMABLE_12_MPPA	401C 02B8h	401E 02B8h	4020 02B8h
2C0h	32	MPU_16_PROGRAMMABLE_13_START_ADDRESS	401C 02C0h	401E 02C0h	4020 02C0h
2C4h	32	MPU_16_PROGRAMMABLE_13_END_ADDRESS	401C 02C4h	401E 02C4h	4020 02C4h
2C8h	32	MPU_16_PROGRAMMABLE_13_MPPA	401C 02C8h	401E 02C8h	4020 02C8h
2D0h	32	MPU_16_PROGRAMMABLE_14_START_ADDRESS	401C 02D0h	401E 02D0h	4020 02D0h
2D4h	32	MPU_16_PROGRAMMABLE_14_END_ADDRESS	401C 02D4h	401E 02D4h	4020 02D4h
2D8h	32	MPU_16_PROGRAMMABLE_14_MPPA	401C 02D8h	401E 02D8h	4020 02D8h
2E0h	32	MPU_16_PROGRAMMABLE_15_START_ADDRESS	401C 02E0h	401E 02E0h	4020 02E0h
2E4h	32	MPU_16_PROGRAMMABLE_15_END_ADDRESS	401C 02E4h	401E 02E4h	4020 02E4h
2E8h	32	MPU_16_PROGRAMMABLE_15_MPPA	401C 02E8h	401E 02E8h	4020 02E8h
2F0h	32	MPU_16_PROGRAMMABLE_16_START_ADDRESS	401C 02F0h	401E 02F0h	4020 02F0h

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Table 5-2113. MPU_16 Registers, Base Address=401C 0000h, Length=1024 (continued)

Offset	Length	Register Name	MPU_R5SS0_CORE0_AHB Physical Address	MPU_R5SS0_CORE1_AHB Physical Address	MPU_R5SS1_CORE0_AHB Physical Address
2F4h	32	MPU_16_PROGRAMMABLE_16_END_ADDRESS	401C 02F4h	401E 02F4h	4020 02F4h
2F8h	32	MPU_16_PROGRAMMABLE_16_MPPA	401C 02F8h	401E 02F8h	4020 02F8h
300h	32	MPU_16_FAULT_ADDRESS	401C 0300h	401E 0300h	4020 0300h
304h	32	MPU_16_FAULT_STATUS	401C 0304h	401E 0304h	4020 0304h
308h	32	MPU_16_FAULT_CLEAR	401C 0308h	401E 0308h	4020 0308h

Table 5-2114. MPU_16 Registers, Base Address=401C 0000h, Length=1024

Offset	Length	Register Name	MPU_R5SS1_CORE1_AHB Physical Address	MPU_SCRM2SCRP0 Physical Address	MPU_SCRM2SCRP1 Physical Address
0h	32	MPU_16_REVISION	4022 0000h	4018 0000h	401A 0000h
10h	32	MPU_16_INTERRUPT_RAW_STATUS_SET	4022 0010h	4018 0010h	401A 0010h
14h	32	MPU_16_INTERRUPT_ENABLED_STATUS_CLEAR	4022 0014h	4018 0014h	401A 0014h
18h	32	MPU_16_INTERRUPT_ENABLE	4022 0018h	4018 0018h	401A 0018h
1Ch	32	MPU_16_INTERRUPT_ENABLE_CLEAR	4022 001Ch	4018 001Ch	401A 001Ch
200h	32	MPU_16_PROGRAMMABLE_1_START_ADDRESS	4022 0200h	4018 0200h	401A 0200h
204h	32	MPU_16_PROGRAMMABLE_1_END_ADDRESS	4022 0204h	4018 0204h	401A 0204h
208h	32	MPU_16_PROGRAMMABLE_1_MPPA	4022 0208h	4018 0208h	401A 0208h
210h	32	MPU_16_PROGRAMMABLE_2_START_ADDRESS	4022 0210h	4018 0210h	401A 0210h
214h	32	MPU_16_PROGRAMMABLE_2_END_ADDRESS	4022 0214h	4018 0214h	401A 0214h
218h	32	MPU_16_PROGRAMMABLE_2_MPPA	4022 0218h	4018 0218h	401A 0218h
220h	32	MPU_16_PROGRAMMABLE_3_START_ADDRESS	4022 0220h	4018 0220h	401A 0220h
224h	32	MPU_16_PROGRAMMABLE_3_END_ADDRESS	4022 0224h	4018 0224h	401A 0224h
228h	32	MPU_16_PROGRAMMABLE_3_MPPA	4022 0228h	4018 0228h	401A 0228h
230h	32	MPU_16_PROGRAMMABLE_4_START_ADDRESS	4022 0230h	4018 0230h	401A 0230h
234h	32	MPU_16_PROGRAMMABLE_4_END_ADDRESS	4022 0234h	4018 0234h	401A 0234h
238h	32	MPU_16_PROGRAMMABLE_4_MPPA	4022 0238h	4018 0238h	401A 0238h
240h	32	MPU_16_PROGRAMMABLE_5_START_ADDRESS	4022 0240h	4018 0240h	401A 0240h
244h	32	MPU_16_PROGRAMMABLE_5_END_ADDRESS	4022 0244h	4018 0244h	401A 0244h
248h	32	MPU_16_PROGRAMMABLE_5_MPPA	4022 0248h	4018 0248h	401A 0248h
250h	32	MPU_16_PROGRAMMABLE_6_START_ADDRESS	4022 0250h	4018 0250h	401A 0250h
254h	32	MPU_16_PROGRAMMABLE_6_END_ADDRESS	4022 0254h	4018 0254h	401A 0254h

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Table 5-2114. MPU_16 Registers, Base Address=401C 0000h, Length=1024 (continued)

Offset	Length	Register Name	MPU_R5SS1_CORE1_AHB Physical Address	MPU_SCRM2SCRP0 Physical Address	MPU_SCRM2SCRP1 Physical Address
258h	32	MPU_16_PROGRAMMABLE_6_MPPA	4022 0258h	4018 0258h	401A 0258h
260h	32	MPU_16_PROGRAMMABLE_7_START_ADDRESS	4022 0260h	4018 0260h	401A 0260h
264h	32	MPU_16_PROGRAMMABLE_7_END_ADDRESS	4022 0264h	4018 0264h	401A 0264h
268h	32	MPU_16_PROGRAMMABLE_7_MPPA	4022 0268h	4018 0268h	401A 0268h
270h	32	MPU_16_PROGRAMMABLE_8_START_ADDRESS	4022 0270h	4018 0270h	401A 0270h
274h	32	MPU_16_PROGRAMMABLE_8_END_ADDRESS	4022 0274h	4018 0274h	401A 0274h
278h	32	MPU_16_PROGRAMMABLE_8_MPPA	4022 0278h	4018 0278h	401A 0278h
280h	32	MPU_16_PROGRAMMABLE_9_START_ADDRESS	4022 0280h	4018 0280h	401A 0280h
284h	32	MPU_16_PROGRAMMABLE_9_END_ADDRESS	4022 0284h	4018 0284h	401A 0284h
288h	32	MPU_16_PROGRAMMABLE_9_MPPA	4022 0288h	4018 0288h	401A 0288h
290h	32	MPU_16_PROGRAMMABLE_10_START_ADDRESS	4022 0290h	4018 0290h	401A 0290h
294h	32	MPU_16_PROGRAMMABLE_10_END_ADDRESS	4022 0294h	4018 0294h	401A 0294h
298h	32	MPU_16_PROGRAMMABLE_10_MPPA	4022 0298h	4018 0298h	401A 0298h
2A0h	32	MPU_16_PROGRAMMABLE_11_START_ADDRESS	4022 02A0h	4018 02A0h	401A 02A0h
2A4h	32	MPU_16_PROGRAMMABLE_11_END_ADDRESS	4022 02A4h	4018 02A4h	401A 02A4h
2A8h	32	MPU_16_PROGRAMMABLE_11_MPPA	4022 02A8h	4018 02A8h	401A 02A8h
2B0h	32	MPU_16_PROGRAMMABLE_12_START_ADDRESS	4022 02B0h	4018 02B0h	401A 02B0h
2B4h	32	MPU_16_PROGRAMMABLE_12_END_ADDRESS	4022 02B4h	4018 02B4h	401A 02B4h
2B8h	32	MPU_16_PROGRAMMABLE_12_MPPA	4022 02B8h	4018 02B8h	401A 02B8h
2C0h	32	MPU_16_PROGRAMMABLE_13_START_ADDRESS	4022 02C0h	4018 02C0h	401A 02C0h
2C4h	32	MPU_16_PROGRAMMABLE_13_END_ADDRESS	4022 02C4h	4018 02C4h	401A 02C4h
2C8h	32	MPU_16_PROGRAMMABLE_13_MPPA	4022 02C8h	4018 02C8h	401A 02C8h
2D0h	32	MPU_16_PROGRAMMABLE_14_START_ADDRESS	4022 02D0h	4018 02D0h	401A 02D0h
2D4h	32	MPU_16_PROGRAMMABLE_14_END_ADDRESS	4022 02D4h	4018 02D4h	401A 02D4h
2D8h	32	MPU_16_PROGRAMMABLE_14_MPPA	4022 02D8h	4018 02D8h	401A 02D8h
2E0h	32	MPU_16_PROGRAMMABLE_15_START_ADDRESS	4022 02E0h	4018 02E0h	401A 02E0h
2E4h	32	MPU_16_PROGRAMMABLE_15_END_ADDRESS	4022 02E4h	4018 02E4h	401A 02E4h

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Table 5-2114. MPU_16 Registers, Base Address=401C 0000h, Length=1024 (continued)

Offset	Length	Register Name	MPU_R5SS1_CORE1_AHB Physical Address	MPU_SCRM2SCRP0 Physical Address	MPU_SCRM2SCRP1 Physical Address
2E8h	32	MPU_16_PROGRAMMABLE_15_MPPA	4022 02E8h	4018 02E8h	401A 02E8h
2F0h	32	MPU_16_PROGRAMMABLE_16_START_ADDRESS	4022 02F0h	4018 02F0h	401A 02F0h
2F4h	32	MPU_16_PROGRAMMABLE_16_END_ADDRESS	4022 02F4h	4018 02F4h	401A 02F4h
2F8h	32	MPU_16_PROGRAMMABLE_16_MPPA	4022 02F8h	4018 02F8h	401A 02F8h
300h	32	MPU_16_FAULT_ADDRESS	4022 0300h	4018 0300h	401A 0300h
304h	32	MPU_16_FAULT_STATUS	4022 0304h	4018 0304h	401A 0304h
308h	32	MPU_16_FAULT_CLEAR	4022 0308h	4018 0308h	401A 0308h

5.17.2 MPU_16 Registers

MPU_16 Registers

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5.17.2.1 MPU_16_REVISION Register

5.17.2.1.1 MPU_16_REVISION Register (Offset = 0h) [reset = 4E815101h]

Revision.

Return to Summary Table

Table 5-2115. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0000h
MPU_R5SS0_CORE1_AHB	401E 0000h
MPU_R5SS1_CORE0_AHB	4020 0000h
MPU_R5SS1_CORE1_AHB	4022 0000h
MPU_SCRM2SCRP0	4018 0000h
MPU_SCRM2SCRP1	401A 0000h

Figure 5-1033. MPU_16_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		MODID			
R		R		R			
1h		0h		E81h			
23	22	21	20	19	18	17	16
MODID							
R							
E81h							
15	14	13	12	11	10	9	8
REVRTL					REVMAJ		
R					R		
Ah					1h		
7	6	5	4	3	2	1	0
REVCUSTOM		REVMIN					
R		R					
0h		1h					

Table 5-2116. MPU_16_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme.
29:28	RESERVED	R	0h	Always read a s0. Writes have no affect.
27:16	MODID	R	E81h	Module ID field.
15:11	REVRTL	R	Ah	RTL revision.Will vary depending on release.
10:8	REVMAJ	R	1h	Major revision.
7:6	REVCUSTOM	R	0h	Custom revision.
5:0	REVMIN	R	1h	Minor revision.

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5.17.2.2 MPU_16_INTERRUPT_RAW_STATUS_SET Register

5.17.2.2.1 MPU_16_INTERRUPT_RAW_STATUS_SET Register (Offset = 10h) [reset = 0h]

Interrupt_Raw_Status_Set.

Return to Summary Table

Table 5-2117. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0010h
MPU_R5SS0_CORE1_AHB	401E 0010h
MPU_R5SS1_CORE0_AHB	4020 0010h
MPU_R5SS1_CORE1_AHB	4022 0010h
MPU_SCRM2SCRP0	4018 0010h
MPU_SCRM2SCRP1	401A 0010h

Figure 5-1034. MPU_16_INTERRUPT_RAW_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						ADDR_ERR	PROT_ERR
R						R/W1TS	R/W1TS
0h						0h	0h

Table 5-2118. MPU_16_INTERRUPT_RAW_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ADDR_ERR	R/W1TS	0h	Addressing violation error. Raw status is read.Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	R/W1TS	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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5.17.2.3 MPU_16_INTERRUPT_ENABLED_STATUS_CLEAR Register

5.17.2.3.1 MPU_16_INTERRUPT_ENABLED_STATUS_CLEAR Register (Offset = 14h) [reset = 0h]

Interrupt_Enabled_Status_Clear.

Return to Summary Table

Table 5-2119. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0014h
MPU_R5SS0_CORE1_AHB	401E 0014h
MPU_R5SS1_CORE0_AHB	4020 0014h
MPU_R5SS1_CORE1_AHB	4022 0014h
MPU_SCRM2SCRP0	4018 0014h
MPU_SCRM2SCRP1	401A 0014h

Figure 5-1035. MPU_16_INTERRUPT_ENABLED_STATUS_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						ENABLED_ADDR_ERR	ENABLED_PROT_ERR
R						R/W0TC	R/W0TC
0h						0h	0h

Table 5-2120. MPU_16_INTERRUPT_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ENABLED_ADDR_ERR	R/W0TC	0h	Addressing violation error. Enabled status is read.Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	R/W0TC	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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5.17.2.4 MPU_16_INTERRUPT_ENABLE Register

5.17.2.4.1 MPU_16_INTERRUPT_ENABLE Register (Offset = 18h) [reset = 0h]

Interrupt_Enable.

Return to Summary Table

Table 5-2121. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0018h
MPU_R5SS0_CORE1_AHB	401E 0018h
MPU_R5SS1_CORE0_AHB	4020 0018h
MPU_R5SS1_CORE1_AHB	4022 0018h
MPU_SCRM2SCRP0	4018 0018h
MPU_SCRM2SCRP1	401A 0018h

Figure 5-1036. MPU_16_INTERRUPT_ENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						ADDR_ERR_EN	PROT_ERR_EN
R						R/W1TS	R/W1TS
0h						0h	0h

Table 5-2122. MPU_16_INTERRUPT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ADDR_ERR_EN	R/W1TS	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	R/W1TS	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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5.17.2.5 MPU_16_INTERRUPT_ENABLE_CLEAR Register

5.17.2.5.1 MPU_16_INTERRUPT_ENABLE_CLEAR Register (Offset = 1Ch) [reset = 0h]

Interrupt_Enable_Clear.

Return to Summary Table

Table 5-2123. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 001Ch
MPU_R5SS0_CORE1_AHB	401E 001Ch
MPU_R5SS1_CORE0_AHB	4020 001Ch
MPU_R5SS1_CORE1_AHB	4022 001Ch
MPU_SCRM2SCRP0	4018 001Ch
MPU_SCRM2SCRP1	401A 001Ch

Figure 5-1037. MPU_16_INTERRUPT_ENABLE_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
R						R/W0TC	R/W0TC
0h						0h	0h

Table 5-2124. MPU_16_INTERRUPT_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	R	0h	Always read as 0.
1	ADDR_ERR_EN_CLR	R/W0TC	0h	Addressing violation error enable. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	R/W0TC	0h	Protection violation error enable. Write a 1 to clear the enable. Writing a 0 has no effect.

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5.17.2.6 MPU_16_PROGRAMMABLE_1_START_ADDRESS Register

5.17.2.6.1 MPU_16_PROGRAMMABLE_1_START_ADDRESS Register (Offset = 200h) [reset = 0h]

Programmable_1_Start_Address.

Return to Summary Table

Table 5-2125. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0200h
MPU_R5SS0_CORE1_AHB	401E 0200h
MPU_R5SS1_CORE0_AHB	4020 0200h
MPU_R5SS1_CORE1_AHB	4022 0200h
MPU_SCRM2SCRP0	4018 0200h
MPU_SCRM2SCRP1	401A 0200h

Figure 5-1038. MPU_16_PROGRAMMABLE_1_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2126. MPU_16_PROGRAMMABLE_1_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.7 MPU_16_PROGRAMMABLE_1_END_ADDRESS Register

5.17.2.7.1 MPU_16_PROGRAMMABLE_1_END_ADDRESS Register (Offset = 204h) [reset = 0h]

Programmable_1_End_Address.

Return to Summary Table

Table 5-2127. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0204h
MPU_R5SS0_CORE1_AHB	401E 0204h
MPU_R5SS1_CORE0_AHB	4020 0204h
MPU_R5SS1_CORE1_AHB	4022 0204h
MPU_SCRM2SCRP0	4018 0204h
MPU_SCRM2SCRP1	401A 0204h

Figure 5-1039. MPU_16_PROGRAMMABLE_1_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2128. MPU_16_PROGRAMMABLE_1_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.8 MPU_16_PROGRAMMABLE_1_MPPA Register

5.17.2.8.1 MPU_16_PROGRAMMABLE_1_MPPA Register (Offset = 208h) [reset = 0h]

Programmable_1_MPPA.

Return to Summary Table

Table 5-2129. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0208h
MPU_R5SS0_CORE1_AHB	401E 0208h
MPU_R5SS1_CORE0_AHB	4020 0208h
MPU_R5SS1_CORE1_AHB	4022 0208h
MPU_SCRM2SCRP0	4018 0208h
MPU_SCRM2SCRP1	401A 0208h

Figure 5-1040. MPU_16_PROGRAMMABLE_1_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2130. MPU_16_PROGRAMMABLE_1_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2130. MPU_16_PROGRAMMABLE_1_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.9 MPU_16_PROGRAMMABLE_2_START_ADDRESS Register

5.17.2.9.1 MPU_16_PROGRAMMABLE_2_START_ADDRESS Register (Offset = 210h) [reset = 0h]

Programmable_2_Start_Address.

Return to Summary Table

Table 5-2131. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0210h
MPU_R5SS0_CORE1_AHB	401E 0210h
MPU_R5SS1_CORE0_AHB	4020 0210h
MPU_R5SS1_CORE1_AHB	4022 0210h
MPU_SCRM2SCRP0	4018 0210h
MPU_SCRM2SCRP1	401A 0210h

Figure 5-1041. MPU_16_PROGRAMMABLE_2_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2132. MPU_16_PROGRAMMABLE_2_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.10 MPU_16_PROGRAMMABLE_2_END_ADDRESS Register

5.17.2.10.1 MPU_16_PROGRAMMABLE_2_END_ADDRESS Register (Offset = 214h) [reset = 0h]

Programmable_2_End_Address.

Return to Summary Table

Table 5-2133. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0214h
MPU_R5SS0_CORE1_AHB	401E 0214h
MPU_R5SS1_CORE0_AHB	4020 0214h
MPU_R5SS1_CORE1_AHB	4022 0214h
MPU_SCRM2SCRP0	4018 0214h
MPU_SCRM2SCRP1	401A 0214h

Figure 5-1042. MPU_16_PROGRAMMABLE_2_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2134. MPU_16_PROGRAMMABLE_2_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.11 MPU_16_PROGRAMMABLE_2_MPPA Register

5.17.2.11.1 MPU_16_PROGRAMMABLE_2_MPPA Register (Offset = 218h) [reset = 0h]

Programmable_2_MPPA.

Return to Summary Table

Table 5-2135. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0218h
MPU_R5SS0_CORE1_AHB	401E 0218h
MPU_R5SS1_CORE0_AHB	4020 0218h
MPU_R5SS1_CORE1_AHB	4022 0218h
MPU_SCRM2SCRP0	4018 0218h
MPU_SCRM2SCRP1	401A 0218h

Figure 5-1043. MPU_16_PROGRAMMABLE_2_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2136. MPU_16_PROGRAMMABLE_2_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2136. MPU_16_PROGRAMMABLE_2_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.12 MPU_16_PROGRAMMABLE_3_START_ADDRESS Register

5.17.2.12.1 MPU_16_PROGRAMMABLE_3_START_ADDRESS Register (Offset = 220h) [reset = 0h]

Programmable_3_Start_Address.

Return to Summary Table

Table 5-2137. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0220h
MPU_R5SS0_CORE1_AHB	401E 0220h
MPU_R5SS1_CORE0_AHB	4020 0220h
MPU_R5SS1_CORE1_AHB	4022 0220h
MPU_SCRM2SCRP0	4018 0220h
MPU_SCRM2SCRP1	401A 0220h

Figure 5-1044. MPU_16_PROGRAMMABLE_3_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2138. MPU_16_PROGRAMMABLE_3_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.13 MPU_16_PROGRAMMABLE_3_END_ADDRESS Register

5.17.2.13.1 MPU_16_PROGRAMMABLE_3_END_ADDRESS Register (Offset = 224h) [reset = 0h]

Programmable_3_End_Address.

Return to Summary Table

Table 5-2139. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0224h
MPU_R5SS0_CORE1_AHB	401E 0224h
MPU_R5SS1_CORE0_AHB	4020 0224h
MPU_R5SS1_CORE1_AHB	4022 0224h
MPU_SCRM2SCRP0	4018 0224h
MPU_SCRM2SCRP1	401A 0224h

Figure 5-1045. MPU_16_PROGRAMMABLE_3_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDR							
R/W							
0h							

Table 5-2140. MPU_16_PROGRAMMABLE_3_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.14 MPU_16_PROGRAMMABLE_3_MPPA Register

5.17.2.14.1 MPU_16_PROGRAMMABLE_3_MPPA Register (Offset = 228h) [reset = 0h]

Programmable_3_MPPA.

Return to Summary Table

Table 5-2141. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0228h
MPU_R5SS0_CORE1_AHB	401E 0228h
MPU_R5SS1_CORE0_AHB	4020 0228h
MPU_R5SS1_CORE1_AHB	4022 0228h
MPU_SCRM2SCRP0	4018 0228h
MPU_SCRM2SCRP1	401A 0228h

Figure 5-1046. MPU_16_PROGRAMMABLE_3_MPPA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED3</td><td>LOCK</td><td colspan="2">RESERVED2</td><td colspan="2">AID15_0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="2">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">AID15_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">AID15_0</td><td>AIDX</td><td>RESERVED1</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>NS</td><td>EMU</td><td>SR</td><td>SW</td><td>SX</td><td>UR</td><td>UW</td><td>UX</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-2142. MPU_16_PROGRAMMABLE_3_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2142. MPU_16_PROGRAMMABLE_3_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.15 MPU_16_PROGRAMMABLE_4_START_ADDRESS Register

5.17.2.15.1 MPU_16_PROGRAMMABLE_4_START_ADDRESS Register (Offset = 230h) [reset = 0h]

Programmable_4_Start_Address.

Return to Summary Table

Table 5-2143. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0230h
MPU_R5SS0_CORE1_AHB	401E 0230h
MPU_R5SS1_CORE0_AHB	4020 0230h
MPU_R5SS1_CORE1_AHB	4022 0230h
MPU_SCRM2SCRP0	4018 0230h
MPU_SCRM2SCRP1	401A 0230h

Figure 5-1047. MPU_16_PROGRAMMABLE_4_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2144. MPU_16_PROGRAMMABLE_4_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.16 MPU_16_PROGRAMMABLE_4_END_ADDRESS Register

5.17.2.16.1 MPU_16_PROGRAMMABLE_4_END_ADDRESS Register (Offset = 234h) [reset = 0h]

Programmable_4_End_Address.

Return to Summary Table

Table 5-2145. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0234h
MPU_R5SS0_CORE1_AHB	401E 0234h
MPU_R5SS1_CORE0_AHB	4020 0234h
MPU_R5SS1_CORE1_AHB	4022 0234h
MPU_SCRM2SCRP0	4018 0234h
MPU_SCRM2SCRP1	401A 0234h

Figure 5-1048. MPU_16_PROGRAMMABLE_4_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2146. MPU_16_PROGRAMMABLE_4_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.17 MPU_16_PROGRAMMABLE_4_MPPA Register

5.17.2.17.1 MPU_16_PROGRAMMABLE_4_MPPA Register (Offset = 238h) [reset = 0h]

Programmable_4_MPPA.

Return to Summary Table

Table 5-2147. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0238h
MPU_R5SS0_CORE1_AHB	401E 0238h
MPU_R5SS1_CORE0_AHB	4020 0238h
MPU_R5SS1_CORE1_AHB	4022 0238h
MPU_SCRM2SCRP0	4018 0238h
MPU_SCRM2SCRP1	401A 0238h

Figure 5-1049. MPU_16_PROGRAMMABLE_4_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2148. MPU_16_PROGRAMMABLE_4_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2148. MPU_16_PROGRAMMABLE_4_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.18 MPU_16_PROGRAMMABLE_5_START_ADDRESS Register

5.17.2.18.1 MPU_16_PROGRAMMABLE_5_START_ADDRESS Register (Offset = 240h) [reset = 0h]

Programmable_5_Start_Address.

Return to Summary Table

Table 5-2149. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0240h
MPU_R5SS0_CORE1_AHB	401E 0240h
MPU_R5SS1_CORE0_AHB	4020 0240h
MPU_R5SS1_CORE1_AHB	4022 0240h
MPU_SCRM2SCRP0	4018 0240h
MPU_SCRM2SCRP1	401A 0240h

Figure 5-1050. MPU_16_PROGRAMMABLE_5_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2150. MPU_16_PROGRAMMABLE_5_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.19 MPU_16_PROGRAMMABLE_5_END_ADDRESS Register

5.17.2.19.1 MPU_16_PROGRAMMABLE_5_END_ADDRESS Register (Offset = 244h) [reset = 0h]

Programmable_5_End_Address.

Return to Summary Table

Table 5-2151. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0244h
MPU_R5SS0_CORE1_AHB	401E 0244h
MPU_R5SS1_CORE0_AHB	4020 0244h
MPU_R5SS1_CORE1_AHB	4022 0244h
MPU_SCRM2SCRP0	4018 0244h
MPU_SCRM2SCRP1	401A 0244h

Figure 5-1051. MPU_16_PROGRAMMABLE_5_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2152. MPU_16_PROGRAMMABLE_5_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.20 MPU_16_PROGRAMMABLE_5_MPPA Register

5.17.2.20.1 MPU_16_PROGRAMMABLE_5_MPPA Register (Offset = 248h) [reset = 0h]

Programmable_5_MPPA.

Return to Summary Table

Table 5-2153. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0248h
MPU_R5SS0_CORE1_AHB	401E 0248h
MPU_R5SS1_CORE0_AHB	4020 0248h
MPU_R5SS1_CORE1_AHB	4022 0248h
MPU_SCRM2SCRP0	4018 0248h
MPU_SCRM2SCRP1	401A 0248h

Figure 5-1052. MPU_16_PROGRAMMABLE_5_MPPA Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="3">RESERVED3</td><td>LOCK</td><td colspan="2">RESERVED2</td><td colspan="2">AID15_0</td></tr>
<tr><td colspan="3">R</td><td>R/W</td><td colspan="2">R</td><td colspan="2">R/W</td></tr>
<tr><td colspan="3">0h</td><td>0h</td><td colspan="2">0h</td><td colspan="2">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">AID15_0</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">AID15_0</td><td>AIDX</td><td>RESERVED1</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>NS</td><td>EMU</td><td>SR</td><td>SW</td><td>SX</td><td>UR</td><td>UW</td><td>UX</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-2154. MPU_16_PROGRAMMABLE_5_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2154. MPU_16_PROGRAMMABLE_5_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.21 MPU_16_PROGRAMMABLE_6_START_ADDRESS Register

5.17.2.21.1 MPU_16_PROGRAMMABLE_6_START_ADDRESS Register (Offset = 250h) [reset = 0h]

Programmable_6_Start_Address.

Return to Summary Table

Table 5-2155. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0250h
MPU_R5SS0_CORE1_AHB	401E 0250h
MPU_R5SS1_CORE0_AHB	4020 0250h
MPU_R5SS1_CORE1_AHB	4022 0250h
MPU_SCRM2SCRP0	4018 0250h
MPU_SCRM2SCRP1	401A 0250h

Figure 5-1053. MPU_16_PROGRAMMABLE_6_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2156. MPU_16_PROGRAMMABLE_6_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.22 MPU_16_PROGRAMMABLE_6_END_ADDRESS Register

5.17.2.22.1 MPU_16_PROGRAMMABLE_6_END_ADDRESS Register (Offset = 254h) [reset = 0h]

Programmable_6_End_Address.

Return to Summary Table

Table 5-2157. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0254h
MPU_R5SS0_CORE1_AHB	401E 0254h
MPU_R5SS1_CORE0_AHB	4020 0254h
MPU_R5SS1_CORE1_AHB	4022 0254h
MPU_SCRM2SCRP0	4018 0254h
MPU_SCRM2SCRP1	401A 0254h

Figure 5-1054. MPU_16_PROGRAMMABLE_6_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2158. MPU_16_PROGRAMMABLE_6_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.23 MPU_16_PROGRAMMABLE_6_MPPA Register

5.17.2.23.1 MPU_16_PROGRAMMABLE_6_MPPA Register (Offset = 258h) [reset = 0h]

Programmable_6_MPPA.

Return to Summary Table

Table 5-2159. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0258h
MPU_R5SS0_CORE1_AHB	401E 0258h
MPU_R5SS1_CORE0_AHB	4020 0258h
MPU_R5SS1_CORE1_AHB	4022 0258h
MPU_SCRM2SCRP0	4018 0258h
MPU_SCRM2SCRP1	401A 0258h

Figure 5-1055. MPU_16_PROGRAMMABLE_6_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2160. MPU_16_PROGRAMMABLE_6_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2160. MPU_16_PROGRAMMABLE_6_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.24 MPU_16_PROGRAMMABLE_7_START_ADDRESS Register

5.17.2.24.1 MPU_16_PROGRAMMABLE_7_START_ADDRESS Register (Offset = 260h) [reset = 0h]

Programmable_7_Start_Address.

Return to Summary Table

Table 5-2161. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0260h
MPU_R5SS0_CORE1_AHB	401E 0260h
MPU_R5SS1_CORE0_AHB	4020 0260h
MPU_R5SS1_CORE1_AHB	4022 0260h
MPU_SCRM2SCRP0	4018 0260h
MPU_SCRM2SCRP1	401A 0260h

Figure 5-1056. MPU_16_PROGRAMMABLE_7_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
START_ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
START_ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDR							
R/W							
0h							

Table 5-2162. MPU_16_PROGRAMMABLE_7_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.25 MPU_16_PROGRAMMABLE_7_END_ADDRESS Register

5.17.2.25.1 MPU_16_PROGRAMMABLE_7_END_ADDRESS Register (Offset = 264h) [reset = 0h]

Programmable_7_End_Address.

Return to Summary Table

Table 5-2163. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0264h
MPU_R5SS0_CORE1_AHB	401E 0264h
MPU_R5SS1_CORE0_AHB	4020 0264h
MPU_R5SS1_CORE1_AHB	4022 0264h
MPU_SCRM2SCRP0	4018 0264h
MPU_SCRM2SCRP1	401A 0264h

Figure 5-1057. MPU_16_PROGRAMMABLE_7_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2164. MPU_16_PROGRAMMABLE_7_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.26 MPU_16_PROGRAMMABLE_7_MPPA Register

5.17.2.26.1 MPU_16_PROGRAMMABLE_7_MPPA Register (Offset = 268h) [reset = 0h]

Programmable_7_MPPA.

Return to Summary Table

Table 5-2165. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0268h
MPU_R5SS0_CORE1_AHB	401E 0268h
MPU_R5SS1_CORE0_AHB	4020 0268h
MPU_R5SS1_CORE1_AHB	4022 0268h
MPU_SCRM2SCRP0	4018 0268h
MPU_SCRM2SCRP1	401A 0268h

Figure 5-1058. MPU_16_PROGRAMMABLE_7_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2166. MPU_16_PROGRAMMABLE_7_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2166. MPU_16_PROGRAMMABLE_7_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.27 MPU_16_PROGRAMMABLE_8_START_ADDRESS Register

5.17.2.27.1 MPU_16_PROGRAMMABLE_8_START_ADDRESS Register (Offset = 270h) [reset = 0h]

Programmable_8_Start_Address.

Return to Summary Table

Table 5-2167. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0270h
MPU_R5SS0_CORE1_AHB	401E 0270h
MPU_R5SS1_CORE0_AHB	4020 0270h
MPU_R5SS1_CORE1_AHB	4022 0270h
MPU_SCRM2SCRP0	4018 0270h
MPU_SCRM2SCRP1	401A 0270h

Figure 5-1059. MPU_16_PROGRAMMABLE_8_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2168. MPU_16_PROGRAMMABLE_8_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.28 MPU_16_PROGRAMMABLE_8_END_ADDRESS Register

5.17.2.28.1 MPU_16_PROGRAMMABLE_8_END_ADDRESS Register (Offset = 274h) [reset = 0h]

Programmable_8_End_Address.

Return to Summary Table

Table 5-2169. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0274h
MPU_R5SS0_CORE1_AHB	401E 0274h
MPU_R5SS1_CORE0_AHB	4020 0274h
MPU_R5SS1_CORE1_AHB	4022 0274h
MPU_SCRM2SCRP0	4018 0274h
MPU_SCRM2SCRP1	401A 0274h

Figure 5-1060. MPU_16_PROGRAMMABLE_8_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2170. MPU_16_PROGRAMMABLE_8_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.29 MPU_16_PROGRAMMABLE_8_MPPA Register

5.17.2.29.1 MPU_16_PROGRAMMABLE_8_MPPA Register (Offset = 278h) [reset = 0h]

Programmable_8_MPPA.

Return to Summary Table

Table 5-2171. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0278h
MPU_R5SS0_CORE1_AHB	401E 0278h
MPU_R5SS1_CORE0_AHB	4020 0278h
MPU_R5SS1_CORE1_AHB	4022 0278h
MPU_SCRM2SCRP0	4018 0278h
MPU_SCRM2SCRP1	401A 0278h

Figure 5-1061. MPU_16_PROGRAMMABLE_8_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2172. MPU_16_PROGRAMMABLE_8_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2172. MPU_16_PROGRAMMABLE_8_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.30 MPU_16_PROGRAMMABLE_9_START_ADDRESS Register

5.17.2.30.1 MPU_16_PROGRAMMABLE_9_START_ADDRESS Register (Offset = 280h) [reset = 0h]

Programmable_9_Start_Address.

Return to Summary Table

Table 5-2173. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0280h
MPU_R5SS0_CORE1_AHB	401E 0280h
MPU_R5SS1_CORE0_AHB	4020 0280h
MPU_R5SS1_CORE1_AHB	4022 0280h
MPU_SCRM2SCRP0	4018 0280h
MPU_SCRM2SCRP1	401A 0280h

Figure 5-1062. MPU_16_PROGRAMMABLE_9_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2174. MPU_16_PROGRAMMABLE_9_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.31 MPU_16_PROGRAMMABLE_9_END_ADDRESS Register

5.17.2.31.1 MPU_16_PROGRAMMABLE_9_END_ADDRESS Register (Offset = 284h) [reset = 0h]

Programmable_9_End_Address.

Return to Summary Table

Table 5-2175. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0284h
MPU_R5SS0_CORE1_AHB	401E 0284h
MPU_R5SS1_CORE0_AHB	4020 0284h
MPU_R5SS1_CORE1_AHB	4022 0284h
MPU_SCRM2SCRP0	4018 0284h
MPU_SCRM2SCRP1	401A 0284h

Figure 5-1063. MPU_16_PROGRAMMABLE_9_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2176. MPU_16_PROGRAMMABLE_9_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.32 MPU_16_PROGRAMMABLE_9_MPPA Register

5.17.2.32.1 MPU_16_PROGRAMMABLE_9_MPPA Register (Offset = 288h) [reset = 0h]

Programmable_9_MPPA.

Return to Summary Table

Table 5-2177. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0288h
MPU_R5SS0_CORE1_AHB	401E 0288h
MPU_R5SS1_CORE0_AHB	4020 0288h
MPU_R5SS1_CORE1_AHB	4022 0288h
MPU_SCRM2SCRP0	4018 0288h
MPU_SCRM2SCRP1	401A 0288h

Figure 5-1064. MPU_16_PROGRAMMABLE_9_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2178. MPU_16_PROGRAMMABLE_9_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2178. MPU_16_PROGRAMMABLE_9_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.33 MPU_16_PROGRAMMABLE_10_START_ADDRESS Register

5.17.2.33.1 MPU_16_PROGRAMMABLE_10_START_ADDRESS Register (Offset = 290h) [reset = 0h]

Programmable_10_Start_Address.

Return to Summary Table

Table 5-2179. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0290h
MPU_R5SS0_CORE1_AHB	401E 0290h
MPU_R5SS1_CORE0_AHB	4020 0290h
MPU_R5SS1_CORE1_AHB	4022 0290h
MPU_SCRM2SCRP0	4018 0290h
MPU_SCRM2SCRP1	401A 0290h

Figure 5-1065. MPU_16_PROGRAMMABLE_10_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2180. MPU_16_PROGRAMMABLE_10_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.34 MPU_16_PROGRAMMABLE_10_END_ADDRESS Register

5.17.2.34.1 MPU_16_PROGRAMMABLE_10_END_ADDRESS Register (Offset = 294h) [reset = 0h]

Programmable_10_End_Address.

Return to Summary Table

Table 5-2181. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0294h
MPU_R5SS0_CORE1_AHB	401E 0294h
MPU_R5SS1_CORE0_AHB	4020 0294h
MPU_R5SS1_CORE1_AHB	4022 0294h
MPU_SCRM2SCRP0	4018 0294h
MPU_SCRM2SCRP1	401A 0294h

Figure 5-1066. MPU_16_PROGRAMMABLE_10_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2182. MPU_16_PROGRAMMABLE_10_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.35 MPU_16_PROGRAMMABLE_10_MPPA Register

5.17.2.35.1 MPU_16_PROGRAMMABLE_10_MPPA Register (Offset = 298h) [reset = 0h]

Programmable_10_MPPA.

Return to Summary Table

Table 5-2183. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0298h
MPU_R5SS0_CORE1_AHB	401E 0298h
MPU_R5SS1_CORE0_AHB	4020 0298h
MPU_R5SS1_CORE1_AHB	4022 0298h
MPU_SCRM2SCRP0	4018 0298h
MPU_SCRM2SCRP1	401A 0298h

Figure 5-1067. MPU_16_PROGRAMMABLE_10_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2184. MPU_16_PROGRAMMABLE_10_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2184. MPU_16_PROGRAMMABLE_10_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.36 MPU_16_PROGRAMMABLE_11_START_ADDRESS Register

5.17.2.36.1 MPU_16_PROGRAMMABLE_11_START_ADDRESS Register (Offset = 2A0h) [reset = 0h]

Programmable_11_Start_Address.

Return to Summary Table

Table 5-2185. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02A0h
MPU_R5SS0_CORE1_AHB	401E 02A0h
MPU_R5SS1_CORE0_AHB	4020 02A0h
MPU_R5SS1_CORE1_AHB	4022 02A0h
MPU_SCRM2SCRP0	4018 02A0h
MPU_SCRM2SCRP1	401A 02A0h

Figure 5-1068. MPU_16_PROGRAMMABLE_11_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2186. MPU_16_PROGRAMMABLE_11_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.37 MPU_16_PROGRAMMABLE_11_END_ADDRESS Register

5.17.2.37.1 MPU_16_PROGRAMMABLE_11_END_ADDRESS Register (Offset = 2A4h) [reset = 0h]

Programmable_11_End_Address.

Return to Summary Table

Table 5-2187. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02A4h
MPU_R5SS0_CORE1_AHB	401E 02A4h
MPU_R5SS1_CORE0_AHB	4020 02A4h
MPU_R5SS1_CORE1_AHB	4022 02A4h
MPU_SCRM2SCRP0	4018 02A4h
MPU_SCRM2SCRP1	401A 02A4h

Figure 5-1069. MPU_16_PROGRAMMABLE_11_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2188. MPU_16_PROGRAMMABLE_11_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.38 MPU_16_PROGRAMMABLE_11_MPPA Register

5.17.2.38.1 MPU_16_PROGRAMMABLE_11_MPPA Register (Offset = 2A8h) [reset = 0h]

Programmable_11_MPPA.

Return to Summary Table

Table 5-2189. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02A8h
MPU_R5SS0_CORE1_AHB	401E 02A8h
MPU_R5SS1_CORE0_AHB	4020 02A8h
MPU_R5SS1_CORE1_AHB	4022 02A8h
MPU_SCRM2SCRP0	4018 02A8h
MPU_SCRM2SCRP1	401A 02A8h

Figure 5-1070. MPU_16_PROGRAMMABLE_11_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2190. MPU_16_PROGRAMMABLE_11_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2190. MPU_16_PROGRAMMABLE_11_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.39 MPU_16_PROGRAMMABLE_12_START_ADDRESS Register

5.17.2.39.1 MPU_16_PROGRAMMABLE_12_START_ADDRESS Register (Offset = 2B0h) [reset = 0h]

Programmable_12_Start_Address.

Return to Summary Table

Table 5-2191. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02B0h
MPU_R5SS0_CORE1_AHB	401E 02B0h
MPU_R5SS1_CORE0_AHB	4020 02B0h
MPU_R5SS1_CORE1_AHB	4022 02B0h
MPU_SCRM2SCRP0	4018 02B0h
MPU_SCRM2SCRP1	401A 02B0h

Figure 5-1071. MPU_16_PROGRAMMABLE_12_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2192. MPU_16_PROGRAMMABLE_12_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.40 MPU_16_PROGRAMMABLE_12_END_ADDRESS Register

5.17.2.40.1 MPU_16_PROGRAMMABLE_12_END_ADDRESS Register (Offset = 2B4h) [reset = 0h]

Programmable_12_End_Address.

Return to Summary Table

Table 5-2193. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02B4h
MPU_R5SS0_CORE1_AHB	401E 02B4h
MPU_R5SS1_CORE0_AHB	4020 02B4h
MPU_R5SS1_CORE1_AHB	4022 02B4h
MPU_SCRM2SCRP0	4018 02B4h
MPU_SCRM2SCRP1	401A 02B4h

Figure 5-1072. MPU_16_PROGRAMMABLE_12_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2194. MPU_16_PROGRAMMABLE_12_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.41 MPU_16_PROGRAMMABLE_12_MPPA Register

5.17.2.41.1 MPU_16_PROGRAMMABLE_12_MPPA Register (Offset = 2B8h) [reset = 0h]

Programmable_12_MPPA.

Return to Summary Table

Table 5-2195. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02B8h
MPU_R5SS0_CORE1_AHB	401E 02B8h
MPU_R5SS1_CORE0_AHB	4020 02B8h
MPU_R5SS1_CORE1_AHB	4022 02B8h
MPU_SCRM2SCRP0	4018 02B8h
MPU_SCRM2SCRP1	401A 02B8h

Figure 5-1073. MPU_16_PROGRAMMABLE_12_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2196. MPU_16_PROGRAMMABLE_12_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2196. MPU_16_PROGRAMMABLE_12_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.42 MPU_16_PROGRAMMABLE_13_START_ADDRESS Register

5.17.2.42.1 MPU_16_PROGRAMMABLE_13_START_ADDRESS Register (Offset = 2C0h) [reset = 0h]

Programmable_13_Start_Address.

Return to Summary Table

Table 5-2197. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02C0h
MPU_R5SS0_CORE1_AHB	401E 02C0h
MPU_R5SS1_CORE0_AHB	4020 02C0h
MPU_R5SS1_CORE1_AHB	4022 02C0h
MPU_SCRM2SCRP0	4018 02C0h
MPU_SCRM2SCRP1	401A 02C0h

Figure 5-1074. MPU_16_PROGRAMMABLE_13_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2198. MPU_16_PROGRAMMABLE_13_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.43 MPU_16_PROGRAMMABLE_13_END_ADDRESS Register

5.17.2.43.1 MPU_16_PROGRAMMABLE_13_END_ADDRESS Register (Offset = 2C4h) [reset = 0h]

Programmable_13_End_Address.

Return to Summary Table

Table 5-2199. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02C4h
MPU_R5SS0_CORE1_AHB	401E 02C4h
MPU_R5SS1_CORE0_AHB	4020 02C4h
MPU_R5SS1_CORE1_AHB	4022 02C4h
MPU_SCRM2SCRP0	4018 02C4h
MPU_SCRM2SCRP1	401A 02C4h

Figure 5-1075. MPU_16_PROGRAMMABLE_13_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
END_ADDR							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
END_ADDR							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
END_ADDR							
R/W							
0h							

Table 5-2200. MPU_16_PROGRAMMABLE_13_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.44 MPU_16_PROGRAMMABLE_13_MPPA Register

5.17.2.44.1 MPU_16_PROGRAMMABLE_13_MPPA Register (Offset = 2C8h) [reset = 0h]

Programmable_13_MPPA.

Return to Summary Table

Table 5-2201. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02C8h
MPU_R5SS0_CORE1_AHB	401E 02C8h
MPU_R5SS1_CORE0_AHB	4020 02C8h
MPU_R5SS1_CORE1_AHB	4022 02C8h
MPU_SCRM2SCRP0	4018 02C8h
MPU_SCRM2SCRP1	401A 02C8h

Figure 5-1076. MPU_16_PROGRAMMABLE_13_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2202. MPU_16_PROGRAMMABLE_13_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2202. MPU_16_PROGRAMMABLE_13_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.45 MPU_16_PROGRAMMABLE_14_START_ADDRESS Register

5.17.2.45.1 MPU_16_PROGRAMMABLE_14_START_ADDRESS Register (Offset = 2D0h) [reset = 0h]

Programmable_14_Start_Address.

Return to Summary Table

Table 5-2203. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02D0h
MPU_R5SS0_CORE1_AHB	401E 02D0h
MPU_R5SS1_CORE0_AHB	4020 02D0h
MPU_R5SS1_CORE1_AHB	4022 02D0h
MPU_SCRM2SCRP0	4018 02D0h
MPU_SCRM2SCRP1	401A 02D0h

Figure 5-1077. MPU_16_PROGRAMMABLE_14_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2204. MPU_16_PROGRAMMABLE_14_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.46 MPU_16_PROGRAMMABLE_14_END_ADDRESS Register

5.17.2.46.1 MPU_16_PROGRAMMABLE_14_END_ADDRESS Register (Offset = 2D4h) [reset = 0h]

Programmable_14_End_Address.

Return to Summary Table

Table 5-2205. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02D4h
MPU_R5SS0_CORE1_AHB	401E 02D4h
MPU_R5SS1_CORE0_AHB	4020 02D4h
MPU_R5SS1_CORE1_AHB	4022 02D4h
MPU_SCRM2SCRP0	4018 02D4h
MPU_SCRM2SCRP1	401A 02D4h

Figure 5-1078. MPU_16_PROGRAMMABLE_14_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2206. MPU_16_PROGRAMMABLE_14_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.47 MPU_16_PROGRAMMABLE_14_MPPA Register

5.17.2.47.1 MPU_16_PROGRAMMABLE_14_MPPA Register (Offset = 2D8h) [reset = 0h]

Programmable_14_MPPA.

Return to Summary Table

Table 5-2207. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02D8h
MPU_R5SS0_CORE1_AHB	401E 02D8h
MPU_R5SS1_CORE0_AHB	4020 02D8h
MPU_R5SS1_CORE1_AHB	4022 02D8h
MPU_SCRM2SCRP0	4018 02D8h
MPU_SCRM2SCRP1	401A 02D8h

Figure 5-1079. MPU_16_PROGRAMMABLE_14_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2208. MPU_16_PROGRAMMABLE_14_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2208. MPU_16_PROGRAMMABLE_14_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.48 MPU_16_PROGRAMMABLE_15_START_ADDRESS Register

5.17.2.48.1 MPU_16_PROGRAMMABLE_15_START_ADDRESS Register (Offset = 2E0h) [reset = 0h]

Programmable_15_Start_Address.

Return to Summary Table

Table 5-2209. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02E0h
MPU_R5SS0_CORE1_AHB	401E 02E0h
MPU_R5SS1_CORE0_AHB	4020 02E0h
MPU_R5SS1_CORE1_AHB	4022 02E0h
MPU_SCRM2SCRP0	4018 02E0h
MPU_SCRM2SCRP1	401A 02E0h

Figure 5-1080. MPU_16_PROGRAMMABLE_15_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2210. MPU_16_PROGRAMMABLE_15_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.49 MPU_16_PROGRAMMABLE_15_END_ADDRESS Register

5.17.2.49.1 MPU_16_PROGRAMMABLE_15_END_ADDRESS Register (Offset = 2E4h) [reset = 0h]

Programmable_15_End_Address.

Return to Summary Table

Table 5-2211. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02E4h
MPU_R5SS0_CORE1_AHB	401E 02E4h
MPU_R5SS1_CORE0_AHB	4020 02E4h
MPU_R5SS1_CORE1_AHB	4022 02E4h
MPU_SCRM2SCRP0	4018 02E4h
MPU_SCRM2SCRP1	401A 02E4h

Figure 5-1081. MPU_16_PROGRAMMABLE_15_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2212. MPU_16_PROGRAMMABLE_15_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.50 MPU_16_PROGRAMMABLE_15_MPPA Register

5.17.2.50.1 MPU_16_PROGRAMMABLE_15_MPPA Register (Offset = 2E8h) [reset = 0h]

Programmable_15_MPPA.

Return to Summary Table

Table 5-2213. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02E8h
MPU_R5SS0_CORE1_AHB	401E 02E8h
MPU_R5SS1_CORE0_AHB	4020 02E8h
MPU_R5SS1_CORE1_AHB	4022 02E8h
MPU_SCRM2SCRP0	4018 02E8h
MPU_SCRM2SCRP1	401A 02E8h

Figure 5-1082. MPU_16_PROGRAMMABLE_15_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2214. MPU_16_PROGRAMMABLE_15_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2214. MPU_16_PROGRAMMABLE_15_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.51 MPU_16_PROGRAMMABLE_16_START_ADDRESS Register

5.17.2.51.1 MPU_16_PROGRAMMABLE_16_START_ADDRESS Register (Offset = 2F0h) [reset = 0h]

Programmable_16_Start_Address.

Return to Summary Table

Table 5-2215. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02F0h
MPU_R5SS0_CORE1_AHB	401E 02F0h
MPU_R5SS1_CORE0_AHB	4020 02F0h
MPU_R5SS1_CORE1_AHB	4022 02F0h
MPU_SCRM2SCRP0	4018 02F0h
MPU_SCRM2SCRP1	401A 02F0h

Figure 5-1083. MPU_16_PROGRAMMABLE_16_START_ADDRESS Name Register

31	30	29	28	27	26	25	24
START_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
START_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
START_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
START_ADDR							
R/W							
0h							

Table 5-2216. MPU_16_PROGRAMMABLE_16_START_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START_ADDR	R/W	0h	Start address for range N. Defaults to input signal value.

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5.17.2.52 MPU_16_PROGRAMMABLE_16_END_ADDRESS Register

5.17.2.52.1 MPU_16_PROGRAMMABLE_16_END_ADDRESS Register (Offset = 2F4h) [reset = 0h]

Programmable_16_End_Address.

Return to Summary Table

Table 5-2217. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02F4h
MPU_R5SS0_CORE1_AHB	401E 02F4h
MPU_R5SS1_CORE0_AHB	4020 02F4h
MPU_R5SS1_CORE1_AHB	4022 02F4h
MPU_SCRM2SCRP0	4018 02F4h
MPU_SCRM2SCRP1	401A 02F4h

Figure 5-1084. MPU_16_PROGRAMMABLE_16_END_ADDRESS Name Register

31	30	29	28	27	26	25	24
END_ADDR							
R/W							
0h							
23	22	21	20	19	18	17	16
END_ADDR							
R/W							
0h							
15	14	13	12	11	10	9	8
END_ADDR							
R/W							
0h							
7	6	5	4	3	2	1	0
END_ADDR							
R/W							
0h							

Table 5-2218. MPU_16_PROGRAMMABLE_16_END_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END_ADDR	R/W	0h	End address for range N. Defaults to input signal value.

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5.17.2.53 MPU_16_PROGRAMMABLE_16_MPPA Register

5.17.2.53.1 MPU_16_PROGRAMMABLE_16_MPPA Register (Offset = 2F8h) [reset = 0h]

Programmable_16_MPPA.

Return to Summary Table

Table 5-2219. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 02F8h
MPU_R5SS0_CORE1_AHB	401E 02F8h
MPU_R5SS1_CORE0_AHB	4020 02F8h
MPU_R5SS1_CORE1_AHB	4022 02F8h
MPU_SCRM2SCRP0	4018 02F8h
MPU_SCRM2SCRP1	401A 02F8h

Figure 5-1085. MPU_16_PROGRAMMABLE_16_MPPA Name Register

31	30	29	28	27	26	25	24
RESERVED3			LOCK	RESERVED2		AID15_0	
R			R/W	R		R/W	
0h			0h	0h		0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
AID15_0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
AID15_0						AIDX	RESERVED1
R/W						R/W	R
0h						0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	EMU	SR	SW	SX	UR	UW	UX
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2220. MPU_16_PROGRAMMABLE_16_MPPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:29	RESERVED3	R	0h	Always read as 0
28	LOCK	R/W	0h	this field is used for locking the corresponding MPU region configurations. Write 1 to lock the configurations along with the lock bit. Writing 1 is alllowed once per boot. Lock bit will clear on reset only. Once locked SW can not modify the MPU configurations along with lock bit.
27:26	RESERVED2	R	0h	Always read as 0.
25:10	AID15_0	R/W	0h	AIDs checked for this region. Defaults to input value. 0 = AID is not checked for these permissions. 1 = AID is checked for these permissions.
9	AIDX	R/W	0h	Additional AIDs checked. Defaults to input value.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R/W	0h	Non-secure permission. Defaults to input value.
6	EMU	R/W	0h	Debug permission. Defaults to input value.
5	SR	R/W	0h	Supervisor read permission. Defaults to input value.

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Table 5-2220. MPU_16_PROGRAMMABLE_16_MPPA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SW	R/W	0h	Supervisor write permission. Defaults to input value.
3	SX	R/W	0h	Supervisor executable permission. Defaults to input value.
2	UR	R/W	0h	User read permission. Defaults to input value.
1	UW	R/W	0h	User write permission. Defaults to input value.
0	UX	R/W	0h	User executable permission. Defaults to input value.

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5.17.2.54 MPU_16_FAULT_ADDRESS Register

5.17.2.54.1 MPU_16_FAULT_ADDRESS Register (Offset = 300h) [reset = 0h]

Fault_Address.

Return to Summary Table

Table 5-2221. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0300h
MPU_R5SS0_CORE1_AHB	401E 0300h
MPU_R5SS1_CORE0_AHB	4020 0300h
MPU_R5SS1_CORE1_AHB	4022 0300h
MPU_SCRM2SCRP0	4018 0300h
MPU_SCRM2SCRP1	401A 0300h

Figure 5-1086. MPU_16_FAULT_ADDRESS Name Register

31	30	29	28	27	26	25	24
FAULT_ADDR							
R							
0h							
23	22	21	20	19	18	17	16
FAULT_ADDR							
R							
0h							
15	14	13	12	11	10	9	8
FAULT_ADDR							
R							
0h							
7	6	5	4	3	2	1	0
FAULT_ADDR							
R							
0h							

Table 5-2222. MPU_16_FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FAULT_ADDR	R	0h	Fault_address.

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5.17.2.55 MPU_16_FAULT_STATUS Register

5.17.2.55.1 MPU_16_FAULT_STATUS Register (Offset = 304h) [reset = 0h]

Fault_Status.

Return to Summary Table

Table 5-2223. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0304h
MPU_R5SS0_CORE1_AHB	401E 0304h
MPU_R5SS1_CORE0_AHB	4020 0304h
MPU_R5SS1_CORE1_AHB	4022 0304h
MPU_SCRM2SCRP0	4018 0304h
MPU_SCRM2SCRP1	401A 0304h

Figure 5-1087. MPU_16_FAULT_STATUS Name Register

31	30	29	28	27	26	25	24
ID							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MSTID							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			PRIVID				RESERVED1
R			R				R
0h			0h				0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NS	RESERVED2	FAULT_TYPE					
R	R	R					
0h	0h	0h					

Table 5-2224. MPU_16_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ID	R	0h	Transfer ID
23:16	MSTID	R	0h	Master ID.
15:13	RESERVED	R	0h	Always read as 0.
12:9	PRIVID	R	0h	Privilege ID.
8	RESERVED1	R	0h	Always read as 0.
7	NS	R	0h	Non-secure access.
6	RESERVED2	R	0h	Always read as 0.
5:0	FAULT_TYPE	R	0h	Fault_type. 100000 = supervisor read fault 010000 = supervisor write fault 001000 = supervisor execute fault 000100 = user read fault 000010 = user write fault 000001 = user execute fault 111111 = relaxed cache linefill fault 010010 = relaxed cache writeback fault 000000 = no fault

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5.17.2.56 MPU_16_FAULT_CLEAR Register

5.17.2.56.1 MPU_16_FAULT_CLEAR Register (Offset = 308h) [reset = 0h]

Fault_Clear.

Return to Summary Table

Table 5-2225. Instance Table

Instance Name	Physical Address
MPU_R5SS0_CORE0_AHB	401C 0308h
MPU_R5SS0_CORE1_AHB	401E 0308h
MPU_R5SS1_CORE0_AHB	4020 0308h
MPU_R5SS1_CORE1_AHB	4022 0308h
MPU_SCRM2SCRP0	4018 0308h
MPU_SCRM2SCRP1	401A 0308h

Figure 5-1088. MPU_16_FAULT_CLEAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							FAULT_CLR
R							W
0h							0h

Table 5-2226. MPU_16_FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	R	0h	Always read as 0.
0	FAULT_CLR	W	0h	Fault_clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

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5.18 MSRAM

MSRAM

5.18.1 MSRAM Summaries

MSRAM Summaries

Table 5-2227. MSRAM Registers, Base Address=7000 0000h, Length=524288

Offset	Length	Register Name	MSRAM_BANK0 Physical Address	MSRAM_BANK1 Physical Address	MSRAM_BANK2 Physical Address
0h	32	MSRAM_START	7000 0000h	7008 0000h	7010 0000h
7FFFC h	32	MSRAM_END	7007 FFFCh	700F FFFCh	7017 FFFCh

Table 5-2228. MSRAM Registers, Base Address=7000 0000h, Length=524288

Offset	Length	Register Name	MSRAM_BANK3 Physical Address	MSRAM_BANK4 Physical Address	MSRAM_BANK5 Physical Address
0h	32	MSRAM_START	7018 0000h	7020 0000h	7028 0000h
7FFFC h	32	MSRAM_END	701F FFFCh	7027 FFFCh	702F FFFCh

5.18.2 MSRAM Registers

MSRAM Registers

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5.18.2.1 MSRAM_START Register

5.18.2.1.1 MSRAM_START Register (Offset = 0h) [reset = 0h]

L2 Memory start address.

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Table 5-2229. Instance Table

Instance Name	Physical Address
MSRAM_BANK0	7000 0000h
MSRAM_BANK1	7008 0000h
MSRAM_BANK2	7010 0000h
MSRAM_BANK3	7018 0000h
MSRAM_BANK4	7020 0000h
MSRAM_BANK5	7028 0000h

Figure 5-1089. MSRAM_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 5-2230. MSRAM_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	L2 Memory start address

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5.18.2.2 MSRAM_END Register

5.18.2.2.1 MSRAM_END Register (Offset = 7FFFCh) [reset = 0h]

L2 Memory end address.

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Table 5-2231. Instance Table

Instance Name	Physical Address
MSRAM_BANK0	7007 FFFCh
MSRAM_BANK1	700F FFFCh
MSRAM_BANK2	7017 FFFCh
MSRAM_BANK3	701F FFFCh
MSRAM_BANK4	7027 FFFCh
MSRAM_BANK5	702F FFFCh

Figure 5-1090. MSRAM_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 5-2232. MSRAM_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	L2 Memory end address

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5.19 PBIST

PBIST

5.19.1 PBIST Summaries

PBIST Summaries

Table 5-2233. PBIST Registers, Base Address=5330 0000h, Length=512

Offset	Length	Register Name	PBIST0 Physical Address
164h	16	PBIST_DLR	5330 0164h
180h	8	PBIST_PACT	5330 0180h
184h	8	PBIST_ID	5330 0184h
190h	8	PBIST_FSFR0	5330 0190h
194h	8	PBIST_FSFR1	5330 0194h
198h	8	PBIST_FSRCR0	5330 0198h
19Ch	8	PBIST_FSRCR1	5330 019Ch
1C0h	8	PBIST_ROM	5330 01C0h
1C4h	32	PBIST_ALGO	5330 01C4h
1C8h	32	PBIST_RINFOL	5330 01C8h
1CCh	32	PBIST_RINFOU	5330 01CCh

5.19.2 PBIST Registers

PBIST Registers

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5.19.2.1 PBIST_DLR Register

5.19.2.1.1 PBIST_DLR Register (Offset = 164h) [reset = 208h]

Datalogger 0 .

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Table 5-2234. Instance Table

Instance Name	Physical Address
PBIST0	5330 0164h

Figure 5-1091. PBIST_DLR Name Register

15	14	13	12	11	10	9	8
DLR1							
R/W							
2h							
7	6	5	4	3	2	1	0
DLR0							
R/W							
8h							

Table 5-2235. PBIST_DLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	DLR1	R/W	2h	Datalogger Register [8] : Reserevd [9] : Default Testing Mode. When in this mode, ROM-based testing is kicked off. If the intention is to perform go/no-go testing via config, write to both this bit and bit [2] of the Datalogger Register simultaneously [15:10] : Reserevd
7:0	DLR0	R/W	8h	Datalogger Register [1:0] : Reserved [2] : ROM-based testing mode. Setting this bit to 1 enables the PBIST controller to execute test algorithms that are stored in the PBIST ROM [3] : Do not change this bit from its default value of 1 [4] : Config access mode. Setting this bit allows the host processor to configure the PBIST controller registers [7:5] : Reserved

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5.19.2.2 PBIST_PACT Register

5.19.2.2.1 PBIST_PACT Register (Offset = 180h) [reset = 0h]

Pbist Active.

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Table 5-2236. Instance Table

Instance Name	Physical Address
PBIST0	5330 0180h

Figure 5-1092. PBIST_PACT Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED							PBIST_PACT
NONE							R/W
0h							0h

Table 5-2237. PBIST_PACT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	NONE	0h	Reserved
0	PBIST_PACT	R/W	0h	Pbist Active/ROM Clock Enable Register [0]: This bit must be set to turn on internal PBIST clocks. Setting this bit asserts an internal signal that is used as the clock gate enable. As long as this bit is 0, any access to PBIST will not go through, and PBIST will remain in an almost zero-power mode. Value 0 = Disable internal PBIST clocks Value 1 = Enable internal PBIST clocks

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5.19.2.3 PBIST_ID Register

5.19.2.3.1 PBIST_ID Register (Offset = 184h) [reset = 1h]

PBIST ID.

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Table 5-2238. Instance Table

Instance Name	Physical Address
PBIST0	5330 0184h

Figure 5-1093. PBIST_ID Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED			PBIST_ID				
NONE			R/W				
0h			1h				

Table 5-2239. PBIST_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	NONE	0h	Reserved
4:0	PBIST_ID	R/W	1h	PBIST ID. This is a unique ID assigned to each PBIST controller in a device with multiple PBIST controllers. The value of this register does not effect the functionality of the CPU interface.

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5.19.2.4 PBIST_FSFR0 Register

5.19.2.4.1 PBIST_FSFR0 Register (Offset = 190h) [reset = 0h]

Fail status fail - port 0 .

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Table 5-2240. Instance Table

Instance Name	Physical Address
PBIST0	5330 0190h

Figure 5-1094. PBIST_FSFR0 Name Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>PBIST_FSFR0</td></tr>
<tr><td colspan="7">NONE</td><td>R</td></tr>
<tr><td colspan="7">0h</td><td>0h</td></tr>
</table>

Table 5-2241. PBIST_FSFR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	NONE	0h	Reserved
0	PBIST_FSFR0	R	0h	Fail Status Fail Register- Port 0 This register indicates if a failure occurred during a memory self-test. Value 0 = No failure occurred Value 1 = Indicates a failure

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5.19.2.5 PBIST_FSFR1 Register

5.19.2.5.1 PBIST_FSFR1 Register (Offset = 194h) [reset = 0h]

Fail status fail - port 1

Return to Summary Table

Table 5-2242. Instance Table

Instance Name	Physical Address
PBIST0	5330 0194h

Figure 5-1095. PBIST_FSFR1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED							PBIST_FSFR1
NONE							R
0h							0h

Table 5-2243. PBIST_FSFR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	NONE	0h	Reserved
0	PBIST_FSFR1	R	0h	Fail Status Fail Register- Port 1 This register indicates if a failure occurred during a memory self-test. Value 0 = No failure occurred Value 1 = Indicates a failure

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5.19.2.6 PBIST_FSRCR0 Register

5.19.2.6.1 PBIST_FSRCR0 Register (Offset = 198h) [reset = 0h]

Fail Count fail - port 0 .

Return to Summary Table

Table 5-2244. Instance Table

Instance Name	Physical Address
PBIST0	5330 0198h

Figure 5-1096. PBIST_FSRCR0 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PBIST_FSRCR0			
NONE				R			
0h				0h			

Table 5-2245. PBIST_FSRCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	NONE	0h	Reserved
3:0	PBIST_FSRCR0	R	0h	Fail Status Count - Port 0 These registers keep count of the number of failures observed during the memory self-test. The PBIST controller stops executing the memory self-test whenever a failure occurs in any memory instance for any of the test algorithms. The value in gets incremented by one whenever a failure occurs

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5.19.2.7 PBIST_FSRCR1 Register

5.19.2.7.1 PBIST_FSRCR1 Register (Offset = 19Ch) [reset = 0h]

Fail Count fail - port 1

Return to Summary Table

Table 5-2246. Instance Table

Instance Name	Physical Address
PBIST0	5330 019Ch

Figure 5-1097. PBIST_FSRCR1 Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED				PBIST_FSRCR1			
NONE				R			
0h				0h			

Table 5-2247. PBIST_FSRCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	NONE	0h	Reserved
3:0	PBIST_FSRCR1	R	0h	Fail Status Count - Port 1 These registers keep count of the number of failures observed during the memory self-test. The PBIST controller stops executing the memory self-test whenever a failure occurs in any memory instance for any of the test algorithms. The value in gets incremented by one whenever a failure occurs

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5.19.2.8 PBIST_ROM Register

5.19.2.8.1 PBIST_ROM Register (Offset = 1C0h) [reset = 3h]

Rom Mask .

Return to Summary Table

Table 5-2248. Instance Table

Instance Name	Physical Address
PBIST0	5330 01C0h

Figure 5-1098. PBIST_ROM Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						PBIST_ROM	
NONE						R/W	
0h						3h	

Table 5-2249. PBIST_ROM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	NONE	0h	Reserved
1:0	PBIST_ROM	R/W	3h	Rom Mask . This two-bit register sets appropriate ROM access modes for the PBIST controller. Value 0h= No information is used from ROM Value 1h= Only RAM Group information from ROM Vaule 2h= Only Algorithm information from ROM Value 3h= Both Algorithm and RAM information from ROM. This option should be selected for application self-test.

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5.19.2.9 PBIST_ALGO Register

5.19.2.9.1 PBIST_ALGO Register (Offset = 1C4h) [reset = FFFFFFFFh]

ROM Algorithm Mask 0

Return to Summary Table

Table 5-2250. Instance Table

Instance Name	Physical Address
PBIST0	5330 01C4h

Figure 5-1099. PBIST_ALGO Name Register

31	30	29	28	27	26	25	24
ALGO3							
R/W							
FFh							
23	22	21	20	19	18	17	16
ALGO2							
R/W							
FFh							
15	14	13	12	11	10	9	8
ALGO1							
R/W							
FFh							
7	6	5	4	3	2	1	0
ALGO0							
R/W							
FFh							

Table 5-2251. PBIST_ALGO Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	ALGO3	R/W	FFh	This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm. Writing a value 1 to the particular bit, enables the corresponding algorithm. Writing a value 0 to the particular bit, disables the corresponding algorithm.
23:16	ALGO2	R/W	FFh	This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm. Writing a value 1 to the particular bit, enables the corresponding algorithm. Writing a value 0 to the particular bit, disables the corresponding algorithm.
15:8	ALGO1	R/W	FFh	This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm. Writing a value 1 to the particular bit, enables the corresponding algorithm. Writing a value 0 to the particular bit, disables the corresponding algorithm.

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Table 5-2251. PBIST_ALGO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	ALGO0	R/W	FFh	This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm. Writing a value 1 to the particular bit, enables the corresponding algorithm. Writing a value 0 to the particular bit, disables the corresponding algorithm.

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5.19.2.10 PBIST_RINFOL Register

5.19.2.10.1 PBIST_RINFOL Register (Offset = 1C8h) [reset = FFFFFFFFh]

RAM Info Mask Lower 0

Return to Summary Table

Table 5-2252. Instance Table

Instance Name	Physical Address
PBIST0	5330 01C8h

Figure 5-1100. PBIST_RINFOL Name Register

31	30	29	28	27	26	25	24
RINFOL3							
R/W							
FFh							
23	22	21	20	19	18	17	16
RINFOL2							
R/W							
FFh							
15	14	13	12	11	10	9	8
RINFOL1							
R/W							
FFh							
7	6	5	4	3	2	1	0
RINFOL0							
R/W							
FFh							

Table 5-2253. PBIST_RINFOL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RINFOL3	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
23:16	RINFOL2	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
15:8	RINFOL1	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
7:0	RINFOL0	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.

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5.19.2.11 PBIST_RINFOU Register

5.19.2.11.1 PBIST_RINFOU Register (Offset = 1CCh) [reset = FFFFFFFFh]

RAM Info Mask Upper 0

Return to Summary Table

Table 5-2254. Instance Table

Instance Name	Physical Address
PBIST0	5330 01CCh

Figure 5-1101. PBIST_RINFOU Name Register

31	30	29	28	27	26	25	24
RINFOU3							
R/W							
FFh							
23	22	21	20	19	18	17	16
RINFOU2							
R/W							
FFh							
15	14	13	12	11	10	9	8
RINFOU1							
R/W							
FFh							
7	6	5	4	3	2	1	0
RINFOU0							
R/W							
FFh							

Table 5-2255. PBIST_RINFOU Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	RINFOU3	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
23:16	RINFOU2	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
15:8	RINFOU1	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
7:0	RINFOU0	R/W	FFh	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.

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5.20 ECC_AGGR

ECC_AGGR

5.20.1 ECC_AGGR Summaries

ECC_AGGR Summaries

Table 5-2256. ECC_AGGR Registers, Base Address=5301 0000h, Length=1024

Offset	Length	Register Name	ECC_AGGR Physical Address
0h	32	ECC_AGGR_AGGR_REVISION	5301 0000h
8h	32	ECC_AGGR_ECC_VECTOR	5301 0008h
Ch	32	ECC_AGGR_MISC_STATUS	5301 000Ch
10h	32	ECC_AGGR_ECC_WRAP_REVISION	5301 0010h
14h	32	ECC_AGGR_CONTROL	5301 0014h
18h	32	ECC_AGGR_ERROR_CTRL1	5301 0018h
1Ch	32	ECC_AGGR_ERROR_CTRL2	5301 001Ch
20h	32	ECC_AGGR_ERROR_STATUS1	5301 0020h
24h	32	ECC_AGGR_ERROR_STATUS2	5301 0024h
28h	32	ECC_AGGR_ERROR_STATUS3	5301 0028h
3Ch	32	ECC_AGGR_SEC_EOI_REG	5301 003Ch
40h	32	ECC_AGGR_SEC_STATUS_REG0	5301 0040h
80h	32	ECC_AGGR_SEC_ENABLE_SET_REG0	5301 0080h
C0h	32	ECC_AGGR_SEC_ENABLE_CLR_REG0	5301 00C0h
13Ch	32	ECC_AGGR_DED_EOI_REG	5301 013Ch
140h	32	ECC_AGGR_DED_STATUS_REG0	5301 0140h
180h	32	ECC_AGGR_DED_ENABLE_SET_REG0	5301 0180h
1C0h	32	ECC_AGGR_DED_ENABLE_CLR_REG0	5301 01C0h
200h	32	ECC_AGGR_AGGR_ENABLE_SET	5301 0200h
204h	32	ECC_AGGR_AGGR_ENABLE_CLR	5301 0204h
208h	32	ECC_AGGR_AGGR_STATUS_SET	5301 0208h
20Ch	32	ECC_AGGR_AGGR_STATUS_CLR	5301 020Ch

5.20.2 ECC_AGGR Registers

ECC_AGGR Registers

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5.20.2.1 ECC_AGGR_AGGR_REVISION Register

5.20.2.1.1 ECC_AGGR_AGGR_REVISION Register (Offset = 0h) [reset = 66A0C200h]

The Revision Register contains the major and minor revisions for the ECC aggregator module. It does not support byte accesses.

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Table 5-2257. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0000h

Figure 5-1102. ECC_AGGR_AGGR_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
18h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		0h					

Table 5-2258. ECC_AGGR_AGGR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business unit
27:16	MODULE_ID	R	6A0h	Module ID
15:11	REVRTL	R	18h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	0h	Minor version

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5.20.2.2 ECC_AGGR_ECC_VECTOR Register

5.20.2.2.1 ECC_AGGR_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

ECC RAM ID to select which ECC RAM to control or read status from.

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Table 5-2259. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0008h

Figure 5-1103. ECC_AGGR_ECC_VECTOR Name Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
NONE							R
0h							0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RD_SVBUS_ADDRESS							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1TS	NONE				R/W		
0h	0h				0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ECC_VECTOR							
R/W							
0h							

Table 5-2260. ECC_AGGR_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED	NONE	0h	Reserved
24	RD_SVBUS_DONE	R	0h	Status to indicate if read on serial bus is complete
23:16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Trigger a read operation to the specified read address that requires a serial bus access. In normal operation, the trigger bit is only '1' for a single cycle and thus can not be read back.
14:11	RESERVED	NONE	0h	Reserved
10:0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

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5.20.2.3 ECC_AGGR_MISC_STATUS Register

5.20.2.3.1 ECC_AGGR_MISC_STATUS Register (Offset = Ch) [reset = 9h]

Contains misc status such as number of ECC RAMs serviced by the ECC aggregator.

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Table 5-2261. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 000Ch

Figure 5-1104. ECC_AGGR_MISC_STATUS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED					NUM_RAMS		
NONE					R		
0h					9h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NUM_RAMS							
R							
9h							

Table 5-2262. ECC_AGGR_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:11	RESERVED	NONE	0h	Reserved
10:0	NUM_RAMS	R	9h	Indicates the number of RAMS serviced by the ECC aggregator

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5.20.2.4 ECC_AGGR_ECC_WRAP_REVISION Register

5.20.2.4.1 ECC_AGGR_ECC_WRAP_REVISION Register (Offset = 10h) [reset = 66A40202h]

Revision parameters.

Return to Summary Table

Table 5-2263. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0010h

Figure 5-1105. ECC_AGGR_ECC_WRAP_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R		R		R			
1h		2h		6A4h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
MODULE_ID							
R							
6A4h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
REVRTL					REVMAJ		
R					R		
0h					2h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		REVMIN					
R		R					
0h		2h					

Table 5-2264. ECC_AGGR_ECC_WRAP_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	Business unit
27:16	MODULE_ID	R	6A4h	Module ID
15:11	REVRTL	R	0h	RTL version
10:8	REVMAJ	R	2h	Major version
7:6	CUSTOM	R	0h	Custom version
5:0	REVMIN	R	2h	Minor version

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5.20.2.5 ECC_AGGR_CONTROL Register

5.20.2.5.1 ECC_AGGR_CONTROL Register (Offset = 14h) [reset = 187h]

ECC Control Register.

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Table 5-2265. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0014h

Figure 5-1106. ECC_AGGR_CONTROL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							CHECK_SVBUS_TIMEOUT
NONE							R/W
0h							1h
7	6	5	4	3	2	1	0
CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	0h	0h	0h	0h	1h	1h	1h

Table 5-2266. ECC_AGGR_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	CHECK_SVBUS_TIMEOUT	R/W	1h	check for svbus timeout errors
7	CHECK_PARITY	R/W	1h	check for parity errors
6	ERROR_ONCE	R/W	0h	Force Error only once
5	FORCE_N_ROW	R/W	0h	Force Error on any RAM read
4	FORCE_DED	R/W	0h	Force Double Bit Error
3	FORCE_SEC	R/W	0h	Force Single Bit Error
2	ENABLE_RMW	R/W	1h	Enable rmw
1	ECC_CHECK	R/W	1h	Enable ECC check
0	ECC_ENABLE	R/W	1h	Enable ECC

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5.20.2.6 ECC_AGGR_ERROR_CTRL1 Register

5.20.2.6.1 ECC_AGGR_ERROR_CTRL1 Register (Offset = 18h) [reset = 0h]

ECC Error Control1 Register.

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Table 5-2267. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0018h

Figure 5-1107. ECC_AGGR_ERROR_CTRL1 Name Register

31	30	29	28	27	26	25	24
ECC_ROW							
R/W							
0h							
23	22	21	20	19	18	17	16
ECC_ROW							
R/W							
0h							
15	14	13	12	11	10	9	8
ECC_ROW							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_ROW							
R/W							
0h							

Table 5-2268. ECC_AGGR_ERROR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R/W	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

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5.20.2.7 ECC_AGGR_ERROR_CTRL2 Register

5.20.2.7.1 ECC_AGGR_ERROR_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ECC Error Control2 Register.

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Table 5-2269. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 001Ch

Figure 5-1108. ECC_AGGR_ERROR_CTRL2 Name Register

31	30	29	28	27	26	25	24
ECC_BIT2							
R/W							
0h							
23	22	21	20	19	18	17	16
ECC_BIT2							
R/W							
0h							
15	14	13	12	11	10	9	8
ECC_BIT1							
R/W							
0h							
7	6	5	4	3	2	1	0
ECC_BIT1							
R/W							
0h							

Table 5-2270. ECC_AGGR_ERROR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT2	R/W	0h	Data bit that needs to be flipped if double bit error needs to be forced
15:0	ECC_BIT1	R/W	0h	Data bit that needs to be flipped when force_sec is set

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5.20.2.8 ECC_AGGR_ERROR_STATUS1 Register

5.20.2.8.1 ECC_AGGR_ERROR_STATUS1 Register (Offset = 20h) [reset = 0h]

ECC Error Status1 Register.

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Table 5-2271. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0020h

Figure 5-1109. ECC_AGGR_ERROR_STATUS1 Name Register

31	30	29	28	27	26	25	24
ECC_BIT1							
R							
0h							
23	22	21	20	19	18	17	16
ECC_BIT1							
R							
0h							
15	14	13	12	11	10	9	8
CLR_CTRL_REG_ERR	CLR_PARITY_ERR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC	
R/W1TC	R/WD		R/W1TC	R/WD		R/WD	
0h	0h		0h	0h		0h	
7	6	5	4	3	2	1	0
CTR_REG_ERR	PARITY_ERR		ECC_OTHER	ECC_DED		ECC_SEC	
R/W1TS	R/W1TS		R/W1TS	R/WI		R/WI	
0h	0h		0h	0h		0h	

Table 5-2272. ECC_AGGR_ERROR_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	ECC_BIT1	R	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	R/W1TC	0h	Clear control reg error Error Status, you must also re write the control register itself to clear this
14:13	CLR_PARITY_ERR	R/WD	0h	Clear parity Error Status
12	CLR_ECC_OTHER	R/W1TC	0h	Clear other Error Status
11:10	CLR_ECC_DED	R/WD	0h	Clear Double Bit Error Status
9:8	CLR_ECC_SEC	R/WD	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	R/W1TS	0h	control register error pending, Level interrupt
6:5	PARITY_ERR	R/W1TS	0h	Level parity error Error Status
4	ECC_OTHER	R/W1TS	0h	Successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3:2	ECC_DED	R/WI	0h	Level Double Bit Error Status
1:0	ECC_SEC	R/WI	0h	Level Single Bit Error Status

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5.20.2.9 ECC_AGGR_ERROR_STATUS2 Register

5.20.2.9.1 ECC_AGGR_ERROR_STATUS2 Register (Offset = 24h) [reset = 0h]

ECC Error Status2 Register.

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Table 5-2273. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0024h

Figure 5-1110. ECC_AGGR_ERROR_STATUS2 Name Register

31	30	29	28	27	26	25	24
ECC_ROW							
R							
0h							
23	22	21	20	19	18	17	16
ECC_ROW							
R							
0h							
15	14	13	12	11	10	9	8
ECC_ROW							
R							
0h							
7	6	5	4	3	2	1	0
ECC_ROW							
R							
0h							

Table 5-2274. ECC_AGGR_ERROR_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	ECC_ROW	R	0h	Row address where the single or double-bit error has occurred

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5.20.2.10 ECC_AGGR_ERROR_STATUS3 Register

5.20.2.10.1 ECC_AGGR_ERROR_STATUS3 Register (Offset = 28h) [reset = 0h]

ECC Error Status3 Register.

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Table 5-2275. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0028h

Figure 5-1111. ECC_AGGR_ERROR_STATUS3 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED						CLR_SVBUS_TIMEOUT_ERR	RESERVED
NONE						R/W1TC	NONE
0h						0h	0h
7	6	5	4	3	2	1	0
RESERVED						SVBUS_TIMEOUT_ERR	WB_PEND
NONE						R/W1TS	R
0h						0h	0h

Table 5-2276. ECC_AGGR_ERROR_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	RESERVED	NONE	0h	Reserved
9	CLR_SVBUS_TIMEOUT_ERR	R/W1TC	0h	Clear svbus timeout Error Status
8:2	RESERVED	NONE	0h	Reserved
1	SVBUS_TIMEOUT_ERR	R/W1TS	0h	Level svbus timeout error Error Status
0	WB_PEND	R	0h	delayed write back pending Status

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5.20.2.11 ECC_AGGR_SEC_EOI_REG Register

5.20.2.11.1 ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

Return to Summary Table

Table 5-2277. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 003Ch

Figure 5-1112. ECC_AGGR_SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 5-2278. ECC_AGGR_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	Write of 1 to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. The bit is self clearing and will be read as a zero.

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5.20.2.12 ECC_AGGR_SEC_STATUS_REG0 Register

5.20.2.12.1 ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

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Table 5-2279. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0040h

Figure 5-1113. ECC_AGGR_SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							MSS_L2SLV5_PEND
NONE							R/W1TS
0h							0h
7	6	5	4	3	2	1	0
MSS_L2SLV4_PEND	TPTC_A1_PEND	TPTC_A0_PEND	MSS_MBOX_PEND	MSS_L2SLV3_PEND	MSS_L2SLV2_PEND	MSS_L2SLV1_PEND	MSS_L2SLV0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2280. ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MSS_L2SLV5_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv5_pend
7	MSS_L2SLV4_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv4_pend
6	TPTC_A1_PEND	R/W1TS	0h	Interrupt Pending Status for tptc_a1_pend
5	TPTC_A0_PEND	R/W1TS	0h	Interrupt Pending Status for tptc_a0_pend
4	MSS_MBOX_PEND	R/W1TS	0h	Interrupt Pending Status for mss_mbox_pend
3	MSS_L2SLV3_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv3_pend
2	MSS_L2SLV2_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv2_pend
1	MSS_L2SLV1_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv1_pend
0	MSS_L2SLV0_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv0_pend

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5.20.2.13 ECC_AGGR_SEC_ENABLE_SET_REG0 Register

5.20.2.13.1 ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

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Table 5-2281. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0080h

Figure 5-1114. ECC_AGGR_SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							MSS_L2SLV5_ENABLE_SET
NONE							R/W1TS
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MSS_L2SLV4_ENABLE_SET	TPTC_A1_ENABLE_SETT	TPTC_A0_ENABLE_SET	MSS_MBOX_ENABLE_SET	MSS_L2SLV3_ENABLE_SET	MSS_L2SLV2_ENABLE_SET	MSS_L2SLV1_ENABLE_SET	MSS_L2SLV0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2282. ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MSS_L2SLV5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv5_pend
7	MSS_L2SLV4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv4_pend
6	TPTC_A1_ENABLE_SETT	R/W1TS	0h	Interrupt Enable Set Register for tptc_a1_pend
5	TPTC_A0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv0_pend

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5.20.2.14 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

5.20.2.14.1 ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 5-2283. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 00C0h

Figure 5-1115. ECC_AGGR_SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							MSS_L2SLV5_ENABLE_CLR
NONE							R/W1TC
0h							0h
7	6	5	4	3	2	1	0
MSS_L2SLV4_ENABLE_CLR	TPTC_A1_ENABLE_CLR	TPTC_A0_ENABLE_CLR	MSS_MBOX_ENABLE_CLR	MSS_L2SLV3_ENABLE_CLR	MSS_L2SLV2_ENABLE_CLR	MSS_L2SLV1_ENABLE_CLR	MSS_L2SLV0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2284. ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MSS_L2SLV5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv5_pend
7	MSS_L2SLV4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv4_pend
6	TPTC_A1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tptc_a1_pend
5	TPTC_A0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv0_pend

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5.20.2.15 ECC_AGGR_DED_EOI_REG Register

5.20.2.15.1 ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

Return to Summary Table

Table 5-2285. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 013Ch

Figure 5-1116. ECC_AGGR_DED_EOI_REG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
NONE							R/W1TS
0h							0h

Table 5-2286. ECC_AGGR_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	EOI_WR	R/W1TS	0h	Write of 1 to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. The bit is self clearing and will be read as a zero.

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5.20.2.16 ECC_AGGR_DED_STATUS_REG0 Register

5.20.2.16.1 ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to Summary Table

Table 5-2287. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0140h

Figure 5-1117. ECC_AGGR_DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							MSS_L2SLV5_PEND
NONE							R/W1TS
0h							0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MSS_L2SLV4_PEND	TPTC_A1_PEND	TPTC_A0_PEND	MSS_MBOX_PEND	MSS_L2SLV3_PEND	MSS_L2SLV2_PEND	MSS_L2SLV1_PEND	MSS_L2SLV0_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2288. ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MSS_L2SLV5_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv5_pend
7	MSS_L2SLV4_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv4_pend
6	TPTC_A1_PEND	R/W1TS	0h	Interrupt Pending Status for tptc_a1_pend
5	TPTC_A0_PEND	R/W1TS	0h	Interrupt Pending Status for tptc_a0_pend
4	MSS_MBOX_PEND	R/W1TS	0h	Interrupt Pending Status for mss_mbox_pend
3	MSS_L2SLV3_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv3_pend
2	MSS_L2SLV2_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv2_pend
1	MSS_L2SLV1_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv1_pend
0	MSS_L2SLV0_PEND	R/W1TS	0h	Interrupt Pending Status for mss_l2slv0_pend

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5.20.2.17 ECC_AGGR_DED_ENABLE_SET_REG0 Register

5.20.2.17.1 ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to Summary Table

Table 5-2289. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0180h

Figure 5-1118. ECC_AGGR_DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							MSS_L2SLV5_ENABLE_SET
NONE							R/W1TS
0h							0h
7	6	5	4	3	2	1	0
MSS_L2SLV4_ENABLE_SET	TPTC_A1_ENABLE_SETT	TPTC_A0_ENABLE_SET	MSS_MBOX_ENABLE_SET	MSS_L2SLV3_ENABLE_SET	MSS_L2SLV2_ENABLE_SET	MSS_L2SLV1_ENABLE_SET	MSS_L2SLV0_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2290. ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MSS_L2SLV5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv5_pend
7	MSS_L2SLV4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv4_pend
6	TPTC_A1_ENABLE_SETT	R/W1TS	0h	Interrupt Enable Set Register for tptc_a1_pend
5	TPTC_A0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for mss_l2slv0_pend

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5.20.2.18 ECC_AGGR_DED_ENABLE_CLR_REG0 Register

5.20.2.18.1 ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to Summary Table

Table 5-2291. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 01C0h

Figure 5-1119. ECC_AGGR_DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							MSS_L2SLV5_ENABLE_CLR
NONE							R/W1TC
0h							0h
7	6	5	4	3	2	1	0
MSS_L2SLV4_ENABLE_CLR	TPTC_A1_ENABLE_CLR	TPTC_A0_ENABLE_CLR	MSS_MBOX_ENABLE_CLR	MSS_L2SLV3_ENABLE_CLR	MSS_L2SLV2_ENABLE_CLR	MSS_L2SLV1_ENABLE_CLR	MSS_L2SLV0_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2292. ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	NONE	0h	Reserved
8	MSS_L2SLV5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv5_pend
7	MSS_L2SLV4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv4_pend
6	TPTC_A1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tptc_a1_pend
5	TPTC_A0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for mss_l2slv0_pend

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5.20.2.19 ECC_AGGR_AGGR_ENABLE_SET Register

5.20.2.19.1 ECC_AGGR_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

Enable set register for aggregator interrupts.

Return to Summary Table

Table 5-2293. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0200h

Figure 5-1120. ECC_AGGR_AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TIMEOUT	PARITY
NONE						R/W1TS	R/W1TS
0h						0h	0h

Table 5-2294. ECC_AGGR_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TS	0h	Interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	Interrupt enable set for parity errors

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5.20.2.20 ECC_AGGR_AGGR_ENABLE_CLR Register

5.20.2.20.1 ECC_AGGR_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

Enable clear register for aggregator interrupts.

Return to Summary Table

Table 5-2295. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0204h

Figure 5-1121. ECC_AGGR_AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
NONE						R/W1TC	R/W1TC
0h						0h	0h

Table 5-2296. ECC_AGGR_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	TIMEOUT	R/W1TC	0h	Interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	Interrupt enable clear for parity errors

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5.20.2.21 ECC_AGGR_AGGR_STATUS_SET Register

5.20.2.21.1 ECC_AGGR_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

Status set register for aggregator interrupts.

Return to Summary Table

Table 5-2297. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 0208h

Figure 5-1122. ECC_AGGR_AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WI		R/WI	
0h				0h		0h	

Table 5-2298. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WI	0h	2-bit saturating counter of the number of timeout errors that have occurred since last cleared. 2'b00 - No timeout errors have occurred 2'b01 - 1 timeout error has occurred 2'b10 - 2 timeout error has occurred 2'b11 - 3 or more timeout errors have occurred A write of a non-zero value to this register increments that many from the timeout fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. . If this register goes from 0 ot non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.

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Table 5-2298. ECC_AGGR_AGGR_STATUS_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	PARITY	R/WI	0h	2-bit saturating counter of the number of parity errors that have occurred since last cleared. 2'b00 - No parity errors have occurred 2'b01 - 1 parity error has occurred 2'b10 - 2 parity error has occurred 2'b11 - 3 or more parity error have occurred A write of a non-zero value to this register incrments that many from the parity fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. If this register goes from 0 ot non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.

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5.20.2.22 ECC_AGGR_AGGR_STATUS_CLR Register

5.20.2.22.1 ECC_AGGR_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

Status clear register for aggregator interrupts.

Return to Summary Table

Table 5-2299. Instance Table

Instance Name	Physical Address
ECC_AGGR	5301 020Ch

Figure 5-1123. ECC_AGGR_AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
NONE				R/WD		R/WD	
0h				0h		0h	

Table 5-2300. ECC_AGGR_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED	NONE	0h	Reserved
3:2	TIMEOUT	R/WD	0h	2'b00 - No timeout errors have occurred 2'b01 - 1 timeout error has occurred 2'b10 - 2 timeout error has occurred 2'b11 - 3 or more timeout errors have occurred A write of a non-zero value to this register decrements that many from the timeout fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will nto be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.
1:0	PARITY	R/WD	0h	2'b00 - No parity errors have occurred 2'b01 - 1 parity error has occurred 2'b10 - 2 parity error has occurred 2'b11 - 3 or more parity error have occurred A write of a non-zero value to this register decrements that many from the parity fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will nto be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.

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5.21 RTI

RTI

5.21.1 RTI Summaries

RTI Summaries

Table 5-2301. RTI Registers, Base Address=5218 0000h, Length=256

Offset	Length	Register Name	RTI0 Physical Address	RTI1 Physical Address	RTI2 Physical Address
0h	32	RTI_RTIGCTRL	5218 0000h	5218 1000h	5218 2000h
4h	32	RTI_RTITBCTRL	5218 0004h	5218 1004h	5218 2004h
8h	32	RTI_RTICAPCTRL	5218 0008h	5218 1008h	5218 2008h
Ch	32	RTI_RTICOMPCTRL	5218 000Ch	5218 100Ch	5218 200Ch
10h	32	RTI_RTIFRC0	5218 0010h	5218 1010h	5218 2010h
14h	32	RTI_RTIUC0	5218 0014h	5218 1014h	5218 2014h
18h	32	RTI_RTICPUC0	5218 0018h	5218 1018h	5218 2018h
20h	32	RTI_RTICAFRC0	5218 0020h	5218 1020h	5218 2020h
24h	32	RTI_RTICAUC0	5218 0024h	5218 1024h	5218 2024h
30h	32	RTI_RTIFRC1	5218 0030h	5218 1030h	5218 2030h
34h	32	RTI_RTIUC1	5218 0034h	5218 1034h	5218 2034h
38h	32	RTI_RTICPUC1	5218 0038h	5218 1038h	5218 2038h
40h	32	RTI_RTICAFRC1	5218 0040h	5218 1040h	5218 2040h
44h	32	RTI_RTICAUC1	5218 0044h	5218 1044h	5218 2044h
50h	32	RTI_RTICOMP0	5218 0050h	5218 1050h	5218 2050h
54h	32	RTI_RTIUDCP0	5218 0054h	5218 1054h	5218 2054h
58h	32	RTI_RTICOMP1	5218 0058h	5218 1058h	5218 2058h
5Ch	32	RTI_RTIUDCP1	5218 005Ch	5218 105Ch	5218 205Ch
60h	32	RTI_RTICOMP2	5218 0060h	5218 1060h	5218 2060h
64h	32	RTI_RTIUDCP2	5218 0064h	5218 1064h	5218 2064h
68h	32	RTI_RTICOMP3	5218 0068h	5218 1068h	5218 2068h
6Ch	32	RTI_RTIUDCP3	5218 006Ch	5218 106Ch	5218 206Ch
70h	32	RTI_RTITBLCOMP	5218 0070h	5218 1070h	5218 2070h
74h	32	RTI_RTITBHCOMP	5218 0074h	5218 1074h	5218 2074h
80h	32	RTI_RTISETINT	5218 0080h	5218 1080h	5218 2080h
84h	32	RTI_RTICLEARINT	5218 0084h	5218 1084h	5218 2084h
88h	32	RTI_RTIINTFLAG	5218 0088h	5218 1088h	5218 2088h
90h	32	RTI_RTIDWDCTRL	5218 0090h	5218 1090h	5218 2090h
94h	32	RTI_RTIDWDPRLD	5218 0094h	5218 1094h	5218 2094h
98h	32	RTI_RTIWDSTATUS	5218 0098h	5218 1098h	5218 2098h
9Ch	32	RTI_RTIWDKEY	5218 009Ch	5218 109Ch	5218 209Ch
A0h	32	RTI_RTIDWDCNTR	5218 00A0h	5218 10A0h	5218 20A0h
A4h	32	RTI_RTIWWDRXNCTRL	5218 00A4h	5218 10A4h	5218 20A4h
A8h	32	RTI_RTIWWDSIZECTRL	5218 00A8h	5218 10A8h	5218 20A8h
ACh	32	RTI_RTIINTCLRENABLE	5218 00ACh	5218 10ACh	5218 20ACh
B0h	32	RTI_RTICOMP0CLR	5218 00B0h	5218 10B0h	5218 20B0h
B4h	32	RTI_RTICOMP1CLR	5218 00B4h	5218 10B4h	5218 20B4h
B8h	32	RTI_RTICOMP2CLR	5218 00B8h	5218 10B8h	5218 20B8h
BCh	32	RTI_RTICOMP3CLR	5218 00BCh	5218 10BCh	5218 20BCh

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Table 5-2302. RTI Registers, Base Address=5218 0000h, Length=256

Offset	Length	Register Name	RTI3 Physical Address	RTI4 Physical Address	RTI5 Physical Address
0h	32	RTI_RTIGCTRL	5218 3000h	5218 4000h	5218 5000h
4h	32	RTI_RTITBCTRL	5218 3004h	5218 4004h	5218 5004h
8h	32	RTI_RTICAPCTRL	5218 3008h	5218 4008h	5218 5008h
Ch	32	RTI_RTICOMPCTRL	5218 300Ch	5218 400Ch	5218 500Ch
10h	32	RTI_RTIFRC0	5218 3010h	5218 4010h	5218 5010h
14h	32	RTI_RTIUC0	5218 3014h	5218 4014h	5218 5014h
18h	32	RTI_RTICPUC0	5218 3018h	5218 4018h	5218 5018h
20h	32	RTI_RTICAFRC0	5218 3020h	5218 4020h	5218 5020h
24h	32	RTI_RTICAUC0	5218 3024h	5218 4024h	5218 5024h
30h	32	RTI_RTIFRC1	5218 3030h	5218 4030h	5218 5030h
34h	32	RTI_RTIUC1	5218 3034h	5218 4034h	5218 5034h
38h	32	RTI_RTICPUC1	5218 3038h	5218 4038h	5218 5038h
40h	32	RTI_RTICAFRC1	5218 3040h	5218 4040h	5218 5040h
44h	32	RTI_RTICAUC1	5218 3044h	5218 4044h	5218 5044h
50h	32	RTI_RTICOMP0	5218 3050h	5218 4050h	5218 5050h
54h	32	RTI_RTIUDCP0	5218 3054h	5218 4054h	5218 5054h
58h	32	RTI_RTICOMP1	5218 3058h	5218 4058h	5218 5058h
5Ch	32	RTI_RTIUDCP1	5218 305Ch	5218 405Ch	5218 505Ch
60h	32	RTI_RTICOMP2	5218 3060h	5218 4060h	5218 5060h
64h	32	RTI_RTIUDCP2	5218 3064h	5218 4064h	5218 5064h
68h	32	RTI_RTICOMP3	5218 3068h	5218 4068h	5218 5068h
6Ch	32	RTI_RTIUDCP3	5218 306Ch	5218 406Ch	5218 506Ch
70h	32	RTI_RTITBLCOMP	5218 3070h	5218 4070h	5218 5070h
74h	32	RTI_RTITBHCOMP	5218 3074h	5218 4074h	5218 5074h
80h	32	RTI_RTISETINT	5218 3080h	5218 4080h	5218 5080h
84h	32	RTI_RTICLEARINT	5218 3084h	5218 4084h	5218 5084h
88h	32	RTI_RTIINTFLAG	5218 3088h	5218 4088h	5218 5088h
90h	32	RTI_RTIDWDCTRL	5218 3090h	5218 4090h	5218 5090h
94h	32	RTI_RTIDWDPRLD	5218 3094h	5218 4094h	5218 5094h
98h	32	RTI_RTIWDSTATUS	5218 3098h	5218 4098h	5218 5098h
9Ch	32	RTI_RTIWDKEY	5218 309Ch	5218 409Ch	5218 509Ch
A0h	32	RTI_RTIDWDCNTR	5218 30A0h	5218 40A0h	5218 50A0h
A4h	32	RTI_RTIWWDRXNCTRL	5218 30A4h	5218 40A4h	5218 50A4h
A8h	32	RTI_RTIWWDSIZECTRL	5218 30A8h	5218 40A8h	5218 50A8h
ACh	32	RTI_RTIINTCLRENABLE	5218 30ACh	5218 40ACh	5218 50ACh
B0h	32	RTI_RTICOMP0CLR	5218 30B0h	5218 40B0h	5218 50B0h
B4h	32	RTI_RTICOMP1CLR	5218 30B4h	5218 40B4h	5218 50B4h
B8h	32	RTI_RTICOMP2CLR	5218 30B8h	5218 40B8h	5218 50B8h
BCh	32	RTI_RTICOMP3CLR	5218 30BCh	5218 40BCh	5218 50BCh

Table 5-2303. RTI Registers, Base Address=5218 0000h, Length=256

Offset	Length	Register Name	RTI6 Physical Address	RTI7 Physical Address
0h	32	RTI_RTIGCTRL	5218 6000h	5218 7000h
4h	32	RTI_RTITBCTRL	5218 6004h	5218 7004h
8h	32	RTI_RTICAPCTRL	5218 6008h	5218 7008h

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Table 5-2303. RTI Registers, Base Address=5218 0000h, Length=256 (continued)

Offset	Length	Register Name	RTI6 Physical Address	RTI7 Physical Address
Ch	32	RTI_RTICOMPCTRL	5218 600Ch	5218 700Ch
10h	32	RTI_RTIFRC0	5218 6010h	5218 7010h
14h	32	RTI_RTIUC0	5218 6014h	5218 7014h
18h	32	RTI_RTICPUC0	5218 6018h	5218 7018h
20h	32	RTI_RTICAFRC0	5218 6020h	5218 7020h
24h	32	RTI_RTICAUC0	5218 6024h	5218 7024h
30h	32	RTI_RTIFRC1	5218 6030h	5218 7030h
34h	32	RTI_RTIUC1	5218 6034h	5218 7034h
38h	32	RTI_RTICPUC1	5218 6038h	5218 7038h
40h	32	RTI_RTICAFRC1	5218 6040h	5218 7040h
44h	32	RTI_RTICAUC1	5218 6044h	5218 7044h
50h	32	RTI_RTICOMP0	5218 6050h	5218 7050h
54h	32	RTI_RTIUDCP0	5218 6054h	5218 7054h
58h	32	RTI_RTICOMP1	5218 6058h	5218 7058h
5Ch	32	RTI_RTIUDCP1	5218 605Ch	5218 705Ch
60h	32	RTI_RTICOMP2	5218 6060h	5218 7060h
64h	32	RTI_RTIUDCP2	5218 6064h	5218 7064h
68h	32	RTI_RTICOMP3	5218 6068h	5218 7068h
6Ch	32	RTI_RTIUDCP3	5218 606Ch	5218 706Ch
70h	32	RTI_RTITBLCOMP	5218 6070h	5218 7070h
74h	32	RTI_RTITBHCOMP	5218 6074h	5218 7074h
80h	32	RTI_RTISETINT	5218 6080h	5218 7080h
84h	32	RTI_RTICLEARINT	5218 6084h	5218 7084h
88h	32	RTI_RTIINTFLAG	5218 6088h	5218 7088h
90h	32	RTI_RTIDWDCTRL	5218 6090h	5218 7090h
94h	32	RTI_RTIDWDPRLD	5218 6094h	5218 7094h
98h	32	RTI_RTIWDSTATUS	5218 6098h	5218 7098h
9Ch	32	RTI_RTIWDKEY	5218 609Ch	5218 709Ch
A0h	32	RTI_RTIDWDCNTR	5218 60A0h	5218 70A0h
A4h	32	RTI_RTIWWDRXNCTRL	5218 60A4h	5218 70A4h
A8h	32	RTI_RTIWWDSIZECTRL	5218 60A8h	5218 70A8h
ACh	32	RTI_RTIINTCLRENABLE	5218 60ACh	5218 70ACh
B0h	32	RTI_RTICOMP0CLR	5218 60B0h	5218 70B0h
B4h	32	RTI_RTICOMP1CLR	5218 60B4h	5218 70B4h
B8h	32	RTI_RTICOMP2CLR	5218 60B8h	5218 70B8h
BCh	32	RTI_RTICOMP3CLR	5218 60BCh	5218 70BCh

5.21.2 RTI Registers

RTI Registers

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5.21.2.1 RTI_RTIGCTRL Register

5.21.2.1.1 RTI_RTIGCTRL Register (Offset = 0h) [reset = 0h]

Global Control Register starts / stops the counters .

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Table 5-2304. Instance Table

Instance Name	Physical Address
RTI0	5218 0000h
RTI1	5218 1000h
RTI2	5218 2000h
RTI3	5218 3000h
RTI4	5218 4000h
RTI5	5218 5000h
RTI6	5218 6000h
RTI7	5218 7000h

Figure 5-1124. RTI_RTIGCTRL Name Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="8">RESERVED2</td></tr>
<tr><td colspan="8">R/W</td></tr>
<tr><td colspan="8">0h</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">RESERVED2</td><td colspan="4">NTUSEL</td></tr>
<tr><td colspan="4">R/W</td><td colspan="4">R/W</td></tr>
<tr><td colspan="4">0h</td><td colspan="4">0h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>COS</td><td colspan="7">RESERVED1</td></tr>
<tr><td>R/W</td><td colspan="7">R/W</td></tr>
<tr><td>0h</td><td colspan="7">0h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="6">RESERVED1</td><td>CNT1EN</td><td>CNT0EN</td></tr>
<tr><td colspan="6">R/W</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="6">0h</td><td>0h</td><td>0h</td></tr>
</table>

Table 5-2305. RTI_RTIGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED2	R/W	0h	Reserved. Reads return 0 and writes have no effect

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Table 5-2305. RTI_RTIGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	NTUSEL	R/W	0h	NTUSEL: Select NTU signal. These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL. User and privilege mode [read]: 0000= NTU0 0101= NTU1 1010= NTU2 1111= NTU3 other = tied to 0 Privilege mode [write]: 0000= NTU0 0101= NTU1 1010= NTU2 1111= NTU3 other = tied to 0
15	COS	R/W	0h	COS: Continue On Suspend. This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting. User and privilege mode [read]: 0 = counters are stopped while in debug mode 1 = counters are running while in debug mode Privilege mode [write]: 0 = stop counters in debug mode 1 = continue counting in debug mode
14:2	RESERVED1	R/W	0h	Reserved. Reads return 0 and writes have no effect
1	CNT1EN	R/W	0h	CNT1EN: Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 [UC1 and FRC1]. User and privilege mode [read]: 0 = counters are stopped 1 = counters are running Privilege mode [write]: 0 = stop counters 1 = start counters Gives the absolute 32 bit destination address [physical].
0	CNT0EN	R/W	0h	CNT0EN: Counter 0 Enable.The CNT0EN bit starts and stops the operation of counter block 0 [UC0 and FRC0]. User and privilege mode [read]: 0 = counters are stopped 1 = counters are running Privilege mode [write]: 0 = stop counters 1 = start counters Gives the absolute 32 bits source address [physical].

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5.21.2.2 RTI_RTITBCTRL Register

5.21.2.2.1 RTI_RTITBCTRL Register (Offset = 4h) [reset = 0h]

Timebase Control selection which source triggers free running counter 0 .

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Table 5-2306. Instance Table

Instance Name	Physical Address
RTI0	5218 0004h
RTI1	5218 1004h
RTI2	5218 2004h
RTI3	5218 3004h
RTI4	5218 4004h
RTI5	5218 5004h
RTI6	5218 6004h
RTI7	5218 7004h

Figure 5-1125. RTI_RTITBCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED3							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED3							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED3						INC	TBEXT
R/W						R/W	R/W
0h						0h	0h

Table 5-2307. RTI_RTITBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED3	R/W	0h	Reserved
1	INC	R/W	0h	INC: Increment Free Running Counter 0. This bit determines wether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected. User and privilege mode [read]: 0 = FRC0 will not be incremented 1 = FRC0 will be incremented Privilege mode [write]: 0 = Do not increment FRC0 on failing external clock 1 = Increment FRC0 on failing external clock

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Table 5-2307. RTI_RTITBCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TBEXT	R/W	0h	TBEXT: Timebase External. The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurence. The only source which is able to increment Free Running Counter 0 is NTUx. When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset. The selection if the external signal should be used, can only be done by software. User and privilege mode [read]: 0 = UC0 clocks FRC0 1 = NTUx clocks FRC0 Privilege mode [write]: 0 = MUX is switched to internal UC0 clocking scheme 1 = MUX is switched to external NTUx clocking scheme

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5.21.2.3 RTI_RTICAPCTRL Register

5.21.2.3.1 RTI_RTICAPCTRL Register (Offset = 8h) [reset = 0h]

Capture Control controls the capture source for the counters.

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Table 5-2308. Instance Table

Instance Name	Physical Address
RTI0	5218 0008h
RTI1	5218 1008h
RTI2	5218 2008h
RTI3	5218 3008h
RTI4	5218 4008h
RTI5	5218 5008h
RTI6	5218 6008h
RTI7	5218 7008h

Figure 5-1126. RTI_RTICAPCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED4						CAPCNTR1	CAPCNTR0
R/W						R/W	R/W
0h						0h	0h

Table 5-2309. RTI_RTICAPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED4	R/W	0h	Reserved. Reads return 0 and writes have no effect
1	CAPCNTR1	R/W	0h	CAPCNTR1: Capture Counter 1. This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1. User and privilege mode [read]: 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode [write]: 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1

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Table 5-2309. RTI_RTICAPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CAPCNTR0	R/W	0h	CAPCNTR0: Capture Counter 0. This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0. User and privilege mode [read]: 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode [write]: 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1 11 indexed 10 reserved 01 post-increment 00 constant

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5.21.2.4 RTI_RTICOMPCTRL Register

5.21.2.4.1 RTI_RTICOMPCTRL Register (Offset = Ch) [reset = 0h]

Compare Control controls the source for the compare registers.

Return to Summary Table

Table 5-2310. Instance Table

Instance Name	Physical Address
RTI0	5218 000Ch
RTI1	5218 100Ch
RTI2	5218 200Ch
RTI3	5218 300Ch
RTI4	5218 400Ch
RTI5	5218 500Ch
RTI6	5218 600Ch
RTI7	5218 700Ch

Figure 5-1127. RTI_RTICOMPCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED8			COMP3SEL	RESERVED7			COMP2SEL
R/W			R/W	R/W			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED6			COMP1SEL	RESERVED5			COMP0SEL
R/W			R/W	R/W			R/W
0h			0h	0h			0h

Table 5-2311. RTI_RTICOMPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED8	R/W	0h	Reserved. Reads return 0 and writes have no effect
12	COMP3SEL	R/W	0h	COMPSEL3: Compare Select 3. This bit determines the counter with which the compare value hold in compare register 3 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
11:9	RESERVED7	R/W	0h	Reserved. Reads return 0 and writes have no effect

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Table 5-2311. RTI_RTICOMPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	COMP2SEL	R/W	0h	COMPSEL2: Compare Select 2. This bit determines the counter with which the compare value hold in compare register 2 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
7:5	RESERVED6	R/W	0h	Reserved. Reads return 0 and writes have no effect
4	COMP1SEL	R/W	0h	COMPSEL1: Compare Select 1. This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
3:1	RESERVED5	R/W	0h	Reserved. Reads return 0 and writes have no effect
0	COMP0SEL	R/W	0h	COMPSEL0: Compare Select 0. This bit determines the counter with which the compare value hold in compare register 0 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1

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5.21.2.5 RTI_RTIFRC0 Register

5.21.2.5.1 RTI_RTIFRC0 Register (Offset = 10h) [reset = 0h]

Free Running Counter 0 current value of free running counter 0

Return to Summary Table

Table 5-2312. Instance Table

Instance Name	Physical Address
RTI0	5218 0010h
RTI1	5218 1010h
RTI2	5218 2010h
RTI3	5218 3010h
RTI4	5218 4010h
RTI5	5218 5010h
RTI6	5218 6010h
RTI7	5218 7010h

Figure 5-1128. RTI_RTIFRC0 Name Register

31	30	29	28	27	26	25	24
FRC0							
R/W							
0h							
23	22	21	20	19	18	17	16
FRC0							
R/W							
0h							
15	14	13	12	11	10	9	8
FRC0							
R/W							
0h							
7	6	5	4	3	2	1	0
FRC0							
R/W							
0h							

Table 5-2313. RTI_RTIFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC0	R/W	0h	FRC0: Free Running Counter 0. This registers holds the current value of the Free Running Counter 0 and will be updated continuously. User and privilege mode [read]: current value of the counter Privilege mode [write]: The counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.

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5.21.2.6 RTI_RTIUC0 Register

5.21.2.6.1 RTI_RTIUC0 Register (Offset = 14h) [reset = 0h]

Up Counter 0 current value of prescale counter 0

Return to Summary Table

Table 5-2314. Instance Table

Instance Name	Physical Address
RTI0	5218 0014h
RTI1	5218 1014h
RTI2	5218 2014h
RTI3	5218 3014h
RTI4	5218 4014h
RTI5	5218 5014h
RTI6	5218 6014h
RTI7	5218 7014h

Figure 5-1129. RTI_RTIUC0 Name Register

31	30	29	28	27	26	25	24
UC0							
R/W							
0h							
23	22	21	20	19	18	17	16
UC0							
R/W							
0h							
15	14	13	12	11	10	9	8
UC0							
R/W							
0h							
7	6	5	4	3	2	1	0
UC0							
R/W							
0h							

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Table 5-2315. RTI_RTIUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC0	R/W	0h	UC0: Up Counter 0. This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0. User and privilege mode [read]: value of the counter when the Free Running Counter 0 was read Privilege mode [write]: the counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.

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5.21.2.7 RTI_RTICPUC0 Register

5.21.2.7.1 RTI_RTICPUC0 Register (Offset = 18h) [reset = 0h]

Compare Up Counter 0 compare value compared with prescale counter 0

Return to Summary Table

Table 5-2316. Instance Table

Instance Name	Physical Address
RTI0	5218 0018h
RTI1	5218 1018h
RTI2	5218 2018h
RTI3	5218 3018h
RTI4	5218 4018h
RTI5	5218 5018h
RTI6	5218 6018h
RTI7	5218 7018h

Figure 5-1130. RTI_RTICPUC0 Name Register

31	30	29	28	27	26	25	24
CPUC0							
R/W							
0h							
23	22	21	20	19	18	17	16
CPUC0							
R/W							
0h							
15	14	13	12	11	10	9	8
CPUC0							
R/W							
0h							
7	6	5	4	3	2	1	0
CPUC0							
R/W							
0h							

Table 5-2317. RTI_RTICPUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC0	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock. If CPUC0 = 0:then, frequency = RTICLK/ [2^32] If CPUC0 0:then , frequency = RTICLK/[CPUC0 + 1] User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed

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5.21.2.8 RTI_RTICAFRC0 Register

5.21.2.8.1 RTI_RTICAFRC0 Register (Offset = 20h) [reset = 0h]

Capture Free Running Counter 0 current value of free running counter 0 on external event.

Return to Summary Table

Table 5-2318. Instance Table

Instance Name	Physical Address
RTI0	5218 0020h
RTI1	5218 1020h
RTI2	5218 2020h
RTI3	5218 3020h
RTI4	5218 4020h
RTI5	5218 5020h
RTI6	5218 6020h
RTI7	5218 7020h

Figure 5-1131. RTI_RTICAFRC0 Name Register

31	30	29	28	27	26	25	24
CAFRC0							
R/W							
0h							
23	22	21	20	19	18	17	16
CAFRC0							
R/W							
0h							
15	14	13	12	11	10	9	8
CAFRC0							
R/W							
0h							
7	6	5	4	3	2	1	0
CAFRC0							
R/W							
0h							

Table 5-2319. RTI_RTICAFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC0	R/W	0h	CAFRC0: Capture Free Running Counter 0. This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block. User and privilege mode [read]: value of Free Running Counter 0 on a capture event

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5.21.2.9 RTI_RTICAUC0 Register

5.21.2.9.1 RTI_RTICAUC0 Register (Offset = 24h) [reset = 0h]

Capture Up Counter 0 current value of prescale counter 0 on external event.

Return to Summary Table

Table 5-2320. Instance Table

Instance Name	Physical Address
RTI0	5218 0024h
RTI1	5218 1024h
RTI2	5218 2024h
RTI3	5218 3024h
RTI4	5218 4024h
RTI5	5218 5024h
RTI6	5218 6024h
RTI7	5218 7024h

Figure 5-1132. RTI_RTICAUC0 Name Register

31	30	29	28	27	26	25	24
CAUC0							
R/W							
0h							
23	22	21	20	19	18	17	16
CAUC0							
R/W							
0h							
15	14	13	12	11	10	9	8
CAUC0							
R/W							
0h							
7	6	5	4	3	2	1	0
CAUC0							
R/W							
0h							

Table 5-2321. RTI_RTICAUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC0	R/W	0h	CAUC0: Capture Up Counter 0. This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode [read]: value of Up Counter 0 on a capture event

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5.21.2.10 RTI_RTIFRC1 Register

5.21.2.10.1 RTI_RTIFRC1 Register (Offset = 30h) [reset = 0h]

Free Running Counter 1 current value of free running counter 1

Return to Summary Table

Table 5-2322. Instance Table

Instance Name	Physical Address
RTI0	5218 0030h
RTI1	5218 1030h
RTI2	5218 2030h
RTI3	5218 3030h
RTI4	5218 4030h
RTI5	5218 5030h
RTI6	5218 6030h
RTI7	5218 7030h

Figure 5-1133. RTI_RTIFRC1 Name Register

31	30	29	28	27	26	25	24
FRC1							
R/W							
0h							
23	22	21	20	19	18	17	16
FRC1							
R/W							
0h							
15	14	13	12	11	10	9	8
FRC1							
R/W							
0h							
7	6	5	4	3	2	1	0
FRC1							
R/W							
0h							

Table 5-2323. RTI_RTIFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC1	R/W	0h	FRC1: Free Running Counter 1. This registers holds the current value of the Free Running Counter 1 and will be updated continuously. User and privilege mode [read]: current value of the counter Privilege mode [write]: The counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.

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5.21.2.11 RTI_RTIUC1 Register

5.21.2.11.1 RTI_RTIUC1 Register (Offset = 34h) [reset = 0h]

Up Counter 1 current value of prescale counter 1

Return to Summary Table

Table 5-2324. Instance Table

Instance Name	Physical Address
RTI0	5218 0034h
RTI1	5218 1034h
RTI2	5218 2034h
RTI3	5218 3034h
RTI4	5218 4034h
RTI5	5218 5034h
RTI6	5218 6034h
RTI7	5218 7034h

Figure 5-1134. RTI_RTIUC1 Name Register

31	30	29	28	27	26	25	24
UC1							
R/W							
0h							
23	22	21	20	19	18	17	16
UC1							
R/W							
0h							
15	14	13	12	11	10	9	8
UC1							
R/W							
0h							
7	6	5	4	3	2	1	0
UC1							
R/W							
0h							

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Table 5-2325. RTI_RTIUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC1	R/W	0h	UC1: Up Counter 1. This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1. User and privilege mode [read]: value of the counter when the Free Running Counter 1 was read Privilege mode [write]: the counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since RTIUC1 has to count up until it overflows.

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5.21.2.12 RTI_RTICPUC1 Register

5.21.2.12.1 RTI_RTICPUC1 Register (Offset = 38h) [reset = 0h]

Compare Up Counter 1 compare value compared with prescale counter 1

Return to Summary Table

Table 5-2326. Instance Table

Instance Name	Physical Address
RTI0	5218 0038h
RTI1	5218 1038h
RTI2	5218 2038h
RTI3	5218 3038h
RTI4	5218 4038h
RTI5	5218 5038h
RTI6	5218 6038h
RTI7	5218 7038h

Figure 5-1135. RTI_RTICPUC1 Name Register

31	30	29	28	27	26	25	24
CPUC1							
R/W							
0h							
23	22	21	20	19	18	17	16
CPUC1							
R/W							
0h							
15	14	13	12	11	10	9	8
CPUC1							
R/W							
0h							
7	6	5	4	3	2	1	0
CPUC1							
R/W							
0h							

Table 5-2327. RTI_RTICPUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC1	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock. If CPUC1 = 0:then, frequency = RTICLK/ [2^32] If CPUC1 0:then , frequency = RTICLK/[CPUC1 + 1] User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed

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5.21.2.13 RTI_RTICAFRC1 Register

5.21.2.13.1 RTI_RTICAFRC1 Register (Offset = 40h) [reset = 0h]

Capture Free Running Counter 1 current value of free running counter 1 on external event.

Return to Summary Table

Table 5-2328. Instance Table

Instance Name	Physical Address
RTI0	5218 0040h
RTI1	5218 1040h
RTI2	5218 2040h
RTI3	5218 3040h
RTI4	5218 4040h
RTI5	5218 5040h
RTI6	5218 6040h
RTI7	5218 7040h

Figure 5-1136. RTI_RTICAFRC1 Name Register

31	30	29	28	27	26	25	24
CAFRC1							
R/W							
0h							
23	22	21	20	19	18	17	16
CAFRC1							
R/W							
0h							
15	14	13	12	11	10	9	8
CAFRC1							
R/W							
0h							
7	6	5	4	3	2	1	0
CAFRC1							
R/W							
0h							

Table 5-2329. RTI_RTICAFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC1	R/W	0h	CAFRC1: Capture Free Running Counter 1. This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block. User and privilege mode [read]: value of Free Running Counter 1 on a capture event

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5.21.2.14 RTI_RTICAUC1 Register

5.21.2.14.1 RTI_RTICAUC1 Register (Offset = 44h) [reset = 0h]

Capture Up Counter 1 current value of prescale counter 1 on external event.

Return to Summary Table

Table 5-2330. Instance Table

Instance Name	Physical Address
RTI0	5218 0044h
RTI1	5218 1044h
RTI2	5218 2044h
RTI3	5218 3044h
RTI4	5218 4044h
RTI5	5218 5044h
RTI6	5218 6044h
RTI7	5218 7044h

Figure 5-1137. RTI_RTICAUC1 Name Register

31	30	29	28	27	26	25	24
CAUC1							
R/W							
0h							
23	22	21	20	19	18	17	16
CAUC1							
R/W							
0h							
15	14	13	12	11	10	9	8
CAUC1							
R/W							
0h							
7	6	5	4	3	2	1	0
CAUC1							
R/W							
0h							

Table 5-2331. RTI_RTICAUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC1	R/W	0h	CAUC1: Capture Up Counter 1. This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC1 register is the corresponding value to the RTICAFRC1 register, even if another capture event happens in between the two reads. User and privilege mode [read]: value of Up Counter 1 on a capture event

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5.21.2.15 RTI_RTICOMP0 Register

5.21.2.15.1 RTI_RTICOMP0 Register (Offset = 50h) [reset = 0h]

Compare 0 compare value to be compared with the counters.

Return to Summary Table

Table 5-2332. Instance Table

Instance Name	Physical Address
RTI0	5218 0050h
RTI1	5218 1050h
RTI2	5218 2050h
RTI3	5218 3050h
RTI4	5218 4050h
RTI5	5218 5050h
RTI6	5218 6050h
RTI7	5218 7050h

Figure 5-1138. RTI_RTICOMP0 Name Register

31	30	29	28	27	26	25	24
COMP0							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP0							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP0							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP0							
R/W							
0h							

Table 5-2333. RTI_RTICOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0	R/W	0h	COMP0: Compare 0. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.21.2.16 RTI_RTIUDCP0 Register

5.21.2.16.1 RTI_RTIUDCP0 Register (Offset = 54h) [reset = 0h]

Update Compare 0 value to be added to the compare register 0 value on compare match.

Return to Summary Table

Table 5-2334. Instance Table

Instance Name	Physical Address
RTI0	5218 0054h
RTI1	5218 1054h
RTI2	5218 2054h
RTI3	5218 3054h
RTI4	5218 4054h
RTI5	5218 5054h
RTI6	5218 6054h
RTI7	5218 7054h

Figure 5-1139. RTI_RTIUDCP0 Name Register

31	30	29	28	27	26	25	24
UDCP0							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP0							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP0							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP0							
R/W							
0h							

Table 5-2335. RTI_RTIUDCP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP0	R/W	0h	UDCP0: Update Compare 0 Register. This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 0 register on the next compare match Privilege mode [write]: new update value

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5.21.2.17 RTI_RTICOMP1 Register

5.21.2.17.1 RTI_RTICOMP1 Register (Offset = 58h) [reset = 0h]

Compare 1 compare value to be compared with the counters.

Return to Summary Table

Table 5-2336. Instance Table

Instance Name	Physical Address
RTI0	5218 0058h
RTI1	5218 1058h
RTI2	5218 2058h
RTI3	5218 3058h
RTI4	5218 4058h
RTI5	5218 5058h
RTI6	5218 6058h
RTI7	5218 7058h

Figure 5-1140. RTI_RTICOMP1 Name Register

31	30	29	28	27	26	25	24
COMP1							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP1							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP1							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP1							
R/W							
0h							

Table 5-2337. RTI_RTICOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1	R/W	0h	COMP1: compare1. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.21.2.18 RTI_RTIUDCP1 Register

5.21.2.18.1 RTI_RTIUDCP1 Register (Offset = 5Ch) [reset = 0h]

Update Compare 1 value to be added to the compare register 1 value on compare match.

Return to Summary Table

Table 5-2338. Instance Table

Instance Name	Physical Address
RTI0	5218 005Ch
RTI1	5218 105Ch
RTI2	5218 205Ch
RTI3	5218 305Ch
RTI4	5218 405Ch
RTI5	5218 505Ch
RTI6	5218 605Ch
RTI7	5218 705Ch

Figure 5-1141. RTI_RTIUDCP1 Name Register

31	30	29	28	27	26	25	24
UDCP1							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP1							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP1							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP1							
R/W							
0h							

Table 5-2339. RTI_RTIUDCP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP1	R/W	0h	UDCP1: Update compare1 Register. This registers holds a value, which is added to the value in the compare1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare1 register on the next compare match Privilege mode [write]: new update value

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5.21.2.19 RTI_RTICOMP2 Register

5.21.2.19.1 RTI_RTICOMP2 Register (Offset = 60h) [reset = 0h]

Compare 2 compare value to be compared with the counters.

Return to Summary Table

Table 5-2340. Instance Table

Instance Name	Physical Address
RTI0	5218 0060h
RTI1	5218 1060h
RTI2	5218 2060h
RTI3	5218 3060h
RTI4	5218 4060h
RTI5	5218 5060h
RTI6	5218 6060h
RTI7	5218 7060h

Figure 5-1142. RTI_RTICOMP2 Name Register

31	30	29	28	27	26	25	24
COMP2							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP2							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP2							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP2							
R/W							
0h							

Table 5-2341. RTI_RTICOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2	R/W	0h	COMP2: compare 2. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.21.2.20 RTI_RTIUDCP2 Register

5.21.2.20.1 RTI_RTIUDCP2 Register (Offset = 64h) [reset = 0h]

Update Compare 2 value to be added to the compare register 2 value on compare match.

Return to Summary Table

Table 5-2342. Instance Table

Instance Name	Physical Address
RTI0	5218 0064h
RTI1	5218 1064h
RTI2	5218 2064h
RTI3	5218 3064h
RTI4	5218 4064h
RTI5	5218 5064h
RTI6	5218 6064h
RTI7	5218 7064h

Figure 5-1143. RTI_RTIUDCP2 Name Register

31	30	29	28	27	26	25	24
UDCP2							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP2							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP2							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP2							
R/W							
0h							

Table 5-2343. RTI_RTIUDCP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP2	R/W	0h	UDCP2: Update compare 2 Register. This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 2 register on the next compare match Privilege mode [write]: new update value

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5.21.2.21 RTI_RTICOMP3 Register

5.21.2.21.1 RTI_RTICOMP3 Register (Offset = 68h) [reset = 0h]

Compare 3 compare value to be compared with the counters.

Return to Summary Table

Table 5-2344. Instance Table

Instance Name	Physical Address
RTI0	5218 0068h
RTI1	5218 1068h
RTI2	5218 2068h
RTI3	5218 3068h
RTI4	5218 4068h
RTI5	5218 5068h
RTI6	5218 6068h
RTI7	5218 7068h

Figure 5-1144. RTI_RTICOMP3 Name Register

31	30	29	28	27	26	25	24
COMP3							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP3							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP3							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP3							
R/W							
0h							

Table 5-2345. RTI_RTICOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3	R/W	0h	COMP3: compare 3. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.21.2.22 RTI_RTIUDCP3 Register

5.21.2.22.1 RTI_RTIUDCP3 Register (Offset = 6Ch) [reset = 0h]

Update Compare 3 value to be added to the compare register 3 value on compare match.

Return to Summary Table

Table 5-2346. Instance Table

Instance Name	Physical Address
RTI0	5218 006Ch
RTI1	5218 106Ch
RTI2	5218 206Ch
RTI3	5218 306Ch
RTI4	5218 406Ch
RTI5	5218 506Ch
RTI6	5218 606Ch
RTI7	5218 706Ch

Figure 5-1145. RTI_RTIUDCP3 Name Register

31	30	29	28	27	26	25	24
UDCP3							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP3							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP3							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP3							
R/W							
0h							

Table 5-2347. RTI_RTIUDCP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP3	R/W	0h	UDCP3: Update compare 3 Register. This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 3 register on the next compare match Privilege mode [write]: new update value

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5.21.2.23 RTI_RTITBLCOMP Register

5.21.2.23.1 RTI_RTITBLCOMP Register (Offset = 70h) [reset = 0h]

Timebase Low Compare compare value to activate edge detection circuit.

Return to Summary Table

Table 5-2348. Instance Table

Instance Name	Physical Address
RTI0	5218 0070h
RTI1	5218 1070h
RTI2	5218 2070h
RTI3	5218 3070h
RTI4	5218 4070h
RTI5	5218 5070h
RTI6	5218 6070h
RTI7	5218 7070h

Figure 5-1146. RTI_RTITBLCOMP Name Register

31	30	29	28	27	26	25	24
TBLCOMP							
R/W							
0h							
23	22	21	20	19	18	17	16
TBLCOMP							
R/W							
0h							
15	14	13	12	11	10	9	8
TBLCOMP							
R/W							
0h							
7	6	5	4	3	2	1	0
TBLCOMP							
R/W							
0h							

Table 5-2349. RTI_RTITBLCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBLCOMP	R/W	0h	TBLCOMP: Timebase Low Compare Value. This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0. User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed Note: Reset behavior A reset does not generate a compare match.

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5.21.2.24 RTI_RTITBHCOMP Register

5.21.2.24.1 RTI_RTITBHCOMP Register (Offset = 74h) [reset = 0h]

Timebase High Compare compare value to deactivate edge detection circuit.

Return to Summary Table

Table 5-2350. Instance Table

Instance Name	Physical Address
RTI0	5218 0074h
RTI1	5218 1074h
RTI2	5218 2074h
RTI3	5218 3074h
RTI4	5218 4074h
RTI5	5218 5074h
RTI6	5218 6074h
RTI7	5218 7074h

Figure 5-1147. RTI_RTITBHCOMP Name Register

31	30	29	28	27	26	25	24
TBHCOMP							
R/W							
0h							
23	22	21	20	19	18	17	16
TBHCOMP							
R/W							
0h							
15	14	13	12	11	10	9	8
TBHCOMP							
R/W							
0h							
7	6	5	4	3	2	1	0
TBHCOMP							
R/W							
0h							

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Table 5-2351. RTI_RTITBHCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBHCOMP	R/W	0h	TBHCOMP: Timebase High Compare Value. This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0. RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached. Example: The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0. RTICPUC0 = 0x00000050 RTITBLCOMP = 0x000046 RTITBHCOMP = 0x00000009 User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed Note: Reset behavior A reset does not generate a compare match.

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5.21.2.25 RTI_RTISETINT Register

5.21.2.25.1 RTI_RTISETINT Register (Offset = 80h) [reset = 0h]

Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.

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Table 5-2352. Instance Table

Instance Name	Physical Address
RTI0	5218 0080h
RTI1	5218 1080h
RTI2	5218 2080h
RTI3	5218 3080h
RTI4	5218 4080h
RTI5	5218 5080h
RTI6	5218 6080h
RTI7	5218 7080h

Figure 5-1148. RTI_RTISETINT Name Register

31	30	29	28	27	26	25	24
RESERVED11							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED11					SETOVL1INT	SETOVL0INT	SETTBINT
R/W					R/W	R/W	R/W
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED10				SETDMA3	SETDMA2	SETDMA1	SETDMA0
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED9				SETINT3	SETINT2	SETINT1	SETINT0
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 5-2353. RTI_RTISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED11	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	SETOVL1INT	R/W	0h	SETOVL1INT: Set Free Running Counter 1 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
17	SETOVL0INT	R/W	0h	SETOVL0INT: Set Free Running Counter 0 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt

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Table 5-2353. RTI_RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SETTBINT	R/W	0h	SETTBINT: Set Timebase Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
15:12	RESERVED10	R/W	0h	Reserved. Reads return 0 and writes have no effect
11	SETDMA3	R/W	0h	SETDMA3: Set Compare DMA Request 3. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
10	SETDMA2	R/W	0h	SETDMA2: Set Compare DMA Request 2. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
9	SETDMA1	R/W	0h	SETDMA1: Set Compare DMA Request 1. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
8	SETDMA0	R/W	0h	SETDMA0: Set Compare DMA Request 0. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
7:4	RESERVED9	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	SETINT3	R/W	0h	SETINT3: Set Compare Interrupt 3. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged
2	SETINT2	R/W	0h	SETINT2: Set Compare Interrupt 2. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
1	SETINT1	R/W	0h	SETINT1: Set Compare Interrupt 1. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt

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Table 5-2353. RTI_RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SETINT0	R/W	0h	SETINT0: Set Compare Interrupt 0. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt

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5.21.2.26 RTI_RTICLEARINT Register

5.21.2.26.1 RTI_RTICLEARINT Register (Offset = 84h) [reset = 0h]

Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.

Return to Summary Table

Table 5-2354. Instance Table

Instance Name	Physical Address
RTI0	5218 0084h
RTI1	5218 1084h
RTI2	5218 2084h
RTI3	5218 3084h
RTI4	5218 4084h
RTI5	5218 5084h
RTI6	5218 6084h
RTI7	5218 7084h

Figure 5-1149. RTI_RTICLEARINT Name Register

31	30	29	28	27	26	25	24
RESERVED14							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED14					CLEAROVL1INT	CLEAROVL0INT	CLEARTBINT
R/W					R/W	R/W	R/W
0h					0h	0h	0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED13				CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED12				CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 5-2355. RTI_RTICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED14	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	CLEAROVL1INT	R/W	0h	CLEAROVL1INT: CLEAR Free Running Counter 1 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt

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Table 5-2355. RTI_RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	CLEAROVL0INT	R/W	0h	CLEAROVL0INT: CLEAR Free Running Counter 0 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
16	CLEARTBINT	R/W	0h	CLEARTBINT: CLEAR Timebase Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
15:12	RESERVED13	R/W	0h	Reserved. Reads return 0 and writes have no effect
11	CLEARDMA3	R/W	0h	CLEARDMA3: CLEAR Compare DMA Request 3. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
10	CLEARDMA2	R/W	0h	CLEARDMA2: CLEAR Compare DMA Request 2. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
9	CLEARDMA1	R/W	0h	CLEARDMA1: CLEAR Compare DMA Request 1. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
8	CLEARDMA0	R/W	0h	CLEARDMA0: CLEAR Compare DMA Request 0. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
7:4	RESERVED12	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	CLEARINT3	R/W	0h	CLEARINT3: CLEAR Compare Interrupt 3. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
2	CLEARINT2	R/W	0h	CLEARINT2: CLEAR Compare Interrupt 2. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt

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Table 5-2355. RTI_RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLEARINT1	R/W	0h	CLEARINT1: CLEAR Compare Interrupt 1. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
0	CLEARINT0	R/W	0h	CLEARINT0: CLEAR Compare Interrupt 0. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt

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5.21.2.27 RTI_RTIINTFLAG Register

5.21.2.27.1 RTI_RTIINTFLAG Register (Offset = 88h) [reset = 0h]

Interrupt Flags interrupt pending bits.

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Table 5-2356. Instance Table

Instance Name	Physical Address
RTI0	5218 0088h
RTI1	5218 1088h
RTI2	5218 2088h
RTI3	5218 3088h
RTI4	5218 4088h
RTI5	5218 5088h
RTI6	5218 6088h
RTI7	5218 7088h

Figure 5-1150. RTI_RTIINTFLAG Name Register

31	30	29	28	27	26	25	24
RESERVED16							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED16					OVL1INT	OVL0INT	TBINT
R/W					R/W	R/W	R/W
0h					0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED15							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED15				INT3	INT2	INT1	INT0
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 5-2357. RTI_RTIINTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED16	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	OVL1INT	R/W	0h	OVL1INT: Free Running Counter 1 Overflow Interrupt Flag. User and privilege mode [read]: determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0

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Table 5-2357. RTI_RTIINTFLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	OVL0INT	R/W	0h	OVL0INT: Free Running Counter 0 Overflow Interrupt Flag. User and privilege mode [read]: determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
16	TBINT	R/W	0h	User and privilege mode [read]: this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software. determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
15:4	RESERVED15	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	INT3	R/W	0h	INT3: Interrupt Flag 3. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
2	INT2	R/W	0h	INT2: Interrupt Flag 2. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
1	INT1	R/W	0h	INT1: Interrupt Flag 1. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
0	INT0	R/W	0h	INT0: Interrupt Flag 0. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0

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5.21.2.28 RTI_RTIDWDCTRL Register

5.21.2.28.1 RTI_RTIDWDCTRL Register (Offset = 90h) [reset = 0h]

Digital Watchdog Control Enables the Digital Watchdog.

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Table 5-2358. Instance Table

Instance Name	Physical Address
RTI0	5218 0090h
RTI1	5218 1090h
RTI2	5218 2090h
RTI3	5218 3090h
RTI4	5218 4090h
RTI5	5218 5090h
RTI6	5218 6090h
RTI7	5218 7090h

Figure 5-1151. RTI_RTIDWDCTRL Name Register

31	30	29	28	27	26	25	24
DWDCTRL							
R/W							
0h							
23	22	21	20	19	18	17	16
DWDCTRL							
R/W							
0h							
15	14	13	12	11	10	9	8
DWDCTRL							
R/W							
0h							
7	6	5	4	3	2	1	0
DWDCTRL							
R/W							
0h							

Table 5-2359. RTI_RTIDWDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DWDCTRL	R/W	0h	DWDCTRL: Digital Watchdog Control. User and priviledge mode [read]: 0x5312ACED = DWD counter is disabled. This is the default value. 0xA98559DA = DWD counter is enabled Any other value = DWD counter state is unchanged [enabled or disabled] Priviledge mode [write]: 0xA98559DA = DWD counter is enabled Any other value = State of DWD counter is unchanged [stays enabled or disabled] Note: One-Write Functionality of DWDCTRL Register The RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this registermore than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again.

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5.21.2.29 RTI_RTIDWDPRLD Register

5.21.2.29.1 RTI_RTIDWDPRLD Register (Offset = 94h) [reset = 0h]

Digital Watchdog Preload sets the experation time of the Digital Watchdog.

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Table 5-2360. Instance Table

Instance Name	Physical Address
RTI0	5218 0094h
RTI1	5218 1094h
RTI2	5218 2094h
RTI3	5218 3094h
RTI4	5218 4094h
RTI5	5218 5094h
RTI6	5218 6094h
RTI7	5218 7094h

Figure 5-1152. RTI_RTIDWDPRLD Name Register

31	30	29	28	27	26	25	24
RESERVED17							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED17							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED17				DWDPRLD			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DWDPRLD							
R/W							
0h							

Table 5-2361. RTI_RTIDWDPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED17	R/W	0h	Reserved. Reads return 0 and writes have no effect
11:0	DWDPRLD	R/W	0h	DWDPRLD: Digital Watchdog Preload Value. User and priviledge mode [read]: A read from this register in any CPU mode returns the current preload value. Priviledge mode [write]: The DWD preload register can be configured only when the DWD is disabled.Therefore, the application can only configure the DWD preload register before it enables the DWD down counter. The expiration time of the DWD Down Counter can be determined with following equation: texp = [RTIDWDPRLD+1] x 2 ^ 13 / RTICLK1 where: RTIDWDPRLD = 0...4095

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5.21.2.30 RTI_RTIWDSTATUS Register

5.21.2.30.1 RTI_RTIWDSTATUS Register (Offset = 98h) [reset = 0h]

Watchdog Status reflects the status of Analog and Digital Watchdog.

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Table 5-2362. Instance Table

Instance Name	Physical Address
RTI0	5218 0098h
RTI1	5218 1098h
RTI2	5218 2098h
RTI3	5218 3098h
RTI4	5218 4098h
RTI5	5218 5098h
RTI6	5218 6098h
RTI7	5218 7098h

Figure 5-1153. RTI_RTIWDSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED18							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED18							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED18							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED18		DWWD_ST	ENDTIMEVIOL	STARTTIMEVIOL	KEYST	DWDST	AWDST
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 5-2363. RTI_RTIWDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED18	R/W	0h	Reserved. Reads return 0 and writes have no effect
5	DWWD_ST	R/W	0h	DWWD ST: Windowed Watchdog Status. This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog. User and priviledge mode [read]: 0 = no time-window violation has occurred. 1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS register except for the AWD ST flag. Clearing of the status flags will deassert the non-maskable interrupt generated due to violation of the DWWD.

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Table 5-2363. RTI_RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ENDTIMEVIOL	R/W	0h	END TIME VIOL: Windowed Watchdog End Time Violation Status. This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag. User and priviledge mode [read]: 0 = no end-time window violation has occurred. 1 = the end-time defined by the windowed watchdog configuration has been violated. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0.
3	STARTTIMEVIOL	R/W	0h	START TIME VIOL: Windowed Watchdog Start Time Violation Status. This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened. User and priviledge mode [read]: 0 = no start-time window violation has occurred. 1 = the start-time defined by the windowed watchdog configuration has been violated. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0.
2	KEYST	R/W	0h	KEYST: Watchdog KeyStatus. This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register. User and priviledge mode [read]: 0 = no wrong key or key-sequence written 1 = wrong key or key-sequence written to RTIWDKEY register Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0
1	DWDST	R/W	0h	DWDST: Digital Watchdog Status. This bit is effectively a copy of the END TIME VIOL status flag and is maintained for compatibility reasons. User and priviledge mode [read]: 0 = DWD timeout period not expired 1 = DWD timeout period has expired Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0
0	AWDST	R/W	0h	AWDST: Analog Watchdog Status. User and priviledge mode [read]: 0 = AWD pin 0 > 1 threshold not exceeded 1 = AWD pin 0 > 1 threshold exceeded Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0

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5.21.2.31 RTI_RTIWDKEY Register

5.21.2.31.1 RTI_RTIWDKEY Register (Offset = 9Ch) [reset = 0h]

Watchdog Key correct written key values discharge the external capacitor.

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Table 5-2364. Instance Table

Instance Name	Physical Address
RTI0	5218 009Ch
RTI1	5218 109Ch
RTI2	5218 209Ch
RTI3	5218 309Ch
RTI4	5218 409Ch
RTI5	5218 509Ch
RTI6	5218 609Ch
RTI7	5218 709Ch

Figure 5-1154. RTI_RTIWDKEY Name Register

31	30	29	28	27	26	25	24
RESERVED19							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED19							
R/W							
0h							
15	14	13	12	11	10	9	8
WDKEY							
R/W							
0h							
7	6	5	4	3	2	1	0
WDKEY							
R/W							
0h							

Table 5-2365. RTI_RTIWDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED19	R/W	0h	Reserved. Reads return 0 and writes have no effect
15:0	WDKEY	R/W	0h	WDKEY: Watchdog Key. User and privilege mode reads are indeterminate. Privilege mode [write]: A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1s. Writing any other value causes a digital watchdog reset, as shown in Table 1-3. Note: Register write access time precaution The user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation.

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5.21.2.32 RTI_RTIDWDCNTR Register

5.21.2.32.1 RTI_RTIDWDCNTR Register (Offset = A0h) [reset = 0h]

Digital Watchdog Down Counter current value of DWD down counter.

Return to Summary Table

Table 5-2366. Instance Table

Instance Name	Physical Address
RTI0	5218 00A0h
RTI1	5218 10A0h
RTI2	5218 20A0h
RTI3	5218 30A0h
RTI4	5218 40A0h
RTI5	5218 50A0h
RTI6	5218 60A0h
RTI7	5218 70A0h

Figure 5-1155. RTI_RTIDWDCNTR Name Register

31	30	29	28	27	26	25	24
RESERVED20							DWDCNTR
R/W							R/W
0h							0h
23	22	21	20	19	18	17	16
DWDCNTR							
R/W							
0h							
15	14	13	12	11	10	9	8
DWDCNTR							
R/W							
0h							
7	6	5	4	3	2	1	0
DWDCNTR							
R/W							
0h							

Table 5-2367. RTI_RTIDWDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED20	R/W	0h	Reserved. Reads return 0 and writes have no effect
24:0	DWDCNTR	R/W	0h	DWDCNTR: Digital Watchdog Down Counter. The value of the DWDCNTR after a system reset is 0x002D_FFFF. When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second. User and privilege mode [read]: Reads return the current counter value. Privilege mode [write]: Writes dont have an effect.

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5.21.2.33 RTI_RTIWWDRXNCTRL Register

5.21.2.33.1 RTI_RTIWWDRXNCTRL Register (Offset = A4h) [reset = 0h]

Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset.

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Table 5-2368. Instance Table

Instance Name	Physical Address
RTI0	5218 00A4h
RTI1	5218 10A4h
RTI2	5218 20A4h
RTI3	5218 30A4h
RTI4	5218 40A4h
RTI5	5218 50A4h
RTI6	5218 60A4h
RTI7	5218 70A4h

Figure 5-1156. RTI_RTIWWDRXNCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED21							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED21							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED21							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED21				WWDRXN			
R/W				R/W			
0h				0h			

Table 5-2369. RTI_RTIWWDRXNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED21	R/W	0h	Reserved. Reads return 0 and writes have no effect

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Table 5-2369. RTI_RTIWWDRXNCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	WWDRXN	R/W	0h	WWDRXN: Digital Windowed Watchdog Reaction. User and privilege mode [read], privileged mode [write]: 0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. 0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Note: Configuration of DWWD Reaction The DWWD reaction can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.

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5.21.2.34 RTI_RTIWWDSIZECTRL Register

5.21.2.34.1 RTI_RTIWWDSIZECTRL Register (Offset = A8h) [reset = 0h]

Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog.

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Table 5-2370. Instance Table

Instance Name	Physical Address
RTI0	5218 00A8h
RTI1	5218 10A8h
RTI2	5218 20A8h
RTI3	5218 30A8h
RTI4	5218 40A8h
RTI5	5218 50A8h
RTI6	5218 60A8h
RTI7	5218 70A8h

Figure 5-1157. RTI_RTIWWDSIZECTRL Name Register

31	30	29	28	27	26	25	24
WWDSIZE							
R/W							
0h							
23	22	21	20	19	18	17	16
WWDSIZE							
R/W							
0h							
15	14	13	12	11	10	9	8
WWDSIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
WWDSIZE							
R/W							
0h							

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Table 5-2371. RTI_RTIWWDSIZECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WWDSIZE	R/W	0h	WWDSIZE: Digital Windowed Watchdog Window Size. User and privilege mode [read], privileged mode [write]: Value written to WWDSIZE Window Size 0x00000005 100% [Functionality same as the time-out digital watchdog.] 0x00000050 50% 0x00000500 25% 0x00005000 12.5% 0x00050000 6.25% 0x00500000 3.125% Any other value 3.125% Note: Incorrect value being written to watchdog window size control register If an incorerct value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration. Note: Configuration of DWWD Window Size The DWWD window size can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDSIZE is made when the watchdog service window is already open, then

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5.21.2.35 RTI_RTIINTCLRENABLE Register

5.21.2.35.1 RTI_RTIINTCLRENABLE Register (Offset = ACh) [reset = 0h]

RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts.

Return to Summary Table

Table 5-2372. Instance Table

Instance Name	Physical Address
RTI0	5218 00ACh
RTI1	5218 10ACh
RTI2	5218 20ACh
RTI3	5218 30ACh
RTI4	5218 40ACh
RTI5	5218 50ACh
RTI6	5218 60ACh
RTI7	5218 70ACh

Figure 5-1158. RTI_RTIINTCLRENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED25				INTCLRENABLE3			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED24				INTCLRENABLE2			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED23				INTCLRENABLE1			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED22				INTCLRENABLE0			
R/W				R/W			
0h				0h			

Table 5-2373. RTI_RTIINTCLRENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED25	R/W	0h	Reserved. Reads return 0 and writes have no effect
27:24	INTCLRENABLE3	R/W	0h	INTCLRENABLE3. Enables the auto-clear functionality on the compare 3 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 3 interrupt is disabled. Any other value = Auto-clear for compare 3 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 3 interrupt. Any other value = Enables the auto-clear functionality on the compare 3 interrupt.
23:20	RESERVED24	R/W	0h	Reserved. Reads return 0 and writes have no effect

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Table 5-2373. RTI_RTIINTCLRENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	INTCLRENABLE2	R/W	0h	INTCLRENABLE2. Enables the auto-clear functionality on the compare 2 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 2 interrupt is disabled. Any other value = Auto-clear for compare 2 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 2 interrupt. Any other value = Enables the auto-clear functionality on the compare 2 interrupt.
15:12	RESERVED23	R/W	0h	Reserved. Reads return 0 and writes have no effect
11:8	INTCLRENABLE1	R/W	0h	INTCLRENABLE1. Enables the auto-clear functionality on the compare 1 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 1 interrupt is disabled. Any other value = Auto-clear for compare 1 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 1 interrupt. Any other value = Enables the auto-clear functionality on the compare 1 interrupt.
7:4	RESERVED22	R/W	0h	Reserved. Reads return 0 and writes have no effect
3:0	INTCLRENABLE0	R/W	0h	INTCLRENABLE0. Enables the auto-clear functionality on the compare 0 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 0 interrupt is disabled. Any other value = Auto-clear for compare 0 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 0 interrupt. Any other value = Enables the auto-clear functionality on the compare 0 interrupt.

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5.21.2.36 RTI_RTICOMP0CLR Register

5.21.2.36.1 RTI_RTICOMP0CLR Register (Offset = B0h) [reset = 0h]

Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line.

Return to Summary Table

Table 5-2374. Instance Table

Instance Name	Physical Address
RTI0	5218 00B0h
RTI1	5218 10B0h
RTI2	5218 20B0h
RTI3	5218 30B0h
RTI4	5218 40B0h
RTI5	5218 50B0h
RTI6	5218 60B0h
RTI7	5218 70B0h

Figure 5-1159. RTI_RTICOMP0CLR Name Register

31	30	29	28	27	26	25	24
COMP0CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP0CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP0CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP0CLR							
R/W							
0h							

Table 5-2375. RTI_RTICOMP0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0CLR	R/W	0h	COMP0CLR: Compare 0 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.21.2.37 RTI_RTICOMP1CLR Register

5.21.2.37.1 RTI_RTICOMP1CLR Register (Offset = B4h) [reset = 0h]

Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line.

Return to Summary Table

Table 5-2376. Instance Table

Instance Name	Physical Address
RTI0	5218 00B4h
RTI1	5218 10B4h
RTI2	5218 20B4h
RTI3	5218 30B4h
RTI4	5218 40B4h
RTI5	5218 50B4h
RTI6	5218 60B4h
RTI7	5218 70B4h

Figure 5-1160. RTI_RTICOMP1CLR Name Register

31	30	29	28	27	26	25	24
COMP1CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP1CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP1CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP1CLR							
R/W							
0h							

Table 5-2377. RTI_RTICOMP1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1CLR	R/W	0h	COMP1CLR: Compare 1 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 1 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.21.2.38 RTI_RTICOMP2CLR Register

5.21.2.38.1 RTI_RTICOMP2CLR Register (Offset = B8h) [reset = 0h]

Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line.

Return to Summary Table

Table 5-2378. Instance Table

Instance Name	Physical Address
RTI0	5218 00B8h
RTI1	5218 10B8h
RTI2	5218 20B8h
RTI3	5218 30B8h
RTI4	5218 40B8h
RTI5	5218 50B8h
RTI6	5218 60B8h
RTI7	5218 70B8h

Figure 5-1161. RTI_RTICOMP2CLR Name Register

31	30	29	28	27	26	25	24
COMP2CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP2CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP2CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP2CLR							
R/W							
0h							

Table 5-2379. RTI_RTICOMP2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2CLR	R/W	0h	COMP2CLR: Compare 2 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 2 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.21.2.39 RTI_RTICOMP3CLR Register

5.21.2.39.1 RTI_RTICOMP3CLR Register (Offset = BCh) [reset = 0h]

Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line.

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Table 5-2380. Instance Table

Instance Name	Physical Address
RTI0	5218 00BCh
RTI1	5218 10BCh
RTI2	5218 20BCh
RTI3	5218 30BCh
RTI4	5218 40BCh
RTI5	5218 50BCh
RTI6	5218 60BCh
RTI7	5218 70BCh

Figure 5-1162. RTI_RTICOMP3CLR Name Register

31	30	29	28	27	26	25	24
COMP3CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP3CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP3CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP3CLR							
R/W							
0h							

Table 5-2381. RTI_RTICOMP3CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3CLR	R/W	0h	COMP3CLR: Compare 3 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 3 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.22 MSS_MBOX

MSS_MBOX

5.22.1 MSS_MBOX Summaries

MSS_MBOX Summaries

Table 5-2382. MSS_MBOX Registers, Base Address=7200 0000h, Length=16384

Offset	Length	Register Name	MSS_MBOX0 Physical Address
0h	32	MSS_MBOX_START	7200 0000h
3FFCh	32	MSS_MBOX_END	7200 3FFCh

5.22.2 MSS_MBOX Registers

MSS_MBOX Registers

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5.22.2.1 MSS_MBOX_START Register

5.22.2.1.1 MSS_MBOX_START Register (Offset = 0h) [reset = 0h]

Return to Summary Table

Table 5-2383. Instance Table

Instance Name	Physical Address
MSS_MBOX0	7200 0000h

Figure 5-1163. MSS_MBOX_START Name Register

31	30	29	28	27	26	25	24
START							
R/W							
0h							
23	22	21	20	19	18	17	16
START							
R/W							
0h							
15	14	13	12	11	10	9	8
START							
R/W							
0h							
7	6	5	4	3	2	1	0
START							
R/W							
0h							

Table 5-2384. MSS_MBOX_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	START	R/W	0h	Memory start address

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5.22.2.2 MSS_MBOX_END Register

5.22.2.2.1 MSS_MBOX_END Register (Offset = 3FFCh) [reset = 0h]

Return to Summary Table

Table 5-2385. Instance Table

Instance Name	Physical Address
MSS_MBOX0	7200 3FFCh

Figure 5-1164. MSS_MBOX_END Name Register

31	30	29	28	27	26	25	24
END							
R/W							
0h							
23	22	21	20	19	18	17	16
END							
R/W							
0h							
15	14	13	12	11	10	9	8
END							
R/W							
0h							
7	6	5	4	3	2	1	0
END							
R/W							
0h							

Table 5-2386. MSS_MBOX_END Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	END	R/W	0h	L2 Memory end address

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5.23 SoC_TIMESYNC_XBAR0

SoC_TIMESYNC_XBAR0

5.23.1 SoC_TIMESYNC_XBAR0 Summaries

SoC_TIMESYNC_XBAR0 Summaries

Table 5-2387. SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG Registers, Base Address=52E0 0000h, Length=1024

Offset	Length	Register Name	SOC_TIMESYNC_XBAR0 Physical Address
0h	32	SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_PID	52E0 0000h
4h	32	SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_MUXCNTL_J	52E0 0004h + formula

5.23.2 SoC_TIMESYNC_XBAR0 Registers

SoC_TIMESYNC_XBAR0 Registers

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5.23.2.1 SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_PID Register

5.23.2.1.1 SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Identification register.

Return to Summary Table

Table 5-2388. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR0	52E0 0000h

Figure 5-1165. SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
694h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTLVER					MAJREV		
R					R		
10h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINREV					
R		R					
0h		0h					

Table 5-2389. SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	FUNCTION	R	694h	function
15:11	RTLVER	R	10h	Rtl version
10:8	MAJREV	R	1h	major version
7:6	CUSTOM	R	0h	custom id
5:0	MINREV	R	0h	minor version

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5.23.2.2 SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_MUXCNTL_J Register

5.23.2.2.1 SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_MUXCNTL_J Register (Offset = 4h) [reset = 0h]

Interrupt mux control register.

Return to Summary Table

Table 5-2390. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR0	52E0 0004h + formula

Figure 5-1166. SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_MUXCNTL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							INT_ENABLE
NONE							R/W
0h							0h
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED			MUX_CNTL				
NONE			R/W				
0h			0h				

Table 5-2391. SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	Interrupt *j* Output Enable.
15:5	RESERVED	NONE	0h	Reserved
4:0	MUX_CNTL	R/W	0h	Mux Control for Interrupt *j*.

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5.24 SoC_TIMESYNC_XBAR1

SoC_TIMESYNC_XBAR1

5.24.1 SoC_TIMESYNC_XBAR1 Summaries

SoC_TIMESYNC_XBAR1 Summaries

Table 5-2392. SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG Registers, Base Address=52E0 4000h, Length=2048

Offset	Length	Register Name	SOC_TIMESYNC_XBAR1 Physical Address
0h	32	SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_PID	52E0 4000h
4h	32	SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_MUXCNTL_J	52E0 4004h + formula

5.24.2 SoC_TIMESYNC_XBAR1 Registers

SoC_TIMESYNC_XBAR1 Registers

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5.24.2.1 SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_PID Register

5.24.2.1.1 SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_PID Register (Offset = 0h) [reset = 66948100h]

Identification register.

Return to Summary Table

Table 5-2393. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR1	52E0 4000h

Figure 5-1167. SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_PID Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		694h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNCTION							
R							
694h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RTLVER					MAJREV		
R					R		
10h					1h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		MINREV					
R		R					
0h		0h					

Table 5-2394. SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme
29:28	BU	R	2h	bu
27:16	FUNCTION	R	694h	function
15:11	RTLVER	R	10h	Rtl version
10:8	MAJREV	R	1h	major version
7:6	CUSTOM	R	0h	custom id
5:0	MINREV	R	0h	minor version

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5.24.2.2 SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_MUXCNTL_J Register

5.24.2.2.1 SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_MUXCNTL_J Register (Offset = 4h) [reset = 0h]

Interrupt mux control register.

Return to Summary Table

Table 5-2395. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR1	52E0 4004h + formula

Figure 5-1168. SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_MUXCNTL_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							INT_ENABLE
NONE							R/W
0h							0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				MUX_CNTL			
NONE				R/W			
0h				0h			

Table 5-2396. SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_MUXCNTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:17	RESERVED	NONE	0h	Reserved
16	INT_ENABLE	R/W	0h	Interrupt *j* Output Enable.
15:4	RESERVED	NONE	0h	Reserved
3:0	MUX_CNTL	R/W	0h	Mux Control for Interrupt *j*.

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5.25 SPINLOCK

SPINLOCK

5.25.1 SPINLOCK Summaries

SPINLOCK Summaries

Table 5-2397. SPINLOCK Registers, Base Address=50E0 0000h, Length=32768

Offset	Length	Register Name	SPINLOCK0 Physical Address
0h	32	SPINLOCK_REVISION	50E0 0000h
10h	32	SPINLOCK_SYSCONFIG	50E0 0010h
14h	32	SPINLOCK_SYSTATUS	50E0 0014h
800h	32	SPINLOCK_LOCK_REG_J	50E0 0800h + formula

5.25.2 SPINLOCK Registers

SPINLOCK Registers

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5.25.2.1 SPINLOCK_REVISION Register

5.25.2.1.1 SPINLOCK_REVISION Register (Offset = 0h) [reset = 66FA6900h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space.

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Table 5-2398. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0000h

Figure 5-1169. SPINLOCK_REVISION Name Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNCTION			
R		R		R			
1h		2h		6FAh			
23	22	21	20	19	18	17	16
FUNCTION							
R							
6FAh							
15	14	13	12	11	10	9	8
RTL_VER					MAJOR_REV		
R					R		
Dh					1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR_REV					
R		R					
0h		0h					

Table 5-2399. SPINLOCK_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used.
29:28	BU	R	2h	BU identifier
27:16	FUNCTION	R	6FAh	Module family.
15:11	RTL_VER	R	Dh	RTL version. R of X.Y.R.Z
10:8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z
7:6	CUSTOM	R	0h	Special version number
5:0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z

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5.25.2.2 SPINLOCK_SYSCONFIG Register

5.25.2.2.1 SPINLOCK_SYSCONFIG Register (Offset = 10h) [reset = 0h]

Provides the SOFTRESET register for backwards compatibility with OMAP Spinlock.

Return to Summary Table

Table 5-2400. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0010h

Figure 5-1170. SPINLOCK_SYSCONFIG Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED						SOFT_RESET	RESERVED
NONE						R/W	NONE
0h						0h	0h

Table 5-2401. SPINLOCK_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED	NONE	0h	Reserved
1	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0 It has the same effect as the hardware reset Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and free all of the locks
0	RESERVED	NONE	0h	Reserved

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5.25.2.3 SPINLOCK_SYSTATUS Register

5.25.2.3.1 SPINLOCK_SYSTATUS Register (Offset = 14h) [reset = 8000000h]

Provides information about the Spinlock module.

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Table 5-2402. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0014h

Figure 5-1171. SPINLOCK_SYSTATUS Name Register

31	30	29	28	27	26	25	24
NUM_LOCKS							
R							
8h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
IN_USE7	IN_USE6	IN_USE5	IN_USE4	IN_USE3	IN_USE2	IN_USE1	IN_USE0
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2403. SPINLOCK_SYSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:24	NUM_LOCKS	R	8h	Module configuration parameter n, the total number of spinlocks divided by 32. e.g. For 256 spin locks, this will return the number 0x08
23:8	RESERVED	NONE	0h	Reserved
7	IN_USE7	R	0h	In-Use flag 7 covering lock registers 224 - 255. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 224 - 255 are in the Not Taken state Read 1 : At least one of the lock registers 224 - 255 are in the Taken state
6	IN_USE6	R	0h	In-Use flag 6 covering lock registers 192 - 223. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 192 - 223 are in the Not Taken state Read 1 : At least one of the lock registers 192 - 223 are in the Taken state
5	IN_USE5	R	0h	In-Use flag 5 covering lock registers 160 - 191. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 160 - 191 are in the Not Taken state Read 1 : At least one of the lock registers 160 - 191 are in the Taken state

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Table 5-2403. SPINLOCK_SYSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	IN_USE4	R	0h	In-Use flag 4 covering lock registers 128 - 159. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 128 - 159 are in the Not Taken state Read 1 : At least one of the lock registers 128 - 159 are in the Taken state
3	IN_USE3	R	0h	In-Use flag 3 covering lock registers 96 - 127. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 96 - 127 are in the Not Taken state Read 1 : At least one of the lock registers 96 - 127 are in the Taken state
2	IN_USE2	R	0h	In-Use flag 2 covering lock registers 64 - 95. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 64 - 95 are in the Not Taken state Read 1 : At least one of the lock registers 64 - 95 are in the Taken state
1	IN_USE1	R	0h	In-Use flag 1 covering lock registers 32 - 63. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 32 - 63 are in the Not Taken state Read 1 : At least one of the lock registers 32 - 63 are in the Taken state
0	IN_USE0	R	0h	In-Use flag 0 covering lock registers 0 - 31. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 0 - 31 are in the Not Taken state Read 1 : At least one of the lock registers 0 - 31 are in the Taken state

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5.25.2.4 SPINLOCK_LOCK_REG_J Register

5.25.2.4.1 SPINLOCK_LOCK_REG_J Register (Offset = 800h) [reset = 0h]

The Lock[a] register is read and written to perform lock and unlock operations on lock 'a'.

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Table 5-2404. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0800h + formula

Figure 5-1172. SPINLOCK_LOCK_REG_j Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED							TAKEN
NONE							R/W
0h							0h

Table 5-2405. SPINLOCK_LOCK_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31:1	RESERVED	NONE	0h	Reserved
0	TAKEN	R/W	0h	Lock Status Read 0 : Lock was previously free. The reader now has been granted the lock. Read 1 : Lock was previously taken. The reader has not been granted the lock and must retry. Write 0 : Free the lock by setting TAKEN to zero. Write 1 : No effect

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5.26 UART

UART

5.26.1 UART Summaries

UART Summaries

Table 5-2406. UART Registers, Base Address=5230 0000h, Length=512

Offset	Length	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	32	UART_DLL	5230 0000h	5230 1000h	5230 2000h
0h	32	UART_RHR	5230 0000h	5230 1000h	5230 2000h
0h	32	UART_THR	5230 0000h	5230 1000h	5230 2000h
4h	32	UART_DLH	5230 0004h	5230 1004h	5230 2004h
4h	32	UART_IER_CIR	5230 0004h	5230 1004h	5230 2004h
4h	32	UART_IER_IRDA	5230 0004h	5230 1004h	5230 2004h
4h	32	UART_IER_UART	5230 0004h	5230 1004h	5230 2004h
8h	32	UART_EFR	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_FCR	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_IIR_CIR	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_IIR_IRDA	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_IIR_UART	5230 0008h	5230 1008h	5230 2008h
Ch	32	UART_LCR	5230 000Ch	5230 100Ch	5230 200Ch
10h	32	UART_MCR	5230 0010h	5230 1010h	5230 2010h
10h	32	UART_XON1_ADDR1	5230 0010h	5230 1010h	5230 2010h
14h	32	UART_LSR_CIR	5230 0014h	5230 1014h	5230 2014h
14h	32	UART_LSR_IRDA	5230 0014h	5230 1014h	5230 2014h
14h	32	UART_LSR_UART	5230 0014h	5230 1014h	5230 2014h
14h	32	UART_XON2_ADDR2	5230 0014h	5230 1014h	5230 2014h
18h	32	UART_MSR	5230 0018h	5230 1018h	5230 2018h
18h	32	UART_TCR	5230 0018h	5230 1018h	5230 2018h
18h	32	UART_XOFF1	5230 0018h	5230 1018h	5230 2018h
1Ch	32	UART_SPR	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART_TLR	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART_XOFF2	5230 001Ch	5230 101Ch	5230 201Ch
20h	32	UART_MDR1	5230 0020h	5230 1020h	5230 2020h
24h	32	UART_MDR2	5230 0024h	5230 1024h	5230 2024h
28h	32	UART_SFLSR	5230 0028h	5230 1028h	5230 2028h
28h	32	UART_TXFLL	5230 0028h	5230 1028h	5230 2028h
2Ch	32	UART_RESUME	5230 002Ch	5230 102Ch	5230 202Ch
2Ch	32	UART_TXFLH	5230 002Ch	5230 102Ch	5230 202Ch
30h	32	UART_RXFLL	5230 0030h	5230 1030h	5230 2030h
30h	32	UART_SFREGL	5230 0030h	5230 1030h	5230 2030h
34h	32	UART_RXFLH	5230 0034h	5230 1034h	5230 2034h
34h	32	UART_SFREGH	5230 0034h	5230 1034h	5230 2034h
38h	32	UART_BLR	5230 0038h	5230 1038h	5230 2038h
38h	32	UART_UASR	5230 0038h	5230 1038h	5230 2038h
3Ch	32	UART_ACREG	5230 003Ch	5230 103Ch	5230 203Ch
40h	32	UART_SCR	5230 0040h	5230 1040h	5230 2040h

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Table 5-2406. UART Registers, Base Address=5230 0000h, Length=512 (continued)

Offset	Length	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
44h	32	UART_SSR	5230 0044h	5230 1044h	5230 2044h
48h	32	UART_EBLR	5230 0048h	5230 1048h	5230 2048h
50h	32	UART_MVR	5230 0050h	5230 1050h	5230 2050h
54h	32	UART_SYSC	5230 0054h	5230 1054h	5230 2054h
58h	32	UART_SYSS	5230 0058h	5230 1058h	5230 2058h
5Ch	32	UART_WER	5230 005Ch	5230 105Ch	5230 205Ch
60h	32	UART_CFPS	5230 0060h	5230 1060h	5230 2060h
64h	32	UART_RXFIFO_LVL	5230 0064h	5230 1064h	5230 2064h
68h	32	UART_TXFIFO_LVL	5230 0068h	5230 1068h	5230 2068h
6Ch	32	UART_IER2	5230 006Ch	5230 106Ch	5230 206Ch
70h	32	UART_ISR2	5230 0070h	5230 1070h	5230 2070h
74h	32	UART_FREQ_SEL	5230 0074h	5230 1074h	5230 2074h
78h	32	UART_ABAUD_1ST_CHAR	5230 0078h	5230 1078h	5230 2078h
7Ch	32	UART_BAUD_2ND_CHAR	5230 007Ch	5230 107Ch	5230 207Ch
80h	32	UART_MDR3	5230 0080h	5230 1080h	5230 2080h
84h	32	UART_TX_DMA_THRESHOLD	5230 0084h	5230 1084h	5230 2084h
88h	32	UART_MDR4	5230 0088h	5230 1088h	5230 2088h
8Ch	32	UART_EFR2	5230 008Ch	5230 108Ch	5230 208Ch
90h	32	UART_ECR	5230 0090h	5230 1090h	5230 2090h
94h	32	UART_TIMEGUARD	5230 0094h	5230 1094h	5230 2094h
98h	32	UART_TIMEOUTL	5230 0098h	5230 1098h	5230 2098h
9Ch	32	UART_TIMEOUTH	5230 009Ch	5230 109Ch	5230 209Ch
A0h	32	UART_SCCR	5230 00A0h	5230 10A0h	5230 20A0h
A4h	32	UART_ERHR	5230 00A4h	5230 10A4h	5230 20A4h
A4h	32	UART_ETHR	5230 00A4h	5230 10A4h	5230 20A4h
A8h	32	UART_MAR	5230 00A8h	5230 10A8h	5230 20A8h
ACh	32	UART_MMR	5230 00ACh	5230 10ACh	5230 20ACh
B0h	32	UART_MBR	5230 00B0h	5230 10B0h	5230 20B0h

Table 5-2407. UART Registers, Base Address=5230 0000h, Length=512

Offset	Length	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	32	UART_DLL	5230 3000h	5230 4000h	5230 5000h
0h	32	UART_RHR	5230 3000h	5230 4000h	5230 5000h
0h	32	UART_THR	5230 3000h	5230 4000h	5230 5000h
4h	32	UART_DLH	5230 3004h	5230 4004h	5230 5004h
4h	32	UART_IER_CIR	5230 3004h	5230 4004h	5230 5004h
4h	32	UART_IER_IRDA	5230 3004h	5230 4004h	5230 5004h
4h	32	UART_IER_UART	5230 3004h	5230 4004h	5230 5004h
8h	32	UART_EFR	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_FCR	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_IIR_CIR	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_IIR_IRDA	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_IIR_UART	5230 3008h	5230 4008h	5230 5008h
Ch	32	UART_LCR	5230 300Ch	5230 400Ch	5230 500Ch
10h	32	UART_MCR	5230 3010h	5230 4010h	5230 5010h

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Table 5-2407. UART Registers, Base Address=5230 0000h, Length=512 (continued)

Offset	Length	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
10h	32	UART_XON1_ADDR1	5230 3010h	5230 4010h	5230 5010h
14h	32	UART_LSR_CIR	5230 3014h	5230 4014h	5230 5014h
14h	32	UART_LSR_IRDA	5230 3014h	5230 4014h	5230 5014h
14h	32	UART_LSR_UART	5230 3014h	5230 4014h	5230 5014h
14h	32	UART_XON2_ADDR2	5230 3014h	5230 4014h	5230 5014h
18h	32	UART_MSR	5230 3018h	5230 4018h	5230 5018h
18h	32	UART_TCR	5230 3018h	5230 4018h	5230 5018h
18h	32	UART_XOFF1	5230 3018h	5230 4018h	5230 5018h
1Ch	32	UART_SPR	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART_TLR	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART_XOFF2	5230 301Ch	5230 401Ch	5230 501Ch
20h	32	UART_MDR1	5230 3020h	5230 4020h	5230 5020h
24h	32	UART_MDR2	5230 3024h	5230 4024h	5230 5024h
28h	32	UART_SFLSR	5230 3028h	5230 4028h	5230 5028h
28h	32	UART_TXFLL	5230 3028h	5230 4028h	5230 5028h
2Ch	32	UART_RESUME	5230 302Ch	5230 402Ch	5230 502Ch
2Ch	32	UART_TXFLH	5230 302Ch	5230 402Ch	5230 502Ch
30h	32	UART_RXFLL	5230 3030h	5230 4030h	5230 5030h
30h	32	UART_SFREGL	5230 3030h	5230 4030h	5230 5030h
34h	32	UART_RXFLH	5230 3034h	5230 4034h	5230 5034h
34h	32	UART_SFREGH	5230 3034h	5230 4034h	5230 5034h
38h	32	UART_BLR	5230 3038h	5230 4038h	5230 5038h
38h	32	UART_UASR	5230 3038h	5230 4038h	5230 5038h
3Ch	32	UART_ACREG	5230 303Ch	5230 403Ch	5230 503Ch
40h	32	UART_SCR	5230 3040h	5230 4040h	5230 5040h
44h	32	UART_SSR	5230 3044h	5230 4044h	5230 5044h
48h	32	UART_EBLR	5230 3048h	5230 4048h	5230 5048h
50h	32	UART_MVR	5230 3050h	5230 4050h	5230 5050h
54h	32	UART_SYSC	5230 3054h	5230 4054h	5230 5054h
58h	32	UART_SYSS	5230 3058h	5230 4058h	5230 5058h
5Ch	32	UART_WER	5230 305Ch	5230 405Ch	5230 505Ch
60h	32	UART_CFPS	5230 3060h	5230 4060h	5230 5060h
64h	32	UART_RXFIFO_LVL	5230 3064h	5230 4064h	5230 5064h
68h	32	UART_TXFIFO_LVL	5230 3068h	5230 4068h	5230 5068h
6Ch	32	UART_IER2	5230 306Ch	5230 406Ch	5230 506Ch
70h	32	UART_ISR2	5230 3070h	5230 4070h	5230 5070h
74h	32	UART_FREQ_SEL	5230 3074h	5230 4074h	5230 5074h
78h	32	UART_ABAUD_1ST_CHAR	5230 3078h	5230 4078h	5230 5078h
7Ch	32	UART_BAUD_2ND_CHAR	5230 307Ch	5230 407Ch	5230 507Ch
80h	32	UART_MDR3	5230 3080h	5230 4080h	5230 5080h
84h	32	UART_TX_DMA_THRESHOLD	5230 3084h	5230 4084h	5230 5084h
88h	32	UART_MDR4	5230 3088h	5230 4088h	5230 5088h
8Ch	32	UART_EFR2	5230 308Ch	5230 408Ch	5230 508Ch
90h	32	UART_ECR	5230 3090h	5230 4090h	5230 5090h
94h	32	UART_TIMEGUARD	5230 3094h	5230 4094h	5230 5094h
98h	32	UART_TIMEOUTL	5230 3098h	5230 4098h	5230 5098h

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Table 5-2407. UART Registers, Base Address=5230 0000h, Length=512 (continued)

Offset	Length	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
9Ch	32	UART_TIMEOUTH	5230 309Ch	5230 409Ch	5230 509Ch
A0h	32	UART_SCCR	5230 30A0h	5230 40A0h	5230 50A0h
A4h	32	UART_ERHR	5230 30A4h	5230 40A4h	5230 50A4h
A4h	32	UART_ETHR	5230 30A4h	5230 40A4h	5230 50A4h
A8h	32	UART_MAR	5230 30A8h	5230 40A8h	5230 50A8h
ACh	32	UART_MMR	5230 30ACh	5230 40ACh	5230 50ACh
B0h	32	UART_MBR	5230 30B0h	5230 40B0h	5230 50B0h

5.26.2 UART Registers

UART Registers

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5.26.2.1 UART_DLL Register

5.26.2.1.1 UART_DLL Register (Offset = 0h) [reset = 0h]

Divisor Latches Low Register.

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Table 5-2408. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 5-1173. UART_DLL Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLOCK_LSB							
R/W							
0h							

Table 5-2409. UART_DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CLOCK_LSB	R/W	0h	Used to store the 8-bit LSB divisor value

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5.26.2.2 UART_RHR Register

5.26.2.2.1 UART_RHR Register (Offset = 0h) [reset = 0h]

The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character.
Note: If an overflow occurs the data in the RHR is not overwritten.

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Table 5-2410. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 5-1174. UART_RHR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RHR							
R							
0h							

Table 5-2411. UART_RHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:0	RHR	R	0h	Receive holding register

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5.26.2.3 UART_THR Register

5.26.2.3.1 UART_THR Register (Offset = 0h) [reset = 0h]

The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.

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Table 5-2412. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 5-1175. UART_THR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
THR							
W							
0h							

Table 5-2413. UART_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:0	THR	W	0h	TRANSMIT HOLDING REGISTER

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5.26.2.4 UART_DLH Register

5.26.2.4.1 UART_DLH Register (Offset = 4h) [reset = 0h]

Divisor Latches High Register.

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Table 5-2414. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 5-1176. UART_DLH Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
CLOCK_MSB							
R/W							
0h							

Table 5-2415. UART_DLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	CLOCK_MSB	R/W	0h	Used to store the 8-bit MSB divisor value

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5.26.2.5 UART_IER_CIR Register

5.26.2.5.1 UART_IER_CIR Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

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Table 5-2416. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 5-1177. UART_IER_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
NOT_USED2		TX_STATUS_IT	NOT_USED1	RX_OVERRUN_IT	RX_STOP_IT	THR_IT	RHR_IT
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 5-2417. UART_IER_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	NOT_USED2	R/W	0h	
5	TX_STATUS_IT	R/W	0h	0 Disables the TX status interrupt. 1 Enables the TX status interrupt.
4	NOT_USED1	R/W	0h	
3	RX_OVERRUN_IT	R/W	0h	0 Disables the RX overrun interrupt. 1 Enables the RX overrun interrupt.
2	RX_STOP_IT	R/W	0h	0 Disables the receive stop interrupt. 1 Enables the receive stop interrupt.
1	THR_IT	R/W	0h	0 Disables the THR interrupt. 1 Enables the THR interrupt.

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Table 5-2417. UART_IER_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RHR_IT	R/W	0h	0 Disables the RHR interrupt. 1 Enables the RHR interrupt.

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5.26.2.6 UART_IER_IRDA Register

5.26.2.6.1 UART_IER_IRDA Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

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Table 5-2418. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 5-1178. UART_IER_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_TRIG_IT	RX_OVERRUN_IT	LAST_RX_BYTE_IT	THR_IT	RHR_IT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2419. UART_IER_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EOF_IT	R/W	0h	0 Disables the received EOF interrupt. 1 Enables the received EOF interrupt.
6	LINE_STS_IT	R/W	0h	0 Disables the receiver line status interrupt. 1 Enables the receiver line status interrupt.
5	TX_STATUS_IT	R/W	0h	0 Disables the TX status interrupt. 1 Enables the TX status interrupt.
4	STS_FIFO_TRIG_IT	R/W	0h	0 Disables the status FIFO trigger level interrupt. 1 Enables the status FIFO trigger level interrupt.

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Table 5-2419. UART_IER_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RX_OVERRUN_IT	R/W	0h	0 Disables the RX overrun interrupt. 1 Enables the RX overrun interrupt.
2	LAST_RX_BYTE_IT	R/W	0h	0 Disables the last byte of frame in RX FIFO interrupt. 1 Enables the last byte of frame in RX FIFO interrupt.
1	THR_IT	R/W	0h	0 Disables the THR interrupt. 1 Enables the THR interrupt.
0	RHR_IT	R/W	0h	0 Disables the RHR interrupt. 1 Enables the RHR interrupt.

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5.26.2.7 UART_IER_UART Register

5.26.2.7.1 UART_IER_UART Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS*/RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.

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Table 5-2420. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 5-1179. UART_IER_UART Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
CTS_IT	RTS_IT	XOFF_IT	SLEEP_MODE	MODEM_STS_IT	LINE_STS_IT	THR_IT	RHR_IT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2421. UART_IER_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7	CTS_IT	R/W	0h	0 Disables the CTS* interrupt 1 Enables the CTS* interrupt
6	RTS_IT	R/W	0h	0 Disables the RTS* interrupt 1 Enables the RTS* interrupt
5	XOFF_IT	R/W	0h	0 Disables the XOFF interrupt 1 Enables the XOFF interrupt
4	SLEEP_MODE	R/W	0h	0 Disables sleep mode 1 Enables sleep mode (stop baud rate clock when the module is inactive)

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Table 5-2421. UART_IER_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MODEM_STS_IT	R/W	0h	0 Disables the modem status register interrupt 1 Enables the modem status register interrupt
2	LINE_STS_IT	R/W	0h	0 Disables the receiver line status interrupt 1 Enables the receiver line status interrupt
1	THR_IT	R/W	0h	0 Disables the THR interrupt 1 Enables the THR interrupt
0	RHR_IT	R/W	0h	0 Disables the RHR interrupt and time out interrupt. 1 Enables the RHR interrupt and time out interrupt.

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5.26.2.8 UART_EFR Register

5.26.2.8.1 UART_EFR Register (Offset = 8h) [reset = 0h]

Enhanced Feature Register.

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Table 5-2422. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 5-1180. UART_EFR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
AUTO_CTS_EN	AUTO_RTS_EN	SPECIAL_CHAR_DETECT	ENHANCED_EN	SW_FLOW_CONTROL			
R/W	R/W	R/W	R/W	R/W			
0h	0h	0h	0h	0h			

Table 5-2423. UART_EFR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	AUTO_CTS_EN	R/W	0h	Auto-CTS enable bit. 0:Normal operation. 1:Auto-CTS flow control is enabled i.e. transmission is halted when the CTS* pin is high (inactive).
6	AUTO_RTS_EN	R/W	0h	Auto-RTS enable bit. 0:Normal operation. 1:Auto- RTS flow control is enabled i.e. RTS* pin goes high (inactive) when the receiver FIFO HALT trigger level, TCR[3:0], is reached, and goes low (active) when the receiver FIFO RESTORE transmission trigger level is reached.
5	SPECIAL_CHAR_DETECT	R/W	0h	0: Normal operation. 1:Special character detect enable. Received data is compared with XOFF2 data. If a match occurs the received data is transferred to RX FIFO and IIR bit 4 is set to 1 to indicate a special character has been detected.

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Table 5-2423. UART_EFR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ENHANCED_EN	R/W	0h	Enhanced functions write enable bit. 0:Disables Writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. 1:Enables Writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7.
3:0	SW_FLOW_CONTROL	R/W	0h	Combinations of Software flow control can be selected by programming bit 3 - bit 0. See Software Flow Control Options

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5.26.2.9 UART_FCR Register

5.26.2.9.1 UART_FCR Register (Offset = 8h) [reset = 0h]

Notes:
Bits 4 and 5 can only be written to when EFR[4] = 1
Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0)
See Table 31 for FCR[5:4] setting restriction when SCR[6]=1
See Table 32 for FCR[7:6] setting restriction when SCR[7]=1

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Table 5-2424. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 5-1181. UART_FCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_FIFO_TRIG		TX_FIFO_TRIG		DMA_MODE	TX_FIFO_CLEAR	RX_FIFO_CLEAR	FIFO_EN
W		W		W	W	W	W
0h		0h		0h	0h	0h	0h

Table 5-2425. UART_FCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:6	RX_FIFO_TRIG	W	0h	Sets the trigger level for the RX FIFO: If SCR[7] = 0 and TLR[7:4] = 0000 br#00: 8 characters br#01:16 characters br#10:56 characters br#11:60 characters If SCR[7] = 0 and TLR[7:4] != 0000 RX_FIFO_TRIG is not considered. If SCR[7]=1, RX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1.

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Table 5-2425. UART_FCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	TX_FIFO_TRIG	W	0h	Sets the trigger level for the TX FIFO: If SCR[6] = 0 and TLR[3:0] = 0000 br#00: 8 spaces br#01:16 spaces br#10:32 spaces br#11:56 spaces If SCR[6] = 0 and TLR[3:0] != 0000 TX_FIFO_TRIG is not considered. If SCR[6]=1, TX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1
3	DMA_MODE	W	0h	This register is considered if SCR[0] = 0. 0 DMA_MODE 0 (No DMA) 1 DMA_MODE 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)
2	TX_FIFO_CLEAR	W	0h	0 No change 1 Clears the transmit FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.
1	RX_FIFO_CLEAR	W	0h	0 No change 1 Clears the receive FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.
0	FIFO_EN	W	0h	0 Disables the transmit and receive FIFOs. The transmit and receive holding registers are one byte FIFOs. 1 : Enables the transmit and receive FIFOs.The transmit and receive holding registers are 64-bytes FIFOs.

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5.26.2.10 UART_IIR_CIR Register

5.26.2.10.1 UART_IIR_CIR Register (Offset = 8h) [reset = 0h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

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Table 5-2426. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 5-1182. UART_IIR_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RESERVED		TX_STATUS_IT	RESERVED	RX_OE_IT	RX_STOP_IT	THR_IT	RHR_IT
NONE		R	NONE	R	R	R	R
0h		0h	0h	0h	0h	0h	0h

Table 5-2427. UART_IIR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED	NONE	0h	Reserved
5	TX_STATUS_IT	R	0h	0 TX status interrupt inactive 1 TX status interrupt active
4	RESERVED	NONE	0h	Reserved
3	RX_OE_IT	R	0h	0 RX overrun interrupt inactive 1 RX overrun interrupt active
2	RX_STOP_IT	R	0h	0 Receive stop interrupt inactive 1 Receive stop interrupt active
1	THR_IT	R	0h	0 THR interrupt inactive 1 THR interrupt active
0	RHR_IT	R	0h	0 RHR interrupt inactive 1 RHR interrupt active

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5.26.2.11 UART_IIR_IRDA Register

5.26.2.11.1 UART_IIR_IRDA Register (Offset = 8h) [reset = 0h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

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Table 5-2428. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 5-1183. UART_IIR_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_IT	RX_OE_IT	RX_FIFO_LAST_BYTE_IT	THR_IT	RHR_IT
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2429. UART_IIR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	EOF_IT	R	0h	0 Received EOF interrupt inactive 1 Received EOF interrupt active
6	LINE_STS_IT	R	0h	0 Receiver line status interrupt inactive 1 Receiver line status interrupt active
5	TX_STATUS_IT	R	0h	0 TX status interrupt inactive 1 TX status interrupt active
4	STS_FIFO_IT	R	0h	0 Status FIFO trigger level interrupt inactive 1 Status FIFO trigger level interrupt active
3	RX_OE_IT	R	0h	0 RX overrun interrupt inactive 1 RX overrun interrupt active

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Table 5-2429. UART_IIR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RX_FIFO_LAST_BYTE_IT	R	0h	0 Last byte of frame in RX FIFO interrupt inactive 1 Last byte of frame in RX FIFO interrupt active
1	THR_IT	R	0h	0 THR interrupt inactive 1 THR interrupt active
0	RHR_IT	R	0h	0 RHR interrupt inactive 1 RHR interrupt active

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5.26.2.12 UART_IIR_UART Register

5.26.2.12.1 UART_IIR_UART Register (Offset = 8h) [reset = 1h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

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Table 5-2430. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 5-1184. UART_IIR_UART Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FCR_MIRROR		IT_TYPE					IT_PENDING
R		R					R
0h		0h					1h

Table 5-2431. UART_IIR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:6	FCR_MIRROR	R	0h	Mirror the contents of FCR[0] on both bits.
5:1	IT_TYPE	R	0h	0 Modem Interrupt. Priority=4 1 THR interrupt. Priority=3 2 RHR interrupt. Priority=2 3 Receiver line status error. Priority=3 6 Rx timeout. Priority=2 8 Xoff/Special character. Priority=5 16 CTS, RTS, DSR change state from active (low) to inactive (high). Priority=6
0	IT_PENDING	R	1h	0 An interrupt is pending 1 No interrupt is pending

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5.26.2.13 UART_LCR Register

5.26.2.13.1 UART_LCR Register (Offset = Ch) [reset = 0h]

LCR[6:0] define parameters of the transmission and reception.
Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.

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Table 5-2432. Instance Table

Instance Name	Physical Address
UART0	5230 000Ch
UART1	5230 100Ch
UART2	5230 200Ch
UART3	5230 300Ch
UART4	5230 400Ch
UART5	5230 500Ch

Figure 5-1185. UART_LCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
DIV_EN	BREAK_EN	PARITY_TYPE 2	PARITY_TYPE 1	PARITY_EN	NB_STOP	CHAR_LENGTH	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0h	0h	0h	0h	0h	0h	0h	

Table 5-2433. UART_LCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7	DIV_EN	R/W	0h	0 Normal operating condition 1 Divisor latch enable. Allows to access to DLL, DLH and other registers (refer to the registers mapping)
6	BREAK_EN	R/W	0h	Break control bit. 0 Normal operating condition. 1 Forces the transmitter output to go low to alert the communication terminal
5	PARITY_TYPE2	R/W	0h	Selects the forced parity format [if LCR[3] = 1]. If LCR[5] = 1 and LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If LCR[5] = 1 and LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data.
4	PARITY_TYPE1	R/W	0h	0 Odd parity is generated (if LCR[3] = 1) 1 Even parity is generated (if LCR[3] = 1)

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Table 5-2433. UART_LCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PARITY_EN	R/W	0h	0 No parity 1 A parity bit is generated during transmission and the receiver checks for received parity.
2	NB_STOP	R/W	0h	Specifies the number of stop bits: 0 1 stop bits (word length = 5, 6, 7, 8) 1 1.5 stop bits (word length = 5) in USART mode. 2 stop bits (word length = 6, 7, 8)
1:0	CHAR_LENGTH	R/W	0h	Specifies the word length to be transmitted or received. 0 5 bits 1 6 bits 2 7 bits 3 8 bits

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5.26.2.14 UART_MCR Register

5.26.2.14.1 UART_MCR Register (Offset = 10h) [reset = 0h]

MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.

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Table 5-2434. Instance Table

Instance Name	Physical Address
UART0	5230 0010h
UART1	5230 1010h
UART2	5230 2010h
UART3	5230 3010h
UART4	5230 4010h
UART5	5230 5010h

Figure 5-1186. UART_MCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED	TCR_TLR	XON_EN	LOOPBACK_EN	CD_STS_CH	RI_STS_CH	RTS	DTR
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2435. UART_MCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7	RESERVED	R	0h	
6	TCR_TLR	R/W	0h	0 No action 1 Enables access to the TCR and TLR registers.
5	XON_EN	R/W	0h	0 Disable 'XON any' function 1 Enable 'XON any' function
4	LOOPBACK_EN	R/W	0h	0 Normal operating mode 1 Enable local loopback mode (internal). In this mode the MCR[3:0] signals are looped back into MSR[7:4]. The transmit output is looped back to the receive input internally
3	CD_STS_CH	R/W	0h	0 In loopback forces DCD* input high and IRQ outputs to inactive state. 1 In loopback forces DCD* input low and IRQ outputs to inactive state.

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Table 5-2435. UART_MCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RI_STS_CH	R/W	0h	0 In loopback forces RI* input high. 1 In loopback forces RI* input low.
1	RTS	R/W	0h	In loop back controls MSR[4]. If auto-RTS is enabled the RTS* output is controlled by hardware flow control. 0 Force RTS* output to inactive (high). 1 Force RTS* output to active (low).
0	DTR	R/W	0h	0 Force DTR* output to inactive (high). 1 Force DTR* output to active (low).

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5.26.2.15 UART_XON1_ADDR1 Register

5.26.2.15.1 UART_XON1_ADDR1 Register (Offset = 10h) [reset = 0h]

XON1/ADDR1 Register.

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Table 5-2436. Instance Table

Instance Name	Physical Address
UART0	5230 0010h
UART1	5230 1010h
UART2	5230 2010h
UART3	5230 3010h
UART4	5230 4010h
UART5	5230 5010h

Figure 5-1187. UART_XON1_ADDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XON_WORD1							
R/W							
0h							

Table 5-2437. UART_XON1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XON_WORD1	R/W	0h	Used to store the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes.

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5.26.2.16 UART_LSR_CIR Register

5.26.2.16.1 UART_LSR_CIR Register (Offset = 14h) [reset = 81h]

IR CIR mode line status register.

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Table 5-2438. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 5-1188. UART_LSR_CIR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
THR_EMPTY	RESERVED	RX_STOP	RESERVED				RX_FIFO_E
R	R	R	NONE				R
1h	0h	0h	0h				1h

Table 5-2439. UART_LSR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	THR_EMPTY	R	1h	0 Transmit holding register (TX FIFO) is not empty 1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed
6	RESERVED	R	0h	
5	RX_STOP	R	0h	The RX_STOP is generated based on the value set in the BOF Length register (EBLR). It is cleared on a single read of the LSR register 0 Reception is on going or waiting for a new frame 1 Reception is completed
4:1	RESERVED	NONE	0h	Reserved
0	RX_FIFO_E	R	1h	0 No data in the receive FIFO 1 At least one data character in the RX FIFO

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5.26.2.17 UART_LSR_IRDA Register

5.26.2.17.1 UART_LSR_IRDA Register (Offset = 14h) [reset = 83h]

IR-IRDA mode line status register.

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Table 5-2440. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 5-1189. UART_LSR_IRDA Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
THR_EMPTY	STS_FIFO_FULL	RX_LAST_BYTE	FRAME_TOO_LONG	ABORT	CRC	STS_FIFO_E	RX_FIFO_E
R	R	R	R	R	R	R	R
1h	0h	0h	0h	0h	0h	1h	1h

Table 5-2441. UART_LSR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7	THR_EMPTY	R	1h	0 Transmit holding register (TX FIFO) is not empty 1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed
6	STS_FIFO_FULL	R	0h	0 Status FIFO not full 1 Status FIFO full
5	RX_LAST_BYTE	R	0h	0 The RX FIFO (RHR) does not contain the last byte of the frame to be read 1 The RX FIFO (RHR) contains the last byte of the frame to be read.This bit is only set when the last byte of a frame is available to be read. It is used to determine the frame boundary. It is cleared on a single read of the LSR register

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Table 5-2441. UART_LSR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	FRAME_TOO_LONG	R	0h	0 No frame-too-long error in frame 1 Frame-too-long error in the frame at the top of the STATUS FIFO, [next character to be read]. This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) has been received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected
3	ABORT	R	0h	0 No abort pattern error in frame 1 Abort pattern is received. SIR & MIR: Abort pattern. FIR: Illegal symbol
2	CRC	R	0h	0 No CRC error in frame 1 CRC error in the frame at the top of the STATUS FIFO (next character to be read)
1	STS_FIFO_E	R	1h	0 Status FIFO not empty 1 Status FIFO empty
0	RX_FIFO_E	R	1h	0 No data in the receive FIFO 1 At least one data character in the RX FIFO

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5.26.2.18 UART_LSR_UART Register

5.26.2.18.1 UART_LSR_UART Register (Offset = 14h) [reset = 60h]

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Table 5-2442. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 5-1190. UART_LSR_UART Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_STS	TX_SR_E	TX_FIFO_E	RX_BI	RX_FE	RX_PE	RX_OE	RX_FIFO_E
R	R	R	R	R	R	R	R
0h	1h	1h	0h	0h	0h	0h	0h

Table 5-2443. UART_LSR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7	RX_FIFO_STS	R	0h	0 Normal operation 1 At least one parity error, framing error or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO.
6	TX_SR_E	R	1h	0 Transmitter hold (TX FIFO) and shift registers are not empty. 1 Transmitter hold (TX FIFO) and shift registers are empty
5	TX_FIFO_E	R	1h	0 Transmit hold register (TX FIFO) is not empty 1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed.

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Table 5-2443. UART_LSR_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RX_BI	R	0h	0 No break condition 1 A break was detected while the data being read from the RX FIFO was being received. (i.e. RX input was low for one character + 1 bit time frame).
3	RX_FE	R	0h	0 No framing error in data being read from RX FIFO. 1 Framing error occurred in data being read from RX FIFO.(received data did not have a valid stop bit)
2	RX_PE	R	0h	0 No parity error in data being read from RX FIFO. 1 Parity error in data being read from RX FIFO
1	RX_OE	R	0h	0 No overrun error 1 Overrun error has occurred. Set when the character held in the receive shift register is not transferred to the RX FIFO. This case can occurs only when receive FIFO is full.
0	RX_FIFO_E	R	0h	Line Status Register 0 No data in the receive FIFO 1 At least one data character in the RX FIFO

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5.26.2.19 UART_XON2_ADDR2 Register

5.26.2.19.1 UART_XON2_ADDR2 Register (Offset = 14h) [reset = 0h]

XON2/ADDR2 Register.

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Table 5-2444. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 5-1191. UART_XON2_ADDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XON_WORD2							
R/W							
0h							

Table 5-2445. UART_XON2_ADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XON_WORD2	R/W	0h	Used to store the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes.

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5.26.2.20 UART_MSR Register

5.26.2.20.1 UART_MSR Register (Offset = 18h) [reset = 0h]

This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.

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Table 5-2446. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 5-1192. UART_MSR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
NCD_STS	NRI_STS	NDSR_STS	NCTS_STS	DCD_STS	RI_STS	DSR_STS	CTS_STS
R	R	R	R	R	R	R	R
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2447. UART_MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7	NCD_STS	R	0h	This bit is the complement of the DCD* input. In loop-back mode it is equivalent to MCR[3]
6	NRI_STS	R	0h	This bit is the complement of the RI* input. In loop-back mode it is equivalent to MCR[2]
5	NDSR_STS	R	0h	This bit is the complement of the DSR* input. In loop-back mode, it is equivalent to MCR[0]
4	NCTS_STS	R	0h	This bit is the complement of the CTS* input. In loop-back mode it is equivalent to MCR[1]
3	DCD_STS	R	0h	Indicates that DCD* input [or MCR[3] in loop back] has changed. Cleared on a read.
2	RI_STS	R	0h	Indicates that RI* input [or MCR[2] in loop back] has changed state from low to high. Cleared on a read.
1	DSR_STS	R	0h	1 Indicates that DSR* input (or MCR[0] in loop back) has changed state. Cleared on a read

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Table 5-2447. UART_MSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CTS_STS	R	0h	1 Indicates that CTS* input (or MCR[1] in loop back) has changed state. Cleared on a read.

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5.26.2.21 UART_TCR Register

5.26.2.21.1 UART_TCR Register (Offset = 18h) [reset = Fh]

Transmission Control Register.

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Table 5-2448. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 5-1193. UART_TCR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG_START				RX_FIFO_TRIG_HALT			
R/W				R/W			
0h				Fh			

Table 5-2449. UART_TCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	RX_FIFO_TRIG_START	R/W	0h	RX FIFO trigger level to RESTORE transmission (0 - 60)
3:0	RX_FIFO_TRIG_HALT	R/W	Fh	RX FIFO trigger level to HALT transmission (0 - 60)

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5.26.2.22 UART_XOFF1 Register

5.26.2.22.1 UART_XOFF1 Register (Offset = 18h) [reset = 0h]

XOFF1 Register.

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Table 5-2450. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 5-1194. UART_XOFF1 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XOFF_WORD1							
R/W							
0h							

Table 5-2451. UART_XOFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XOFF_WORD1	R/W	0h	Used to store the 8-bit XOFF1 character in used in UART modes.

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5.26.2.23 UART_SPR Register

5.26.2.23.1 UART_SPR Register (Offset = 1Ch) [reset = 0h]

This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.

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Table 5-2452. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 5-1195. UART_SPR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
SPR_WORD							
R/W							
0h							

Table 5-2453. UART_SPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:0	SPR_WORD	R/W	0h	Scratchpad register

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5.26.2.24 UART_TLR Register

5.26.2.24.1 UART_TLR Register (Offset = 1Ch) [reset = 0h]

Trigger Level Register.

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Table 5-2454. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 5-1196. UART_TLR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG_DMA				TX_FIFO_TRIG_DMA			
R/W				R/W			
0h				0h			

Table 5-2455. UART_TLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:4	RX_FIFO_TRIG_DMA	R/W	0h	Receive FIFO trigger level
3:0	TX_FIFO_TRIG_DMA	R/W	0h	Transmit FIFO trigger level

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5.26.2.25 UART_XOFF2 Register

5.26.2.25.1 UART_XOFF2 Register (Offset = 1Ch) [reset = 0h]

XOFF2 Register.

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Table 5-2456. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 5-1197. UART_XOFF2 Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
XOFF_WORD2							
R/W							
0h							

Table 5-2457. UART_XOFF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	XOFF_WORD2	R/W	0h	Used to store the 8-bit XOFF2 character in used in UART modes.

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5.26.2.26 UART_MDR1 Register

5.26.2.26.1 UART_MDR1 Register (Offset = 20h) [reset = 7h]

The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation.
Note: If the module is disabled by setting the MODE_SELECT field to.

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Table 5-2458. Instance Table

Instance Name	Physical Address
UART0	5230 0020h
UART1	5230 1020h
UART2	5230 2020h
UART3	5230 3020h
UART4	5230 4020h
UART5	5230 5020h

Figure 5-1198. UART_MDR1 Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
FRAME_END_MODE	SIP_MODE	SCT	SET_TXIR	IR_SLEEP	MODE_SELECT		
R/W	R/W	R/W	R/W	R/W	R/W		
0h	0h	0h	0h	0h	7h		

Table 5-2459. UART_MDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7	FRAME_END_MODE	R/W	0h	IrDA mode only. 0 Frame-length method 1 Set EOT bit method
6	SIP_MODE	R/W	0h	MIR/FIR modes only. 0 Manual SIP mode: SIP is generated with the control of ACREG[3] 1 Automatic SIP mode: SIP is generated after each transmission.

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Table 5-2459. UART_MDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SCT	R/W	0h	Store and control the transmission 0 Starts the Infrared transmission as soon as a value is written to THR 1 Starts the Infrared transmission with the control of ACREG[2]. Note: before starting any transmission, there must be no reception on going.
4	SET_TXIR	R/W	0h	Used to configure the infrared transceiver. 0 No action if MDR2[7]=0. TXIR pin output is forced low if MDR2[7]=1 1 TXIR pin output is forced high (not dependant of MDR2[7] value).
3	IR_SLEEP	R/W	0h	0 IrDA/CIR sleep mode disabled 1 IrDA/CIR sleep mode enabled
2:0	MODE_SELECT	R/W	7h	0 UART 16x mode 1 SIR mode 2 UART 16x auto-baud 3 UART 13x mode 4 MIR mode 5 FIR mode 6 CIR mode 7 Disable (default state)

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5.26.2.27 UART_MDR2 Register

5.26.2.27.1 UART_MDR2 Register (Offset = 24h) [reset = 0h]

IR-IrDA and IR-CIR modes only.
MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX_UNDERRUN bit should be read after an IIR[5] TX_STATUS_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].
Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.

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Table 5-2460. Instance Table

Instance Name	Physical Address
UART0	5230 0024h
UART1	5230 1024h
UART2	5230 2024h
UART3	5230 3024h
UART4	5230 4024h
UART5	5230 5024h

Figure 5-1199. UART_MDR2 Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
SET_TXIR_ALT	IRRXINVERT	CIR_PULSE_MODE		UART_PULSE	STS_FIFO_TRIG		IRTX_UNDERRUN
R/W	R/W	R/W		R/W	R/W		R
0h	0h	0h		0h	0h		0h

Table 5-2461. UART_MDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7	SET_TXIR_ALT	R/W	0h	Provide alternate functionnality for MDR1[4] [SET_TXIR] 0 Normal mode 1 Alternate mode for SET_TXIR
6	IRRXINVERT	R/W	0h	Only for IR mode [IRDA & CIR]Invert RX pin inside the module before the voting or sampling system logic of the infra red block. This will not effect the RX path in UART Modem modes. 0 inversion is performed 1 No inversion is performed

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Table 5-2461. UART_MDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:4	CIR_PULSE_MODE	R/W	0h	CIR Pulse modulation definition. It defines high level of the pulse width associated with a digit: 0 Pulse width of 3 from 12 cycles 1 Pulse width of 4 from 12 cycles 2 Pulse width of 5 from 12 cycles 3 Pulse width of 6 from 12 cycles
3	UART_PULSE	R/W	0h	UART mode only. Used to allow pulse shaping in UART mode. 0 normal UART mode 1 UART mode with a pulse shaping
2:1	STS_FIFO_TRIG	R/W	0h	Only for IR-IRDA mode. Frame Status FIFO Threshold select: 0 1 entry 1 4 entries 2 7 entries 3 8 entries
0	IRTX_UNDERRUN	R	0h	IRDA Transmission status interrupt.When the IIR[5] interrupt occurs, the meaning of the interrupt is : 0 the last bit of the frame has been transmitted successfully without error. 1 an underrun has occurred. The last bit of the frame has been transmitted but with an underrun error present. The bit is reset to '0' when the RESUME register is read.

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5.26.2.28 UART_SFLSR Register

5.26.2.28.1 UART_SFLSR Register (Offset = 28h) [reset = 0h]

IrDA modes only.
Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).

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Table 5-2462. Instance Table

Instance Name	Physical Address
UART0	5230 0028h
UART1	5230 1028h
UART2	5230 2028h
UART3	5230 3028h
UART4	5230 4028h
UART5	5230 5028h

Figure 5-1200. UART_SFLSR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED5			OE_ERROR	FRAME_TOO_LONG_ERROR	ABORT_DETECT	CRC_ERROR	RESERVED0
R			R	R	R	R	R
0h			0h	0h	0h	0h	0h

Table 5-2463. UART_SFLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:5	RESERVED5	R	0h	
4	OE_ERROR	R	0h	1 `Overrun error in RX FIFO when frame at top of RX FIFO was received.`
3	FRAME_TOO_LONG_ERROR	R	0h	1 `Frame-length too long error in frame at top of RX FIFO.`
2	ABORT_DETECT	R	0h	1 `Abort pattern detected in frame at top of RX FIFO`
1	CRC_ERROR	R	0h	1 `CRC error in frame at top of RX FIFO. top of RX FIFO = Next frame to be read from RX FIFO`

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Table 5-2463. UART_SFLSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED0	R	0h	

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5.26.2.29 UART_TXFLL Register

5.26.2.29.1 UART_TXFLL Register (Offset = 28h) [reset = 0h]

IrDA modes only.
The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

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Table 5-2464. Instance Table

Instance Name	Physical Address
UART0	5230 0028h
UART1	5230 1028h
UART2	5230 2028h
UART3	5230 3028h
UART4	5230 4028h
UART5	5230 5028h

Figure 5-1201. UART_TXFLL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
TXFLL							
W							
0h							

Table 5-2465. UART_TXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:0	TXFLL	W	0h	LSB register used to specify the frame length

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5.26.2.30 UART_RESUME Register

5.26.2.30.1 UART_RESUME Register (Offset = 2Ch) [reset = 0h]

IR-IrDA and IR-CIR modes only.
This register is used to clear internal flags, which halt transmission/reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.

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Table 5-2466. Instance Table

Instance Name	Physical Address
UART0	5230 002Ch
UART1	5230 102Ch
UART2	5230 202Ch
UART3	5230 302Ch
UART4	5230 402Ch
UART5	5230 502Ch

Figure 5-1202. UART_RESUME Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESUME							
R							
0h							

Table 5-2467. UART_RESUME Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:0	RESUME	R	0h	Dummy read to restart the TX or RX

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5.26.2.31 UART_TXFLH Register

5.26.2.31.1 UART_TXFLH Register (Offset = 2Ch) [reset = 0h]

IrDA modes only.
The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

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Table 5-2468. Instance Table

Instance Name	Physical Address
UART0	5230 002Ch
UART1	5230 102Ch
UART2	5230 202Ch
UART3	5230 302Ch
UART4	5230 402Ch
UART5	5230 502Ch

Figure 5-1203. UART_TXFLH Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			TXFLH				
R			W				
0h			0h				

Table 5-2469. UART_TXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:5	RESERVED	R	0h	
4:0	TXFLH	W	0h	MSB register used to specify the frame length

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5.26.2.32 UART_RXFLL Register

5.26.2.32.1 UART_RXFLL Register (Offset = 30h) [reset = 0h]

IrDA modes only.
The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

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Table 5-2470. Instance Table

Instance Name	Physical Address
UART0	5230 0030h
UART1	5230 1030h
UART2	5230 2030h
UART3	5230 3030h
UART4	5230 4030h
UART5	5230 5030h

Figure 5-1204. UART_RXFLL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RXFLL							
W							
0h							

Table 5-2471. UART_RXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:0	RXFLL	W	0h	LSB register used to specify the frame length in reception

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5.26.2.33 UART_SFREGL Register

5.26.2.33.1 UART_SFREGL Register (Offset = 30h) [reset = 0h]

IrDA modes only.
The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

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Table 5-2472. Instance Table

Instance Name	Physical Address
UART0	5230 0030h
UART1	5230 1030h
UART2	5230 2030h
UART3	5230 3030h
UART4	5230 4030h
UART5	5230 5030h

Figure 5-1205. UART_SFREGL Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
SFREGL							
R							
0h							

Table 5-2473. UART_SFREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:0	SFREGL	R	0h	LSB part of the frame length

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5.26.2.34 UART_RXFLH Register

5.26.2.34.1 UART_RXFLH Register (Offset = 34h) [reset = 0h]

IrDA modes only.
The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is n bytes, then program RXFLL and RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

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Table 5-2474. Instance Table

Instance Name	Physical Address
UART0	5230 0034h
UART1	5230 1034h
UART2	5230 2034h
UART3	5230 3034h
UART4	5230 4034h
UART5	5230 5034h

Figure 5-1206. UART_RXFLH Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				RXFLH			
R				W			
0h				0h			

Table 5-2475. UART_RXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:4	RESERVED	R	0h	
3:0	RXFLH	W	0h	MSB register used to specify the frame length in reception

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5.26.2.35 UART_SFREGH Register

5.26.2.35.1 UART_SFREGH Register (Offset = 34h) [reset = 0h]

IrDA modes only.
The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

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Table 5-2476. Instance Table

Instance Name	Physical Address
UART0	5230 0034h
UART1	5230 1034h
UART2	5230 2034h
UART3	5230 3034h
UART4	5230 4034h
UART5	5230 5034h

Figure 5-1207. UART_SFREGH Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED				SFREGH			
R				R			
0h				0h			

Table 5-2477. UART_SFREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:4	RESERVED	R	0h	
3:0	SFREGH	R	0h	MSB part of the frame length

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5.26.2.36 UART_BLR Register

5.26.2.36.1 UART_BLR Register (Offset = 38h) [reset = 40h]

IrDA modes only.
Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).

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Table 5-2478. Instance Table

Instance Name	Physical Address
UART0	5230 0038h
UART1	5230 1038h
UART2	5230 2038h
UART3	5230 3038h
UART4	5230 4038h
UART5	5230 5038h

Figure 5-1208. UART_BLR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
STS_FIFO_RESET	XBOF_TYPE	RESERVED					
R/W1TS	R/W	R					
0h	1h	0h					

Table 5-2479. UART_BLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7	STS_FIFO_RESET	R/W1TS	0h	Status FIFO reset. This bit is self-clearing
6	XBOF_TYPE	R/W	1h	SIR xBOF select. 0 0xFF 1 0xC0
5:0	RESERVED	R	0h	

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5.26.2.37 UART_UASR Register

5.26.2.37.1 UART_UASR Register (Offset = 38h) [reset = 0h]

UART Autobauding Status Register.

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Table 5-2480. Instance Table

Instance Name	Physical Address
UART0	5230 0038h
UART1	5230 1038h
UART2	5230 2038h
UART3	5230 3038h
UART4	5230 4038h
UART5	5230 5038h

Figure 5-1209. UART_UASR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
NONE							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
NONE							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PARITY_TYPE		BIT_BY_CHAR	SPEED				
R		R	R				
0h		0h	0h				

Table 5-2481. UART_UASR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:6	PARITY_TYPE	R	0h	00 => No Parity identified. 01 => Parity space. 10 => Even Parity. 11 => Odd Parity
5	BIT_BY_CHAR	R	0h	0 => 7 bits character identified. 1 => 8 bits character identified
4:0	SPEED	R	0h	Used to report the speed identified. 00000 => No speed identified. 00001 => 115200 bauds. 00010 => 57600 bauds. 00011 => 38400 bauds. 00100 => 28800 bauds. 00101 => 19200 bauds. 00110 => 14400 bauds. 00111 => 9600bauds. 01000 => 4800bauds. 01001 => 2400bauds. 01010 => 1200bauds

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5.26.2.38 UART_ACREG Register

5.26.2.38.1 UART_ACREG Register (Offset = 3Ch) [reset = 0h]

IR-IrDA and IR-CIR modes only.

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Table 5-2482. Instance Table

Instance Name	Physical Address
UART0	5230 003Ch
UART1	5230 103Ch
UART2	5230 203Ch
UART3	5230 303Ch
UART4	5230 403Ch
UART5	5230 503Ch

Figure 5-1210. UART_ACREG Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PULSE_TYPE	SD_MOD	DIS_IR_RX	DIS_TX_UNDERRUN	SEND_SIP	SCTX_EN	ABORT_EN	EOT_EN
R/W	R/W	R/W	R/W	R/W1TS	R/W1TS	R/W	R/W1TS
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2483. UART_ACREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7	PULSE_TYPE	R/W	0h	SIR pulse width select: 0 3/16 of baud-rate pulse width 1 1.6us
6	SD_MOD	R/W	0h	Primary output used to configure transceivers. Connected to the SD/MODE input pin of IrDA transceivers. 0 SD pin is set to high 1 SD pin is set to low
5	DIS_IR_RX	R/W	0h	0 Normal operation (RX input automatically disabled during transmit but enabled outside of transmit operation). 1 Disables RX input (permanent state - independent of transmit).

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Table 5-2483. UART_ACREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DIS_TX_UNDERRUN	R/W	0h	It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting ACREG[4]=1, garbage data is sent over TX line. 0 Long stop bits cannot be transmitted, TX underrun is enabled 1 Long stop bits can be transmitted, TX underrun is disabled
3	SEND_SIP	R/W1TS	0h	MIR/FIR Modes only.Send Serial Infrared Interaction Pulse [SIP] If this bit is set during a MIR/FIR transmission, the SIP will be send at the end of it.This bit automatically gets cleared at the end of the SIP transmission. 0 No action 1 Send SIP pulse.
2	SCTX_EN	R/W1TS	0h	Store and controlled TX start. When MDR1[5] = 1 and the LH writes 1 to this bit the TX state machine starts frame transmission. This bit is self-clearing.
1	ABORT_EN	R/W	0h	Frame Abort. The LH can intentionally abort transmission of a frame by Writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame. If transmit FIFO is not empty and MDR1[5]=1, UART IrDA will start a new transfer with data of previous frame as soon as abort frame has been sent. Therefore, TX FIFO must be reset before sending an abort frame.
0	EOT_EN	R/W1TS	0h	EOT [end of transmission] bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit automatically gets cleared when the LH writes to the THR [TX FIFO].

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5.26.2.39 UART_SCR Register

5.26.2.39.1 UART_SCR Register (Offset = 40h) [reset = 0h]

Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.

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Table 5-2484. Instance Table

Instance Name	Physical Address
UART0	5230 0040h
UART1	5230 1040h
UART2	5230 2040h
UART3	5230 3040h
UART4	5230 4040h
UART5	5230 5040h

Figure 5-1211. UART_SCR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RX_TRIG_GRANU1	TX_TRIG_GRANU1	DSR_IT	RX_CTS_DSR_WAKE_UP_ENABLE	TX_EMPTY_CTL_IT	DMA_MODE_2		DMA_MODE_CTL
R/W	R/W	R/W	R/W	R/W	R/W		R/W
0h	0h	0h	0h	0h	0h		0h

Table 5-2485. UART_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7	RX_TRIG_GRANU1	R/W	0h	0 DISABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL. 1 ENABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL.
6	TX_TRIG_GRANU1	R/W	0h	0 DISABLES THE GRANULARITY OF 1 FOR TRIGGER TX LEVEL. 1 Enables the granularity of 1 for trigger TX level.
5	DSR_IT	R/W	0h	0 DISABLES DSR* INTERRUPT. 1 ENABLES DSR* INTERRUPT.

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Table 5-2485. UART_SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RX_CTS_DSR_WAKE_UP_ENABLE	R/W	0h	0 DISABLES THE WAKE UP INTERRUPT AND CLEARS SSR[1]. 1 Waits for a falling edge of pins RX, CTS* or DSR* to generate an interrupt
3	TX_EMPTY_CTL_IT	R/W	0h	0 Normal mode for THR interrupt (See UART mode interrupts table). 1 THE THR INTERRUPT IS GENERATED WHEN TX FIFO AND TX SHIFT REGISTER ARE EMPTY.
2:1	DMA_MODE_2	R/W	0h	Used to specify the DMA mode valid if SCR[0] = 1 0 DMA mode 0 (no DMA) 1 DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX) 2 DMA mode 2 (UART_nDMA_REQ[0] in RX) 3 DMA mode 3 (UART_nDMA_REQ[0] in TX)
0	DMA_MODE_CTL	R/W	0h	0 The DMA_MODE is set with FCR[3] 1 The DMA_MODE is set with SCR[2:1]

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5.26.2.40 UART_SSR Register

5.26.2.40.1 UART_SSR Register (Offset = 44h) [reset = 4h]

Note: Bit 1 is reset only when SCR[4] is reset to 0.

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Table 5-2486. Instance Table

Instance Name	Physical Address
UART0	5230 0044h
UART1	5230 1044h
UART2	5230 2044h
UART3	5230 3044h
UART4	5230 4044h
UART5	5230 5044h

Figure 5-1212. UART_SSR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					DMA_COUNTER_RST	RX_CTS_DSR_WAKE_UP_STS	TX_FIFO_FULL
R					R/W	R	R
0h					1h	0h	0h

Table 5-2487. UART_SSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:3	RESERVED	R	0h	
2	DMA_COUNTER_RST	R/W	1h	0 The DMA counter will not be reset if the corresponding FIFO is reset (via FCR[1] or FCR[2]) 1 The DMA counter will be reset if corresponding FIFO is reset (via FCR[1] or FCR[2])
1	RX_CTS_DSR_WAKE_UP_STS	R	0h	0 No falling edge event on RX, CTS* and DSR* 1 A falling edge occurred on RX, CTS* or DSR*
0	TX_FIFO_FULL	R	0h	0 TX FIFO is not full 1 TX FIFO is full.

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5.26.2.41 UART_EBLR Register

5.26.2.41.1 UART_EBLR Register (Offset = 48h) [reset = 0h]

IR-IrDA and IR-CIR modes only.
In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.
In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).
In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to.

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Table 5-2488. Instance Table

Instance Name	Physical Address
UART0	5230 0048h
UART1	5230 1048h
UART2	5230 2048h
UART3	5230 3048h
UART4	5230 4048h
UART5	5230 5048h

Figure 5-1213. UART_EBLR Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
EBLR							
R/W							
0h							

Table 5-2489. UART_EBLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved

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Table 5-2489. UART_EBLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	EBLR	R/W	0h	IR-IRDA mode: This register allows to define up to 176 xBOFs, the maximum required by IrDA specification. IR-CIR mode: This register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt [IIR[2]]. 0x00: feature disabled. 0x01: generate RX_STOP interrupt after receiving one zero bit. ... 0xFF: generate RX_STOP interrupt after receiving 255 zero bits.

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5.26.2.42 UART_MVR Register

5.26.2.42.1 UART_MVR Register (Offset = 50h) [reset = 47424E03h]

The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returned
Notes:
UART / IRDA SIR only module is revision 1.x (WMU_012_1 specification).
UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU_012_2 specification).
UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).
For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8

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Table 5-2490. Instance Table

Instance Name	Physical Address
UART0	5230 0050h
UART1	5230 1050h
UART2	5230 2050h
UART3	5230 3050h
UART4	5230 4050h
UART5	5230 5050h

Figure 5-1214. UART_MVR Name Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R		R		R			
1h		0h		742h			
23	22	21	20	19	18	17	16
FUNC							
R							
742h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R					R		
9h					6h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R		R					
0h		3h					

Table 5-2491. UART_MVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:30	SCHEME	R	1h	Scheme revision number of module
29:28	RESERVED	R	0h	Reserved
27:16	FUNC	R	742h	Function revision number of module
15:11	RTL	R	9h	Rtl revision number of module
10:8	MAJOR	R	6h	Major revision number of the module.
7:6	CUSTOM	R	0h	Custom revision number of the module.
5:0	MINOR	R	3h	Minor revision number of the module.

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5.26.2.43 UART_SYSC Register

5.26.2.43.1 UART_SYSC Register (Offset = 54h) [reset = 0h]

The auto idle bit controls a power saving technique to reduce the logic power consumption of the OCP interface. That is to say when the feature is enabled, the clock will be gated off until an OCP command for this device has been detected. When the software reset bit is set high it causes a full device reset.

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Table 5-2492. Instance Table

Instance Name	Physical Address
UART0	5230 0054h
UART1	5230 1054h
UART2	5230 2054h
UART3	5230 3054h
UART4	5230 4054h
UART5	5230 5054h

Figure 5-1215. UART_SYSC Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED_24							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED_24							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R			R/W		R/W	W	R/W
0h			0h		0h	0h	0h

Table 5-2493. UART_SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:5	RESERVED	R	0h	
4:3	IDLEMODE	R/W	0h	POWER MANAGEMENT REQ/ACK CONTROL REF: OCP DESIGN GUIDELINES VERSION 1.1 0 Force idle. An idle request is acknowledged unconditionally 1 No-idle. An idle request is never acknowledged. 2 Smart idle. Acknowledgement to an idle request is given based in the internal activity of the module. 3 reserved
2	ENAWAKEUP	R/W	0h	WAKE UP FEATURE CONTROL 0 Wake up is disabled 1 Wake up capability is enabled

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Table 5-2493. UART_SYSC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SOFTRESET	W	0h	Software reset. Set this bit to 1 to trigger a module reset. This bit is automatically reset by the hardware. During reads it always returns a 0. 0 Normal mode 1 The module is reset
0	AUTOIDLE	R/W	0h	Internal OCP clock gating strategy 0 Clock is running 1 Automatic OCP clock gating strategy is applied, based on the OCP interface activity

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5.26.2.44 UART_SYSS Register

5.26.2.44.1 UART_SYSS Register (Offset = 58h) [reset = 0h]

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Table 5-2494. Instance Table

Instance Name	Physical Address
UART0	5230 0058h
UART1	5230 1058h
UART2	5230 2058h
UART3	5230 3058h
UART4	5230 4058h
UART5	5230 5058h

Figure 5-1216. UART_SYSS Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R							R
0h							0h

Table 5-2495. UART_SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:1	RESERVED	R	0h	
0	RESETDONE	R	0h	Internal Reset Monitoring 0 Internal Module Reset is ongoing 1 Reset completed

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5.26.2.45 UART_WER Register

5.26.2.45.1 UART_WER Register (Offset = 5Ch) [reset = FFh]

The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.

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Table 5-2496. Instance Table

Instance Name	Physical Address
UART0	5230 005Ch
UART1	5230 105Ch
UART2	5230 205Ch
UART3	5230 305Ch
UART4	5230 405Ch
UART5	5230 505Ch

Figure 5-1217. UART_WER Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
EVENT_7_TX_WAKEUP_EN	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	EVENT_5_RHR_INTERRUPT	EVENT_4_RX_ACTIVITY	EVENT_3_DCD_CD_ACTIVITY	EVENT_2_RI_ACTIVITY	EVENT_1_DSR_ACTIVITY	EVENT_0_CTS_ACTIVITY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1h	1h	1h	1h	1h	1h	1h	1h

Table 5-2497. UART_WER Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7	EVENT_7_TX_WAKEUP_EN	R/W	1h	0 Event is not allowed to wake up the system 1 EVENT CAN WAKE UP THE SYSTEM: Event can be: THR_IT or TX_DMA request and/or TX_SATUS_IT
6	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system
5	EVENT_5_RHR_INTERRUPT	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system
4	EVENT_4_RX_ACTIVITY	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system

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Table 5-2497. UART_WER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EVENT_3_DCD_CD_ACTIVITY	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system
2	EVENT_2_RI_ACTIVITY	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system
1	EVENT_1_DSR_ACTIVITY	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system
0	EVENT_0_CTS_ACTIVITY	R/W	1h	0 Event is not allowed to wake up the system 1 Event can wake up the system

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5.26.2.46 UART_CFPS Register

5.26.2.46.1 UART_CFPS Register (Offset = 60h) [reset = 69h]

Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.

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Table 5-2498. Instance Table

Instance Name	Physical Address
UART0	5230 0060h
UART1	5230 1060h
UART2	5230 2060h
UART3	5230 3060h
UART4	5230 4060h
UART5	5230 5060h

Figure 5-1218. UART_CFPS Name Register

31	30	29	28	27	26	25	24
RESERVED_24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED_24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED_24							
R							
0h							
7	6	5	4	3	2	1	0
CFPS							
R/W							
69h							

Table 5-2499. UART_CFPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED_24	R	0h	Reserved
7:0	CFPS	R/W	69h	System clock frequency prescaler at [12x multiple]. Examples for CFPS values are given in the table below. Target Freq [KHz] CFPS [decimal] Actual Freq[KHz] 30 133 30.08 32.75 122 32.79 36 111 36.04 36.7 109 36.69 38* 105 38.1 40 100 40 56.8 70 57.14 * configured at reset to this value Note: CFPS = 0 is not supported.

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5.26.2.47 UART_RXFIFO_LVL Register

5.26.2.47.1 UART_RXFIFO_LVL Register (Offset = 64h) [reset = 0h]

Level of the RX FIFO.

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Table 5-2500. Instance Table

Instance Name	Physical Address
UART0	5230 0064h
UART1	5230 1064h
UART2	5230 2064h
UART3	5230 3064h
UART4	5230 4064h
UART5	5230 5064h

Figure 5-1219. UART_RXFIFO_LVL Name Register

31	30	29	28	27	26	25	24
RESERVED24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED24							
R							
0h							
7	6	5	4	3	2	1	0
RXFIFO_LVL							
R							
0h							

Table 5-2501. UART_RXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED24	R	0h	Reserved
7:0	RXFIFO_LVL	R	0h	

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5.26.2.48 UART_TXFIFO_LVL Register

5.26.2.48.1 UART_TXFIFO_LVL Register (Offset = 68h) [reset = 0h]

Level of the TX FIFO.

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Table 5-2502. Instance Table

Instance Name	Physical Address
UART0	5230 0068h
UART1	5230 1068h
UART2	5230 2068h
UART3	5230 3068h
UART4	5230 4068h
UART5	5230 5068h

Figure 5-1220. UART_TXFIFO_LVL Name Register

31	30	29	28	27	26	25	24
RESERVED24							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED24							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED24							
R							
0h							
7	6	5	4	3	2	1	0
TXFIFO_LVL							
R							
0h							

Table 5-2503. UART_TXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED24	R	0h	Reserved
7:0	TXFIFO_LVL	R	0h	

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5.26.2.49 UART_IER2 Register

5.26.2.49.1 UART_IER2 Register (Offset = 6Ch) [reset = 0h]

Enables RX/TX FIFOs empty corresponding interrupts.

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Table 5-2504. Instance Table

Instance Name	Physical Address
UART0	5230 006Ch
UART1	5230 106Ch
UART2	5230 206Ch
UART3	5230 306Ch
UART4	5230 406Ch
UART5	5230 506Ch

Figure 5-1221. UART_IER2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED					RHR_IT_DIS	EN_TXFIFO_EMPTY	EN_RXFIFO_EMPTY
R					R/W	R/W	R/W
0h					0h	0h	0h

Table 5-2505. UART_IER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:3	RESERVED	R	0h	
2	RHR_IT_DIS	R/W	0h	0 Enables the RHR interrupt. 1 Disables the RHR interrupt.
1	EN_TXFIFO_EMPTY	R/W	0h	Enables[1]/DISABLES[00 EN_TXFIFO_EMPTY interrupt.
0	EN_RXFIFO_EMPTY	R/W	0h	Enables[1]/disables[0] EN_RXFIFO_EMPTY interrupt.

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5.26.2.50 UART_ISR2 Register

5.26.2.50.1 UART_ISR2 Register (Offset = 70h) [reset = 3h]

Status of RX/TX FIFOs empty corresponding interrupts.

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Table 5-2506. Instance Table

Instance Name	Physical Address
UART0	5230 0070h
UART1	5230 1070h
UART2	5230 2070h
UART3	5230 3070h
UART4	5230 4070h
UART5	5230 5070h

Figure 5-1222. UART_ISR2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED						TXFIFO_EMPTY_STS	RXFIFO_EMPTY_STS
R						R/W1TC	R/W1TC
0h						1h	1h

Table 5-2507. UART_ISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	Reserved
7:2	RESERVED	R	0h	Reserved
1	TXFIFO_EMPTY_STS	R/W1TC	1h	TXFIFO interrupt pending 0 `TXFIFO_EMPTY interrupt not pending.` 1 `TXFIFO_EMPTY interrupt pending.`
0	RXFIFO_EMPTY_STS	R/W1TC	1h	RXFIFO interrupt pending 0 `RXFIFO_EMPTY interrupt not pending.` 1 `RXFIFO_EMPTY interrupt pending.`

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5.26.2.51 UART_FREQ_SEL Register

5.26.2.51.1 UART_FREQ_SEL Register (Offset = 74h) [reset = 1Ah]

Sample per bit value selector.

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Table 5-2508. Instance Table

Instance Name	Physical Address
UART0	5230 0074h
UART1	5230 1074h
UART2	5230 2074h
UART3	5230 3074h
UART4	5230 4074h
UART5	5230 5074h

Figure 5-1223. UART_FREQ_SEL Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED2							
R							
0h							
7	6	5	4	3	2	1	0
FREQ_SEL							
R/W							
1Ah							

Table 5-2509. UART_FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED2	R	0h	RESERVED
7:0	FREQ_SEL	R/W	1Ah	Sets the sample per bit if non default frequency is used. MDR3[1] must be set to 1 after this value is set. Must be equal or higher then 6.

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5.26.2.52 UART_ABAUD_1ST_CHAR Register

5.26.2.52.1 UART_ABAUD_1ST_CHAR Register (Offset = 78h) [reset = 0h]

Unused.

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Table 5-2510. Instance Table

Instance Name	Physical Address
UART0	5230 0078h
UART1	5230 1078h
UART2	5230 2078h
UART3	5230 3078h
UART4	5230 4078h
UART5	5230 5078h

Figure 5-1224. UART_ABAUD_1ST_CHAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 5-2511. UART_ABAUD_1ST_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	

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5.26.2.53 UART_BAUD_2ND_CHAR Register

5.26.2.53.1 UART_BAUD_2ND_CHAR Register (Offset = 7Ch) [reset = 0h]

Unused.

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Table 5-2512. Instance Table

Instance Name	Physical Address
UART0	5230 007Ch
UART1	5230 107Ch
UART2	5230 207Ch
UART3	5230 307Ch
UART4	5230 407Ch
UART5	5230 507Ch

Figure 5-1225. UART_BAUD_2ND_CHAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED							
R							
0h							

Table 5-2513. UART_BAUD_2ND_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	RESERVED	R	0h	

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5.26.2.54 UART_MDR3 Register

5.26.2.54.1 UART_MDR3 Register (Offset = 80h) [reset = 0h]

Mode definition register 3.

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Table 5-2514. Instance Table

Instance Name	Physical Address
UART0	5230 0080h
UART1	5230 1080h
UART2	5230 2080h
UART3	5230 3080h
UART4	5230 4080h
UART5	5230 5080h

Figure 5-1226. UART_MDR3 Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED2							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED2							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED1			DIR_EN	DIR_POL	SET_DMA_TX_THRESHOLD	NONDEFAULT_FREQ	DISABLE_CIR_RX_DEMOD
R			R/W	R/W	R/W	R/W	R/W
0h			0h	0h	0h	0h	0h

Table 5-2515. UART_MDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED2	R	0h	Reserved
7:5	RESERVED1	R	0h	Reserved
4	DIR_EN	R/W	0h	RS-485 External Transceiver Direction Enable
3	DIR_POL	R/W	0h	RS-485 External Transceiver Direction Polarity. 0 => TX: RTS=0, RX: RTS=1. 1 => TX: RTS=1, RX: RTS=0
2	SET_DMA_TX_THRESHOLD	R/W	0h	Enable to set different TX DMA threshold then 64-trigger [usage of new register TX_DNA_THRESHOLD]
1	NONDEFAULT_FREQ	R/W	0h	Enables[1]/Disables[0] using NONDEFAULT fclk frequencies
0	DISABLE_CIR_RX_DEMOD	R/W	0h	Disables[1]/Enables[0] CIR RX demodulation 0 Enables CIR RX demodulation 1 Disables CIR RX demodulation

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5.26.2.55 UART_TX_DMA_THRESHOLD Register

5.26.2.55.1 UART_TX_DMA_THRESHOLD Register (Offset = 84h) [reset = 0h]

Use to manually set the TX DMA threshold level.
MDR3[2] SET_TX_DMA_THRESHOLD must be one and
must be value + tx_trigger_level <= 64 (TX FIFO size).
If not, 64-tx_trigger_level will be used w/o modifying
the value of this register.

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Table 5-2516. Instance Table

Instance Name	Physical Address
UART0	5230 0084h
UART1	5230 1084h
UART2	5230 2084h
UART3	5230 3084h
UART4	5230 4084h
UART5	5230 5084h

Figure 5-1227. UART_TX_DMA_THRESHOLD Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		TX_DMA_THRESHOLD					
R		R/W					
0h		0h					

Table 5-2517. UART_TX_DMA_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	RESERVED
7:6	RESERVED	R	0h	Reserved
5:0	TX_DMA_THRESHOLD	R/W	0h	Use to manually set the TX DMA threshold level.

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5.26.2.56 UART_MDR4 Register

5.26.2.56.1 UART_MDR4 Register (Offset = 88h) [reset = 0h]

Mode definition register 4

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Table 5-2518. Instance Table

Instance Name	Physical Address
UART0	5230 0088h
UART1	5230 1088h
UART2	5230 2088h
UART3	5230 3088h
UART4	5230 4088h
UART5	5230 5088h

Figure 5-1228. UART_MDR4 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	MODE9	FREQ_SEL_H			MODE		
R	R/W	R/W			R/W		
0h	0h	0h			0h		

Table 5-2519. UART_MDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	RESERVED	R	0h	
6	MODE9	R/W	0h	9-bit character length. When '1', overrides character length setting in LCR
5:3	FREQ_SEL_H	R/W	0h	Upper 3 bits of FREQ_SEL register for higher division values, as required for example for FI/Di in ISO7816 mode
2:0	MODE	R/W	0h	New modes [when set, overrides MDR1 modes] 0 disabled (no override) 1 reserved 2 Synchronous mode with external clock 3 Synchronous mode with generated clock 4 ISO 7816 mode T=0 5 ISO 7816 mode T=1 6 reserved 7 reserved

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5.26.2.57 UART_EFR2 Register

5.26.2.57.1 UART_EFR2 Register (Offset = 8Ch) [reset = 0h]

Enhanced Features Register 2

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Table 5-2520. Instance Table

Instance Name	Physical Address
UART0	5230 008Ch
UART1	5230 108Ch
UART2	5230 208Ch
UART3	5230 308Ch
UART4	5230 408Ch
UART5	5230 508Ch

Figure 5-1229. UART_EFR2 Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
BROADCAST	TIMEOUT_BEHAVE	C8	C4	C2	MULTIDROP	RHR_OVERRUN	ENDIAN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0h	0h	0h	0h	0h	0h	0h	0h

Table 5-2521. UART_EFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	BROADCAST	R/W	0h	Enables broadcast address matching in multi-drop address match mode
6	TIMEOUT_BEHAVE	R/W	0h	Specifies how timeout is measured 0 `timeout after at least one character has been received` 1 `periodic timeout even when no character has been received`
5	C8	R/W	0h	Value for ISO 7816C8 pin for software control
4	C4	R/W	0h	Value for ISO 7816C4 pin for software control
3	C2	R/W	0h	Value for ISO 7816reset pin [software controllable]
2	MULTIDROP	R/W	0h	Enables parity Multi-drop mode [overrides LCR[5..3]] when '1'

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Table 5-2521. UART_EFR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RHR_OVERRUN	R/W	0h	RHR Overrun behaviour when buffer full 0 data in RHR is not overwritten (standard) 1 data in RHR is overwritten when buffer full (and FIFO disabled)
0	ENDIAN	R/W	0h	Endianness 0 Little Endian (LSB First) 1 Big Endian (MSB First)

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5.26.2.58 UART_ECR Register

5.26.2.58.1 UART_ECR Register (Offset = 90h) [reset = 18h]

Enhanced Control register.

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Table 5-2522. Instance Table

Instance Name	Physical Address
UART0	5230 0090h
UART1	5230 1090h
UART2	5230 2090h
UART3	5230 3090h
UART4	5230 4090h
UART5	5230 5090h

Figure 5-1230. UART_ECR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED1							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED1							
R							
0h							
7	6	5	4	3	2	1	0
RESERVED		CLEAR_TX_PE	TX_EN	RX_EN	TX_RST	RX_RST	A_MULTIDROP
R		W	R/W	R/W	W	W	W
0h		0h	1h	1h	0h	0h	0h

Table 5-2523. UART_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7:6	RESERVED	R	0h	
5	CLEAR_TX_PE	W	0h	Write 1 to clear parity error from the Transmitter to allow it to continue to try sending data [ISO7816 transmit only]
4	TX_EN	R/W	1h	Enables/Disables the transmitter 0 Transmitter is shut down 1 Transmitter is working
3	RX_EN	R/W	1h	Enables/Disables the receiver 0 Receiver is shut down 1 Receiver is operating
2	TX_RST	W	0h	Writing '1' resets the transmitter
1	RX_RST	W	0h	Writing '1' resets the receiver
0	A_MULTIDROP	W	0h	In multi-drop mode, when written with the value '1' causes the next byte written into THR to be transmitted with the parity bit set, signaling an address

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5.26.2.59 UART_TIMEGUARD Register

5.26.2.59.1 UART_TIMEGUARD Register (Offset = 94h) [reset = 0h]

Timeguard.

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Table 5-2524. Instance Table

Instance Name	Physical Address
UART0	5230 0094h
UART1	5230 1094h
UART2	5230 2094h
UART3	5230 3094h
UART4	5230 4094h
UART5	5230 5094h

Figure 5-1231. UART_TIMEGUARD Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEGUARD							
R/W							
0h							

Table 5-2525. UART_TIMEGUARD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEGUARD	R/W	0h	Specifies the amount of idle baud clocks [transmitter bit period] to insert between transmitted bytes, useful when comunicating with slower devices

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5.26.2.60 UART_TIMEOUTL Register

5.26.2.60.1 UART_TIMEOUTL Register (Offset = 98h) [reset = 0h]

Timeout lower byte.

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Table 5-2526. Instance Table

Instance Name	Physical Address
UART0	5230 0098h
UART1	5230 1098h
UART2	5230 2098h
UART3	5230 3098h
UART4	5230 4098h
UART5	5230 5098h

Figure 5-1232. UART_TIMEOUTL Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEOUT_L							
R/W							
0h							

Table 5-2527. UART_TIMEOUTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEOUT_L	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Lower byte of the 16 bit value]

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5.26.2.61 UART_TIMEOUTH Register

5.26.2.61.1 UART_TIMEOUTH Register (Offset = 9Ch) [reset = 0h]

Timeout higher byte.

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Table 5-2528. Instance Table

Instance Name	Physical Address
UART0	5230 009Ch
UART1	5230 109Ch
UART2	5230 209Ch
UART3	5230 309Ch
UART4	5230 409Ch
UART5	5230 509Ch

Figure 5-1233. UART_TIMEOUTH Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							
R							
0h							
7	6	5	4	3	2	1	0
TIMEOUT_H							
R/W							
0h							

Table 5-2529. UART_TIMEOUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	R	0h	
7:0	TIMEOUT_H	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Higher byte of the 16 bit value]

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5.26.2.62 UART_SCCR Register

5.26.2.62.1 UART_SCCR Register (Offset = A0h) [reset = 7h]

Smartcard (ISO7816) mode Control Register.

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Table 5-2530. Instance Table

Instance Name	Physical Address
UART0	5230 00A0h
UART1	5230 10A0h
UART2	5230 20A0h
UART3	5230 30A0h
UART4	5230 40A0h
UART5	5230 50A0h

Figure 5-1234. UART_SCCR Name Register

31	30	29	28	27	26	25	24
RESERVED1							
R							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED1							
R							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED1							
R							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DSNACK	INACK	RESERVED			MAX_ITERATION		
R/W	R/W	R			R/W		
0h	0h	0h			7h		

Table 5-2531. UART_SCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED1	R	0h	
7	DSNACK	R/W	0h	Applies Max_Iteration to receiver aswell - when maximum number of NACKs have been returned, the receiver will accept the data regardless of error. The data will be loaded into the receiver FIFO and PE will be set when Reading it.
6	INACK	R/W	0h	Inhibit NACK when receiving, even if an error is received. The data will be loaded into the receiver FIFO and PE will be set when Reading it.
5:3	RESERVED	R	0h	
2:0	MAX_ITERATION	R/W	7h	Number of times to repeat transmitted character, if the receiver did not acknowledge. If not acknowledged after the max value is reached, the UART transmitter will set parity error, stop and not continue until it is cleared.

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5.26.2.63 UART_ERHR Register

5.26.2.63.1 UART_ERHR Register (Offset = A4h) [reset = 0h]

Extended Receive Holding Register.

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Table 5-2532. Instance Table

Instance Name	Physical Address
UART0	5230 00A4h
UART1	5230 10A4h
UART2	5230 20A4h
UART3	5230 30A4h
UART4	5230 40A4h
UART5	5230 50A4h

Figure 5-1235. UART_ERHR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							ERHR
R							R
0h							0h
7	6	5	4	3	2	1	0
ERHR							
R							
0h							

Table 5-2533. UART_ERHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	R	0h	
8:0	ERHR	R	0h	Extended Receive Holding Register - allows accessing the full 9bit RHR

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5.26.2.64 UART_ETHR Register

5.26.2.64.1 UART_ETHR Register (Offset = A4h) [reset = 0h]

Extended Transmit Holding Register.

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Table 5-2534. Instance Table

Instance Name	Physical Address
UART0	5230 00A4h
UART1	5230 10A4h
UART2	5230 20A4h
UART3	5230 30A4h
UART4	5230 40A4h
UART5	5230 50A4h

Figure 5-1236. UART_ETHR Name Register

31	30	29	28	27	26	25	24
RESERVED							
R							
0h							
23	22	21	20	19	18	17	16
RESERVED							
R							
0h							
15	14	13	12	11	10	9	8
RESERVED							ETHR
R							W
0h							0h
7	6	5	4	3	2	1	0
ETHR							
W							
0h							

Table 5-2535. UART_ETHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:9	RESERVED	R	0h	
8:0	ETHR	W	0h	Extended Transmit Holding Register - allows Writing the full 9bit RHR

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5.26.2.65 UART_MAR Register

5.26.2.65.1 UART_MAR Register (Offset = A8h) [reset = 0h]

Multidrop Address Register.

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Table 5-2536. Instance Table

Instance Name	Physical Address
UART0	5230 00A8h
UART1	5230 10A8h
UART2	5230 20A8h
UART3	5230 30A8h
UART4	5230 40A8h
UART5	5230 50A8h

Figure 5-1237. UART_MAR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
ADDRESS							
R/W							
0h							

Table 5-2537. UART_MAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	ADDRESS	R/W	0h	Multidrop match address value

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5.26.2.66 UART_MMR Register

5.26.2.66.1 UART_MMR Register (Offset = ACh) [reset = 0h]

Multidrop Mask Register.

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Table 5-2538. Instance Table

Instance Name	Physical Address
UART0	5230 00ACh
UART1	5230 10ACh
UART2	5230 20ACh
UART3	5230 30ACh
UART4	5230 40ACh
UART5	5230 50ACh

Figure 5-1238. UART_MMR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
MASK							
R/W							
0h							

Table 5-2539. UART_MMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	MASK	R/W	0h	Address match masking value ? Writing a 0 to a bit means that the corresponding address bit will be ignored in matching

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5.26.2.67 UART_MBR Register

5.26.2.67.1 UART_MBR Register (Offset = B0h) [reset = 0h]

Multidrop Broadcast Address Register.

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Table 5-2540. Instance Table

Instance Name	Physical Address
UART0	5230 00B0h
UART1	5230 10B0h
UART2	5230 20B0h
UART3	5230 30B0h
UART4	5230 40B0h
UART5	5230 50B0h

Figure 5-1239. UART_MBR Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED							
NONE							
0h							
7	6	5	4	3	2	1	0
BROADCAST_ADDRESS							
R/W							
0h							

Table 5-2541. UART_MBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:8	RESERVED	NONE	0h	Reserved
7:0	BROADCAST_ADDRESS	R/W	0h	Broadcast address for address matching

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5.27 WDT

WDT

5.27.1 WDT Summaries

WDT Summaries

Table 5-2542. WDT Registers, Base Address=5210 0000h, Length=256

Offset	Length	Register Name	WDT0 Physical Address	WDT1 Physical Address	WDT2 Physical Address
0h	32	WDT_RTIGCTRL	5210 0000h	5210 1000h	5210 2000h
4h	32	WDT_RTITBCTRL	5210 0004h	5210 1004h	5210 2004h
8h	32	WDT_RTICAPCTRL	5210 0008h	5210 1008h	5210 2008h
Ch	32	WDT_RTICOMPCTRL	5210 000Ch	5210 100Ch	5210 200Ch
10h	32	WDT_RTIFRC0	5210 0010h	5210 1010h	5210 2010h
14h	32	WDT_RTIUC0	5210 0014h	5210 1014h	5210 2014h
18h	32	WDT_RTICPUC0	5210 0018h	5210 1018h	5210 2018h
20h	32	WDT_RTICAFRC0	5210 0020h	5210 1020h	5210 2020h
24h	32	WDT_RTICAUC0	5210 0024h	5210 1024h	5210 2024h
30h	32	WDT_RTIFRC1	5210 0030h	5210 1030h	5210 2030h
34h	32	WDT_RTIUC1	5210 0034h	5210 1034h	5210 2034h
38h	32	WDT_RTICPUC1	5210 0038h	5210 1038h	5210 2038h
40h	32	WDT_RTICAFRC1	5210 0040h	5210 1040h	5210 2040h
44h	32	WDT_RTICAUC1	5210 0044h	5210 1044h	5210 2044h
50h	32	WDT_RTICOMP0	5210 0050h	5210 1050h	5210 2050h
54h	32	WDT_RTIUDCP0	5210 0054h	5210 1054h	5210 2054h
58h	32	WDT_RTICOMP1	5210 0058h	5210 1058h	5210 2058h
5Ch	32	WDT_RTIUDCP1	5210 005Ch	5210 105Ch	5210 205Ch
60h	32	WDT_RTICOMP2	5210 0060h	5210 1060h	5210 2060h
64h	32	WDT_RTIUDCP2	5210 0064h	5210 1064h	5210 2064h
68h	32	WDT_RTICOMP3	5210 0068h	5210 1068h	5210 2068h
6Ch	32	WDT_RTIUDCP3	5210 006Ch	5210 106Ch	5210 206Ch
70h	32	WDT_RTITBLCOMP	5210 0070h	5210 1070h	5210 2070h
74h	32	WDT_RTITBHCOMP	5210 0074h	5210 1074h	5210 2074h
80h	32	WDT_RTISETINT	5210 0080h	5210 1080h	5210 2080h
84h	32	WDT_RTICLEARINT	5210 0084h	5210 1084h	5210 2084h
88h	32	WDT_RTIINTFLAG	5210 0088h	5210 1088h	5210 2088h
90h	32	WDT_RTIDWDCTRL	5210 0090h	5210 1090h	5210 2090h
94h	32	WDT_RTIDWDPRLD	5210 0094h	5210 1094h	5210 2094h
98h	32	WDT_RTIWDSTATUS	5210 0098h	5210 1098h	5210 2098h
9Ch	32	WDT_RTIWDKEY	5210 009Ch	5210 109Ch	5210 209Ch
A0h	32	WDT_RTIDWDCNTR	5210 00A0h	5210 10A0h	5210 20A0h
A4h	32	WDT_RTIWWDRXNCTRL	5210 00A4h	5210 10A4h	5210 20A4h
A8h	32	WDT_RTIWWDSIZECTRL	5210 00A8h	5210 10A8h	5210 20A8h
ACh	32	WDT_RTIINTCLRENABLE	5210 00ACh	5210 10ACh	5210 20ACh
B0h	32	WDT_RTICOMP0CLR	5210 00B0h	5210 10B0h	5210 20B0h
B4h	32	WDT_RTICOMP1CLR	5210 00B4h	5210 10B4h	5210 20B4h
B8h	32	WDT_RTICOMP2CLR	5210 00B8h	5210 10B8h	5210 20B8h
BCh	32	WDT_RTICOMP3CLR	5210 00BCh	5210 10BCh	5210 20BCh

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Table 5-2543. WDT Registers, Base Address=5210 0000h, Length=256

Offset	Length	Register Name	WDT3 Physical Address
0h	32	WDT_RTIGCTRL	5210 3000h
4h	32	WDT_RTITBCTRL	5210 3004h
8h	32	WDT_RTICAPCTRL	5210 3008h
Ch	32	WDT_RTICOMPCTRL	5210 300Ch
10h	32	WDT_RTIFRC0	5210 3010h
14h	32	WDT_RTIUC0	5210 3014h
18h	32	WDT_RTICPUC0	5210 3018h
20h	32	WDT_RTICAFRC0	5210 3020h
24h	32	WDT_RTICAUC0	5210 3024h
30h	32	WDT_RTIFRC1	5210 3030h
34h	32	WDT_RTIUC1	5210 3034h
38h	32	WDT_RTICPUC1	5210 3038h
40h	32	WDT_RTICAFRC1	5210 3040h
44h	32	WDT_RTICAUC1	5210 3044h
50h	32	WDT_RTICOMP0	5210 3050h
54h	32	WDT_RTIUDCP0	5210 3054h
58h	32	WDT_RTICOMP1	5210 3058h
5Ch	32	WDT_RTIUDCP1	5210 305Ch
60h	32	WDT_RTICOMP2	5210 3060h
64h	32	WDT_RTIUDCP2	5210 3064h
68h	32	WDT_RTICOMP3	5210 3068h
6Ch	32	WDT_RTIUDCP3	5210 306Ch
70h	32	WDT_RTITBLCOMP	5210 3070h
74h	32	WDT_RTITBHCOMP	5210 3074h
80h	32	WDT_RTISETINT	5210 3080h
84h	32	WDT_RTICLEARINT	5210 3084h
88h	32	WDT_RTIINTFLAG	5210 3088h
90h	32	WDT_RTIDWDCTRL	5210 3090h
94h	32	WDT_RTIDWDPRLD	5210 3094h
98h	32	WDT_RTIWDSTATUS	5210 3098h
9Ch	32	WDT_RTIWDKEY	5210 309Ch
A0h	32	WDT_RTIDWDCNTR	5210 30A0h
A4h	32	WDT_RTIWWDRXNCTRL	5210 30A4h
A8h	32	WDT_RTIWWDSIZECTRL	5210 30A8h
ACh	32	WDT_RTIINTCLRENABLE	5210 30ACh
B0h	32	WDT_RTICOMP0CLR	5210 30B0h
B4h	32	WDT_RTICOMP1CLR	5210 30B4h
B8h	32	WDT_RTICOMP2CLR	5210 30B8h
BCh	32	WDT_RTICOMP3CLR	5210 30BCh

5.27.2 WDT Registers

WDT Registers

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5.27.2.1 WDT_RTIGCTRL Register

5.27.2.1.1 WDT_RTIGCTRL Register (Offset = 0h) [reset = 0h]

Global Control Register starts / stops the counters .

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Table 5-2544. Instance Table

Instance Name	Physical Address
WDT0	5210 0000h
WDT1	5210 1000h
WDT2	5210 2000h
WDT3	5210 3000h

Figure 5-1240. WDT_RTIGCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED2							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED2				NTUSEL			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
COS	RESERVED1						
R/W	R/W						
0h	0h						
7	6	5	4	3	2	1	0
RESERVED1						CNT1EN	CNT0EN
R/W						R/W	R/W
0h						0h	0h

Table 5-2545. WDT_RTIGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:20	RESERVED2	R/W	0h	Reserved. Reads return 0 and writes have no effect
19:16	NTUSEL	R/W	0h	NTUSEL: Select NTU signal. These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL. User and privilege mode [read]: 0000= NTU0 0101= NTU1 1010= NTU2 1111= NTU3 other = tied to 0 Privilege mode [write]: 0000= NTU0 0101= NTU1 1010= NTU2 1111= NTU3 other = tied to 0

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Table 5-2545. WDT_RTIGCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	COS	R/W	0h	COS: Continue On Suspend. This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting. User and privilege mode [read]: 0 = counters are stopped while in debug mode 1 = counters are running while in debug mode Privilege mode [write]: 0 = stop counters in debug mode 1 = continue counting in debug mode
14:2	RESERVED1	R/W	0h	Reserved. Reads return 0 and writes have no effect
1	CNT1EN	R/W	0h	CNT1EN: Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 [UC1 and FRC1]. User and privilege mode [read]: 0 = counters are stopped 1 = counters are running Privilege mode [write]: 0 = stop counters 1 = start counters Gives the absolute 32 bit destination address [physical].
0	CNT0EN	R/W	0h	CNT0EN: Counter 0 Enable.The CNT0EN bit starts and stops the operation of counter block 0 [UC0 and FRC0]. User and privilege mode [read]: 0 = counters are stopped 1 = counters are running Privilege mode [write]: 0 = stop counters 1 = start counters Gives the absolute 32 bits source address [physical].

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5.27.2.2 WDT_RTITBCTRL Register

5.27.2.2.1 WDT_RTITBCTRL Register (Offset = 4h) [reset = 0h]

Timebase Control selection which source triggers free running counter 0 .

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Table 5-2546. Instance Table

Instance Name	Physical Address
WDT0	5210 0004h
WDT1	5210 1004h
WDT2	5210 2004h
WDT3	5210 3004h

Figure 5-1241. WDT_RTITBCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED3							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED3							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED3							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED3						INC	TBEXT
R/W						R/W	R/W
0h						0h	0h

Table 5-2547. WDT_RTITBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED3	R/W	0h	Reserved
1	INC	R/W	0h	INC: Increment Free Running Counter 0. This bit determines wether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected. User and privilege mode [read]: 0 = FRC0 will not be incremented 1 = FRC0 will be incremented Privilege mode [write]: 0 = Do not increment FRC0 on failing external clock 1 = Increment FRC0 on failing external clock

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Table 5-2547. WDT_RTITBCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TBEXT	R/W	0h	TBEXT: Timebase External. The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurence. The only source which is able to increment Free Running Counter 0 is NTUx. When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset. The selection if the external signal should be used, can only be done by software. User and privilege mode [read]: 0 = UC0 clocks FRC0 1 = NTUx clocks FRC0 Privilege mode [write]: 0 = MUX is switched to internal UC0 clocking scheme 1 = MUX is switched to external NTUx clocking scheme

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5.27.2.3 WDT_RTICAPCTRL Register

5.27.2.3.1 WDT_RTICAPCTRL Register (Offset = 8h) [reset = 0h]

Capture Control controls the capture source for the counters.

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Table 5-2548. Instance Table

Instance Name	Physical Address
WDT0	5210 0008h
WDT1	5210 1008h
WDT2	5210 2008h
WDT3	5210 3008h

Figure 5-1242. WDT_RTICAPCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED4							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED4							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED4							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED4						CAPCNTR1	CAPCNTR0
R/W						R/W	R/W
0h						0h	0h

Table 5-2549. WDT_RTICAPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:2	RESERVED4	R/W	0h	Reserved. Reads return 0 and writes have no effect
1	CAPCNTR1	R/W	0h	CAPCNTR1: Capture Counter 1. This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1. User and privilege mode [read]: 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode [write]: 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1

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Table 5-2549. WDT_RTICAPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CAPCNTR0	R/W	0h	CAPCNTR0: Capture Counter 0. This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0. User and privilege mode [read]: 0 = capture event is triggered by Capture Event Source 0 1 = capture event is triggered by Capture Event Source 1 Privilege mode [write]: 0 = enable capture event triggered by Capture Event Source 0 1 = enable capture event triggered by Capture Event Source 1 11 indexed 10 reserved 01 post-increment 00 constant

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5.27.2.4 WDT_RTICOMPCTRL Register

5.27.2.4.1 WDT_RTICOMPCTRL Register (Offset = Ch) [reset = 0h]

Compare Control controls the source for the compare registers.

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Table 5-2550. Instance Table

Instance Name	Physical Address
WDT0	5210 000Ch
WDT1	5210 100Ch
WDT2	5210 200Ch
WDT3	5210 300Ch

Figure 5-1243. WDT_RTICOMPCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED8							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED8							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED8			COMP3SEL	RESERVED7			COMP2SEL
R/W			R/W	R/W			R/W
0h			0h	0h			0h
7	6	5	4	3	2	1	0
RESERVED6			COMP1SEL	RESERVED5			COMP0SEL
R/W			R/W	R/W			R/W
0h			0h	0h			0h

Table 5-2551. WDT_RTICOMPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:13	RESERVED8	R/W	0h	Reserved. Reads return 0 and writes have no effect
12	COMP3SEL	R/W	0h	COMPSEL3: Compare Select 3. This bit determines the counter with which the compare value hold in compare register 3 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
11:9	RESERVED7	R/W	0h	Reserved. Reads return 0 and writes have no effect
8	COMP2SEL	R/W	0h	COMPSEL2: Compare Select 2. This bit determines the counter with which the compare value hold in compare register 2 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1

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Table 5-2551. WDT_RTICOMPCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:5	RESERVED6	R/W	0h	Reserved. Reads return 0 and writes have no effect
4	COMP1SEL	R/W	0h	COMPSEL1: Compare Select 1. This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1
3:1	RESERVED5	R/W	0h	Reserved. Reads return 0 and writes have no effect
0	COMP0SEL	R/W	0h	COMPSEL0: Compare Select 0. This bit determines the counter with which the compare value hold in compare register 0 is compared. User and privilege mode [read]: 0 = value will be compared with FRC 0 1 = value will be compared with FRC 1 Privilege mode [write]: 0 = enable compare with FRC 0 1 = enable compare with FRC 1

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5.27.2.5 WDT_RTIFRC0 Register

5.27.2.5.1 WDT_RTIFRC0 Register (Offset = 10h) [reset = 0h]

Free Running Counter 0 current value of free running counter 0

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Table 5-2552. Instance Table

Instance Name	Physical Address
WDT0	5210 0010h
WDT1	5210 1010h
WDT2	5210 2010h
WDT3	5210 3010h

Figure 5-1244. WDT_RTIFRC0 Name Register

31	30	29	28	27	26	25	24
FRC0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FRC0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FRC0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FRC0							
R/W							
0h							

Table 5-2553. WDT_RTIFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC0	R/W	0h	FRC0: Free Running Counter 0. This registers holds the current value of the Free Running Counter 0 and will be updated continuously. User and privilege mode [read]: current value of the counter Privilege mode [write]: The counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.

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5.27.2.6 WDT_RTIUC0 Register

5.27.2.6.1 WDT_RTIUC0 Register (Offset = 14h) [reset = 0h]

Up Counter 0 current value of prescale counter 0

Return to Summary Table

Table 5-2554. Instance Table

Instance Name	Physical Address
WDT0	5210 0014h
WDT1	5210 1014h
WDT2	5210 2014h
WDT3	5210 3014h

Figure 5-1245. WDT_RTIUC0 Name Register

31	30	29	28	27	26	25	24
UC0							
R/W							
0h							
23	22	21	20	19	18	17	16
UC0							
R/W							
0h							
15	14	13	12	11	10	9	8
UC0							
R/W							
0h							
7	6	5	4	3	2	1	0
UC0							
R/W							
0h							

Table 5-2555. WDT_RTIUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC0	R/W	0h	UC0: Up Counter 0. This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0. User and privilege mode [read]: value of the counter when the Free Running Counter 0 was read Privilege mode [write]: the counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.

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5.27.2.7 WDT_RTICPUC0 Register

5.27.2.7.1 WDT_RTICPUC0 Register (Offset = 18h) [reset = 0h]

Compare Up Counter 0 compare value compared with prescale counter 0

Return to Summary Table

Table 5-2556. Instance Table

Instance Name	Physical Address
WDT0	5210 0018h
WDT1	5210 1018h
WDT2	5210 2018h
WDT3	5210 3018h

Figure 5-1246. WDT_RTICPUC0 Name Register

31	30	29	28	27	26	25	24
CPUC0							
R/W							
0h							
23	22	21	20	19	18	17	16
CPUC0							
R/W							
0h							
15	14	13	12	11	10	9	8
CPUC0							
R/W							
0h							
7	6	5	4	3	2	1	0
CPUC0							
R/W							
0h							

Table 5-2557. WDT_RTICPUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC0	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock. If CPUC0 = 0:then, frequency = RTICLK/ [2^32] If CPUC0 0:then , frequency = RTICLK/[CPUC0 + 1] User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed

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5.27.2.8 WDT_RTICAFRC0 Register

5.27.2.8.1 WDT_RTICAFRC0 Register (Offset = 20h) [reset = 0h]

Capture Free Running Counter 0 current value of free running counter 0 on external event.

Return to Summary Table

Table 5-2558. Instance Table

Instance Name	Physical Address
WDT0	5210 0020h
WDT1	5210 1020h
WDT2	5210 2020h
WDT3	5210 3020h

Figure 5-1247. WDT_RTICAFRC0 Name Register

31	30	29	28	27	26	25	24
CAFRC0							
R/W							
0h							
23	22	21	20	19	18	17	16
CAFRC0							
R/W							
0h							
15	14	13	12	11	10	9	8
CAFRC0							
R/W							
0h							
7	6	5	4	3	2	1	0
CAFRC0							
R/W							
0h							

Table 5-2559. WDT_RTICAFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC0	R/W	0h	CAFRC0: Capture Free Running Counter 0. This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block. User and privilege mode [read]: value of Free Running Counter 0 on a capture event

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5.27.2.9 WDT_RTICAUC0 Register

5.27.2.9.1 WDT_RTICAUC0 Register (Offset = 24h) [reset = 0h]

Capture Up Counter 0 current value of prescale counter 0 on external event.

Return to Summary Table

Table 5-2560. Instance Table

Instance Name	Physical Address
WDT0	5210 0024h
WDT1	5210 1024h
WDT2	5210 2024h
WDT3	5210 3024h

Figure 5-1248. WDT_RTICAUC0 Name Register

31	30	29	28	27	26	25	24
CAUC0							
R/W							
0h							
23	22	21	20	19	18	17	16
CAUC0							
R/W							
0h							
15	14	13	12	11	10	9	8
CAUC0							
R/W							
0h							
7	6	5	4	3	2	1	0
CAUC0							
R/W							
0h							

Table 5-2561. WDT_RTICAUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC0	R/W	0h	CAUC0: Capture Up Counter 0. This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode [read]: value of Up Counter 0 on a capture event

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5.27.2.10 WDT_RTIFRC1 Register

5.27.2.10.1 WDT_RTIFRC1 Register (Offset = 30h) [reset = 0h]

Free Running Counter 1 current value of free running counter 1

Return to Summary Table

Table 5-2562. Instance Table

Instance Name	Physical Address
WDT0	5210 0030h
WDT1	5210 1030h
WDT2	5210 2030h
WDT3	5210 3030h

Figure 5-1249. WDT_RTIFRC1 Name Register

31	30	29	28	27	26	25	24
FRC1							
R/W							
0h							
23	22	21	20	19	18	17	16
FRC1							
R/W							
0h							
15	14	13	12	11	10	9	8
FRC1							
R/W							
0h							
7	6	5	4	3	2	1	0
FRC1							
R/W							
0h							

Table 5-2563. WDT_RTIFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	FRC1	R/W	0h	FRC1: Free Running Counter 1. This registers holds the current value of the Free Running Counter 1 and will be updated continuously. User and privilege mode [read]: current value of the counter Privilege mode [write]: The counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.

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5.27.2.11 WDT_RTIUC1 Register

5.27.2.11.1 WDT_RTIUC1 Register (Offset = 34h) [reset = 0h]

Up Counter 1 current value of prescale counter 1

Return to Summary Table

Table 5-2564. Instance Table

Instance Name	Physical Address
WDT0	5210 0034h
WDT1	5210 1034h
WDT2	5210 2034h
WDT3	5210 3034h

Figure 5-1250. WDT_RTIUC1 Name Register

31	30	29	28	27	26	25	24
UC1							
R/W							
0h							
23	22	21	20	19	18	17	16
UC1							
R/W							
0h							
15	14	13	12	11	10	9	8
UC1							
R/W							
0h							
7	6	5	4	3	2	1	0
UC1							
R/W							
0h							

Table 5-2565. WDT_RTIUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UC1	R/W	0h	UC1: Up Counter 1. This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1. User and privilege mode [read]: value of the counter when the Free Running Counter 1 was read Privilege mode [write]: the counter can be preset by Writing to this register. The counter increments then from this written value upwards. Note: Presetting counters If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1. Note: Preset value concern If the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since RTIUC1 has to count up until it overflows.

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5.27.2.12 WDT_RTICPUC1 Register

5.27.2.12.1 WDT_RTICPUC1 Register (Offset = 38h) [reset = 0h]

Compare Up Counter 1 compare value compared with prescale counter 1

Return to Summary Table

Table 5-2566. Instance Table

Instance Name	Physical Address
WDT0	5210 0038h
WDT1	5210 1038h
WDT2	5210 2038h
WDT3	5210 3038h

Figure 5-1251. WDT_RTICPUC1 Name Register

31	30	29	28	27	26	25	24
CPUC1							
R/W							
0h							
23	22	21	20	19	18	17	16
CPUC1							
R/W							
0h							
15	14	13	12	11	10	9	8
CPUC1							
R/W							
0h							
7	6	5	4	3	2	1	0
CPUC1							
R/W							
0h							

Table 5-2567. WDT_RTICPUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CPUC1	R/W	0h	This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock. If CPUC1 = 0:then, frequency = RTICLK/ [2^32] If CPUC1 0:then , frequency = RTICLK/[CPUC1 + 1] User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed

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5.27.2.13 WDT_RTICAFRC1 Register

5.27.2.13.1 WDT_RTICAFRC1 Register (Offset = 40h) [reset = 0h]

Capture Free Running Counter 1 current value of free running counter 1 on external event.

Return to Summary Table

Table 5-2568. Instance Table

Instance Name	Physical Address
WDT0	5210 0040h
WDT1	5210 1040h
WDT2	5210 2040h
WDT3	5210 3040h

Figure 5-1252. WDT_RTICAFRC1 Name Register

31	30	29	28	27	26	25	24
CAFRC1							
R/W							
0h							
23	22	21	20	19	18	17	16
CAFRC1							
R/W							
0h							
15	14	13	12	11	10	9	8
CAFRC1							
R/W							
0h							
7	6	5	4	3	2	1	0
CAFRC1							
R/W							
0h							

Table 5-2569. WDT_RTICAFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAFRC1	R/W	0h	CAFRC1: Capture Free Running Counter 1. This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block. User and privilege mode [read]: value of Free Running Counter 1 on a capture event

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5.27.2.14 WDT_RTICAUC1 Register

5.27.2.14.1 WDT_RTICAUC1 Register (Offset = 44h) [reset = 0h]

Capture Up Counter 1 current value of prescale counter 1 on external event.

Return to Summary Table

Table 5-2570. Instance Table

Instance Name	Physical Address
WDT0	5210 0044h
WDT1	5210 1044h
WDT2	5210 2044h
WDT3	5210 3044h

Figure 5-1253. WDT_RTICAUC1 Name Register

31	30	29	28	27	26	25	24
CAUC1							
R/W							
0h							
23	22	21	20	19	18	17	16
CAUC1							
R/W							
0h							
15	14	13	12	11	10	9	8
CAUC1							
R/W							
0h							
7	6	5	4	3	2	1	0
CAUC1							
R/W							
0h							

Table 5-2571. WDT_RTICAUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	CAUC1	R/W	0h	CAUC1: Capture Up Counter 1. This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC1 register is the corresponding value to the RTICAFRC1 register, even if another capture event happens in between the two reads. User and privilege mode [read]: value of Up Counter 1 on a capture event

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5.27.2.15 WDT_RTICOMP0 Register

5.27.2.15.1 WDT_RTICOMP0 Register (Offset = 50h) [reset = 0h]

Compare 0 compare value to be compared with the counters.

Return to Summary Table

Table 5-2572. Instance Table

Instance Name	Physical Address
WDT0	5210 0050h
WDT1	5210 1050h
WDT2	5210 2050h
WDT3	5210 3050h

Figure 5-1254. WDT_RTICOMP0 Name Register

31	30	29	28	27	26	25	24
COMP0							
R/W							
0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
COMP0							
R/W							
0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
COMP0							
R/W							
0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMP0							
R/W							
0h							

Table 5-2573. WDT_RTICOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0	R/W	0h	COMP0: Compare 0. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.27.2.16 WDT_RTIUDCP0 Register

5.27.2.16.1 WDT_RTIUDCP0 Register (Offset = 54h) [reset = 0h]

Update Compare 0 value to be added to the compare register 0 value on compare match.

Return to Summary Table

Table 5-2574. Instance Table

Instance Name	Physical Address
WDT0	5210 0054h
WDT1	5210 1054h
WDT2	5210 2054h
WDT3	5210 3054h

Figure 5-1255. WDT_RTIUDCP0 Name Register

31	30	29	28	27	26	25	24
UDCP0							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP0							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP0							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP0							
R/W							
0h							

Table 5-2575. WDT_RTIUDCP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP0	R/W	0h	UDCP0: Update Compare 0 Register. This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 0 register on the next compare match Privilege mode [write]: new update value

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5.27.2.17 WDT_RTICOMP1 Register

5.27.2.17.1 WDT_RTICOMP1 Register (Offset = 58h) [reset = 0h]

Compare 1 compare value to be compared with the counters.

Return to Summary Table

Table 5-2576. Instance Table

Instance Name	Physical Address
WDT0	5210 0058h
WDT1	5210 1058h
WDT2	5210 2058h
WDT3	5210 3058h

Figure 5-1256. WDT_RTICOMP1 Name Register

31	30	29	28	27	26	25	24
COMP1							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP1							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP1							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP1							
R/W							
0h							

Table 5-2577. WDT_RTICOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1	R/W	0h	COMP1: compare1. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.27.2.18 WDT_RTIUDCP1 Register

5.27.2.18.1 WDT_RTIUDCP1 Register (Offset = 5Ch) [reset = 0h]

Update Compare 1 value to be added to the compare register 1 value on compare match.

Return to Summary Table

Table 5-2578. Instance Table

Instance Name	Physical Address
WDT0	5210 005Ch
WDT1	5210 105Ch
WDT2	5210 205Ch
WDT3	5210 305Ch

Figure 5-1257. WDT_RTIUDCP1 Name Register

31	30	29	28	27	26	25	24
UDCP1							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP1							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP1							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP1							
R/W							
0h							

Table 5-2579. WDT_RTIUDCP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP1	R/W	0h	UDCP1: Update compare1 Register. This registers holds a value, which is added to the value in the compare1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare1 register on the next compare match Privilege mode [write]: new update value

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5.27.2.19 WDT_RTICOMP2 Register

5.27.2.19.1 WDT_RTICOMP2 Register (Offset = 60h) [reset = 0h]

Compare 2 compare value to be compared with the counters.

Return to Summary Table

Table 5-2580. Instance Table

Instance Name	Physical Address
WDT0	5210 0060h
WDT1	5210 1060h
WDT2	5210 2060h
WDT3	5210 3060h

Figure 5-1258. WDT_RTICOMP2 Name Register

31	30	29	28	27	26	25	24
COMP2							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP2							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP2							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP2							
R/W							
0h							

Table 5-2581. WDT_RTICOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2	R/W	0h	COMP2: compare 2. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.27.2.20 WDT_RTIUDCP2 Register

5.27.2.20.1 WDT_RTIUDCP2 Register (Offset = 64h) [reset = 0h]

Update Compare 2 value to be added to the compare register 2 value on compare match.

Return to Summary Table

Table 5-2582. Instance Table

Instance Name	Physical Address
WDT0	5210 0064h
WDT1	5210 1064h
WDT2	5210 2064h
WDT3	5210 3064h

Figure 5-1259. WDT_RTIUDCP2 Name Register

31	30	29	28	27	26	25	24
UDCP2							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP2							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP2							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP2							
R/W							
0h							

Table 5-2583. WDT_RTIUDCP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP2	R/W	0h	UDCP2: Update compare 2 Register. This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 2 register on the next compare match Privilege mode [write]: new update value

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5.27.2.21 WDT_RTICOMP3 Register

5.27.2.21.1 WDT_RTICOMP3 Register (Offset = 68h) [reset = 0h]

Compare 3 compare value to be compared with the counters.

Return to Summary Table

Table 5-2584. Instance Table

Instance Name	Physical Address
WDT0	5210 0068h
WDT1	5210 1068h
WDT2	5210 2068h
WDT3	5210 3068h

Figure 5-1260. WDT_RTICOMP3 Name Register

31	30	29	28	27	26	25	24
COMP3							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP3							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP3							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP3							
R/W							
0h							

Table 5-2585. WDT_RTICOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3	R/W	0h	COMP3: compare 3. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.27.2.22 WDT_RTIUDCP3 Register

5.27.2.22.1 WDT_RTIUDCP3 Register (Offset = 6Ch) [reset = 0h]

Update Compare 3 value to be added to the compare register 3 value on compare match.

Return to Summary Table

Table 5-2586. Instance Table

Instance Name	Physical Address
WDT0	5210 006Ch
WDT1	5210 106Ch
WDT2	5210 206Ch
WDT3	5210 306Ch

Figure 5-1261. WDT_RTIUDCP3 Name Register

31	30	29	28	27	26	25	24
UDCP3							
R/W							
0h							
23	22	21	20	19	18	17	16
UDCP3							
R/W							
0h							
15	14	13	12	11	10	9	8
UDCP3							
R/W							
0h							
7	6	5	4	3	2	1	0
UDCP3							
R/W							
0h							

Table 5-2587. WDT_RTIUDCP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	UDCP3	R/W	0h	UDCP3: Update compare 3 Register. This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode [read]: value to be added to the compare 3 register on the next compare match Privilege mode [write]: new update value

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5.27.2.23 WDT_RTITBLCOMP Register

5.27.2.23.1 WDT_RTITBLCOMP Register (Offset = 70h) [reset = 0h]

Timebase Low Compare compare value to activate edge detection circuit.

Return to Summary Table

Table 5-2588. Instance Table

Instance Name	Physical Address
WDT0	5210 0070h
WDT1	5210 1070h
WDT2	5210 2070h
WDT3	5210 3070h

Figure 5-1262. WDT_RTITBLCOMP Name Register

31	30	29	28	27	26	25	24
TBLCOMP							
R/W							
0h							
23	22	21	20	19	18	17	16
TBLCOMP							
R/W							
0h							
15	14	13	12	11	10	9	8
TBLCOMP							
R/W							
0h							
7	6	5	4	3	2	1	0
TBLCOMP							
R/W							
0h							

Table 5-2589. WDT_RTITBLCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBLCOMP	R/W	0h	TBLCOMP: Timebase Low Compare Value. This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0. User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed Note: Reset behavior A reset does not generate a compare match.

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5.27.2.24 WDT_RTITBHCOMP Register

5.27.2.24.1 WDT_RTITBHCOMP Register (Offset = 74h) [reset = 0h]

Timebase High Compare compare value to deactivate edge detection circuit.

Return to Summary Table

Table 5-2590. Instance Table

Instance Name	Physical Address
WDT0	5210 0074h
WDT1	5210 1074h
WDT2	5210 2074h
WDT3	5210 3074h

Figure 5-1263. WDT_RTITBHCOMP Name Register

31	30	29	28	27	26	25	24
TBHCOMP							
R/W							
0h							
23	22	21	20	19	18	17	16
TBHCOMP							
R/W							
0h							
15	14	13	12	11	10	9	8
TBHCOMP							
R/W							
0h							
7	6	5	4	3	2	1	0
TBHCOMP							
R/W							
0h							

Table 5-2591. WDT_RTITBHCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	TBHCOMP	R/W	0h	TBHCOMP: Timebase High Compare Value. This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0. RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached. Example: The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0. RTICPUC0 = 0x00000050 RTITBLCOMP = 0x000046 RTITBHCOMP = 0x00000009 User and privilege mode [read]: current compare value Privilege mode [write when TBEXT = 0]: the compare value is updated Privilege mode [write when TBEXT = 1]: the compare value is not changed Note: Reset behavior A reset does not generate a compare match.

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5.27.2.25 WDT_RTISETINT Register

5.27.2.25.1 WDT_RTISETINT Register (Offset = 80h) [reset = 0h]

Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.

Return to Summary Table

Table 5-2592. Instance Table

Instance Name	Physical Address
WDT0	5210 0080h
WDT1	5210 1080h
WDT2	5210 2080h
WDT3	5210 3080h

Figure 5-1264. WDT_RTISETINT Name Register

31	30	29	28	27	26	25	24
RESERVED11							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED11					SETOVL1INT	SETOVL0INT	SETTBINT
R/W					R/W	R/W	R/W
0h					0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED10				SETDMA3	SETDMA2	SETDMA1	SETDMA0
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED9				SETINT3	SETINT2	SETINT1	SETINT0
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 5-2593. WDT_RTISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED11	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	SETOVL1INT	R/W	0h	SETOVL1INT: Set Free Running Counter 1 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
17	SETOVL0INT	R/W	0h	SETOVL0INT: Set Free Running Counter 0 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt

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Table 5-2593. WDT_RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SETTBINT	R/W	0h	SETTBINT: Set Timebase Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
15:12	RESERVED10	R/W	0h	Reserved. Reads return 0 and writes have no effect
11	SETDMA3	R/W	0h	SETDMA3: Set Compare DMA Request 3. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
10	SETDMA2	R/W	0h	SETDMA2: Set Compare DMA Request 2. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
9	SETDMA1	R/W	0h	SETDMA1: Set Compare DMA Request 1. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
8	SETDMA0	R/W	0h	SETDMA0: Set Compare DMA Request 0. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable DMA request
7:4	RESERVED9	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	SETINT3	R/W	0h	SETINT3: Set Compare Interrupt 3. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged
2	SETINT2	R/W	0h	SETINT2: Set Compare Interrupt 2. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt
1	SETINT1	R/W	0h	SETINT1: Set Compare Interrupt 1. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt

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Table 5-2593. WDT_RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SETINT0	R/W	0h	SETINT0: Set Compare Interrupt 0. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = enable interrupt

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5.27.2.26 WDT_RTICLEARINT Register

5.27.2.26.1 WDT_RTICLEARINT Register (Offset = 84h) [reset = 0h]

Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.

Return to Summary Table

Table 5-2594. Instance Table

Instance Name	Physical Address
WDT0	5210 0084h
WDT1	5210 1084h
WDT2	5210 2084h
WDT3	5210 3084h

Figure 5-1265. WDT_RTICLEARINT Name Register

31	30	29	28	27	26	25	24
RESERVED14							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED14					CLEAROVL1INT	CLEAROVL0INT	CLEARTBINT
R/W					R/W	R/W	R/W
0h					0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED13				CLEARDMA3	CLEARDMA2	CLEARDMA1	CLEARDMA0
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h
7	6	5	4	3	2	1	0
RESERVED12				CLEARINT3	CLEARINT2	CLEARINT1	CLEARINT0
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 5-2595. WDT_RTICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED14	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	CLEAROVL1INT	R/W	0h	CLEAROVL1INT: CLEAR Free Running Counter 1 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
17	CLEAROVL0INT	R/W	0h	CLEAROVL0INT: CLEAR Free Running Counter 0 Overflow Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt

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Table 5-2595. WDT_RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CLEARTBINT	R/W	0h	CLEARTBINT: CLEAR Timebase Interrupt. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
15:12	RESERVED13	R/W	0h	Reserved. Reads return 0 and writes have no effect
11	CLEARDMA3	R/W	0h	CLEARDMA3: CLEAR Compare DMA Request 3. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
10	CLEARDMA2	R/W	0h	CLEARDMA2: CLEAR Compare DMA Request 2. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
9	CLEARDMA1	R/W	0h	CLEARDMA1: CLEAR Compare DMA Request 1. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
8	CLEARDMA0	R/W	0h	CLEARDMA0: CLEAR Compare DMA Request 0. User and privilege mode [read]: 0 = DMA request is disabled 1 = DMA request is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable DMA request
7:4	RESERVED12	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	CLEARINT3	R/W	0h	CLEARINT3: CLEAR Compare Interrupt 3. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
2	CLEARINT2	R/W	0h	CLEARINT2: CLEAR Compare Interrupt 2. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt
1	CLEARINT1	R/W	0h	CLEARINT1: CLEAR Compare Interrupt 1. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt

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Table 5-2595. WDT_RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLEARINT0	R/W	0h	CLEARINT0: CLEAR Compare Interrupt 0. User and privilege mode [read]: 0 = interrupt is disabled 1 = interrupt is enabled Privilege mode [write]: 0 = leaves the corresponding bit unchanged 1 = disable interrupt

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5.27.2.27 WDT_RTIINTFLAG Register

5.27.2.27.1 WDT_RTIINTFLAG Register (Offset = 88h) [reset = 0h]

Interrupt Flags interrupt pending bits.

Return to Summary Table

Table 5-2596. Instance Table

Instance Name	Physical Address
WDT0	5210 0088h
WDT1	5210 1088h
WDT2	5210 2088h
WDT3	5210 3088h

Figure 5-1266. WDT_RTIINTFLAG Name Register

31	30	29	28	27	26	25	24
RESERVED16							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED16					OVL1INT	OVL0INT	TBINT
R/W					R/W	R/W	R/W
0h					0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED15							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED15				INT3	INT2	INT1	INT0
R/W				R/W	R/W	R/W	R/W
0h				0h	0h	0h	0h

Table 5-2597. WDT_RTIINTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31:19	RESERVED16	R/W	0h	Reserved. Reads return 0 and writes have no effect
18	OVL1INT	R/W	0h	OVL1INT: Free Running Counter 1 Overflow Interrupt Flag. User and privilege mode [read]: determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
17	OVL0INT	R/W	0h	OVL0INT: Free Running Counter 0 Overflow Interrupt Flag. User and privilege mode [read]: determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0

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Table 5-2597. WDT_RTIINTFLAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	TBINT	R/W	0h	User and privilege mode [read]: this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software. determines if an interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
15:4	RESERVED15	R/W	0h	Reserved. Reads return 0 and writes have no effect
3	INT3	R/W	0h	INT3: Interrupt Flag 3. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
2	INT2	R/W	0h	INT2: Interrupt Flag 2. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
1	INT1	R/W	0h	INT1: Interrupt Flag 1. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0
0	INT0	R/W	0h	INT0: Interrupt Flag 0. User and privilege mode [read]: determines if a interrupt is pending 0 = no interrupt pending 1 = interrupt pending Privilege mode [write]: 0 = leaves the bit unchanged 1 = set the bit to 0

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5.27.2.28 WDT_RTIDWDCTRL Register

5.27.2.28.1 WDT_RTIDWDCTRL Register (Offset = 90h) [reset = 0h]

Digital Watchdog Control Enables the Digital Watchdog.

Return to Summary Table

Table 5-2598. Instance Table

Instance Name	Physical Address
WDT0	5210 0090h
WDT1	5210 1090h
WDT2	5210 2090h
WDT3	5210 3090h

Figure 5-1267. WDT_RTIDWDCTRL Name Register

31	30	29	28	27	26	25	24
DWDCTRL							
R/W							
0h							
23	22	21	20	19	18	17	16
DWDCTRL							
R/W							
0h							
15	14	13	12	11	10	9	8
DWDCTRL							
R/W							
0h							
7	6	5	4	3	2	1	0
DWDCTRL							
R/W							
0h							

Table 5-2599. WDT_RTIDWDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	DWDCTRL	R/W	0h	DWDCTRL: Digital Watchdog Control. User and priviledge mode [read]: 0x5312ACED = DWD counter is disabled. This is the default value. 0xA98559DA = DWD counter is enabled Any other value = DWD counter state is unchanged [enabled or disabled] Priviledge mode [write]: 0xA98559DA = DWD counter is enabled Any other value = State of DWD counter is unchanged [stays enabled or disabled] Note: One-Write Functionality of DWDCTRL Register The RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this registermore than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again.

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5.27.2.29 WDT_RTIDWDPRLD Register

5.27.2.29.1 WDT_RTIDWDPRLD Register (Offset = 94h) [reset = 0h]

Digital Watchdog Preload sets the experation time of the Digital Watchdog.

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Table 5-2600. Instance Table

Instance Name	Physical Address
WDT0	5210 0094h
WDT1	5210 1094h
WDT2	5210 2094h
WDT3	5210 3094h

Figure 5-1268. WDT_RTIDWDPRLD Name Register

31	30	29	28	27	26	25	24
RESERVED17							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED17							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED17				DWDPRLD			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
DWDPRLD							
R/W							
0h							

Table 5-2601. WDT_RTIDWDPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31:12	RESERVED17	R/W	0h	Reserved. Reads return 0 and writes have no effect
11:0	DWDPRLD	R/W	0h	DWDPRLD: Digital Watchdog Preload Value. User and priviledge mode [read]: A read from this register in any CPU mode returns the current preload value. Priviledge mode [write]: The DWD preload register can be configured only when the DWD is disabled.Therefore, the application can only configure the DWD preload register before it enables the DWD down counter. The expiration time of the DWD Down Counter can be determined with following equation: texp = [RTIDWDPRLD+1] x 2 ^ 13 / RTICLK1 where: RTIDWDPRLD = 0...4095

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5.27.2.30 WDT_RTIWDSTATUS Register

5.27.2.30.1 WDT_RTIWDSTATUS Register (Offset = 98h) [reset = 0h]

Watchdog Status reflects the status of Analog and Digital Watchdog.

Return to Summary Table

Table 5-2602. Instance Table

Instance Name	Physical Address
WDT0	5210 0098h
WDT1	5210 1098h
WDT2	5210 2098h
WDT3	5210 3098h

Figure 5-1269. WDT_RTIWDSTATUS Name Register

31	30	29	28	27	26	25	24
RESERVED18							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED18							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED18							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED18		DWWD_ST	ENDTIMEVIOL	STARTTIMEVIOL	KEYST	DWDST	AWDST
R/W		R/W	R/W	R/W	R/W	R/W	R/W
0h		0h	0h	0h	0h	0h	0h

Table 5-2603. WDT_RTIWDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31:6	RESERVED18	R/W	0h	Reserved. Reads return 0 and writes have no effect
5	DWWD_ST	R/W	0h	DWWD ST: Windowed Watchdog Status. This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog. User and priviledge mode [read]: 0 = no time-window violation has occurred. 1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS register except for the AWD ST flag. Clearing of the status flags will deassert the non-maskable interrupt generated due to violation of the DWWD.

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Table 5-2603. WDT_RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ENDTIMEVIOL	R/W	0h	END TIME VIOL: Windowed Watchdog End Time Violation Status. This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag. User and priviledge mode [read]: 0 = no end-time window violation has occurred. 1 = the end-time defined by the windowed watchdog configuration has been violated. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0.
3	STARTTIMEVIOL	R/W	0h	START TIME VIOL: Windowed Watchdog Start Time Violation Status. This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened. User and priviledge mode [read]: 0 = no start-time window violation has occurred. 1 = the start-time defined by the windowed watchdog configuration has been violated. Priviledge mode [write]: 0 = leaves the current value unchanged. 1 = clears the bit to 0.
2	KEYST	R/W	0h	KEYST: Watchdog KeyStatus. This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register. User and priviledge mode [read]: 0 = no wrong key or key-sequence written 1 = wrong key or key-sequence written to RTIWDKEY register Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0
1	DWDST	R/W	0h	DWDST: Digital Watchdog Status. This bit is effectively a copy of the END TIME VIOL status flag and is maintained for compatibility reasons. User and priviledge mode [read]: 0 = DWD timeout period not expired 1 = DWD timeout period has expired Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0
0	AWDST	R/W	0h	AWDST: Analog Watchdog Status. User and priviledge mode [read]: 0 = AWD pin 0 > 1 threshold not exceeded 1 = AWD pin 0 > 1 threshold exceeded Priviledge mode [write]: 0 = leaves the current value unchanged 1 = clears the bit to 0

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5.27.2.31 WDT_RTIWDKEY Register

5.27.2.31.1 WDT_RTIWDKEY Register (Offset = 9Ch) [reset = 0h]

Watchdog Key correct written key values discharge the external capacitor.

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Table 5-2604. Instance Table

Instance Name	Physical Address
WDT0	5210 009Ch
WDT1	5210 109Ch
WDT2	5210 209Ch
WDT3	5210 309Ch

Figure 5-1270. WDT_RTIWDKEY Name Register

31	30	29	28	27	26	25	24
RESERVED19							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED19							
R/W							
0h							
15	14	13	12	11	10	9	8
WDKEY							
R/W							
0h							
7	6	5	4	3	2	1	0
WDKEY							
R/W							
0h							

Table 5-2605. WDT_RTIWDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31:16	RESERVED19	R/W	0h	Reserved. Reads return 0 and writes have no effect
15:0	WDKEY	R/W	0h	WDKEY: Watchdog Key. User and privilege mode reads are indeterminate. Privilege mode [write]: A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1s. Writing any other value causes a digital watchdog reset, as shown in Table 1-3. Note: Register write access time precaution The user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation.

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5.27.2.32 WDT_RTIDWDCNTR Register

5.27.2.32.1 WDT_RTIDWDCNTR Register (Offset = A0h) [reset = 1FFFFFFh]

Digital Watchdog Down Counter current value of DWD down counter.

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Table 5-2606. Instance Table

Instance Name	Physical Address
WDT0	5210 00A0h
WDT1	5210 10A0h
WDT2	5210 20A0h
WDT3	5210 30A0h

Figure 5-1271. WDT_RTIDWDCNTR Name Register

31	30	29	28	27	26	25	24
RESERVED20							DWDCNTR
R/W							R/W
0h							1FFFFFFh
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DWDCNTR							
R/W							
1FFFFFFh							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DWDCNTR							
R/W							
1FFFFFFh							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DWDCNTR							
R/W							
1FFFFFFh							

Table 5-2607. WDT_RTIDWDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:25	RESERVED20	R/W	0h	Reserved. Reads return 0 and writes have no effect
24:0	DWDCNTR	R/W	1FFFFFFh	DWDCNTR: Digital Watchdog Down Counter. The value of the DWDCNTR after a system reset is 0x01FF_FFFF. When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second. User and privilege mode [read]: Reads return the current counter value. Privilege mode [write]: Writes dont have an effect.

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5.27.2.33 WDT_RTIWWDRXNCTRL Register

5.27.2.33.1 WDT_RTIWWDRXNCTRL Register (Offset = A4h) [reset = 0h]

Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset.

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Table 5-2608. Instance Table

Instance Name	Physical Address
WDT0	5210 00A4h
WDT1	5210 10A4h
WDT2	5210 20A4h
WDT3	5210 30A4h

Figure 5-1272. WDT_RTIWWDRXNCTRL Name Register

31	30	29	28	27	26	25	24
RESERVED21							
R/W							
0h							
23	22	21	20	19	18	17	16
RESERVED21							
R/W							
0h							
15	14	13	12	11	10	9	8
RESERVED21							
R/W							
0h							
7	6	5	4	3	2	1	0
RESERVED21				WWDRXN			
R/W				R/W			
0h				0h			

Table 5-2609. WDT_RTIWWDRXNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:4	RESERVED21	R/W	0h	Reserved. Reads return 0 and writes have no effect

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Table 5-2609. WDT_RTIWWDRXNCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	WWDRXN	R/W	0h	WWDRXN: Digital Windowed Watchdog Reaction. User and privilege mode [read], privileged mode [write]: 0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. 0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Note: Configuration of DWWD Reaction The DWWD reaction can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.

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5.27.2.34 WDT_RTIWWDSIZECTRL Register

5.27.2.34.1 WDT_RTIWWDSIZECTRL Register (Offset = A8h) [reset = 0h]

Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog.

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Table 5-2610. Instance Table

Instance Name	Physical Address
WDT0	5210 00A8h
WDT1	5210 10A8h
WDT2	5210 20A8h
WDT3	5210 30A8h

Figure 5-1273. WDT_RTIWWDSIZECTRL Name Register

31	30	29	28	27	26	25	24
WWDSIZE							
R/W							
0h							
23	22	21	20	19	18	17	16
WWDSIZE							
R/W							
0h							
15	14	13	12	11	10	9	8
WWDSIZE							
R/W							
0h							
7	6	5	4	3	2	1	0
WWDSIZE							
R/W							
0h							

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Table 5-2611. WDT_RTIWWDSIZECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	WWDSIZE	R/W	0h	WWDSIZE: Digital Windowed Watchdog Window Size. User and privilege mode [read], privileged mode [write]: Value written to WWDSIZE Window Size 0x00000005 100% [Functionality same as the time-out digital watchdog.] 0x00000050 50% 0x00000500 25% 0x00005000 12.5% 0x00050000 6.25% 0x00500000 3.125% Any other value 3.125% Note: Incorrect value being written to watchdog window size control register If an incorerct value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration. Note: Configuration of DWWD Window Size The DWWD window size can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDSIZE is made when the watchdog service window is already open, then

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5.27.2.35 WDT_RTIINTCLRENABLE Register

5.27.2.35.1 WDT_RTIINTCLRENABLE Register (Offset = ACh) [reset = 0h]

RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts.

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Table 5-2612. Instance Table

Instance Name	Physical Address
WDT0	5210 00ACh
WDT1	5210 10ACh
WDT2	5210 20ACh
WDT3	5210 30ACh

Figure 5-1274. WDT_RTIINTCLRENABLE Name Register

31	30	29	28	27	26	25	24
RESERVED25				INTCLRENABLE3			
R/W				R/W			
0h				0h			
23	22	21	20	19	18	17	16
RESERVED24				INTCLRENABLE2			
R/W				R/W			
0h				0h			
15	14	13	12	11	10	9	8
RESERVED23				INTCLRENABLE1			
R/W				R/W			
0h				0h			
7	6	5	4	3	2	1	0
RESERVED22				INTCLRENABLE0			
R/W				R/W			
0h				0h			

Table 5-2613. WDT_RTIINTCLRENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31:28	RESERVED25	R/W	0h	Reserved. Reads return 0 and writes have no effect
27:24	INTCLRENABLE3	R/W	0h	INTCLRENABLE3. Enables the auto-clear functionality on the compare 3 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 3 interrupt is disabled. Any other value = Auto-clear for compare 3 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 3 interrupt. Any other value = Enables the auto-clear functionality on the compare 3 interrupt.
23:20	RESERVED24	R/W	0h	Reserved. Reads return 0 and writes have no effect

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Table 5-2613. WDT_RTIINTCLRENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19:16	INTCLRENABLE2	R/W	0h	INTCLRENABLE2. Enables the auto-clear functionality on the compare 2 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 2 interrupt is disabled. Any other value = Auto-clear for compare 2 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 2 interrupt. Any other value = Enables the auto-clear functionality on the compare 2 interrupt.
15:12	RESERVED23	R/W	0h	Reserved. Reads return 0 and writes have no effect
11:8	INTCLRENABLE1	R/W	0h	INTCLRENABLE1. Enables the auto-clear functionality on the compare 1 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 1 interrupt is disabled. Any other value = Auto-clear for compare 1 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 1 interrupt. Any other value = Enables the auto-clear functionality on the compare 1 interrupt.
7:4	RESERVED22	R/W	0h	Reserved. Reads return 0 and writes have no effect
3:0	INTCLRENABLE0	R/W	0h	INTCLRENABLE0. Enables the auto-clear functionality on the compare 0 interrupt. User and Privileged mode [read]: 0x5 = Auto-clear for compare 0 interrupt is disabled. Any other value = Auto-clear for compare 0 interrupt is enabled. Privileged mode [write]: 0x5 = Disables the auto-clear functionality on the compare 0 interrupt. Any other value = Enables the auto-clear functionality on the compare 0 interrupt.

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5.27.2.36 WDT_RTICOMP0CLR Register

5.27.2.36.1 WDT_RTICOMP0CLR Register (Offset = B0h) [reset = 0h]

Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line.

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Table 5-2614. Instance Table

Instance Name	Physical Address
WDT0	5210 00B0h
WDT1	5210 10B0h
WDT2	5210 20B0h
WDT3	5210 30B0h

Figure 5-1275. WDT_RTICOMP0CLR Name Register

31	30	29	28	27	26	25	24
COMP0CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP0CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP0CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP0CLR							
R/W							
0h							

Table 5-2615. WDT_RTICOMP0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP0CLR	R/W	0h	COMP0CLR: Compare 0 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.27.2.37 WDT_RTICOMP1CLR Register

5.27.2.37.1 WDT_RTICOMP1CLR Register (Offset = B4h) [reset = 0h]

Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line.

Return to Summary Table

Table 5-2616. Instance Table

Instance Name	Physical Address
WDT0	5210 00B4h
WDT1	5210 10B4h
WDT2	5210 20B4h
WDT3	5210 30B4h

Figure 5-1276. WDT_RTICOMP1CLR Name Register

31	30	29	28	27	26	25	24
COMP1CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP1CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP1CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP1CLR							
R/W							
0h							

Table 5-2617. WDT_RTICOMP1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP1CLR	R/W	0h	COMP1CLR: Compare 1 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 1 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.27.2.38 WDT_RTICOMP2CLR Register

5.27.2.38.1 WDT_RTICOMP2CLR Register (Offset = B8h) [reset = 0h]

Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line.

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Table 5-2618. Instance Table

Instance Name	Physical Address
WDT0	5210 00B8h
WDT1	5210 10B8h
WDT2	5210 20B8h
WDT3	5210 30B8h

Figure 5-1277. WDT_RTICOMP2CLR Name Register

31	30	29	28	27	26	25	24
COMP2CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP2CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP2CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP2CLR							
R/W							
0h							

Table 5-2619. WDT_RTICOMP2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP2CLR	R/W	0h	COMP2CLR: Compare 2 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 2 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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5.27.2.39 WDT_RTICOMP3CLR Register

5.27.2.39.1 WDT_RTICOMP3CLR Register (Offset = BCh) [reset = 0h]

Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line.

Return to Summary Table

Table 5-2620. Instance Table

Instance Name	Physical Address
WDT0	5210 00BCh
WDT1	5210 10BCh
WDT2	5210 20BCh
WDT3	5210 30BCh

Figure 5-1278. WDT_RTICOMP3CLR Name Register

31	30	29	28	27	26	25	24
COMP3CLR							
R/W							
0h							
23	22	21	20	19	18	17	16
COMP3CLR							
R/W							
0h							
15	14	13	12	11	10	9	8
COMP3CLR							
R/W							
0h							
7	6	5	4	3	2	1	0
COMP3CLR							
R/W							
0h							

Table 5-2621. WDT_RTICOMP3CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31:0	COMP3CLR	R/W	0h	COMP3CLR: Compare 3 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 3 interrupt or DMA request line is cleared. User and privilege mode [read]: current compare value Privilege mode [write]: update of the compare register with a new compare value Note: Reset behavior A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

6 Revision History

DATE	REVISION	NOTES
November 2023	*	Initial Release

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DATE	REVISION	NOTES
March 2025	A	• Updated register names with nomenclature used in other register addenda. • Updated EPWM register compaction by maintaining only one EPWM Instance table . • Removed OTTOCAL, DEBUGSS register chapters. • ADC_CFG and ADC_RESULT_REGS have been compacted into ADC. Similar compaction is done for ADC_R. • Updated CMPSSB register names to align with CMPSSA register names. • Top Level Register Name updates: – r5ss_core to R5SS – PWMXBAR to CONTROLSS_PWMXBAR – PWMSYNCOUTXBAR to CONTROLSS_PWMSYNCOUTXBAR – OUTPUTXBAR to CONTROLSS_OUTPUTXBAR – ICLXBAR to CONTROLSS_ICLXBAR – INTXBAR to CONTROLSS_INTXBAR – MDLXBAR to CONTROLSS_MDLXBAR – TOP_ESM to ESM – fss to FSS_TIMEOUT_CFG – fss_of_ul to FSS – mmchs to MMCSD – ECC_AGG to ECC_AGGR – rl2_of to RL2 – MBOX_RAM to MSS_MBOX • Updated IP and instance names across large portions of the document. • Updated register name to align with software names applied across large portions of the document. • Updated document-wide issues with incorrect reset values and offsets. • Updated PBIST Registers Base Address from "0x53300200" to "0x53300000". • Added AM263Px collateral links.
June 2025	B	• Corrected the region name in Device Memory Map chapter by changing "R5SS0_STC" to "R5SS1_STC" for the region starting at address 0x5351 0000 • Added the OTTOCAL register chapter. • Added the description for the following TOP_CTRL registers. – EFUSE1_ROW_12 – EFUSE_OVERRIDE_LDO_TRIM – MASK_ANA_ISO • Updates the PBIST register classifications. • Fixed physical address error in the following IPs – RL2 – CPSW – FSS – ESM

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