



ABSTRACT

This document provides the SK-AM68 capabilities and interface details.



This design incorporates HDMI® technology.

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1 Introduction

1.1 Inside the Box

The SK-AM68 Processor Starter Kit includes:

- SK-AM68 EVM (two PCB board solution)
- Micro-SD Card
- USB Cable (Type-A to Micro-B) for serial terminal/logging
- Paper Card with Start-up Link/Support Information

The EVM is powered from a Type-C power supply, but is NOT INCLUDED. For more information on the types of supplies recommended with the EVM, see [Table 2-1](#)


1.2 Key Features and Interfaces

- Processor
 - Texas Instruments Jacinto AM68 Super-Set device
- Optimized Power Management Solution
 - Dynamic Voltage Scaling
 - Multiple Clock and Power Domains
- Memory
 - 16GByte LPDDR4 DRAM (2133 MHz)
 - 512 Mb Non-Volatile Flash, Octal-SPI NOR
 - Multimedia Card (MMC)/Secure Digital Card (Micro SD) Cage, UHS-I
- USB
 - USB3.1 (Gen1) Hub to 3x Type A (Host)
 - USB3.1 (Gen1) Type C (DFP mode)
 - USB2.0 Micro B (for Quad UART-over-USB Transceiver)
- Display
 - VESA Display Port (v1.4), supports 2K HD
 - DVI (v1.0) via HDMI Type A, supports 1080p
- Wired Network
 - Gigabit Ethernet (RJ45 Connector)
 - 4x CAN-FD Headers (1x3)
- Camera Interfaces
 - 2x 22-Pin Flex Cable Interface (CSI-4L)
 - 40-pin High Speed Connector (dual CSI-4L, I2C, GPIO, and so forth)
- Expansion/Add-on
 - M.2 Key M Interface (PCIe/Gen3 x 2 Lane)
 - 40-pin Header (2x20) (I2C, SPI, UART, I2S, GPIO, PWM, and so forth)
 - Fan Header (5 V)
- User Control/Indication
 - Pushbuttons (Reset, Power/User Defined)
 - LEDs (Power, User Defined, Serial Port)
 - User Configuration (Boot Mode)
 - External JTAG/Emulator Support (20-pin Header)
- REACH and RoHS Compliant
- EMI/EMC Radiation Compliant

1.3 Thermal Compliance

There is elevated heat on the processor/heatsink, use caution particularly at elevated ambient temperatures!

Although the processor/heatsink is not a burn hazard, caution should be used when handling the EVM due to increased heat in the area of the heatsink

| | | |
|---|---------|---|
|  | Caution | Caution Hot surface. Contact may cause burns. Do not touch! |
|---|---------|---|

1.4 EMC, DMI, and ESD Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). It is recommended this product be used in an ESD controlled environment. This may include a temperature and/or humidity controlled environment to limit the buildup of ESD. It is also recommended to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory condition and the applied standard will be as per EN IEC 61326-1:2021.

2 User Interfaces

Figure 2-1 and Figure 2-2 identify the key user interfaces on the EVM (top and bottom view).

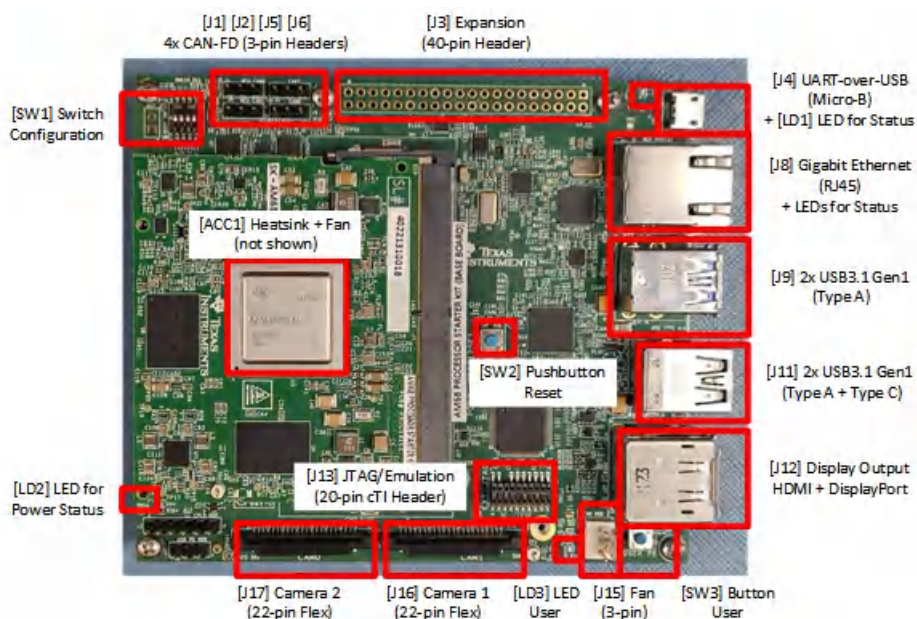


Figure 2-1. User Interfaces (Top)

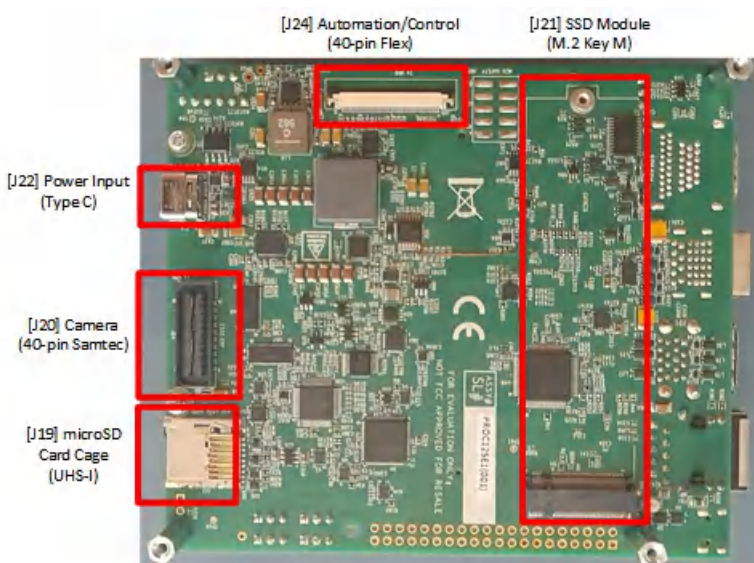


Figure 2-2. User Interfaces (Bottom)

2.1 Power Input

A power supply is not included with the EVM and must be purchased separately.

External Power Supply or Power Accessory Requirements:

- Nominal Output Voltage: 5-20VDC
- Maximum Output Current: 5000 mA
- Efficiency Level V

Note

TI recommends using an external power supply or power accessory that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, and so forth.

2.1.1 Power Input [J22] With LED for Status [LD2]

The dedicated power input connector is a USB Type C connector [J22] with Power Delivery 3.0 support. The input can accept wide range of input voltages (5 V to 20 V). The exact power required for the SK EVM is largely dependent on the application and the connected peripherals. The recommended supplies are listed in [Table 2-1](#). These supplies are 20 V Type C supplies capable of supplying up to 60W of power (20VDC at 3A). The minimum supply required is 15W supply (5VDC at 3A). However, a 5 V supply may limit available processing with the processor as well as limit some of the available peripherals. USB peripherals require VBUS and depending on their power needs, may have too much voltage drop from a 5 V input supply. This is a reason higher voltage supply is recommended.

There are many USB Type C power supply manufactures and models available in the market, and it is not possible to test the SK EVM with every combination.

[Table 2-1](#) lists a few recommended supplies the EVM has tested.

Table 2-1. Recommended External Power Supply

| Manufacturer | Part # | Digikey # |
|---------------|----------------------|--------------|
| GlobTek, Inc. | TR9CZ3000USBCG2R6BF2 | 1939-1794-ND |
| Qualtek | QADC-65-20-08CB | Q1251-ND |

2.1.2 Power Budget Considerations

The exact power required for the EVM is largely dependent on the application, usage of the on-board peripherals, and power needs of add-on devices. [Table 2-2](#) shows the designs power allocations. (Again, the input supply must be capable of supplying the power needs for your application.)

Table 2-2. Power Supply Allocation

| Function | Power | Description |
|------------------------|-----------|---|
| Processor Core | Up to 15W | Processor, Memory |
| On-board Peripherals | Up to 3W | SD card, Ethernet, Logic, and so forth |
| USB Port(s) | Up to 20W | USB Hub Type A Ports(2.8A at 5V) Type C Port(1.5A at 5V) |
| Camera Ports | Up to 2W | Cam Ports (0.5A at 3.3V) |
| Expansion Interface(s) | Up to 20W | M.2 M Key (3A at 3.3V) 40p Expansion(2A at 3.3V,1.5A at 5V) |
| Display(s) | Up to 3W | HDMI Transceiver HDMI Panel(55mA at 5V) DP Panel (0.5A at 3.3V) |

2.2 User Inputs

The EVM supports several mechanisms for the user to configure, control, and provide input to the system.

2.2.1 Board Configuration Settings [SW1]

Dip Switch [SW1] is used to configure different options available on the EVM, including processor boot mode.

Table 2-3. Processor Bootmode Settings [SW1 Switch 1-3]

| TDA4VM Boot Source | SW1.1 | SW1.2 | SW1.3 |
|---------------------------|-------|-------|-------|
| MicroSD Card [J19] | OFF | OFF | OFF |
| Non-Volatile Flash (xSPI) | OFF | OFF | ON |
| Reserved | OFF | ON | ON |

Table 2-3. Processor Bootmode Settings [SW1 Switch 1-3] (continued)

| TDA4VM Boot Source | SW1.1 | SW1.2 | SW1.3 |
|--------------------------|-------|-------|-------|
| UART [J4] (for Flashing) | ON | OFF | ON |
| No Boot (JTAG/Emulator) | ON | OFF | OFF |
| Ethernet[J8] | OFF | ON | OFF |

2.2.2 Reset Power Down Pushbutton [SW2]

When pressed [SW2], the EVM is issued a Power-On (Cold) Reset, and is held in reset until the button is released.

If the pushbutton is held longer than 5 seconds, the system will power down. The system can be restarted by either pressing the User Pushbutton [SW3] or by cycling power to the board.

2.2.3 User Pushbutton [SW3] With User LED Indication [LD3]

The pushbutton [SW3] can be used for several different functions.

Function 1: System Wake from Shutdown. After power down using either Pushbutton [SW2] or Software-Initiated (WKUP_GPIO0_69), pressing pushbutton [SW3] will re-enable and boot the EVM.

Function 2: Power Management Enable. The pushbutton [SW3] is connected with Power Management IC (EN), and can be programmed for different power related functions (ex. Wake from Sleep).

Function 3: User Defined Input/Interrupt. The pushbutton [SW3] is connected with the TDA4VE processor (WKUP_GPIO0_69), and can be programmed for variety of user input/interrupt needs.

A red LED [LD3] is available as user indicator, and is controlled via the processor (WKUP_GPIO0_29)

2.3 Standard Interfaces

The EVM provides industry standard interfaces/connectors to connect a wide variety of peripherals. As these interfaces are standard, specific pin information is not provided in this document.

2.3.1 Uart-Over-USB [J4 With LED for Status [LD1]

Four UART ports of the processor are interfaced with UART-over-USB transceiver on the EVM. When the EVM's USB micro-B connector (J4) is connected to a Host-PC using supplied USB cable (Type-A to Micro-B), the computer can establish Virtual Com Port(s) which can be used with any terminal emulation application. Virtual Com Port drivers for the transceiver (CP2108-B02-GM) can be obtained from <https://www.silabs.com/developers/usb-touart-bridge-vcp-drivers>.

Once installed, the Host-PC will create four Virtual Com Ports. Depending on the other Host-PC resources available - the Virtual COM Ports not be located at COM1-4. However, they will remain in the same numerical order.

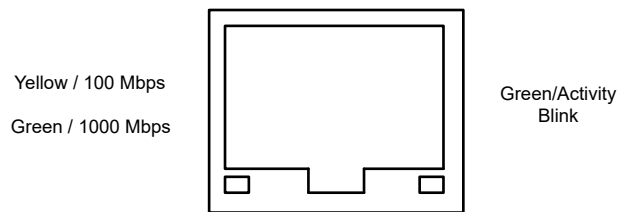
Table 2-4. UART to COM Port Mapping

| TDA4VE UART | Host-PC COM Port |
|-------------|------------------|
| WKUP_UART0 | COM 1 |
| MCU_UART0 | COM 2 |
| UART8 | COM 3 |
| UART2 | COM 4 |

The circuit is powered through BUS power and therefore the COM connection not be lost when the EVM power is removed. An LED [LD1] is used to indicate an active COM connection with Host-PC.

2.3.2 Gigabit Ethernet [J8] With Integrated LEDs for Status

A wired Ethernet network is supported on the EVM via [Figure 2-3](#), and is compatible with IEEE 802.3 10BASETe, 100BASE-TX, and 1000BASE-T specifications. The connector includes status indicators for link and activity.

**Figure 2-3. RJ45 LED Indicators [J8]**

Power-Over-Ethernet (PoE) is not supported.

2.3.3 JTAG Emulation Interface [J13]

The EVM supports JTAG emulation/debugger through a dedicated emulation connector [J13] on the baseboard. The connector is aligned with the Texas Instrument 20-pin CTI header standard (2x20, 1.27mm pitch), and is compatible with Texas Instruments modules (XDS110, XDS200, XDS560v2) and 3rd party modules.

Table 2-5. Expansion Header Pin Definition [J9]

| Pin No. | Pin Name | Description (Processor Pin #) | Dir |
|---------|----------|-------------------------------|--------|
| 1 | TMS | Test Mode Select(TMS) | Input |
| 2 | TRSTn | Test Reset | Input |
| 3 | TDI | Test Data Input | Input |
| 4 | TDIS | Target Disconnect | Output |
| 5 | Vref | Target Voltage Detect, 3.3V | Output |
| 6 | <No pin> | No pin/Key | |
| 7 | TDO | Test Data Output | Output |
| 8 | GND | Ground | |
| 9 | RTCK | Test Clock Return | Output |
| 10 | GND | Ground | |
| 11 | TCK | Test Clock | Input |
| 12 | GND | Ground | |
| 13 | EMU0 | Emulation Pin 0 | Bi-Dir |
| 14 | EMU1 | Emulation Pin 1 | Bi-Dir |
| 15 | RESETz | Target Reset | Input |
| 16 | GND | Ground | |
| 17 | | Open | |
| 18 | | Open | |
| 19 | | Open | |
| 20 | GND | Ground | |

Note

In the DIR column, output is to the JTAG module, input is from the JTAG module. Bi-Dir signals can be configured as either input or output.

2.3.4 USB3.1 Gen1 Interfaces [J9] [J11]

The EVM supports three USB3.1 Gen1 Type A ports [J9][J11], which operate in Host mode. The combined VBUS output for these ports is limited to 2.8A. Also supported is one USB3.1 Gen1 Type C interface [J11], which can function as DFP. The VBUS output for this port is limited to 1.5A.

Note

The USB2.0 Micro-B connector [J4] is discussed in Uart-over-USB section.

Note

The VBUS power capability assumes the selected input supply is capable of supplying power for both SK-AM68 system and connected peripherals.

Note

An example optional add-on USB Camera module for this interface is the Logitech USB C270.

Note

The maximum length for the IO cables should not exceed 3 meters.

2.3.5 Stacked DisplayPort and HDMI Type A [J12]

The EVM supports DisplayPort panel via standard DP cable interface [J12]. The interface supports resolutions to 2K HD (1920x1080). A second display interface is supported via HDMI connector [J12], and supports resolutions up to 2K HD (1920x1080). The interface is DVI, and therefore does not support the integrated audio. Both DisplayPort and HDMI interfaces can be used simultaneously.

2.3.6 M 2 Key M Connector [J21] for SSD Modules

The EVM supports a Mini-PCIe M.2, Key M slot (2280) for expansion modules [J21]. This expansion interface is primarily used for Solid State Drives (SSD), and supports the following interfaces: PCIe (2L) and I2C.

2.3.7 MicroSD Card Cage [J19]

The EVM supports a micro-SD card cage. It supports UHS-1 class memory cards, including SDHC and SXDC. The connector is a PUSH-PUSH connector, meaning you push to insert the card and push again to remove the card.

A MicroSD Card is included with the EVM kit.

2.4 Expansion Interfaces

The EVM supports expansion interfaces that have non-standard/custom pinouts. Each of those interfaces are introduced and specific pin information is provided.

2.4.1 Heatsink [ACC1] With [J15] Fan Header

The heatsink supports cooling of the device at ambient temperatures which will be mounted on the processor. If your environment or use case requires additional cooling, a fan can be added to the Heatsink.

The fan connector is a 3-pin header (WURTH ELEKTRONIK, Part number 61900311121).

Table 2-6. Fan Header Pin Definition [J15]

| Pin # | Pin Name | Description | Direction |
|-------|----------|----------------|-----------|
| 1 | <open> | Unconnected | N/A |
| 2 | 5V | Main 5V supply | Output |
| 3 | GND | Ground | |

2.4.2 CAN-FD Connector(s) [J1] [J2] [J5] [J6]

The EVM supports four (4x) CAN Bus interfaces.

Table 2-7. CAN-FD Interface Assignment

| Connector Ref | TDA4VE Resource |
|---------------|-----------------|
| J1 | MCU_CAN0 |
| J2 | CAN7 |
| J5 | MCU_CAN1 |
| J6 | CAN6 |

Each Controller Area Network (CAN) Bus interface is supported on a 3-pin, 2.54 mm pitch header. The interface meets ISO 11898-2 and ISO 11898-5 physical standards, and supports CAN and optimized CAN-FD performance up to 8 Mbps. Each includes CAN Bus end-point termination. If the EVM is included in a network with more than two nodes, the termination may need to be adjusted.

Table 2-8. CAN-FD Header Pin Definition [J1][J2][J5][J6]

| Pin# | Pin Name | Description | Direction |
|------|----------|-------------------------|-----------|
| 1 | CAN-H | High-Level CAN Bus Line | Bi-Dir |
| 2 | GND | Ground | |
| 3 | CAN-L | Low-Level CAN Bus Line | Bi-Dir |

2.4.3 Expansion Header [J3]

The EVM includes a 40-pin (2x20, 2.54mm pitch) expansion interface [J3]. The expansion connector supports variety of interfaces including: I2C, serial peripheral interface (SPI), I2S with Audio clock, UART, pulse width modulator (PWM), and GPIO. All signals on the interfaces are 3.3 V levels.

Table 2-9. Expansion Header Pin Definition [J3]

| Pin # | Pin Name | Description(Processor Pin #) | Dir |
|-------|-------------|--------------------------------|--------|
| 1 | Power | Power,3.3 V | Output |
| 2 | Power | Power,5.0 V | Output |
| 3 | I2C_SDA | I2C Bus #4, Data (AF28) | Bi-Dir |
| 4 | Power | Power,5.0 V | Output |
| 5 | I2C_SCL | I2C Bus #4, Clock (AD25) | Bi-Dir |
| 6 | GND | Ground | |
| 7 | GP_CLK/GPIO | REFCLK0/WKUP_GPIO0_66 (G25) | Bi-Dir |
| 8 | UART_TXD | UART#5 Transmit (W25) | Output |
| 9 | GND | Ground | |
| 10 | UART_RXD | UART#5 Receive (AC24) | Input |
| 11 | GPIO | GPIO0_42 (U24) | Bi-Dir |
| 12 | I2S_SCLK | McASP#1 ACLKX (AA24) | Bi-Dir |
| 13 | GPIO | GPIO0#36 (W24) | Bi-Dir |
| 14 | GND | Ground | |
| 15 | GPIO | WKUP_GPIO0_49 (K26) | Bi-Dir |
| 16 | GPIO | GPIO0#3 (AE28) | Bi-Dir |
| 17 | Power | Power,3.3V | Output |
| 18 | GPIO | AUDIO_EXT_REFCLK0(AD24) | Bi-Dir |
| 19 | SPI_MOSI | MCU SPI#0 Data 0 (E24) | Bi-Dir |
| 20 | GND | Ground | |
| 21 | SPI_MISO | MCU SPI#0 Data 1 (C28) | Bi-Dir |
| 22 | GPIO | WKUP_GPIO0_67 (J27) | Bi-Dir |
| 23 | SPI_SCLK | MCU SPI#0 Clock (D26) | Bi-Dir |
| 24 | SPI_CS0 | MCU SPI #0 Chip Select 0 (C27) | Bi-Dir |
| 25 | GND | Ground | |
| 26 | SPI_CS1 | MCU SPI #0 Chip Select 2 (D25) | Bi-Dir |
| 27 | ID_SDA | Wkup I2C Data (H27) | Bi-Dir |
| 28 | ID_SCL | Wkup I2C Clock (H24) | Bi-Dir |
| 29 | GPIO | WKUP_GPIO0_56 (G27) | Bi-Dir |
| 30 | GND | Ground | |
| 31 | GPIO | WKUP_GPIO0_57(J26) | Bi-Dir |
| 32 | PWM0 | PWM3_A (T25) | Output |

Table 2-9. Expansion Header Pin Definition [J3] (continued)

| Pin # | Pin Name | Description(Processor Pin #) | Dir |
|-------|----------|------------------------------|--------|
| 33 | PWM1 | PWM0_A (AE27) | Output |
| 34 | GND | Ground | |
| 35 | I2S_FS | McASP #1 FSX (V28) | Bi-Dir |
| 36 | GPIO | GPIO0_41 (T23) | Bi-Dir |
| 37 | GPIO | GPIO0_27 (V26) | Bi-Dir |
| 38 | I2S_DIN | McASP #1 (T28) | Bi-Dir |
| 39 | GND | Ground | |
| 40 | I2S_DOUT | McASP #1 (U25) | Bi-Dir |

Note

In the DIR column, output is to the expansion module, input is from the expansion module. Bi-Dir signals can be configured as either input or output.

Note

All processor signals on the Expansion connector can support other functions including GPIO. For full list of functions available on each pin, see the AM68 Processors Data Manual. Functions like UART and PWM set as INPUT or OUTPUT can be BI-DIR when configured as GPIO

2.4.4 Camera Interface 22-Pin Flex Connectors [J16][J17]

The EVM supports two (2) 22-pin flex (0.5mm pitch) connectors [J16][J17] for interfacing with camera modules. Each camera interface provides MIPI CSI-2interface (4Lane), Clock/Control signals, and power (3.3 V) to the camera.

To enable camera modules with same addressing to be used simultaneously, I2C mux is used to select each camera. The voltage level for Clock/Control signals is selectable between 1.8 V/3.3 V.

Table 2-10. Camera 1 Flex Pin Definition [J16]

| Pin # | Pin Name | Description | Dir |
|----------|------------|-----------------------|--------|
| 1/ 1A | Power | Power, 3.3V | Output |
| 3/ 2A | I2C_SDA | I2C Data # 1, Mux 0 | Bi-Dir |
| 5/ 3A | I2C_SCL | I2C Clock #1, Mux 0 | Output |
| 7/4A | GND | Ground | |
| 9/ 5A | CAM0_AUX | AUX (WKUP_GPIO0_88) | Bi-Dir |
| 11/ 6A | CAM0_PWDN | Pwr-Dwn(IO expander) | Output |
| 13/ 7A | GND | Ground | |
| 15/ 8A | CSI0_D3_P | CSIPort 0 Data Lane 3 | Input |
| 17/ 9A | CSI0_D3_N | CSIPort 0 Data Lane 3 | Input |
| 19/10A | GND | Ground | |
| 21/ 11A | CSI0_D2_P | CSIPort 0 Data Lane 0 | Input |
| 23 / 12A | CSI0_D2_N | CSIPort 0 Data Lane 0 | Input |
| 25 / 13A | GND | Ground | |
| 27 / 14A | CSI0_CLK_P | CSIPort 0 CLK | Input |
| 29 / 15A | CSI0_CLK_N | CSIPort 0 CLK | Input |
| 31 / 16A | GND | Ground | |
| 33 / 17A | CSI0_D1_P | CSIPort 0 Data Lane 1 | Input |
| 35 / 18A | CSI0_D1_N | CSIPort 0 Data Lane 1 | Input |
| 37 / 19A | GND | Ground | |
| 39 / 20A | CSI0_D1_P | CSIPort 0 Data Lane 0 | Input |
| 41 / 21A | CSI0_D1_N | CSIPort 0 Data Lane 0 | Input |

Table 2-10. Camera 1 Flex Pin Definition [J16] (continued)

| Pin # | Pin Name | Description | Dir |
|----------|----------|-------------|-----|
| 43 / 22A | GND | Ground | |

Table 2-11. Camera 2 Flex Pin Definition [J17]

| Pin # | PinName | Description | Dir |
|----------|------------|-----------------------|--------|
| 1/ 1A | Power | Power, 3.3V | Output |
| 3/ 2A | I2C_SDA | I2C Data # 1, Mux 1 | Bi-Dir |
| 5/ 3A | I2C_SCL | I2C Clock #1, Mux 1 | Output |
| 7/4A | GND | Ground | |
| 9/ 5A | CAM1_AUX | AUX (WKUP_GPIO0_70) | Bi-Dir |
| 11/ 6A | CAM1_PWDN | Pwr-Dwn(IO expander) | Output |
| 13/ 7A | GND | Ground | |
| 15/ 8A | CSI1_D3_P | CSIPort 1 Data Lane 3 | Input |
| 17/ 9A | CSI1_D3_N | CSIPort 1 Data Lane 3 | Input |
| 19/ 10A | GND | Ground | |
| 21/ 11A | CSI1_D2_P | CSIPort 1 Data Lane 0 | Input |
| 23 / 12A | CSI1_D2_N | CSIPort 1 Data Lane 0 | Input |
| 25 / 13A | GND | Ground | |
| 27 / 14A | CSI1_CLK_P | CSIPort 1 CLK | Input |
| 29 / 15A | CSI1_CLK_N | CSIPort 1 CLK | Input |
| 31 / 16A | GND | Ground | |
| 33 / 17A | CSI1_D1_P | CSIPort 1 Data Lane 1 | Input |
| 35 / 18A | CSI1_D1_N | CSIPort 1 Data Lane 1 | Input |
| 37 / 19A | GND | Ground | |
| 39 / 20A | CSI1_D1_P | CSIPort 1 Data Lane 0 | Input |
| 41 / 21A | CSI1_D1_N | CSIPort 1 Data Lane 0 | Input |
| 43 / 22A | GND | Ground | |

Note

In the DIR column, output is to the camera module, input is from the camera module. Bi-Dir signals can be configured as either input or output.

2.4.5 Camera Interface 40-Pin High Speed [J20]

The EVM includes a 40-pin (2x20, 2.54 mm pitch) high speed camera interface [J20]. The expansion connector supports two CSI-2 (4 Lanes each), power, and control signals (I2C, GPIO, and so forth): All control signals are configurable for 3.3 V or 1.8 V voltage levels.

Table 2-12. Camera IO Voltage Control

| I2C IO Expander (P00) | CameraIO Level |
|-----------------------|----------------|
| Lower '0' | 1.8V (Default) |
| Highor '1' | 3.3V |

Table 2-13. 40-Pin High-Speed Camera Expansion Pin Definition [J20]

| Pin # | Pin Name | Description(Processor Pin #) | Dir |
|-------|------------|------------------------------|--------|
| 1 | Power | | Output |
| 2 | I2C_SCL | I2C Bus #1, Clock (AC25) | Bi-Dir |
| 3 | Power | | Output |
| 4 | I2C_SDA | I2C Bus #1, Data (AD26) | Bi-Dir |
| 5 | CSI0_CLK_P | CSIPort 0 Clock | Input |
| 6 | GPIO/PWMA | WKUP_GPIO0_32(B20) | Bi-Dir |

Table 2-13. 40-Pin High-Speed Camera Expansion Pin Definition [J20] (continued)

| Pin # | Pin Name | Description(Processor Pin #) | Dir |
|-------|------------|-------------------------------|--------|
| 7 | CSI0_CLK_N | CSI Port 0 Clock | Input |
| 8 | GPIO/PWMB | WKUP_GPIO0_36 (C20) | Bi-Dir |
| 9 | CSI0_D0_P | CSI Port 0 Data Lane 0 | Input |
| 10 | REFCLK | MCU CLKOUT0(F25) | Bi-Dir |
| 11 | CSI0_D0_N | CSI Port 0 Data Lane 0 | Input |
| 12 | GND | Ground | |
| 13 | CSI0_D1_P | CSI Port 0 Data Lane 1 | Input |
| 14 | RESETz | FROM IO EXPANDER | Output |
| 15 | CSI0_D1_N | CSI Port 0 Data Lane 1 | Input |
| 16 | GND | Ground | |
| 17 | CSI0_D2_P | CSI Port 0 Data Lane 2 | Input |
| 18 | GPIO | WKUP_GPIO0_37 (A20) | Bi-Dir |
| 19 | CSI0_D2_N | CSI Port 0 Data Lane 2 | Input |
| 20 | GPIO | WKUP_GPIO0_38 (D20) | Bi-Dir |
| 21 | CSI0_D3_P | CSI Port 0 Data Lane 3 | Input |
| 22 | GPIO | WKUP_GPIO0_35 (G20) | Bi-Dir |
| 23 | CSI0_D3_N | CSI Port 0 Data Lane 3 | Input |
| 24 | GND | Ground | |
| 25 | CSI1_CLK_P | CSI Port 1 Clock | Input |
| 26 | CSI1_D3_P | CSI Port 1 Data Lane 3 | Input |
| 27 | CSI1_CLK_N | CSI Port 1 Clock | Input |
| 28 | CSI1_D3_N | CSI Port 1 Data Lane 3 | Input |
| 29 | CSI1_D0_P | CSI Port 1 Data Lane 0 | Input |
| 30 | Power | Power, 3.3V | Output |
| 31 | CSI1_D0_N | CSI Port 1 Data Lane 0 | Input |
| 32 | Power | Power, 3.3V | Output |
| 33 | CSI1_D1_P | CSI Port 1 Data Lane 1 | Input |
| 34 | Power | Power, 3.3V | Output |
| 35 | CSI1_D1_N | CSI Port 1 Data Lane 1 | Input |
| 36 | Power | Power, 3.3V | Output |
| 37 | CSI1_D2_P | CSI Port 1 Data Lane 2 | Input |
| 38 | Power | Power, IO Level (1.8 or 3.3V) | Output |
| 39 | CSI1_D2_N | CSI Port 1 Data Lane 2 | Input |
| 40 | Power | Power, IO Level (1.8 or 3.3V) | Output |

Note

In the DIR column, output is to the expansion module, input is from the expansion module. Bi-Dir signals can be configured as either input or output.

2.4.6 Automation and Control Connector [J24]

The EVM supports an interface to allow for automated control of the system, including functions like on/off, reset, and boot mode settings.

Table 2-14. Test Automation Interface Pin Definition [J24]

| Pin | Pin Name | Description(Processor Pin #) | Dir |
|-----|----------|------------------------------|--------|
| 1 | Power | Power,3.3 V | Output |
| 2 | Power | Power,3.3 V | Output |

Table 2-14. Test Automation Interface Pin Definition [J24] (continued)

| Pin | Pin Name | Description(Processor Pin #) | Dir |
|-------|---------------|------------------------------|--------|
| 3 | Power | Power,3.3 V | Output |
| 4-6 | <open> | | N/A |
| 7 | GND | Ground | |
| 8-15 | <open> | | N/A |
| 16 | GND | Ground | |
| 17-24 | <open> | | N/A |
| 25 | GND | Ground | |
| 26 | POWERDOWNz | EVM Power Down | Input |
| 27 | PORz | EVM Power-On/Cold Reset | Input |
| 28 | RESETz | EVM Warm Reset | Input |
| 29 | <open> | | N/A |
| 30 | INT1z | MCU_ADC1_AIN0 (P25) | Input |
| 31 | INT2z | MCU_ADC1_AIN1 (R25) | Bi-Dir |
| 32 | <open> | | N/A |
| 33 | BOOTMODE_RSTz | Bootmode Buffer Reset | Input |
| 34 | GND | Ground | |
| 35 | <open> | | N/A |
| 36 | I2C_SCL | MCU I2C Bus #0, Clock (G24) | Bi-Dir |
| 37 | BOOTMODE_SCL | Bootmode Buffer I2C Clock | Input |
| 38 | I2C_SDA | MCU I2C Bus #0, Data (J25) | Bi-Dir |
| 39 | BOOTMODE_SDA | Bootmode Buffer I2C Data | Bi-Dir |
| 40 | GND | Ground | |
| 41 | GND | Ground | |
| 42 | GND | Ground | |

Note

In the DIR column, output is to the test automation module, input is from the test automation module. Bi-Dir signals can be configured as either input or output.

Note

The signal polarity is identified with a trailing 'z' in the Pin Name, which indicates the signal is active LOW. For example, POWERDOWNz is an active low signal, meaning '0' = EVM is Powered Down, '1' = EVM is NOT Powered Down.

3 Circuit Details

This section provides additional details on the EVM design and processor connections.

3.1 Top Level Diagram

Figure 3-1 shows the functional block diagram of the EVM Board.

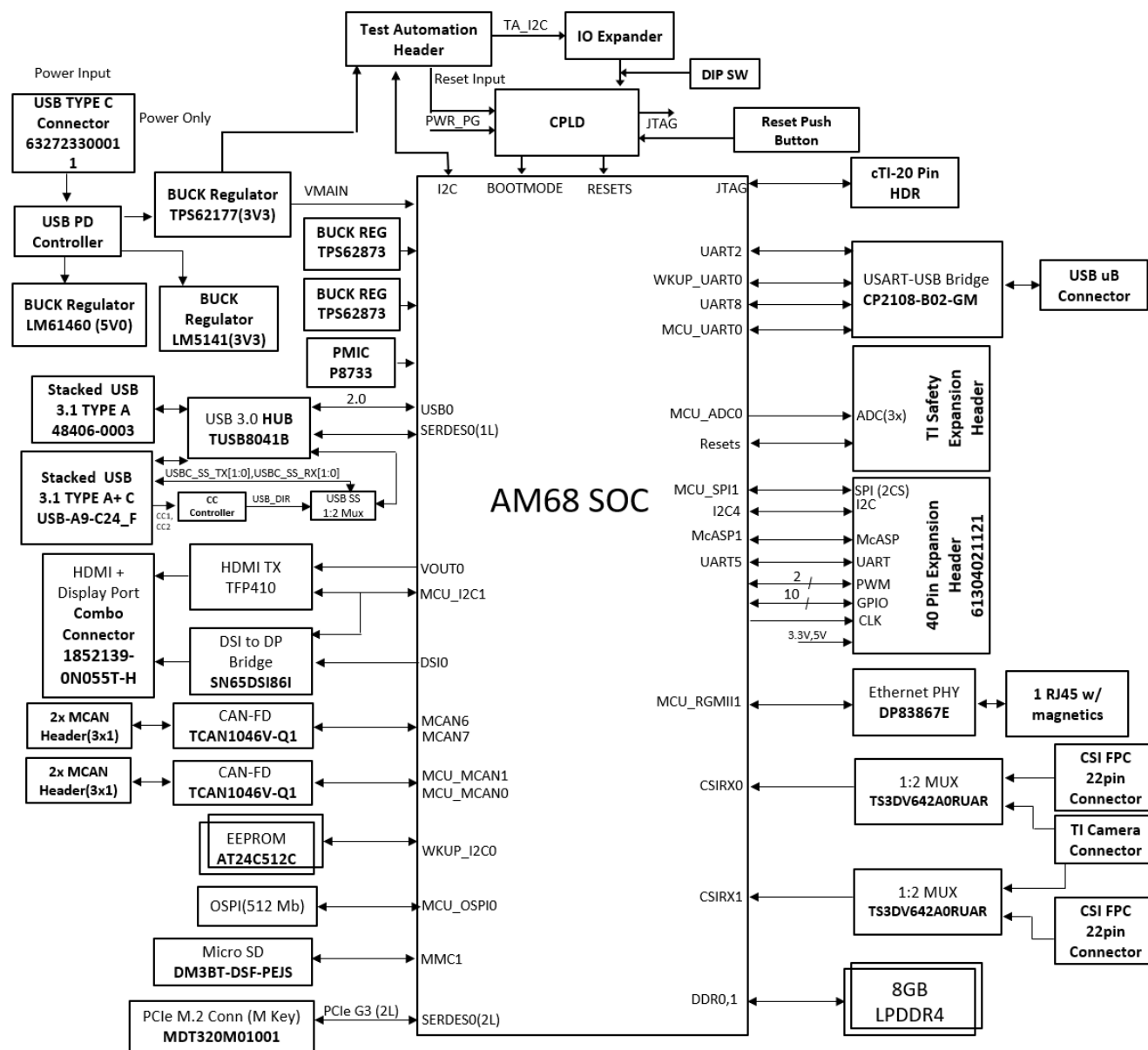


Figure 3-1. SK-AM68 EVM Functional Block Diagram

3.2 AM68 SK EVM Interface Mapping

Table 3-1 is provided below.

Table 3-1. Interface Mapping Table

| Connected Peripheral | Processor Resources | Components/ Part Numbers |
|------------------------|---------------------|--------------------------------|
| Memory, LPDDR4 DRAM | DDR0, DDR1 | Micron MT53E2G32D4DE-046 AUT:C |
| Memory, xSPI NOR Flash | MCU_OSPI0 | CypressS28HS512TGABHM010 |
| Micro-SDCard Cage | MMC1 | |

Table 3-1. Interface Mapping Table (continued)

| Connected Peripheral | Processor Resources | Components/ Part Numbers |
|-------------------------------|------------------------------------|-----------------------------|
| EEPROM, Board Identification | WKUP_I2C0 | MicrochipTech AT24C512C |
| Wired Ethernet | MCU_RGMII1, MCU_MDIO | Texas Instruments DP83867E |
| USB Type C + CC Controller | USB0(SERDES0) | Texas Instruments TUSB321 |
| USB Type A (3x) | USB0(SERDES0) | Texas Instruments TUSB8041 |
| HDMI | DPI0, MCU_I2C1 | Texas Instruments TFP410 |
| DisplayPort | DSI0, MCU_I2C1 | Texas Instruments SN65DSI86 |
| PCIe– M.2 Socket (M-Key 2280) | PCIe1 (SERDES0), I2C0 | |
| CSIRx Interface | CSI0,CSI1, I2C1 | |
| UART Terminal (UART-to-USB) | WKUP_UART0,MCU_UART0, UART8, UART2 | SiliconLabs CP2108 |
| CAN(4x) | MCU_MCAN0, MCU_MCAN1, MCAN6, MCAN7 | Texas Instruments TCAN1046V |
| Expansion Header (40-pin) | McASP1, MCU_SPI1, UART5, I2C4 | |
| Expansion Header (10-pin) | MCU_ADC0,RESETs | |
| TestAutomation Header | MCU_I2C0 | |

3.3 I2C Address Mapping

[Table 3-2](#) provides the complete I2C address mapping details on EVM.

Table 3-2. I2C Mapping Table

| Connected Peripheral | Processor Resources | | Components/ Part Numbers |
|-----------------------------|---------------------|------------|-----------------------------|
| | I2C Port | I2CAddress | |
| Power Management IC | WKUP_I2C0 | 0x60 | Texas Instruments LP8733 |
| Buck Regulator | WKUP_I2C0 | 0x40 | Texas Instruments TPS62873 |
| Buck Regulator | WKUP_I2C0 | 0x43 | Texas Instruments TPS62873 |
| EEPROM, Board Id SOM | WKUP_I2C0 | 0x51 | Microchip Tech AT24C512C |
| EEPROM, Board Id Base Board | WKUP_I2C0 | 0x52 | Microchip Tech AT24C512C |
| ExpansionHeader (40p) | WKUP_I2C0 | Add-on | |
| Current Monitor IC | MCU_I2C0 | 0x40-0x45 | Texas Instruments INA231 |
| Automation Header | MCU_I2C0 | | |
| Bootmode IO expander | MCU_I2C0 | 0x20 | Texas Instruments TCA6408 |
| HDMIDDC | MCU_I2C1 | Add-on | |
| eDP Bridge | MCU_I2C1 | 0x2C | Texas Instruments SN65DSI86 |
| Input PD Controller | I2C0 | 0x20 | Texas Instruments TPS25750 |
| PCIe M.2 Key E/M | I2C0 | Add-on | |
| Camera Expansion | I2C0 | 0x70Add-on | Texas Instruments TCA9543A |
| CSI FPC Conn | I2C1 | Add-on | |
| Expansion Header (40p) | I2C4 | Add-On | |

3.4 GPIO Mapping

The General Purpose IOs (GPIO) of the AM68 SoC are segmented into two major groups, WKUP and MAIN. For this design, there is no functional difference between the GPIOs. [Table 3-3](#) describes the processor's GPIO mapping to the EVM peripherals and provides the default settings.

Table 3-3. GPIO Mapping Table

| Processor Pin Name | GPIO | Function | Dir/ Level | Remarks |
|-----------------------------|---------------|--|---------------|--|
| WKUP_GPIO0_10 | WKUP_GPIO0_10 | ADC external trigger from TI safety header(Default connection)/CLKREQ# | Input | External ADC Trigger Signal |
| WKUP_GPIO0_11 | WKUP_GPIO0_11 | 40pin Expansion HeaderSignal (REFCLK0/ GPIO) | Output | Expansion Board Specific (Pin 10) |
| WKUP_GPIO0_15 | WKUP_GPIO0_15 | MCU SPI1 signal | Output | SPI chip select Signal for 40 pin Header |
| MCU_OSPI0_CS _n 1 | WKUP_GPIO0_28 | Enable for eFUSE Programming Supply | Output | '0' – Disabled(Default) '1' – Enabled |
| MCU_OSPI0_CS _N 2 | WKUP_GPIO0_29 | User LED [LD2] | Output | '0' – LED [LD2] is OFF (default) '1' – LED [LD2] is ON |
| MCU_OSPI1_CLK | WKUP_GPIO0_31 | Ethernet PHY Interrupt | Input | '0' – Active Interrupt Request '1' – No Interrupt Request (default) |
| MCU_OSPI1_LBCLKO | WKUP_GPIO0_32 | GPIO Signals for CSI expansion connector | Bi-Dir | ExpansionBoard Specific (Pin 6) |
| MCU_OSPI1_DQS | WKUP_GPIO0_33 | SW2 Pushbutton | Output | '0' – SW2 is Pressed '1' – SW2 is NOT Pressed (default) |
| MCU_OSPI1_D0 | WKUP_GPIO0_34 | SW3 Pushbutton | Input | '0' – SW3 is Pressed '1' – SW3 is NOT Pressed (default) |
| MCU_OSPI1_D1 | WKUP_GPIO0_35 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | ExpansionBoard Specific (Pin 22) |
| MCU_OSPI1_D2 | WKUP_GPIO0_36 | GPIO Signals for CSI expansion connector | Bi-Dir | ExpansionBoard Specific (Pin 8) |
| MCU_OSPI1_D3 | WKUP_GPIO0_37 | GPIO Signals for CSI expansion connector | Bi-Dir | ExpansionBoard Specific (Pin 18) |
| MCU_OSPI1_CS _N 0 | WKUP_GPIO0_38 | CSI Expansion Signal (GPIO) | Bi-Dir | CSI2 Expansion Board Specific (Pin 20) |
| MCU_OSPI1_CS _N 1 | WKUP_GPIO0_39 | Power Management IC Interrupt | Input | '0' – Active Interrupt Request '1' – No Interrupt Request (default) |
| WKUP_GPIO0_49 | WKUP_GPIO0_49 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | Expansion Board Specific (Pin 15) |
| MCU_SPI0_CLK | WKUP_GPIO0_54 | MUX select | Output | '0' – A to B1 port selected '1' – A to B2 port selected |
| WKUP_GPIO0_56 | WKUP_GPIO0_56 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | Expansion Board Specific (Pin 29) |
| WKUP_GPIO0_57 | WKUP_GPIO0_57 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | Expansion Board Specific (Pin 31) |
| WKUP_GPIO0_66 | WKUP_GPIO0_66 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | Expansion Board Specific (Pin 7) |

Table 3-3. GPIO Mapping Table (continued)

| Processor Pin Name | GPIO | Function | Dir/ Level | Remarks |
|--------------------|---------------|--------------------------------------|---------------|---|
| WKUP_GPIO0_67 | WKUP_GPIO0_67 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | Expansion Board Specific (Pin 22) |
| MCU_SPI0_D1 | WKUP_GPIO0_69 | System Power Down | Output | '0' - Normal Operation (default) '1' - System Power Down/Off |
| MCU_SPI0_CS0 | WKUP_GPIO0_70 | Camera #1 Flex Signal (GPIO) | Bi-Dir | Camera Specific (Pin 5a) |
| MCU_ADC1_AIN0 | WKUP_GPIO0_79 | Test Automation Interrupt #1 | Input | '0' - To Be Defined by User '1' - To Be Defined by User (default) |
| MCU_ADC1_AIN1 | WKUP_GPIO0_80 | Test Automation Interrupt #2 | Input | '0' - To Be Defined by User '1' - To Be Defined by User (default) |
| PMIC_POWER_EN1 | WKUP_GPIO0_88 | Camera #0 Flex Signal (GPIO) | Bi-Dir | Camera Specific (Pin 5a) |
| EXTINTN | GPIO0_0 | HDMI Monitor Detect | Input | Active High Signal '0' – No Monitor Detected (default) '1' – Monitor Detected |
| MCAN13_TX | GPIO0_3 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | Expansion Board Specific (Pin 16) |
| MCAN1_TX | GPIO0_27 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | Expansion Board Specific (Pin 37) |
| MCASP0_AXR8 | GPIO0_36 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | Expansion Board Specific (Pin 13) |
| MCASP0_AXR13 | GPIO0_41 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | Expansion Board Specific (Pin 36) |
| MCASP0_AXR14 | GPIO0_42 | 40pin Expansion Header Signal (GPIO) | Bi-Dir | Expansion Board Specific (Pin 11) |
| ECAP0_IN_APWM_OUT | GPIO0_49 | SD Card IO Voltage Selection | Output | '0' – SD Card IO Voltage is 1.8 V '1' – SD Card IO Voltage is 3.3 V (default) |
| TIMER_IO0 | GPIO0_58 | SD card detect signal | Input | Active Low Signal '0'- SD Card Detected '1'- SD Card Not Detected |
| TIMER_IO1 | GPIO0_59 | USB VBUS Drive signal | Output | Active High Signal '0'- VBUS Disabled '1'- VBUS Enabled |

3.5 I2C GPIO Expander Table

The EVM uses I2C-based IO expander(s) for some peripheral controls. The below table explains the functionality of the pins.

Table 3-4. I2C GPIO Mapping Table

| PORT NO | Net name | Function | Dir/ Level | Remarks |
|---|------------------------|-----------------------------------|---------------|--|
| I2C Bus: I2C0, 0x21 (TCA6416A) | | | | |
| P05 | BOARDID_EEPROM_WP | EEPROM Write Protect | Output | '0' – EEPROM is NOT Write Protected (default) '1' – EEPROM is Write Protected |
| P06 | CAN_STB | CAN Standby signal | Output | '0' – Normal Mode '1' – Standby Mode (default) |
| P10 | GPIO_uSD_PWR_EN | SD Card Power Enable | Output | '0' – SD Card Power Disabled '1' – SD Card Power Enable (default) |
| P12 | IO_EXP_PCl_e1_M.2_RTSz | M.2 Key M Interface Signal (RSTz) | Output | RSTz, See M.2 Key M specification for more details. (Default = '0') |
| P13 | IO_EXP_MCU_RGMII_RST# | Ethernet PHY Reset | Output | '0' – Ethernet is Reset '1' – Ethernet is NOT Reset (default) |
| I2C Bus: I2C1, 0x20 (TCA6408A) | | | | |
| P0 | CSI_VIO_SEL | CSI I2C/GPIO Voltage Selection | Output | '0' – 1.8 V IO (default) '1' – 3.3 V IO |
| P1 | CSI_SEL_FPC_EXPn | CSI Expansion Interface Selection | Output | CSI I2C MUX select '0' – Camera/Flex Selected (default) '1' – 40-pin Camera Expansion Selected |
| P2 | IO_EXP_CSI2_EXP_RSTz | CSI Expansion Signal (RESETz) | Output | '0' – CSI Board is Reset (Default) '1' – CSI Board is NOT Reset |
| P3 | CSI0_B_GPIO1 | Camera #0 Flex Signal (PwrDwn) | Output | Camera Specific '0' – Normal Operation (default) '1' – Power Down |
| P4 | CSI1_B_GPIO1 | Camera #1 Flex Signal (PwrDwn) | Output | Camera Specific '0' – Normal Operation (default) '1' – Power Down |
| I2C Bus: MCU_I2C1, 0x20 (TCA6408A) | | | | |
| P0 | HDMI_PDn | HDMI Transceiver Enable | Output | '0' – Power Down (default) '1' – Normal Operation |
| P1 | HDMI_LS_OE | HDMI Monitor Enable | Output | '0' – Power Down '1' – Normal Operation (default) |
| P2 | DP0_3V3_EN | Display Port Monitor Enable | Output | '0' – Monitor is Disabled (default) '1' – Monitor is Enabled |
| P3 | eDP_ENABLE | DSI to eDP bridge Enable | Output | '1' – Bridge is Enabled(default) '0' – Bridge is Disabled |

Note

In the DIR column, output is to the test automation module, input is from the test automation module. Bi-Dir signals can be configured as either input or output.

3.6 Identification EEPROM

The SK-AM68 board identified and revision information are stored in an on-board EEPROM. The first 259 bytes of memory are pre-programmed with EVM identification information. The format of that data is provided in [Table 3-5](#). The remaining 32509 bytes are available for data or code storage.

The EEPROM is accessible from WKUP I2C0 port of processor at address 0x51 and 0x52

Table 3-5. Board ID memory Header information

| Field Name | Offset / Size | Value | Comments |
|------------|---------------|-------------------------------|--|
| MAGIC | 0000/ 4B | 0xEE3355AA | Header Identifier |
| M_TYPE | 0004/1B | 0x1 | Fixed length and variable position board ID header |
| M_LENGTH | 0005/2B | 0x37 | Size of payload |
| B_TYPE | 0007/1B | 0x10 | Payload type |
| B_LENGTH | 0008/2B | 0x2E | Offset to next header |
| B_NAME | 000A/16B | J7AEP SK SOM/J7AEP BASE BOARD | Name of the board |
| DESIGN_REV | 001A/2B | E1 | Revision number of the design |
| PROC_NBR | 001C/4B | 131/125 | PROC number |
| VARIANT | 0020/2B | 1 | Design variant number |
| PCB_REV | 0022/2B | E1 | Revision number of the PCB |
| SCHBOM_REV | 0024/2B | 0 | Revision number of the schematic |
| SWR_REV | 0026/2B | 1 | First software release number |
| VENDORID | 0028/2B | 1 | |
| BUILD_WK | 002A/2B | | Week of the year of production |
| BUILD_YR | 002C/2B | | Year of production |
| BOARDID | 002E/6B | 0 | |
| SERIAL_NBR | 0034/4B | | Incrementing board number |
| DDR_INFO | TYPE | 1 | |
| | Length | 2 | Offset to next header |
| | DDRcontrol | 2 | DDR Control Word |
| MAC_ADDR | TYPE | 1 | Payload type |
| | Length | 2 | Size of payload |
| | MAC control | 2 | MAC header control word |
| | MAC_adrs | 192 | |
| END_LIST | TYPE | 1 | End Marker |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from January 30, 2023 to October 31, 2025 (from Revision * (January 2023) to Revision A (October 2025))
Page

- Updated the numbering format for tables, figures and cross-references throughout the document..... **1**
- Replaced TDA4VM EAIK with SK-TDA4VM throughout the document..... **1**

-
- Added HDMI trademark information..... 1
-

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3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

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3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/sds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/sds/ti_ja/general/eStore/notice_02.page

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3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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