Technical Article

Why scalable high-performance SoCs are the future of autonomous vehicles

Alec Schott

Summary

The automotive industry is ascending to higher levels of vehicle autonomy with the help of central computing platforms. SoCs like the TDA5 family offer safe, efficient AI performance through an integrated C7™ NPU and chiplet-ready design. These SoCs enable automakers to more easily implement ADAS capabilities, bringing premium features to all types of vehicles, from base models to luxury cars.

Figure 1. Visualization of ADAS features for autonomous driving in a software-defined vehicle analyzing environmental data

Introduction

How long have advanced driver assistance systems (ADAS) and autonomous driving been trendy topics? For the last decade or so, automakers at trade shows have shown consumers visions of a future with roads full of intelligent, autonomous vehicles.

We are finally closer to that vision. You likely have driven in or may even own a vehicle with features that existed only conceptually 10 years ago.

In terms of broad availability and the adoption of intelligent ADAS features and artificial intelligence (AI) capabilities, the industry is progressing through the Society of Automotive Engineers' levels of vehicle autonomy from Level 1 to Level 2 and Level 3. This proliferation of autonomous features is currently occurring in both

domain-based and central computing vehicle architectures. The next, biggest steps toward vehicle autonomy will occur in the latter, with software-defined vehicles (SDVs), as visualized in Figure 1, poised to become the standard vehicle configuration.

This emerging vehicle architecture consolidates traditional distributed electronic control units (ECUs) into powerful central computing platforms, enabling over-the-air updates, feature additions and enhanced functionality throughout a vehicle's lifetime. SDVs use hardware as a platform and software for iterative updates, giving automakers the flexibility to continuously improve a vehicle's capabilities and deliver new autonomous driving features without hardware changes.

SoCs for the next generation of automotive designs

At the core of central computing architectures (Figure 2) are heterogeneous SoCs that integrate a variety of IP blocks and support advanced software, such as the TDA54-Q1, the first device in the TDA5 family of SoCs.

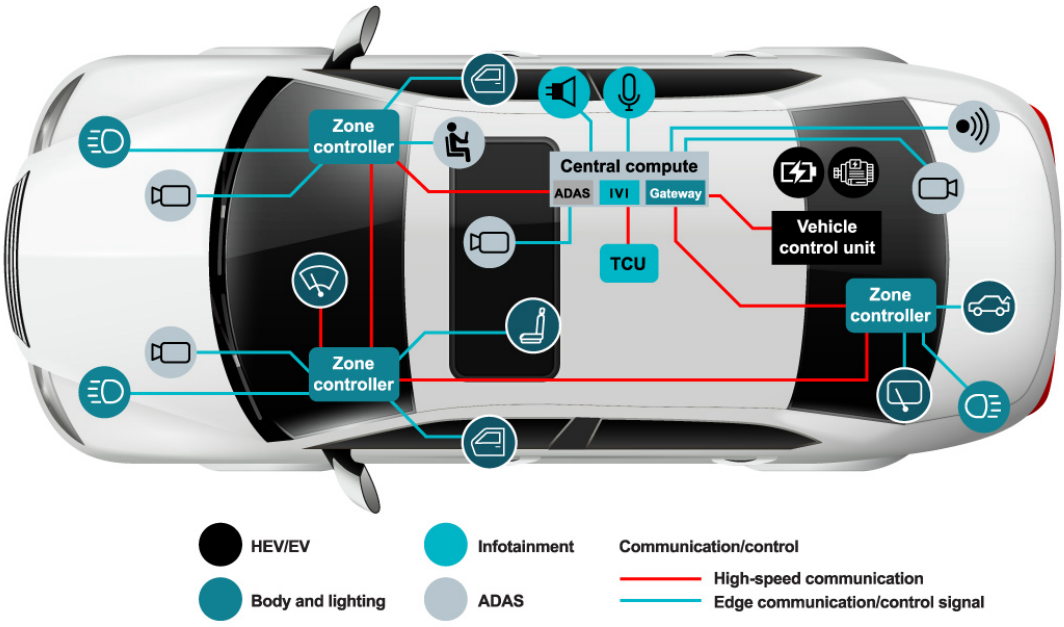

Figure 2. Simplified overview of the central computing architecture and connected systems in a software-defined vehicle

While there are multiple types of high-performance SoCs on the market, SoCs that employ a variety of computing components are more power-efficient and able to increase performance in a central computing ECU when compared to SoCs primarily based on a single type of computing element (such as graphics processing units). SoCs with a variety of computing elements simplify development, deployment and execution of software for advanced autonomous driving features because they can offload specific tasks to their specialized IP blocks, including high-performance neural processing units (NPUs) and vision processors, supported by dedicated onboard memory.

Heterogeneous SoCs such as the TDA54-Q1 bring more autonomous driving capabilities and design flexibility to more vehicles through:

- **Scalable AI performance.** In terms of edge AI capabilities, TDA5 SoCs were designed using the latest automotive qualified 5nm process technology and feature integrated NPUs based on TI's proprietary C7™ digital signal processing architecture. These technologies help deliver an efficient power envelope and scalable AI performance from 10 to 1,200 trillion operations per second (TOPS). Engineers can leverage the AI resources of these SoCs to increase vehicle responsiveness through support for multibillion-parameter

large language models, vision language models and advanced transformer networks. This level of AI performance is scalable over time to meet the evolving needs of different application requirements, from supporting Level 1 features such as adaptive cruise control all the way up to Level 3 autonomy, which covers conditional driving automation or self-driving under specified conditions.

- **Safety-first architecture.** TDA5 SoCs deliver a higher level of specialized performance and efficiency through a cross-domain hardware safety architecture that provides deterministic, real-time monitoring that software cannot achieve alone. Such performance enables OEMs to meet Automotive Safety Integrity Level D, the highest risk classification in the International Organization for Standardization 26262 standard. Using the latest Armv9 cores from Arm®, TDA5 SoCs feature lockstep capabilities in their application and microcontroller cores.
- **Chiplet-ready architecture.** The scalability of the TDA5 SoC family isn't limited to its processing performance; these devices also have a chiplet-ready architecture. Chiplets are an emerging semiconductor architectural design approach where individual integrated circuits serve a similar role as IP blocks in a heterogeneous SoC, allowing for the modular design of specialized chips. Built-in support for the Universal Chiplet Interconnect Express interface open technology standard enables greater scalability and adaptability of TDA5 SoCs through future chiplet extensions, offering developers a future-proof platform that can evolve with their needs.

Conclusion

Over the next decade, ADAS features will become standard and potentially even mandatory. Premium driving features will become mainstream and available for all vehicles, from entry-level base models to luxury cars. With devices like TDA5 SoCs, it's only a matter of time.

Additional resources

- Learn more about the TDA54 Virtualizer™ Development Kit , developed in collaboration between Texas Instruments and Synopsys.
- Read the article, *Accelerating next-generation automotive designs with the TDA5 Virtualizer™ Development Kit*.

Trademarks

All trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025