

TIDA-00423 High-Speed Front-End for PCIe Gen-3 Cards

SVA Datapath Solutions

Abstract

This report summarizes the results of the DS80PCI810 when tested under PCI-SIG repeater requirements for PCIe Gen-3 Tx and automatic link equalization compliance. The DS80PCI810 is a low-power 8 Gbps 8-channel linear redriver that can be combined in the data path with a PCIe Gen-3 add-in card, such as an NVMe or graphics card, for improved signal integrity performance. This reference design provides schematic and layout guidelines to implement the DS80PCI810 repeater in a PCIe system. The tests shown in this report demonstrate the excellent signal conditioning capability of the DS80PCI810 linear repeater not only to improve signal quality through equalization and VOD amplification, but also to preserve the ASIC Tx FIR preshoot and de-emphasis presets to support automatic link equalization.

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1. Introduction

The testing in this report involves the DS80PCI810 PCIe Gen-3 low-power 8 Gbps 8-channel linear repeater. The linear nature of the DS80PCI810 equalization allows the DS80PCI810 to preserve the transmit signal precursor and postcursor used for link training between system root complex (RC) and endpoint (EP). An example of a typical application for the DS80PCI810 is shown in Figure 1.

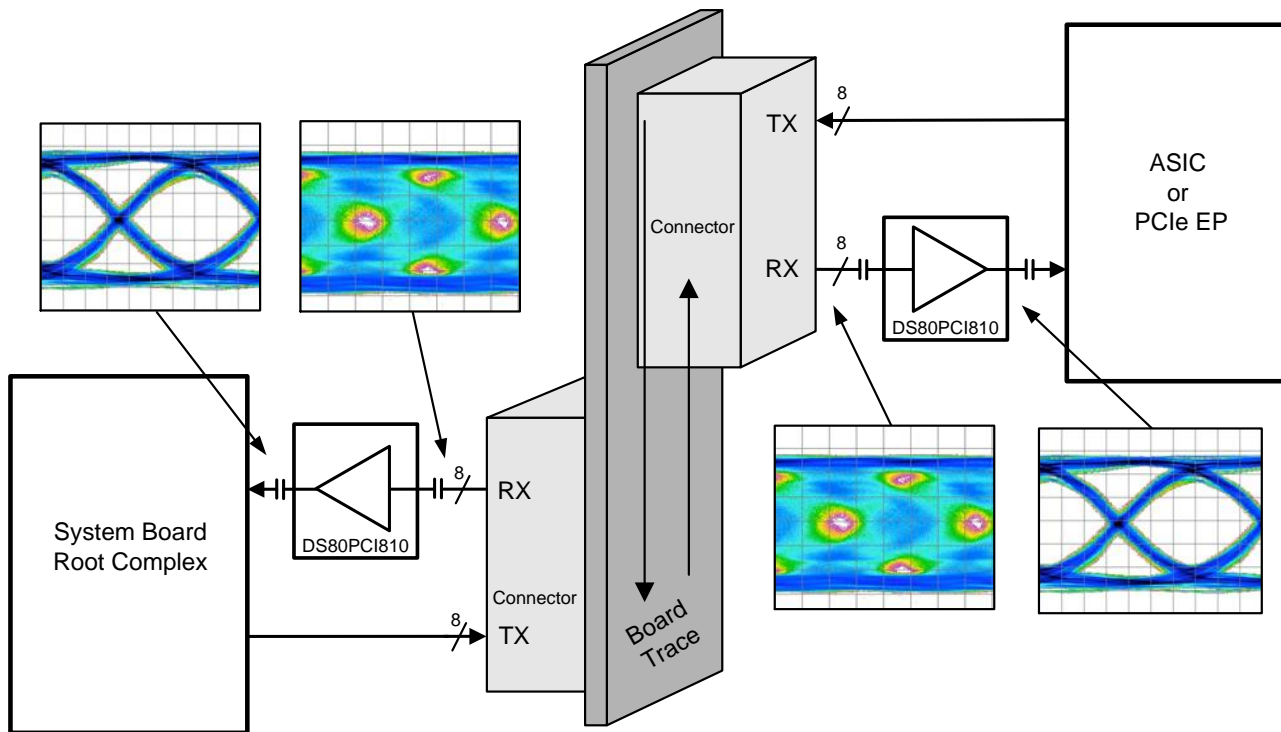


Figure 1. Typical DS80PCI810 Application

The TIDA-00423 Gen-3 riser card reference design provides a practical reference for implementing the DS80PCI810 within the data path for optimal signal integrity performance. Users can use the layout

arrangement shown in this reference design to incorporate the DS80PCI810 into their own PCIe card, such as a graphics card. With four DS80PCI810 ICs on board (two for upstream data and two for downstream data), the TIDA-00423 is a front-end platform for PCIe Gen-3 cards that can be placed mid-channel between a motherboard and add-in card via the PCIe edge finger slots. For this test report, the TIDA-00423 reference design card was tested in combination with a golden graphics card to verify proper behavior under PCIe compliance testing.

2. DS80PCI810 Device Configuration

For all compliance testing, the DS80PCI810s on board were configured to operate in pin mode with the output differential voltage (VOD) set to Level 6. VOD Level 6 provides the highest linearity available between input and output. The EQ was configured to the lowest level (EQ Level 1), since the DS80PCI810 is located within close proximity to the PCIe Gen-3 graphics card. The RXDET pin was set to “Float” in order to auto-detect both downstream and upstream receiver terminations.

Table 1. DS80PCI810 Settings Used for Compliance Testing

EQ Setting		VOD Setting		RXDET	
Value	Pin Strap	Value	Pin Strap	Value	Pin Strap
Level 0	0: 1 kΩ to GND	Level 6	VODA1= VODB1=1 (1 kΩ to VIH) VODA0= VODB0=0 (1 kΩ to GND)	Auto termination detection	F: Floating

A view of the DS80PCI810 board with these pin strap settings is highlighted in Figure 2. For more details about switch settings, refer to Appendix A: TIDA-00423 DIP Switch Setting Notes.

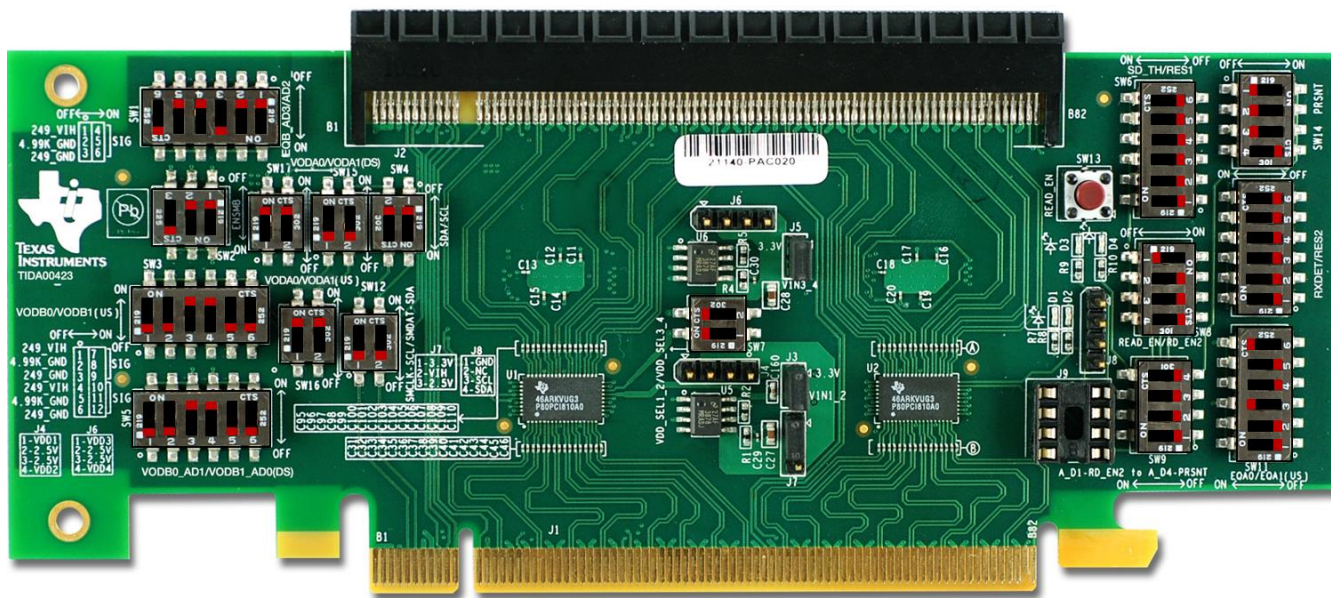


Figure 2. TIDA-00423 Riser Card with Pin Settings described in Table 1

3. PCIe Gen-3 Tx Equalization Testing

PCI-SIG specifies that, for PCIe Gen-3 Tx Equalization compliance, the DUT must be tested at 8 Gbps, where the eye quality under different Tx preset values is evaluated. In addition, the DUT must also pass signal quality tests for previous data rates. The DS80PCI810 and graphics card combination was tested using the PCIe Compliance Base Board (CBB) to prompt the golden graphics card to cycle through preset values at 8 Gbps (Gen-3) as well as Tx compliance patterns for 5 Gbps (Gen-2) and 2.5 Gbps (Gen-1). After the source Tx from the Add-In golden graphics card was passed through the DS80PCI810 on Lane 0, the output was measured by a Tektronix DSA71604 Real-Time Scope. The functional block diagram for this test is shown in Figure 3.

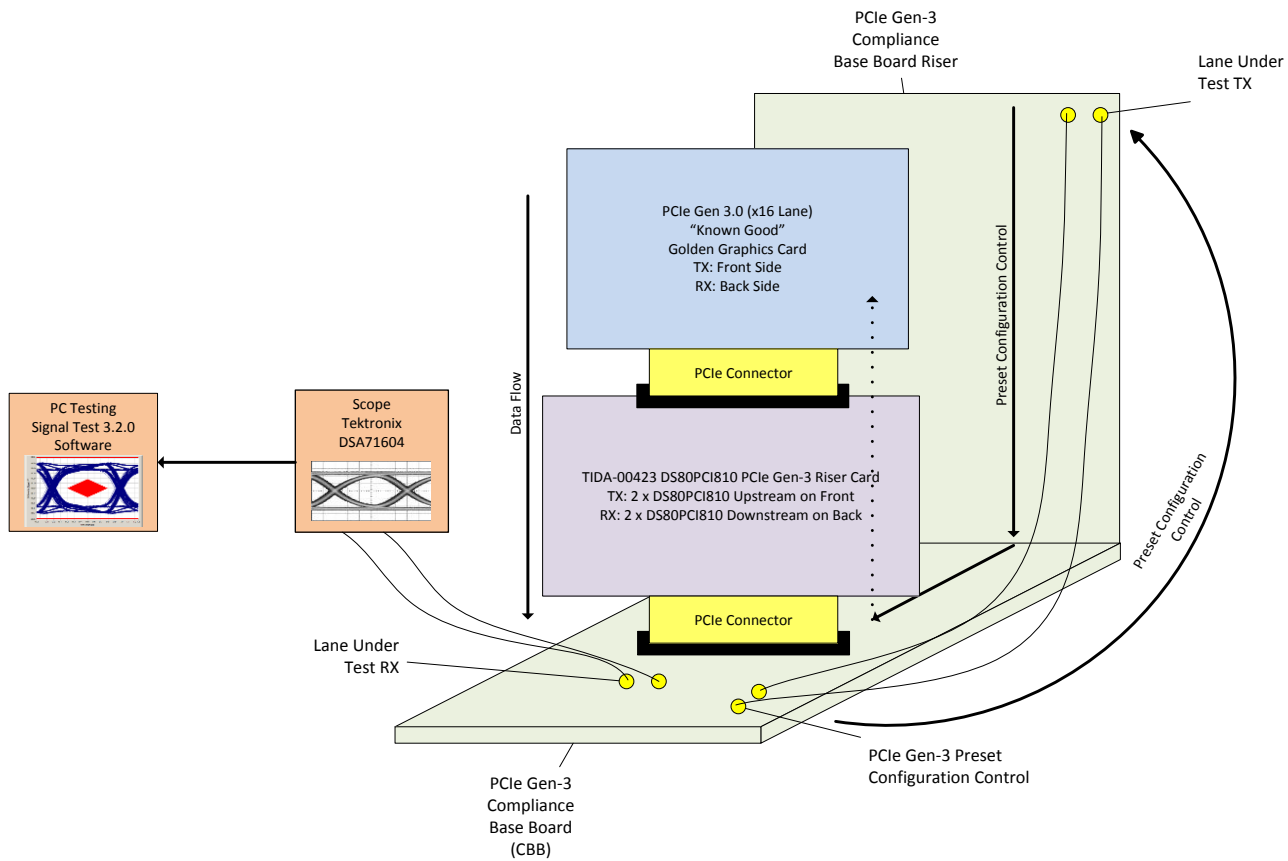


Figure 3. Tx Equalization Setup for PCIe Gen-3 Testing

3.1. PCIe Gen-3 Tx EQ Testing Parametric Results

The results show that the test combination passes PCIe Gen-3 signal integrity compliance tests at 2.5 Gbps, 5 Gbps, and 8 Gbps. These results were found to comply with the signal integrity limits described in the PCIe base specification section 4.3.3.13 and PCIe CEM specification sections 4.8.3, 4.8.2, and 4.8.1.

Table 2. DS80PCI810 Parametric Results at 2.5 Gbps and 5 Gbps¹

Sigttest	2.5Gbps	5Gbps - 3.5dB	5Gbps - 6dB
Overall Sigttest Result	Pass!	Pass!	Pass!
Mean Unit Interval (ps)	400.027404	200.013705	200.013688
Max Unit Interval (ps)	400.03089	193.79088	193.722838
Min Unit Interval (ps)	400.024481	4.999657	4.999658
Min Time Between Crossovers (ps)	393.675794	43.164744	53.397347
Data Rate (Gb/s)	2.499829	54.953644	64.837914
Per Edge RMS Jitter (ps)	9.773846	145.046356	135.162086
Mean Median to Peak Jitter (ps)	30.572091	13.14934	22.469588
Max Median to Peak Jitter (ps)	41.331154	2.973279	3.013395
Min Median to Peak Jitter (ps)	25.313324	-0.4684	-0.4612
Mean Peak to Peak Jitter (ps)	46.122963	0.46	0.46
Max Peak to Peak Jitter (ps)	60.62883	-0.4348	-0.392
Minimum eye width (ps)	339.37117	0.4324	0.386
Min Peak to Peak Jitter (ps)	40.331998	0.631882	0.476433
Minimum Transition Eye Voltage (V)	-0.5412	0.5	0.5
Maximum Transition Eye Voltage (V)	0.54	0.173797	0.223194
Composite Eye Height	0.542117	-0.180557	-0.221835
Composite Eye Location	0.5	0.734354	0.751029
Minimum Transition Eye Voltage Margin Above Eye (V)	0.041778	0.123275	0.103901
Minimum Transition Eye Voltage Margin Below Eye (V)	-0.047894	-0.128607	-0.112531
Minimum Transition Eye Height (V)	0.603672	0.631882	0.476433

Table 3. DS80PCI810 Parametric Test Results at 8 Gbps

Sigttest	Preset 0	Preset 1	Preset 2	Preset 3	Preset 4	Preset 5	Preset 6	Preset 7	Preset 8	Preset 9	Preset 10
Overall Sigttest Result	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!	Pass!
Mean Unit Interval (ps)	125.009	125.009	125.009	125.009	125.009	125.009	125.009	125.009	125.009	125.009	125.009
Min Time Between Crossovers (ps)	103.747	102.102	101.657	99.746	96.609	104.313	103.616	106.528	107.018	107.702	106.483
Data Rate (Gb/s)	7.999	7.999	7.999	7.999	7.999	7.999	7.999	7.999	7.999	7.999	7.999
Max Peak to Peak Jitter(ps)	41.982	34.513	35.779	29.913	34.530	33.297	34.705	40.480	37.045	39.537	45.913
Total Jitter at BER of 10E-12(ps)	42.241	34.064	36.182	30.021	33.913	33.068	33.225	40.147	37.016	39.212	45.487
Minimum eye width(ps)	82.759	90.936	88.818	94.979	91.087	91.932	91.775	84.853	87.984	85.788	79.513
Deterministic Jitter Delta-Delta(ps)	34.722	27.095	28.850	23.201	27.383	26.387	26.622	32.727	29.967	32.198	37.752
Random Jitter (RMS)	0.535	0.496	0.522	0.485	0.464	0.475	0.470	0.528	0.501	0.499	0.550
Minimum Transition Eye Voltage(volts)	-0.177	-0.189	-0.190	-0.190	-0.198	-0.185	-0.176	-0.163	-0.163	-0.150	-0.142
Maximum Transition Eye Voltage(volts)	0.170	0.183	0.184	0.184	0.198	0.185	0.176	0.158	0.159	0.147	0.139
Minimum Non Transition Eye Voltage(volts)	-0.175	-0.189	-0.193	-0.192	-0.201	-0.191	-0.178	-0.163	-0.163	-0.152	-0.142
Maximum Non Transition Eye Voltage(volts)	0.171	0.184	0.186	0.187	0.200	0.187	0.178	0.157	0.158	0.150	0.139
Composit Eye Height	0.116	0.134	0.133	0.139	0.137	0.147	0.135	0.124	0.131	0.119	0.091
Composit Eye Location	0.448	0.444	0.444	0.436	0.464	0.448	0.464	0.500	0.480	0.452	0.480
Minimum Transition Eye Voltage Margin Above Eye(volts)	0.039	0.044	0.044	0.046	0.045	0.049	0.042	0.037	0.039	0.036	0.026
Minimum Transition Eye Voltage Margin Below Eye(volts)	-0.043	-0.047	-0.046	-0.049	-0.044	-0.050	-0.045	-0.041	-0.043	-0.034	-0.027
Minimum Transition Eye Height(volts)	0.132	0.142	0.141	0.145	0.139	0.149	0.137	0.129	0.132	0.120	0.103
Minimum Non Transition Eye Voltage Margin Above Eye(volts)	0.043	0.053	0.050	0.054	0.054	0.064	0.058	0.049	0.052	0.042	0.026
Minimum Non Transition Eye Voltage Margin Below Eye(volts)	-0.042	-0.051	-0.050	-0.052	-0.056	-0.063	-0.056	-0.052	-0.053	-0.039	-0.031
Minimum Non Transition Eye Height(volts)	0.135	0.154	0.151	0.156	0.160	0.177	0.163	0.151	0.155	0.131	0.108
CTLE equalization index	7	6	7	5	3	4	3	7	5	3	7

¹ Testing at 5 Gbps requires signal quality tests for two Tx de-emphasis levels: -3.5 dB and -6.0 dB.

3.2. PCIe Gen-3 Tx EQ Testing Eye Diagrams

The data in the following sections shows Tx EQ eye diagram test results for 2.5 Gbps, 5 Gbps, and 8 Gbps analyzed by the PCI-SIG SigTest 3.2.0 software package. All eyes pass PCIe Gen-1, Gen-2, and Gen-3 signal quality requirements.

3.2.1. Eye Diagram at 2.5 Gbps

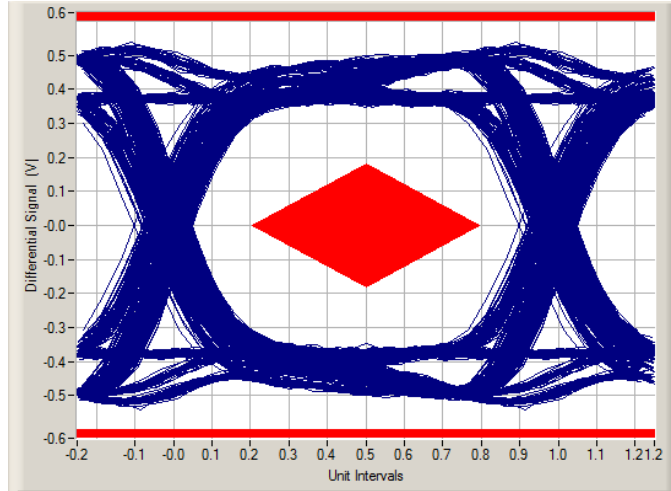


Figure 4. Eye Diagram at 2.5 Gbps

3.2.2. Eye Diagram at 5 Gbps

Table 4. Non Transition Eye Diagrams at 5 Gbps

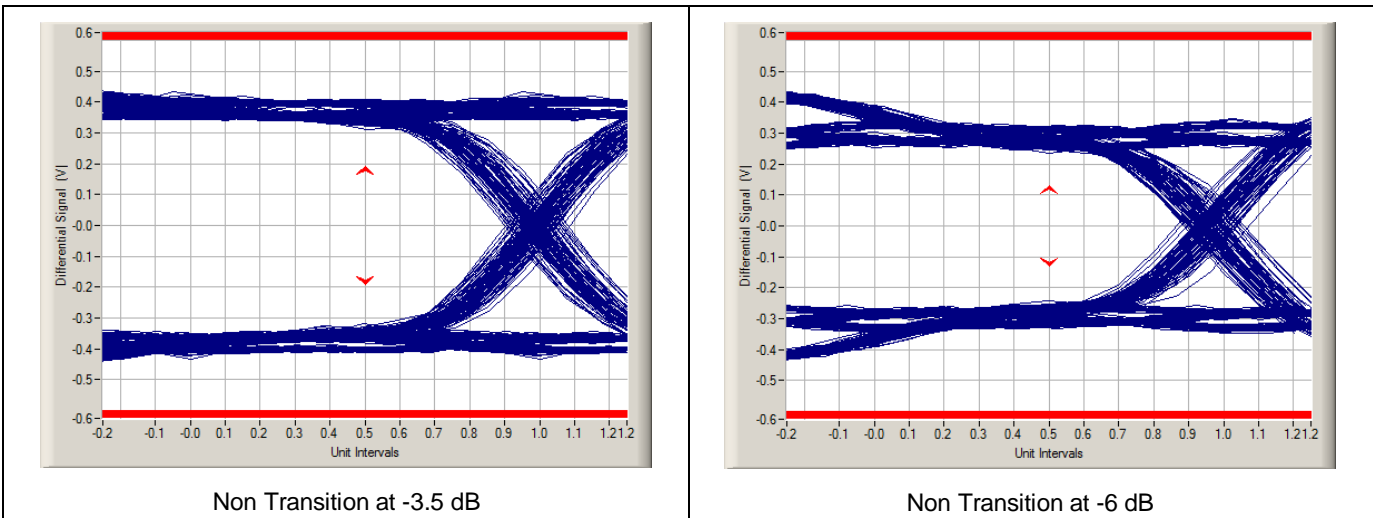
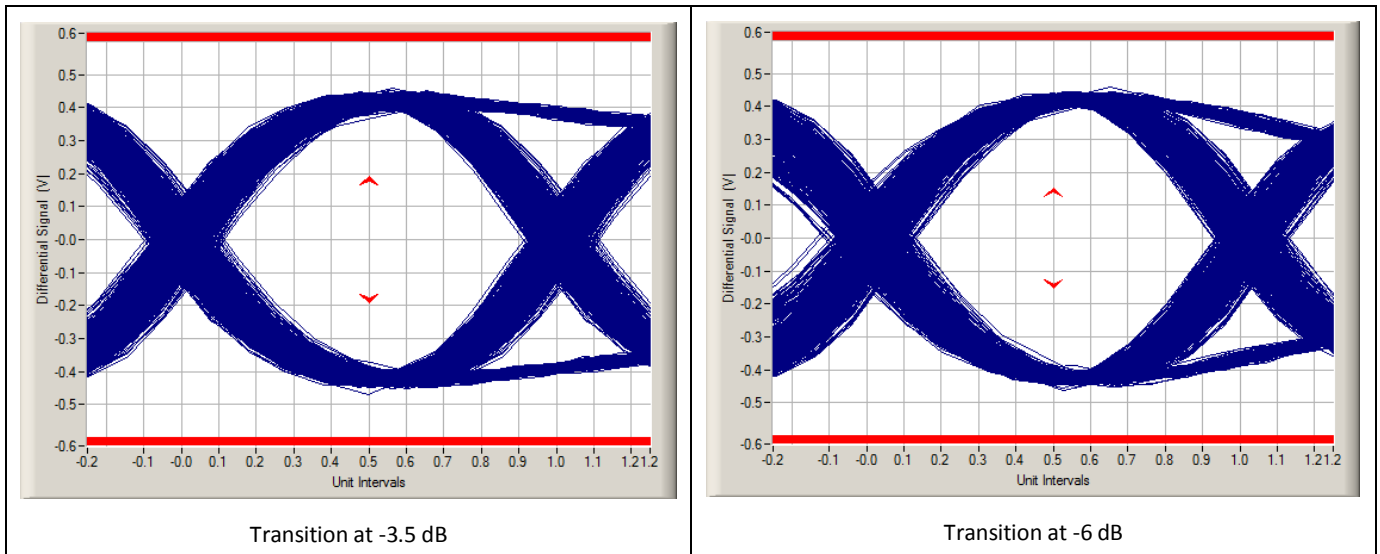
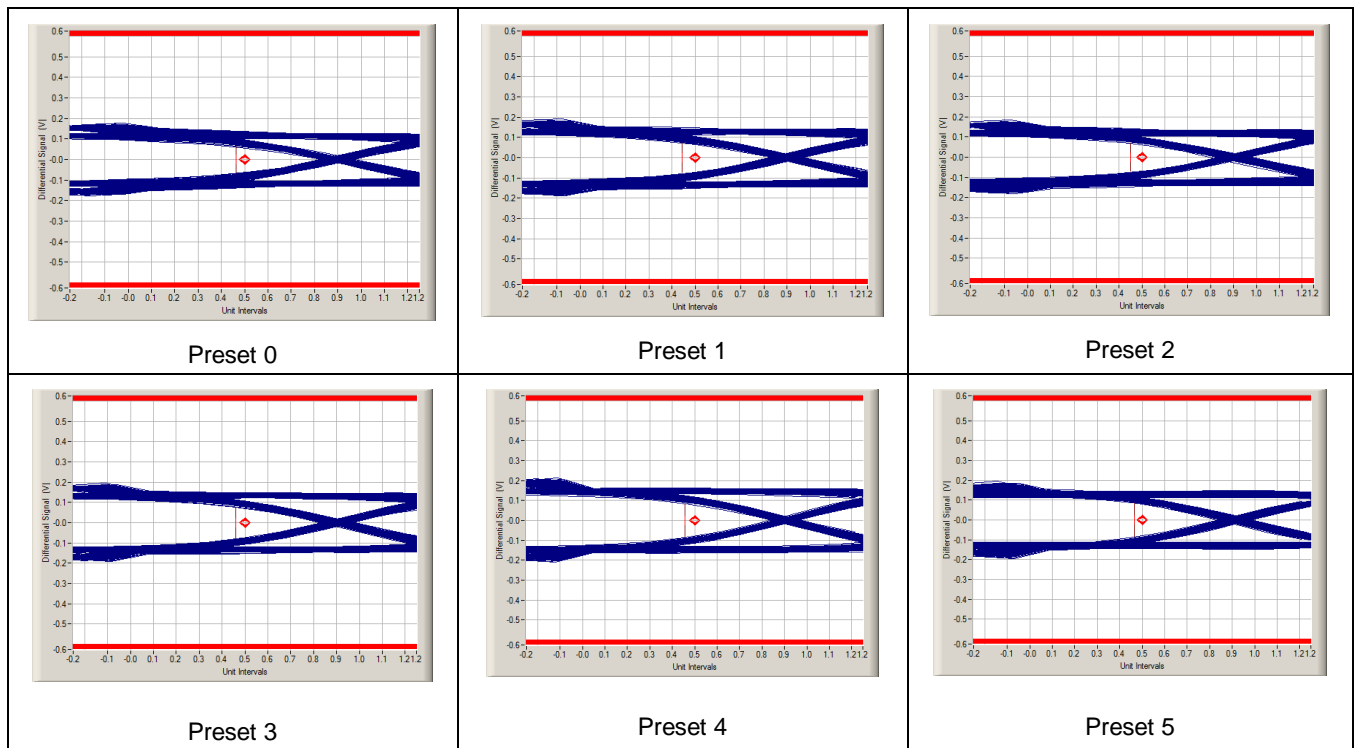


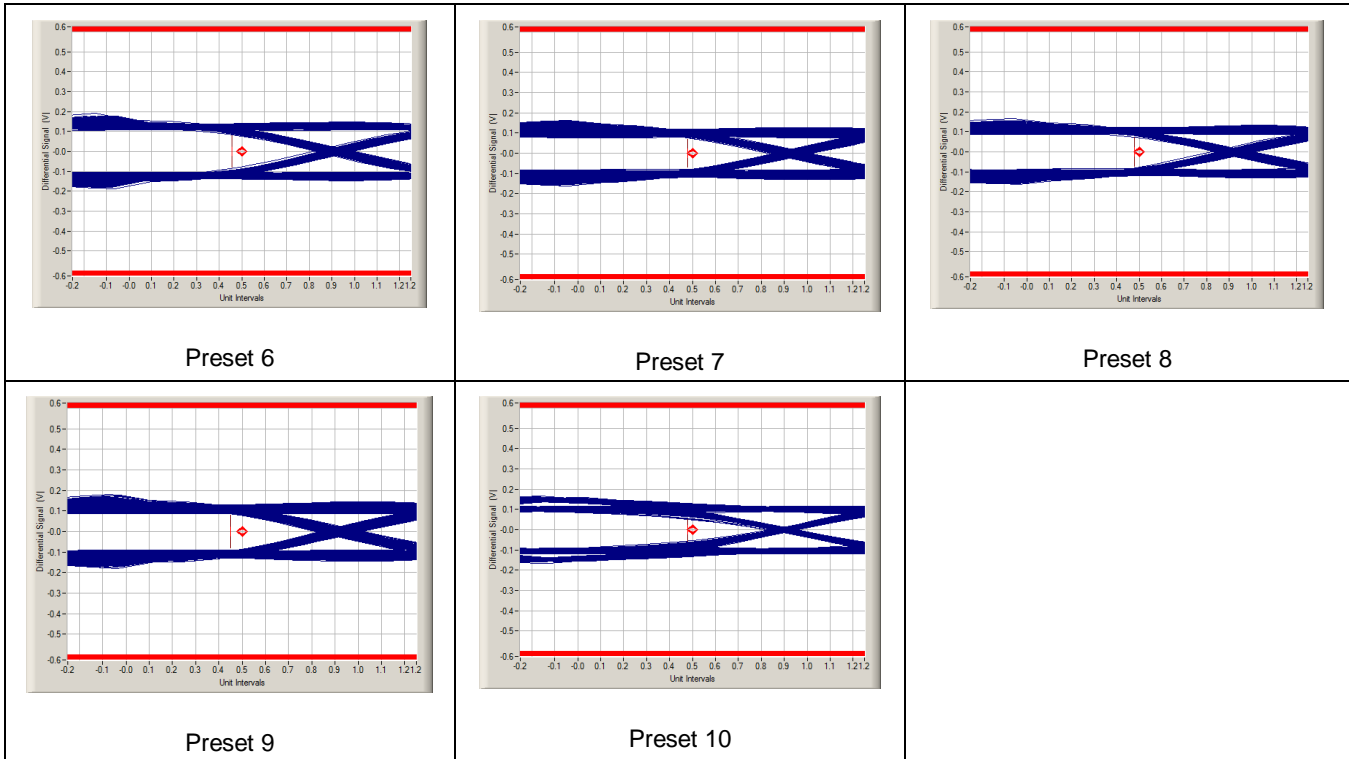
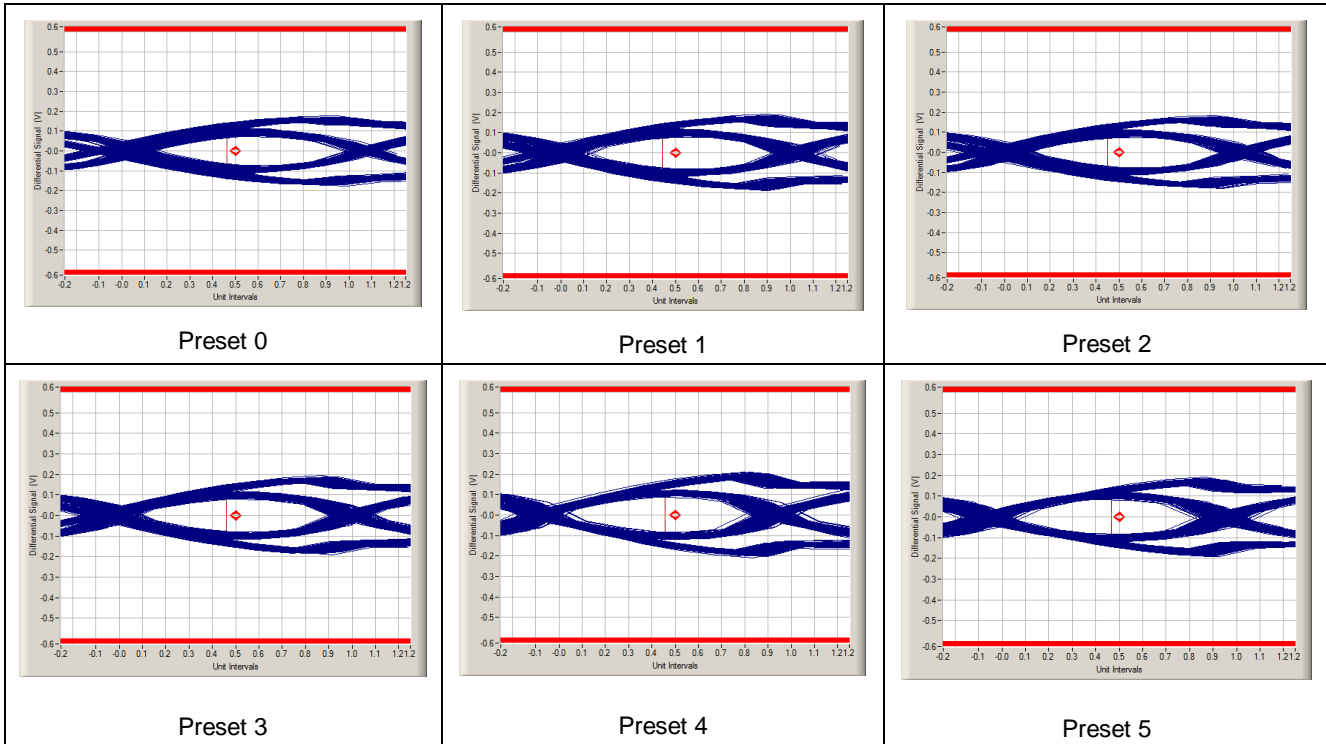
Table 5. Transition Eye Diagrams at 5 Gbps

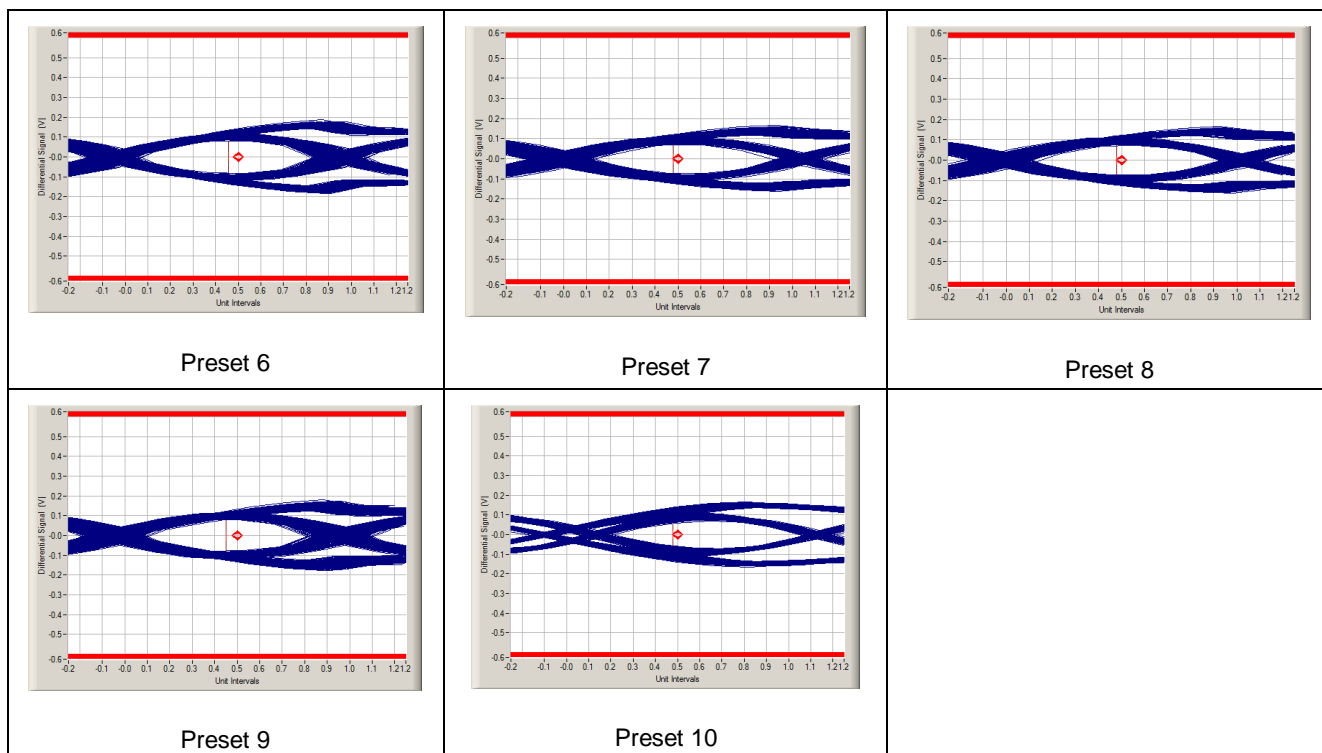


3.2.3. Eye Diagram at 8 Gbps

Table 6. Non Transition Eye Digrams at 8 Gbps




Table 7. Transition Eye Diagrams at 8 Gbps




3.3. PCIe Gen-3 Tx EQ Preset Margin Results

For PCIe Gen-3 Tx EQ compliance, the DUT is also required to generate the necessary preshoot and de-emphasis Tx FIR levels within the margins for presets P0-P9 shown in Table 8.

Table 8. PCIe Gen-3 Tx Preset Ratios and Corresponding Coefficient Values²

Preset Number	Preshoot (dB)	De-emphasis (DB)	C_{-1}	C_{+1}
P4	0.0	0.0	0.000	0.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167
P0	0.0	-6.0 ± 1 dB	0.000	-0.250
P9	3.5 ± 1 dB	0.0	-0.166	0.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125
P7	3.5 ± 1 dB	-6.0 ± 1 dB	-0.100	-0.200
P5	1.9 ± 1 dB	0.0	-0.100	0.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125
P2	0.0	-4.4 ± 1 dB	0.000	-0.200

Figure 5 shows the preset results with the DS80PCI810 inserted in the data path. Figure 6 shows the preset results for the golden graphics card without the DS80PCI810. The difference between Preset 1 for the golden graphics card versus Preset 1 with the DS80PCI810 is approximately 0.7 dB. Table 9 summarizes the delta observed when using Preset 1 and Preset 9 with and without the DS80PCI810 inserted.

² P10 boost limits are determined by the Low Frequency level that the Tx advertises during training. For a full-swing transmitter, P10 specifies 0.0 dB preshoot and -9.5 ± 1.5 dB de-emphasis. It is uncommon for a PCIe Tx-Rx pair to declare P10 as the optimal link negotiation setting. Thus, the P10 de-emphasis level is widely regarded as an informative test to determine the maximum source Tx de-emphasis capability.

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It is normal to expect some change in the measured preset preshoot and de-emphasis values when comparing the source output directly versus the output of the DS80PCI810 repeater after the source Tx. The DS80PCI810 repeater does not create preshoot or de-emphasis on its own. Rather, the DS80PCI810 is designed to be transparent to the preshoot and de-emphasis present at its input with minimum distortion through the repeater. This transparency evident in Figure 5 and Figure 6 makes the DS80PCI810 an ideal candidate for systems that rely heavily on the root complex and endpoint preshoot and de-emphasis capabilities.

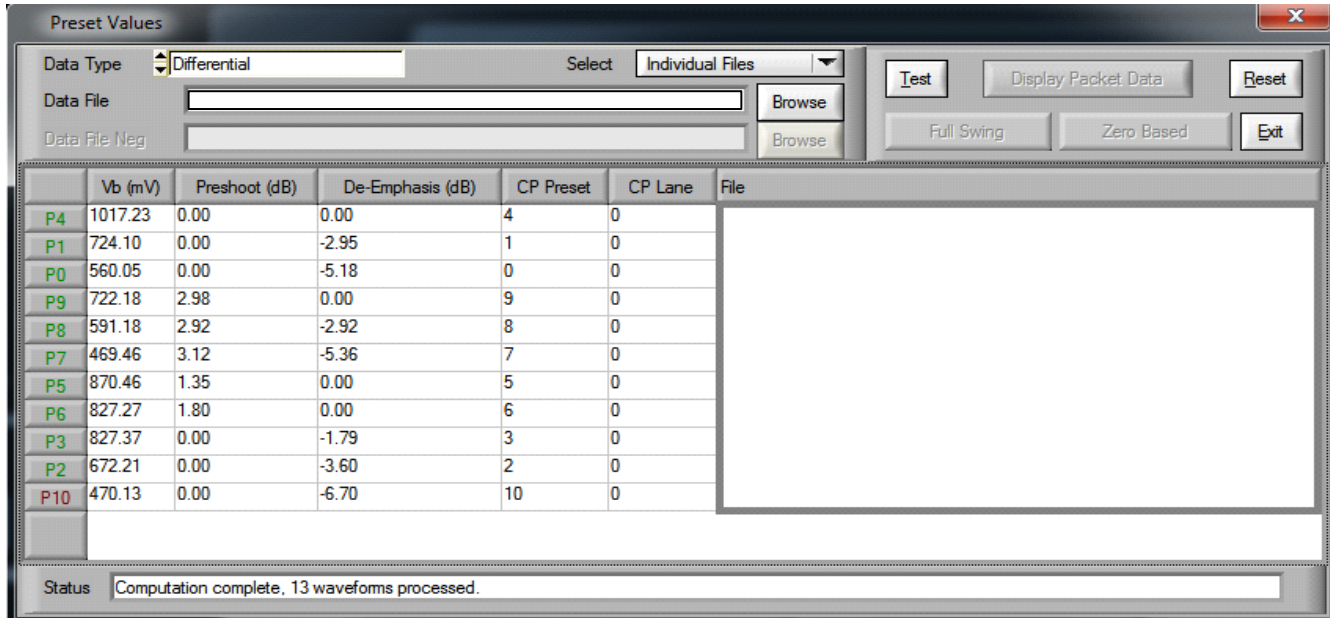


Figure 5. SigTest 3.2.0 Tx Preset Test Results with Golden Graphics Card + DS80PCI810

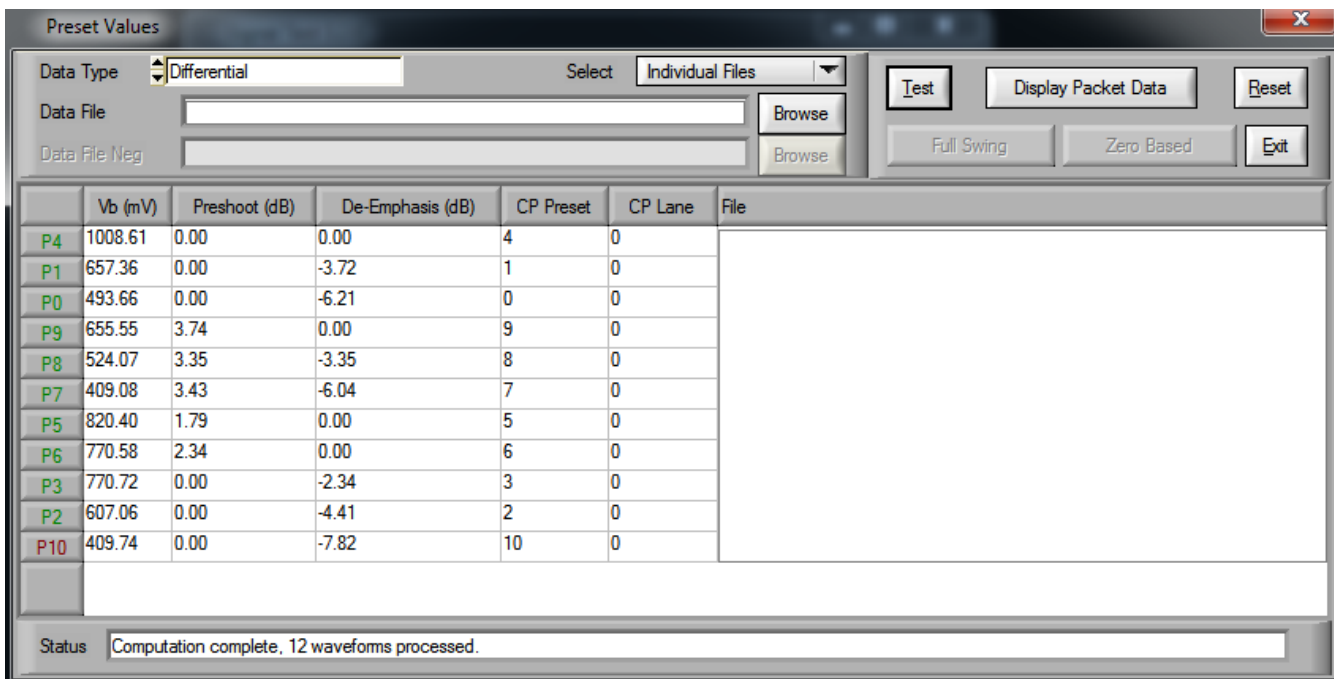


Figure 6. SigTest 3.2.0 Tx Preset Test Results with Golden Graphics Card Only

Table 9. Comparison of Source + DS80PCI810 Output and Source Tx Only Output

Condition	Preset 1	Preset 9
(1) Graphics Card + DS80PCI810	-2.95 dB	2.98 dB
(2) Graphics Card Only	-3.72 dB	3.74 dB
Delta between Condition (1) and (2)	0.77 dB	0.76 dB

4. PCIe Gen-3 Link Equalization Testing

The DS80PCI810 and graphics card combination was also tested for automatic link equalization compliance. To comply with automatic link equalization requirements, the Tx EQ and Rx EQ must change dynamically at run-time in order to work at the highest advertised bit rates in the most optimal setting. Details about automatic link equalization functionality can be found in the PCIe Base Specification, sections 4.2.3, 4.2.4, and 4.2.10.

When automatic link equalization is tested, the following channel flow is expected:

1. Tx implements FIR equalization using one of 11 possible presets.
2. The Rx implements a behavior equalization algorithm with its CTLE, DFE, and CDR.
3. After adjusting its own settings, the Rx requests the Tx to adjust FIR settings dynamically at runtime to find a combination that yields 1E-12 BER or better.

To implement automatic link equalization testing, the DS80PCI810 and graphics card combination was tested with a LeCroy Protocol Aware BERT and a Lecroy Real-Time Scope, as shown in Figure 7.

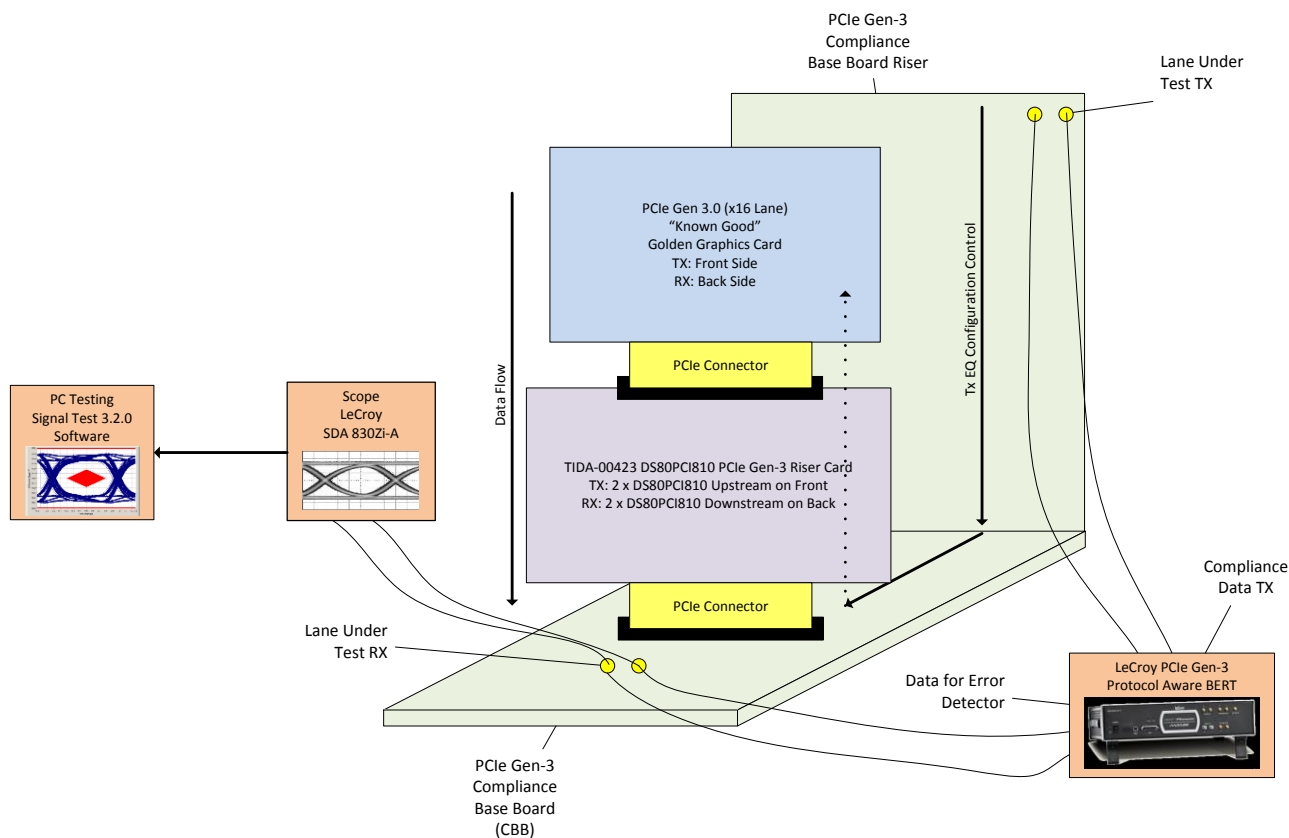


Figure 7. Link Equalization Setup for PCIe Gen-3 Testing

4.1. PCIe Gen-3 Rx Link EQ Test Results

With the DS80PCI810 in the data path, the DUT was first tested for initial Tx preset levels. The required initial preset values for testing link EQ were taken from P0-P9. Results are shown in Figure 8.

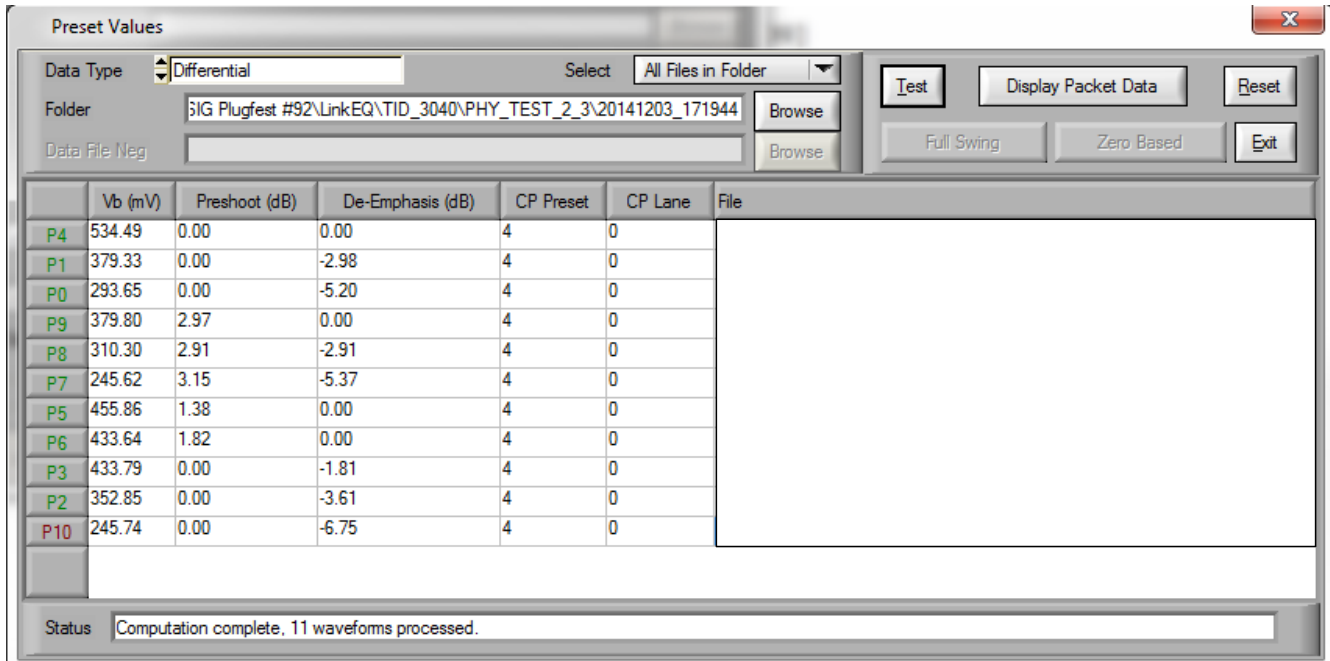


Figure 8. Measured Initial Tx EQ Preset Values from DS80PCI810 and Golden Graphics Card

Once Tx preset values were verified, the DUT was tested to respond to an Rx request to change each Tx preset, cycling from P0-P9. During this time, the response was monitored for proper Tx EQ output levels and response time. Results of the response output presets are shown in Figure 9.

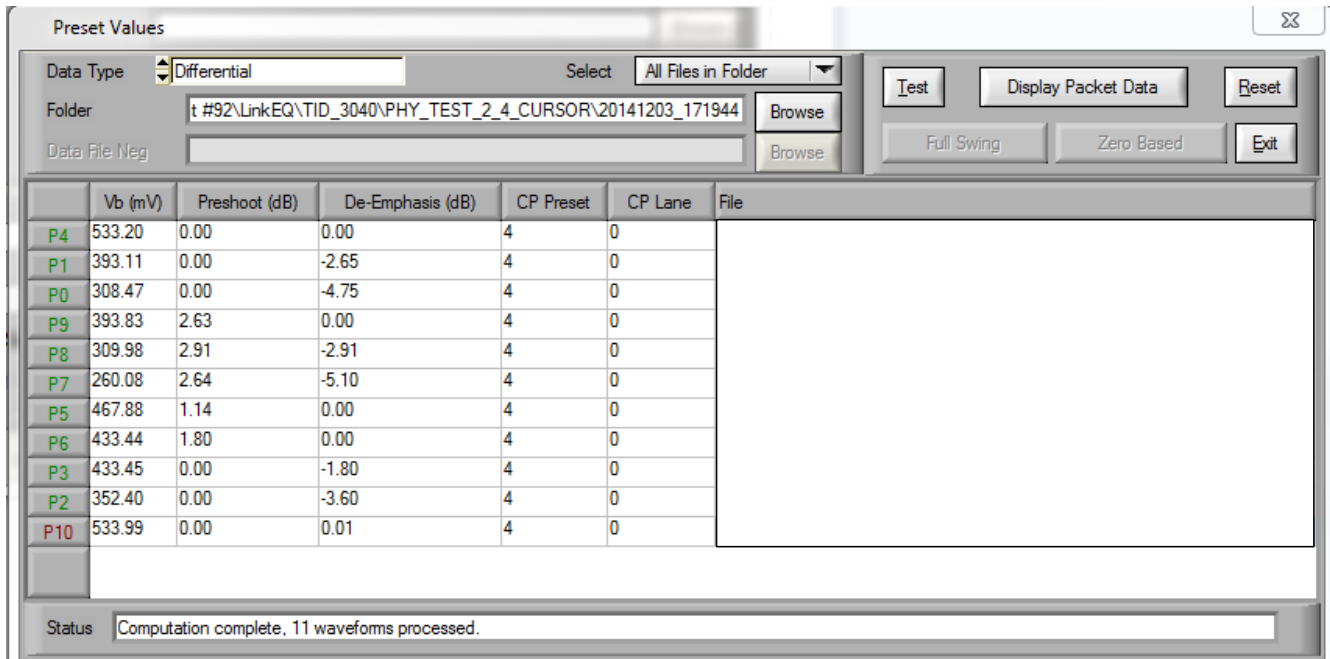


Figure 9. Measured Tx EQ Responses to Link Equalization Preset Requests

On the oscilloscope, the DUT responded to Tx EQ change requests with a delay of approximately 200 ns, significantly less than the maximum 500 ns response time allowed.

4.2. PCIe Gen-3 Rx Link EQ BER Test Results

After verifying that the DUT responded correctly to all Preset Tx FIR requests, the LeCroy BERT initiated a link-training procedure, with Tx Preset P7 as the default starting preset. During link-training, the DUT auto-negotiated an optimal Tx preset value for data transmission. After completion of automatic link equalization, a compliance pattern was then sent for 125 seconds, the amount of time for the Rx to measure 1E12 bits at 8 Gbps. To pass, a maximum of one error is allowed during this time. In the test log shown in Figure 11, the DUT negotiated Preset P1 as the optimal preset value, and several repeated BER tests revealed zero errors after 1E12 bits were measured by the BERT error detector.


 TELEDYNE LECROY	
Title:	PCIe 3.0 Link Equalization Compliance Test Report
Test Spec:	PCI Express Architecture PHY Test Specification 3.0
Score:	PASS (partial)
<hr/>	
Date/Time:	2014-12-03 17:19:44
Equipment:	Phoenix 8211 Software 2.60.475 with SDA820Zi-A LCRY0436N68015 Firmware 7.6.1.1 (build 204282)
Procedure:	Script PCIe_3.0_LEQ_1.0.2
Device:	DS80PCI810 + Golden Graphics Card (AIC)
<hr/>	
PHY Test Headings	Score Comment
PHY_TEST_2_3	PASS
PHY_TEST_2_4_PRESET	PASS
PHY_TEST_2_4_CURSOR	PASS

Figure 10. Link Equalization Results after Link EQ Preset and BER Testing

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Below is an excerpt from the Link Equalization test log:

```

INFO:root:*****
INFO:root:This is the PCIe Gen3 Automatic Link Equalization Test log.
INFO:root:PCIe_3.0_LEQ_1.0.2
DEBUG:root:Verbose logging is enabled
INFO:root:Begin Receiver Testing 2014-12-03 17:11:56
INFO:root:Results file tag for this run is: 20141203_171156
INFO:root:Results path: D:\PCI-SIG\WS92\Python.rev1.0.2\Results\LinkEQ\DS80PCI810
INFO:root:Scope virtual probe function enabled, parameters [R, L, C, Z, Td] = [40.0, 0.0, 5e-13, 50.0, 2.96e-09]
INFO:root:Change preset (P1).
INFO:root:PASS (Bits=1.0e+12 Errors=0.0e+00 BER=0.0e+00 TxEQ=[-6.0, 6.0])
INFO:root:Began Compliance Test 2014-12-03 17:11:56
INFO:root:Ended Compliance Test 2014-12-03 17:14:52
INFO:root:Ended Compliance Test 2014-12-03 17:19:07
INFO:root:*****
INFO:root:This is the PCIe Gen3 Automatic Link Equalization Test log.
INFO:root:PCIe_3.0_LEQ_1.0.2
DEBUG:root:Verbose logging is enabled
INFO:root:Begin Receiver Testing 2014-12-03 17:19:44
INFO:root:Results file tag for this run is: 20141203_171944
INFO:root:Results path: D:\PCI-SIG\WS92\Python.rev1.0.2\Results\LinkEQ\DS80PCI810
INFO:root:Scope virtual probe function enabled, parameters [R, L, C, Z, Td] = [40.0, 0.0, 5e-13, 50.0, 2.96e-09]
INFO:root:Change preset (P1).
INFO:root:Measured bit rate 2.5 GT/s
INFO:root:Measured bit rate 7.99999 GT/s
INFO:root:Measured bit rate 2.5 GT/s
INFO:root:Measured bit rate 7.99999 GT/s
INFO:root:Measured bit rate 2.5 GT/s
INFO:root:Measured bit rate 7.99999 GT/s
INFO:root:Measured bit rate 2.5 GT/s
INFO:root:Measured bit rate 7.99999 GT/s
INFO:root:Measured bit rate 2.5 GT/s
INFO:root:Measured bit rate 7.99999 GT/s
INFO:root:Measured bit rate 2.5 GT/s
INFO:root:Measured bit rate 7.99999 GT/s
INFO:root:Measured bit rate 2.5 GT/s
INFO:root:Measured bit rate 7.99999 GT/s
INFO:root:Measured bit rate 2.5 GT/s
INFO:root:Measured bit rate 7.99828 GT/s
INFO:root:Measured bit rate 2.5 GT/s
INFO:root:Measured bit rate 7.99828 GT/s
INFO:root:Measured bit rate 2.5 GT/s
INFO:root:Measured bit rate 7.99958 GT/s
INFO:root:Presets Grade: PASS
INFO:root:Began Compliance Test 2014-12-03 17:19:44
INFO:root:Ended Compliance Test 2014-12-03 17:48:03

```

Figure 11. Link Equalization Test Log of BER Measurements

5. Summary

The TIDA-00423 design is a high-speed front-end for PCIe Gen-3 cards that allows users to incorporate TI repeaters into the data path between PCIe Gen-3 root complex and add-in card. Through this design, users can reference the schematic and layout arrangement to include the DS80PCI810 into PCIe card designs of their own. This report summarizes the results of the DS80PCI810 redriver when tested under PCI-SIG repeater requirements for PCIe Gen-3 Tx and automatic link equalization compliance. The results of this test report show that the DS80PCI810 riser card can be combined with a golden graphics card successfully to pass critical PCIe Tx and automatic link equalization requirements for PCIe Gen-3 repeaters.

Appendix A: TIDA-00423 DIP Switch Setting Notes

- On this riser card, Downstream => U1, U2. Upstream => U3, U4.
- In the notation of EQ and VOD below, “x” means that the settings apply to both A- and B-channels.
- Both downstream device settings are controlled by the same switches. Both upstream device settings are controlled by the same switches.

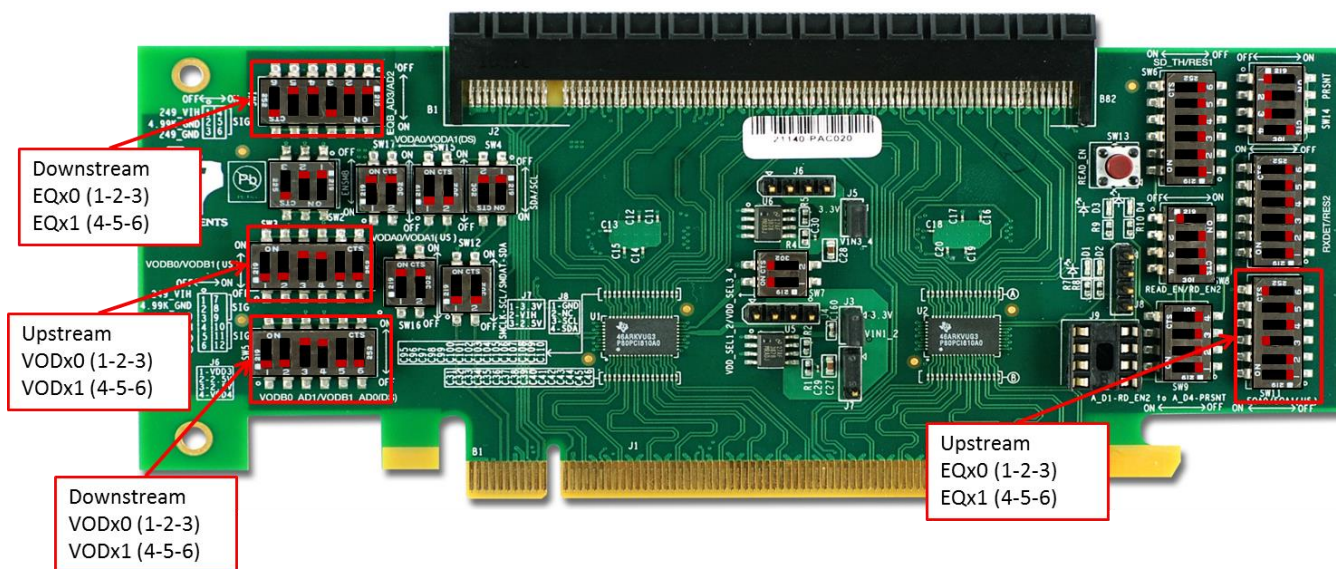


Figure 12. TIDA-00423 with Description of Recommended DIP Switch Settings

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