Design Guide: TIDA-080009

Portable, Smallest 1080p Display Reference Design Using TI DLP® Technology

Description

This reference design features the DLP® Pico™ Products p23-inch TRP 1080p display chipset and is implemented in the DLP LightCrafter™ Display 230NP evaluation model (EVM). The design incorporates the DLP230NP 1080p digital micromirror device (DMD), DLPC3436 display controller, and the DLPA2005 PMIC, and LED driver. The design enables the development of a p23 1080p DLP product with a small form factor interfacing to a low-cost processor, similar to the BeagleBone Black and Raspberry Pi. The design can be used in a variety of applications including mobile projectors, appliances, mobile smart TV, and many more. This reference design includes electronics and optics along with a connector to easily interface with the Raspberry Pi 4B.

Features

- Affordable evaluation of 1080p DLP display technology
- Plug and play DLP 1080p optical engine supporting < 100 lumens
- I^2C and 18-bit parallel RGB video interfaces to support low-cost embedded processors
- Compact form factor
- Raspberry Pi 4 compatibility

Applications

- Personal Electronics
- Portable Electronics, Gaming
- Appliances
- Wearables, (Non-Medical)

Resources

TIDA-080009	Design Folder
DLP230NP	Product Folder
DLPC3436	Product Folder
DLPA2005	Product Folder

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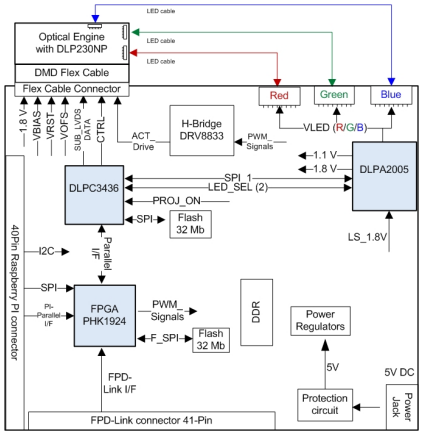

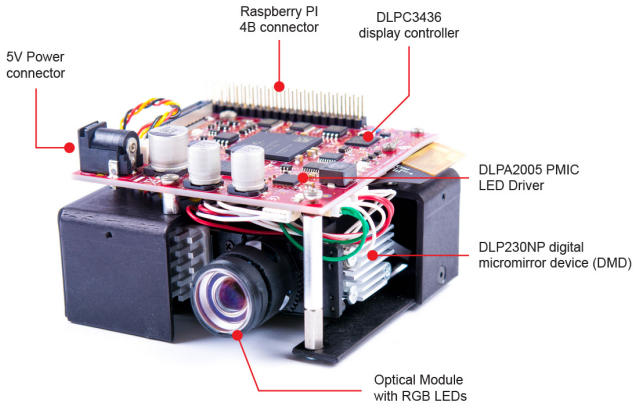

1 System Description

The .23-inch TRP 1080p display chipset enables the use of DLP technology in a variety of applications that require 1080p resolution, low power, and a very small form factor. This reference design provides developers the ability to quickly implement a full 1080p display subsystem using a Raspberry Pi 4B as low-cost front-end processor.

1.1 Applications for Smart Home and IoT

Smart home is a broad category of products and services that bring automation and inter connectivity to a variety of devices in the home, such as lighting, thermostats, appliances, and entertainment devices.

Bringing smart displays based on DLP Pico™ technology into the home can offer many benefits such as interactive, adaptive, and reconfigurable interfaces that can replace buttons, tablets, LCD panels, and mechanical knobs in virtually every room of the house. DLP technology-based smart displays offer advantages in brightness, resolution, small form factor, low power consumption, throw ratio, and interactivity.

Find more about smart home displays using DLP technology in the white paper *TI DLP Pico Technology for Smart Home Applications*.

Table 1-1. DLP Features and Design Benefits for Smart Home Applications

DLP FEATURE	DESIGN BENEFIT
Displays of any shape on virtually any surface	Smart displays using DLP chips can project directly onto existing surfaces in the home, delivering convenient information just about anywhere.
On-demand display	Smart home projection can instantly provide a display without the intrusion of a permanent display panel. In addition, DLP Pico technology enables small optical module designs that can be tucked out of sight or be integrated into existing home devices.
High optical efficiency	Digital micromirror devices (DMDs) incorporate highly reflective and polarization agnostic aluminum micromirrors, which enable bright, power-efficient, compact smart home display systems.
High resolution	DLP Pico DMDs enable high-resolution projected images—up to Full HD 1080p resolution.
Solid-state illumination compatible	DLP chips are compatible with solid-state illumination, such as LEDs and lasers, which further enables compact sizes and long illumination lifetimes.

1.2 Applications for Mobile Smart TVs and Mobile Projectors

Mobile projectors can be used as a portable big-screen display for any device with video output, such as laptops, smart phones, tablets, and gaming consoles. These projectors can offer users an easy and lightweight means to project large and colorful videos in a variety of settings.

Mobile smart TV products combine three exciting technologies: Wireless connectivity, video content streaming, and pico projection. A mobile smart TV can stream wireless the internet content and project it onto virtually any surface. To learn more about mobile smart TVs and mobile projectors, go to the DLP Pico Applications Portal.

Table 1-2. DLP Features and Design Benefits for Mobile Smart TVs and Mobile Projectors

DLP FEATURE	DESIGN BENEFIT
High optical efficiency	DMDs incorporate highly reflective and polarization agnostic aluminum micromirrors, which enable bright and power efficient display products.
Small size, high resolution	With micromirrors as small as 5.4 µm, DLP Pico chips deliver resolutions up to 1080p while enabling very compact projection designs.
High contrast	Optical modules designed with DLP Pico chips can achieve full on/off contrast ratios of over 1000:1, depending on system design. Higher contrast translates to more vivid colors and darker blacks.
Mature ecosystem	A mature global ecosystem of established optical module manufacturers eases the design process and allows product developers to go to market faster by using an existing, off-the-shelf optical engine that is already in production.

1.3 Industrial Applications

DLP Pico display chipsets can be incorporated into a variety of industrial applications.

Digital signage is a category of displays designed for commercial and industrial spaces, including retailers, stadiums, casinos, hotels, restaurants, and airports. Digital signage delivers up-to-date information such as advertising, menus, event status, and maps in locations where people gather. The low power and compact size of DLP Pico chipsets enable effective digital signage solutions that can be tucked away for free-form, on-demand displays on virtually any surface.

For more information, read *Using TI DLP® Technology to Make Digital Signage More Effective*.

Integrating DLP Pico technology into appliances can enhance their effectiveness. Adding smart displays to appliances can offer many benefits such as interactive, adaptive, and reconfigurable interfaces that can replace buttons, tablets, LCD panels, and mechanical knobs in virtually every room of the house.

To learn more, read *TI DLP® Pico™ technology for smart home applications*.

2 System Overview

This reference design features the DLP230NP DMD, the DLPC3436 display controller and the DLPA2005 PMIC and LED driver. The DLP230NP chipset requires an FPGA between the DLP display controller and the front-end processor for image processing purposes. The design is specifically target to connect to the Raspberry Pi 4B via the parallel interface. To connect externally to the FPD-Link interface of this chipset a connector needs to be installed on the DLPDLCR230NPEVM.

2.1 Block Diagram

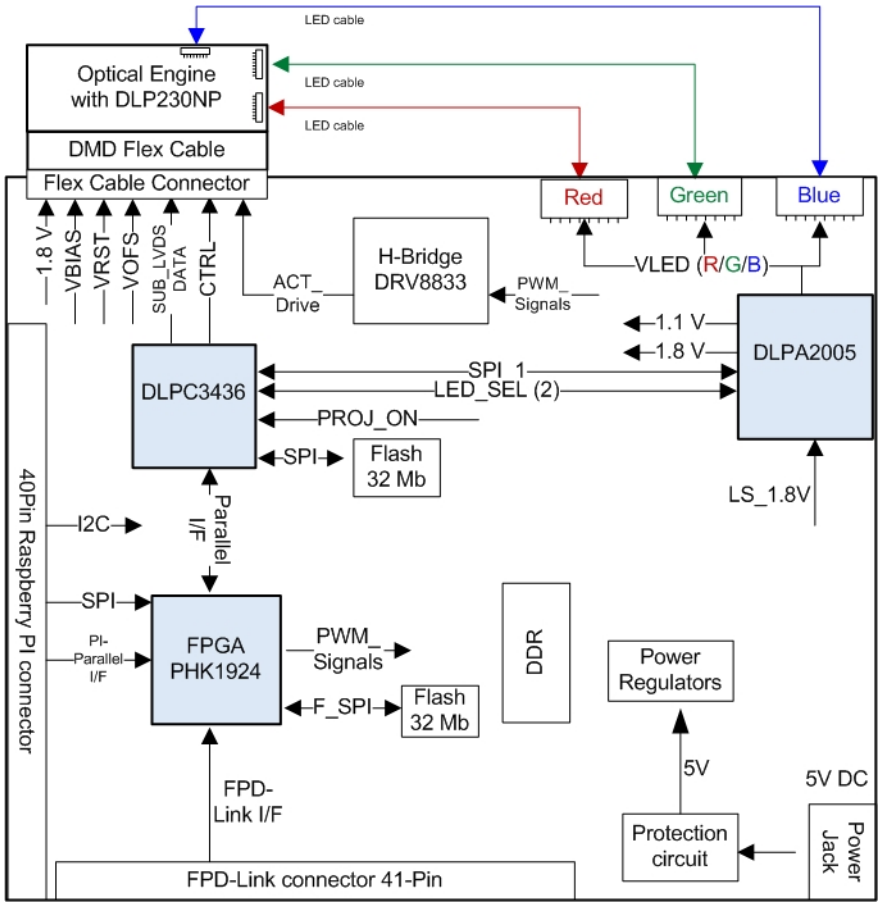

Figure 2-1. DLP LightCarfter Display 230NP EVM Block Diagram

2.2 Design Considerations

See the following documents for consideration in DLP system design:

- TI DLP® PICO™ System Overview: Optical Module Specifications
- TI DLP® System Design: Brightness Requirements and Tradeoffs

2.3 General Layout Recommendations

The layout guidelines listed in this design guide are subsets of the guidelines included in the component data sheets. For more information, refer to the DLPC3436 Display Controller, DLP230NP 0.23 1080p DMD, and DLPA2005 PMIC and LED Driver IC Data data sheets.

2.3.1 DLPC3436 Layout Guidelines

2.3.1.1 PLL Power Layout

Follow these recommended guidelines to achieve acceptable controller performance for the internal PLL. The DLPC3436 controller contains two internal PLLs which have dedicated analog supplies (VDD_PLLM, VSS_PLLM, VDD_PLLD, and VSS_PLLD). At a minimum, isolate the VDD_PLLx power and VSS_PLLx ground pins using a simple passive filter consisting of two series ferrite beads and two shunt capacitors (to widen the spectrum of noise absorption). It's recommended that one capacitor be 0.1 µF and one be 0.01 µF. Place all four components as close to the controller as possible. It's especially important to keep the leads of the high frequency capacitors as short as possible. Connect both capacitors from VDD_PLLM to VSS_PLLM and VDD_PLLD to VSS_PLLD on the controller side of the ferrite beads. Select ferrite beads with these characteristics:

- DC resistance less than 0.40 Ω
- Impedance at 10 MHz equal to or greater than 180 Ω
- Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the DLPC3436 controller to both capacitors and then through the series ferrites to the power source. Make the power and ground traces as short as possible, parallel to each other, and as close as possible to each other.

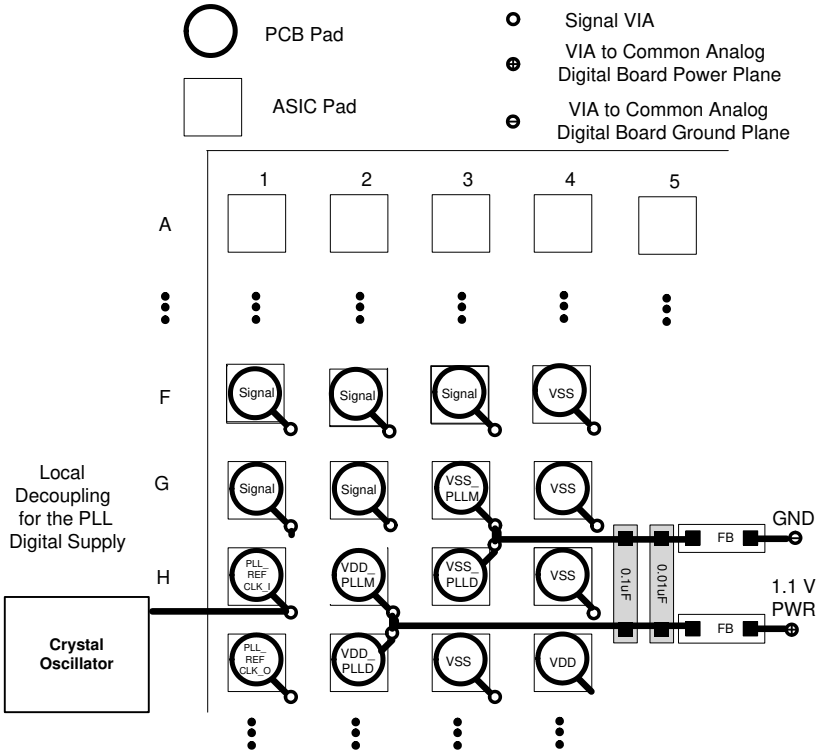

Figure 2-2. PLL Filter Layout

2.3.1.2 I2C Interface Performance

Both DLPC3436 I^2C interface ports support a 100-kHz baud rate. By definition, I^2C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

2.3.1.3 DMD Control and Sub-LVDS Signals

Table 2-1. Maximum Pin-to-Pin PCB Interconnect Recommendations

DMD BUS SIGNAL[1] [2]	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE-BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 (152.4)	See [3]	in (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 (152.4)	See [3]	in (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 (165.1)	See [3]	in (mm)
DMD_LS_WDATA	6.5 (165.1)	See [3]	in (mm)
DMD_LS_RDATA	6.5 (165.1)	See [3]	in (mm)
DMD_DEN_ARSTZ	7.0 (177.8)	See [3]	in (mm)

(1) Maximum signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to PCB variations, these recommendations cannot be defined. Any board design should SPICE simulate with the controller IBIS model (found under the *Tools & Software* tab of the controller web page) to ensure routing lengths do not violate signal requirements.

Table 2-2. High Speed PCB Signal Routing Matching Requirements

SIGNAL GROUP LENGTH MATCHING[1] [2] [3]				
INTERFACE	**SIGNAL GROUP**	**REFERENCE SIGNAL**	**MAX MISMATCH[4]**	**UNIT**
DMD[5]	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	in (mm)
	DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
	DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
	DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
	DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
	DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
	DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
	DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD	DMD_HS_WDATA_x_P	DMD_HS_WDATA_x_N	±0.025 (±0.635)	in (mm)
DMD	DMD_HS_CLK_P	DMD_HS_CLK_N	±0.025 (±0.635)	in (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	in (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	in (mm)

(1) The length matching values apply to PCB routing lengths only. Internal package routing mismatch associated with the DLPC34xx controller or the DMD require no additional consideration.

(2) Training is applied to DMD HS data lines. This is why the defined matching requirements are slightly relaxed compared to the LS data lines.

(3) DMD LS signals are single ended.

(4) Mismatch variance for a signal group is always with respect to the reference signal.

(5) DMD HS data lines are differential, thus these specifications are pair-to-pair.

Table 2-3. Signal Requirements

PARAMETER	REFERENCE	REQUIREMENT
Source series termination	DMD_LS_WDATA	Required
	DMD_LS_CLK	Required
	DMD_DEN_ARSTZ	Acceptable
	DMD_LS_RDATA	Required
	DMD_HS_WDATA_x_y	Not acceptable
	DMD_HS_CLK_y	Not acceptable
Endpoint termination	DMD_LS_WDATA	Not acceptable
	DMD_LS_CLK	Not acceptable
	DMD_DEN_ARSTZ	Not acceptable
	DMD_LS_RDATA	Not acceptable
	DMD_HS_WDATA_x_y	Not acceptable
	DMD_HS_CLK_y	Not acceptable
PCB impedance	DMD_LS_WDATA	68 Ω ±10%
	DMD_LS_CLK	68 Ω ±10%
	DMD_DEN_ARSTZ	68 Ω ±10%
	DMD_LS_RDATA	68 Ω ±10%
	DMD_HS_WDATA_x_y	100 Ω ±10%
	DMD_HS_CLK_y	100 Ω ±10%
Signal type	DMD_LS_WDATA	SDR (single data rate) referenced to DMD_LS_DCLK
	DMD_LS_CLK	SDR referenced to DMD_LS_DCLK
	DMD_DEN_ARSTZ	SDR
	DMD_LS_RDATA	SDR referenced to DMD_LS_DLCK
	DMD_HS_WDATA_x_y	sub-LVDS
	DMD_HS_CLK_y	sub-LVDS

2.3.1.4 Layout Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers. Ideally, ensure that the signals of a given pair do not change layers.

2.3.1.5 Stubs

- Avoid using stubs.

2.3.1.6 Terminations

- DMD_HS differential signals require no external termination resistors.
- Make sure the DMD_LS_CLK and DMD_LS_WDATA signal paths include a 43-Ω series termination resistor located as close as possible to the corresponding controller pins.
- Make sure the DMD_LS_RDATA signal path includes a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- The DMD_DEN_ARSTZ pin requires no series resistor.

2.3.1.7 Routing Vias

- The number of vias on DMD_HS signals must be minimized.
- Any and all vias on DMD_HS signals must be located as close to the controller as possible.
- The number of vias on the DMD_LS_CLK and DMD_LS_WDATA signals must be minimized and ideally not exceed two.
- Any and all vias on the DMD_LS_CLK and DMD_LS_WDATA signals must be located as close to the controller as possible.

2.3.2 FPGA DDR3L SDRAM Interface Routing

The FPGA to DDR3L SDRAM interface is based on a 533-MHz DDR clock rate. The Xilinx Zynq FPGA (XC7Z020-1CLG484I4493) to a Micron low power DDR3 SDRAM (MT41K64M16TW-107 IT) interface diagram is shown in Figure 2-3 and the recommended interface layout guidelines are defined in Table 2-4.

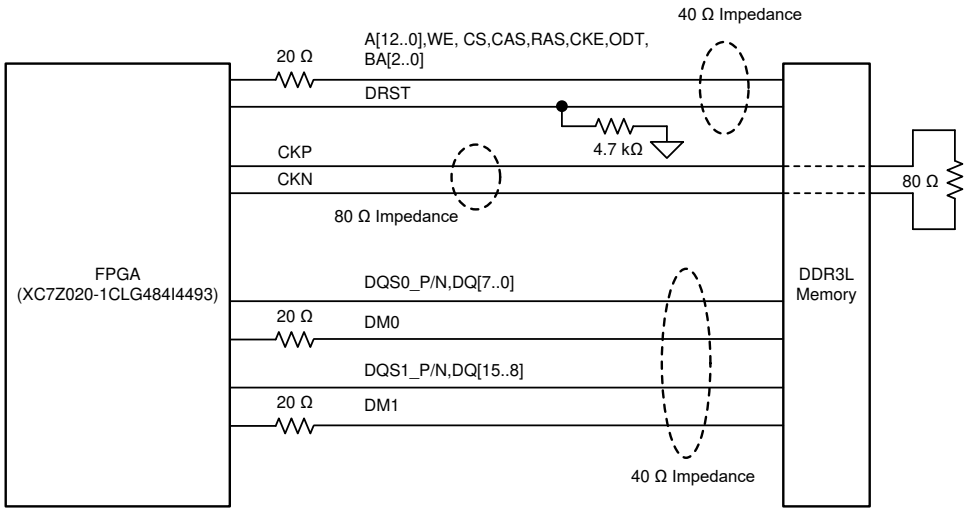

Figure 2-3. FPGA-DDR3L Interface

Table 2-4. Recommended FPGA-DDR3L PCB Trace Delays

NET NAME	MINIMUM TRACE DELAY (ps)	MAXIMUM TRACE DELAY (ps)	TRACE IMPEDANCE (Ω)
DDR_A(12:0)	175	225	40
DDR_BA(2:0)	175	225	40
DDR_CAS_B	175	225	40
DDR_CKE	150	175	40
DDR_CS_B	175	225	40
DDR_DRST_B	175	225	40
DDR_ODT	175	225	40
DDR_RAS_B	175	225	40
DDR_WE_B	150	175	40
DDR_CK(P,N)	208	212	80 Differential
DDR_DQS_P0, DDR_DQS_N0	180	190	40
DDR_DM0	180	200	40
DDR_DQ(7:0)	180	200	40
DDR_DQS_P1, DDR_DQS_N1	180	190	40
DDR_DM1	180	200	40
DDR_DQ(15:8)	180	200	40

PCB routing best practices:

- Use inner PCB layers when possible.
- Route DDR_DQ(7:0), DDR_DM0 and DDR_DQS_(P,N)0 on the same layer(s).
- Route DDR_DQ(15:8), DDR_DM1 and DDR_DQS_(P,N)1 on the same layer(s).
- DDR_DQS_P0/N0 should have equal delays.
- DDR_DQS_P1/N1 should have equal delays.

2.3.3 DLPA2005 Layout Recommendations

2.3.3.1 Layout Guidelines

As for all chips with switching power supplies, the layout is an important step in the design, especially in the case of high peak currents and high switching frequencies. If the layout is not carefully done, the regulators could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths and for the power ground tracks. Input capacitors, output capacitors, and inductors should be placed as close as possible to the IC.

Figure 2-4 shows an example layout that has critical parts placed as close as possible to the pins they are connected to. Following are recommendations for the components:

R1 is RLIM and is connected through a wide trace (low resistance) to the system ground. The analog ground at pin 5 should be star connected to the point where RLIM is connected to the system ground. Aim on a wide and low-ohmic trace as well, although this one is less critical (tens of mA).

L1 is the big inductor for the VLED that is connected through two wide traces to the pins

C4 are the decoupling capacitors for the VLED and they are as close as possible placed to the part and directly connected to ground.

L3/C20 are components used for the VCORE BUCK. L3 is placed close to the pin and connected with a wide trace to the part. C20 is placed directly beside the inductor and connected to the PGND pin

L2 This inductor is part of the DMD reset regulators and is also placed as close as possible to the DLPA2005 using wide PCB traces.

2.3.3.2 Layout Example

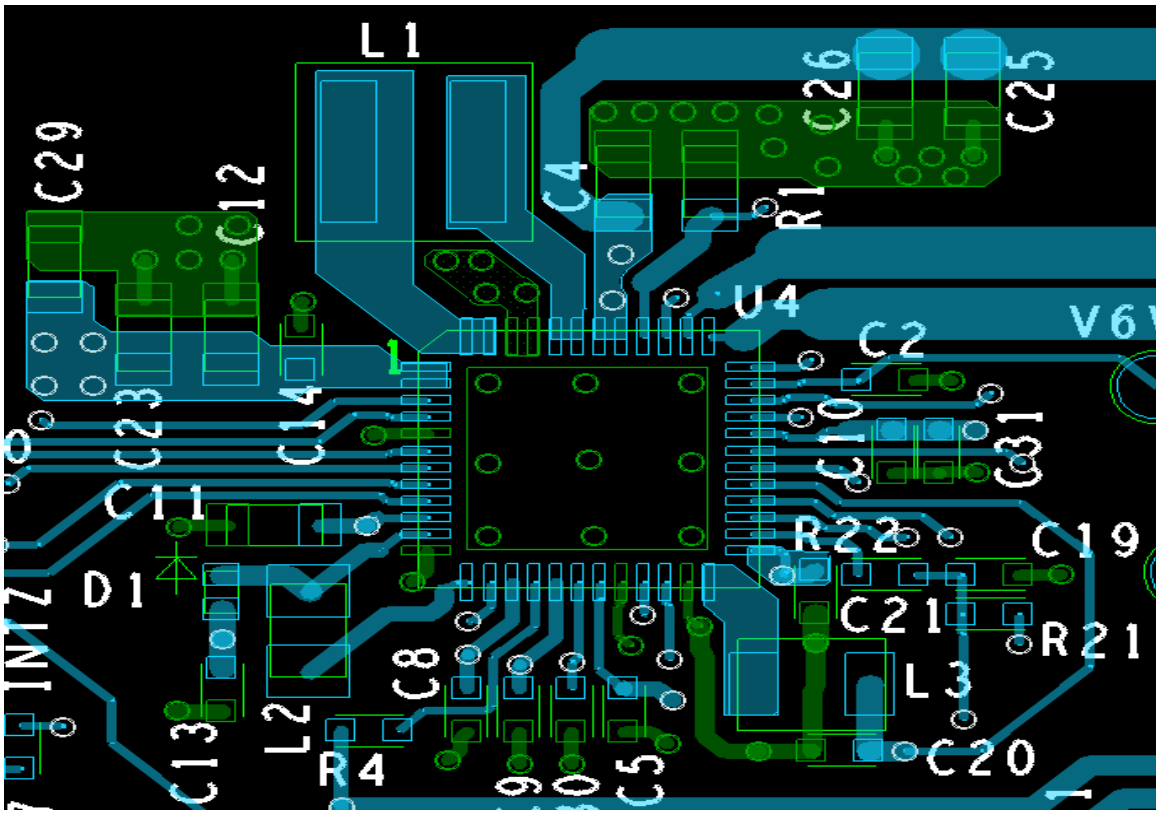

Figure 2-4. Example Layout of DLPA2005

2.3.3.3 Thermal Considerations

An important consequence of the efficiency numbers shown in Figure 2-5 is that it enables to perform DLPA2005 thermal calculations. Since the efficiency is not 100%, power is dissipated in the DLPA2005 chip. Due to that dissipation, die temperature will rise. For reliability reasons, it is good to aim for as low as possible die temperatures. Using a heat sink and airflow are efficient means to keep die temperature reasonably low. In cases that airflow and or a heat sink are or is not feasible, the system designer should specifically pay attention to the thermal design. The die temperature for regular operation should remain below 120°C.

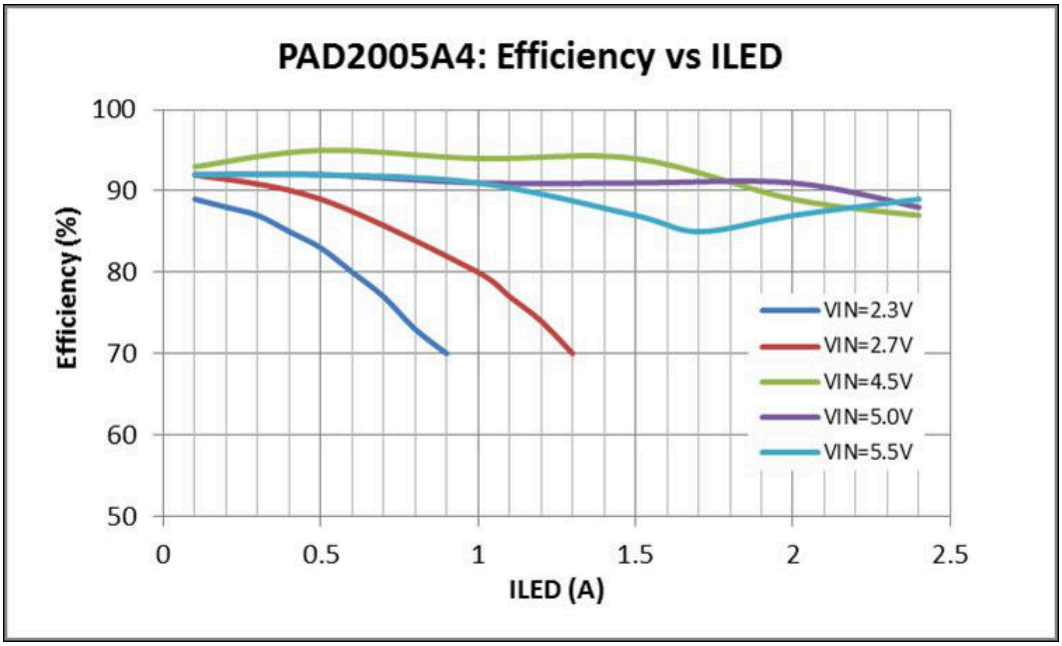

Figure 2-5. Measured Typical Power Converter Efficiency as a Function of ILED for Several Supply Voltages (V_{OUTmax} = 4.8 V for Each Supply)

In the following, an example is given of such a thermal calculation. The calculation starts with summarizing all blocks in the DLPA2005 that dissipate. The buck-boost converter supplying the LED power is the main source of dissipation. For illustrating purposes, we assume this buck-boost converter to be the only block that dissipates significantly. For the example assume: VOUT=4.8 V (for all three LEDs), IOUT=2.4 A and VIN=5 V. From Figure 2-5 it can be derived that the related efficiency equals about n_{eff}=88%.

The power dissipated by the DLPA2005 is then given by:

$$P_{DISS} = P_{IN} - P_{OUT} = P_{OUT}\left(\frac{100\%}{\eta_{eff}} - 1\right) = 4.8V \cdot 2.4A \cdot \left(\frac{100\%}{88\%} - 1\right) = 1.6W \quad (1)$$

The rise of die temperature due to this power dissipation can be calculated using the thermal resistance from junction to ambient, □JA=27.9°C/W. This calculation yields:

$$T_{JUNCTION} = T_{AMBIENT} + P_{DISS} \cdot \theta_{JA} = 25°C + 1.6W \cdot 27.9°C/W = 69.6°C \quad (2)$$

It is also possible to calculate the maximum allowable ambient temperature to prevent surpassing the maximum die temperature. Assume again the dissipation of PDISS=1.6W. The maximum ambient temperature that is allowed is then given by:

$$T_{AMBIENT-\max} = T_{JUNCTION-\max} - P_{DISS} \cdot \theta_{JA} = 120°C - 1.6W \cdot 27.9°C/W = 75.4°C \quad (3)$$

It is again stressed that for proper calculations, the total power dissipation of the DLPA2005 should be taken into account. Also, if components that are close to the DLPA2005 also dissipate a significant amount of power, the (local) ambient temperature can be higher than the ambient temperature of the system.

If calculations show that the die temperature will surpass the maximum specified value, two basic options exist:

- Adding a heat sink with or without airflow. This will reduce 0_{JA} yielding lower die temperature.
- Lowering the dissipation in the DLPA2005 implying lowering the maximum allowable LED current.

2.3.4 DMD Flex Cable Interface Layout Guidelines

The DLP230NP DMD is connected to a PCB or a flex circuit using an interposer. For additional layout guidelines regarding length matching, impedance, and so on, see the *DLPC3436 Display Controller data sheet*.

Some layout guidelines for routing to the DLP230NP DMD include:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer to Figure 2-6.
- Minimum of two 100-nF (25 V) capacitors - one close to V_{BIAS} pin. Capacitors C4 and C8 in Figure 2-6.
- Minimum of two 100-nF (25 V) capacitors - one close to each V_{RST} pin. Capacitors C3 and C7 in Figure 2-6.
- Minimum of two 220-nF (25 V) capacitors - one close to each V_{OFS} pin. Capacitors C5 and C6 in Figure 2-6.
- Minimum of four 100-nF (6.3 V) capacitors - two close to each side of the DMD. Capacitors C1, C2, C9 and C10 in Figure 2-6.

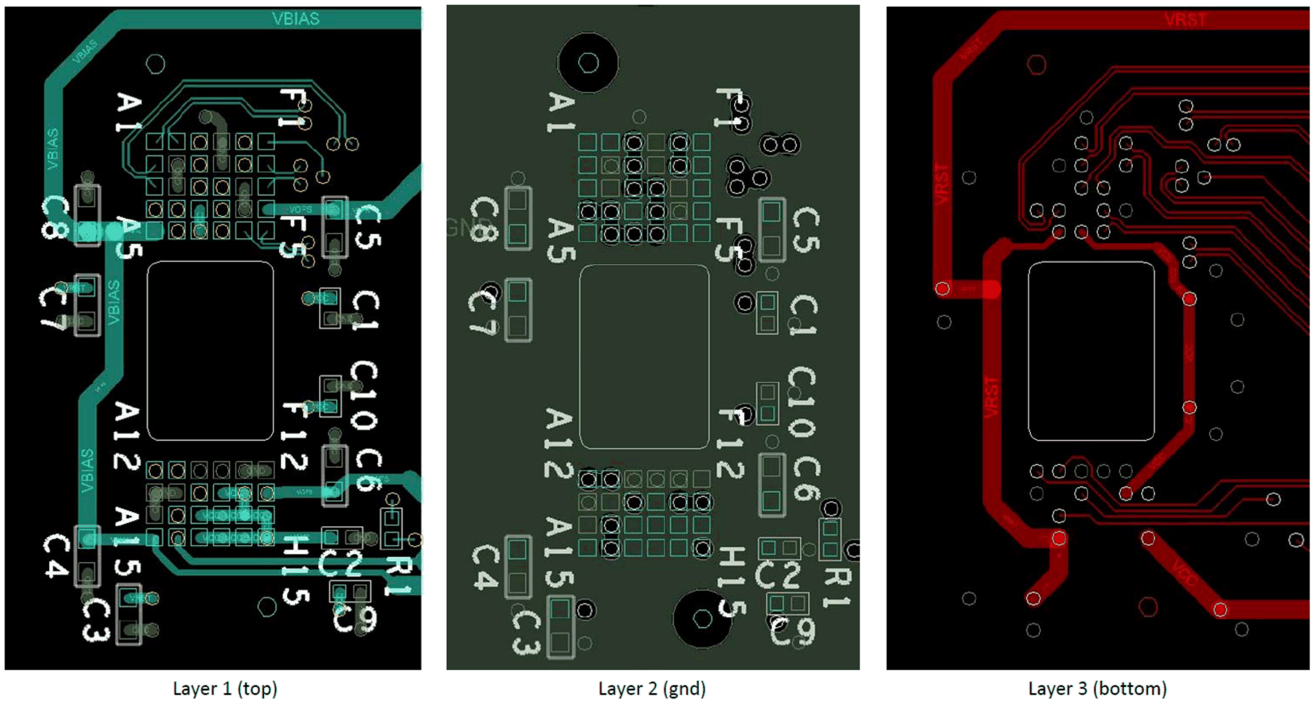

Figure 2-6. Power Supply Connections

2.4 Highlighted Products

This chipset reference design guide draws upon figures and content from several other published documents related to the 0.23 inch 1080p DLP chipset. For a list of these documents, see Section 4.3

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

This section assumes the default DLPDLCR230NPEVM design:

1. If a Raspberry Pi is available, proceed with connecting the DLPDLCR230NPEVM to the Raspberry Pi. Ensure that the Raspberry Pi has been setup as described in the DLPDLCR230NPEVM User's Guide. If the Raspberry Pi is currently not needed, proceed with step 2.

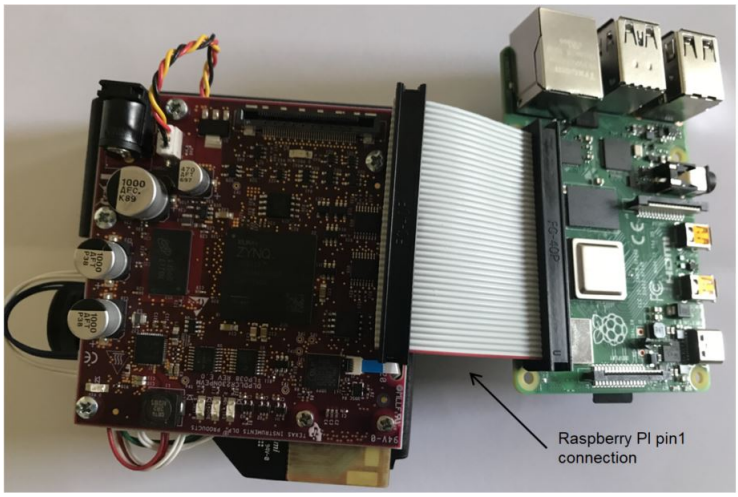

Figure 3-1. DLPDLCR230NPEVM With Raspberry PI

2. Power up the DLP LightCrafter Display 230NP EVM by applying an external DC power supply (5 V DC) to the JPWR1 connector. The D_P5V LED will indicate that the 5-V DC power supply has been applied to the system.
   External Power Supply Requirements:
   - Nominal Output Voltage: 5 VDC
   - Minimum Output Current: 3 A; Maximum Output Current: 4 A
   - Efficiency Level: VI

   NOTE: TI recommends using an external power supply that complies with applicable regional safety standards such as UL, CSA, VDE, CCC, PSE, and so forth.
3. The system will automatically drive Proj-ON high when the 5-V DC power supply is applied and the fan is plugged in. If the fan is not plugged in or a loose connection is present Proj-ON will not be driven high. The DLPDLCR230NPEVM includes a input voltage monitor which drives Proj-ON low if the input voltage drops below approximately 4.65 V for any reason during operation.
4. After the DLP LightCrafter Display 230NP EVM is turned on; the projector will default to displaying a DLP logo followed by a LightCrafter Display test pattern image. The D_HOST_IRQ will be OFF which indicates a successful boot of the DLPC3436. The D_DONE and D_INIT_B will be ON to indicate a successful boot-up of the FPGA.

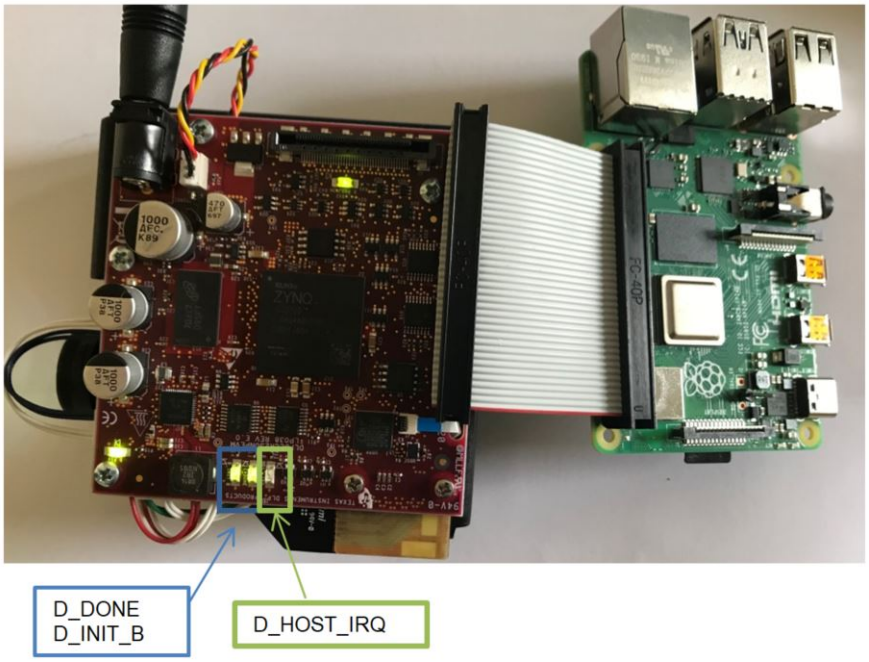

Figure 3-2. DLPDLCR230NPEVM LED Indications

5. The focus of the image can be adjusted manually on the optical engine.

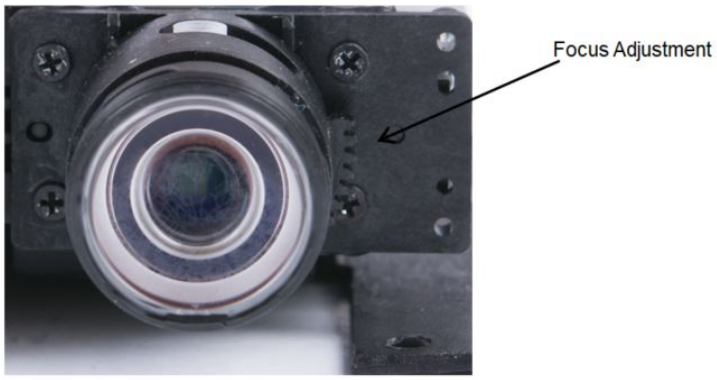

Figure 3-3. Optical Engine With Focus Adjustment

6. Ensure that the Raspberry Pi has been configured correctly as described in theDLPDLCR230NPEVM User's Guide before applying power to the Raspberry Pi via the USB Type C cable.
7. Power down with the Raspberry Pi connected:
   - Drive PROJ_ON LOW via Raspberry Pi GPIO 25 (refer to DLPDLCR230NPEVM User's Guide)
   - Shutdown the Raspberry Pi (refer to DLPDLCR230NPEVM User's Guide)
   - Remove power from the Raspberry Pi by removing the USB Type C cable
   - Remove the power adapter to the DLPDLCR230NPEVM
8. Power down without Raspberry Pi connected: The projector can be turned off by just removing the power cable. A voltage monitor on the EVM will detect the input voltage drop below 4.65 V and will drive Proj-ON low automatically.

There are five indicator LEDs on the DLP LightCrafter Display 230NP EVM, and they are defined in Table 3-1:

Table 3-1. LEDs on the DLP® LightCrafter™ Display 230NP EVM

LED REFERENCE	SIGNAL INDICATION	DECSCRIPTION
D_HOST_IRQ	HOST_IRQ	ON during DLPC3436 boot, OFF when projector is running. Indication of DLPC3436 boot-up completed and ready to receive commands
D_PROJ_ON	PROJ_ON	PROJ_ON signal is HIGH
D_INIT_B	INT_B	ON when FPGA initialization is completed. OFF indicates that the FPGA is in RESET or a configuration error occured.
D_DONE	DONE	ON when FPGA configuration is completed.
D_P5V	P5V	Input voltage 5 V applied

The connectors on the DLP LightCrafter Display 230NP EVM are defined in Table 3-2:

Table 3-2. Installed Connectors on Formatter Board

INSTALLED CONNECTORS AND HEADERS	DESCRIPTION
JPWR1	Connector for 5-V external power supply interface
J1	Connector for optical engine flex cable.
J2	Connector (40 pin) for Raspberry Pi cable
J3	Connector (41 pin) for FPD Link interface (not installed by default)
J4	Connector for 5-V cooling fan
J500	Connector for DMD interface flex cable
J501	Connector for Green LED cable
J502	Connector for Red LED cable
J503	Connector for Blue LED cable

3.2 Test Setup

The DLP LightCrafter Display 230NP EVM is composed of two main parts:

- DLPDLCR230NPEVM formatter board
- Engine with LED connection, flex cable, and mechanical setup

The formatter board contains the connector for the power supply, the connector for the fan, and the Raspberry Pi ribbon cable connector. It also contains a protection circuit which prevents the power up of the DLP chipset when no fan is connected to the board. This also applies if the connection is loose or in case a fan wire is broken. Figure 3-4 shows the DLPDLCR230NPEVM formatter board with the main connections:

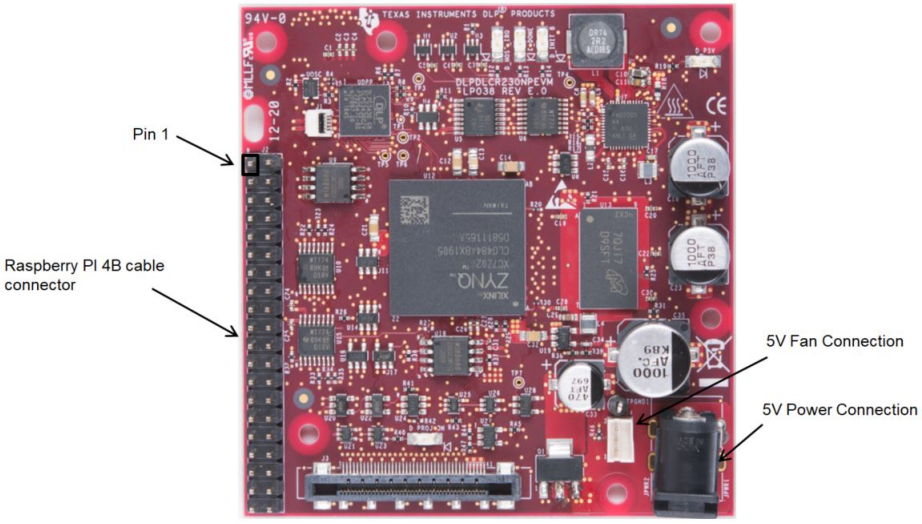

Figure 3-4. DLP® LightCrafter™ 230NP EVM Formatter Board

The light engine contains the LED connectors and the flex cable which connects to the formatter board on the bottom via J500. Figure 3-5 shows the optical engine connections.

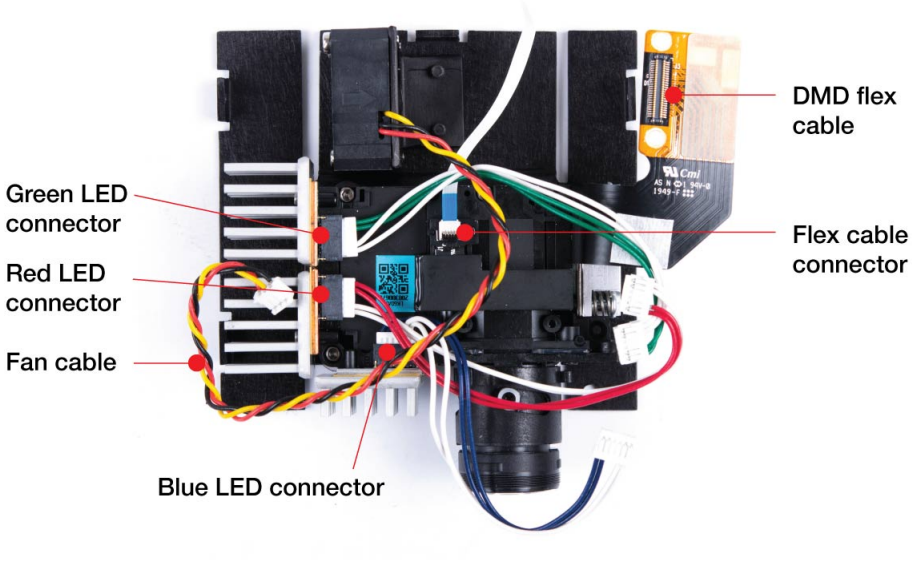

Figure 3-5. DLPDLCR230NPEVM Optical Engine Connection

The DLPDLCR230NPEVM formatter board is mounted on top of the mechanical base. The fan cable has to be connected all the way to ensure proper connection of the fan wires to the PCB. Figure 3-6 shows the formatter board mounted on the mechanical assembly with all cables connected.

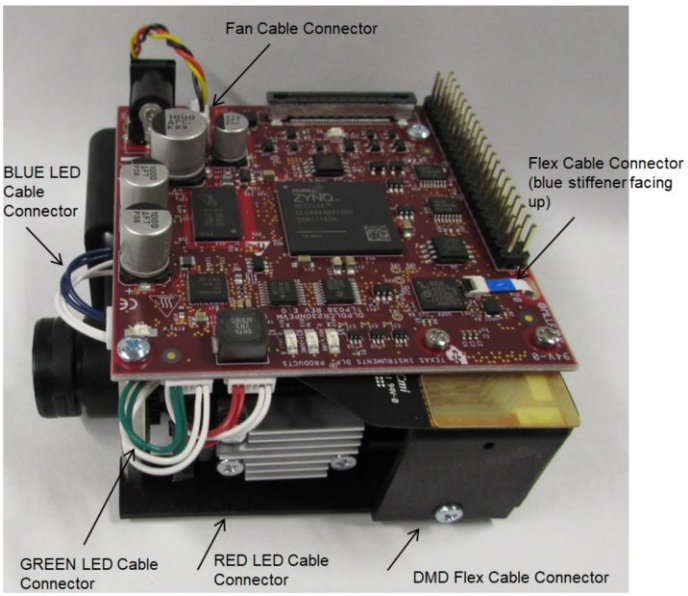

Figure 3-6. DLP® LightCrafter™ Display 230NPEVM

Ensure a good connection of the flex cable, fan, and LED cables to the DLP LightCrafter Display 230NPEVM formatter board before turning it on.

3.3 Test Results

The successful test result of this system is the appearance of a splash screen followed by a color bar test pattern on the display. The splash screen is shown in Figure 3-7

Figure 3-7. DLPDLCR230NPEVM Splash Image

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-080009.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-080009.

4.1.3 Layout Files

To download the bill of materials (BOM), see the design files at TIDA-080009.

4.1.4 Mechanical Files

To download the bill of materials (BOM), see the design files at TIDA-080009.

4.2 Software

DLPC3436 firmware and FPGA binary code DLPDLCR230NPEVM Firmware

DLPDLCR230NPEVM Raspberry PI Python support package DLPDLCR230NPEVM Raspberry PI Software

4.3 Documentation Support

1. Texas Instruments, *DLP® LightCrafter™ Display 230NP EVM User's Guide*
2. Texas Instruments, *DLPC3436 Display Controller Data Sheet*
3. Texas Instruments, *DLP230NP 0.23 1080p DMD Data Sheet*
4. Texas Instruments, *DLPA2005 PMIC and LED Driver IC Data Sheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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