Design Guide: TIDA-010979

48V 1kW Robot Joint Motor Control With Industrial Communication Reference Design

Description

This reference design features TI Sitara™ MCU-AM261x devices handling an industrial Ethernet-connected motor drive. The design uses a 70mm diameter printed circuit board (PCB) to drive a humanoid robot joint (48V, 1kW Eyoubot motor). The design demonstrates a small form factor and simplified integrated platform. The platform includes a high-power density section using three DRV7167 half-bridge GaN motor driver power stages, an accurate real-time control stage with an AM2612 500MHz R5F core MCU and AMC0106 functionally isolated delta-sigma modulator, plus high-bandwidth communication through industrial Ethernet.

Resources

TIDA-010979	Design Folder
AM2612, DRV7167	Product Folder
AMC0106, DP83826A	Product Folder
AM261x Motor Control SDK	Tool Folder

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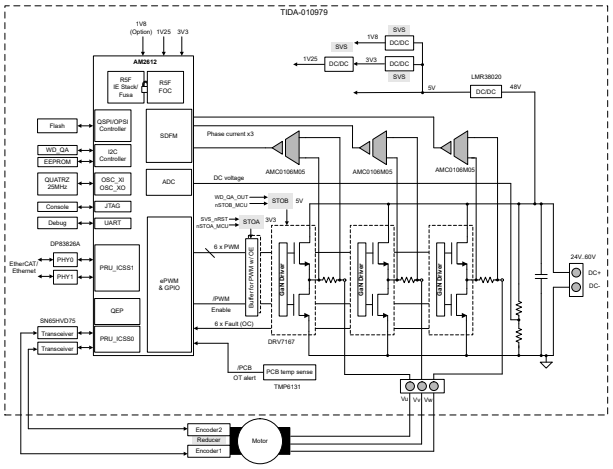
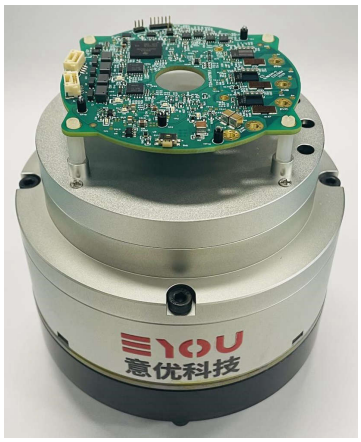
Features

- Compact design with highly integrated ICs facilitating a 70mm diameter PCB and a 15mm diameter through hole
- Supports multiprotocol industrial Ethernet communication and multiprotocol encoder interface
- Small form factor DRV7167 half-bridge GaN motor driver power stage
- Precision phase current sense using 1mΩ shunt and the AMC0106M05 functional isolated modulator

Applications

- Humanoid robot motor drive
- Collaborative robot servo drive
- Mobile robot motor control
- Robot communication module
- Servo drive power stage module





1 System Description

This reference design demonstrates the capacity of TI Sitara™ MCU-AM261x devices to handle an industrial Ethernet-connected real-time servo motor control with a 70mm diameter printed circuit board (PCB) for a 48V, 1kW robot joint.

The control part of this design includes one 500MHz R5F core on an AM261x MCU with a small 10mm × 10mm BGA package to perform closed loop field-oriented control (FOC) and another 500MHz R5F core of this AM261x MCU to run EtherCAT stack. Also, two Programmable Real-Time Unit - Industrial Communication Subsystems (PRU-ICSS) are used on this AM261x MCU to support multi-protocol encoder and industrial Ethernet MAC layer. This reference design employs two BissC digital encoders to feedback the position information of the rotor and reducer. Other encoder protocols like EnDAT, HDSL, BissC and Tamagawa can also be supported by PRU-ICSS.

The power part includes three 100V, 70A half-bridge GaN motor driver power stage DRV7167A devices with integrated driver and overcurrent protection, optimized for extremely low gate loop and power loop impedance. The PCB offers mounting holes for an optional heat sink with the top-side cooled DRV7167A GaN motor driver power stage. An integrated bootstrap diode helps further reduce space for the high-side GaN-FET bias supply.

For precision phase-current sensing, this reference design uses three functional isolated delta-sigma modulator AMC0106M05 devices plus three 1mΩ phase-current shunts to measure the 3-phase current with a linear measurement range of ±50A. A digital interface connects the AMC0106M05 to the MCU to run the $SINC^3$ decimation filter.

This reference design also showcases the unique functional safety concept with AM2612 MCU and safe power approach. This safety concept is targeted to build a safety certified CAT3, PLd or PLe architecture to achieve logical redundancy with one MCU.

1.1 Terminology

SOC	System On-Chip
FOC	Field-Oriented Control
MCU	Microcontroller Unit
RPM	Revolutions Per Minute
EnDAT/HDSL/BissC/Tamagawa	Multi-digital, bidirectional interface protocols for absolute encoders
EtherCAT	Ethernet for Control Automation Technology
Profinet	Portmanteau for Process Field Network
ICSS	Industrial Communication Subsystem
PRU	Programmable Real-time Unit
SDFM	Sigma-Delta Filter Module
SDM	Sigma-Delta Modulator
EPWM	Enhanced Pulse-Width Modulation
CMP	Event Comparator
CAP	Event Capture
ISR	Interrupt Service Routine
EPWM	Enhanced Pulse-Width Modulation
TCM	Tightly Coupled Memory
GPIO	General-Purpose Input Output
FIFO	First In, First Out
SPI	Serial Peripheral Interface
PHP	Hypertext Preprocessor
PDO	PHP data objects

1.2 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	TYPICAL VALUE	COMMENT
DC input voltage	48V (12V to 60V)	80V absolute maximum
Maximum three-phase continues output current	$17A_{RMS}$	Test condition: No heat sink at 25°C ambient temperature
Maximum output power	1kW at 48VDC	At power factor 0.98
Power FET type	GaN technology	Half-bridge power module with integrated high and low side gate drivers (DRV7167A)
PWM switching frequency	20kHz to 100kHz	Higher than 80kHz PWM frequencies supported
PWM dead band	40ns	Configurable
Functional isolated modulator	1mΩ shunt | AMC0106M05	Precision, ±50mV input, functional isolated, Delta-Sigma modulator with external clock
Delta-sigma digital filter	OSR64 or OSR32	Configurable according to PWM frequency
Phase current maximum range	±50A	3.3V digital interface (clock and data) to MCU
PCB layer stack	6-layer, 1oz copper	
PCB size	70mm diameters round with 15mm diameters through hole	
Encoder1	BissC, 20-bit resolution, single turn	Used for speed loop
Encoder2	BissC, 19-bit resolution, single turn	Used for position loop

Table 1-2 lists the TIDA-010979 interface and connectors specifications.

Table 1-2. Interface and Connectors Specification

PIN	SIGNAL	FUNCTION
J1-1	GND	JTAG
J1-2	JTAG_TMS	
J1-3	JTAG_TDI	
J1-4	JTAG_TCK	
J1-5	JTAG_TDO	
J1-6	3V3	
J2-1	GND	UART
J2-2	UART_TXD	
J2-3	UART_RXD	
J3	Jumper ON (QSPI) Jumper OFF (UART)	BOOT MODE
J4-1	H0_TD_N	PHY0 MDI
J4-2	H0_TD_P	
J4-3	H0_RD_N	
J4-4	H0_RD_P	
J5-1	H1_TD_N	PHY1 MDI
J5-2	H1_TD_P	
J5-3	H1_RD_N	
J5-4	H1_RD_P	
J6-1	GND	Encoder 1 RS485 interface
J6-2	ENC1_CLK_P	
J6-3	ENC1_CLK_N	
J6-4	ENC1_DATA_P	
J6-5	ENC1_DATA_N	
J6-6	ENC_5V0	
J7-1	GND	Encoder 2 RS485 interface
J7-2	ENC2_CLK_P	
J7-3	ENC2_CLK_N	
J7-4	ENC2_DATA_P	
J7-5	ENC2_DATA_N	
J7-6	ENC_5V0	

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the TIDA-010979 system block diagram indicated in the dotted box.

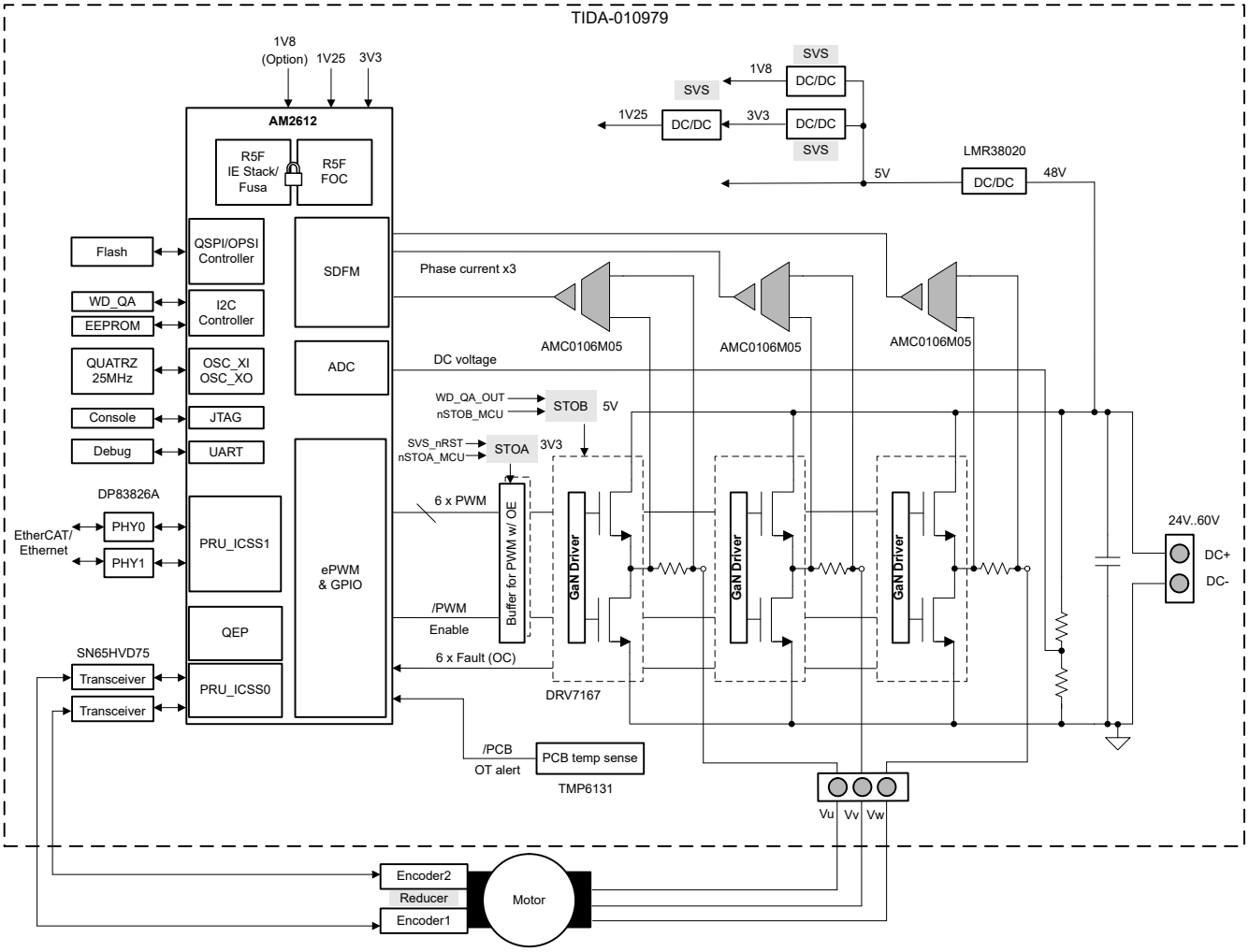


Figure 2-1. TIDA-010979 System Block Diagram

2.2 Design Considerations

The design goal is to implement an integrated single axis servo control for humanoid robot joint. This design can operate from a single DC input voltage from 12V to 60V DC, nominal 48V and output three-phase sinusoidal wave to drive an AC motor. The design contains several subsystems including:

- Power tree – A wide input voltage range DC/DC converter (LMR38020) generates the 5V rail to supply the GaN motor driver power stage, encoders power, and downstream 3.3V and 1.8V rails. The 1V25 core voltage rail for AM2612 is sourced from 3.3V through DC/DC module (TPSM82823). A 3.3V power module also supplies the current-sense modulators, PWM buffers, EEPROM, Ethernet PHYs, MCU IOs and other analog parts.
- Power inverter – each of the three inverter half-bridges employ an integrated 100V, 70A half-bridge GaN motor driver power stage (DRV7167A) with short-circuit and overtemperature protection.
- Current sense – The inverter phase employs 1mΩ phase-current shunt resistor plus a functional isolated modulator (AMC0106M05) with a ±50A linear measurement range and a digital interface to the MCU for precision current sensing.
- Control and communication – The motor control and communication employs 500MHz dual-core Arm® Cortex®-R5F-based MCU (AM2612) with real-time control, safety, and security. This subsystem includes

one 500MHz R5F core to perform closed loop field-oriented control (FOC) and another 500MHz R5F core to run industrial EtherNet stack. Also, two PRU-ICSS cores support the multi-protocol encoder and the industrial Ethernet MAC layer. This reference design employs two BissC digital encoders to feedback the position information of the rotor and reducer. Other encoder protocols like EnDAT®, HDSL, BissC, and Tamagawa® can also be supported by PRU-ICSS. As for the Ethernet protocols, AM2612 can support EtherCAT®, EtherNet/IP, Profinet® and standard Ethernet also. Two 10/100Mbps Ethernet PHYs (DP83826A) with EtherCAT, IEEE and EMC compliant are employed to provide the system timing with low and deterministic latency for EtherCAT applications.

2.3 Highlighted Products

2.3.1 AM2612

The AM261x Sitara Arm Microcontrollers are part of the Sitara AM26x real-time MCU families designed to meet the complex real-time processing needs of next-generation industrial and automotive embedded products. With scalable Arm Cortex-R5F performance and an extensive set of peripherals, the AM261x device is designed for a broad range of applications while offering safety features and optimized peripherals for real-time control. Figure 2-2 shows the functional block diagram. Table 2-1 summarizes the key features and benefits.

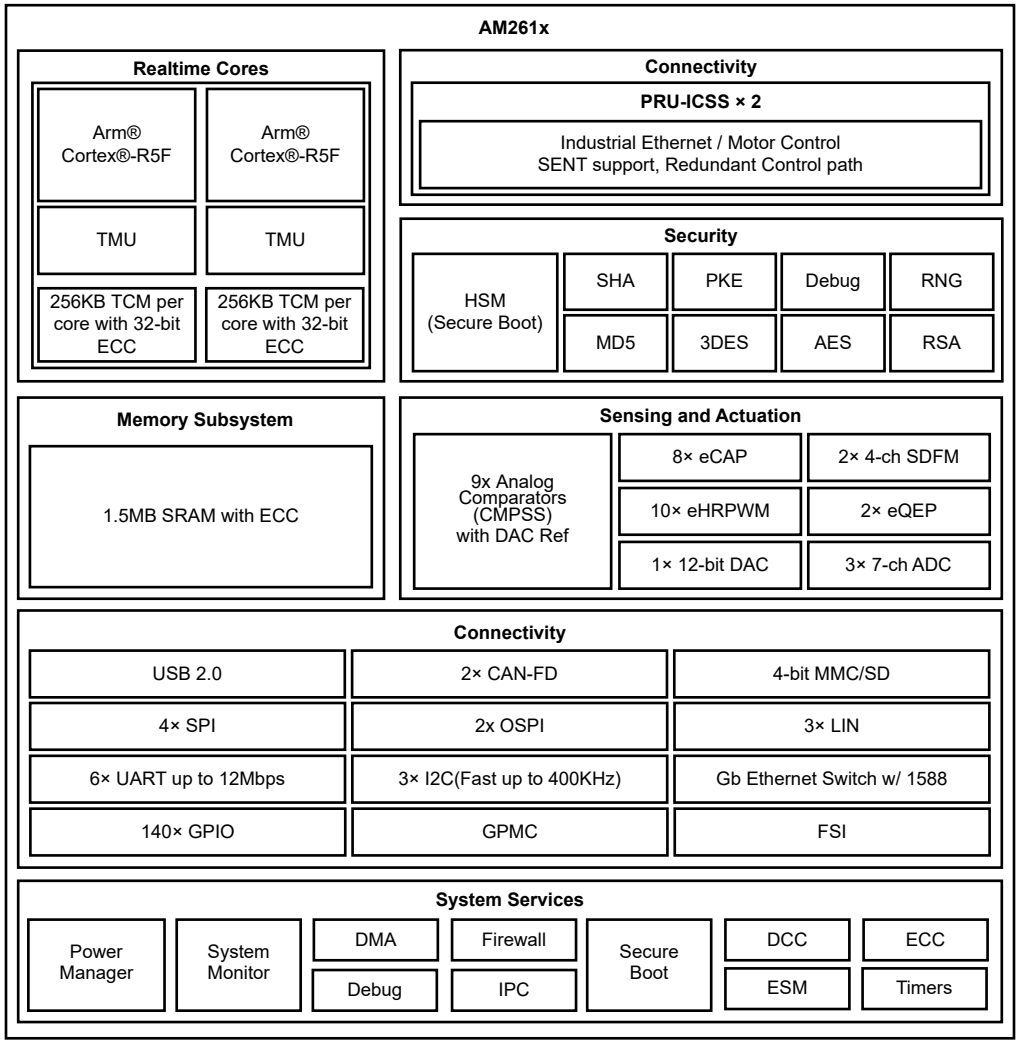


Figure 2-2. AM261x Functional Block Diagram

Table 2-1. AM261x Features and Benefits

FEATURES	BENEFITS
Dual Cortex-R5F cores with 2K DMIPS and 512KB TCM	Provide high CPU performance to meet complex real-time processing needs
Trigonometric Math Unit (TMU) on each R5F	Accelerate trigonometric function for motor control
21-channel 12-bit ADC, 10 × PWM (20-channel), 18 × analog comparators, 8 × eCAP, 8-channel SDFM	Multiple peripherals for low latency control loop
2 × PRU-ICSS, USB, Integrated Ethernet Switch (CPSW) with up to 2 × Gigabit ports to support cut-through and TSN	Rich communication and connectivity options. PRU-ICSS enables motor control feedback protocols such as EnDat2.2, Tamagawa, BiSS and so forth. Also enables industrial Ethernet protocols such as EtherCAT, Ethernet/IP, Profinet, IO-link, and so forth.
Lock-step optional, hardware security module (HSM)	SIL3 certified for functional safety. Enables secure system design with cryptographic acceleration, secure boot and granular firewalls managed by the HSM.

2.3.2 DRV7167A

The DRV7167A is a 100V half-bridge GaN motor driver power stage with integrated gate-driver and enhancement-mode Gallium Nitride (GaN) FETs. The device consists of two GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration, as shown in Figure 2-3. The device supports turn-on and turn-off slew-rate control for both FETs, single PWM mode for use with IO-limited controllers, short-circuit protection (SCP), Overtemperature Detection (OTD), and zero-voltage detection (ZVD) reporting to minimize third quadrant conduction time. Table 2-2 summarizes the key features.

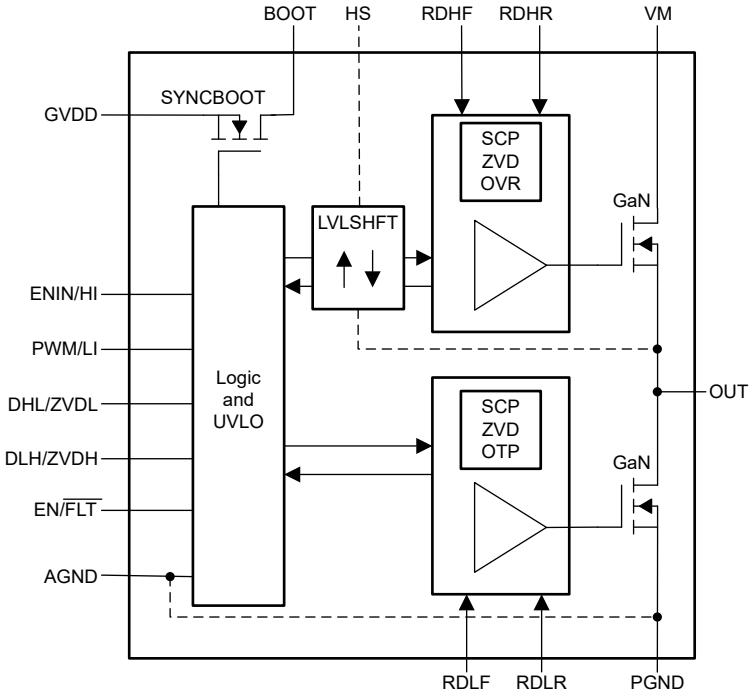


Figure 2-3. DRV7167A Functional Block Diagram

Table 2-2. DRV7167A Features and Benefits

FEATURES	BENEFIT
Integrated high-side and low-side GaN driver and 100V GaN FETs, 2.2mΩ devices for 70A DC operation.	Enables up to 60VDC, three-phase inverter with $16A_{RMS}$ phase current at 80kHz high-switching frequency for low inductance and high-speed drives.
Completely bond-wire-free package and optimized pinout.	Minimized package parasitic elements enable ultra-fast switching for reduced switching losses to reduce or eliminate heat sink. Easy PCB layout.
GaN FETs have zero reverse recovery (3^{rd} quadrant operation) and very small input capacitance C_{ISS}.	Reduces or eliminates ringing in hard switching, like in inverters reduces EMI. Very low overshoot and undershoot allows higher nominal DC-link voltage than Si-FET for the same maximum rated voltage.
Excellent propagation delay matching (2ns FETs).	Enables ultra-low dead band per half-bridge for major reduction of switching losses in three-phase inverter applications and elimination of dead-time distortions in the phase voltage.
Independent high-side and low-side transistor-transistor logic (TTL) inputs.	Direct PWM interface to 3.3V MCU.
Single 5V gate driver supply with bootstrap voltage clamping and undervoltage lockout.	Ease power management. UVLO provides simultaneous shutdown of high-side and low-side GaN FET in case of gate driver undervoltage.
Two exposed GaN dies on top (SW and PGND). Big PGND pad on bottom.	Realize lower top thermal resistance. Accepts both sides cooling.
Integrated SCP, OTD, and ZVD	BOM reduced for external protection circuitry.

2.3.3 AMC0106M05

The AMC0106M05 and AMC0106M25 are precision, functionally isolated, second-order delta-sigma modulators designed for shunt-based current sensing. The M05 version supports a linear input range of ±50mV. The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The AMC0106M05 modulators are specifically designed for low-voltage applications, are functionally isolated, and come in a small, 2.7mm × 3.5mm leadless package with 1mm creepage and clearance. With the small package size, the AMC0106Mxx isolated modulators enable small PCB layouts that are essential for small form-factor motor drives in robotic applications. Figure 2-4 and Table 2-3 show the functional block diagram and key features.

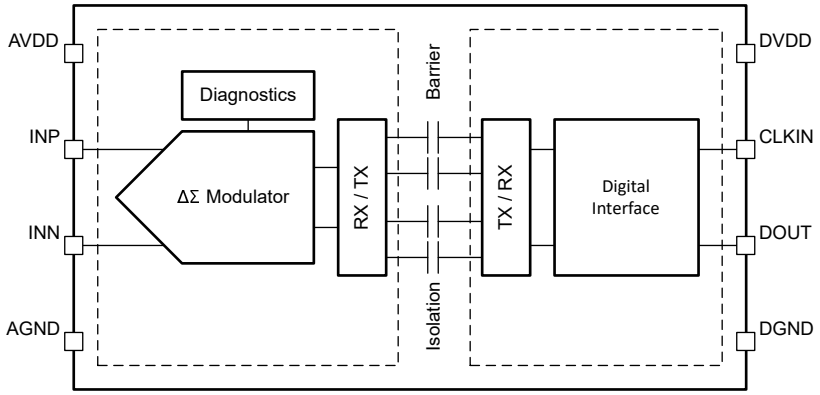


Figure 2-4. AMC0106M05 Functional Block Diagram

Table 2-3. AMC0106M05 Features and Benefits

FEATURES	BENEFITS
Low noise, second-order delta-sigma modulator	Enables precise current sensing up to 14 effective number of bits (ENOB)
Offset drift: ±3µV/°C (maximum)	Allows precise current sensing over entire temperature range without temperature-dependent calibration
High CMTI: 150V/ns (minimum)	Accurate current measurement even during PWM switching and PWM frequencies of 100kHz and above
Digital interface	High EMC immunity, transient ground noise between modulator and MCU does not impact the measurement accuracy
Small, 2.7mm × 3.5mm leadless package	Reduces PCB space and enables smaller servo drives and robotics

2.3.4 DP83826A

The DP83826Ax offers low and deterministic latency, low power and supports 10BASE-Te, 100BASE-TX Ethernet protocols to meet stringent requirements in real-time industrial Ethernet systems. The device includes hardware bootstraps to achieve fast link-up time, fast link-drop detection modes and dedicated reference CLKOUT to clock synchronize other modules on the systems. The two configurable modes are basic standard Ethernet mode that uses a common Ethernet pinout, and *enhanced* Ethernet mode which supports standard Ethernet mode and multiple industrial Ethernet fieldbus applications with additional features and hardware bootstraps configuration. Figure 2-5 shows the functional block diagram and Table 2-4shows the key features and benefits.

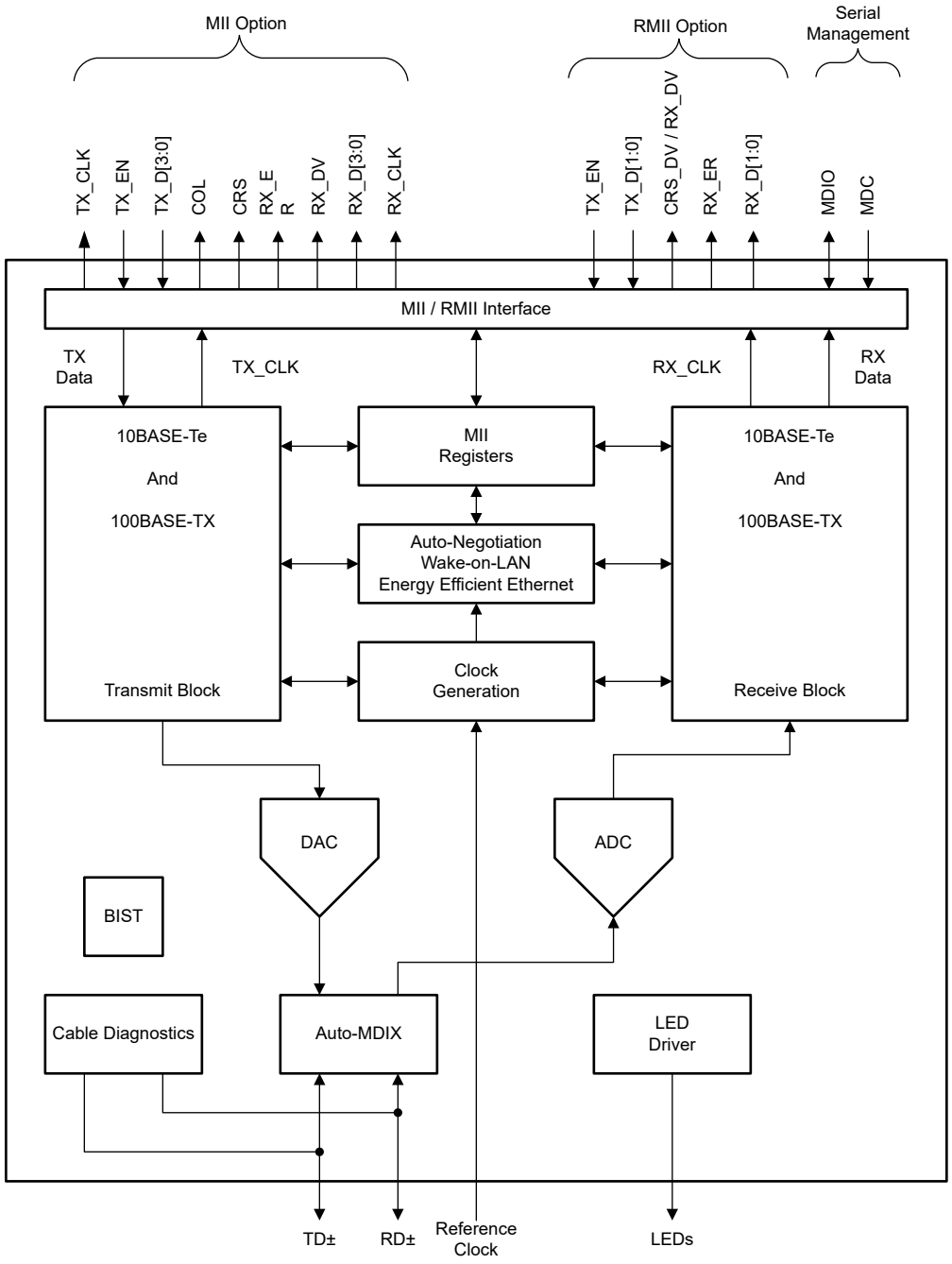


Figure 2-5. DP83826A Functional Block Diagram

Table 2-4. DP83826A Features and Benefits

FEATURES	BENEFITS
Low and deterministic latency	To meet stringent requirements in real-time industrial Ethernet systems such as EtherCAT
Integrated circuitry for enhanced EMC, IEEE 802.3 compliant	Enables robust and EMC compliant system design
Low power consumption, programmable energy-saving modes	Enables less power requirements of the system
Two selectable pin modes in single device	Provides flexible hardware bootstraps without any software for easy configuration
Extended operation temperature range	To support higher ambient temperature such as robot joint application

3 System Design Theory

This section provides design guidelines for this reference design.

3.1 AM2612 Motor Control and Communication Interface

This design leverages the AM2612 ZNC (10mm × 10mm) package as the motor control and communication controller. The motor control interface includes:

- Enhanced Pulse Width Modulator (ePWM) – The PWM peripheral is built up from smaller single-channel submodules with separate resources that can operate together as required to form a system. This design employs ePWM0, ePWM1, and ePWM2 for the three-phase GaN driver. Each ePWM submodule has two channels A and B to generate two complementary PWM signals with configurable dead-band. All these three PWM submodules share the same time base clock of 250MHz and synchronized with each other. Each ePWM module has a synchronization input and an output which can be configured to link to several sources and events such as EtherCAT sync0 pulse and FSI RXTRIG to close the loop between communication and PWM.
- Sigma-delta filter module (SDFM) – The SDFM is a four-channel digital filter designed specifically for current measurement. Each input channel can receive an independent delta-sigma modulator bit stream. The bit streams are processed by four individually programmable digital decimation filters. In this design, Sinc3 filter type and oversampling rate (OSR) 32 are selected for the filter. With 20MHz clock (data rate of Sinc filter), the latency equals 4.8µs. The SDFM clock and SDM clock are generated by ePWM8A and ePWM8B respectively. The benefit of using the ePWM module is the clock phase and frequency can be adjusted and configured according to the real application. The filter triggered by the ePWM0 SOCA event at the center of each PWM period to output the average value of current during the cycle. In addition, the filter set also includes a fast comparator (secondary filter) for immediate digital threshold comparisons for overcurrent and undercurrent monitoring, and zero crossing detection.
- PRU-ICSS GPIO module three channel peripheral interface – This interface supports functionality for operations utilizing the HDSL, Tamagawa, EnDat 2.2 and BiSS protocols. The interface supports both 2-wire and 4-wire serial RS-485 communication. Each channel ranges from 100kHz to 16MHz. The data FIFO size is 32 bits for transmitting and 4 bits for receiving. The shift size and oversampling on receiving input can be configured. In this design, two BiSS encoders are implemented for the motor rotator angle and absolute position feedback after the reducer gearbox. And two PRU-ICSS instances are used for the data decoding of these two encoders. The position feedback is triggered by ePWM3 compare event C which matches ePWM0 SOCA timing.
- PRU-ICSS real-time Media Independent Interface (MII_RT) module – This module provides a programmable I/O interface for the PRUs to access and control up to two MII ports. Each port has 2 level FIFO up to 64-bytes to support different use cases such as auto-forward, on-the-fly and ping-pong processing. Also, this module has the link detection feature and cyclic redundancy check (CRC) on both the TX and RX path. With the deterministic instruction set, the minimum latency is only 3ns under the 100Mbps link.

Figure 3-1 shows the motor control and communication interface of TIDA-010979 and Figure 3-2 shows the motor control configuration.

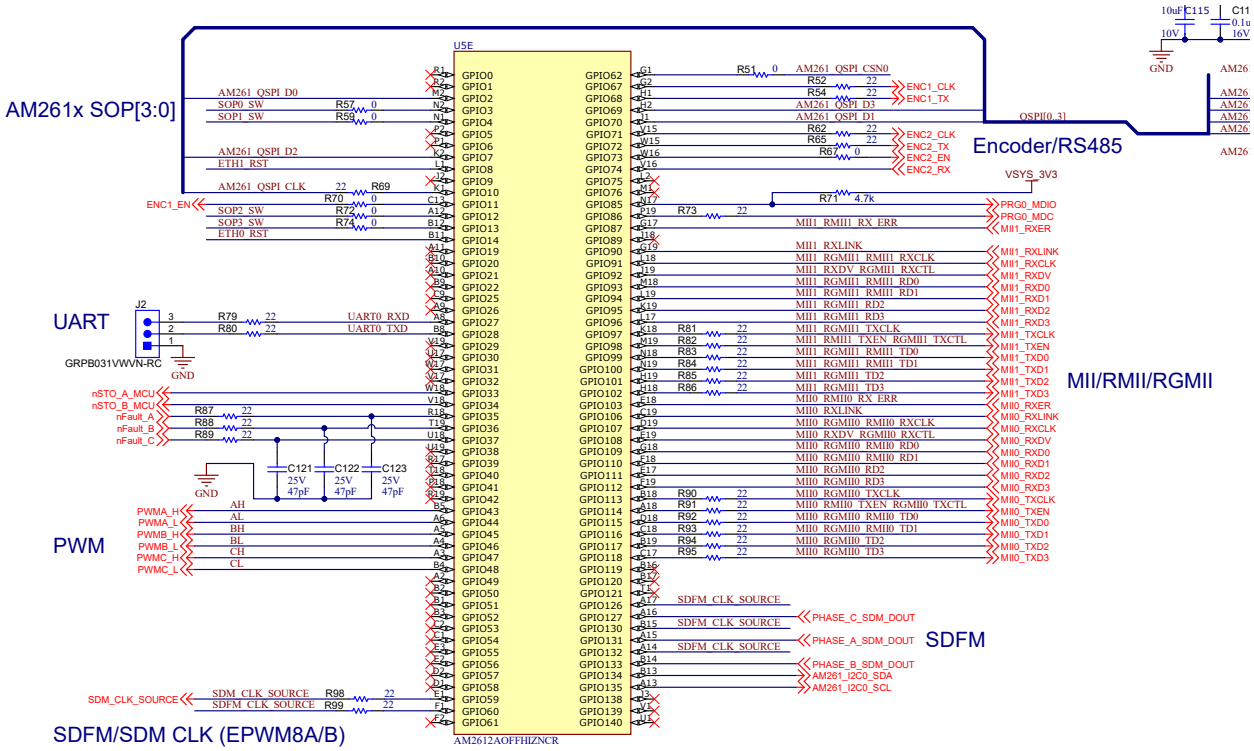


Figure 3-1. TIDA-010979 – AM2612 Motor Control and Communication Interface

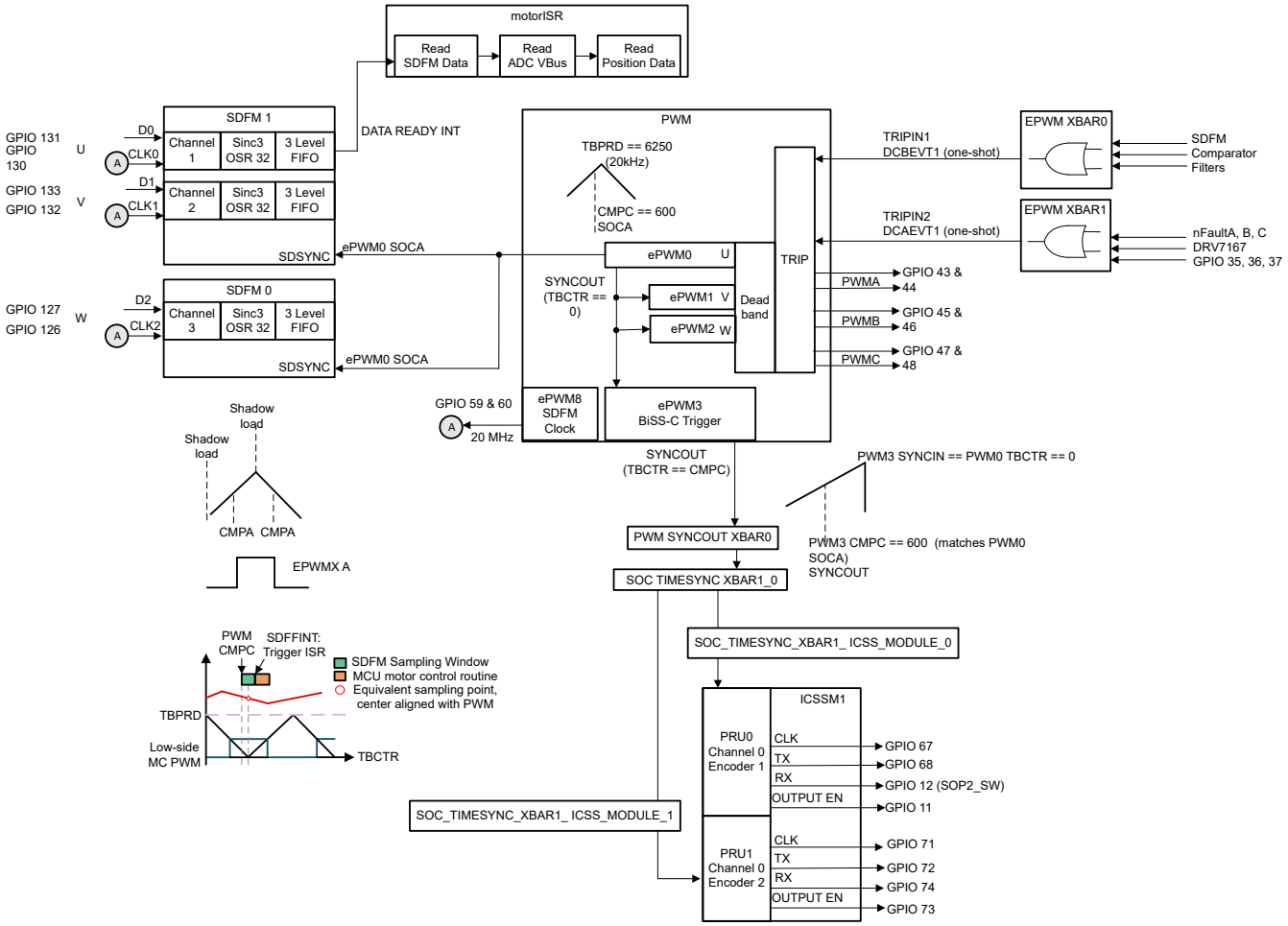


Figure 3-2. TIDA-010979 Motor Control Configuration

3.2 DC Link and Ground Configuration

The nominal 48V DC input voltage is buffered with seventeen 10µF ceramic capacitors to get a total of 170µF DC-bus capacitance. The PCB employs two separated ground planes: the power ground (PGND) and the logic or analog ground (GND). Both ground planes are connected in a star configuration through net ties to minimize the crosstalk of high switching frequency currents in the power ground plane into the logic plane. Figure 3-3 shows the DC-link decoupling and ground configuration schematic.

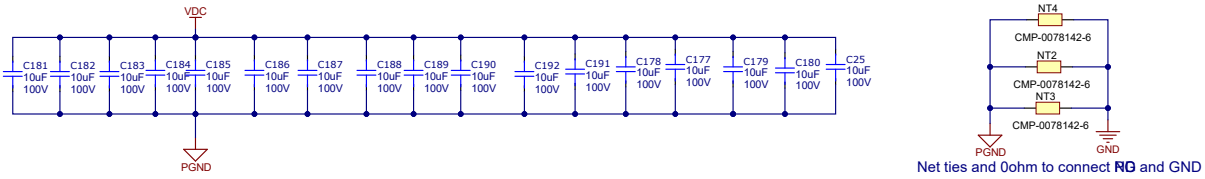


Figure 3-3. DC-Link Decoupling and Ground (GND) Configuration

3.3 Three-Phase Inverter With DRV7167A Half-Bridge GaN Motor Driver Power Stage

This design leverages three DRV7167A 100V pulsed, 70A half-bridge power stage devices, with integrated gate-driver, enhancement-mode GaN FETs and short-circuit protection. The PCB space is further reduced due to high integration and the fact that only a few additional passive components are required. Figure 3-4 shows the schematic of one half-bridge.

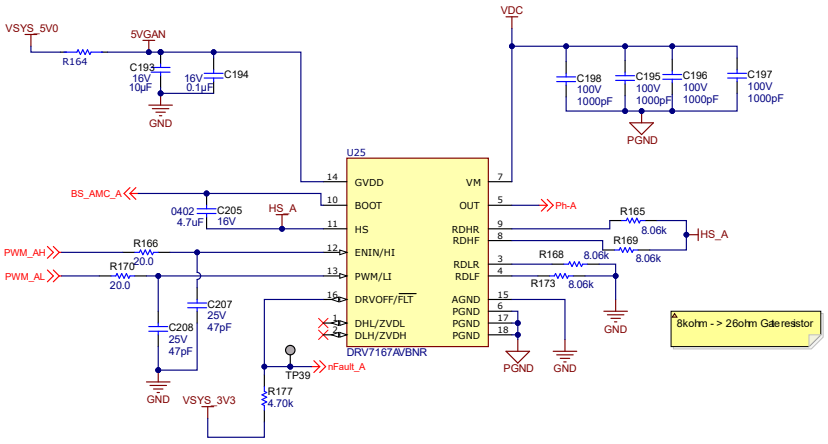


Figure 3-4. Half-Bridge Power Stage Schematic for Phase A

The 48V DC-link voltage is connected to the DRV7167A VM pin and referenced to the power ground (PGND) pin. Local ceramic bypass capacitors C195, C196, C197, and C198 (1nF) are placed in parallel close between the VM and PGND pins to minimize loop inductance.

The DRV7167A integrated gate driver is supplied with 5V. A 10µF and 0.1µF ceramic bypass capacitor (C193, C194) are placed close to the GVDD pin and GND pin, as suggested in the datasheet.

Sequencing is not required for the 5V at GVDD and the 48V at VM, neither during the power up nor power down of the DC voltage input.

A 4.7µF ceramic bootstrap capacitor (C205) is placed close to the BOOT and HS (high-side GaN-FET source connection) pins. R165, R169, R168, and R173 are placed to configure the slew rate of the switch node rising and falling edge. The slew rate control resistors for the tests are 8.06kΩ which equals 2.6Ω gate resistors.

The complementary PWM signals for the high-side and low-side switch from the PWM buffer are low-pass filtered with R166, C207 and R170, and C208 to reject high-frequency impulse noise and avoid false switching with a cutoff frequency of around 160MHz and a propagation of around 1ns. The OUT pin is connected to the motor phase A terminal through a series inline shunt for phase-current sensing, and respectively for the other DRV7167A half-bridges to the phase B and the phase C terminal.

The DRV7167A implements three kinds of protection:

- Short-circuit protection – implements drain-to-source voltage monitoring based short-circuit protection on both FETs which operate on a cycle-by-cycle basis.
- Undervoltage detection – implements UVLO on both the GVDD and BOOT supplies. When the GVDD voltage is below the threshold voltage of 3.8V, both the HI and LI inputs are ignored, to prevent the GaN FETs from being partially turned on. When the BOOT to HS bootstrap voltage is below the UVLO threshold of 3.2V, only the high-side GaN FET gate is pulled low.
- Overtemperature detection – monitors the die temperature of the integrated gate-driver and indicates a fault when the threshold is exceeded. The device does not take any other action, leaving any such protection action to the external PWM controller.

These faults are indicated on the DRVOFF/$\overline{\text{FLT}}$ pin which is the open-drain output. Once asserted, the active low fault signal remains asserted as long any of the three faults exist.

3.4 Inline Shunt Precision Phase-Current Sensing With AMC0106M05 Functionally Isolated, Delta-Sigma Modulator

For precision and small form factor phase-current sensing, this reference design employs delta-sigma modulator current sensing technology to measure the phase current with a 1mΩ inline shunt. The three-phase current is measured with the functional isolated modulator AMC0106M05 that comes in a small leadless package and transmits to the delta-sigma digital filter which is integrated in the AM2612 MCU.

Figure 3-5 shows the schematic of the phase-current sense subsystem using the functionally isolated modulator AMC0106M05 (U28) with a ±50mV linear input voltage range, and a 1mΩ, 3W shunt (R187). The 1mΩ shunt value determines that the linear input range is ±50A. The AMC0106M05 has a ±64mV input clipping range; therefore, the maximum current range is ±64A. The power dissipation in the shunt at $35A_{RMS}$ is 1.25W.

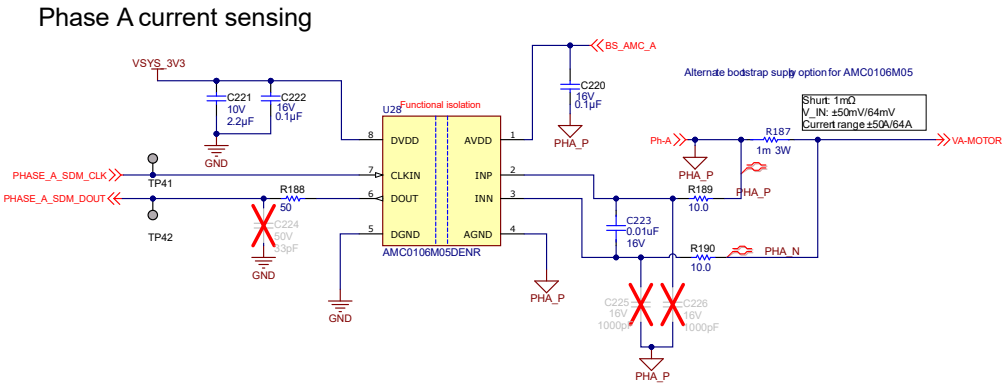


Figure 3-5. Inline Phase Current Sense Schematic With AMC0106M05 for Phase A

The differential anti-aliasing low-pass filter (R189 = 10Ω, R190 = 10Ω, C223 = 10nF) in front of the isolated modulator has a cutoff frequency of 795kHz and helps to improve the signal-to-noise performance of the signal path. The purpose of the low-pass filter is to attenuate high-frequency input noise below the desired noise level of the measurement. Without the input filter, noise close to the sampling frequency or multiples of the sampling frequency, are aliased to low-frequencies by the delta-sigma modulator and are passed through the digital low-pass filter. The capacitors C225 = 1nF and C226 = 1nF are optional and improve common-mode input voltage rejection at frequencies above 10MHz. C225 and C226 are sized ten times smaller than C223. For best performance, make sure C225 and C226 values match better than 5%. Mismatches between C225 and C226 cause differential input errors during common-mode transients. NP0-type capacitors offer low temperature drift and are preferred for common-mode filtering. The analog supply AVDD is decoupled with a 100nF capacitor, C220.

AVDD is supplied by DRV7167A built-in bootstrap supply with C205 = 4.7µF. The AMC0106M05 typically draws 6.6mA from the AVDD supply. This configuration allows for operating at PWM frequencies from 10kHz to 100kHz with a maximum continuous duty cycle of around 95%. See also the test results in the *High Resolution, Small Form Factor Phase Current Sense for 48V Robotics and Servo Drives* application note.

The digital supply DVDD is decoupled with capacitors C221 = 2.2µF and C222 = 100nF. A 50Ω series line termination resistor R188 at the AMC0106M05 DOUT pin improves signal integrity. An optional capacitor C224 = 33pF allows for slew rate reduction of the modulator output bit-stream signal to further reduce EMI. For more information on improving the digital interface from an isolated modulator to a microcontroller, see also the *Achieving Better Signal Integrity with Isolated Delta-Sigma Modulators in Motor Drives* and *Clock Edge Delay Compensation With Isolated Modulators Digital Interface to MCUs application notes* application notes.

3.5 System Power Management

Figure 3-6 shows the power supply tree. A wide input voltage DC/DC buck converter generates the 5V rail. Two independent power modules then generate two rails 3.3V and 1.8V from 5V, respectively. The 3.3V supplies all the IO voltage of the MCU and another analog parts such as logic gate, modulator, and transceivers. The 1.8V supplies the voltage shifter for the clock input of AM2612 and can also supply the 1.8V flash as another option. Another power module generates the 1.25V rail from 3.3V which supplies the core voltage of AM2612.

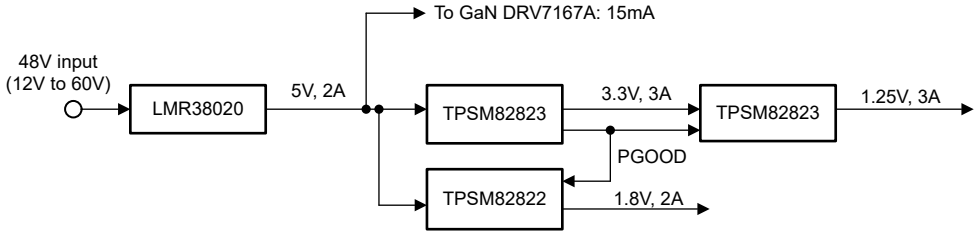


Figure 3-6. TIDA-010979 System Power Tree

The LMR38020 DC/DC buck converter operates with an input voltage ranging from 12V to 60V. The output voltage reaches 5V. The DC/DC buck converter feedback circuit achieves minimum output voltage ripple and delivers at least 2A output current. To minimize size, the switching frequency operates at 617kHz requiring only a 22µH inductor. The output ripple measures less than 15mV when output current exceeds 0.1A through simulation. The 5V rail powers downstream power rails and provides logic power for GaN DRV7167A devices.

For the 3.3V rail and 1.25V rail, two independent power modules TPSM82823 with 2mm × 2.5mm super small package meets the 3A output current requirement. The power modules integrate a synchronous step-down converter and an inductor to simplify design, reduce external components, and save PCB area.

In the same manner as the 3.3V rail, the 1.8V rail generated by TPSM82822 with fixed output application to reduce the external components. The controller MCU AM2612 needs to be supplied with 3.3V (VDDS33, VDDA33), 1.8V (VDDS1833_FLASH0, VDDS1833_FLASH1), and 1.2V (VDD, VDDARx) supplies externally. There is no power sequence requirement with 3.3V flash for MCU AM2612. But when 1.8V flash is used, the 1.2V and 1.8V rails are recommended to ramp up at least 50µs after 3.3V (VDDS33, VDDA33) ramp up. This reference design leverages the power good signal generated by 3.3V power module to enable the 1.2V and 1.8V rails according to the recommendation from the technical reference manual. This reference design uses 3.3V flash.

3.6 Functional Safety Concept

Figure 3-7 shows the functional safety concept of this reference design. The safety goal is Category 3, Performance D or E according to the safety standard ISO13849-1. This safety concept is not accessed by any notified body and is just an example to showcase the safety chain inside a motor control system. Additional circuitry such as redundancy channels for power rails (dual 3.3V for both safe channels), safe switch to turn off the power supplies, and diagnostic circuitry are not implemented in this design.

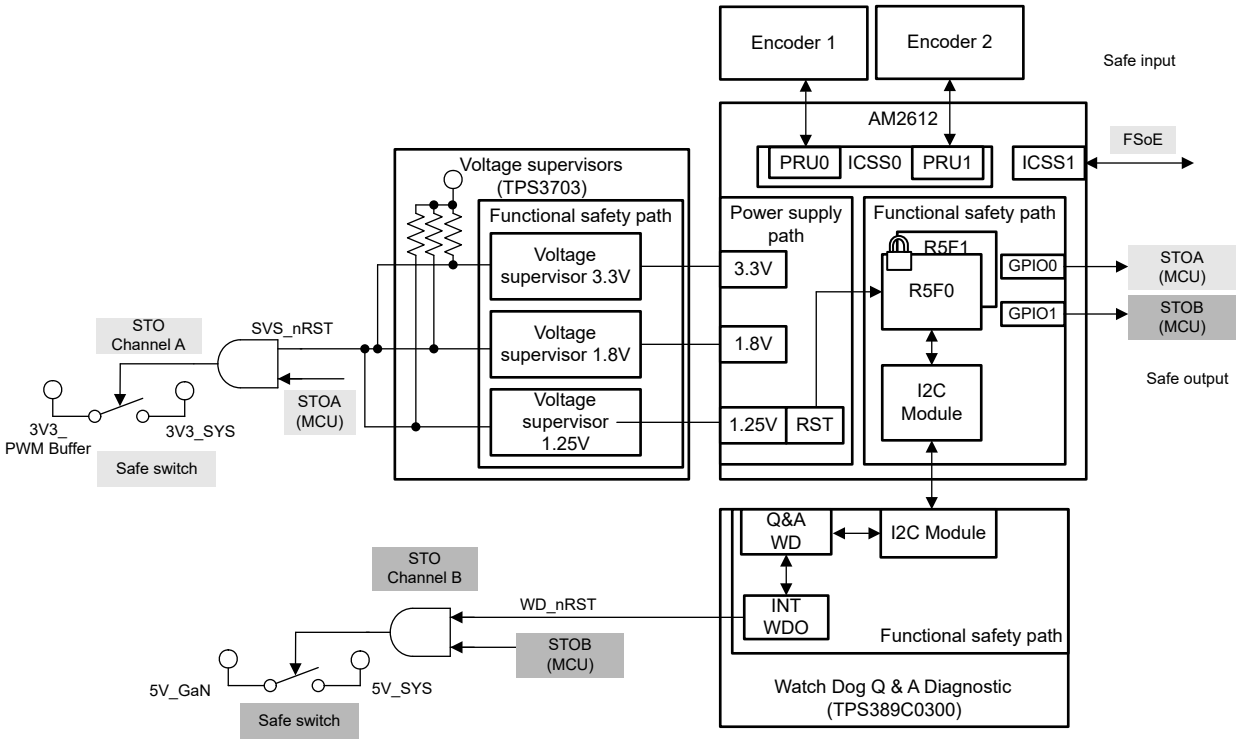


Figure 3-7. TIDA-010979 Functional Safety Concept

The safety chain includes safe input, safe logic (MCU), and safe output. The safe input can be either from dual-channel encoders or from safe Ethernet according to the different requirements. The safety data is transmitted as black channel and the safe MCU performs cross monitoring for the safety data. Once the safe MCU receives the trigger command or the fault is detected by the diagnostic circuitry, then the dual-channel safe output turns off the safe switches to trigger the safety function. The system enters a pre-defined safe state. Table 3-1 describes how the power-supply diagnostic works to detect the dangerous fault to fulfill category 3, performance D safety target.

Table 3-1. Power Supply Fault and Diagnostic

FAULT TYPE	SAFE MCU	SUPPLY VOLTAGE SUPERVISORS (SVS)	POWER SUPPLIES	WATCHDOG Q&A
Power supplies overvoltage (OV)	MCU in dangerous state	Detects error and triggers safe state	Power not functioning	Q&A detects wrong behavior (logic or timing) of MCU and triggers safe state
Power supplies undervoltage (UV)	Brownout trigger of MCU and triggers safe state	Detects error and triggers safe state	Power not functioning	Q&A detects wrong behavior (logic or timing) of MCU and triggers safe state
Watchdog (WD) Q&A fails	Q&A detects wrong behavior (logic or timing) of MCU and triggers safe state	SVS Detecting OV and UV	Power within specification of MCU	Q&A not functioning
SVS fails OV	Q&A detects wrong behavior (logic or timing) of MCU and triggers safe state	SVS not functioning	Power within specification of MCU	Q&A detects wrong behavior (logic or timing) of MCU and triggers safe state
SVS fails UV	Brownout trigger of MCU and triggers safe state	SVS not functioning	Power within specification of MCU	Q&A detects wrong behavior (logic or timing) of MCU and triggers safe state

3.7 Ethernet Physical Layer

This design leverages two DP83826A Ethernet PHYs to enable the daisy chain connection for EtherCAT sub-device applications. Figure 3-8 shows one of the PHY circuitry with transformers and connector.

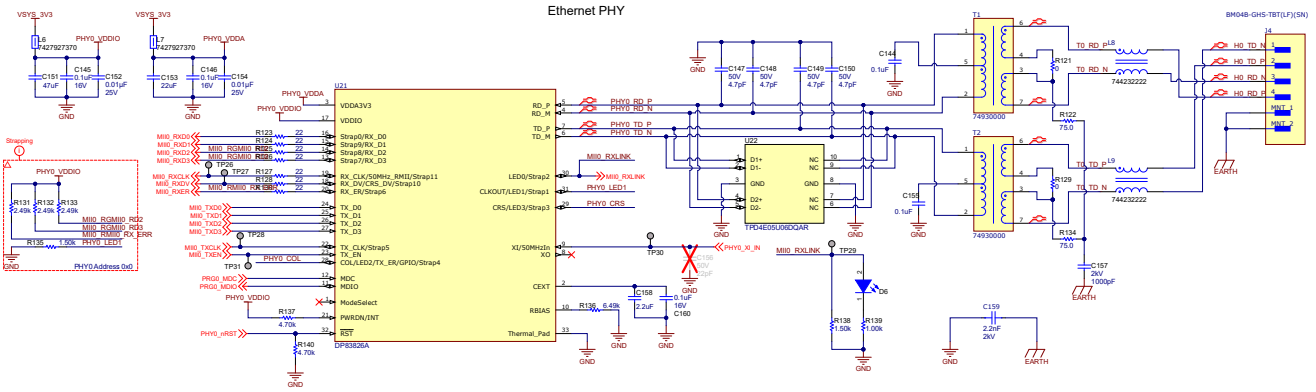


Figure 3-8. Ethernet PHY0 Schematic

Enhanced mode is selected by floating pin 1 of U21 to enable hardware strap configuration for EtherCAT usage. R131, R132, R133, and R135 are strap resistors. See the *How and Why to Use the DP83826 for EtherCAT® Applications* application note for the details. Both the analog power (VDDA3V3) and digital IO power (VDDIO) are decoupled by ferrite bead L6 and L7. Media Independent Interface (MII) is used for minimum latency on the Ethernet signal path to connect between PHY and medium access control (MAC) layer. ESD diode U22 is put on the Media Dependent Interface (MDI) differential lines to suppress the noise. Discrete transformers (T1, T2), common mode choke (L8, L9) and connector (J4) are implemented instead of integrated RJ45 port to reduce the PCB space. R122, R134, and C157 are also connected as Bob Smith termination to reduce the noise.

3.8 Position Feedback Interface

This design leverages four SN65HVD75 RS-485 transceivers to provide feedback from two position encoders using the BiSS-C protocol. Encoder 1, with 20-bit resolution, provides feedback on the absolute position data of the motor rotor, which is used for FOC loop motor control. Encoder 2, with 19-bit resolution, provides feedback on the absolute position data for the end user and is located after the gearbox reducer. The differential lines, including clock and data signals, are connected to the position board. The CMOS signals from the transceivers are connected directly to the PRU-ICSS IOs using Three Channel Peripheral Interface mode, which is designed specifically for absolute encoder position feedback. Figure 3-9 shows the schematics of these two position feedback interface.

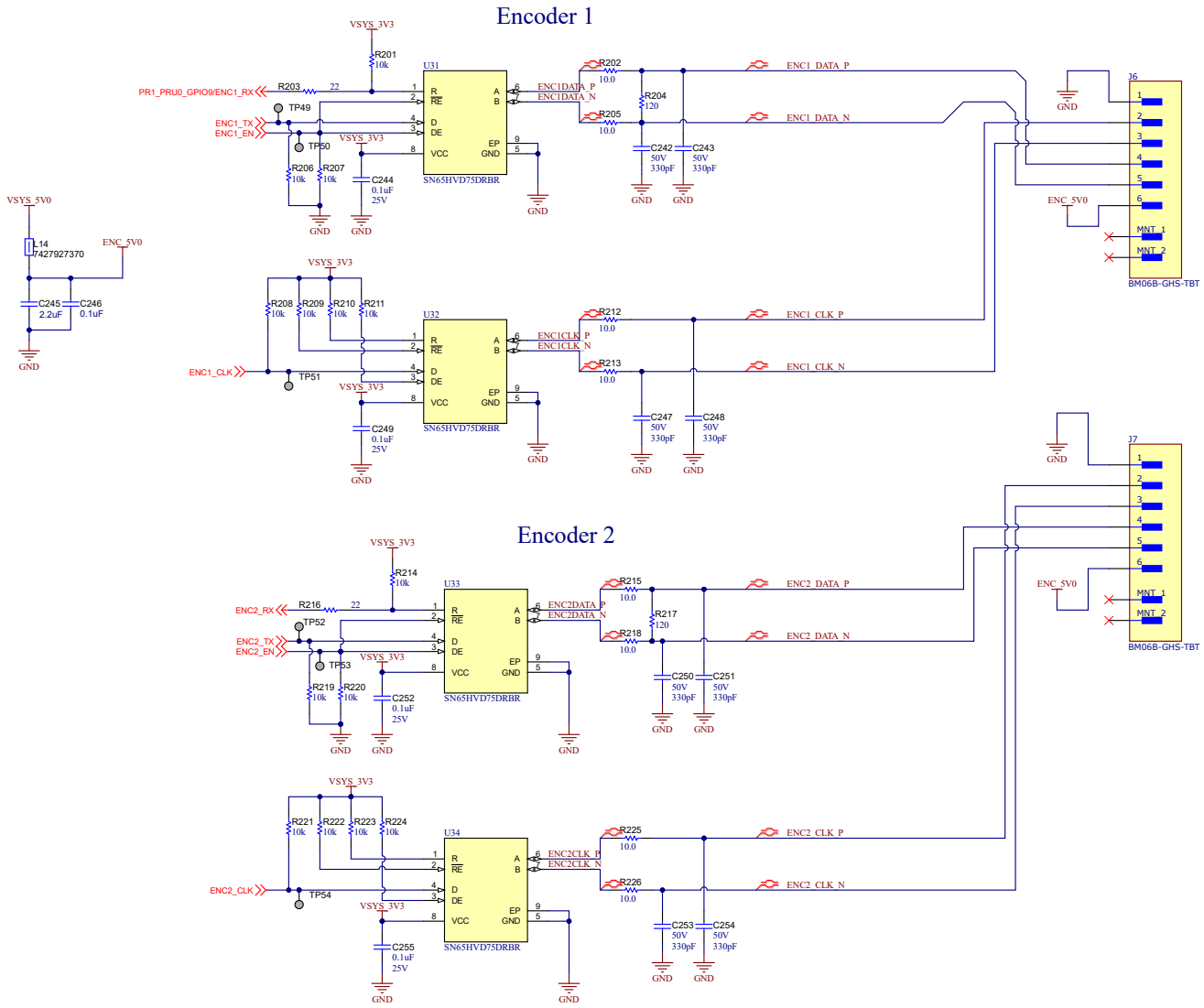


Figure 3-9. Position Feedback Encoder Interface Schematics

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

4.1.1 TIDA-010979 PCB Overview

Figure 4-1 and Figure 4-2 show labeled photos of the top and bottom views of the PCB.

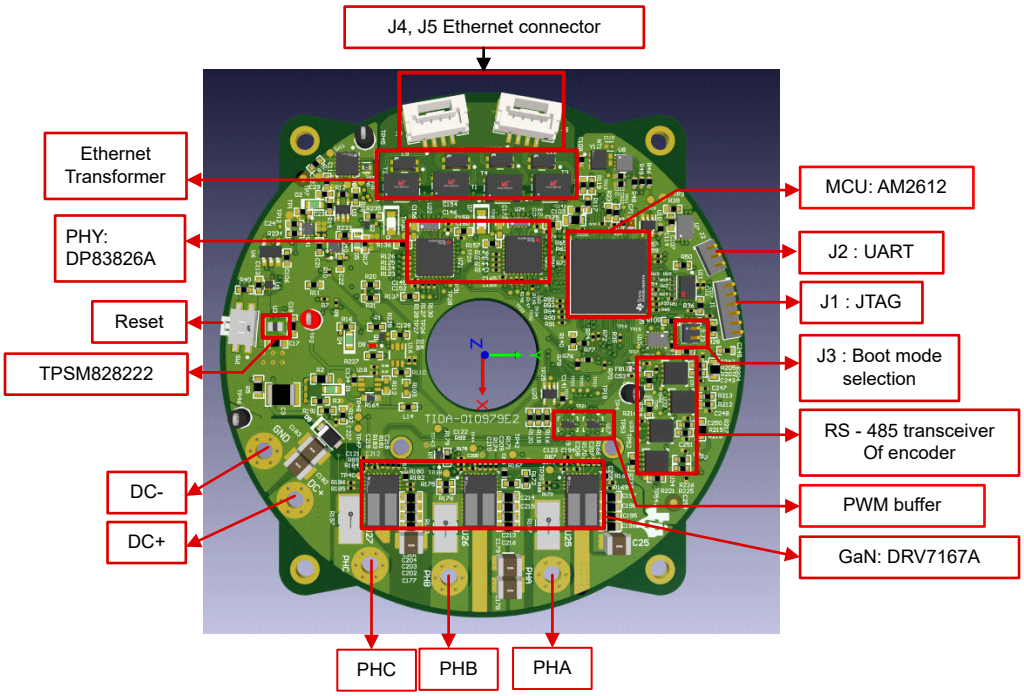


Figure 4-1. TIDA-010979 PCB Top View

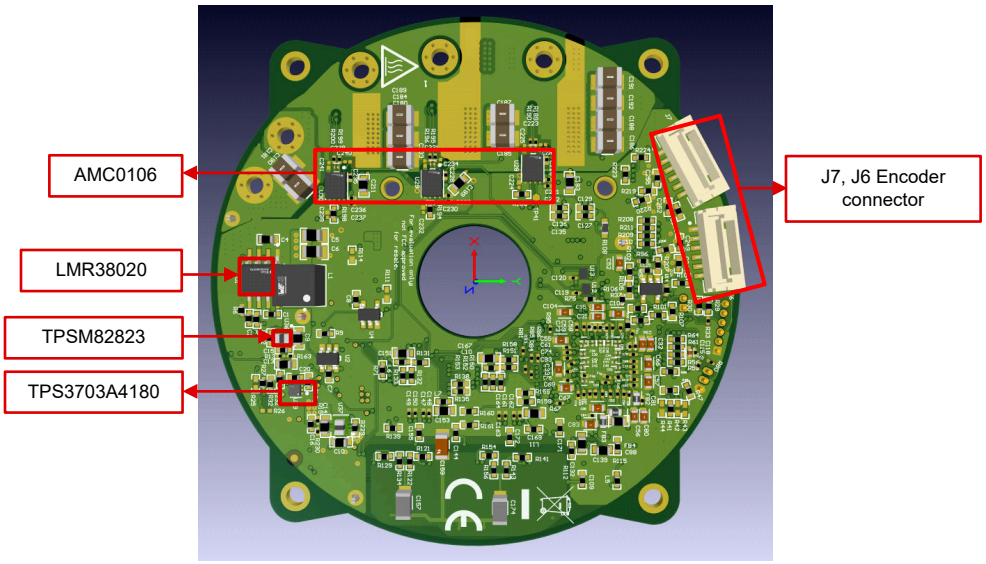


Figure 4-2. TIDA-010979 PCB Bottom View

4.1.2 TIDA-010979 Hardware Setting

To enable the TIDA-010979 board, apply DC voltage 48V (or lower voltage depending on motor rating) between DC+ and DC– through holes. Connect the three motor phase power cables to PHA, PHB, and PHC through holes.

J1 serves as the JTAG connector for software code debugging. Connect the XDS110 JTAG Debug Probe to J1. J2 serves as the UART connector and can also connect to the XDS110 AUX pins to print information on terminal or transmit data such as writing the flash through UART communications.

J3 serves as the boot mode selection jumper. With J3 shorted, the OPSI (4S) – Quad Read mode is enabled as the MCU boot mode. With J3 opened, the UART mode is enabled as the MCU boot mode. For more information regarding AM2612 boot mode, see also the EVM setup in the *AM261x MCU+ SDK 11.01.00* user guide.

J6 serves as the connector for encoder 1 to provide feedback for the position information of motor rotator while J7 serves as the connector for encoder 2 to provide feedback for the position information of the gearbox reducer. J4 and J5 serve as Ethernet connectors that can function as one port IN and one port OUT for daisy chain applications. Figure 4-3 shows the TIDA-010979 hardware setup overview.

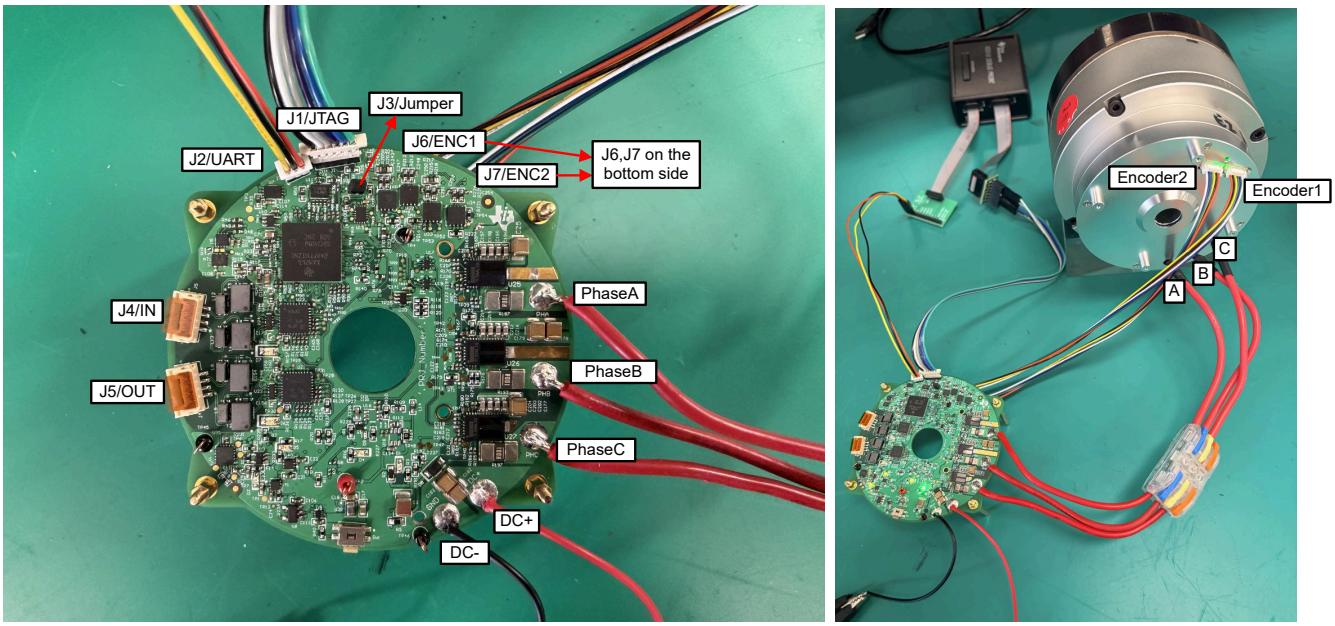


Figure 4-3. TIDA-010979 Hardware Setup Overview

4.2 Software Requirements

A TI internal test software is developed for the AM2612 ZNC package to validate this reference design.
For AM2612 software support, see the MCU-PLUS-SDK-AM261X Software development kit (SDK), MOTOR CONTROL SDK for AM261x, and IND-COMMS-SDK Software development kit (SDK) tool page and the Arm-based microcontrollers forum - Arm-based microcontrollers - TI E2E support forums for Sitara microcontrollers.

4.3 Test Setup

Table 4-1 lists the key test equipment. Description and pictures of the test setup for specific tests are provided in the section of the corresponding test results.

Table 4-1. Key Test Equipment

DESCRIPTION	PART NUMBER
High-speed oscilloscope	Tektronix MSO4104B
Single-ended probes	Tektronix P6139B
Isolated current probe	CYBERTEK CP8030H, HIOKI CT6872
Dynamometer	MAGTROL DSP6000
Multimeter	Fluke 17B+
Thermal camera	TESTO 865
Adjustable power supply (10A)	ITECH IT6724H
Adjustable power supply (20A)	ITECH M3902C
Low voltage servo motor (72V, 21A)	7H2207124422

4.4 Test Results

4.4.1 Power Management and System Power Up and Power Down

The is used to validate the onboard power supplies, voltage, and sequence including 5V, 3.3V, 1.8V, and 1.25V rails.

Figure 4-4 and Figure 4-5 showcase the power up and down waveforms, respectively.

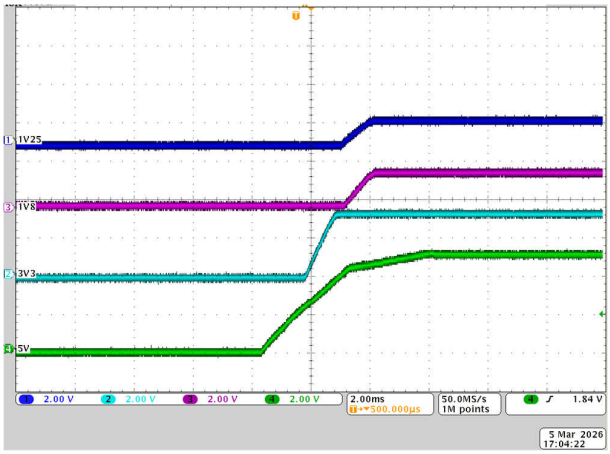


Figure 4-4. TIDA-010979 System Power Up

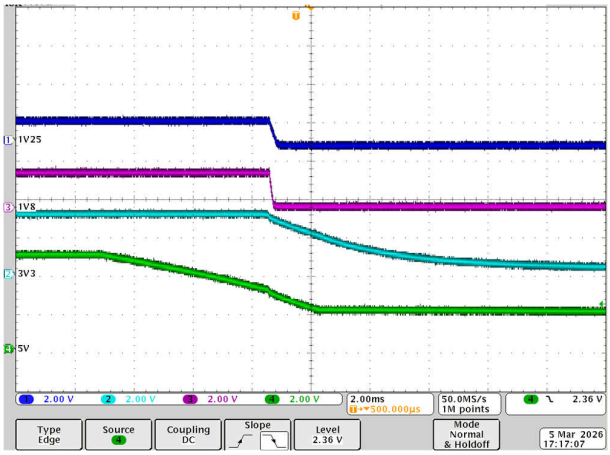


Figure 4-5. TIDA-010979 System Power Down

4.4.2 Half-Bridge GaN Motor Driver Power Stage Switch Node

Figure 4-6 through Figure 4-9 outline the switching transient voltage, propagation delay, and the configurable slew rate (20% to 80%) for both rising and falling edge with the output phase current at $10A_{RMS}$ and 80kHz PWM frequency. Overshoot voltage is around 14V when 0Ω control resistors are implemented.

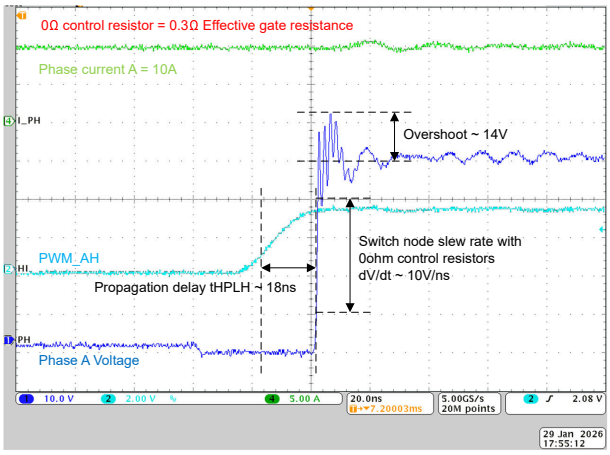


Figure 4-6. Rising Slew Rate With 0Ω Control Resistor

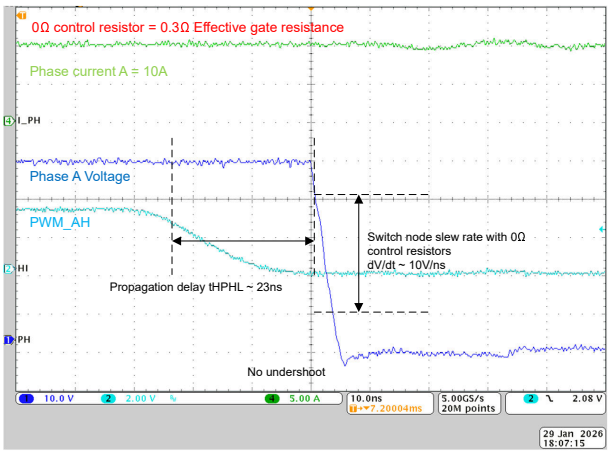


Figure 4-7. Falling Slew Rate With 0Ω Control Resistor

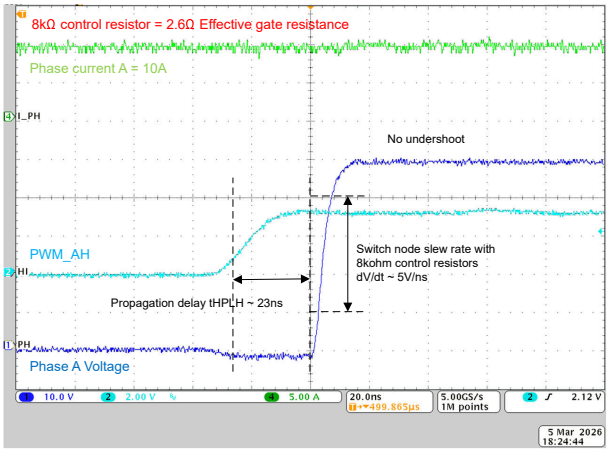


Figure 4-8. Rising Slew Rate With 8kΩ Control Resistor

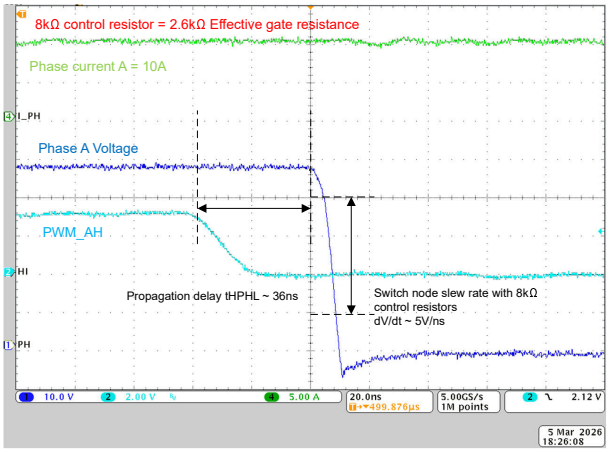


Figure 4-9. Falling Slew Rate With 8kΩ Control Resistor

4.4.3 Power Stage Thermal Measurements

The thermal measurement testing is done at a lab temperature of 25°C. The TIDA-010979 board is powered by a 48V DC source and connected to a high-power servo motor that serves as a load with a maximum 72V, 21A capability. A dynamometer supplies a high load to the motor. The PWM carrier frequency operates from 40kHz to 80kHz. The dead band operates at 40ns. The motor speed operates at 80Hz. Figure 4-10 shows the thermal test setup. For all these thermal tests, neither a heat sink nor a fan operates, hence only natural convection of the TIDA-010979 PCB applies.

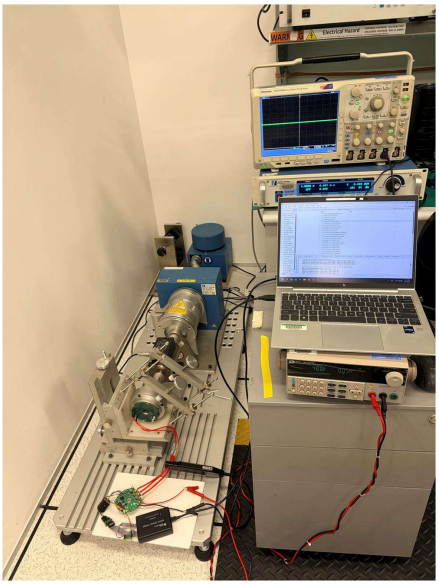


Figure 4-10. Thermal Measurement Test Setup

Since DRV7167A has exposed dies on top, the case temperature of DRV7167A can be very close to the temperature of the die. The recommended junction temperature is up to 125°C. In this test, the GaN device achieved 115°C with $16A_{RMS}$ phase current at 20kHz PWM frequency and achieved 118°C with $14A_{RMS}$ phase current at 80kHz PWM frequency when thermal balance status is reached. Figure 4-11 shows the thermal picture of TIDA-010979 at $16A_{RMS}$ at 20kHz PWM and Figure 4-12 shows the thermal picture of TIDA-010979 at $14A_{RMS}$ at 80kHz PWM. Figure 4-13 shows the temperature rise curve for both test conditions. The maximum phase-current within 2 minutes is around $17.4A_{RMS}$ at 20kHz PWM carrier frequency. With $17A_{RMS}$ at 48V, the inverter output peak power reaches 1kW assuming the power factor equals 1.

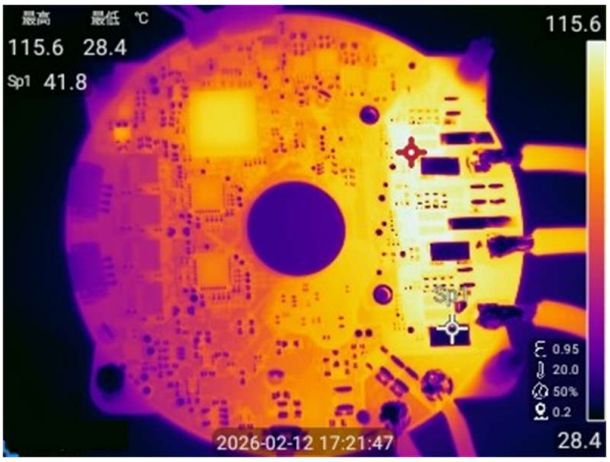


Figure 4-11. DRV7167 Thermal Picture at $16A_{RMS}$ at 20kHz PWM

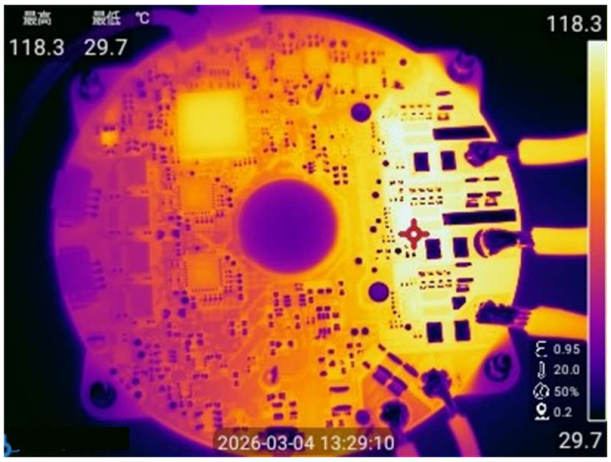


Figure 4-12. DRV7167 Thermal Picture at $14A_{RMS}$ at 80kHz PWM

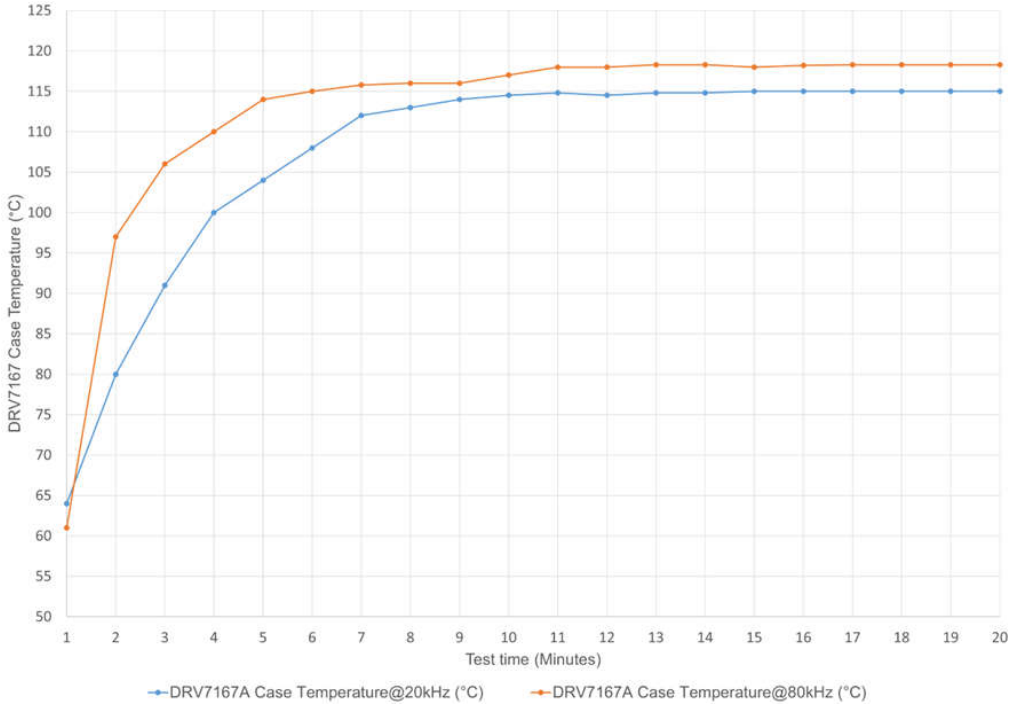


Figure 4-13. DRV7167A Temperature Rise Curve

4.4.4 Phase-Current Sensing and Position Feedback

The AMC0106M05 modulator clock input is driven from one EPWM module and the modulator output data bitstream is decimated on AM2612 MCU through a Sinc3 filter running at oversampling ratios (OSR) from 32 to 256. For detailed test results on phase-current sensing with the functional isolated modulator AMC0106M05, see the *High Resolution, Small Form Factor Phase Current Sense for 48V Robotics and Servo Drives* application note. Figure 4-14 shows the phase A and phase B current waveform when reference current of Q axis is set to 20A. From the test results, observe that the peak current is matched well with the reference current given in software.

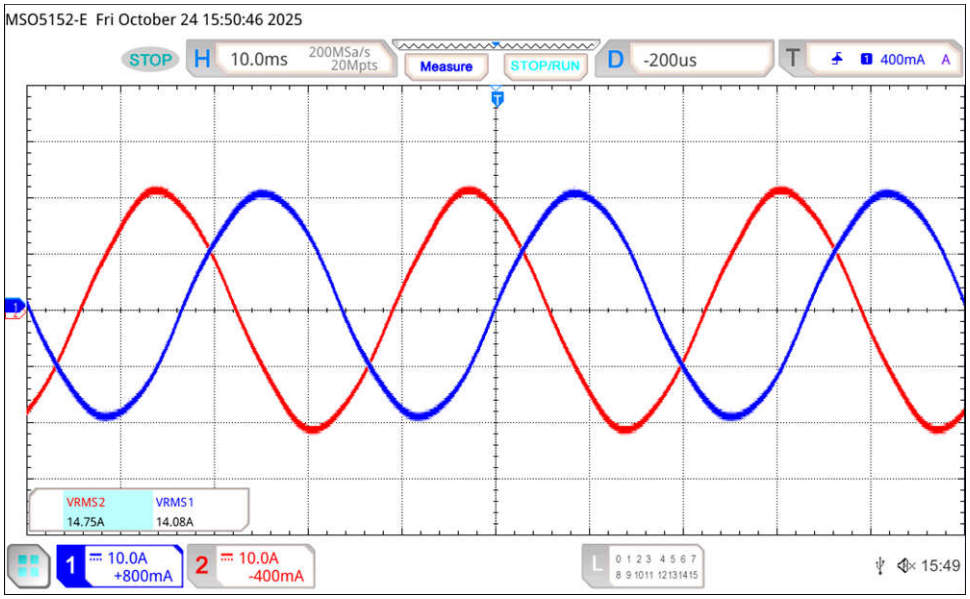


Figure 4-14. Phase-Current at 20A Peak

Figure 4-15 showcases the position data gathering from encoder 1 which represents the mechanical motor rotating angle and the electrical angle which is used for FOC control loop. The electrical angle equals the motor mechanical angle multiplied by motor pole pairs. The EYOU motor has eight pole pairs.

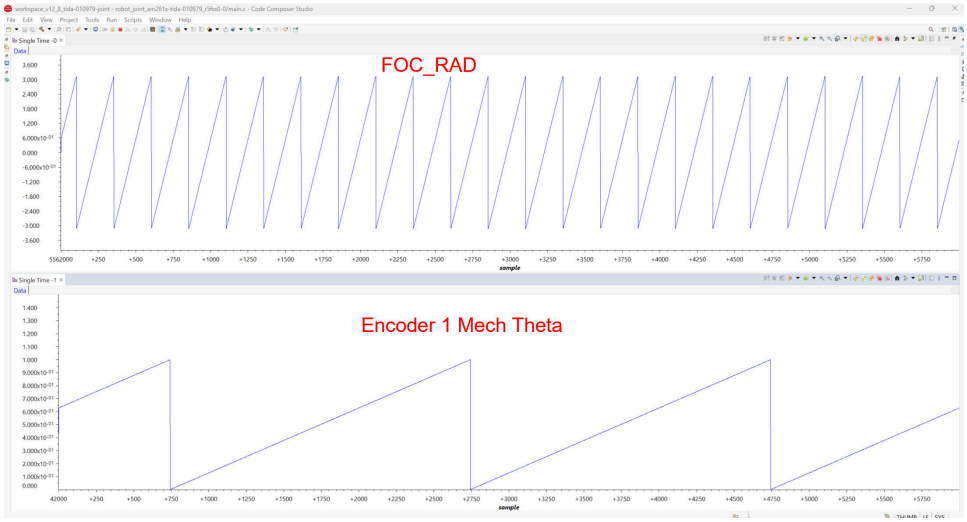


Figure 4-15. Encoder Position Feedback Data

4.4.5 EtherCAT® Communication

This test verifies the data transmitting between physical layer and medium access control (MAC) layer. Additionally, the EtherCAT link and PHP data objects (PDO) are verified establishing on data-access abstraction layer which is used for position loop control. Figure 4-16 shows the physical layer and MAC layer connectivity.

```
Local Implementation
Pruicss  max =3 selected PRU:3
pRegPerm = 0x48002000, dram1=0x48002000, offset = 0x00000000, size = 0x00001400
PRU ESC: Rev 0590 | Bld 0537 | INTC base: 0x48020000 , id = 0x4e82a900
INTC.HIDISR addr: 0x48020038
EC_SLV_INT_EEPEMU_prepare:652: Set CatSyncMan[1]:sa=0x1000, len=0x100, ctrl=0x26, ena=1
EC_SLV_INT_EEPEMU_prepare:661: Set CatSyncMan[2]:sa=0x1100, len=0x100, ctrl=0x22, ena=1
EC_SLV_INT_EEPEMU_prepare:670: Set CatSyncMan[3]:sa=0x1200, len=0xc00, ctrl=0x64, ena=1
EC_SLV_INT_EEPEMU_prepare:687: Set CatSyncMan[4]:sa=0x1e00, len=0xc00, ctrl=0x20, ena=1
+EC_SLV_APP_setObdValues
Configure Phy bits: PhyAddr:2, LinPol:LOW, PhyAddr:0, LinPol:LOW, (0x5)
DP83826E detected
DP83826E detected
PRU_PHY_detect:152 Phy 0 alive
PRU_PHY_detect:152 Phy 2 alive
PHY Disable Magnetics
PHY Enable Magnetics
TI EtherCAT Toolkit CiA402 for AM261X.R5F - e000059dh / 54490029h
Explicit Device ID : 0x   5

****EC SubDevice************************************************************
Numeric Version: 0x00020101
Source Id: <04930bfed349b5aced41953f837ced6ed9d62c30>
****HWAL********************************************************************
Numeric Version: 0x00020100
Friendly Version: <KB HWAL v00.02.01.00>
Source Id: <3764cbbee02563e73129376ccac8d785bd6e2773>
****OSAL********************************************************************
Numeric Version: 0x00010301
Friendly Version: <KB OSAL v00.01.03.01>
Source Id: <5e1dcc50bb40791bdb358cecc4e4fd35beca6d1e>
****************************************************************************
SSC_checkTimer:MaxD:9420448 (9)
SSC_checkTimer:MaxET:7
SSC_checkTimer:MaxD:11999872 (11)
PDO size In:0x27/0xd
PDO size Out:0x27/0xd, In:0x27/0xd
```

Figure 4-16. Data Transmitting Between PHY and MAC

Figure 4-17 showcases the EtherCAT state machine and PDO box data.

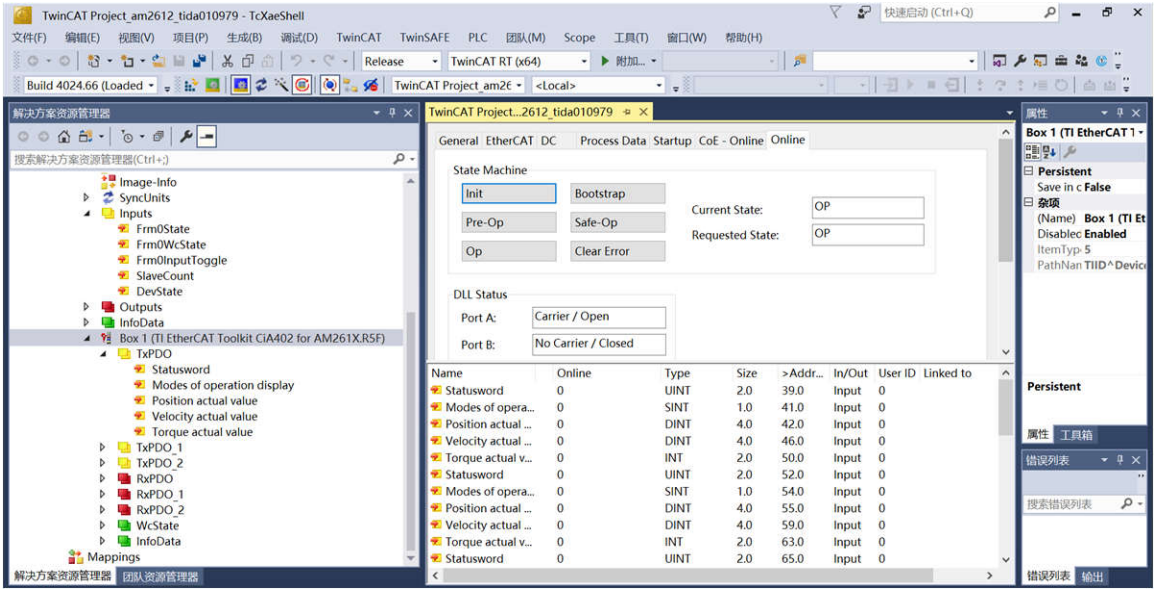


Figure 4-17. EtherCAT® State Machine and PDO Box

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010979.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010979.

5.1.3 Layout Prints

To download the layer plots, see the design files at TIDA-010979.

5.1.4 Altium Project

To download the Altium project files, see the design files at TIDA-010979.

5.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010979.

5.1.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010979.

5.2 Tools and Software

Tools

CCSTTUDIO	Code Composer Studio™ integrated development environment (IDE): download CCS 12 or 20 version for Microsoft® Windows® or Linux®
ARM-CGT-CLANG	Arm® code generation tools - compiler: download TI ARM CLANG LTS for Microsoft Windows or Linux
SYSCONFIG	Standalone desktop version of SysConfig: download SysConfig 1.26.2 for Microsoft Windows or Linux

Software

AM261x MCU+ SDK	MCU PLUS SDK Microsoft Windows Installer
AM261x Motor Control SDK	Motor Control SDK Microsoft Windows Installer
AM261x Industrial Communication SDK	Industrial Communications SDK Microsoft Windows Installer

5.3 Documentation Support

1. Texas Instruments, *AM261x Sitara™ Microcontrollers Datasheet*
2. Texas Instruments, *AM261x Sitara™ Microcontrollers Technical Reference Manual (TRM)*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.5 Trademarks

6 About the Author

CHEN GAO is a System Engineer in the Industrial System Robotics team at Texas Instruments and responsible for specifying and developing reference designs for industrial motor drive and robotics.

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The authors recognize the excellent contribution from **HAN ZHANG** and **LORI HEUSTESS** to support the software development of the TIDA-010979 reference design.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2025) to Revision A (March 2026)	Page
• Updated entire document for full TIDA-010979 reference design support	2

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