Design Guide: TIDA-020101

Automotive 48V 300W HVAC Pump, Blower, and Fan Reference Design

Description

This reference design demonstrates a 48V, 300W peak smart motor brushless direct current (BLDC) implementation. The discrete approach enables compact and flexible form factors with diameters as small as 55mm. The design maintains low power sleep modes of less than 100µA. The design leverages TI semiconductors to facilitate efficient operation. The architecture provides a robust foundation for demanding automotive heating, ventilation, and air conditioning (HVAC) applications requiring high power, precision, and miniaturization.

Resources

TIDA-020101	Design Folder
DRV8363-Q1	Product Folder
TLIN4029A-Q1	Product Folder
MSPM0G3507-Q1	Product Folder
LM5168-Q1	Product Folder
TPS7B81-Q1	Product Folder
MSPM0 Sensorless FOC Tuning	User's Guide

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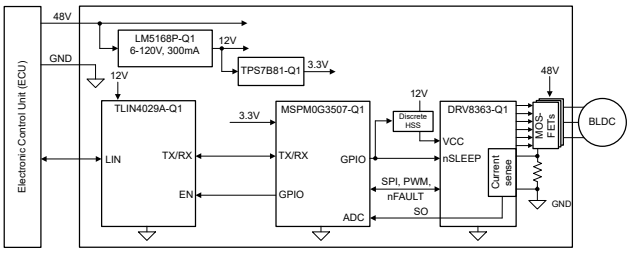
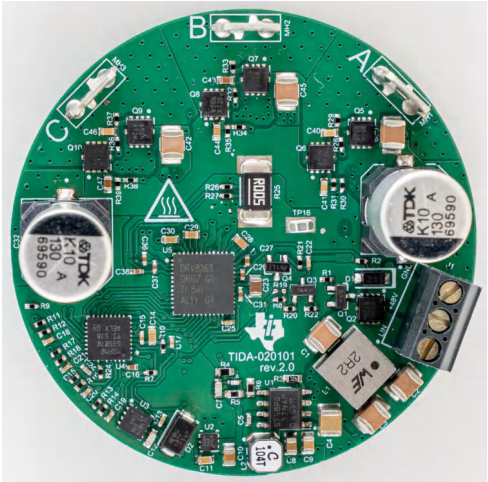
Features

- Small form factor (55mm diameter PCB, single-sided component placement)
- Low sleep current (<100µA maximum)
- 70V LIN bus fault voltage robust LIN communication in 48V architecture
- Ready-to-use field-oriented control (FOC) algorithm plus royalty-free microcontroller abstraction layer (MCAL) driver (local interconnect network [LIN] 2.x and approximately 50Hz to 10kHz pulse width modulation [PWM])
- Sleep and wake over LIN
- Flexible communication interface supports LIN2.x and PWM (about 50Hz to 10kHz PWM)

Applications

- Automotive thermal management blower, fan, and pump module
- Engine fan
- Automotive pump





1 System Description

Brushless DC (BLDC) motors gain momentum in automotive applications due to enhanced performance characteristics compared to brushed DC (BDC) motors. BLDC motors offer higher efficiency, extended lifespan, and reduced electrical noise.

Meanwhile, the shift toward 48V architecture continues to gain momentum. Within smart actuators, loads beginning at approximately 100W are anticipated to be among the first to transition from 12V to 48V, as these loads offer the greatest potential for weight reduction.

This reference design presents a comprehensive approach for implementing a 48V BLDC smart motor in various automotive equipment, including HVAC blowers, electric fluid pumps, cooling fans, and other related devices. The design addresses the evolving market trend by supporting a compact form factor of 55mm diameter round shape. Additionally, this reference design takes advantage of TI low sleep current (<100µA maximum) for enhanced power efficiency.

A primary feature of this reference design uses TI single-shunt sensorless FOC algorithm for commutation control, which can be fully customized and integrated into user-specific applications. This algorithm integrates with a royalty-free MCAL driver supporting LIN2.x and PWM frequencies up to 10kHz, providing flexible communication options for seamless system integration.

To enable secure system operation, this reference design features built-in secure boot and firmware update capabilities, allowing users to maintain precise control over the system software configuration. Furthermore, the implementation of industry-leading robust LIN communication in 48V architecture showcases TI's commitment to reliability and performance, with a notable exception being the industry-first 70V LIN bus fault voltage transmitter in the market.

To address scalability requirements, this reference design engineers pin-to-pin compatibility across various interfaces, including LIN TX and LIN RX, motor power, and other relevant connections. The system also supports sleep and wake functionality over LIN, allowing devices to enter low-power states during periods of inactivity while maintaining quick responsiveness.

The analog components feature reverse polarity protection and PI-filter, encapsulated in a compact circular PCB with a diameter of 55mm. This form factor closely replicates the typical motor drive board, facilitating easy integration into existing systems. The PCB is using a 3-pin screw connector providing access to +48V, GND, and LIN signals.

1.1 Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	Recommended operating condition	13	48	85	V
I_{IN}	Input current	Input current capabilities EMI filter	–	-	12.4	A
$I_{OUT,rms}$	Output current		–	6.25	–	A
I_{SLEEP}	Sleep current	Current at input connector when system is in sleep mode	–	80.7	–	µA
V_{LIN_FAULT}	LIN bus fault voltage		–	–	±70	V
f_{PWM}	PWM frequency		–	20	–	kHz
f_{FOC}	FOC rate	FOC control loop rate		5	16	kHz
T_A	Ambient temperature		–40	25	125	°C
d	Diameter	Diameter of circular PCB	–	55	–	mm

WARNING

Hot surface! Contact can cause burns. Do not touch!

Some components can reach high temperatures >55°C when the board is powered on. Do not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

2 System Overview

Figure 2-1 and Figure 2-2 show photos of the system architecture, highlighting the key components of the FR4 four-layer PCB. The PCB comprises a LIN communication interface, a microcontroller (MCU), a gate driver for BLDC motors and a power supply. The ICs receive additional support from three half-bridge MOSFETs, one MOSFET for active reverse polarity protection, an EMI filter inductor, and a shunt resistor.

Careful consideration is given to component placement when designing this board. All active components are strategically positioned to distribute heat across the PCB surface while maintaining an efficient current path from and to the connector. Additionally, all essential components for the design are placed on the top side of the PCB, thereby maximizing space in alignment with the latest requirements in the pump, blower, and fan sector. The bottom side of the PCB is reserved for testing purposes and can be fully removed in a final product.

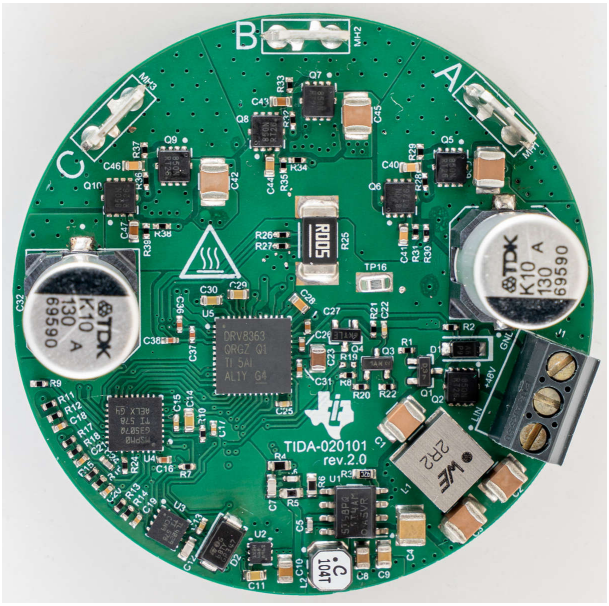


Figure 2-1. TIDA-020101 PCB Top View

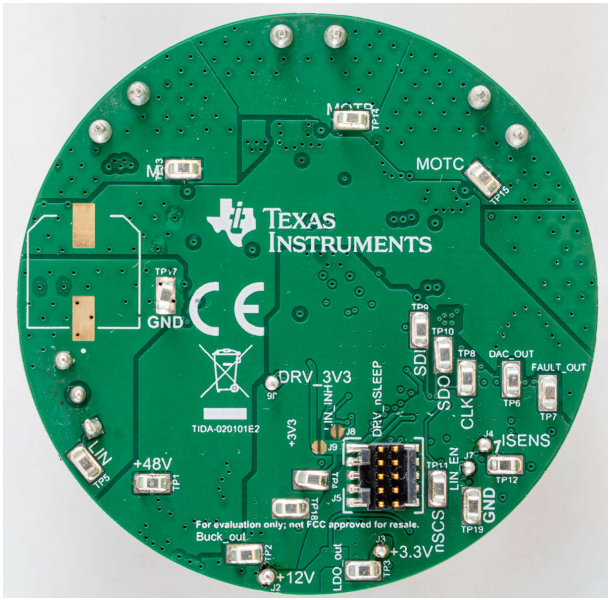


Figure 2-2. TIDA-020101 PCB Bottom View

2.1 Block Diagram

Figure 2-3 shows the TIDA-020101 block diagram.

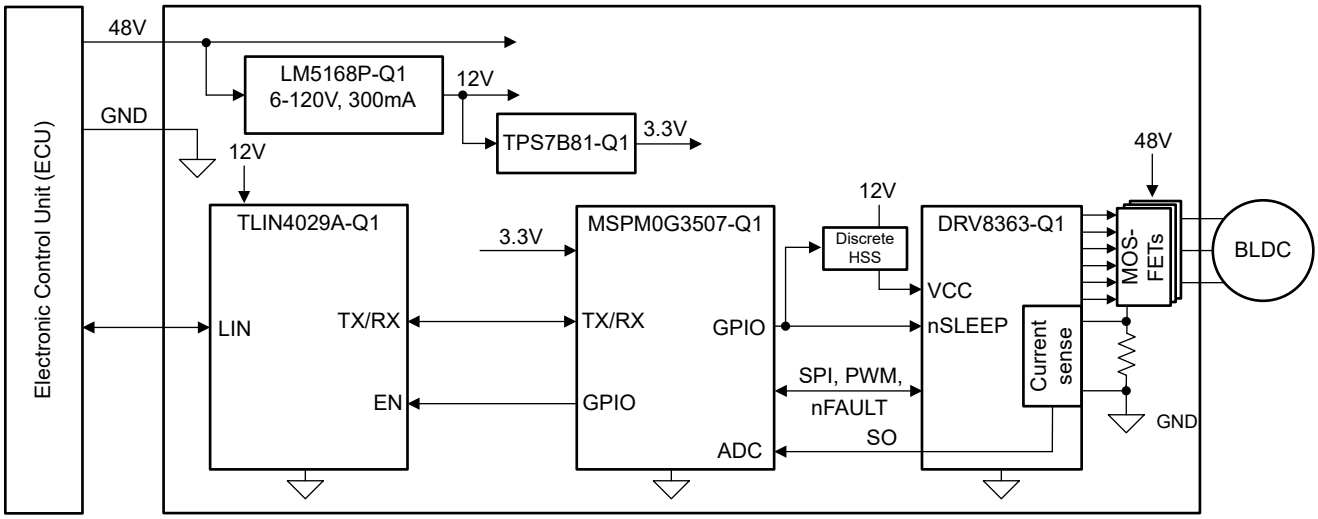


Figure 2-3. TIDA-020101 Block Diagram

2.2 Design Considerations

2.2.1 48V Smart Actuator Architectures

Modern automotive systems evolve toward higher voltage architectures to support increased electrification. Three primary architectures exist for implementing 48V smart actuator systems, each with distinct characteristics and trade-offs.

2.2.1.1 48V Distribution Architecture

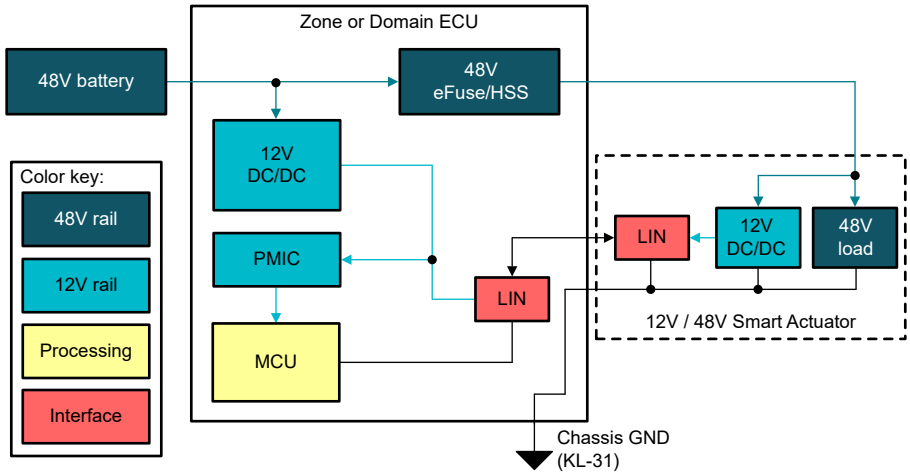


Figure 2-4. 48V Architecture

The 48V architecture, as shown in Figure 2-4, utilizes a simplified wiring approach with just two to three wires (48V, LIN, GND) connecting the zone or domain electronic control unit (ECU) to the smart actuator. The smart actuator contains power stages to generate required voltages for a communication interface, MCU, and motor driver. This approach requires minimal wiring complexity while providing sufficient power for actuator operation.

Key characteristics include:

- Simple wiring implementation
- DC-DC converter required within each smart actuator
- Potential system faults include shorts between 48V and LIN and loss of ground

2.2.1.2 48V and 12V Distribution Architecture

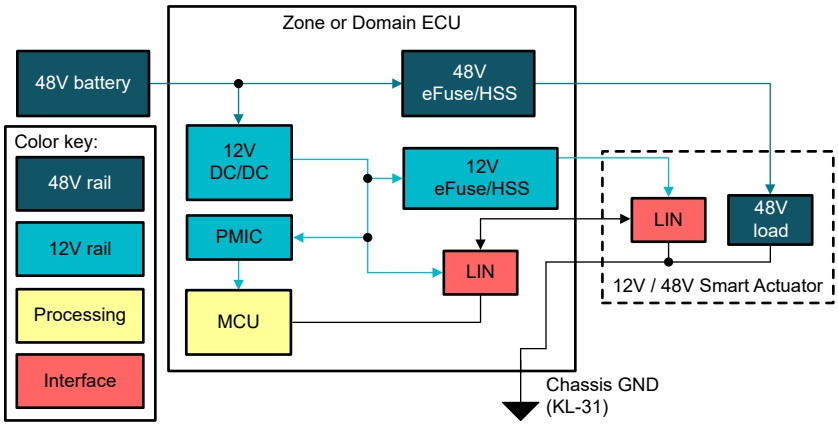


Figure 2-5. 48V and 12V Distribution Architecture

This intermediate approach distributes both 48V and 12V power to the smart actuators, requiring three to four wires (48V, 12V, LIN, GND) as shown in Figure 2-5. The upper ECU contains both 48V and 12V high-side switches, adding complexity to the power distribution system.

Key characteristics include:

- Moderate wiring complexity
- Potential for 48V LIN bus faults
- System faults include shorts between 48V and LIN, and shorts between 48V and 12V

2.2.1.3 48V and 12V Supplies Architecture

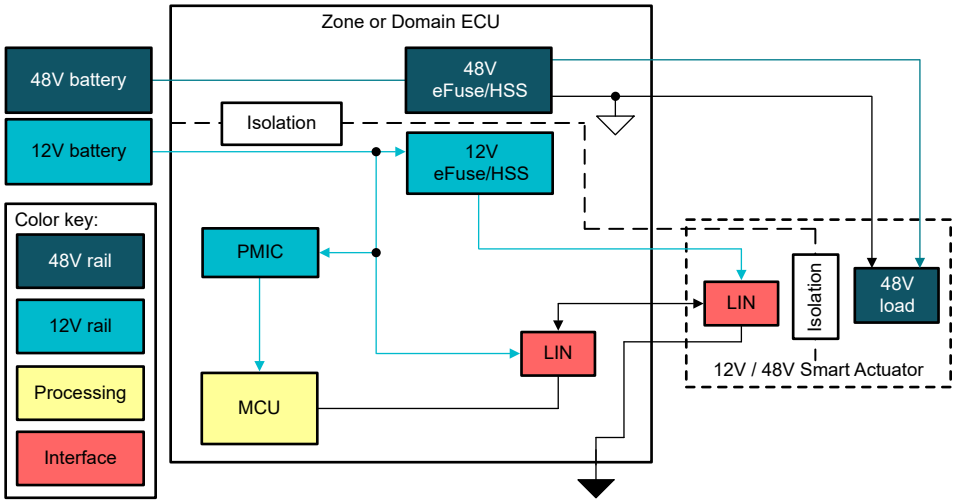


Figure 2-6. 48V and 12V Supplies Architecture

The most complex architecture is shown in Figure 2-6 and uses five wires (48V, 12V, LIN, GND_12V, GND_48V) with isolation between power domains. This approach provides the highest level of protection and fault tolerance for mixed voltage architectures.

Key characteristics include:

- Most complex wiring implementation
- Isolation components protect 48V to LIN or 12V
- Isolation eliminates ground loss concerns
- Requires additional isolation components, increasing system cost

2.2.1.4 Reference Design Architecture

For this reference design, the 48V distribution architecture is selected, as the approach represents the current market trend and delivers the most cost-efficient approach. This architecture balances system complexity, component count, and reliability while meeting performance requirements. The simplified wiring scheme reduces vehicle weight and manufacturing costs, while the integrated DC-DC converter in each smart actuator provides the necessary voltage conversion locally, improving overall system efficiency and reducing electromagnetic interference.

2.2.2 Low Power Sleep Mode Architecture

Many applications operate periodically or irregularly rather than continuously. Therefore, a low power mode is sometimes implemented to save power and thus increase the range of EVs. The two methods for implementing such a mode follow:

- High-side switch or eFuse implemented in the upper ECU to fully cut off the power supply to the edge in low power mode
- Continuously powered edge node with wake over LIN capabilities to enable sleep mode and remote wake over LIN

This reference design utilizes the remote wake over LIN approach because of the latest market trends. The approach enables a reliable way, independent from the upper ECU, to achieve sleep currents of less than 100µA.

Figure 2-7 graphically shows the system functional modes.

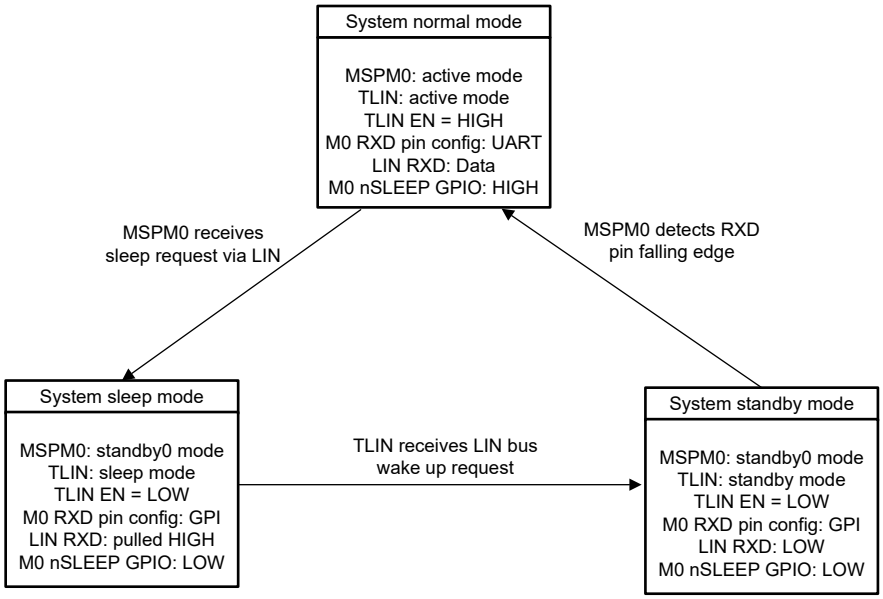


Figure 2-7. System Functional Modes

2.2.3 Bulk Capacitance Estimation

The high-frequency PWM signal used to drive the BLDC motor creates voltage fluctuations and alternating currents in the DC-link capacitors. In particular, for a PMSM that operates at near unity power factor, the maximum estimated current stress on these capacitors can be calculated with Equation 1.

$$I_{C,\,rms} \cong \frac{1}{\sqrt{2}} \times I_{OUT,\,rms} \tag{1}$$

Equation 2 describes the momentary value of the current.

$$I_{C,\,rms} = C_{bulk} \times \frac{dV}{dt} \tag{2}$$

With a maximum capacitor ripple voltage accepted of V_{ripple} = 1V at $I_{OUT,rms}$ = 6.25A, the required minimum capacitance is estimated using Equation 3.

$$C_{bulk} = I_{C,\,rms} \times \frac{dt}{dV} = I_{C,\,rms} \times \frac{1}{f_{PWM} \times dV} = \frac{1}{\sqrt{2}} \times I_{OUT,\,rms} \times \frac{1}{f_{PWM} \times dV} = \frac{1}{\sqrt{2}} \times 6.25A \times \frac{1}{20kHz \times 1V} = 221\mu F \tag{3}$$

This estimate serves as a useful baseline for lab validation to determine whether the ripple voltage of V_{ripple} = 1V can be achieved, or whether additional capacitance is needed. Based on this calculation, a bulk capacitance of C_{bulk} = 290µF has been provided, along with an additional footprint to accommodate a further 130µF if required.

2.2.4 EMI PI Filter

The onboard EMI input filter is designed to suppress low-frequency noise generated by PWM operation. This filtering circuit includes capacitors C1, C2, and C3, as well as a power inductor L1. Figure 2-8 shows the frequency response of this filter, which shows attenuation exceeding 30dB for frequencies above 150kHz.

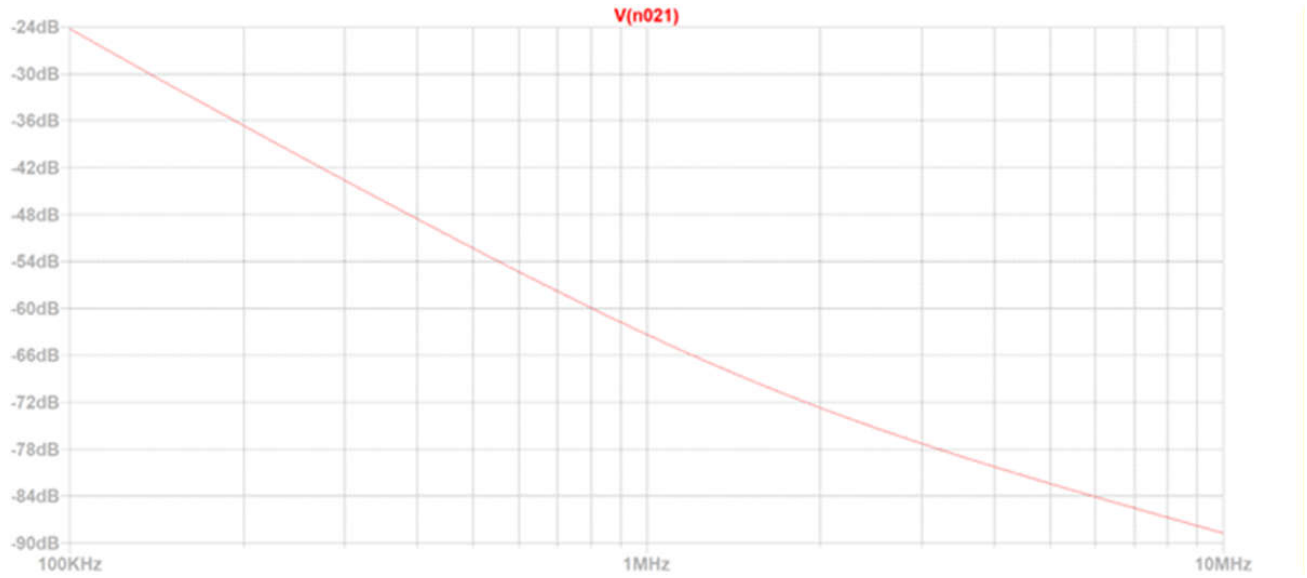


Figure 2-8. EMI PI Filter Frequency Response

2.2.5 Reverse Polarity Protection

Reverse polarity protection is implemented utilizing the DRV8363-Q1 integrated charge pump. With that approach, the system can support the required overdrive voltage for the NMOS gate without the need for additional external circuitry.

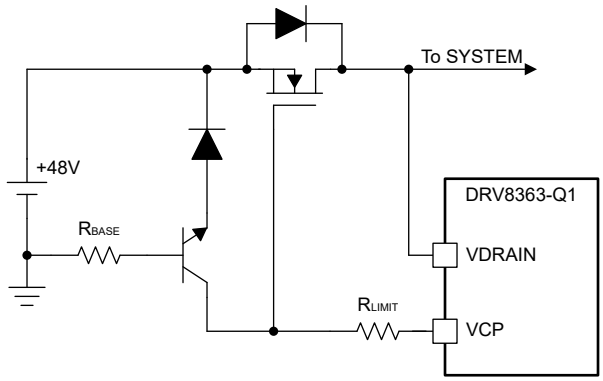


Figure 2-9. Reverse Polarity Protection Circuit

The body diode of the FET allows current to flow into the device initially, allowing the device to power on. When the device is powered on, the boost regulator output BOOST or the charge pump output VCP provides a voltage above the supply voltage which is high enough to turn on the reverse blocking FET, creating low $R_{DS(on)}$ to maximize efficiency of the reverse battery protection circuit. To minimize cost and simplify the bill of materials (BOM), the same power NMOS model used for the half bridges of the driver stage can be used as the reverse battery protection NMOS.

Detailed information is found in the *NMOS and BJT* chapter of the *Protecting automotive motor-drive systems from reverse polarity conditions* application report.

2.2.6 LIN Bus Fault Voltage for 48V Architecture

Contemporary automotive electrical standards for 48V systems establish comprehensive requirements for electrical and electronic components across 12V, 24V, and 48V supply voltages. Advanced specifications for alternator or generator-supplied systems mandate higher protection thresholds compared to DC-DC converter-supplied architectures, reflecting the demanding operational environment of modern automotive power systems.

State-of-the-art 48V automotive systems require LIN bus architectures capable of withstanding short-circuit conditions to V_{BAT} under maximum rating specifications of 70V, particularly when multiple conductors share common wire harness routing. This 70V fault voltage tolerance represents current industry-best practices for robust automotive communication networks.

Additionally, ground loss scenarios at edge nodes can cause LIN bus lines to float to battery potential, again reaching the 70V maximum threshold. This elevated fault voltage capability creates reliable operation under the most challenging automotive electrical fault conditions, establishing 70V tolerance as the benchmark for advanced 48V system designs.

2.3 Highlighted Products

This reference design closely replicates the form factor, dimensions, and capabilities of an actual end product, with each component thoughtfully chosen to deliver a compact, low quiescent current (IQ) smart motor solution. Central to the design is the integrated smart gate driver DRV8363-Q1, which drives 48V motors while offering advanced diagnostics and robust protection. Motor control is handled seamlessly by the MSPM0G-Q1 MCU series, which runs a sensorless field-oriented control (FOC) algorithm and takes full advantage of the DRV8363-Q1's built-in current sense amplifiers. The TLIN4029A-Q1 — TI's ±70V bus fault voltage LIN transceiver — delivers a reliable, cost-effective communication interface within a 48V architecture. Complementing the low-power capabilities of these key components, a low IQ power tree built around the LM5168P-Q1 and TPS7B81-Q1 enables a holistic system design that meets the latest market demands.

2.3.1 TLIN4029A-Q1

This reference design makes use of a ±70V bus fault voltage LIN transceiver to support 48V smart motors with headroom.

If a lower bus fault voltage of ±60V is acceptable, the pin-compatible TLIN2021A-Q1 can be used instead. The device features additional integrated wake and INH capabilities, thus removing the need for an external LDO to generate 3.3V. Rather than using an external 3.3V LDO, the LDO integrated in the DRV8363-Q1 can be used to reduce cost.

2.3.2 MSPM0G3507-Q1

The 80MHz MSPM0G3507-Q1 MCU enables use of an integrated math accelerator to achieve sensorless FOC control loop rates of up to 10kHz while maintaining an PWM output frequency of 20kHz. In case a lower FOC control loop rate is sufficient, MSPM0G3106-Q1 can be used to optimize cost. For more details about how to select the correct MSPM0 MCU for smart actuators, refer to Automotive Smart Actuators.

2.3.3 DRV8363-Q1

The DRV8363-Q1 is an integrated smart gate driver purpose-built for 48V automotive three-phase BLDC applications, making the device a practical choice for this 300W HVAC pump, blower, and fan design. The device provides three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs, and generates the correct gate drive voltages using an external 12V supply with an integrated bootstrap diode for the high-side MOSFETs. A key advantage of the DRV8363-Q1 for this application is the integrated three-channel low-side current sense amplifiers (CSA) and VDS monitoring across all six switches, enabling precise FOC current sensing and robust overcurrent protection without any additional external circuitry. Implementing either of these functions discretely can add significant BOM cost, board area, and design complexity — incompatible with the compact 55mm form factor of this design. This is further complemented by a comprehensive suite of advanced diagnostics and configurable fault protection, enabling a robust motor drive system with minimal external support components. The smart gate drive architecture supports configurable peak gate drive current from 16mA up to 1A source and 2A sink — well-matched to the 300W peak power level — and operates over a wide 8V to 85V input range, comfortably covering the full 48V battery operating window including transients. An integrated trickle charge pump supports 100% PWM duty cycle control. The integrated charge pump output (VCP) is additionally leveraged for active reverse polarity protection, and a P-channel MOSFET can be used to fully disconnect the 12V supply during sleep mode, contributing to the sub-100µA system sleep current. The highly configurable serial peripheral interface (SPI) enables seamless integration with the MSPM0G3507-Q1 MCU, making the DRV8363-Q1 a practical gate driver design for this compact, cost-efficient, and robust 48V smart motor reference design.

2.3.4 LM5168P-Q1

The LM5168P-Q1 synchronous buck converter regulates over a wide input voltage range, minimizing the need for external surge suppression components. A minimum controllable on-time of 50ns facilitates large step-down conversion ratios, enabling the direct step-down from a 48V nominal input to low-voltage rails for reduced system complexity and cost. With integrated high-side and low-side power MOSFETs, the LM5168P-Q1 delivers up to 0.3A of output current. A constant on-time (COT) control architecture provides nearly constant switching frequency with excellent load and line transient response. The LM5168P-Q1 uses auto mode which enables ultra-low I_Q and diode emulation mode operation for high light-load efficiency which is essential to achieve a system requirement of less than 100µA current in system sleep mode.

2.3.5 TPS7B81-Q1

In automotive battery-connected applications, low quiescent current (I_Q) is important to conserve energy and to extend battery lifetime. Always-on systems must have ultra-low I_Q over an extended temperature range to enable sustained operation when the system is in sleep mode. The TPS7B81-Q1 is a low-dropout (LDO) linear regulator with only a 2.7µA typical quiescent current at light load. Thus, the device is an efficient design for powering microcontrollers and transceivers in standby systems.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

This reference design demonstrates proof-of-concept functionality and showcases the exceptional miniaturization capabilities of TI portfolio components within highly constrained form factors. The current implementation prioritizes spatial optimization and functional validation. The design illustrates how TI's advanced semiconductor technologies integrate into compact PCB geometries while maintaining essential performance characteristics. Future design iterations will incorporate comprehensive electromagnetic interference (EMI) optimization strategies and enhanced creepage and clearance considerations to meet stringent automotive compliance standards. This approach allows engineers to first validate the core functionality and feasibility before advancing to full production-ready implementations with complete regulatory compliance.

3.1.1 Reference Design Hardware and Programming Setup

A programming header (J5) is located on the bottom side of the reference design. The header serves as an interface point for connecting an XDS110 programmer. Figure 3-1 shows the recommended setup.

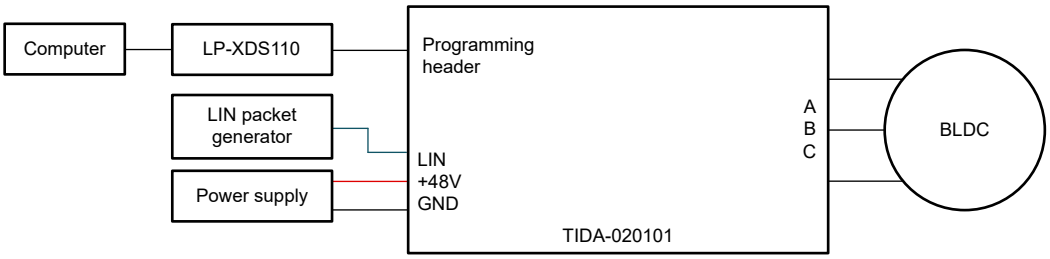


Figure 3-1. Hardware Setup

Use the following links to obtain tools needed for setup:

- XDS110 LaunchPad™ development kit debugger
- Samtec programming cable: FFSD-05-D-06.00-01-N

3.2 Software

The comprehensive software package for this reference design downloads within the reference design folder. The package provides engineers with immediate access to a proven implementation framework. The software represents an adaptation of the sensorless field-oriented control (FOC) algorithm derived within the M0 SDK. The algorithm receives reconfiguration specifically for this hardware.

To facilitate seamless integration and performance enhancement, engineers can leverage the *MSPM0 Sensorless FOC Tuning* user's guide. The guide provides detailed guidance for algorithm adjustment and parameter tuning. This combination of readily accessible software and comprehensive tuning documentation enables rapid development cycles. This combination maintains motor control performance across diverse operating conditions.

The software specifications are listed in Table 3-1.

Table 3-1. TIDA-020101 Sensorless FOC Software Specifications

PARAMETER	VALUE
Filename	sensorless-foc_TIDA020101_nortos_ticlang
Flash size used	40kb, 128kb (32%)
SRAM size used	1.2kb, 32kb (4%)

3.3 Test Setup

This design is tested with a Teknic® M-2310P-LN-04K three-phase BLDC motor. Table 3-2 displays brief specifications for this motor.

Table 3-2. Teknic® M-2310P-LN-04K Three-Phase BLDC Motor Specifications

PARAMETER	VALUE	UNIT
Motor part number	M-2310P-LN-04K	–
Phase-to-phase resistance	720	mΩ
Phase-to-phase inductance	400	µH
Back EMF constant	4.64	V_{peak}/k_{RPM}
Back EMF constant	348	mV/Hz × 10
Number of pole pairs	4	–
Maximum motor speed	400	Hz

To provide a load for the motor, a second motor of the same type connects through a shaft coupler and aluminum frame mount to the design under test (DUT). The phases of the load motor are shorted through adjustable load resistors to load the DUT motor.

CAUTION

Several items require attention related to this test setup:

1. The motor rotates at high speeds and has sufficient torque to cause damage or injury. Take care to keep clothing, tools, and other items away from the rotating shaft during testing.
2. Supply voltages above 50V present a shock hazard. Use caution when setting the 48V supply to higher than nominal values.
3. A solid connection between both motors remains important for safe operation and for accurate measurement of the motor performance. Misalignment can lead to damage of the coupling or incorrect test results.
4. Rapid changes of the motor speed can lead to overvoltage generated by the motor. Be aware that the generated voltage can exceed the voltage set-point of the 48V supply.

Table 3-3 summarizes the tests performed with this reference design.

Table 3-3. List of Performed Tests

TEST NAME	PASS CRITERIA
LIN Remote Wake-Up Timing Analysis	$t_{wakeup} \leq 10ms$ (4)
System Sleep Current Analysis	$I_{sleep} \leq 100\mu A$ (5)
DC Link Voltage Ripple	$V_{ripple} \leq 1V$ (6)
Thermal Images	–

3.4 Test Results

Table 3-4 summarizes the tests performed with this reference design.

Table 3-4. List of Test Results

TEST NAME	TEST RESULTS
LIN Remote Wake-Up Timing Analysis	$t_{wakeup} = 148\mu s$ (7)
System Sleep Current Analysis	$I_{sleep} = 81\mu A$ (8)

Table 3-4. List of Test Results (continued)

TEST NAME	TEST RESULTS
DC Link Voltage Ripple	$V_{ripple} = 26.5mV$ (9)
Thermal Images	Available

3.4.1 LIN Remote Wake-Up Timing Analysis

The LIN remote wake-up timing analysis evaluates the timing characteristics and response parameters when a LIN network node transitions from sleep mode to active operation. The transition occurs upon receiving a wake-up signal through the LIN bus. This analysis confirms that wake-up sequences meet specified timing requirements for reliable system activation. The analysis includes signal propagation delays and node response times.

3.4.1.1 Test Setup

In the following oscilloscope plots, the input to the LIN transceiver (U3) is driven by an external source connected to TLIN2029EVM. Software puts the system into system sleep mode (MSPM0 in STANDBY0), according to the Low Power Sleep Mode section. The software outputs a LOW signal on PA16 (TP7) whenever the MCU is in sleep mode. When the MCU is in active mode, PA16 (TP7) is driven HIGH.

Test conditions:

- Software used: TIDA-020101_sleep_mode_current_test
- Power supply: +48V and GND supplied to J1
- Ambient air temperature: 25°C

Wake up procedure:

- To wake up TIDA-020101 using LIN, the external connected TLIN2029EVM outputs a wakeup signal. This is a dominant pulse lasting 250µs.

Pass criteria:

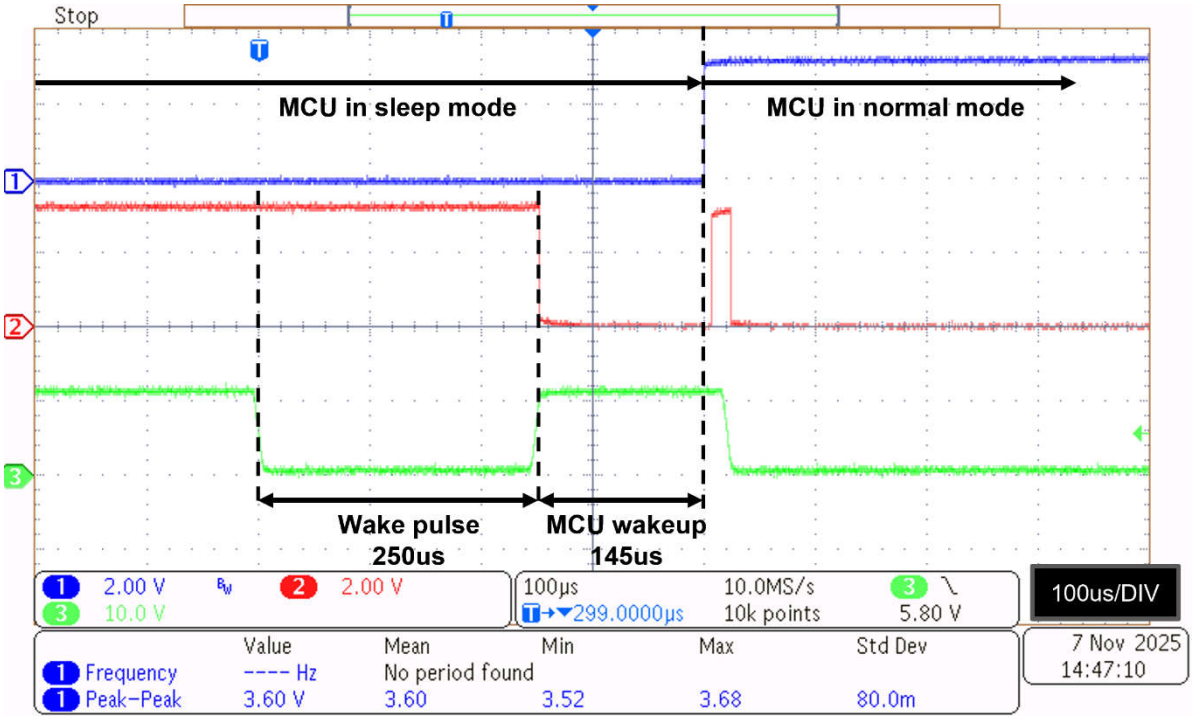
- The MCU of TIDA-020101 must be in normal mode again not later than 10ms after the rising edge of the LIN bus.

Oscilloscope plots signals:

- CH1: MCU_normal_mode (TP7)
- CH2: LIN_RXD (R7)
- CH3: LIN (TP5)

3.4.1.2 Test Results

Figure 3-2 shows the oscilloscope plots of the LIN remote wake-up timing analysis.



CH1: MCU_normal_mode (TP7) blue
CH2: LIN_RXD (R7) red
CH3: LIN (TP5) light green
t_{wakeup} = 148µs → Test PASSED

Figure 3-2. LIN Remote Wake-Up Timing Analysis Oscilloscope Plots

3.4.2 System Sleep Current Analysis

A low-power mode, detailed in Section 2.2.2, is integrated to decrease power consumption when the system remains idle. This analysis evaluates the low power capabilities of the design.

3.4.2.1 Test Setup

A TIDA-020101 DUT PCB is supplied with 48V and GND through J1. The supply current is monitored using a 8½ digit multimeter. A test software is flashed onto the MCU which drives PA3 LOW to disable the DRV8363 using a discrete high-side switch and further put TLIN4029A-Q1 into sleep mode. The MSPM0 internal pullup on PA17 is disabled. The MSPM0 is put into STANDBY0 mode. The sleep current is measured in that state.

Test conditions:

- Software used: TIDA-020101_sleep_mode_current_test
- Power supply: +48V and GND supplied to J1
- Ambient air temperature: 25°C

Pass criteria:

- The test is passed under the following condition: I_{sleep} < 100µA

3.4.2.2 Test Results

The sleep current reading is taken from the 8½ digit multimeter.

- I_{sleep} = 81µA → Test PASSED

3.4.3 DC Link Voltage Ripple

The PCBs DC link capacitance, as estimated in Section 2.2.3, is evaluated in this analysis.

3.4.3.1 Test Setup

A TIDA-020101 DUT PCB is supplied with 48V and GND through J1. Using the test setup, specified in Section 3.3 without a load motor connected and the software, specified in Section 3.2, the motor is spinning at 400Hz electrical frequency. To measure the DC link voltage ripple, an oscilloscope is used to probe the voltage across C35.

Test conditions:

- Software used: TIDA-020101_sleep_mode_current_test
- Power supply: +48V and GND supplied to J1
- Ambient air temperature: 25°C
- No mechanical load

Pass criteria:

- The test is passed under the following condition:

$$V_{ripple} \leq 1V \quad (10)$$

Oscilloscope plots signals:

- CH1: DC bus voltage (C35)
- CH1: PHASE A (TP13)

3.4.3.2 Test Results

Figure 3-3 shows the oscilloscope plots of the DC link voltage ripple test.

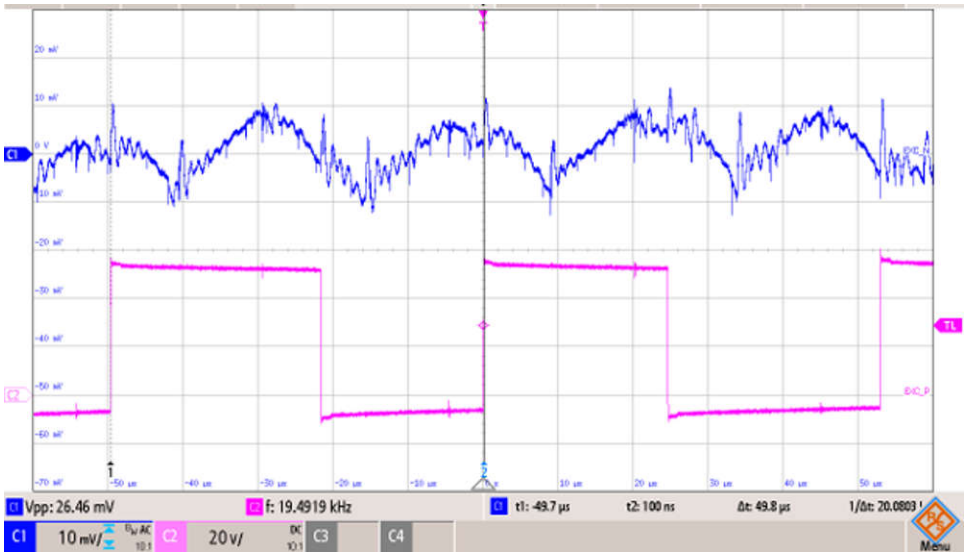


Figure 3-3. DC link voltage ripple

$$V_{ripple} = 26.5mV \rightarrow \text{Test PASSED} \quad (11)$$

3.4.4 Thermal Images

In Figure 3-4, the surface temperature of the various components is visible. The ambient temperature was room temperature. The layer stack below is used. More details about the layer stack can be found in the design files.

- Top copper layer: 2oz
- Inner copper layer 1: 1oz
- Inner copper layer 2: 1oz
- Bottom layer: 2oz

All thermal images were taken under the following test conditions:

- Software used: sensorless-foc_TIDA020101_nortos_ticlang
- V_{bus}: 48V
- Electrical input power: 300W RMS
- Ambient air temperature: 25°C
- Mechanical speed: 6000RPM
- Thermal Camera: TESTO 883

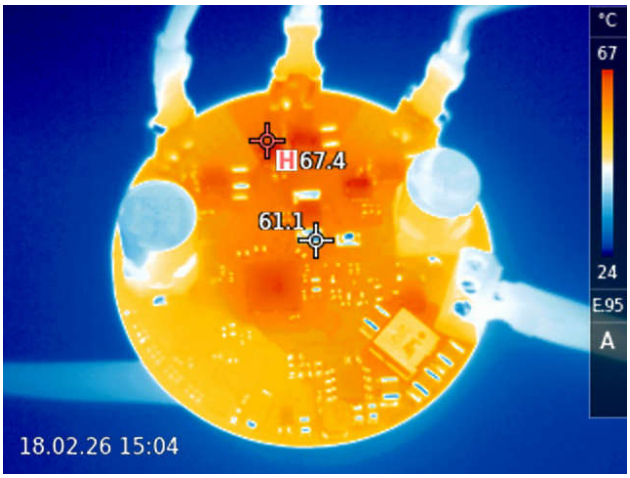


Figure 3-4. TIDA-020101 Thermal Images

4 Design and Documentation Support

4.1 Design Files

To access all available design files, see TIDA-020101.

4.1.1 Schematics

To download the schematics, see the design files at TIDA-020101.

Figure 4-1 shows the TIDA-020101 48V BLDC pump, blower, engine, and fan schematic.

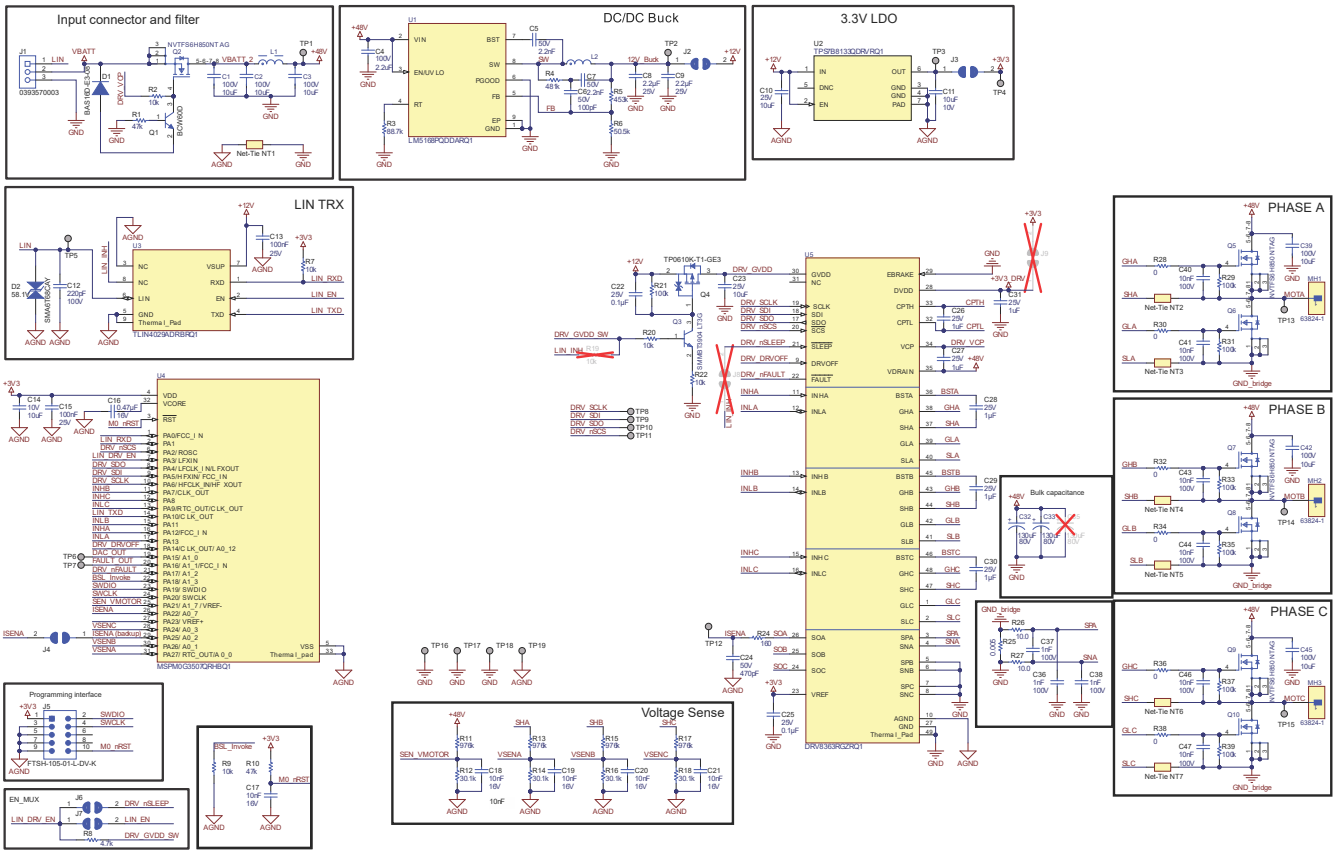


Figure 4-1. TIDA-020101 Schematic

4.1.2 BOM

To download the BOM, see the design files at TIDA-020101.

4.1.3 PCB Layout Recommendations

Follow the *TI Shunt Resistor Layout Considerations*.

4.1.3.1 Layout Prints

To download the layer prints, see the design files at TIDA-020101.

4.1.3.2 Gerber Files

To download the Gerber files, see the design files at TIDA-020101.

4.2 Tools and Software

Tools

CCSTUDIO-THEIA	Code Composer Studio™ Theia v1.x.
MSPM0 Sensorless FOC Tuning User's Guide	This tuning user's guide provides step-by-step guidance to set up an MSPM0 MCU and supported DRV hardware board to tune a 3-phase brushless DC motor.
2MTR-DYNO	2MTR-DYNO InstaSPIN-FOC™ Evaluation Module
LP-XDS110	XDS110 LaunchPad™ development kit debugger
FFSD-05-D-06.00-01-N	Samtec™ programming cable

Software

MSPM0-SDK	MSPM0 software development kit (SDK)

4.3 Documentation Support

1. Texas Instruments, *Automotive Smart Actuator Application Brief*
2. Texas Instruments, *TLIN4029A-Q1 Automotive LIN Transceiver with Dominant State Timeout and Extended Fault Protection Datasheet*
3. Texas Instruments, *DRV8363-Q1 48V Battery Three-Phase Smart Gate Driver with Accurate Current Sensing and Advanced Monitoring Datasheet*
4. Texas Instruments, *MSPM0G350x-Q1 Automotive Mixed-Signal Microcontrollers With CAN-FD Interface Datasheet*
5. Texas Instruments, MSPM0 Sensorless FOC Tuning User's Guide

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

FABIAN BARTH is a highly-skilled systems engineer contributing to the automotive body Systems Engineering Team at Texas Instruments. In this role, he plays a pivotal part in the development of cutting-edge reference designs within the automotive sector. With a wealth of expertise in areas such as smart motors, remote controlled edge node, single-pair Ethernet, Power over Data Lines, and hardware time synchronization, Fabian brings a depth of knowledge and experience to his responsibilities.

He holds a Master of Engineering degree in Electrical Engineering from the Landshut University of Applied Science in Germany, reflecting his commitment to academic excellence and proficiency in his field.

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