

Implementing RapidIO

Travis Scheckel and Sandeep Kumar

Communications Infrastructure Group, Texas Instruments

In today's telecommunications market, slow and proprietary is not the direction for success. Case in point: the bus interfaces that allow devices and subsystems to communicate with one another. When proprietary approaches are used, these interfaces become increasingly inefficient as they strive to keep pace with growing bandwidth demands.

A smarter alternative is RapidIO, an open, standards-based interconnection technology for chip- and board-level communications in medium- and large-size embedded systems. This technology enables high-speed, packet-switched, peer-to-peer connectivity between ASICs, DSPs, FPGAs, microprocessors, network processors and backplanes.

Unlike technologies borrowed from the computing and IT worlds, such as PCI Express, RapidIO was designed from the ground up for embedded infrastructure applications. (For more examples of how PCI Express compares to RapidIO, see the white paper, *RapidIO Technology and PCI Express - A Comparison*, at www.rapidio.org.) It supports device-level, peer-to-peer communications, which is a must-have in embedded applications because multiple devices routinely work together to perform functions. RapidIO also scales up to 64,000 devices – more than enough to meet the demands of today's and tomorrow's telecommunications infrastructure.

RapidIO is particularly attractive because it supports serial connections, which OEMs prefer as a way to reduce cost and increase system bandwidth. RapidIO also cuts costs through its ability to work with standard, off-the-shelf I/O technology and adjunct equipment. These savings add up, and they help OEMs compete in today's price-sensitive markets.

Fast, Open and Reliable

RapidIO's other key benefits include:

- **A global, industry-wide ecosystem** – Industry leaders such as Texas Instruments have integrated RapidIO into DSPs, FPGAs and network processors. (An updated membership list for the RapidIO Trade Association is available at www.rapidio.org/about/list.) The technology also is backed by many major manufacturers, including Alcatel, Ericsson, Lucent Technologies and

Motorola. This broad support ensures that RapidIO won't languish as a niche play. Instead, it's already emerging as the technology of choice.

- **QoS** – RapidIO features quality-of-service (QoS) mechanisms, including the ability to detect and manage errors in hardware, without software intervention. That's attractive to telecommunications OEMs and their carrier customers because QoS is a smarter market differentiator than price. For designers, RapidIO's QoS mechanisms mean that faster or bigger links no longer are the only options for ensuring performance levels.
- **Reduced protocol overhead** – RapidIO is designed from the ground up for embedded systems requiring low transaction overhead.
- **Serial and parallel support** – RapidIO includes a parallel interface for system connectivity and a serial interface for applications such as backplanes.
- **Flexibility** – RapidIO is transparent to operating systems and application software. For designers, this approach saves time and money because they don't have to re-engineer an existing OS or software to reap RapidIO benefits. It's also not locked into a single topology: RapidIO supports the mesh and star architectures commonly used in embedded infrastructure applications. With additional support for daisy-chain and dual-star topologies, RapidIO gives designers maximum flexibility, including the ability to use redundant links to ensure reliability. Finally, Rapid IO's link rate and width are variable, with support for parallel and serial connections.
- **Interoperability** – RapidIO includes bridging functions so it can work with other bus technologies, such as PCI and PCI Express, and with system-area networks such as InfiniBand. This flexibility acknowledges that other technologies have their place. Indeed, PCI-Express-to-RapidIO bridge devices are one likely example of how the two technologies can complement each other. Finally, RapidIO also supports encapsulation, so protocols such as Ethernet can be transported across a RapidIO network.
- **High throughput** – RapidIO busts bottlenecks by letting embedded devices communicate at speeds up to 60 Gbps. That's far faster than bus technologies such as PCI, which have transfer rates in the range of hundreds of megabits. Interconnection speeds can be more effective than faster processors in terms of improving overall system performance. RapidIO also defines congestion-control mechanisms for high-utilization switch fabrics.
- **Reliability** – RapidIO's peer-to-peer architecture is inherently robust because the system never is at the mercy of a single device. By putting error management in hardware, RapidIO improves error handling, with additional flexibility via extensions for housekeeping by software. In the case of catastrophic errors, such as a device failure, RapidIO can redirect data.

Dissecting RapidIO

Switches are at the heart of RapidIO-based embedded systems, passing packets between end points. The switches use information in the packet header, but they don't alter the three layer RapidIO packet header fields, with the exception of the Serial Physical layer *ackid* field, which is updated sequentially for each packet between link

partners. This allows the CRC to remain unchanged as the packet moves through the fabric from source to destination. The three layers of RapidIO include:

- **Logical** – defines the formats of the protocols and packets
- **Transport** – information needed to route packets from one end point to another
- **Physical** – covers attributes such as flow control, low-level error management and packet-transport mechanisms.

A key benefit of this hierarchical design is that more transaction types can be added to the logical specs without requiring changes to the physical or transport layer specs. RapidIO is flexible in another way: The switch fabric passes the packets rather than interpreting them, so it can easily accommodate future changes, such as protocol extensions.

Like any technology, RapidIO consists of multiple specifications. (More information about many of these specs is available at www.rapidio.org/specs, but some require membership in the RapidIO Trade Association.) Here's an overview of the current specs:

- **I/O Logical, Messaging, Transport and Parallel Physical Layer** – Released in June 2002, these four specs define protocol and packet formats, transaction types, addressing procedures, transport mechanisms and flow control.
- **GSM** – An optional feature, this spec covers the global shared memory (GSM) logic layer, which provides directory-based coherent memory. Released in June 2002, GSM lets a single protocol span distributed I/O processing and general, multipurpose processing.
- **Serial Physical Layer** – Released in June 2002, this spec covers the physical layer header, 8B/10B coding, symbol generation, buffer management, lane striping and the characteristics for the driver and receiver. The spec provides a full-duplex, serial link and includes the ability to gang together four serial links to boost throughput in high-performance applications.
- **Interoperability** – Released in June 2002, this spec provides the interoperability requirements for RapidIO devices and for RapidIO-to-PCI devices. A separate spec, released in November 2002, covers the electrical and mechanical features that affect hardware interoperability in serial and parallel RapidIO links.

RapidIO also includes several extensions as part of the RapidFabric initiative, which began in June 2003 and expands the technology's support for a wide range of data-plane applications. This initiative is another example of how RapidIO is designed to adapt to meet the needs of networks as they evolve.

Extensions released or currently under development will cover applications in wired and wireless networks, including multiprotocol switches, edge routers, DSLAMs and IP service switches. This diversity is important because it helps expand the RapidIO

ecosystem beyond a single industry or a small set of applications. (More information about the extensions is available at www.rapidio.org/about/RapidFabric.)

The current RapidIO extensions are:

- **Error Management** – Added in September 2002, these extensions cover the way that error conditions are reported to host devices. They also provide the register definitions used to collect information about a device's state.
- **Flow Control** – These extensions give designers a way to control congestion in complex, medium-rate data-plane applications. Released in September 2003, the extensions complement RapidIO's link-based flow-control features.
- **Data Streaming Logical Methods** – This spec was released in August 2004 and covers techniques for protocol-independent encapsulation of payloads up to 64 kilobytes.
- **Multicast** – Released in August 2004, these extensions define switch-based multicasting for packets.

Balance the Present and Future

RapidIO already enjoys wide vendor support, with parallel and serial products now available, so there's ample equipment for designers to choose from. For example, Tektronix added a RapidIO support package to its TLA family of logic analyzers more than three years ago. Paired with an oscilloscope, the logic analyzer lets designers perform RapidIO test and debug tasks, such as viewing and characterizing jitter and predicting bit error rate.

Although RapidIO is a major advance in terms of speed and flexibility, implementing it on existing backplanes doesn't require a major upheaval, such as significantly modifying hardware and software.

One example is the serial spec, which was created to complement the existing parallel spec. As a result, designers with a portfolio of parallel RapidIO products can quickly and easily port them to a serial environment to produce a new line of semiconductors and ASICs. RapidIO also respects current technology by, for example, working with .13- and .25-micron CMOS systems.

The bottom line is that although it's a major advance in terms of performance, QoS, reliability and flexibility, RapidIO bridges the present and the future, giving wireless designers tomorrow's tools today.

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