

Lifetime Estimates and Unique Failure Mechanisms of the Digital Micromirror Device (DMD)

M.R. Douglass
 Texas Instruments, Digital Imaging
 Post Office Box 869305, MS 8477
 Plano, Texas 75086

972-575-6774; fax: 972-575-0457; e-mail: m-douglass@ti.com

ABSTRACT

The Digital Micromirror Device™ (DMD™) has made great strides in both performance and reliability. Each device consists of more than 500,000 individually addressable micromirrors. Digital Light Processing™ technology, based on the DMD, has been used in such diverse products as projection displays with film-like projected images and photographic-quality printers. Reliability testing of the DMD has demonstrated greater than 100,000 operating hours and more than 1 trillion mirror cycles.

This paper discusses DMD reliability development activities; failure modes investigated (e.g., hinge fatigue, hinge memory, stuck mirrors, and environmental robustness); various acceleration techniques (e.g., temperature and duty cycle); corrective actions implemented; and the resulting evidence that the DMD is exceeding original reliability goals.

INTRODUCTION

The use of a DMD to digitize light is referred to as Digital Light Processing™ or DLP™. A DLP subsystem consists of a light source, optics, color filters, digital processing and formatting, a DMD, and a projection lens, as shown in Figure 1. References [1] and [2] describe DLP in more detail and give additional examples.

The DMD is an array of aluminum micromirrors monolithically fabricated over an array of SRAM cells. Each SRAM cell corresponds to a micromirror and allows each mirror to be individually addressed so as to rotate ± 10 degrees, limited by a mechanical stop. The micromirror superstructure is fabricated through a series of aluminum

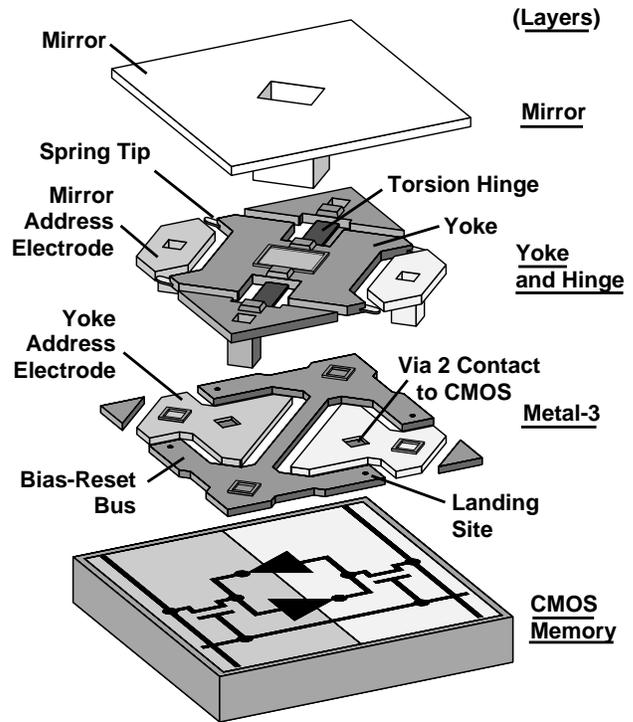


Figure 2. Exploded view of a DMD pixel

metal depositions, oxide masks, metal etches, and organic spacers. The organic spacers are subsequently ashed away to leave the micromirror structure free to move. Reference [1] discusses this process in more detail. Figure 2 shows an exploded view of a micromirror.

The mirror is rotated as a result of electrostatic attraction between the mirror structure and the underlying memory cell. The mirror and yoke are connected to a bias/reset voltage. The address electrodes are connected to the underlying CMOS memory through via contacts. Movement of the mirror is accomplished by storing a 1 or a 0 in the memory cell (one address electrode at ground and the other address electrode at V_{DD}) and applying a bias voltage to the mirror/yoke structure. When this occurs, the mirror is attracted to the side with the largest electrostatic field differential, as shown in Figure 3. To release the mirror, a short reset pulse is applied to the mirror that excites the resonant mode of the structure and the bias voltage is removed. The combination of these two occurrences results in the mirror leaving the landing site. The mirror lands again when the bias voltage is reapplied [2]. Mirror control during this transition is a critical aspect of device reliability and is discussed in subsequent sections of this paper.

Each micromirror is 16 μm square. The array places each micromirror on a 17 μm pitch, leaving a gap of less than 1 μm between

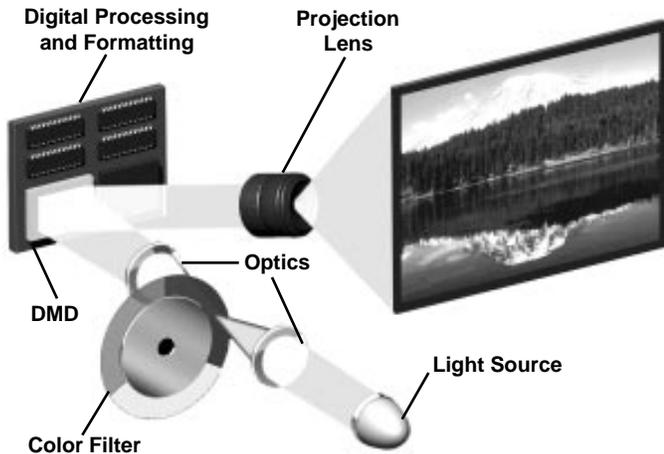


Figure 1. An example of a DLP projection system using a single DMD

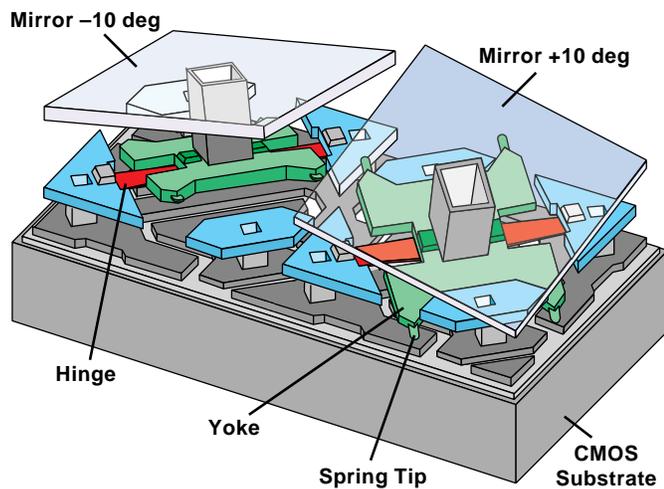


Figure 3. Two DMD pixels

the micromirrors. This results in a >90% fill factor and is one significant advantage of the DMD. The configuration of the array is flexible, depending on the application. DMD array sizes have been produced in the following configurations: 840×1 (first production DMD used for low-resolution printing), 640×480 (VGA resolution), 848×600 (SVGA resolution), 1024×768 (XGA resolution), and 1280×1024 (SXGA resolution), as well as demonstrations of other array sizes, such as, 7056×64 (high-resolution printing) and 2048×1024 (HDTV demonstration for a DARPA contract). Figure 4 is a photograph of a small portion of an array.

DMD RELIABILITY DEVELOPMENT

Reliability development activities started in early 1992. We began with a detailed failure modes and effects analysis (FMEA) so that we could brainstorm potential failure modes and mechanisms. We then wrote a test plan to verify these failures as well as to highlight any unanticipated failure modes. We used Texas Instruments standard semiconductor qualification test requirements as our baseline, including applicable tests such as storage life, temperature cycling, thermal shock, moisture resistance, vibration, wire bond strength, and die shear. The standard test requirements adequately covered package and die integrity concerns but did not specifically address microelectromechanical systems (MEMS) concerns associated with a three-dimensional, moving integrated circuit.

To address the MEMS aspects of the DMD, the test plan focused on such obvious potential failure mechanisms as:

- Hinges breaking (fatiguing) over time as a result of routine operation
- Mirrors breaking as a result of handling (vibration/shock)
- Device lifetime limitations caused by high operating temperatures
- Device lifetime limitations due to intense light exposure.

We designed a series of tests to address each of these concerns as well as to try to simulate how a DMD would be used in actual applications. As our reliability development program progressed, we identified several acceleration techniques that allowed us to highlight subtle failure modes and, in turn, implement design improvements much more rapidly.

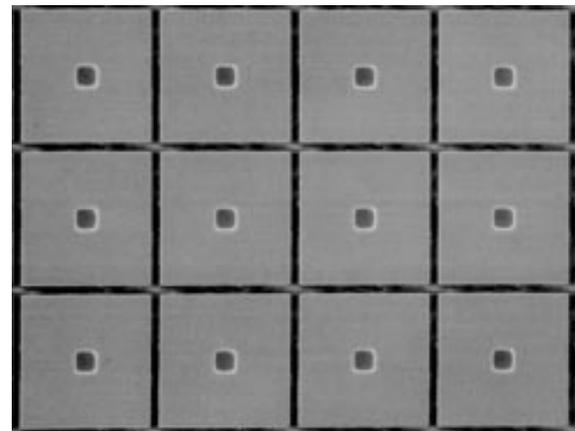


Figure 4. Top surface of micromirror array

As the tests progressed, we soon realized that a DMD is more than a MEMS device. A DMD has unique optical requirements as well as chemical properties that offer challenges we did not consider. In other words, the DMD is a microsystem with mechanical-electrical-optical-chemical properties that all need to be jointly optimized [3,4].

References [5] and [6] summarize some of the early test results and potential failure modes. These failure modes and others are discussed in more detail in the next section.

UNIQUE FAILURE MECHANISMS INVESTIGATED

Hinge Fatigue

Hinge fatigue was certainly one of the most significant concerns. Simple calculations (a mirror switching once every 200 microseconds for 5 years at 1000 operating hours per year) showed that each mirror element needed to rotate, or switch, more than 90×10^9 times to ensure a reliable product. Initial finite element analyses using bulk properties of aluminum highlighted this as a potential concern. A life test was designed to accelerate the number of mirror cycles per second by a factor of 10. The test accomplished this by switching the mirrors more rapidly (once every 20 microseconds) than would occur during actual operation (a time-based average of 200 to 300 microseconds). On a small sample, we rapidly exceeded 100×10^9 with no hinge fatigue failures. We increased the sample size and the results were similarly successful. Several devices also remained on test for more than 10^{12} cycles with no evidence of hinge fatigue.

More recently, we repeated this test on DMDs sampled from the production flow. Four devices (three with zero defects and one with one nonfunctional mirror at the start) have been on test for nearly 19,000 hours. Each device has exceeded 1.7×10^{12} cycles with no evidence of hinge fatigue. One device has one added defect. After 1.7×10^{12} cycles, all functional mirrors were still functional except for the one added defect, which does not appear to be due to fatigue. Because each DMD in this test has 307,200 functional mirrors (640×480) and each mirror switched more than 1.7×10^{12} times, the test has demonstrated more than 2×10^{18} total micromirror movements with only one added micromirror defect and no device failures!

Additional research into why demonstrated hinge lifetimes greatly exceeded our initial finite element analysis estimates proved that MEMS models need to use thin-film properties of metal, not bulk properties. Bulk models of macroscopic fatigue are based on dislocations coalescing or "piling up" at the surface of the metal. As the density of the dislocations increases, fatigue cracks form. The dislocations then

accumulate at the fatigue crack, further concentrating mechanical stresses, until the yield point is exceeded and breakage occurs.

With extremely thin films such as the DMD hinge, the material is only one grain thick, thus providing two free surfaces to restrain any dislocations. Because of this, the thin film material does not accumulate a high enough density of dislocations to form fatigue cracks. In addition to the test results, hinges from several devices were thoroughly inspected for fatigue damage using a transmission electron microscope (TEM). Even at the sections of the hinge where the most stress was expected, there was no evidence of dislocations, grain irregularity, or fatigue.

As we refined our finite element analysis models based on thin film properties and actual test results, we were able to predict the performance of new designs that matched test results. We now estimate, as we have demonstrated, that hinges will not break during at least 10 years of normal use in any application and more than 50 years in most applications. To date, we have not identified the point at which a hinge wears out.

A significant lesson learned from this potential failure mechanism is that a thorough understanding of thin film properties as well as models that support thin film material are critical to successful MEMS development.

Hinge Memory

One of the most significant failure modes identified during our development program and also one of the last remaining life-limiting modes is called "hinge memory." Hinge memory occurs as a mirror is operated in the same direction for a long period of time. For example, a mirror continually landed on the off-side (that is, when the mirror appears dark in a projected image) will exhibit a small amount of residual tilt when all voltages are removed, as shown in Figure 5.

The mirror will continue to operate properly as long as the electrostatic fields can direct the mirror to the proper state. When the residual tilt exceeds approximately 35 to 40% of the 10 degree rotation angle, most mirrors will not function properly and the pixel will appear non-

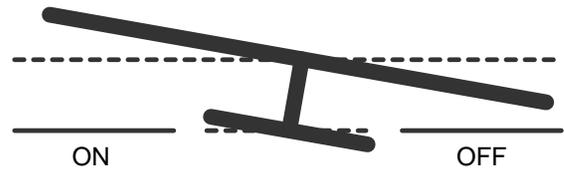


Figure 5. A mirror that does not return to a flat position after electrostatic fields are removed exhibits "hinge memory."

functional to the observer. Although the address state under the mirror is changing, when the bias voltage is reapplied to the mirror, the electrostatic forces on the off-side are greater than those on the on-side because of the smaller distance. Thus, the mirror will land only to the off-side.

The factors that contribute to hinge memory consist of operating temperature and mirror duty cycle. (For hinge memory calculations, duty cycle is the percentage of time the mirrors are addressed to one side in relation to the other. For instance, a 95/5 duty cycle means the mirrors touch the on-side 95% of the time and the off-side 5% of the time. A duty cycle of 50/50 means the mirrors touch both sides equally and no hinge memory occurs.)

To evaluate DMD performance, we have developed a measure of hinge memory using our DMD optical test equipment. The test equipment sweeps the bias voltage while it counts the number of functional mirrors at each voltage step. This is referred to as a bias voltage sweep or V_{bias} curve. Figure 6 shows a series of V_{bias} curves. The Y-axis shows the number of nonfunctional mirrors; the X-axis shows the bias voltage. At low bias voltages, mirrors will not land because there are insufficient electrostatic forces. As the test equipment increases the bias voltage, more mirrors become functional.

To accelerate hinge memory, we have established a life test using the standard test conditions of 65 °C and 95/5 duty cycle. As residual tilt builds up in a DMD, a larger bias voltage is required to land the mirror on both sides. This is evident in Figure 6. Curve A is the average V_{bias} curve for a group of DMDs as fabricated. After life testing the devices at high temperature and high duty cycle, the curve shifts to the

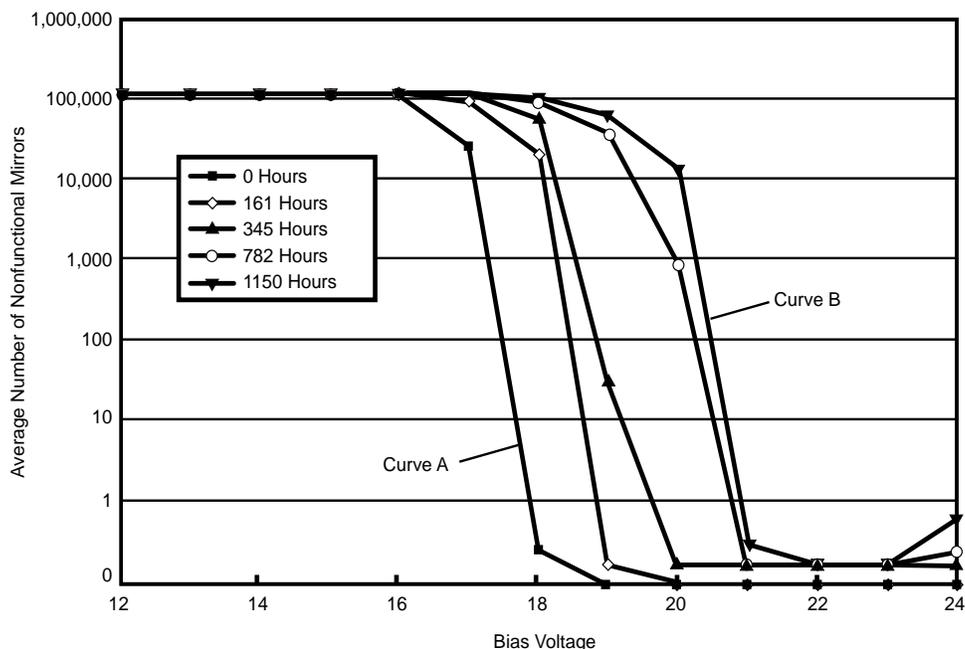


Figure 6. Series of bias voltage curves for a group of DMDs. Shifting of these curves is a measure of hinge memory.

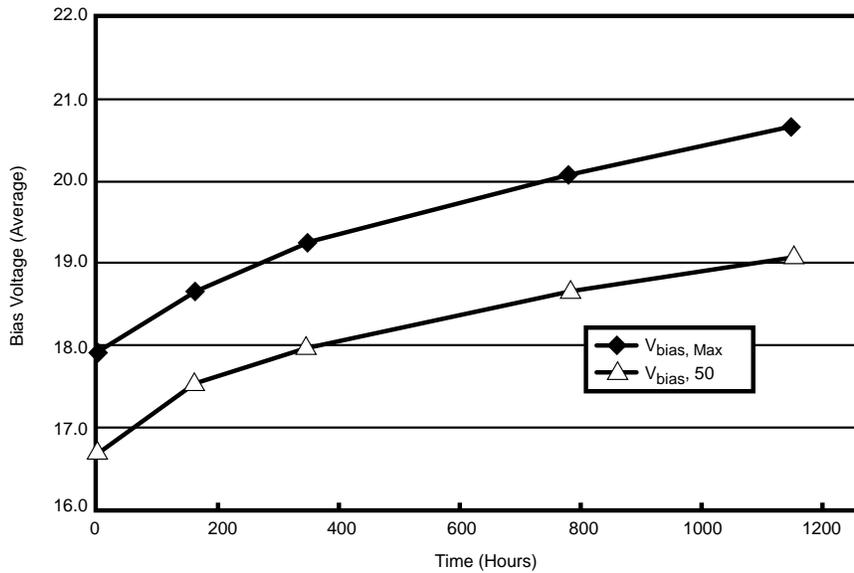


Figure 7. Plot of $V_{bias, max}$ and $V_{bias, 50}$ as a function of time. These parametric curves have been used to monitor process control, implement design improvements, and predict DMD lifetimes

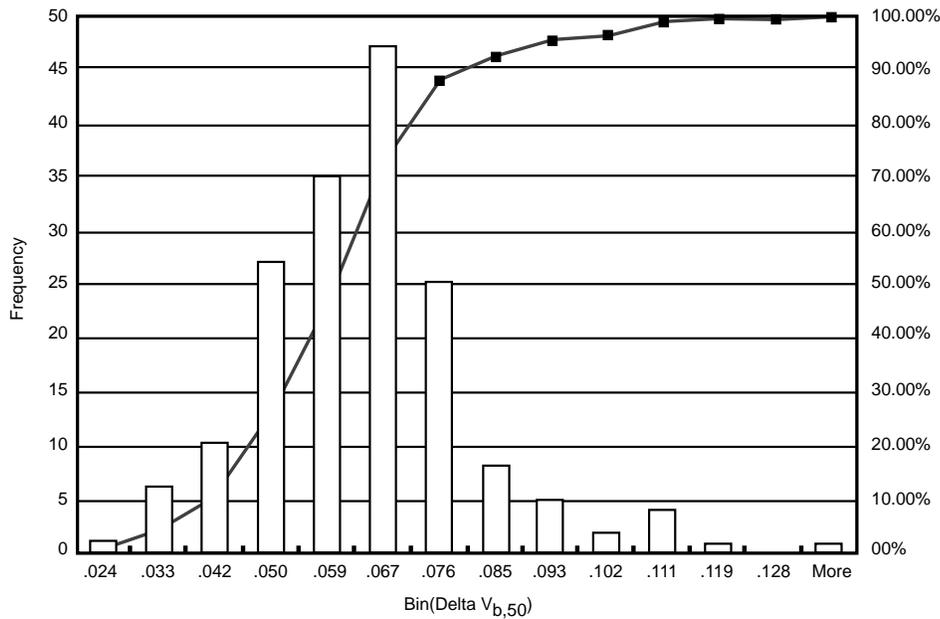


Figure 8. Distribution of $V_{bias, 50}$ shift after 160 hours of accelerated life test (high temperature and high duty cycle). This is a statistically normal distribution.

right, indicating a need for higher bias voltage to maintain mirror functionality. Curve B is the average V_{bias} curve for the same group of DMDs after 1150 hours of operation at 65 °C and 95/5 duty cycle. This series of curves is typical of device performance, and the shape of the curves is consistent from device to device.

Because the curves are consistent, we can take representative points and plot their shift in relation to time. Figure 7 shows a plot of $V_{bias, max}$ (the bias voltage at which the last mirror becomes functional) and $V_{bias, 50}$ (the median of the V_{bias} curve). Notice that both curves are parallel and that the rate of change is slowing as the test progresses. This, again, is typical of all DMDs.

Hinge memory on any given device follows a curve similar to that shown in Figure 7. Several hundred devices were sampled to determine their behavior over time. We placed each device on a life test at

the same test conditions (65 °C, 95/5 duty cycle) and tested them again after 160 hours. By comparing the $V_{bias, 50}$ before the life test and after 160 hours, we found that the $V_{bias, 50}$ shift is a normal distribution, as shown in Figure 8. Now that we know this phenomenon is predictable, we can estimate lifetime by extrapolating time and stress after a shortened life test. Based on a series of tests with devices operating at various temperatures and duty cycles, we have determined that temperature is the dominant factor for hinge memory lifetime. Figure 9 shows projected lifetimes at various temperatures and the performance improvements achieved since we initiated the reliability development effort.

The root cause of hinge memory is metal creep of the hinge material. We evaluated alternate materials and process enhancements to determine if we could affect hinge memory by reducing metal creep. Through experimentation and the use of the parametric curves described

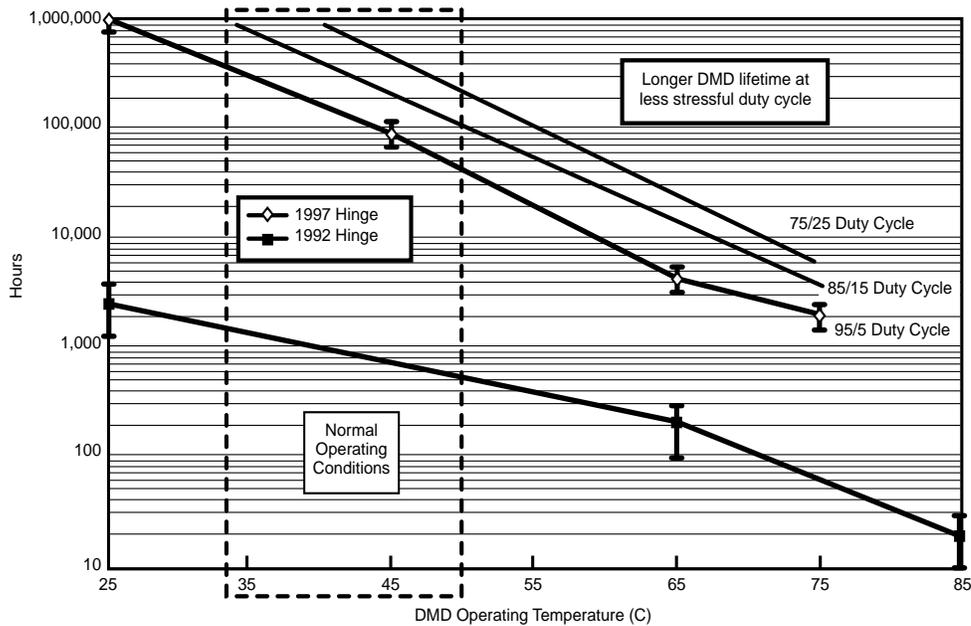


Figure 9. DMD lifetime estimates when operated at high temperature (65 °C) and high duty cycle

above, we selected an improved hinge material that did not exhibit the same degree of metal creep. This increased lifetime by a factor of approximately 5 but was still not sufficient for product reliability, since we estimated a worst-case (65 °C, 95/5 duty cycle) lifetime of only 1000 hours.

The next significant improvement was the implementation of stepped V_{DD} and a “bipolar reset.” Stepped V_{DD} provides a higher voltage to the address electrode while the mirror is in transition to the proper side. Bipolar reset uses a positive bias voltage to land the mirrors and a negative reset voltage to resonate the mirrors. These two changes provide a greatly increased electrostatic field differential and allow the mirrors to be dynamically controlled over a wider range of hinge memory. As a result of having better control of the mirror during its transition, DMD lifetime increased by another factor of five to about 5000 hours. At normal DMD operating temperatures of 35 to 45 °C and a high duty cycle of 95/5, we extrapolate DMD lifetimes of more than 100,000 hours. At typical duty cycles, such as 85/15 and 75/25, the lifetime is even higher.

It is evident from this discussion that thermal management is integral to DMD lifetimes. There are several sources of heat that could contribute to hinge memory and, therefore, shortened DMD lifetime. The primary source is radiant energy from the light source. Although, this would appear to be a significant source of heat, in reality, the mirror surface reflects most of the energy. Radiant energy striking the package is much more likely to be absorbed and heat up the entire package. System apertures and optical integrators are very effective at reducing the temperature of the DMD package. Since the ceramic package is an inefficient thermal conductor, most applications attach a simple heatsink and radiator to the back of the package. This can dissipate sufficient thermal energy to maintain the DMD at just a few degrees above its ambient. The second source of thermal energy is from the projector assembly surrounding the DMD. Significant sources of heat in a projector include: lamp, lamp ballast, power supply, and electronics. Efficient and well-designed thermal management is necessary to ensure that the ambient temperature surrounding the DMD is maintained at a reasonable level. A third, but insignificant, source of heat is self-heating of the DMD CMOS.

In most applications developed to date, the DMD operates at temperatures only 7 to 10 °C above the projector ambient. Thus, even

with a projector continuously operating in an ambient temperature of 40 °C, the DMD is operating below 50 °C, thus ensuring a lifetime greater than 40,000 hours. A thorough discussion of DMD thermal management techniques can be found in reference [7].

We have recently identified additional improvements to the hinge material. These changes are expected to further reduce metal creep and, therefore, increase robustness for operation at high temperature by at least another order of magnitude. As these improvements are realized, the resulting reduction in hinge memory can allow more flexibility in DMD design, DMD control, DMD operating limits, and system thermal management requirements.

Nonfunctional (Stuck) Mirrors

One of the most obvious defects in a DMD array is the appearance of a nonfunctional mirror. There are numerous potential causes for improper mirror function. As discussed in the previous section, hinge memory could eventually result in a mirror appearing to be stuck on one side or the other. It is still functional, but the electrostatic field is not sufficient to move the mirror from one side to the other.

Other conditions that contribute to nonfunctional mirrors are particulate contamination, surface residue, capillary condensation, CMOS defects, and van der Waals forces.

Most mirror defects in today’s delivered DMDs can be traced to a particle, either on the surface of the mirror or under the mirror. A particle in either location, if it is of sufficient size and in a critical location, can result in improper mirror operation. A particle may be wedged between mirrors (thus interfering with mirror movement); the particle may be on the surface of the mirror (thus affecting mirror rotation dynamics); a particle may have affected the mirror during processing and damaged a hinge; or a conductive particle can result in a high-resistance short on the address electrode so that the mirror is not addressed properly. We have observed instances of all these defects during DMD fabrication.

As in most wafer fabs, particles are the number one contributor to yield loss, and the DMD is no different. In addition to causing fabrication yield loss, particles can contribute to reliability failures since the mirror array is exposed to any loose particles in the package cavity.

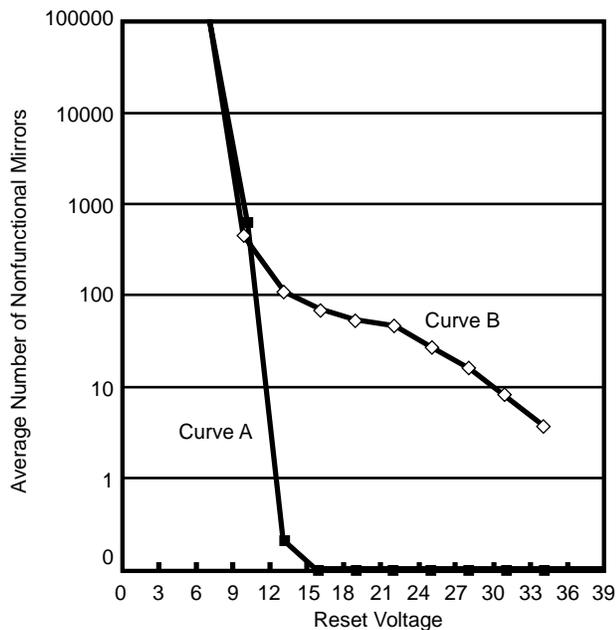


Figure 10. V_{reset} curves indicating qualitative measurement of surface adhesion

Our particle reduction activity is continuously resulting in improved yields. More importantly, the effort is further reducing our reliability risk. There are now fewer opportunities for mobile particles that may eventually result in premature mirror failure or damage.

The second most prevalent cause of nonfunctional mirrors is the existence of a surface contaminant or residue at the mirror tip landing point. The contaminant may contribute to increased surface adhesion, which prevents a mirror from functioning. We observe this occasionally as a result of improper surface cleaning during the superstructure processing. Gross processing errors that would result in premature device failure are readily identified during our normal burn-in and screening steps. Reliability sample testing identifies more subtle process variations. Parameters are measured based on a reset voltage sweep or V_{reset} curve, much the same as the V_{bias} curve discussed in the hinge memory section of this paper. DMD optical test equipment sweeps the reset voltage while it counts the number of functional mirrors at each voltage step. This is referred to as a V_{reset} curve (Figure 10). The Y-axis shows the number of nonfunctional mirrors; the X-axis shows the reset voltage. At low reset voltages, mirrors will not release because of the forces holding the mirrors to the surface. As the reset voltage is increased, more mirrors release from the surface as the mechanical energy stored in the mirror overcomes the forces holding the mirror tips to the landing surface. At even higher reset voltages, energy is added to the mirror by pulsing it at its resonant frequency.

In this test, we are able to measure the distribution of surface adhesion across the DMD by reducing the magnitude of the voltage pulse used to excite the mirror. As the magnitude of the voltage is reduced from its maximum, any mirrors with excessive surface adhesion cease to function. As the sweep continues, we can develop a distribution curve that represents the adhesion signature of each device. Figure 10 provides an example of two curves taken after 160 hours of life test. Curve A is the distribution of mirrors from a sample of production DMDs (control devices) and curve B is the distribution of mirrors from a proposed process change (test devices). It is apparent that the test devices have a small number of mirrors that exhibit surface adhesion after the test, whereas the control devices are unchanged. Based on this information, the test devices were deemed “not as robust” as the control devices, and the process was further optimized before we in-

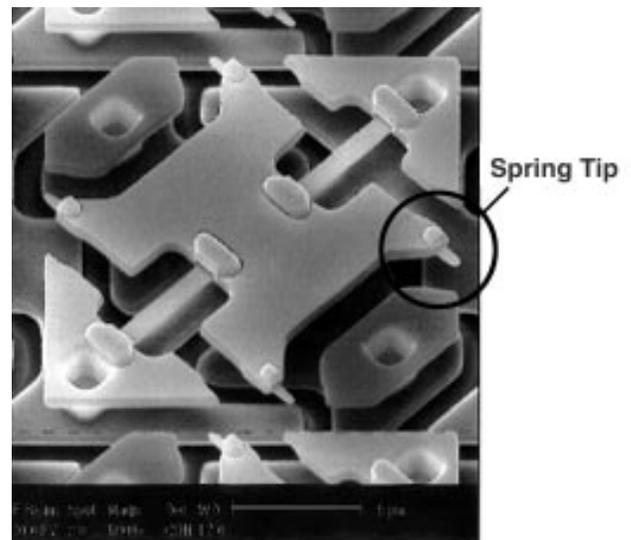


Figure 11. Closeup image of a micromirror landing tip showing a spring tip. The spring not only absorbs energy during landing but stores energy for more efficient mirror release.

corporated the design change. As a result of monitoring the shift in this parametric curve over time, we have developed a leading indicator of potential reliability degradation attributable to excessive surface adhesion.

Before DMD production was started in 1996, the V_{reset} parametric curve indicated that surface adhesion was too great to deliver a reliable device. An innovative approach to overcoming surface adhesion was the addition of “springs” to the landing tips of the mirrors (Figure 11). As bias is applied to a mirror, the mirror lands, the springs deform, and energy is stored in the springs. When a reset pulse is applied and bias voltage is removed, the stored energy pushes the mirror tip off the surface. This has virtually eliminated the impact of surface adhesion due to surface contamination.

The remaining three contributors to nonfunctional mirrors, capillary condensation, CMOS defects, and van der Waals forces are minor contributors to reliability degradation. We control capillary condensation by sealing the device in a controlled atmosphere and maintaining this atmosphere through robust package design methods. Although CMOS defects are a contributor to yield loss, extensive life testing has shown no evidence of CMOS parametric degradation contributing to added defects. Surface adhesion due to van der Waals forces (molecular surface forces) are minimized by applying a special coating to the landing surface. The spring tips also provide additional margin against any increase in surface adhesion forces.

Light Exposure

More than 300 DMDs have been exposed to intense, broad-spectrum light while operating for more than 1000 hours, with some operating for well over 5000 hours. Throughout all of these tests, there was no evidence that light exposure resulted in a fundamental performance degradation. Many of the devices were tested again after light exposure, and the reset curves and bias curves (as described previously) were unchanged from initial outgoing tests. Destructive analyses, such as residual gas analysis (RGA), X-ray photoelectron spectroscopy (XPS), and time-of-flight secondary ion mass spectrometry (ToFSIMS), were also performed on several devices after light exposure. Again, there was no evidence of fundamental chemical degradation or damage to the landing surface or superstructure.

Particles68%
Window Quality18%
Random Pixel10%
Other	...4%

Figure 12. Pareto analysis of DMD field returns

Occasionally we noticed a slight statistical trend toward some DMDs having more defects when exposed to UV and near-violet light. There were also several DMDs that failed because of stuck pixels in preproduction projectors. To better understand this phenomenon, we ran a series of tests using actual projectors. Each projector was modified to have a different UV cutoff filter. We found that DMDs were more likely to fail as a result of nonfunctional stuck pixels if exposed to light at wavelengths of 400 nm and below. A UV filter was, therefore, added to the DLP optics path to ensure a flux density of no more than 0.7 mW/cm² below 400 nm, most of which is beyond the visible spectrum of light. Since the addition of the UV filter, there have been no reported projector failures.

ENVIRONMENTAL ROBUSTNESS

One of the first steps we performed during the early stages of our reliability development program was to conduct a series of environmental tests similar to those performed in accordance with TI Semiconductor Group standards. These tests consisted of thermal shock, temperature cycling, moisture exposure, mechanical shock, vibration, acceleration, temperature storage, altitude, bond wire integrity, substrate attachment integrity, and ESD characterization. The superstructure was extremely robust [5]. The mirrors were not damaged by mechanical shock, vibration, or acceleration. There was no physical or parametric curve degradation due to temperature shock, cycling, or storage.

These results, especially the robustness against vibration and shock, are surprising to some but easily explained. The micromirrors resonate at frequencies greater than 100 kHz. Normal handling occurs at frequencies less than 1000 Hz. Thus, the DMD micromirrors are unaffected by any vibration modes set up during assembly or handling.

Although the mirrors were robust, the tests identified some weaknesses in the package that were subsequently corrected. The tests also demonstrated that loose particles in the package cavity can land on and damage the mirror superstructure. The evidence of mirror damage due to loose particles was the impetus to accelerate our particle reduction program to minimize our field reliability risk. The primary source of particles was found to be from the chemical interaction of the die attachment adhesive with the coating used to reduce surface adhesion. The secondary source was silicon particles, mostly from the edge of the die, and mostly due to the die sawing and separation process. Other miscellaneous particles (for example, carbon-based and aluminum) were found to come from handling, assembly, and equipment sources. Corrective actions to reduce our risk due to particles included the selection of a new die attachment adhesive, an improved wafer sawing process, better handling methods, more frequent particle monitoring,

and numerous other process improvements throughout the fabrication line. Yield loss due to particles has been reduced by a significant percentage and continues to improve.

LIFETIME DEMONSTRATIONS AND RELIABILITY ESTIMATES

Through the use of accelerated life testing, the development of rudimentary models, and environmental qualification, we have identified what we believe to be the complete list of life-limiting factors. As discussed previously, hinge fatigue and environmental exposure are not life limiting. Particulate contamination appears to be random and not dependent on time or stress. We have not identified any correlation between light exposure and life. Through design robustness and process control, we have eliminated all known contributors to surface adhesion degradation. This leaves hinge memory. Because hinge memory is so predictable, we have easily estimated our lifetime to be greater than 100,000 hours, as long as the DMD die temperature is maintained at 45 °C or below.

Although an actual lifetime of 100,000 hours has not yet been demonstrated, there is supporting evidence that DMD lifetime is measured in thousands of hours. Existing data through nearly 2 years of product deliveries have confirmed no DMD failures due to parametric curve degradation (bias voltage parametric curves and reset voltage parametric curves). Several DMDs remain on test through 19,000 actual operating hours with no failures to date. This certainly supports the test results and estimates.

In terms of random failures, few devices have failed during end-user use. We anticipated that particles would dominate random failures, and that has proved to be true. Particles remain our primary cause of yield loss, but we have not observed a significant amount of customer returns caused by particles. In fact, even though particles are our primary pareto item (Figure 12), the field failure rate for all DMDs delivered to date is less than 0.2%. We have estimated a mean time between failures (MTBF) by using the total number of units shipped, multiplied by an estimate of usage hours per month, divided by the total number of reported DMD failures. Using conservative estimates for all three of these factors, we have a demonstrated MTBF (random failures) of 119,000 hours.

SUMMARY

This paper has highlighted DMD failure modes, failure mechanisms, and actions taken to improve reliability. Figure 13 presents a summary of DMD lifetime estimates as a result of major design enhancements implemented since 1992. The reliability development program has achieved the following milestones:

- The DMD has been subjected to typical semiconductor environmental qualification tests and proved to be robust to all, including temperature cycling, mechanical shock, and vibration.
- We have calculated an MTBF of greater than 119,000 hours based on actual field data.
- We have projected a lifetime of more than 100,000 hours based on actual test results and modeling data developed for the DMD. The only life-limiting failure mechanism identified to date is temperature-accelerated hinge memory.
- We have demonstrated more than 1.7×10^{12} mirror cycles with no hinge fatigue failures. This correlates to 95,000 hours of normal operation.

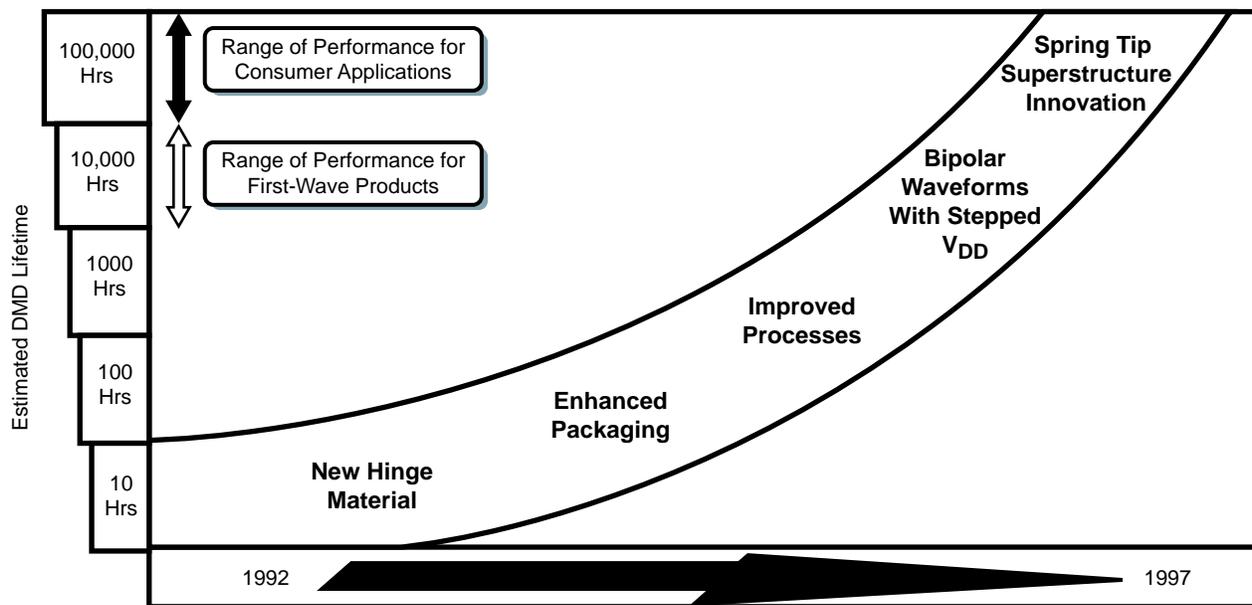


Figure 13. Reliability development and lifetime improvement

In summary, test results and field performance have demonstrated that DMD reliability is surpassing its original projections.

ACKNOWLEDGMENTS

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