DIGITAL MICROMIRROR DEVICE (DMD) HINGE MEMORY LIFETIME RELIABILITY MODELING

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ABSTRACT

The Digital Micromirror Device (DMD) continues to make significant improvements in high temperature operating lifetime. This paper will briefly describe the DMD, the hinge memory failure mode and parametrics important to characterize hinge memory, provide lifetime estimates and compare results to practical experience. The methods employed to develop an understanding of DMD lifetime are very similar to those used throughout the semiconductor industry to model reliability. While the failure modes and mechanisms may be quite different, the approach of identifying failure modes, accelerating the failures and applying acceleration to estimate lifetime is the same.

INTRODUCTION

DLP™ projector applications continue to push for smaller, lighter and brighter systems. These requirements translate into increased demands on the components that make up these projectors. The lamps must produce more lumens, the optics must be more efficient, the ASICs must integrate more system functions and the DMD must operate at higher temperatures [1] with system cooling fans operating at lower speed for noise reduction. Tests have shown a significant increase in DMD reliability at high operating temperatures. This paper will provide a brief description of the DMD and the operating voltages applied to the device. It will describe hinge memory testing, the parametrics developed to characterize hinge memory and the empirical models that are derived from the testing, and provide lifetime estimates. Two methods for predicting hinge memory lifetime will be presented, one based on parametric degradation, and another based on non-functional mirrors using Weibull life distributions and Arrhenius acceleration. The results of both methods will be compared to practical experience.

The DMD

A DMD is an array of microscopic aluminum mirrors on the surface of a CMOS static random access memory (SRAM) integrated circuit (Figure 1). The device is fabricated with standard semiconductor processes. [2] [3]

The output of each SRAM cell and its complement control the potential applied to the mirror electrodes. One electrode is tied to the output and the other to the complementary output. When one electrode is set high (typically 5V), the other is set low (0V) depending on the information loaded into the memory cells. Under normal operating conditions, when a bias is applied (typically 26V), the mirror/yoke assembly, rotating on the axis of the hinge, is attracted to the electrode with the greatest potential difference. The spring tip, made of the same material as the hinge, lands on the top metal layer of the substrate. When the bias is removed (allowed to float or set to 0V), the mirror normally returns to the flat processed state. Landing the mirror to produce a -10 degree tilt angle is considered a minus (-) landing while landing the mirror to the +10 degree side is a plus (+) landing.

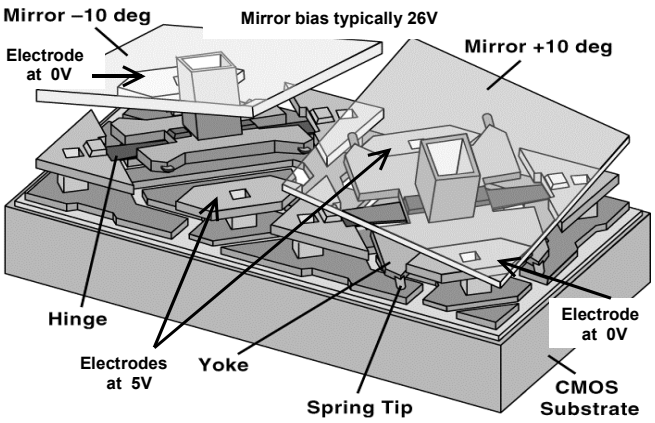

Figure1. DMD Superstructure.

HINGE MEMORY

Hinge memory is a situation that occurs when the mirror bias is removed and the mirror returns to a non-flat state due to a set twist in the hinge (Figure 2). The angle created from this non-flat state is called the residual torque angle. If this angle becomes too large, the mirror will no longer be able to land on the side opposite the torque angle direction resulting in a hinge memory failure.

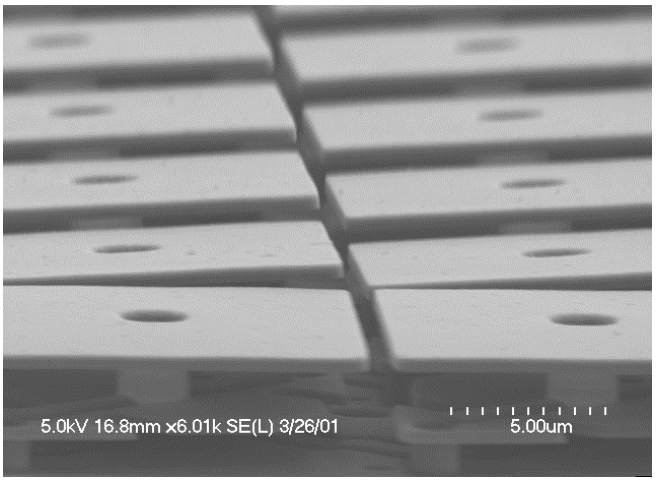

Figure 2. SEM image of mirrors exhibiting hinge memory. The first row at the bottom of the image is in the normal flat unbiased state. The second and subsequent rows are tilted to the minus side following extended operation at accelerated conditions.

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Operating DMDs with a pattern that lands mirrors on one side more than the other produces hinge memory. Tests for hinge memory are routinely performed with all the active array mirrors landing on the minus side 5 times and then the plus side 95 times (see [3] for a more complete description of DMD operation). This is commonly referred to as a 5/95 duty cycle. This duty cycle was chosen to represent system applications where certain parts of the display will command the mirrors to land on one side more than the other for a large portion of the projector's lifetime. This situation occurs when either static full on (100/0) or off (0/100) is displayed for a large part of the display's lifetime but is not representative of applications with random video like cinema or home entertainment. Lifetimes for applications with random video where the duty cycle is more likely to be 15/85 or 25/75 are much higher than for the static images represented in these tests. [4]

Hinge Memory Parametrics

Several parametrics have been developed by Texas Instruments to characterize the DMD performance. The parameters that are important to understanding hinge memory will be described in this paper as well as how the parameters are used in reliability modeling.

Testing is performed to characterize the mirror landing performance of the device. In this test, the memory cells are set to land all the pixels in one direction (either plus or minus) and a DC bias is applied to the mirrors and stepped up from 11 to 22 volts. For each voltage setting, the number of landed mirrors is counted using optical microscopy and image processing software. A small portion, or frame, of a device can be imaged at a time by the microscope and a sample of frames is taken across the device to characterize the device's performance. A plot of voltage versus number of landed pixels on the minus side is generated (Figure 3).

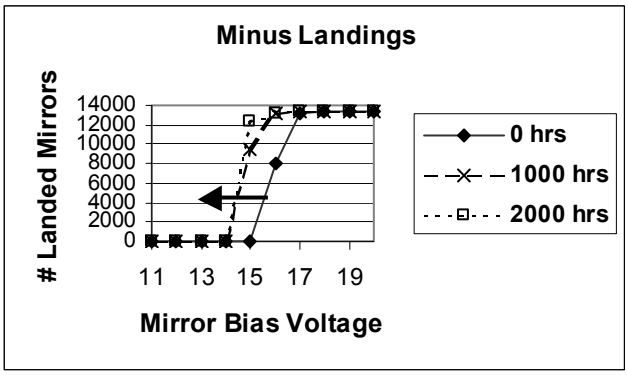

Figure 3. Minus side landing voltage decreases with test time.

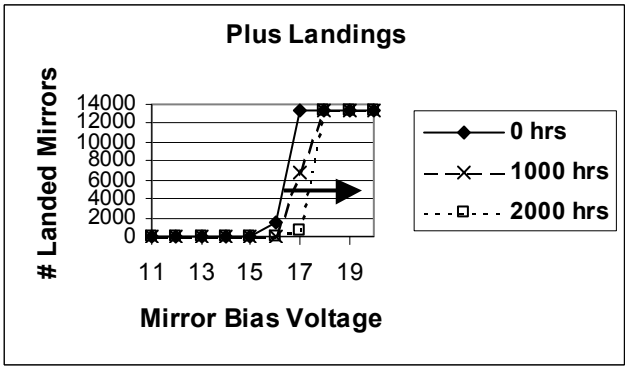

Figure 4. Plus side landing voltage increases with test time.

As the device accrues hinge memory during the 5/95 duty cycle test, the mirrors land at lower voltages on the minus side (Figure 3). Conversely, when the mirrors are addressed to land on the plus side, higher voltage is required to land the mirrors (Figure 4).

Vb50 +/- is the difference between the DC bias applied to the mirrors required to land half the mirrors on one side versus the other side (Figure 5). This median voltage difference is correlated with the amount of residual torque angle of the mirrors when no bias is applied and is the key parametric for monitoring hinge memory.

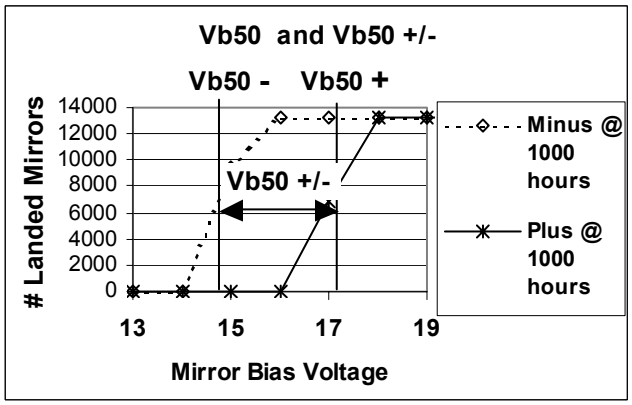

Figure 5. Vb50 - is the voltage required to land half the mirrors on the minus side, Vb50 + is the voltage required to land half the mirrors on the plus side and Vb50 +/- is the difference between the plus and minus landing voltages.

Change of this parametric, and thus hinge memory, is accelerated by testing at high temperatures. Hinge memory testing is typically performed at 65°C, 85°C and 95°C while operating the mirrors at a 5/95 duty cycle. Figure 6 is a plot of Vb50 +/- and shows the relationship between hinge memory, time and temperature. The three lines are the average Vb50 +/- for a sample of devices tested at 65°C, 85°C and 95°C. The higher temperature devices have a more rapid change in this parametric than at lower temperatures.

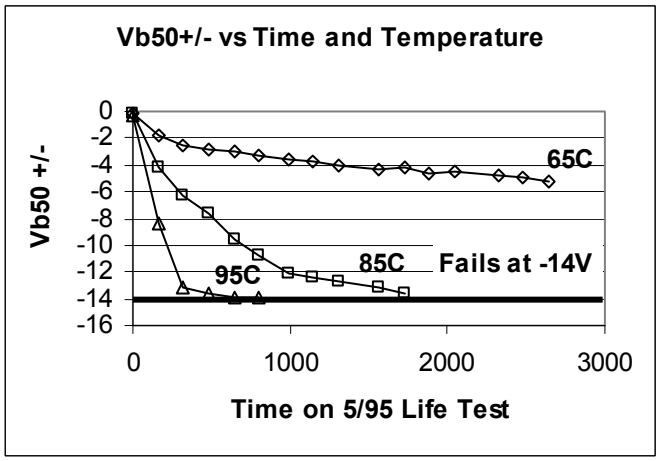

Figure 6. Vb50 +/- changes with time and is accelerated by temperature.

By operating devices to failure at 85°C and 95°C, it was observed that non-functional mirrors begin to occur at Vb50 +/- of -14V. Yet some devices continued to work well past this value. –14V is used in modeling as a conservative limit of DMD operation while devices in projectors may continue to operate well beyond this point. Testing at 65°C was suspended at 2,700 hours with no hinge memory failures.

Linear extrapolation of the 65°C Vb50 +/- data to –14V yields a conservative estimated average lifetime of 11,000 hours (Figure 7).

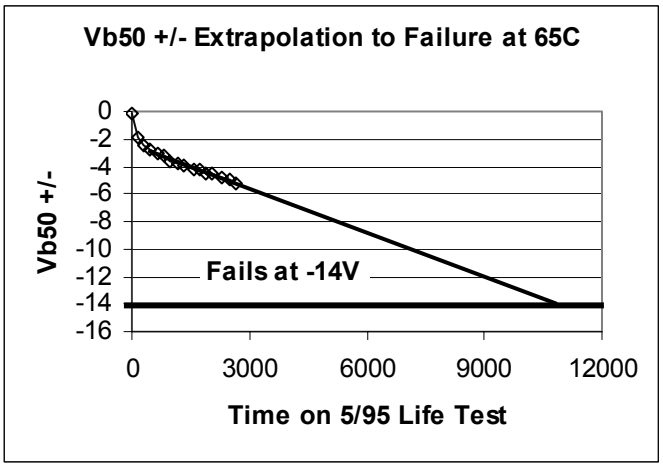

Figure 7. Vb50 +/- extrapolation to failure gives average lifetime of over 11,000 hours at 65C.

Non-functional mirrors

The number of additional non-functional mirrors is monitored periodically throughout the tests and has been shown to be a useful metric for predicting lifetimes. A typical hinge memory failure occurs when the mirror will no longer land to one side when operated at projector bias conditions. This is because the residual torque angle is so great that the electrostatic forces can no longer land the mirror on the opposite side. Figure 8 is a Weibull plot of the 0.7 Extended Graphics Adapter (XGA) 14 micron 10° tilt angle device lifetime as a function of temperature at three test temperatures of 65°C, 85°C and 95°C using non-functional mirrors as the failure criteria. Figure 8 uses the same population of test devices as Figures 6 and 7.

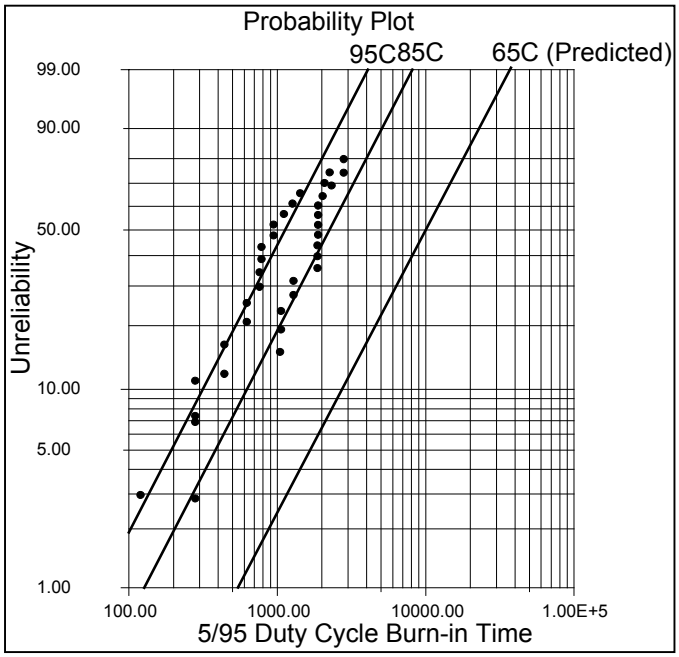

Figure 8. Weibull plot of hinge memory lifetimes at accelerated temperatures and worst-case duty cycle.

Arrhenius acceleration

Conventional practice in the semiconductor industry is to model temperature stress acceleration using an Arrhenius model. This method can also be applied to the DMD. The Arrhenius acceleration factor equation derived from the results of Figure 8 is:

$$A_F = e^{\left(\left(\frac{Ea}{K_B Tuse}\right)-\left(\frac{Ea}{K_B Taccel}\right)\right)}$$

Where A_F is the acceleration factor,

Ea is the activation energy ≥ 0.78

K_B is Boltzman's constant = 8.623 X 10-5eVK^{-1}

Tuse is the use temperature in Kelvin

Taccel is the accelerated temperature in Kelvin

The 65°C line (in Figure 8) is a prediction based on failure data from 85°C and 95°C because no hinge memory failures were observed through 2,700 hours of testing at 65°C. The mean lifetime predicted at 65°C using this method is 11,700 hours.

Using the above model, predicted mean lifetimes at typical operating temperatures of 55°C and 45°C, are dramatically higher than at the absolute maximum operating temperature of 65°C, with 27,000 and 63,000 hours respectively.

LIFETIME ESTIMATES

Comparing the lifetime estimates from the two methods shows that the methods yield similar results. The Vb50 +/- degradation method predicts a mean lifetime of 11,000 hours at 65°C and the Weibull-Arrhenius method using non-functional mirrors failure criteria yields a mean lifetime of 11,700 hours at 65°C. While the two prediction methods agree reasonably well, the latter approach also predicts a 1% failure rate at 500 hours. This does not agree with practical experience from qualification testing where hundreds of devices have completed 1000 hours of 5/95 duty cycle life testing at 65°C with no hinge memory failures. The actual activation energy is likely higher than the 0.78 calculated from Figure 8. Reasons for the discrepancy between modeling results and qualification may include:

- The accelerated tests at 85°C and 95°C are pushing the limits of the life test equipment, which introduced error into the temperature control. Since hinge memory is so highly dependent on temperature, this in turn may have resulted in error in the acceleration model.
- A linear function was used to extrapolate the degradation of Vb50 +/- at 65°C. Results from the 85°C and 95°C tests indicate that the degradation rate slows as this parameter nears –14V. If this same effect occurs at 65°C, we would expect longer lifetimes at 65°C.
- Testing at the higher temperatures may have introduced failure mechanisms that do not occur at the lower operating temperatures.

Tests are currently underway with improved temperature control at accelerated test temperatures and longer duration at 65°C, which

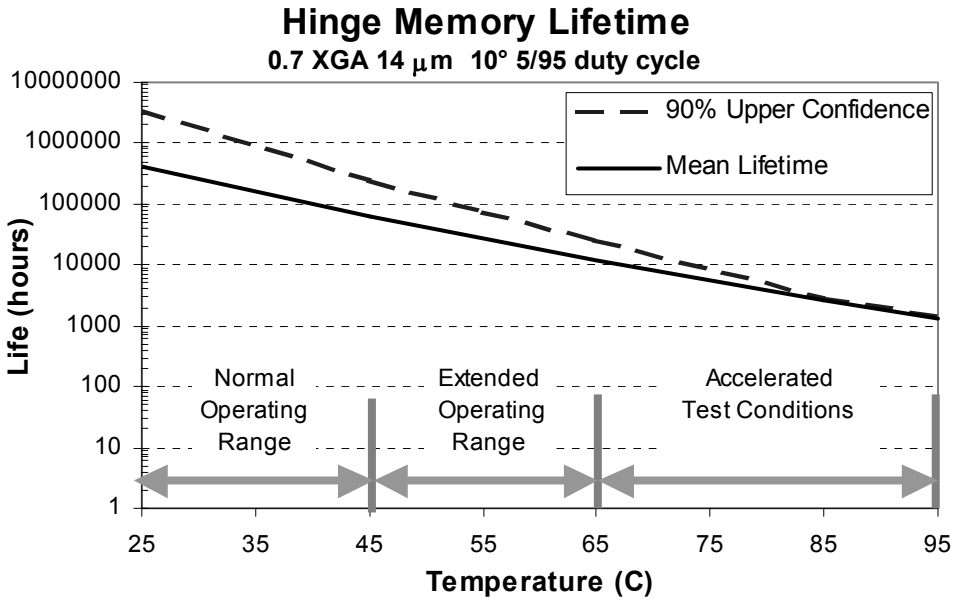

Figure 9. DMD hinge memory lifetime estimates for static images. Projectors showing primarily random video images, such as cinema or home entertainment TVs, will have significantly longer lifetimes.

are expected to improve the accuracy of the modeling methods. Results from these tests were not available in time for inclusion in this paper.

Review of DMD return history also supports the qualification test results with no reported hinge memory failures from field returns. Some of the reasons for this difference between accelerated test results and actual field experience are:

- The DMD is typically operated at lower temperatures with a normal operating temperature range of 25°C to 45°C.
- The DMD is typically not operated with a static image but with random images.
- The average duty cycle experienced in the field is typically less stressful than the nearly full off 5/95 duty cycle used in the accelerated tests.
- The projectors are not operated continuously, thus allowing the stress in the hinge to relieve during off time.

Future studies are anticipated to explore these factors and quantify their effects on hinge memory lifetimes to develop a more complete model of hinge memory. The reliability models will be updated to more accurately agree with the outstanding field reliability record of the DMD.

Figure 9 provides lifetime estimates for the 0.7 XGA 14 micron 10° tilt angle device derived from the Weibull-Arrhenius lifetime distributions at elevated temperatures using non-functional mirrors as the failure criteria. The lifetime estimate assumes continuous operation at a 5/95 duty cycle. Given the conservativeness of the modeling approach, our future studies are expected to demonstrate that the true mean life is between the predicted mean and the upper 90% confidence interval on the mean. Hinge memory lifetimes in projector applications with temperatures in the normal operating range of 25°C to 45°C are in excess of 100,000 hours. Even with temperatures of 45°C to 55°C in the extended operating range, lifetimes are in excess of 50,000 hours.

These results are a dramatic improvement on previous studies [4] and are the result of several device fabrication and packaging process improvements.

SUMMARY

The methods employed to develop an understanding of DMD hinge memory lifetime are very similar to the methods used throughout the semiconductor industry to model reliability. While the failure modes and mechanisms may be quite different, the approach of identifying failure modes, accelerating the failures and applying acceleration to estimate lifetime is the same. Parametrics and accelerated test methods have been developed to model DMD lifetime performance, to assess device reliability during the development process, and to assure new products meet reliability demands of the market. Results from accelerated testing and field experience show that the DMD has met or exceeded customer needs with over 100,000 hour mean hinge memory lifetimes under normal operating conditions.

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