Texas Instruments

Data Sheet
TI DN 2509699 Rev B
March 2009

DLP® Discovery .7 XGA 2xLVDS 12^0 Type A Customer Datasheet

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Table 1. Product Description		
DMD Part #	Mechanical ICD	Description
*1076N732c	2507867	0.7 inch diagonal spatial light modulator of aluminum micro-mirrors. Pixel array size is (1024 x 768) in a Square Grid Pixel Arrangement. Low Voltage Differential Signaling (LVDS) data interface, Double Data Rate (DDR). Pixel Architecture is FTP with DarkChip3™.
*1076N732(UV)	2507867	0.7 inch diagonal spatial light modulator of aluminum micro-mirrors. Pixel array size is (1024 x 768) in a Square Grid Pixel Arrangement. Low Voltage Differential Signaling (LVDS) data interface, Double Data Rate (DDR). Pixel Architecture is FTP with DarkChip3™. UV – Modified Cover Glass to enable transmission of UV light

Device Status:

A lead alpha character of “X” implies the device has been released for restricted sales only.
When no lead alpha character (*) is present, the device has been released for unrestricted sales.

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Table 2. Pin Descriptions		
Pin Name	Description	Type
D_AN(15:0) D_AP(15:0)	• LVDS pair for Data Bus A (15:0)	I
D_BN(15:0) D_BP(15:0)	• LVDS pair for Data Bus B (15:0)	I
DCLK_AN DCLK_AP	• LVDS pair for Data Clock A	I
DCLK_BN DCLK_BP	• LVDS pair for Data Clock B	I
SCTRL_AN SCTRL_AP	• LVDS pair for Serial Control (Sync) A	I
SCTRL_BN SCTRL_BP	• LVDS pair for Serial Control (Sync) B	I
MBRST(15:0)	• Non-logic compatible Mirror Bias Reset signals • Connected directly to the array of pixel mirrors • Used to hold or release the mirrors • Bond Pads connect to an internal Pull-down resistor	I
MODE_A	• Data Bandwidth Mode Select • Bond Pad connects to an internal pull-down circuit • Refer to Table 3 for DLP® system board connection information	I
MODE_B	• Data Bandwidth Mode Select • Bond Pad connects to an internal pull-down circuit • Refer to Table 3 for DLP® system board connection information	I
PWRDNZ	• Active Low Device Reset • Bond Pad connects to an internal pull-down circuit	I
SCPCLK	• Serial Communications Port Clock Input. • Bond Pad connects to an internal pull-down circuit	I
SCPDI	• Serial Communications Port Data Input • Synchronous to the rising-edge of SCPCLK • Bond Pad connects to an internal pull-down circuit	I
SCPENZ	• Active Low Serial Communications Port Enable • Synchronous to the rising-edge of SCPCLK • Bond Pad connects to an internal pull-down circuit	I
SCPDO	• Serial Communications Port Output	O
EVCC	• Unused • Do Not Connect on the DLP® system board	NC (U)
VCC (Note 1)	• Power supply for Low Voltage CMOS logic • Power supply for normal high voltage at mirror address electrodes	PWR
VCCI (Note 1)	• Power supply for Low Voltage CMOS LVDS interface	PWR
VCC2 (Note 1)	• Power supply for High Voltage CMOS logic • Power supply for stepped high voltage at mirror address electrodes	PWR
VSS (Note 1)	• Common return for all power	PWR
RESERVED_FC	• Connect to GND on the DLP® system board • Bond Pad connects to an internal pull-down circuit	I
RESERVED_FD	• Connect to GND on the DLP® system board • Bond Pad connects to an internal pull-down circuit	I

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Table 2. Pin Descriptions		
Pin Name	Description	Type
RESERVED_PFE	• Connect to GND on the DLP® system board • Bond Pad connects to an internal pull-down circuit	I
RESERVED_STM	• Connect to GND on the DLP® system board • Bond Pad connects to an internal pull-down circuit	I
RESERVED_TP0	• Do Not Connect on the DLP® system board	I
RESERVED_TP1	• Do Not Connect on the DLP® system board	I
RESERVED_TP2	• Do Not Connect on the DLP® system board	I
RESERVED_XI1	• Do Not Connect on the DLP® system board • Bond Pad connects to an internal pull-down circuit	I
RESERVED_XI2	• Do Not Connect on the DLP® system board • Bond Pad connects to an internal pull-down circuit	I
RESERVED_XI3	• Unused • Do Not Connect on the DLP® system board • Bond Pad connects to an internal pull-down circuit	NC (U)
RESERVED_BA	• Do Not Connect on the DLP® system board	O
RESERVED_BB	• Do Not Connect on the DLP® system board	O
RESERVED_RA0	• Do Not Connect on the DLP® system board	O
RESERVED_RA1	• Do Not Connect on the DLP® system board	O
RESERVED_RB0	• Do Not Connect on the DLP® system board	O
RESERVED_RB1	• Do Not Connect on the DLP® system board	O
RESERVED_TS	• Do Not Connect on the DLP® system board	O
RESERVED_XO1	• Do Not Connect on the DLP® system board	O
RESERVED_XO2	• Do Not Connect on the DLP® system board	O

Note 1: VCC2, VCCI, VCC, and VSS power supplies are required for all DMD operating modes.

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Table 3. Data Bus LVDS Pairs versus MODE_A and MODE_B (Note 1)		
MODE_A	MODE_B	D_A & D_B
GND	GND	(0:15)
GND	VCC	(1, 3, 5, 7, 9, 11, 13, 15)
VCC	GND	Reserved – Do Not Use
VCC	VCC	(3, 7, 11, 15)

Note 1: DLP® ASICs or Drive Circuits (DDC4000) that drive data to the DMD typically do not support every mode shown in Table 3.

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Table 4. Absolute Maximum Ratings Note 1				
Parameters		Min	Max	Units
LVCMOS Logic Supply voltage: VCC	Note 2	– 0.5	4	VDC
LVCMOS LVDS Interface Supply voltage: VCCI	Note 2	– 0.5	4	VDC
Supply Voltage Delta | VCCI – VCC |	Note 5		0.3	VDC
Mirror Electrode and HVCMOS voltage: VCC2	Note 2	– 0.5	8	VDC
Input voltage: MBRST(15:0)	Note 2	– 28	28	V
Input voltage: other inputs	Note 2 Note 3 Note 4	– 0.5	VCC + 0.3	VDC
Input Differential Voltage: $\|V_{ID}\|$			700	mV
High level output current @ Voh = 2.4v : I_{OH}			– 20	mA
Low level output current @ Vol = 0.4v : I_{OL}			15	mA
Clock Frequency: DCLK_A and DCLK_B			460	MHz
Operating Temperature: Reference Locations 1 and 2 in Figure 1 Reference Locations 3 and Array in Figure 1	 Note 6 Note 7	 10 10	 65 65	 °C °C
Differential Temperature: Location 1 minus Location 3 in Figure 1 Location 2 minus Location 3 in Figure 1			 10 10	 °C °C
Storage Temperature (non-operating): Reference Locations 1, 2, and 3 in Figure 1		 – 40	 80	 °C
Operating Relative Humidity (non-condensing)		0	95	%
Storage Relative Humidity (non-condensing)		0	95	%

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Note 1:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the DMD. This is a stress rating only and functional operation of the DMD at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this product spec are not implied. Exposure to absolute maximum rated conditions for extend periods may affect device reliability.

Note 2:

All voltage values are with respect to GND (VSS)
VCC2, VCCI, VCC, and VSS (GND) power supplies are required for all DMD operating modes.

Note 3:

Excludes Mirror Bias Reset inputs MBRST(15:0)

Note 4:

This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS differential inputs must not exceed $|V_{ID}|$ = 700mV or damage may result to the internal termination resistors.

Note 5:

To prevent excess current, | VCCI – VCC | should be less than 0.3v

Note 6:

The DMD can be operated between 0° C and 10° C at power-up for a maximum period of 10 minutes without damage.

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Note 7:

Active array temperature cannot be measured directly. Therefore it must be computed analytically from measurement points on the outside of the Type A package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature, thermocouple location 3 (TC3) in Figure 1,is provided by the following equations.

$T_{array} = T_{ceramic} + (Q_{array} \bullet R_{array\text{-}to\text{-}ceramic})$

$Q_{array} = (0.00274 \bullet SL) + 2.0$

Where:

T_{array} = computed array temperature (°C)

$T_{ceramic}$ = measured ceramic temperature (°C) (TC3 location)

Q_{array} = Total DMD array power (electrical + absorbed) (watts)

$R_{array\text{-}to\text{-}ceramic}$ = DMD package thermal resistance from array to outside ceramic (°C/watt)

SL = measured screen lumens (lumens)

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. The nominal electrical power dissipation to use when calculating array temperature is 2.0 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source. The equations shown above are valid for a 1-Chip DMD system with total projection efficiency from DMD to the screen of 87%. The constant 0.00274 is based on array characteristics. It assumes a spectral efficiency of 300 lumens/watt for the projected light and illumination distribution of 83.7% on the active array, and 16.3% on the array border and window aperture.

Sample Calculation:

Screen lumens = 2000 lumens

$T_{ceramic}$ = 55.0 C

$Q_{array} = (0.00274 \bullet 2000) + 2.0 = 7.48$ watts

$T_{array} = 55.0\ °C + (7.48 \text{ watts} \bullet 0.9\ °C/\text{watt}) = 61.7\ °C$

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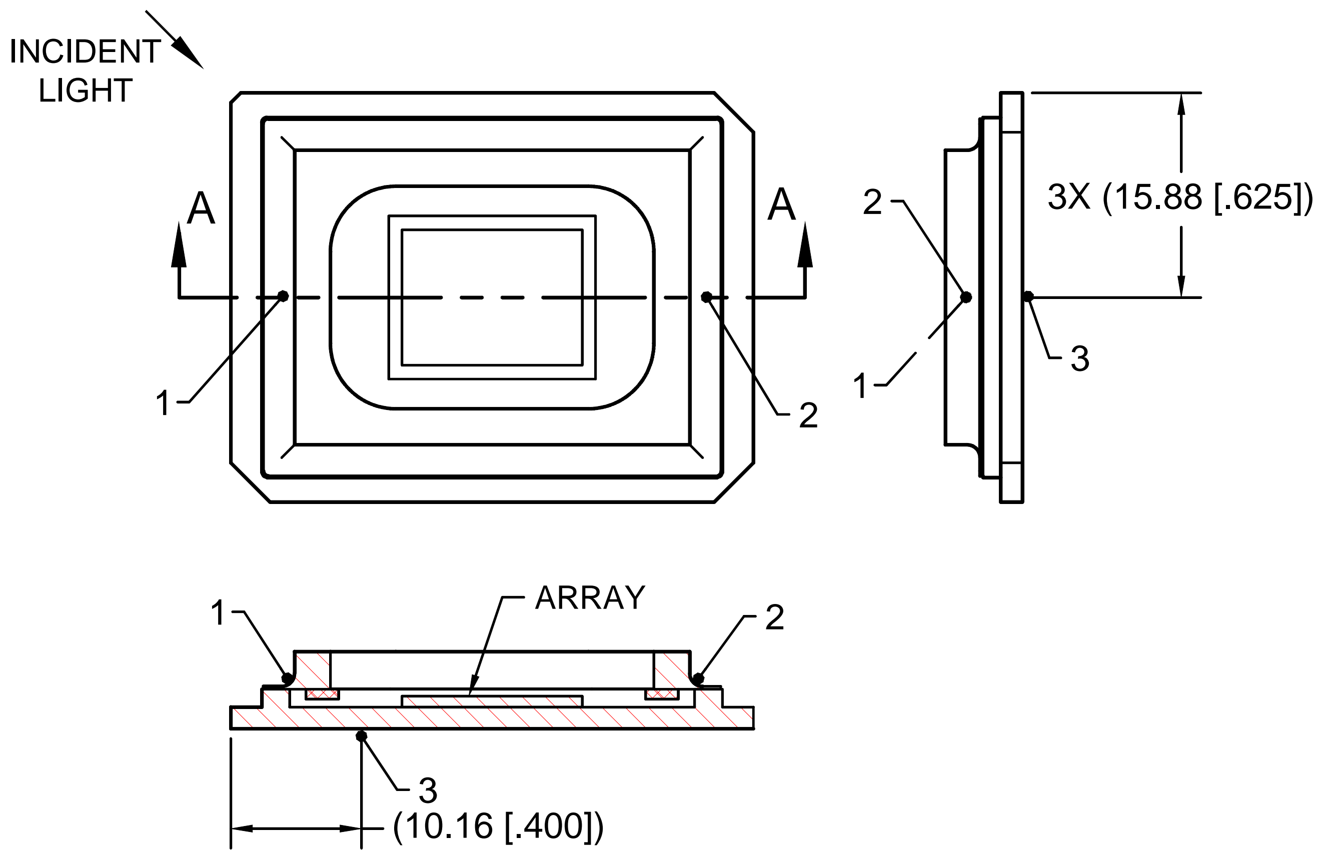

Figure 1. DMD Thermocouple Locations

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Table 5. Recommended Operating Conditions						
Parameters			Min	Nom	Max	Units
VCC	LVCMOS Logic Supply voltage	Note 12	3.0	3.3	3.6	V
VCCI	LVCMOS LVDS Interface Supply voltage	Note 12	3.0	3.3	3.6	V
	Supply Voltage Delta | VCCI – VCC |	Note 11		0	0.3	V
VCC2	Mirror Electrode and HVCMOS voltage	Note 12	7.25	7.5	7.75	V
V_{MBRST}	Mirror Bias / Reset voltage	Note 9	– 27		26.5	V
T_C	Operating Case temperature	Note 1	25		45	^oC
ILLvis	Typical Operating Range (continuous wave, 400-800nm)				25	W/cm^2
ILL_{UV}	Illumination , wavelength < 400nm	Note 13			0.68	mW/cm^2
ILL_{IR}	Illumination , wavelength > 800nm				10	mW/cm^2
LVCMOS parameters						
V_{IH}	High level Input voltage	Note 2	1.7	2.5	VCC + 0.3	V
V_{IL}	Low level Input voltage	Note 2	– 0.3		0.7	V
I_{OH}	High level Output current @ Voh = 2.4v				– 20	mA
I_{OL}	Low level Output current @ Vol = 0.4v				15	mA
T_{PWRDNZ}	PWRDNZ pulse width	Note 8	10			ns
SCP parameters		Note 7				
f_{SCPCLK}	SCP Clock frequency	Note 3	50		500	kHz
T_{SCP_SKEW}	Time between valid SCPDI and rising–edge of SCPCLK		– 300		300	ns
T_{SCP_DELAY}	Time between valid SCPDO and rising–edge of SCPCLK	Note 3 Note 5			960	ns
$T_{SCP_NEG_ENZ}$	Time between falling–edge of SCPENZ and the first rising–edge of SCPCLK	Note 3 Note 6	30			ns
$T_{SCP_PW_ENZ}$	SCPENZ inactive pulse width (high level)		1			$1/f_{SCPCLK}$
$T_{SCP_OUT_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tri-state)				1.5	ns
T_r , T_f	Rise/Fall Time (20% to 80%)				200	ns
400MHz LVDS parameters		Note 4				
$\|V_{ID}\|$	Input Differential Voltage (absolute value)	Note 10	100	400	600	mV
V_{CM}	Common Mode Voltage	Note 10		1200		mV
V_{LVDS}	LVDS Voltage	Note 10	0		2000	mv
Z_{LINE}	Line Differential Impedance (PWB/trace)		90	100	110	Ω
T_r	Rise Time (20% to 80%)		100		400	ps
T_f	Fall Time (20% to 80%)		100		400	ps
Z_{IN}	Internal Differential Termination Resistance		95		105	Ω
T_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ				10	ns

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Note 1:

Operating case temperature limits apply to the Array and Thermocouple location points 1, 2, 3, referenced in Figure 1

Note 2:

Tester Conditions for V_{IH} and V_{IL}:
Frequency = 60MHz. Maximum Rise/Fall Time = 2.5ns @ (20% - 80%)

Note 3:

The SCP clock is a gated clock. Duty cycle shall be 50% +/- 10%.
This parameter is related to the frequency of DCLK_A and DCLK_B, which are assumed to be 400MHz.
f_{DCLK} less than 400 MHz will impact the maximum f_{SCPCLK} range.

Note 4:

For timing parameters, refer to Table 9

Note 5:

This parameter is related to the frequency of DCLK_A and DCLK_B, which are assumed to be 400MHz.
Use $T_{SCP_DELAY} = (1/f_{DCLK})*(384)$ for f_{DCLK} less than 400 MHz.
f_{DCLK} less than 400 MHz will impact the maximum f_{SCPCLK} range.

Note 6:

This parameter is related to the frequency of DCLK_A and DCLK_B, which are assumed to be 400MHz.
Use $T_{SCP_NEG_ENZ} = (1/f_{DCLK})*(12)$ for f_{DCLK} less than 400 MHz.
f_{DCLK} less than 400 MHz will impact the maximum f_{SCPCLK} range.

Note 7:

For all Serial Communications Port (SCP) operations, DCLK_A and DCLK_B are required.

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Note 8:

PWRDNZ input pin resets the SCP and disables the LVDS receivers.
PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.

Note 9:

The positive voltage level of this input waveform must be optimized for DMD performance. Each DMD is assigned a bias voltage bin letter, which is marked on the DMD package in the approximate location shown in Figure 2. See the appropriate Hardware and Software ICDs and the electrical reference design schematic for implementation details. The bin letter in Table 6 corresponds to the positive voltage level shown.

Table 6. V_B Bias Voltage Bins

Bin Designation	Min (V)	Max (V)
E	25.5	26.5

Note 10:

See Figure 4. $V_{LVDS} = V_{CM}$ +/- $|1/2V_{ID}|$, where V_{CM} is bounded by the voltage values of V_{LVDS} and $|V_{ID}|$.

Note 11:

To prevent excess current, | VCCI – VCC | should be less than 0.3v

Note 12:

VCC2, VCCI, VCC, and VSS (GND) power supplies are required for all DMD operating modes.

Note 13:

UV light below < 395 nm @ 2mW/cm2 may degrade DMD performance. Consult with TI or TI authorized distributor for applications requiring UV light.

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DMD Marking Locations:

The device marking is shown in Figure 2 below. The marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

Example: *1076-732c GHXXXXX LLLLLLM

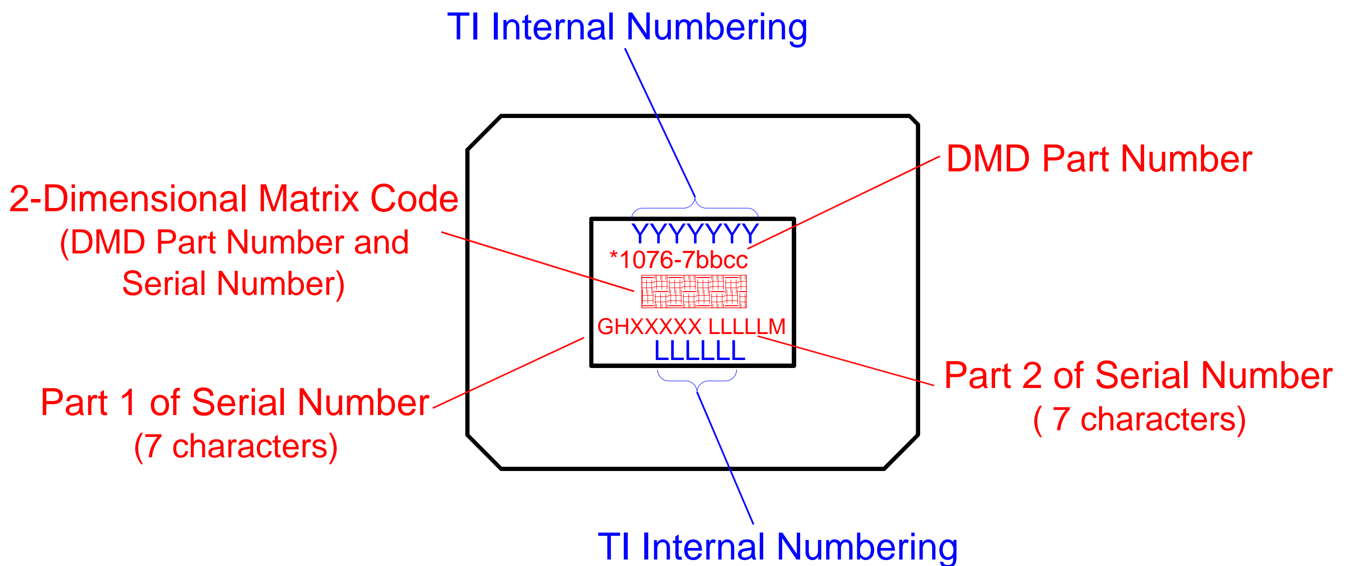

Figure 2. DMD Marking Locations

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Table 7. Electrical Characteristics For Recommended Operating Conditions						
Parameters			Test Condition	Min	Max	Units
V_{OH}	High level output voltage		VCC = 3 V I_{OH} = – 20 mA	2.4		V
V_{OL}	Low level output voltage		VCC = 3.6 V I_{OL} = 15 mA		0.4	V
I_{OZ}	Output high impedance current		VCC = 3.6 V		10	uA
I_{IL}	Low level input current		VCC = 3.6 V V_I = 0		– 60	uA
I_{IH}	High level input current	Note 1	VCC = 3.6 V V_I = VCC		200	uA
I_{CC}	ICC current	Note 2	VCC = 3.6 V		815	mA
I_{CCI}	ICCI current	Note 2	VCCI = 3.6 V		485	mA
I_{CC2}	ICC2 current		VCC2 = 7.8 V		25	mA
	Electrical input power				3.4	W

Note 1:
includes LVCMOS pins only
excludes LVDS pins and MBRST(15:0) pins

Note 2:
To prevent excess current, | VCCI – VCC | should be less than 0.3v

Table 8. Capacitance at Recommended Operating Conditions					
Parameters		Test Condition	Min	Max	Units
C_I	Input Capacitance	f = 1 MHz		10	pf
C_O	Output Capacitance	f = 1 MHz		10	pf
C_{IM}	MBRST(15:0) Input Capacitance	f = 1 MHz all inputs interconnected	220	270	pf

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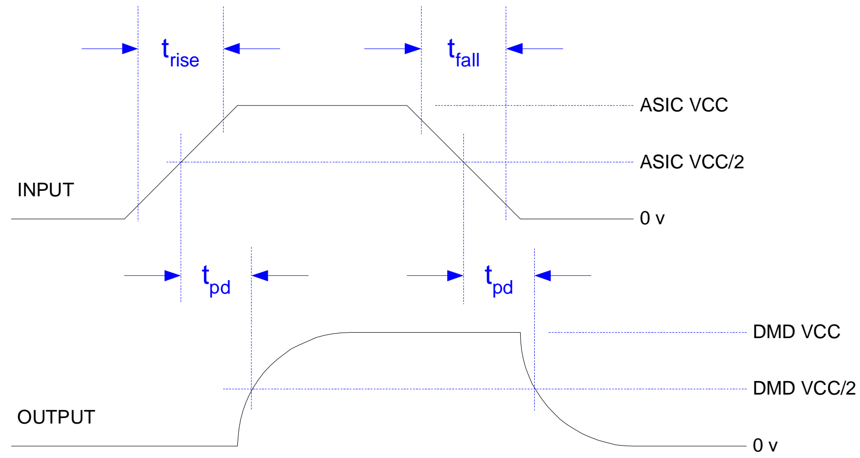
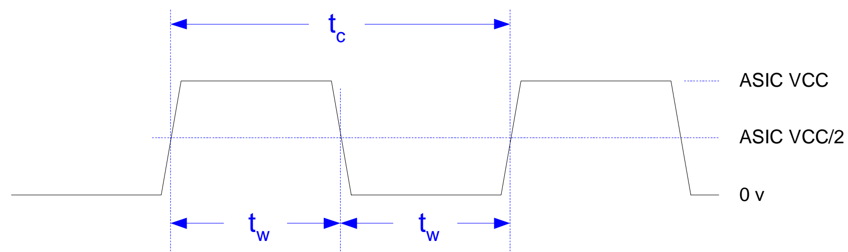
Propagation Time Voltage Waveforms



Switching Voltage Waveforms



Load Circuit

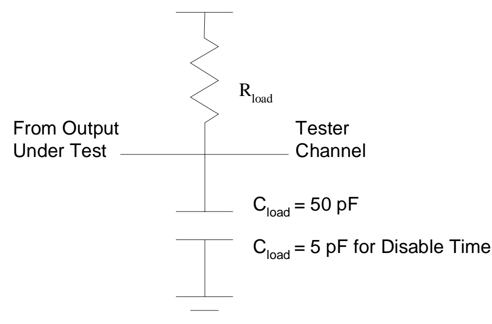


Figure 3. Measurement Conditions

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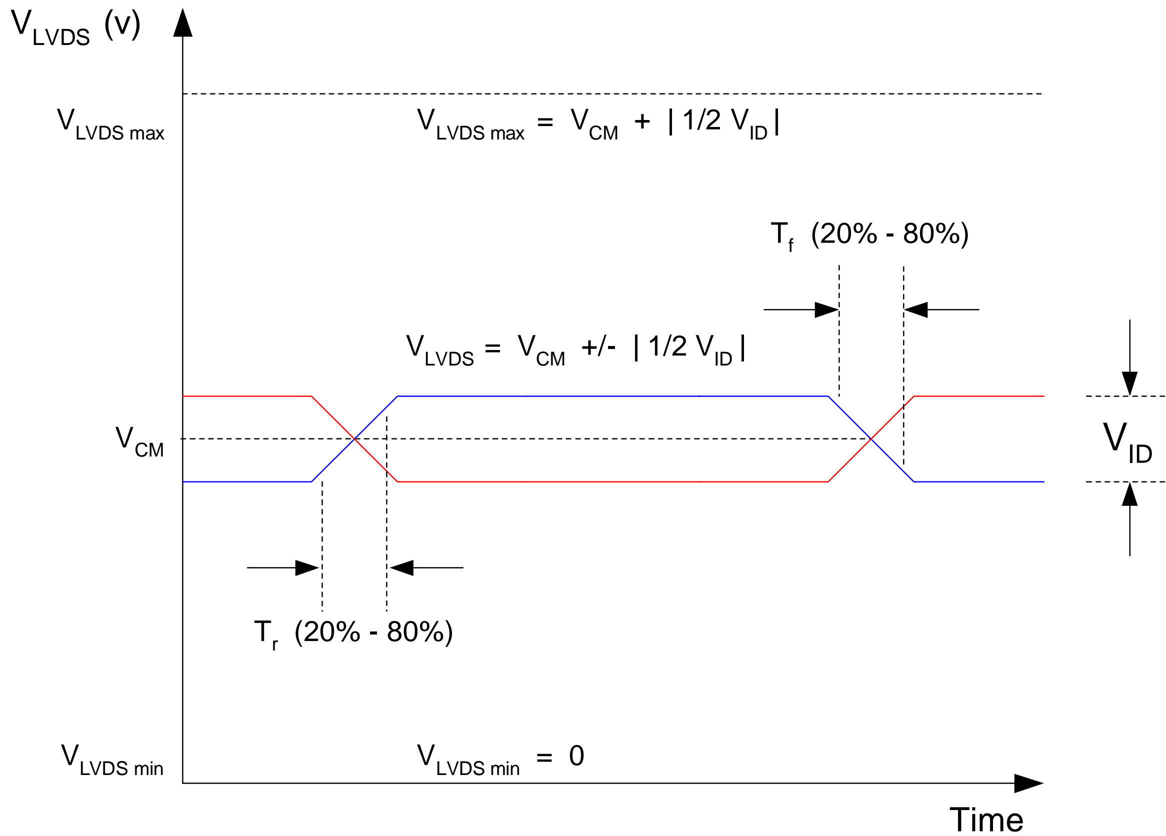

Figure 4. LVDS Waveform Requirements

Note:

Recommended Operating Conditions for V_{CM}, V_{ID}, and V_{LVDS} are listed in Table 5

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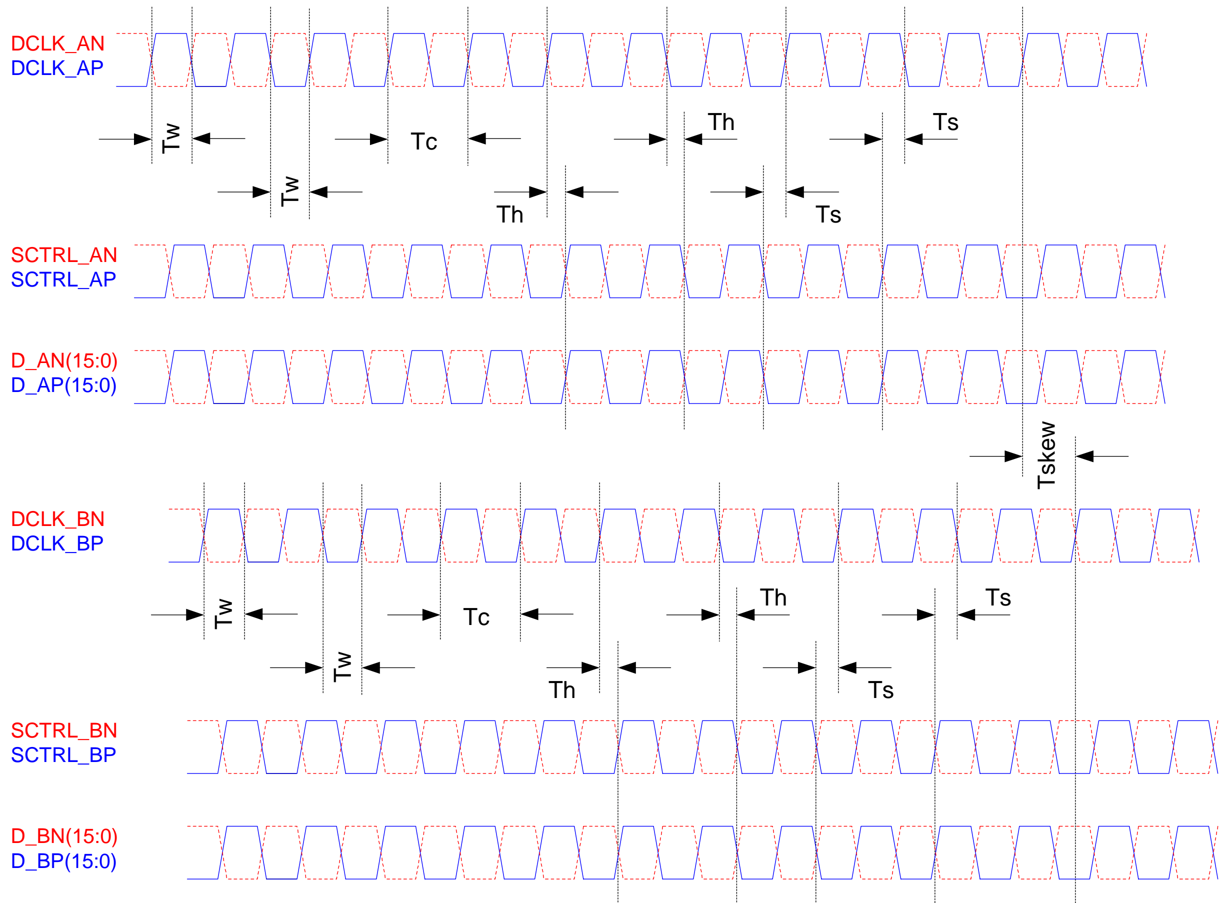

Figure 5. LVDS Critical Timing Waveforms

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Table 9. LVDS Critical Timing							
Parameter				Min	Typ	Max	Units
T_C	Clock Cycle	DCLK_A	LVDS pair	2.5			ns
T_C	Clock Cycle	DCLK_B	LVDS pair	2.5			ns
T_W	Pulse Width	DCLK_A	LVDS pair	1.19	1.25		ns
T_W	Pulse Width	DCLK_B	LVDS pair	1.19	1.25		ns
T_S	Setup Time	D_A(15:0) before DCLK_A	LVDS pair	0.35			ns
T_S	Setup Time	D_B(15:0) before DCLK_B	LVDS pair	0.35			ns
T_S	Setup Time	SCTRL_A before DCLK_A	LVDS pair	0.35			ns
T_S	Setup Time	SCTRL_B before DCLK_B	LVDS pair	0.35			ns
T_H	Hold Time	D_A(15:0) after DCLK_A	LVDS pair	0.35			ns
T_H	Hold Time	D_B(15:0) after DCLK_B	LVDS pair	0.35			ns
T_H	Hold Time	SCTRL_A after DCLK_A	LVDS pair	0.35			ns
T_H	Hold Time	SCTRL_B after DCLK_B	LVDS pair	0.35			ns
T_{SKEW}	Skew Time	Channel B relative to Channel A	LVDS pair	– 1.25		+ 1.25	ns

Channel A (Bus A):

- DCLK_AN
- DCLK_AP
- SCTRL_AN
- SCTRL_AP
- D_AN(15:0)
- D_AP(15:0)

Channel B (Bus B):

- DCLK_BN
- DCLK_BP
- SCTRL_BN
- SCTRL_BP
- D_BN(15:0)
- D_BP(15:0)

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Table 10. Physical Parameters					
Parameter		Min	Nom	Max	Units
Number of Columns			1024		
Number of Rows			768		
Mirror (Pixel) Pitch			13.68		um
Total Width of Active Mirror Array • 1024 pixels			14.008		mm
Total Height of Active Mirror Array • 768 pixels			10.506		mm
Active Array Border	Note 1		POM		
Active Array Border Size			6		mirrors/side

Note 1:

The structure and qualities of the border around the active array includes a band of partially functional mirrors called the “Pond Of Mirrors” (POM). These mirrors are structurally and/or electrically prevented from tilting toward the bright or “on” state but still require an electrical bias to tilt toward “off.”

Table 11. Thermal Parameters					
Parameter		Min	Nom	Max	Unit
Thermal Resistance Active Area to Case	Note 1			0.9	°C/W

Note 1:

The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the specified operational temperatures.

The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.

Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

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Table 12. Optical Parameters					
Parameter		Min	Nom	Max	Unit
Mirror Tilt – half angle Variation device to device	Note 1	11	12	13	Degrees
Axis of Rotation with respect to System Datums Variation device to device	Figure 6	44	45	46	Degrees
DMD Efficiency (420nm – 700nm)	Note 2, 3		68		%
Window Material Designation			Corning 7056		
Window Refractive Index @ 545nm			1.487		
Window Flatness @ 632.8nm spherical power / irregularity (astigmatism, etc)				4 / 2	fringes

Note 1: Mirror Tilt

Mirror tilt angle variations within these limits may be observed across a device and/or from device to device. The specified limits represent the tolerances of the tilt angles within a device.

Note 2:

The minimum or maximum DMD Efficiency observed in a specific application depends upon application-specific variables (such as illumination wavelength, illumination bandwidth, illumination coherence, etc.) as well as system-design variables (such as illumination angle, illumination and collection aperture size, aberrations in illumination and collection optics, optical overfill, etc.).

The DMD Efficiency specified here is a nominal value, and is based on the following assumptions which are derived from a typical consumer projection system:

- Light Source: broadband visible (420nm – 700nm)
- Illumination Angle: 24 degrees (relative to the window normal)
- Collection Angle: 0 degrees (relative to the window normal)
- Illumination Aperture: f/3.0
- Collection Aperture: f/2.4

The overall DMD Efficiency is a function of the following four components:

1) Fill Factor – Approximately 92.5%
2) Diffraction Efficiency – Approximately 86% for broadband visible (420nm-700nm) light.
3) Mirror Reflectivity – Approximately 88% for broadband visible (420nm-700nm) light.
4) Window Transmission – Approximately 97% for broadband visible (420nm-700nm) light.
   a) Assumes that the angle of incidence is 0° - 45° at 420-700nm, and each AR coated surface has ~.5% reflectivity.
   b) 4 passes of light through the AR coating results in ~97% efficiency. (e.g. 2 passes into the DMD, and 2 passes out of the DMD)

Note 3:

DMDs can be optimized for Ultraviolet (UV) or Near Infrared (NIR) applications. For information related to the DMD efficiency for these devices please contact TI Application engineer or DLP Discovery website for additional application notes.

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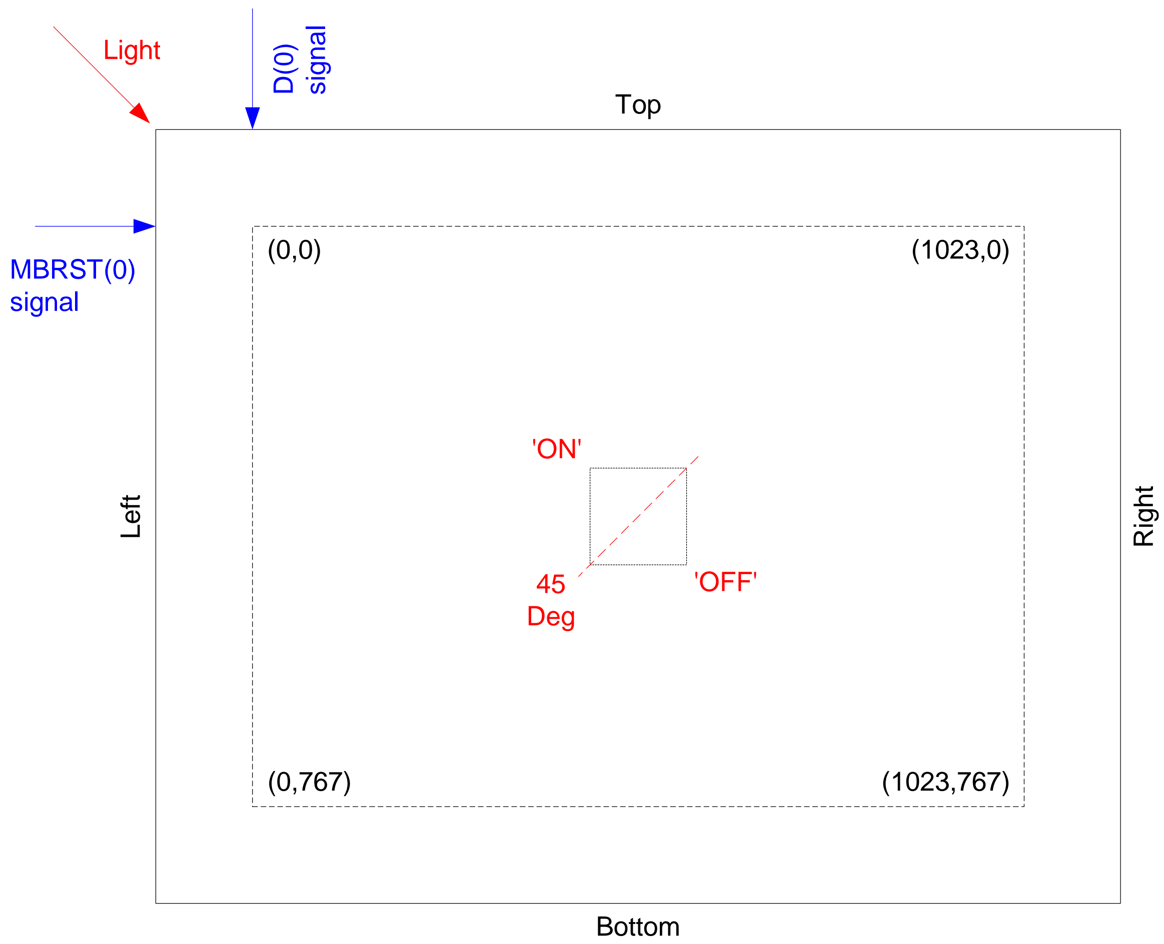

Figure 6. Mirror Tilt Axis Orientation

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Table 13. Optical Interface and System Image Quality					
Parameter		Min	Nom	Max	Unit
	Note 1				

Note 1:

Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in a) through c) below:

a) Numerical Aperture and Stray Light Control.
The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

b) Pupil Match.
TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

c) Illumination Overfill.
The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the area outside the active array can create artifacts from the mechanical features that surround the active array and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere outside the active array more than 20 pixels from the edge of the active array on all sides. Depending on the particular system's optical architecture and assembly tolerances, this amount of overfill light on the outside of the active array may still cause artifacts to still be visible.

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED ABOVE.

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Type A package mechanical dimensions and tolerances are shown in the DMD Mechanical ICD drawing referenced in Table 1.

Table 14. System Interface Parameters

Parameter		Min	Nom	Max	Unit
Maximum Load to be Applied to the	Figure 7				
• Thermal Interface area				25	lbs
• Electrical Interface area				95	lbs
• Datum "A" Interface area	Note 1			90	lbs

Note 1:

Combined loads of the thermal and electrical interface areas in excess of the Datum "A" load shall be evenly distributed outside the Datum "A" area (95 + 25 – Datum "A"). Refer to Figure 7 for package system interface load diagrams

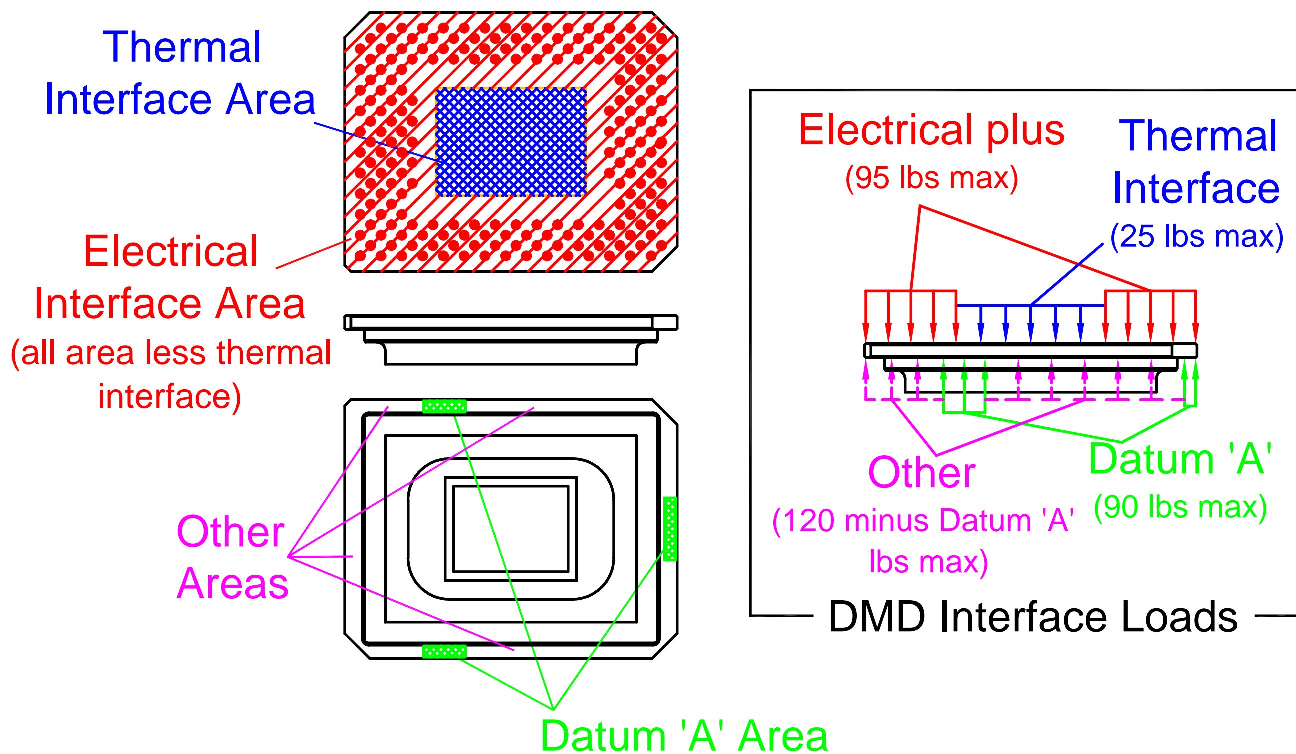

Figure 7. System Interface Loads

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Table 15. DMD Type A Package Pins

Pin ID	Pin Name	Net Lengths (mil) – Note 1
A1	VSS	
A3	VSS	
A5	VSS	
A7	VCC	
A9	VSS	
A11	D_AP(1)	417.47
A13	D_AN(1)	424.61
A15	VCC	
A17	D_AN(5)	391.13
A19	D_AP(5)	389.01
A21	VCCI	
A23	D_AP(6)	562.92
A25	D_AN(6)	563.26
A27	VCCI	
A29	D_AP(8)	594.61
B2	SCPDO	480.91
B4	VSS	
B6	RESERVED_STM	544.28
B8	VSS	
B10	D_AN(0)	368.72
B12	D_AP(0)	366.99
B14	VSS	
B16	D_AP(4)	437.30
B18	D_AN(4)	438.57
B20	VSS	
B22	DCLK_AN	477.10
B24	DCLK_AP	477.11
B26	VSS	
B28	D_AP(9)	539.88
B30	VSS	
C1	VCC	
C3	PWRDNZ	406.28
C5	RESERVED_TS	325.27
C7	VSS	
C9	RESERVED_BB	360.40
C11	MODE_B	208.86
C13	VSS	
C15	D_AP(3)	394.67
C17	D_AN(3)	391.39
C19	VSS	
C21	SCTRL_AN	477.07
C23	SCTRL_AP	477.14
C25	VSS	
C27	D_AP(10)	456.78
C29	D_AN(8)	595.11

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Table 15. DMD Type A Package Pins		
Pin ID	Pin Name	Net Lengths (mil) – Note 1
D2	RESERVED_XI1	695.06
D4	SCPENZ	326.99
D6	VSS	
D8	MODE_A	396.05
D10	RESERVED_RB1	313.78
D12	VSS	
D14	D_AP(2)	434.89
D16	D_AN(2)	433.87
D18	VSS	
D20	D_AP(7)	410.34
D22	D_AN(7)	411.62
D24	VSS	
D26	D_AP(11)	360.68
D28	D_AN(9)	543.07
D30	VCCI	
E1	VCC	
E3	SCPCLK	379.29
E5	RESERVED_RB0	457.18
E27	D_AN(10)	455.98
E29	VSS	
F2	VSS	
F4	SCPDI	323.56
F26	D_AN(11)	359.50
F28	VSS	
F30	D_AP(12)	543.97
G1	VCC2	
G3	VSS	
G5	RESERVED_XO1	830.18
G27	VSS	
G29	D_AN(12)	542.67
H2	VSS	
H4	VSS	
H6	EVCC	
H26	VSS	
H28	D_AN(13)	551.51
H30	D_AP(13)	570.85
J1	VCC2	
J3	VSS	
J5	MBRST(13)	876.96
J25	VSS	
J27	D_AN(14)	528.04
J29	D_AP(14)	527.18
K2	VSS	
K4	MBRST(9)	813.88
K6	MBRST(14)	753.35

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Table 15. DMD Type A Package Pins		
Pin ID	Pin Name	Net Lengths (mil) – Note 1
K26	D_AN(15)	484.38
K28	D_AP(15)	481.02
K30	VSS	
L1	VCC2	
L3	MBRST(7)	941.20
L5	MBRST(10)	742.95
L25	VSS	
L27	VSS	
L29	VSS	
M2	VSS	
M4	MBRST(4)	1092.91
M6	VSS	
M26	VSS	
M28	VSS	
M30	VCCI	
N1	VCC2	
N3	MBRST(3)	926.71
N5	VSS	
N25	VSS	
N27	D_BN(15)	441.14
N29	VSS	
P2	MBRST(0)	1225.87
P4	VSS	
P6	RESERVED_TP1	512.15
P26	D_BP(15)	440.00
P28	D_BP(14)	534.59
P30	VSS	
R1	VCC2	
R3	VSS	
R5	VSS	
R25	VSS	
R27	D_BN(14)	532.59
R29	D_BN(13)	519.37
T2	VSS	
T4	RESERVED_FD	483.09
T6	EVCC	
T26	VSS	
T28	D_BP(13)	509.74
T30	D_BN(12)	575.85
U1	VCC	
U3	RESERVED_BA	650.26
U5	RESERVED_FC	323.10
U27	VSS	
U29	D_BP(12)	578.46

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Table 15. DMD Type A Package Pins		
Pin ID	Pin Name	Net Lengths (mil) – Note 1
V2	RESERVED_XI3	
V4	RESERVED_XI2	346.33
V26	D_BN(11)	360.94
V28	VSS	
V30	VSS	
W1	VCC	
W3	RESERVED_TP2	687.22
W5	VSS	
W27	D_BN(10)	455.98
W29	VSS	
Y2	RESERVED_TP0	744.46
Y4	VSS	
Y6	MBRST(8)	458.84
Y8	MBRST(12)	377.26
Y10	RESERVED_RA1	302.99
Y12	VSS	
Y14	D_BP(2)	434.89
Y16	D_BN(2)	433.87
Y18	VSS	
Y20	D_BP(7)	410.34
Y22	D_BN(7)	411.62
Y24	VSS	
Y26	D_BP(11)	360.68
Y28	D_BN(9)	543.07
Y30	VCCI	
AA1	RESERVED_PFE	477.72
AA3	VSS	
AA5	MBRST(6)	1186.57
AA7	MBRST(2)	1306.01
AA9	VSS	
AA11	RESERVED_XO2	261.14
AA13	VSS	
AA15	D_BP(3)	394.67
AA17	D_BN(3)	391.39
AA19	VSS	
AA21	SCTRL_BN	477.07
AA23	SCTRL_BP	477.14
AA25	VSS	
AA27	D_BP(10)	456.78
AA29	D_BN(8)	595.11
AB2	VCC	
AB4	MBRST(1)	1277.24
AB6	MBRST(5)	1238.86
AB8	VSS	
AB10	D_BN(0)	368.72
AB12	D_BP(0)	366.99

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Table 15. DMD Type A Package Pins		
Pin ID	Pin Name	Net Lengths (mil) – Note 1
AB14	VSS	
AB16	D_BP(4)	437.30
AB18	D_BN(4)	438.57
AB20	VSS	
AB22	DCLK_BN	477.10
AB24	DCLK_BP	477.11
AB26	VSS	
AB28	D_BP(9)	539.88
AB30	VSS	
AC3	RESERVED_RA0	826.38
AC5	MBRST(11)	824.02
AC7	MBRST(15)	749.82
AC9	VCC	
AC11	D_BP(1)	417.47
AC13	D_BN(1)	424.61
AC15	VCC	
AC17	D_BN(5)	391.13
AC19	D_BP(5)	389.01
AC21	VCCI	
AC23	D_BP(6)	562.92
AC25	D_BN(6)	563.26
AC27	VCCI	
AC29	D_BP(8)	594.61

Note 1: Use 260 ps/in propagation delay for the DMD Type A ceramic package trace lengths.

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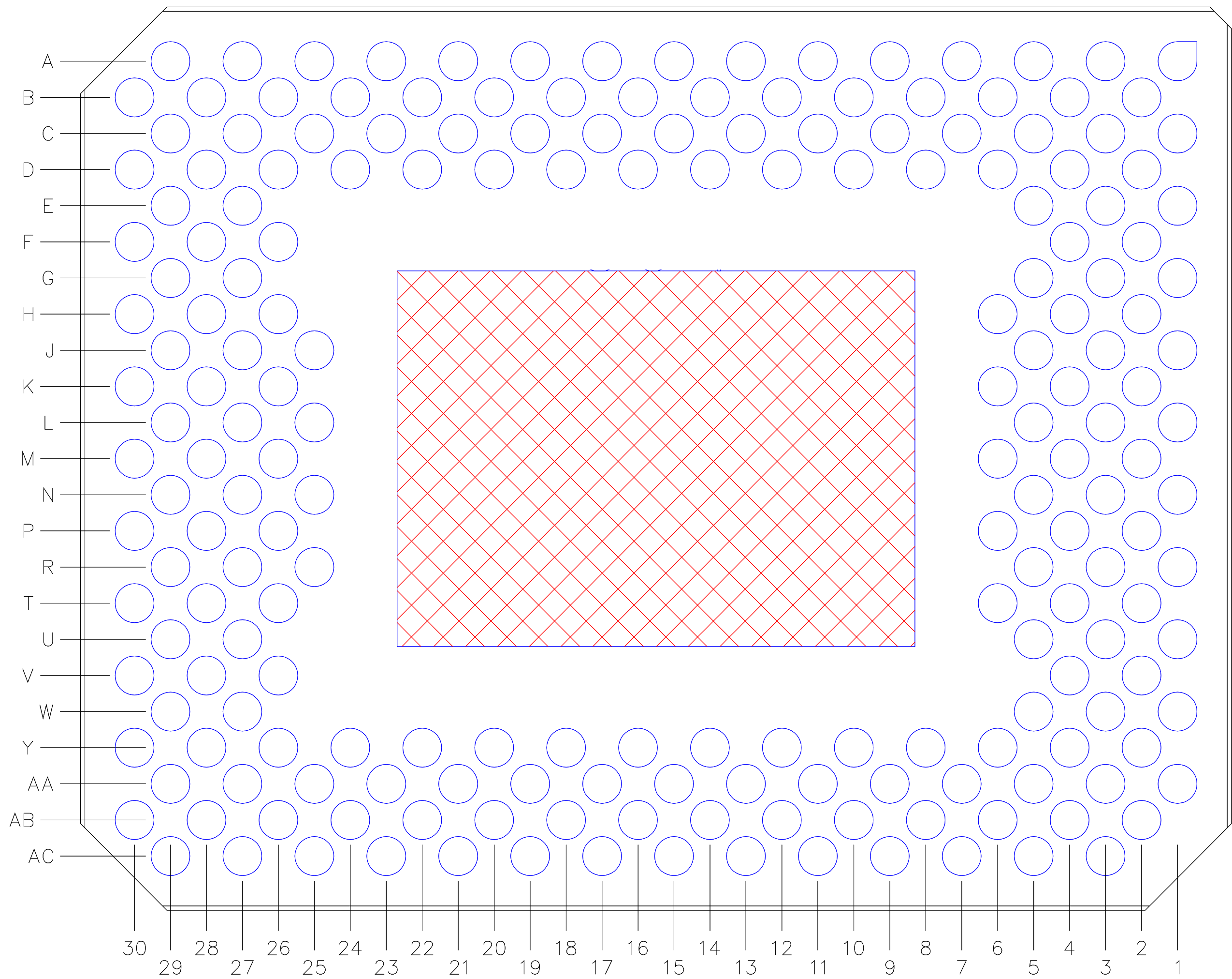

Figure 8. Package Pins – Bottom View

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Electrostatic Discharge Immunity:

All external signals on the DMD are protected from damage by electrostatic discharge, and are tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).

Table 16. DMD ESD Protection Limits

Package Pin Type	Voltage (maximum)	Units
Input	2000	V
Output	2000	V
Power	2000	V
MBRST(15:0)	< 250	V

Notes on Handling:

All CMOS devices require proper Electrostatic Discharge (ESD) handling procedures.

Refer to drawing # 2504641 DMD Handling Specification, for precautions to protect the DMD from ESD and to protect the DMD’s glass and electrical contacts.

Refer to drawing # 2504640 DMD Glass Cleaning Procedure, for correct and consistent methods for cleaning the glass of the DMD, in such a way that the anti reflective coatings on the glass surface are not damaged.

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