



TEXAS INSTRUMENTS

TI DN 2510510 Rev A
May 2009

DLP® Pico MAIN-B SCHEMATIC

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Reference

1. DLP® Pico Kit Functional Guide, TI drawing number 2510476
2. DLP® Pico Chipset Interface Manual, TI drawing number 2510477
3. DLP® Pico DVI-B SCHEMATIC, TI drawing number 2510511
4. DLP® Pico DMD-B SCHEMATIC, TI drawing number 2510512
5. DLP® Pico Geber MAIN BOARD, TI drawing number 2510513
6. DLP® Pico Geber DVI BOARD, TI drawing number 2510514
7. DLP® Pico Geber DMD CONTROL BOARD, TI drawing number 2510515

DLP® Pico Kit main board schematic

For a reference of the DLP® Pico Kit main board schematic see the design file, ***TI2510510_L9502G001_MAIN-B_SCHEMATIC_D02_12222008.DSN***. This file contains the schematic information for the Pico Kit main board.

How do I get the design file?

The design file for the DLP® Pico Kit main board schematic is available to you through an authorized DLP® Discovery™ value-added reseller (VAR). A list of the VARs can be found at: www.dlpdiscovery.com/var. Please reference the file name above when contacting a VAR.

Content :

P01_Content

P02_Block_Diagram

P03_FPGA_I/O_1

P04_FPGA_I/O_2

P05_FPGA_Power&Memory

P06_External_Connector

P07_DMD_REG

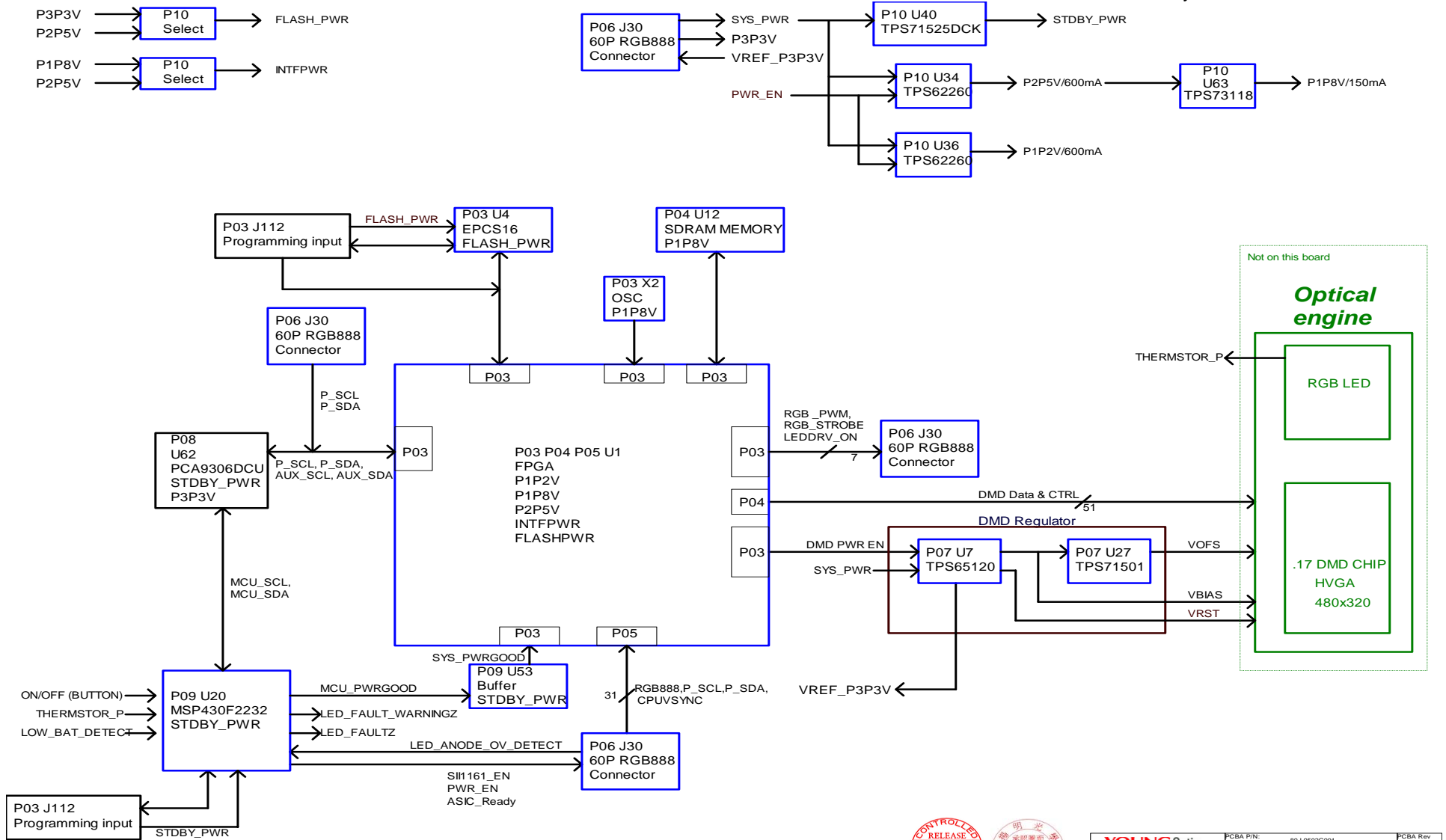
P08_I2C_Level_Shift

P09_MCU

P10_Power

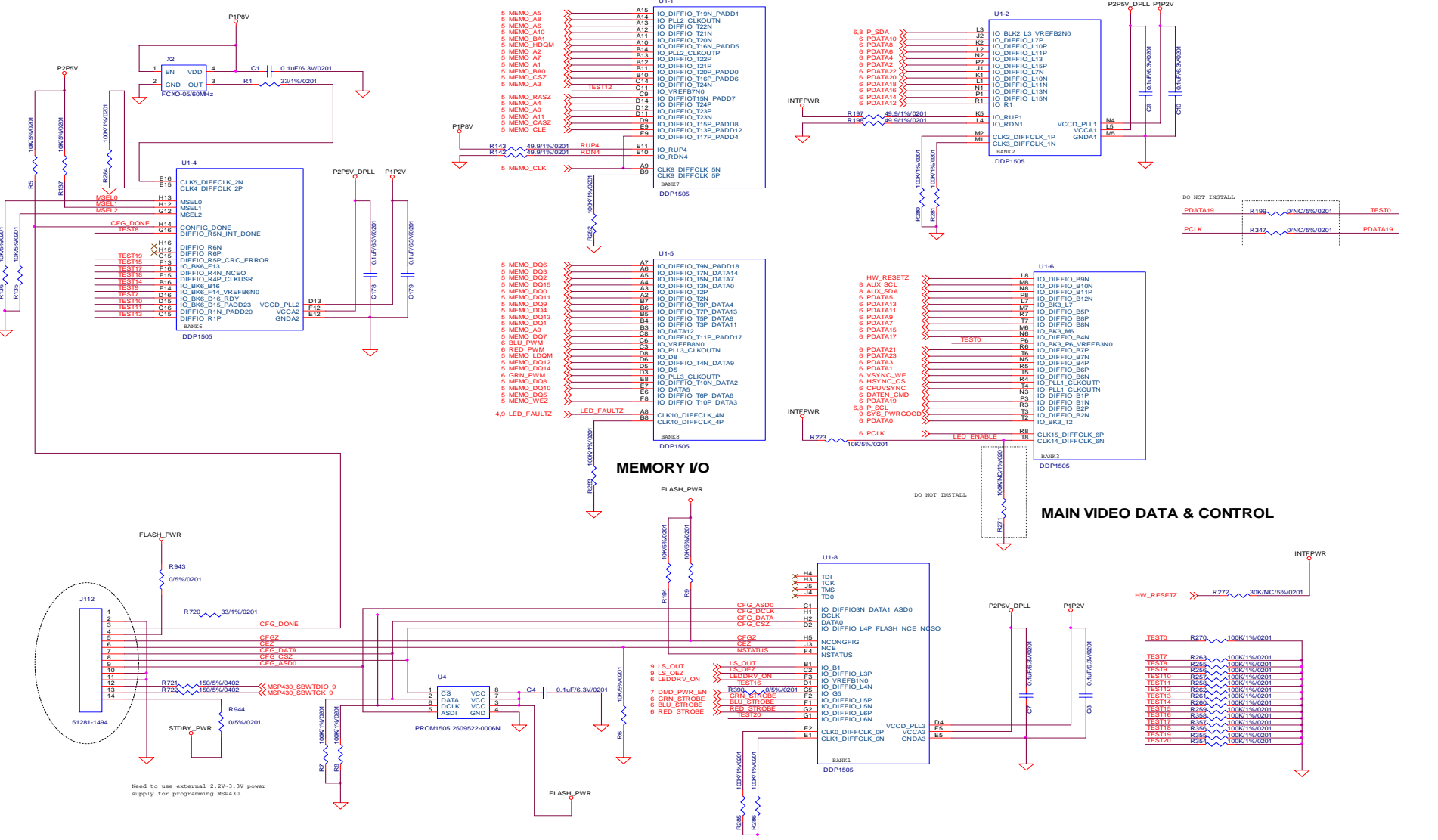


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Approver	Designer	Draw er	Title	
Daniel	Larry	Larry	Content	
			Size C	Rev A
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Approver:	Designer:	Draw er:	Title:		
Daniel	Larry	Larry	Block Diagram		
			Size:	Plotting Number:	Rev:
			C:	PLD	A
			Date:	Issue Date:	Sheet:
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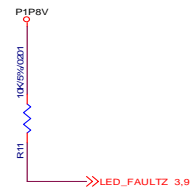
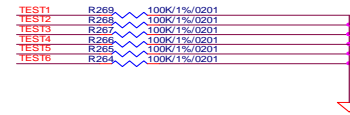
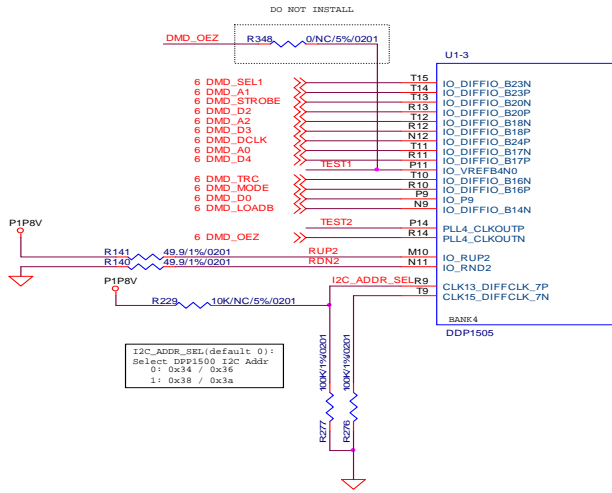
01-04-098TLF1 Ver. A



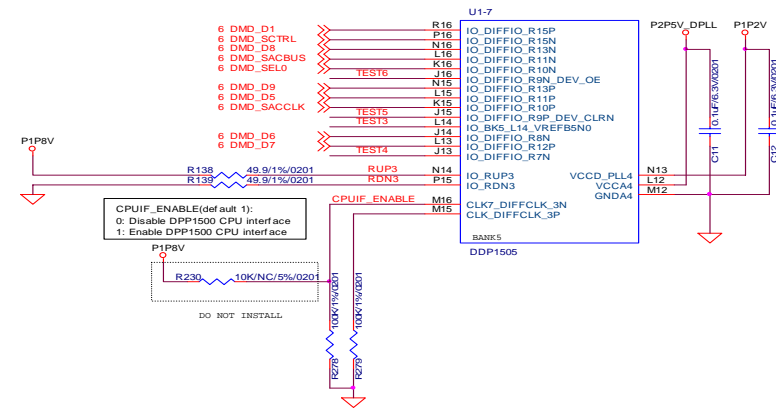
Need to use external 0.2V-3.3V power supply for programming MSP430.



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Approver:	Designer:	Draw er:	Title:	FPGA U/I-1/2	Rev:	A
Daniel	Larry	Larry	Size:	Document Number	File:	0
			Date:	Tuesday, May 19, 2009	Sheet:	3 of 10
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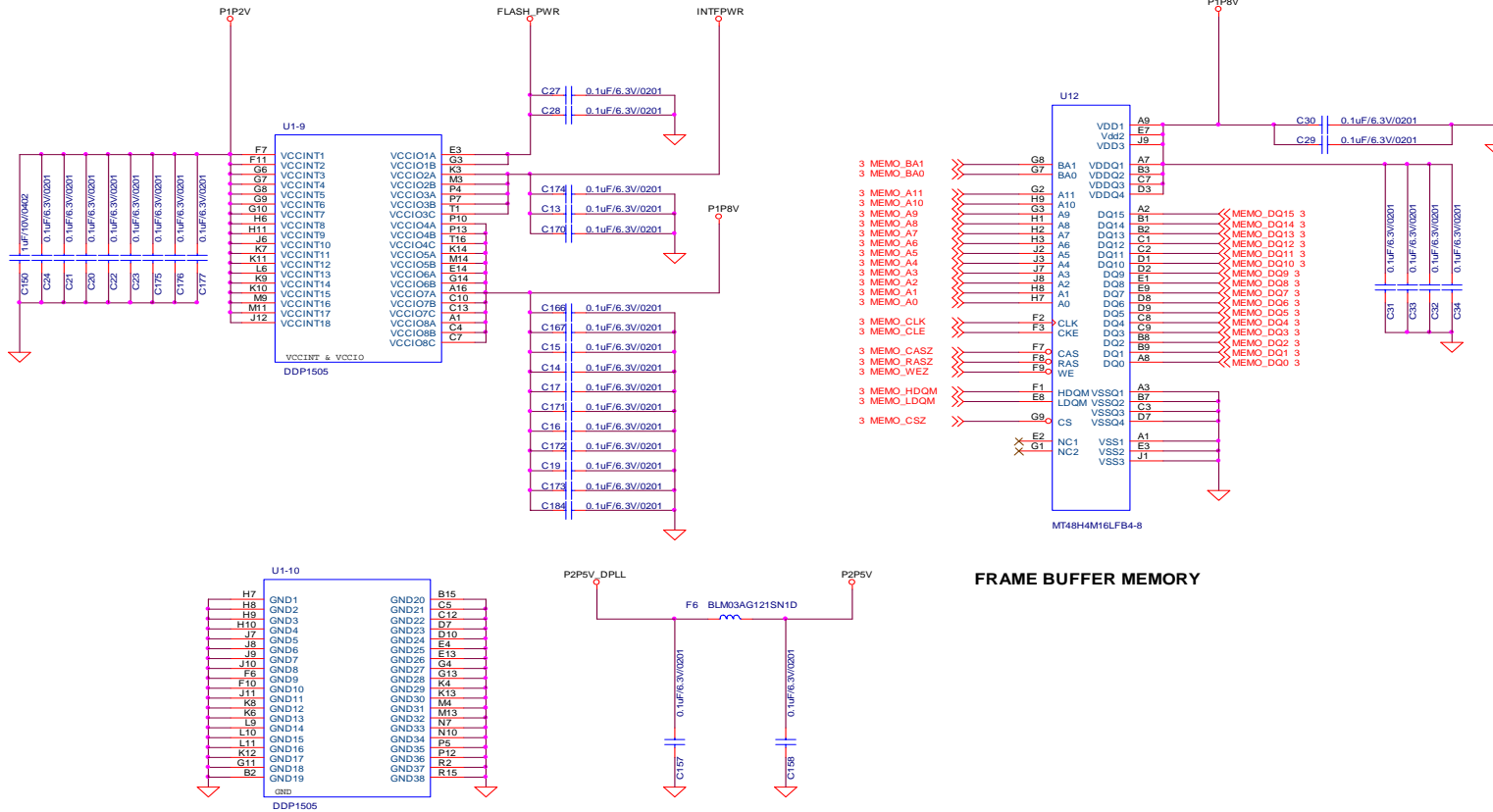
If U51 is not installed
LED_FAULTZ must be pulled
up at the DPP1500 input.



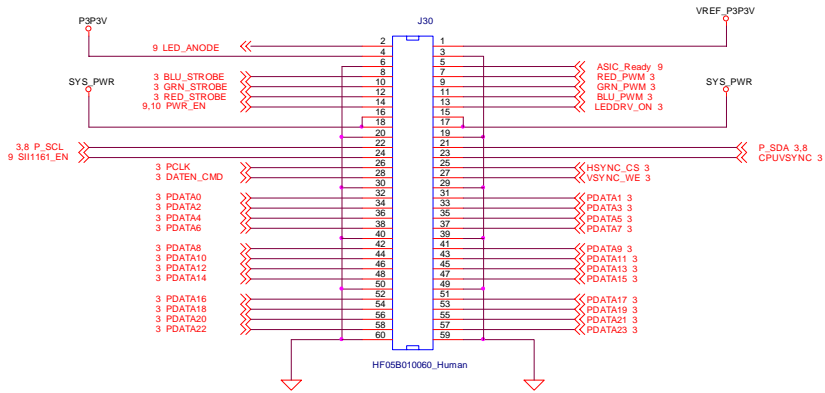
DMD I/O



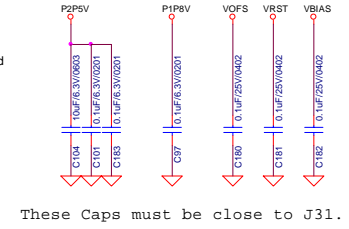
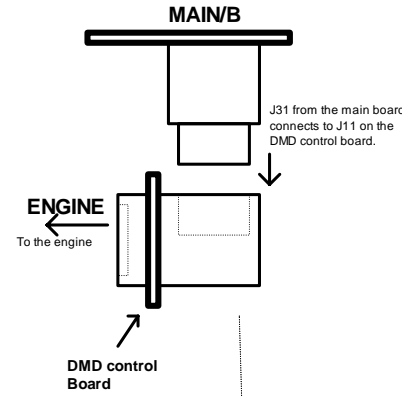
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Approver	Designer	Draw er	Title	
Daniel	Larry	Larry	FPGA I/O 2/2	
Size	Document Number	Rev	A	
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01-04-00BTLF1 Ver.A				



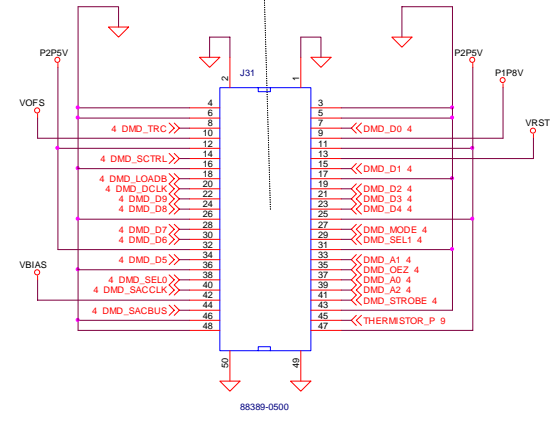
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Approver	Designer	Drawer	Title: FPGA Power & Memory	
Daniel	Larry	Larry	Size: Document Number	Rev: A
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VIDEO CONNECTION



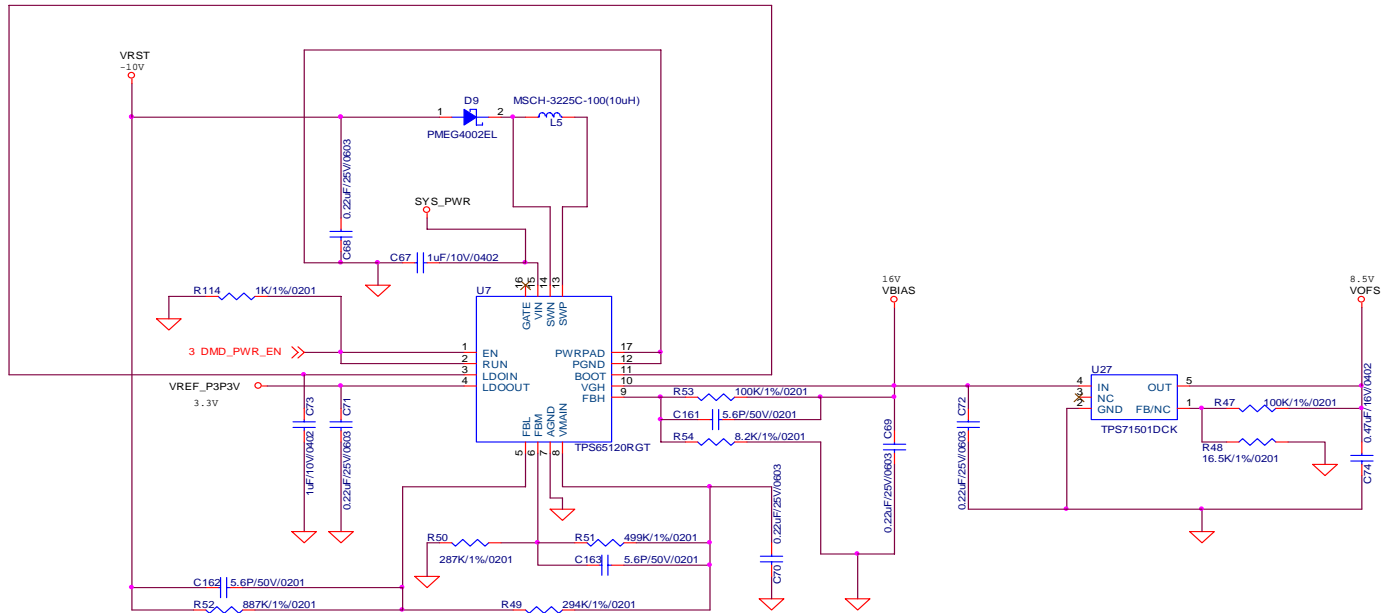
These Caps must be close to J31.



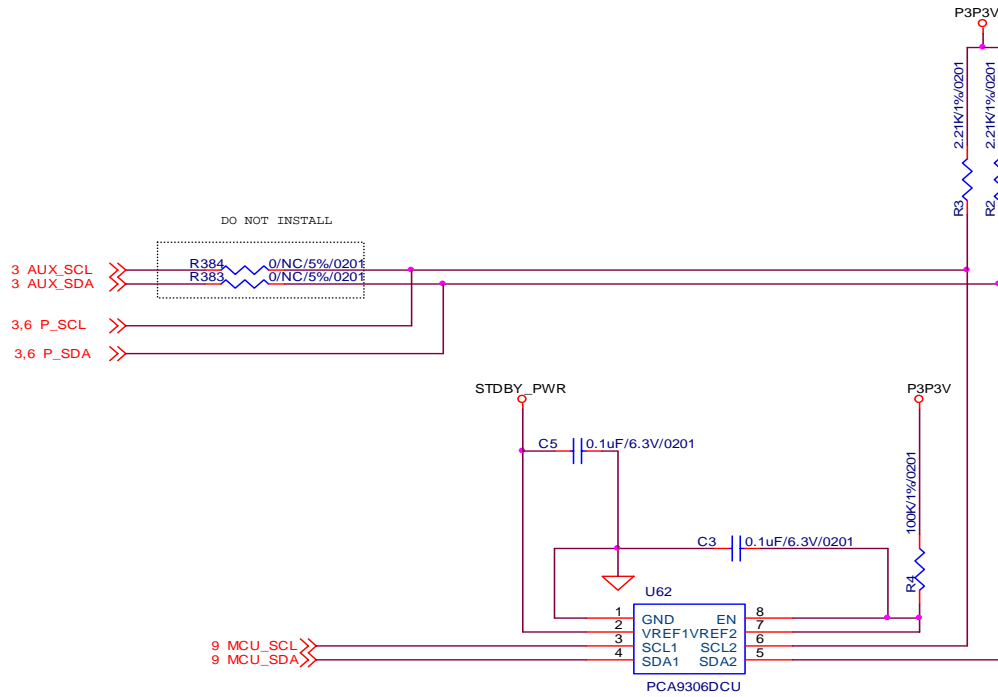
To DMD



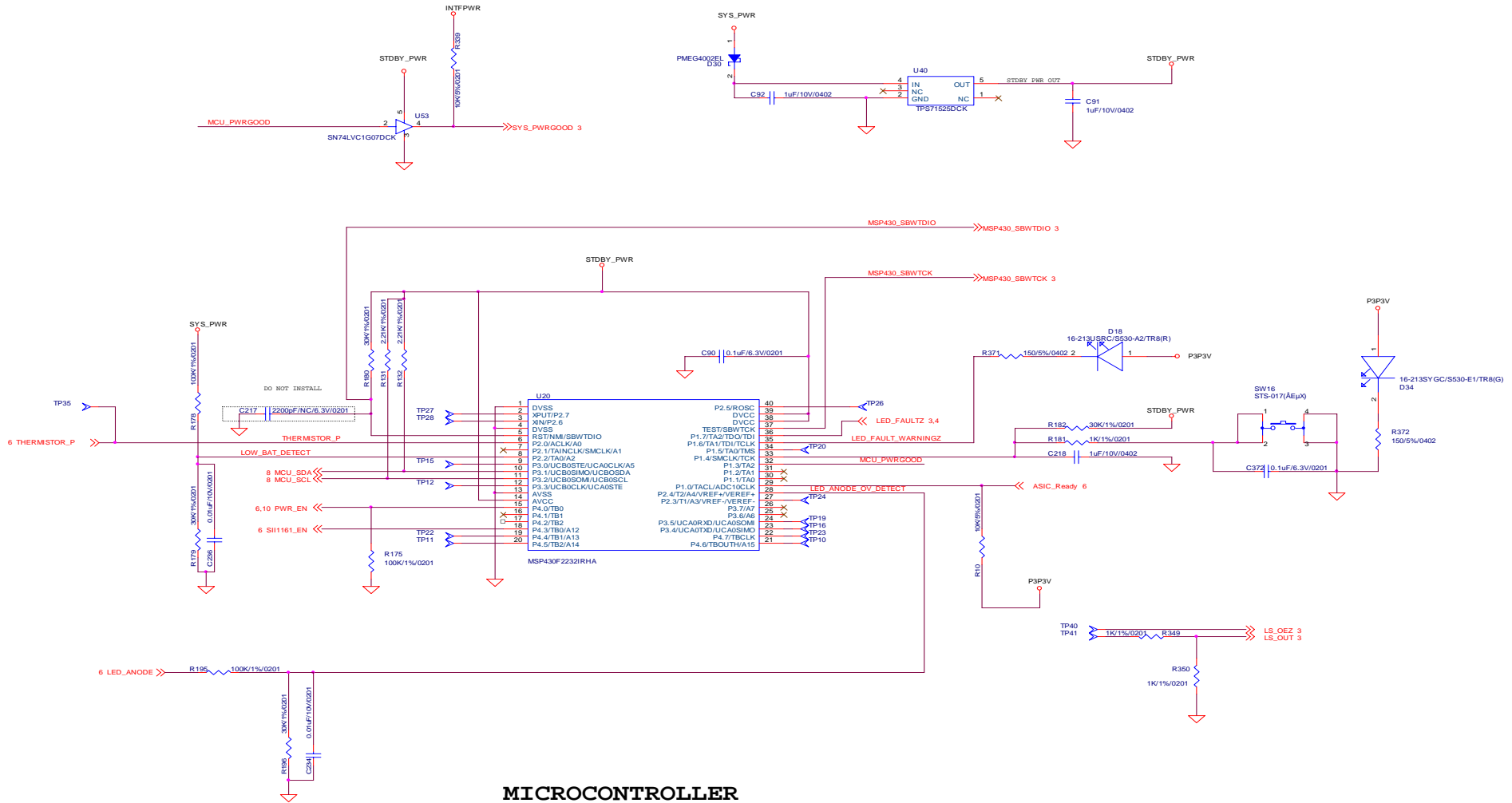
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Approver	Designer	Draw er	Title: External Connector	
Daniel	Larry	Larry	Size: Document Number	
			Date: Tuesday, May 19, 2009	
			Sheet 6 of 10	
			01-04-0081P1 Ver A	



YOUNG Optics			PCBA P/N:	80.L9502G001	PCBA Rev	B
			PCB P/N:	00.L9502G001	PCB Rev	D
Approver	Designer	Draw er	Title			
Daniel	Larry	Larry	DMD REG			
Size	Document Number				Rev	
C	FLD				A	
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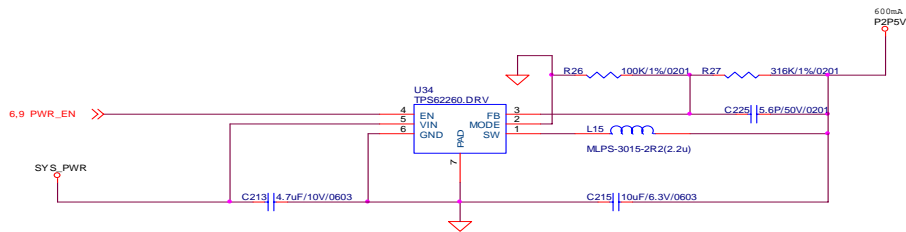
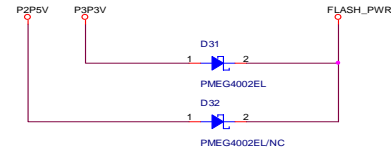
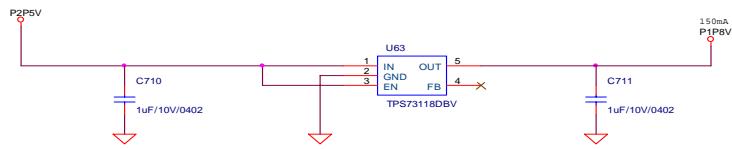
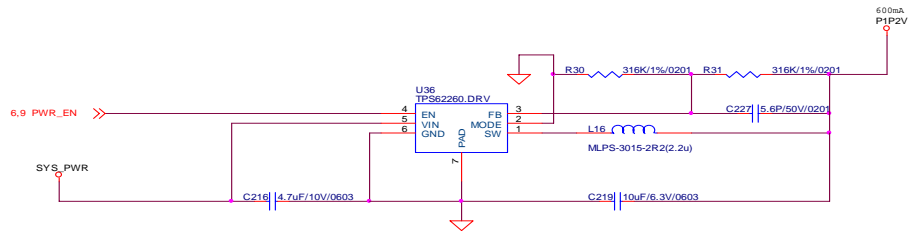
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Approver	Designer	Drawer	Title			
Daniel	Larry	Larry	I2C Level Shift			
Size	Document Number				Rev	A
C	FLD					
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MICROCONTROLLER



YOUNG Optics			PCBA P/N: 80.L9502G001	PCBA Rev B
Approver	Designer	Draw er	PCB P/N: 00.L9502G001	PCB Rev D
Daniel	Larry	Larry	Title: MCU	Rev A
Size: C	Document Number: ELD	Date: Tuesday, March 31, 2009	Sheet 9 of 10	Rev A



YOUNG Optics			PCBA P/N:	80.L9502G001	PCBA Rev	B
Approver	Designer	Drawer	PCB P/N:	00.L9502G001	PCB Rev	D
Daniel	Larry	Larry	Title	Power	Rev	A
			Size	Document Number	FLD	
			Date:	Tuesday, March 31, 2009	Sheet	10 of 10
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