

introducing +12 V to the control gate (with grounded source), which helps accelerate electrons in the source through the channel toward the floating gate. The internal charge pump is utilized for this operation also. An internal Write State Machine (WSM) automatically executes the timing and algorithms necessary for programming and erasure [7]. Both the erase and write operations require a much longer time than the read timer, which is comparable to that of an SDRAM.

After an erasure, the cell is designed to hold a logic “1” state, while a written (or programmed) cell provides a logic “0” state in this family. In order to accomplish the erase, write, and read operations, a device is made up of various control sections as well as the memory section, as shown in Figure 3.

TEST METHOD

It has been expected that upsets may occur at various sections in a die in addition to the memory section (see Figures 1 and 3.) Therefore, SEE may encompass single event upset (SEU), single event latchup (SEL), single event transient (SET), and single event functional interrupt (SEFI) [10]. While running the test, the upset rate was kept below about 10 events per second. This made the dead time caused by controlling the device under test negligible compared to the total test time. After a sufficient number of errors had been recorded, the test was stopped and the total fluence of particles and total number of errors were recorded. The device error probability for each type of upset or cross-section, σ is calculated from the expression

$$\sigma = (N/F) \sec \theta$$

where N and F are the number of errors and beam fluence, respectively, and θ is the incident angle of the beam measured with respect to the chip-surface normal. We have used various ion species including protons available at the Lawrence Berkeley Laboratory 88-inch cyclotron. Characteristics of some of these ions are shown in Table 2.

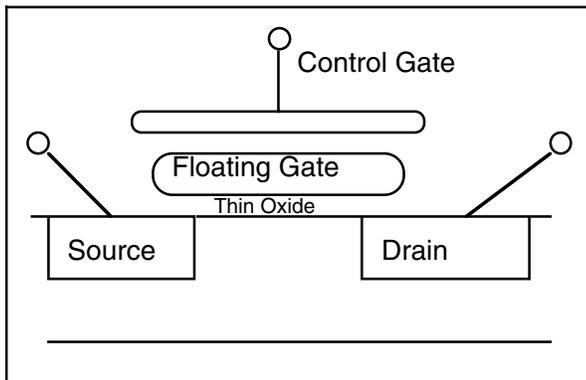


Figure 2. Schematic of a flash memory cell

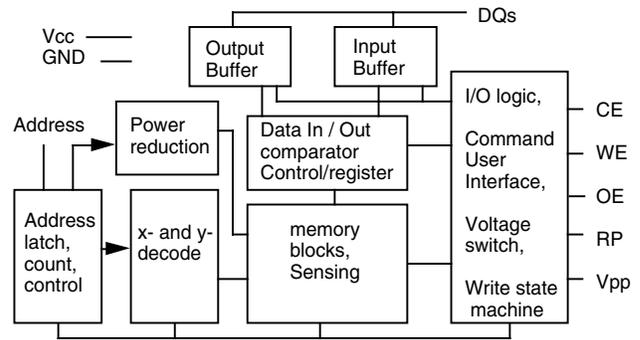


Figure 3. Functional block diagram of flash memory.

TABLE 2. SAMPLES OF LBNL 4.5 MEV/NUCLEON AND 10 MEV/NUCLEON HEAVY ION COCKTAIL BEAMS

IONS	AMU	Energy (MeV)	LET [MeV/(mg/cm²)]	Range in Si (μm)
B	10	45	1.5	80
Ne	20	90	5.6	50
Ne	20	214	3.2	190
Ar	40	180	15	45
Kr	86	387	41	46
Xe	136	1471	53	115
Bi	209	950	95	50

TEST RESULTS

We show test results for FIFO memories followed by those for flash memories.

A. FIFO Memory Sensitivities to SEE

We observed upsets, which most likely occurred in the memory section. These are shown as SEU in Figures 4, 5, and 6 for IDT, TI, and HBA devices, respectively. The saturation cross-section is somewhere between 1×10^{-7} and 1×10^{-6} cm²/bit for IDT and TI devices. HBA devices were very sensitive to latchup at high LET regions. Therefore, we could not obtain SEU cross-sections at high LET values. The threshold LET values are relatively low. Most SEUs are of “one-bit error/word” type. However, IDT devices showed some sensitivity to “two-bit error/word” type. Weibull curve fits to heavy ion SEU cross-sections have been made. The coefficients for the two SEU curves are shown in Table 3.

TABLE 3. WEIBULL PARAMETERS FOR TWO SEU TEST SAMPLE TYPES

Device type	Onset	Power	Width	Limit
IDT	1.4	1.65	25	8×10^{-7}
TI	0.99	0.85	7	1×10^{-7}

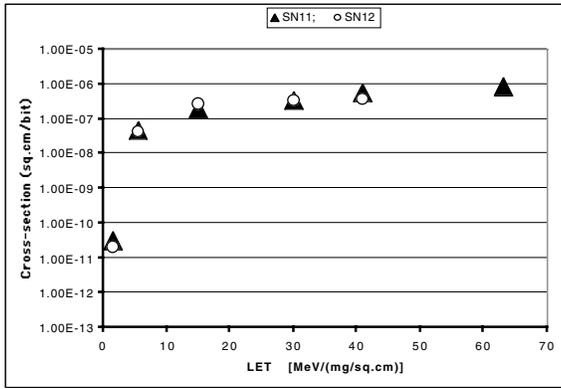


Figure 4. SEU results for IDT FIFO.

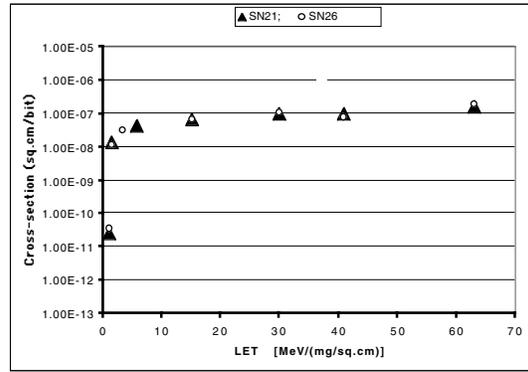


Figure 5. SEU results for TI FIFO.

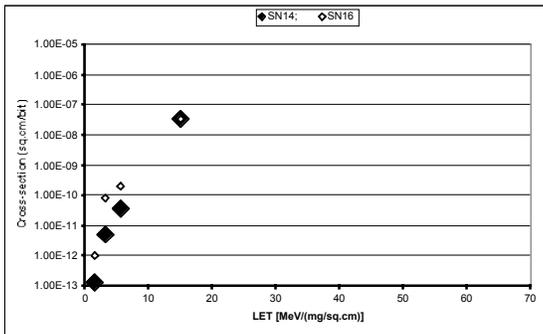


Figure 6. SEU results for HBA FIFO.

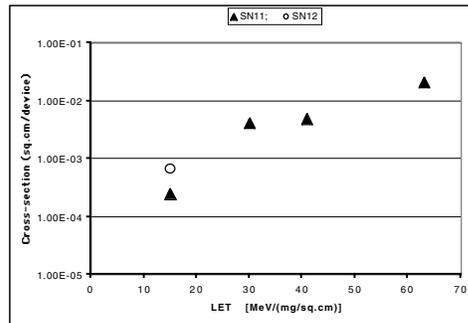


Figure 7. SEFI results for IDT FIFO.

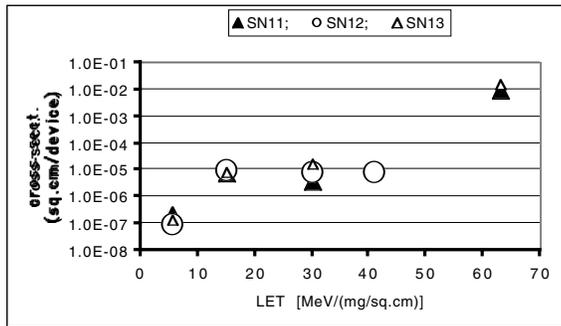


Figure 8. SEL results for IDT FIFO.

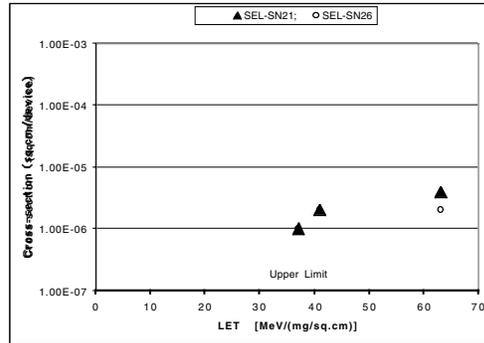


Figure 9. SEL results for TI FIFO.

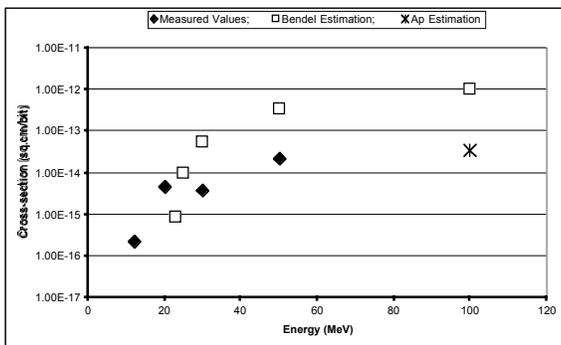


Figure 10. Proton induced SEU sensitivity for IDT FIFO. Measured and estimated values are shown.

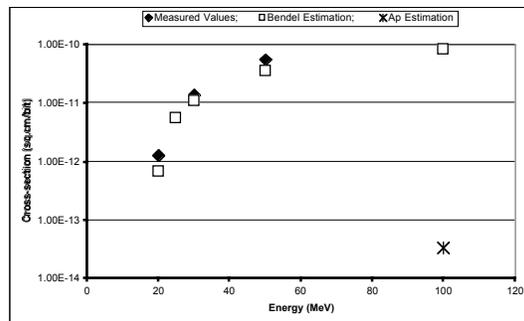


Figure 11. Proton induced SEU sensitivity for TI FIFO. Measured and estimated values are shown.

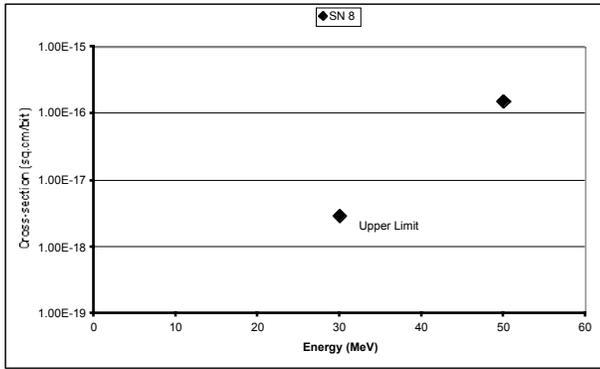


Figure 12. Proton induced SEU sensitivity for HBA FIFO.

Some devices such as the IDT FIFO are sensitive to SEFI (single event functional interrupt) as shown in Figure 7. Upon encountering SEFI, the device output often shows unusual patterns such as “all 0’s” or “all 1’s” for consecutive address locations. IDT FIFO showed a relatively high sensitivity to SEL as compared with TI devices as shown in Figures 8 and 9, respectively. The SEL current often exceeded 100 mA.

Proton irradiation was carried out at the LBL 88-inch cyclotron soon after heavy ion irradiation. We used 12, 20, 30, and 50 MeV protons. The three device types responded very differently to protons as shown below:

IDT FIFO: The energy threshold for this device type was about 10 MeV as shown in Figure 10. The cross-sections were relatively flat at the energy levels between 20 and 30 MeV. The cross-section increased to 2×10^{-14} cm²/bit at 50 MeV. All upsets appeared to have taken place at memory cell area, since most upsets were isolated errors representing one upset bit per word. In Figure 10 the SEU cross-sections are compared to those which are model dependent estimations derived with the use of an old method (by Petersen [11]) as well as a new method (by Chiba [12]). The latter method provides the saturation cross-section only. We have plotted the estimated saturation cross-section at an arbitrary energy of 100 MeV. The saturation cross-section seems to provide a good agreement for this device type. Both methods attempt to deduce proton cross-sections utilizing respective heavy ion results, as briefly described in SUMMARY. The old method yields a cross-section curve with the use of the Bendel model [13]. The curve provides a much larger cross-sections at higher energy values. No SEFI or SEL was observed for this device type with protons.

TI FIFO: The threshold energy of this device type was about 20 MeV as shown in Figure 11. The cross-sections increased to about 5×10^{-11} cm²/bit at 50 MeV. Most upsets appeared to have originated in the control section. Once an error emerged at one address location (while we were reading the device), some following address locations showed upsets. The affected locations varied. Also the number of affected locations was not constant. It was as small as a few locations and as many as 10 locations in some cases. In Figure 11 the

SEU cross-sections are compared to those which are model dependent estimations. The derived Bendel curve appears to show a good agreement for this device type. No SEFI or SEL was observed with protons.

HBA FIFO: This device type showed a relatively low sensitivity to protons as shown in Figure 12. We did not detect any sign of upsets at the energy levels of 20 and 30 MeV. The upper limit of the cross-section was about 3×10^{-18} cm²/bit at 30 MeV. At 50 MeV we observed upsets resulting in an upset cross-section of about 1.5×10^{-16} cm²/bit. No SEFI or SEL was observed for this device type with protons.

B. Flash Memory Sensitivities to SEE

Flash memories were programmed to hold a 5555(hex), AAAA(hex), FFFF(hex), or 0000(hex) at each address location during irradiation with heavy ions. Any deviation in the pattern at any location was reported as an error during read operations. All address locations were continuously interrogated starting from 0 to the maximum address location. A write (or program) instruction was used to write over with “0’s”. If an error were to occur during the write operation, it would be detected during subsequent read operations. An erase instruction was used to “write over” specified address locations (e.g., one entire block) with “1’s”. If an error were to occur during the erase operation, it would be detected during subsequent read operations. All exposures were carried out while keeping the test device at room temperature. The bias voltage was 3.0 volts.

SEU sensitivities during READ operations were measured as shown in Figure 13 for 28F640C3BC. The “saturation cross-sections” were about 5×10^{-4} cm²/device. The threshold (associated with 1 % of the saturation value) LET value was about 4 MeV/(mg/cm²). Since these upsets were not “written in the memory”, it was expected that they were induced in the readout buffers and/or control sections of the device.

SEFI sensitivities were measured. The SEFI events were expected to have originated from upsets in the control section of the device. As is often the case, some SEFI events were accompanied by an increased bias current (e.g., 30 mA). SEFI cross-sections of 28F640C3s are shown in Figure 14, for two cases of reset conditions. Assertion of reset (during which the device was in the RESET condition) normally reduced the occurrence of SEFIs. The reduction was more pronounced for measurements made at low LET values. SEFI events took place during WRITE (or PROGRAM) and ERASE operations. The cross-sections during these operations were similar to what we observed during READ operations. Test samples were not permanently damaged after SEFI. We kept test samples in the high current condition for an extended time. An example is shown in Figure 15. In each case, a proper application of the power cycle (“off” followed by “on”) restored normal operating conditions. The bias current increased with increasing fluence, if the power was not cycled, and multiple occurrences of SEFI appeared to have taken place. These increases are shown in Figure 16 for 28F640C3BC. We used Kr ions (LET of 41) in order to observe these events. It was

expected that multiple SEFI sites in a die were the cause of the raised bias current values.

For low LET values near 10 MeV/(mg/cm²), the current increase due to SEFI was limited to below 20 mA as shown in Figure 17 for 28F640C3BC. In this figure all SEFI current values were those associated with the occurrence of the first SEFI (no multiple SEFIs were included.)

We consider that the current increase due to SEFI is somewhat different from the current increase due to SEL, which is assumed to be caused by an activation of parasitic SCR (silicon controlled rectifier). A typical I-V characteristic of SEL with AT22V10B is shown in Figure 18 [14]. When an SEL takes place, the bias current jumps to about 1 A at 5V. As the bias voltage is reduced, the bias current decreases to the holding point, at which the bias current suddenly returns to a low value and the SEL condition is removed. In Figures 19 we show I-V characteristics associated with a SEFI event for 28F640C3BC. For these devices, (1) the holding points are not well specified, (2) the bias current decrease (in association with reduced bias voltage) is not always monotonic, and (3) the current decrease is not semi-logarithmic.

We observed the phenomenon of “leaky bits” (hard errors) in flash memories, that is, bits that appear to lose their stored charge so that they revert to the erased state (a “1” in this device). We saw leaky bits even when the device was not powered during irradiation with ions of a large LET value. We investigated the threshold for these bits by irradiating the devices with low LET ions and progressively increasing the LET of the ions until leaky bits were observed. Two fresh devices were used to investigate the threshold for the leaky bit effect. Each device was irradiated in stages beginning with low-LET ions and progressing to higher LET to see when the leaky bits began. Neither device showed any sign of leaky bits after exposure to a fluence of more than 1.0 X 10⁶ ions/cm² of ions up to Cu [LET= 30 MeV/(mg/cm²)], in several cases more than 1.0 x 10⁷ ions/cm² were used. Leaky bits occurred in both devices after exposure to Kr ions [LET= 41 MeV/(mg/cm²)]. For one device they appeared at a fluence greater than 8.4 x 10⁴ Kr ions/cm² (4.7krad integral dose from all ions), for another they were produced at a fluence less than 4.1 x 10⁴ Kr ions/cm² (1krad integral dose) as shown in Figure 20. Conclusions regarding leaky bits: None of the tested devices have shown leaky bits without exposure to Kr ions [LET= 41 MeV/(mg/cm²)]. Persistent errors (leaky bits or hard errors) can appear with lower LET ions after a Kr exposure as the total dose accumulates. Once exposed to Kr ions, the onset of leaky bits is highly variable among devices. SEU sensitivity during WRITE and ERASE operations were measured yielding negative results. The upper limit of the cross-section was about 5 x 10⁻⁴ cm²/device.

Similar results were observed with 28F320C3BC devices. Examples for SEU and SEFI are shown in Figure 21. SEFI cross-sections in Figure 21 were measured while RESET was not asserted.

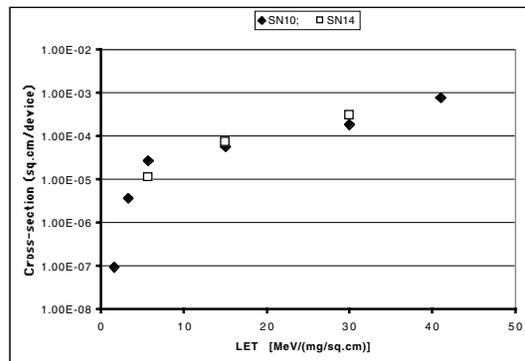


Figure 13. SEU results during READ operation.

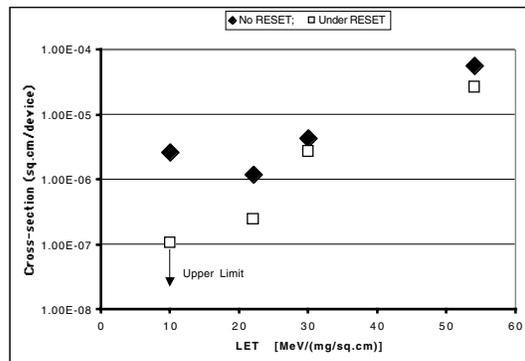


Figure 14. SEFI results for two cases: (1) No RESET and (2) under RESET conditions.

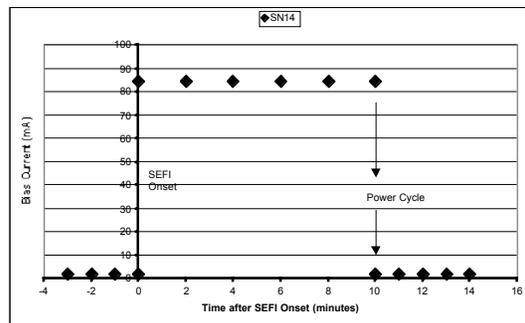


Figure 15. Onset and recovery (via power cycle) from SEFI.

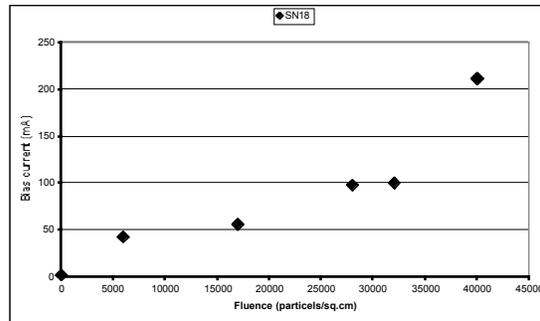


Figure 16. SEFI bias current increased due to multiple SEFIs. RESET was not asserted. Ions with LET of 41 MeV/(mg/cm²) were used.

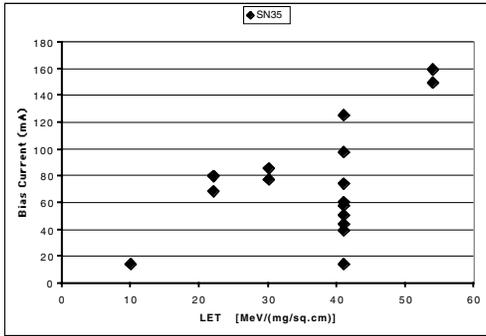


Figure 17. SEFI induced bias current vs. LET. No multiple SEFIs are included.

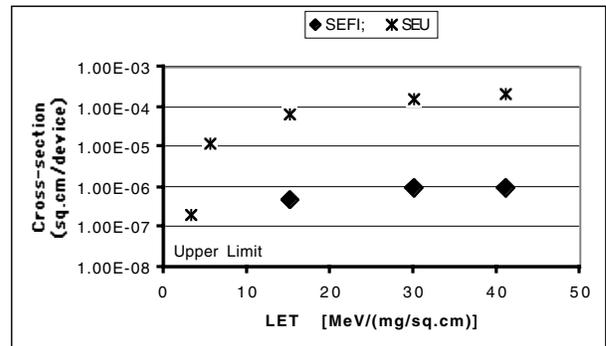


Figure 21. SEU and SEFI test results for 28F320C3BC during read cycles.

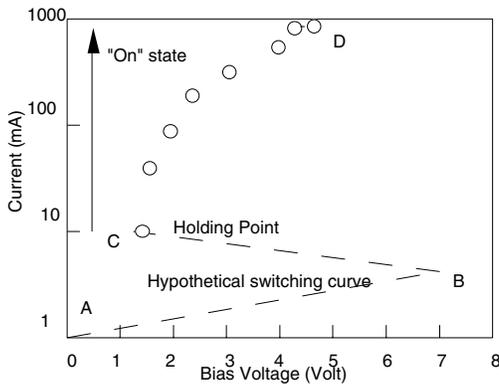


Figure 18. I-V characteristics for SEL at AT22V10B.

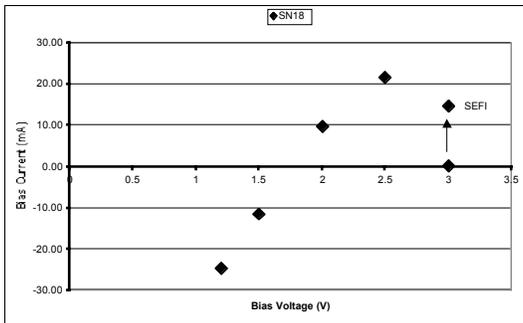


Figure 19. I-V characteristics for SEFI.

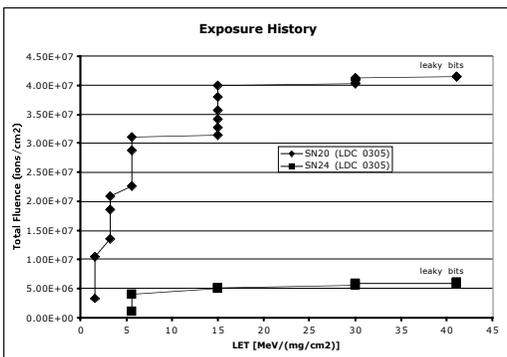


Figure 20. Appearance of hard errors with Kr ions.

SUMMARY

Heavy ion induced SEE test results of the three FIFO types showed that TI devices yielded the lowest sensitivities to SEFI as well as to SEL. HBA devices were most sensitive to SEL. Proton induced SEU results for the three devices types (see Figures 10 through 12) are presented. In Figures 10 and 11 the results are shown along with predicted (estimated) values derived from associated heavy ions results. In 1992 Petersen showed that one could obtain the Bendel parameter A via $A = L_{0.1} + 15$, where $L_{0.1}$ is the LET value at which the cross-section is 10 % of the saturation value [11]. The Bendel parameter A may be used to show proton induced cross-sections at any proton energy [13]. As we can see in Figure 10, this formulation does not seem to always work properly. For TI devices the formulation seems to work well (see Figure 11). Another method may be used to estimate proton induced saturation cross-sections [12]. They are shown at an arbitrarily chosen energy level of 100 MeV (see Figures 10 and 11.) For IDT FIFO, the derived value seems to fit well. In general SEE sensitivity of present FIFO test samples is similar to that observed with smaller memory devices several years ago [1,2,3]. For example SEU LET_{th} is at about 3 MeV/(mg/cm²) for Matra 67204EV-50 (4K x 9) FIFO [2].

Various types of SEE were observed with the present flash memory samples. Similar observations with other devices were reported by other investigators [4,5,6]. Since many cross-sections were relatively small (e.g., 1×10^{-5} cm²/device for SEU at LET of 6 in Figure 13), we have used a rather large fluence. After many irradiations, test samples seem to approach the total dose limit [5,6,15,16]. Therefore, it is essential to have a large number of test samples in order to measure various types of SEE cross-sections.

The thickness of the oxide between the floating gate and the channel is about 100 Angstroms in the area where the tunneling takes place [7]. In this region, stored charges may be lost along an ionization track introduced by an incoming ion [15,16]. For the present devices, these ion tracks, produced by ions with a large LET value, seem to leave some "latent damage", if it is not an outright "short circuit". After latent damage has been created, an ion with lower LET value may cause a short across

the floating gate and the channel removing the stored charge in the floating gate.

SEFIs seem to take place in various sections in the present test samples. They emerge during any of READ, WRITE, or ERASE operations as well as in the stand-by condition. The SEFI cross-section is reduced when the device is RESET (and held) during irradiation. Various types of SEFI were reported to have existed in other flash memories manufactured by Aeroflex and Intel [4,5,6].

Testing of present FIFO and flash memories tend to take a longer time than some devices that we tested only several years ago. It is another indication that the complexity of these devices is expanding.

ACKNOWLEDGEMENT

The authors wish to acknowledge the on-site-staff at the Lawrence Berkeley National Laboratory 88-inch cyclotron facility.

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