

Backplane Driver Technical Summary

GTLP Signal Level Background Information

Gunning Transceiver Logic (GTL), approved as a JEDEC Standard JEDS8-3 in 1993, was originally created as a reduced swing I/O driver technology to support high-speed buses and backplanes. The output structure is an open drain NMOS transistor that requires the bus or backplane to be actively terminated for proper signaling. GTL is used in ASICs, processors and logic and has surfaced as a leader in backplane driver technology.

A GTL bus is designed to work with low voltage swings. The input buffer works like an analog comparator rather than an inverter. This allows the GTL inputs to switch quickly without needing to be driven rail to rail. Driver output swings of 0.8 V to 1 V are common, and V_{IL}/V_{IH} as low as 100 mV can be detected at the input.

Initially, GTL drivers were designed to pull a 1.2-V signal down to 0.4 V when it switched on. The 0.4-V V_{OL} is common for an N-channel MOSFET pull-down device in saturation. However, since the reference voltage for the input comparator is set at 0.8 V, which makes such devices are susceptible to ground bounce noise.

A variant of GTL, called GTL+, was used on the Intel Pentium Pro (P6) processor to address the noise margin concern. In GTL+, the termination reference voltage is raised to 1.5 V, with the driver pulling down to V_{OL} of 0.5 V. This gives another 100 mV of lower threshold noise margin, and moves the input comparator reference voltage out of the range of most ground bounce noise.

A 1996 Fairchild extension of the GTL standard was called GTLP. The termination reference voltage is raised to 1.5 V, with the driver pulling down to V_{OL} of 0.65 V with input V_{IL}/V_{IH} swings of 200 mV. It was used in three devices, the Fairchild Semiconductor GTLP16612/16616 and the Pericom GTLP16612. GTLP is also normally associated with slower edge rates and improved performance with distributed loads.

The original GTL specification did not have any output signal edge slew rate definition. When fast drivers were used it was discovered that the devices' ground bounce and signal integrity deteriorated. The GTL+ specification requires that the driver slew rate be between 0.3 V/ns and 0.8 V/ns. This has been found to offer enough speed to operate at high clock frequencies without causing excessive ground bounce or signal crosstalk.

The following table compares GTL, GTL+ and GTLP signal levels:

	GTL	GTL+	GTLP	Unit
V_{TT}	1.2	$1.5 \pm 10\%$	1.5	V
$V_{OL} \text{ (max)}$	0.4	0.5	0.65	V
V_{REF}	0.8	$2/3 V_{TT} \pm 2\%$	$2/3 V_{TT}$	V
$V_{IL} \text{ (max)}$	$V_{REF} - 50 \text{ mV}$	$V_{REF} - 200 \text{ mV}$	$V_{REF} - 100 \text{ mV}$	mV
$V_{IL} \text{ (min)}$	$V_{REF} + 50 \text{ mV}$	$V_{REF} + 200 \text{ mV}$	$V_{REF} + 100 \text{ mV}$	mV
$V_{EDGE} \text{ (min)}$	No Spec	0.3	No Spec	V/ns
$V_{EDGE} \text{ (max)}$	No Spec	0.8	No Spec	V/ns

The V_{REF} threshold (50 mV, 100 mV or 200 mV) is set by device design and cannot be changed. GTL and GTLP devices can operate at GTL, GTL+, or GTLP signal levels. However, the 50



mV V_{IL} GTL specification is normally used, improving the noise margin enjoyed at GTL+ or GTLP levels. Most applications have moved to the GTL+/GTLP ($V_{TT} = 1.5V$, $V_{REF} = 1V$) signal level standard as it provides a higher system noise margin and better system performance.

Texas Instruments GTL devices are optimized for GTL signal levels but also operate at GTL+ signal levels. GTL devices have a fast edge rate and are best used for memory interface/bus-on-a-board applications.

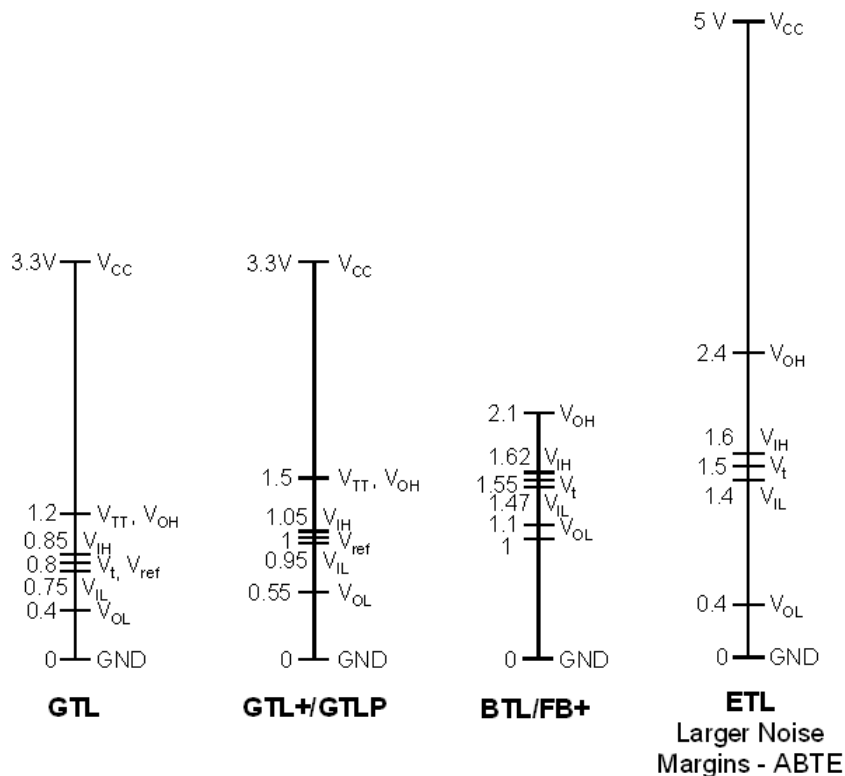
Texas Instruments GTLP devices are optimized for GTLP signal levels but can also operate at GTL signal levels. GTLP devices have slow edge rates and are best used for parallel backplane applications.

Reference:

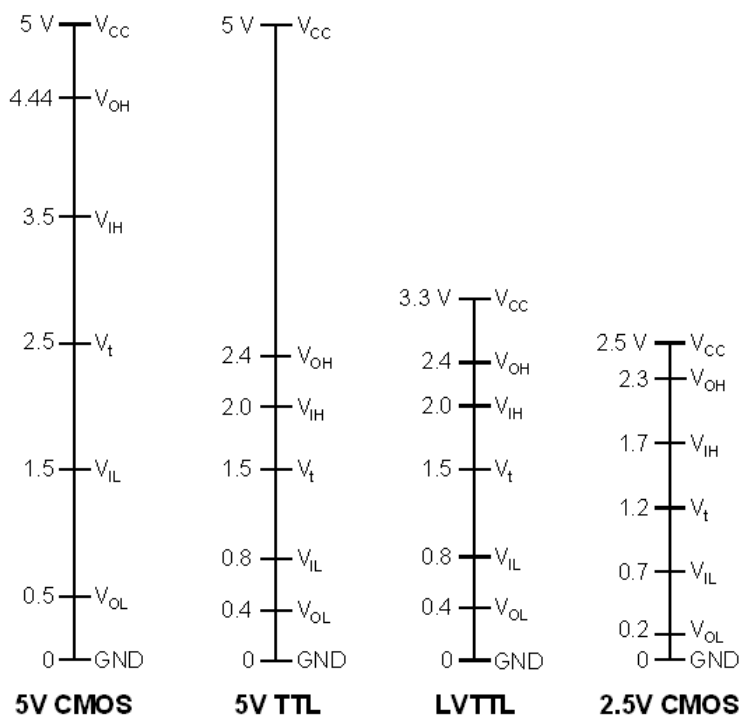
California Micro Devices, Application Note AP-200, *GTL+ Termination Applications*, 1996

Where To Use GTLP

In general, TTL/LVTTL based devices (ABT, FCT, LVT, and ALVT) can operate in distributed backplane applications in excess of 30 MHz while reduced swing I/O devices (GTL, BTL, ECL) can operate in excess of 40 MHz. GTLP can operate in excess of 80 MHz because it is specifically designed with a slower edge rate for optimum performance in a distributed load configuration. Each data sheet provides both lumped load and RLC network data for the designer to use. The RLC data will more closely approximate the device response in a distributed load.



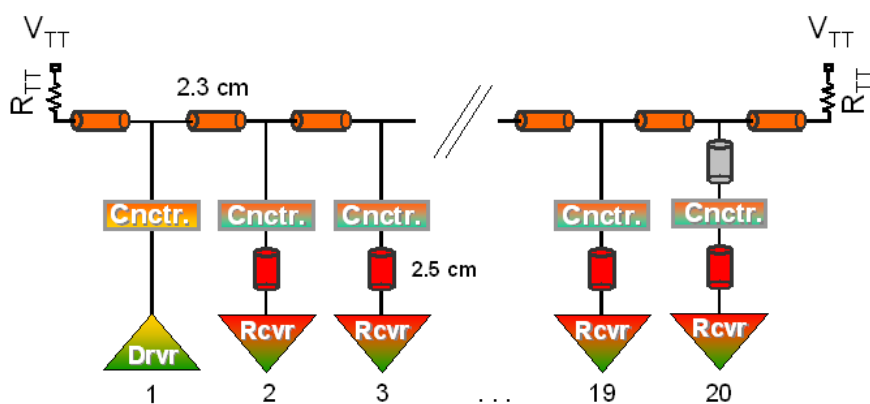
Logic Switching Levels



Logic Switching Levels (continued)

GTLP family devices operate at LVTTTL signal levels on the A-Port and GTLP signal levels on the B-Port (backplane/distributed load side).

Transition from TTL type logic to GTLP logic is relatively simple. The backplane architecture is the same with the exception of the termination scheme (termination voltage (V_{TT}) and locally generated reference voltage (V_{REF}).

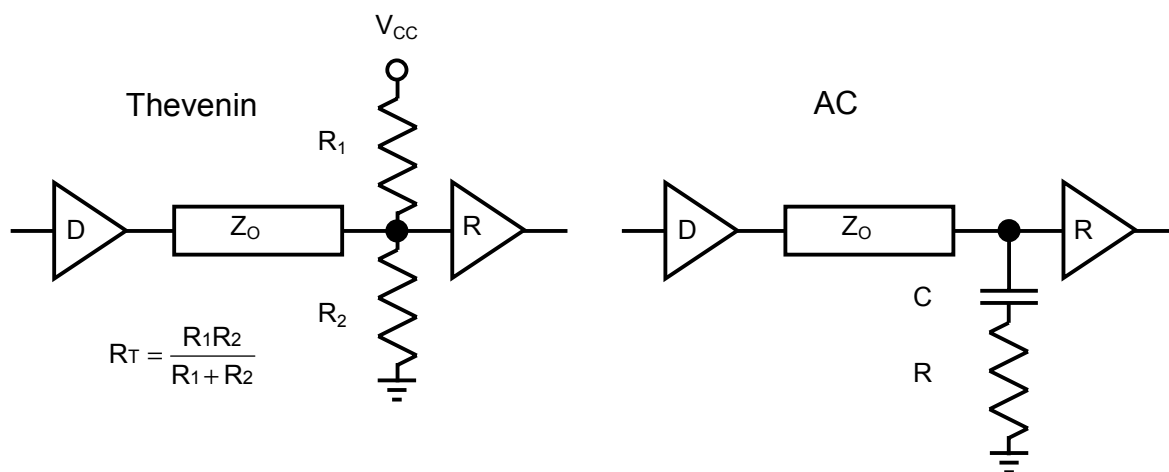


The GTLP backplane can be configured in a double-ended pull-up termination scheme where bi-directional data transmission is required (as shown above). The bus is pulled to the termination voltage (V_{TT}) through the termination resistor (R_{TT}) when the GTLP open drain device is off and pulled low when the GTLP open drain device is on.

Benefits include:

- No bus contention
- Reduced power consumption
- Simple implementation

TTL devices typically use a Thevenin or AC termination scheme.



Backplane Architecture Considerations

Single-Ended Transmission - One signal line, its output is interpreted with respect to ground.

- Advantages – Simplicity and low implementation cost
- Disadvantages – Reliable operating distance and speed limited by poor noise immunity.

Differential Transmission - A pair of cables (lines) is necessary for each channel. One line transmits the “true” signal while the second line transmits its complement.

- Advantages – Less susceptible to common-mode noise.
- Disadvantages – Higher cost, requires well-designed impedance and correct line termination, and twisted pair cables are more expensive.

Parallel Transmission – The driver attached to the bus places n-bits of data in parallel onto the bus and all the information is sent at one time.

- Offer very high data rates over short distances.
- No software overhead with parallel standards.
- One bit could be used as a signal flag, with a very fast system reaction time, since a serially sent word must first be fully received and decoded.
- Many industrial and telecom applications already use parallel backplanes, meaning designers, and engineers are familiar with these kinds of systems and have the knowledge and experience to quickly implement new designs.

Differential Transmission – Data is converted into a serial stream, transmitted at high speed along the line to the receiver then de-serialized back into the original parallel data.

- Differential devices are new and are extremely useful in serial data transmission applications that allow a more flexible approach, longer cable length and lower cable cost.
- Reduction of the number of signal and GND lines required to transmit data from one point to another can have major board savings.

Differential devices may not fit all applications where the simplicity and low cost of implementation really points to single-ended device use.

Reduced voltage swing, **single-ended open drain** construction allows GTLP devices higher frequency operation than older TTL/LVTTL signal level devices in existing **parallel** backplane architectures.

More information on both serial and parallel bus solution technology is available from Texas Instruments can be found in the [*Comparing Bus Solutions*](#) (SLLA067) application report.

Optimum R_{TT} Versus Backplane Loading

One of the most important considerations is the proper sizing of the termination resistor (R_{TT}). R_{TT} should not be automatically chosen at 50 ohms but should be matched to the loaded impedance of the backplane to minimize overshoot and maximize signal integrity. However, care should be used to not exceed the recommend operating conditions.

- Backplane impedance is a function of board capacitance and slot spacing (pF/inch)
- Incident wave switching is optimized when R_{TT} matches the loaded backplane impedance
- Use the optimum R_{TT} (not to exceed medium or high drive recommended I_{OL}) for best signal integrity and maximum backplane speed

The following illustrates calculation of the lowest R_{TT} possible for your chosen device in a bi-directional system:

$$V_{TT} = 1.5V$$

R_{TT} (Termination resistor at the end of the line) is 2X Ohms

DC-conditions (static low) give a load of 2X Ohms in parallel with 2X Ohms yielding a device load of X Ohms

Calculating the current for this condition:

$$V_{TT} - V_{OL} \text{ (GTLP side)} = 1.5 V - 0.55 V = 0.95 V$$

$$I_{OL} \text{ max} = 0.95 V \div X \text{ Ohms}$$

$$X = 0.95 V \div I_{OL} \text{ max}$$

$$R_{TT} = 2X$$

$$R_{TT} = 1.9 V \div I_{OL} \text{ max}$$

Minimum R_{TT} not to exceed recommend operating conditions would be:

- Medium drive devices (50 mA @ 0.55 V) = $1.9 \div 0.050 = 38$ ohms
- High drive devices (100 mA @ 0.55 V) = $1.9 \div 0.100 = 19$ ohms



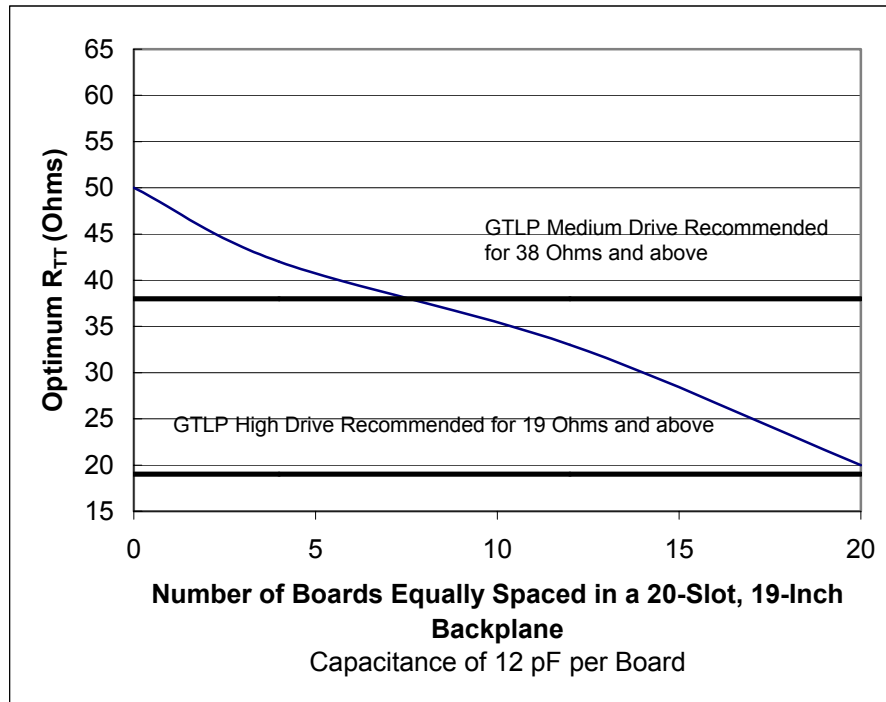
The medium and high drive devices would be most useful in the following applications:

High Drive

- Low impedance backplanes with matched termination resistors
- Tightly spaced, larger (10 to 20 slot) multi-slot backplanes

Medium Drive

- Medium impedance, smaller (2 to 14 slot) multi-slot backplanes
- When power consumption or price is a concern



Texas Instruments Demonstration Backplane

To help telecom and datacom designers who are unfamiliar with high-speed backplanes, Texas Instruments has developed a portable backplane evaluation module (EVM). The EVM is 48-bits wide with 1 extra bit for a source synchronous clock. The backplane length varies from 2 to 20 slots in 8-bit widths and has removable cards with various GTLP devices so the designer can position cards to most closely approximate their intended design and test hindrances such as crosstalk and noise in a real-world environment. An EVM is available world wide, please call your supporting Field Sales Office to schedule a demonstration.

GTLP Application Reports

Texas Instruments has made available several excellent downloadable GTLP and backplane application reports that can be used to help you more fully understand GTLP devices and backplane architectures.

- [Basic Design Considerations For Backplanes](#) (SZZA016)
- [Fast GTL Backplanes With The GTL1655](#) (SCBA015)
- [GTL/BTL: A Low-Swing Solution For High-Speed Digital Logic](#) (SCEA003A)
- [High-Performance Backplane Design With GTL+](#) (SCEA011A)
- [Implications Of Slow Or Floating CMOS Inputs](#) (SCBA004C)
- [Achieving Maximum Speed on Parallel Buses With Gunning Transceiver Logic \(GTLP\)](#) (SCEA022)
- [Fast GTLP Backplanes With the GTLPH1655](#) (SCBA015A)
- [GTLP/GTL Logic High-Performance Backplane Drivers Data Book](#) (SCED004A)
- [High Level Brochure of Gunning Transceiver Logic Plus](#) (SCEB005)
- [Texas Instruments GTLP Frequently Asked Questions](#) (SCEA019)

Universal Bus Transceivers (UBTs)

Universal bus transceivers are devices that can be used to obtain different functions by setting control pins to different levels. Using UBTs can minimize procurement and supply problems by using one device in the place of multiple devices. GTLP devices are available as UBTs or as common bus transceivers (i.e. '16245 functionality).

Function	8-Bit	9-Bit	10-Bit	16-Bit	18-Bit
Transceiver	`245, `623, `645	`863	`861	`16245, `16623	`16863
Buffer/Driver	`214, `244, `541		`827	`16241, `16244, `16541	`16825
Latched Transceiver	`543			`16543	`16472
Latch	`373, `573	`843	`841	`16373	`16843
Registered Transceiver	`646, `652			`16646, `16652	`16474
Flip-Flop	`374, `574		`821	`16374	
Universal Bus Driver					`16835
Standard UBT					`16500, `16501
GTLPH1655 UBT replaces above functions but at GTLP levels on the B-Port					
Registered Transceiver w/CLK Enable	`2952			`16470, `16952	
Flip-Flop w/CLK Enable	`377	`823			`16823
Standard UBT w/CLK Enable					`16600, `16601
GTLPH16912, 16612 and 1612 replace all above functions but at GTLP levels on the B-Port					