Public Version

OMAP4430 Multimedia Device

Texas Instruments OMAP™ Family of Products

Silicon Errata

Literature number: SWPZ009A

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Revision History

Revision Initial	2010, October 22
Revision A	2010, December 21

Added Section 1.25, “HS USB Host HSIC Not Functional”.

Added Section 1.26, “I2C SCL and SDA Glitch At Reset Release”.

Added Section 1.27, “Retention/Sleep Voltage Transitions Ramp Time”.

Added Section 1.28, “Interrupt Enable Registers Not Restored”.

Added Section 1.29, “MMCHS_HCTL.HSPE Is Not Functional”.

Changed Section 2.6, “LPDDR2 Instability”.

Added Section 2.7, “HDQ™/1-Wire® Communication Constraints”.

Added ES2.2 impact for all bugs and limitations

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Release Notes

Revision	A
State	Approved

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Modules Impacted

Table 1. Module DISPC (3 sections)

DISPC	Section
	i525: Section 1.13, “Deadlock Between DISPC And DSI When PCD = 2, VP_CLK_RATIO = 0”
	i596: Section 2.4, “BITMAP1-2-4 Formats Not Supported By The Graphics Pipeline ”
	i597: Section 2.5, “Limitation On DISPC Dividers Settings When Using BITMAP Format”

Table 2. Module DMA4 (1 section)

DMA4	Section
	i378: Section 1.6, “sDMA Channel Is Not Disabled After A Transaction Error”

Table 3. Module DMM (1 section)

DMM	Section
	i614: Section 1.24, “DMM Hang Issue During Unmapped Accesses”

Table 4. Module DSI (11 sections)

DSI	Section
	i339: Section 1.1, “DSI: Minimum Of 2 Pixels Should Be Transferred Through DISPC Video Port”
	i340: Section 1.2, “DSI: Cancel Tearing Effect Transfer”
	i341: Section 1.3, “DSI: RX FIFO Fullness”
	i342: Section 1.4, “DSI: Access Restriction On DSI_TIMING2 Register”
	i343: Section 1.5, “DSI: Tx FIFO Flush Is Not Supported”
	i422: Section 1.7, “DSI SOF Packet Not Send”
	i483: Section 1.11, “DSI VSYNC HSYNC Detection In Video Mode”
	i524: Section 1.12, “Dual Video Mode”
	i525: Section 1.13, “Deadlock Between DISPC And DSI When PCD = 2, VP_CLK_RATIO = 0”
	i575: Section 2.1, “ Transfer Of Multiple Command Packets Coming From L4/L3 Interconnect During A Blanking Period In Interleaving Mode”
	i576: Section 2.2, “Nonburst Video Mode Using Sync Pulses: NO HE Packets Sent VSA, VFP, And VBP Blanking.”

Table 5. Module EMIF (2 sections)

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	i603: Section 1.19, “Deep Power-Down Support During Off Mode”
	i615: Section 2.6, “LPDDR2 Instability”

Table 6. Module HDQ (1 section)

HDQ	Section
	i621: Section 2.7, “HDQ™/1-Wire® Communication Constraints”

Table 7. Module HS USB (1 section)

HS USB	Section
	i620: Section 1.25, “HS USB Host HSIC Not Functional”

Table 8. Module I2C (5 sections)

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	i592: Section 1.15, “I2C: In SCCB Mode, Under Specific Conditions, The Module Might Hold The Bus By Keeping SCL Low.”
	i593: Section 1.16, “I2C: Spurious Wake-Up Event When Sysclk Period Is Higher Than Ocpclk Period ”
	i594: Section 1.17, “I2C: Wrong Behavior When A Data With MSB 0 Is Put In The FIFO Before A Transfer With SBLOCK Is Started ”
	i595: Section 1.18, “I2C: After An Arbitration Is Lost, The Module Starts Incorrectly The Next Transfer Incorrectly”
	i622: Section 1.26, “I2C SCL and SDA Glitch At Reset Release”

Table 9. Module ISS (3 sections)

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	i488: Section 1.8, “ISS: SOFTRESET Bit Status Not Working For Circular Buffer”
	i489: Section 1.9, “ISS: SOFTRESET Bit Status Not Working For Burst Translation Engine”
	i496: Section 1.10, “ISS State Can Be Corrupted During Debug Mode”

Table 10. Module MMC (1 section)

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	i626: Section 1.29, “MMCHS_HCTL.HSPE Is Not Functional”

Table 11. Module McBSP (1 section)

McBSP	Section
	i588: Section 1.14, “McBSP Used In Slave Mode Can Create A Deadlock Situation When Doing Power Management”

Table 12. Module PRCM (6 sections)

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	i608: Section 1.20, “RTA Feature Is Not Supported”
	i609: Section 1.21, “I/O Daisy Wakeup During Device Off Mode Transition Stalls The Device Power Transition”
	i611: Section 1.22, “Off Mode Power Consumption On VDD_WKUP”
	i612: Section 1.23, “Wkup Clk Recycling Needed After Warm Reset”
	i623: Section 1.27, “Retention/Sleep Voltage Transitions Ramp Time”

Table 13. Module ROM code (1 section)

ROM code	Section
	i625: Section 1.28, “Interrupt Enable Registers Not Restored”

Chapter 1. Bugs

1.1. DSI: Minimum Of 2 Pixels Should Be Transferred Through DISPC Video Port

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i339

CRITICALITY

Low

DESCRIPTION

Minimum number of pixels for MIPI command mode from the video port should be greater than 1 (at least 2). Image with less than 2 pixels is not expected to be used in a real applicative use case.

WORKAROUND

If sending a single pixel is needed, the OCP L4 slave port can be used (through CPU or sDMA).

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.2. DSI: Cancel Tearing Effect Transfer

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i340

CRITICALITY

Low

DESCRIPTION

Transfer using tearing effect cannot be cancelled (writing TE_SIZE to 0). Writing TE_SIZE would have no effect and transfer would continue.

WORKAROUND

Always wait for tearing effect to complete before changing any configuration.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.3. DSI: RX FIFO Fullness

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i341

CRITICALITY

Low

DESCRIPTION

RX FIFO fullness can be incorrect just after a FIFO read. FIFO fullness should be read only once at the beginning of the transfer. Other accesses during a transfer are not guaranteed.

WORKAROUND

Use only programming model provided in TRM section.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.4. DSI: Access Restriction On DSI_TIMING2 Register

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i342

CRITICALITY

Low

DESCRIPTION

This register must not be written twice when TxByteClkHS is stopped to avoid L4 OCP port deadlock.

WORKAROUND

User must check that the TxByteClkHS clock is activated before initiating any write access to DSI_TIMING2 register.

To ensure the TxByteClkHS clock is active, the user must check:

1. PLL is locked (DSI_PLL_STATUS register; DSI_PLL_LOCK bit)
2. DSIPHY must be in ON power state (PWRCMDON).
3. Clock/Data lane positions are correctly set (DSI_COMPLEXIO_CFG1.xxx_POSITION).

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.5. DSI: Tx FIFO Flush Is Not Supported

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i343

CRITICALITY

Low

DESCRIPTION

Executing a FIFO flush does not properly clean the logic, thus resulting in unpredictable behavior of the module.

WORKAROUND

User must perform module software reset when a transfer is aborted.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.6. sDMA Channel Is Not Disabled After A Transaction Error

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i378

CRITICALITY

Medium

DESCRIPTION

In case of destination synchronized transfer on the write port (or source sync with SDMA.DMA4_CCRi[25] BUFFERING_DISABLE = 1), if a transaction error is reported at the last element of the transaction, the channel is not automatically disabled by DMA.

WORKAROUND

Whenever a transaction error is detected on a transaction on the write side of the channel i, software must disable the channel(i) by setting the DMA4_CCRi[7] ENABLE bit to 0.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.7. DSI SOF Packet Not Send

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i422

CRITICALITY

Low

DESCRIPTION

The first packet in command mode is not sent due to inaccurate clock gating.

Root cause description: In command mode when DDR_CLK_ALWAYS_ON and IF_EN are set to 1, DDR clock is not present immediately after the IF_EN bit is set to 1 but when the first HS packet from OCP is ready to be sent to PPI HS link.

The DDR_CLK_PRE field is used between the start of the DDR clock and the assertion of the data request signal. After the time defined by the DDR_CLK_PRE field, the clock lane is always present until the IF_EN bit is set to 0. So, there is a delay between IF_EN set to 1 and assertion of the clock lane.

WORKAROUND

In case of command mode where DDR clock should be provided to peripheral before data, the workaround is to program DDR_CLK_PRE =! 0. The value of DDR_CLK_PRE must take into account the different timings: TCLK_PREPARE, TCLK_ZERO.

Sequence to enable the DSI:

1. Set the ForceTxStopMode bit to 1 (DSI_TIMING1 register). This asserts the ForceTxStopMode.
2. Enable virtual channel in command mode / Enable DSI interface.
3. Poll the ForceTxStopMode bit to 0 (DSI_TIMING1 register) until deassertion of the ForceTxStopMode bit. The hardware resets this bit at the end of the counter value.
4. Send SOF(0x00000000) packet in command mode.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.8. ISS: SOFTRESET Bit Status Not Working For Circular Buffer

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i488

CRITICALITY

Low

DESCRIPTION

The SOFTRESET bit of the SYSCONFIG register inside CBUFF (CBUFF_HL_SYSCONFIG[0] SOFTRESET) is set to 0x0 (reset done state) after reset only if CBUFF is out of IDLE.

While CBUFF slave data port is in IDLE, the SOFTRESET bit is always set to 0x1 (status bit gives an ongoing reset, but reset is finished).

WORKAROUND

Ignore status of the the SOFTRESET bit. After a software reset, wait a few cycles before using the module.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.9. ISS: SOFTRESET Bit Status Not Working For Burst Translation Engine

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i489

CRITICALITY

Low

DESCRIPTION

The SOFTRESET bit of the SYSCONFIG register inside BTE (BTE_HL_SYSCONFIG[0] SOFTRESET) is set to 0x0 (reset done state) after reset only if BTE is out of IDLE.

While BTE slave data port is in IDLE, the SOFTRESET bit is always set to 0x1 (status bit gives an ongoing reset, but reset is finished).

WORKAROUND

Ignore the status of the SOFTRESET bit. After a software reset, wait a few cycles before using the module.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.10. ISS State Can Be Corrupted During Debug Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i496

CRITICALITY

Medium

DESCRIPTION

Debug read operations should not impact the internal state of the module.

That cannot be guaranteed because debug reads of some locations can impact DMA requests. Also, some read accesses may be stalled for a long time while ISP operation is ongoing.

WORKAROUND

To avoid read access from being stalled, the CPU must have the priority. This can be configured in the ISP5_MPSR register. Dummy accesses during frame processing lead to data corruption however response is given immediately. This register can be used to avoid stalling debug accesses. Dummy data is returned in that case but does not hurt functionality because debug accesses do not make sense while ISP5 is processing data.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.11. DSI VSYNC HSYNC Detection In Video Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i483

CRITICALITY

High

DESCRIPTION

DSI engine is not always detecting the first VSYNC HSYNC signals received on the video port in video mode.

WORKAROUND

The total number of cycles that must be generated before first VSYNC must be greater than:

- Configuration with line buffers: 3 VP_PCLK + 6 VP_CLK + 6 DSI_CLK.
- Configuration without line buffers: 3 VP_PCLK + 2 VP_CLK.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.12. Dual Video Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i524

CRITICALITY

High

DESCRIPTION

When two video ports are available at the input of the DSI protocol engine, the two streams are interleaved by the DSI protocol engine. Only one video mode is supported by the current implementation on VP1 only. VP2 cannot be in video mode even if VP1 is not in video mode.

WORKAROUND

No

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.13. Deadlock Between DISPC And DSI When PCD = 2, VP_CLK_RATIO = 0

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i525

CRITICALITY

Medium

DESCRIPTION

The buffer handshake feature in the DISPC avoids underflow of the DISPC DMA FIFO. The fullness of the DISPC DMA FIFO is checked before providing data to the pipeline when STALL signal is inactive. When the FIFO hand check feature is activated, the pixel transfer to the DSI module during STALL inactivity period can be stopped (no DISPC_PCLK pulse) and restarted when there is enough data in the FIFO. The DSI protocol engine is configured in command mode.

On video port 1 in command mode, when DISPC_DIVISOR1.PCD = 2, DISPC_CONFIG1.BUFFERHANDCHECK = 1 and DSI_CTRL.VP_CLK_RATIO = 0, the FRAMEDONE IRQ might not be triggered and TE_SIZE counter might not be decremented to 0. This is caused by a deadlock between the DISPC and DSI modules during the transfer of the last pixel of a line

On video port 2 in command mode, when DISPC_DIVISOR2.PCD = 2, DISPC_CONFIG2.BUFFERHANDCHECK = 1 and DSI_CTRL2.VP_CLK_RATIO = 0, the FRAME-DONE IRQ might not be triggered and TE_SIZE counter might not be decremented to 0. This is caused by a deadlock between the DISPC and DSI modules during the transfer of the last pixel of a line.

The DSI protocol engine sends a STALL to the DISPC (stall mode); in parallel the DISPC stops the pixel clock to the DSI because it is waiting for its FIFO DMA to be refilled (buffer handcheck feature). When FIFO DMA is refilled, the DISPC being in stall mode does not provide back the pixel clock to the DSI to deassert the stall and it does not send the last pixel to the DSI.

WORKAROUND

Enable DSI_CTRL.VP_CLK_RATIO and DSI_CTRL2.VP_CLK_RATIO to 0x1 for all PCD values and set WC using following equation:

WC – 1 = N * PPL * BPP

Where:

- N is the number of lines to be sent in a packet. N is an integer.
- BPP is the bytes per pixel configure in DISPC.
- PPL is number of pixels per line configure in DISPC.
- – 1 is the extra command added for continue memory.
- WC is the word count set in DSI_VCn_LONG_PACKET_HEADER.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.14. McBSP Used In Slave Mode Can Create A Deadlock Situation When Doing Power Management

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i588

CRITICALITY

High

DESCRIPTION

When using McBSP in slave mode and doing power management (McBSP going to IDLE state), if external CLKX clock is not provided by external peripheral component, McBSP cannot exit IDLE state. The consequence is that McBSP registers can no longer be accessed.

Note: There is similar limitation on the CLKR when the module is configured as a receiver.

WORKAROUND

The following workarounds are still valid by replacing CLKX with CLKR.

Workaround 1:

- Do not use power-management features of McBSP (SIDLEMODE field in MCBSPLP_SYSCONFIG_REG register set to NO-IDLE all the time).
- Impact of workaround 1: As McBSP transition to IDLE is avoided (SIDLEMODE = NO-IDLE); PRCM cannot transition the chip to low-power mode.

Workaround 2:

Keep external CLKX clock always running during application (for example, during an Audio Playback).

Workaround 2 implementation details:

- At the beginning of the application (for example, Audio Playback): Keep CLKX always running by setting external peripheral component register accordingly.
- At the end of the application (for example, Audio Playback): Unload McBSP2 drivers (and set XRST bit from SPCR2 to 0). Then stop CLKX by software (by setting external peripheral component register accordingly).
- Impact of workaround 2: Serial clock kept active during whole application (for example, Audio Playback).

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.15. I2C: In SCCB Mode, Under Specific Conditions, The Module Might Hold The Bus By Keeping SCL Low.

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i592

CRITICALITY

Low

DESCRIPTION

In SCCB mode if the XRDY/RRDY are not served during address phase, the module starts to hold the bus by keeping SCL low (FIFO empty or full).

Then, after serving these interrupts, the module does not continue the current transfer and blocks in this state.

This bug appears only in applications where the module is used in SCCB mode. The bug does not appear at all if interrupts are served before the address phase starts (quickly enough to avoid entering this context).

WORKAROUND

None.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.16. I2C: Spurious Wake-Up Event When Sysclk Period Is Higher Than Ocpclk Period

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i593

CRITICALITY

Medium

DESCRIPTION

Expected behavior: The scenario occurs when the IDLEREQ is sent after serving an interrupt/DMA and system clock period is higher than ocp clock period (at least two times higher) and prescaler value > 4 (internal clock is sysclk/(PSC+1)). If there is no other interrupt or DMA request, the module enters IDLE state, and exits this idle with a wakeup generated from some event.

Observed behavior: A spurious wakeup is asserted and maintained while no IRQ/DMA request is generated once the module is brought out of IDLE state.

WORKAROUND

If the values of the sysclk period and ocpclk period are close, the prescaler PSC value of the I2C_PSC register should be programmed to any value less than or equal to 4. For higher values,a bug may occur. There is no issue for prescaler value PSC = 1 (that is high speed).

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.17. I2C: Wrong Behavior When A Data With MSB 0 Is Put In The FIFO Before A Transfer With SBLOCK Is Started

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i594

CRITICALITY

Low

DESCRIPTION

Expected behavior: Before starting a new transfer from another I2C device, 1 byte of data is written to TX FIFO. The module is addressed on a 10-bit address as a slave transmitter (one of his addresses) and I2C clock blocking is enabled. After a repeated start condition, SBLOCK is activated again for the second part of the address.

Observed behavior: Given the addressing and SBLOCK conditions defined above, if the data put in FIFO has its MSB 0, the module makes a glitch on SDA bus on the eighth bit (SDA is set to 0 for a short period) which can be interpreted as an illegal start/stop condition.

WORKAROUND

The scenario described is a corner case. It may very seldom happen in applications. To avoid the situation, before a transfer is started on the I2C bus, all interrupts should have been cleared (part of the guideline given in the specification), or when I2C is a transmitter, no data should be placed in the FIFO, without receiving the request to do so from the slave.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.18. I2C: After An Arbitration Is Lost, The Module Starts Incorrectly The Next Transfer Incorrectly

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i595

CRITICALITY

Low

DESCRIPTION

Expected behavior: After a transfer on the I2C bus, where the module lost the arbitration during the address phase, a new transfer as a master is programmed in I2C_CON by setting the MST bit to 1, having the start bit STT in the I2C_CON register still unset. The STT bit can be set after a significant delay, to point the moment in which the transfer starts on the I2C bus. The module should only start the transfer on I2C after setting this STT start bit in I2C_CON.

Observed behavior: The module starts the transfer on I2C before setting STT, immediately after setting the MST bit in the I2C_CON to 1.

WORKAROUND

The MST and STT bits inside I2C_CON should be set to 1 at the same moment (avoid setting the MST bit to 1 while STT = 0).

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.19. Deep Power-Down Support During Off Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i603

CRITICALITY

Medium

DESCRIPTION

When coming out of off mode, the memory controllers assume connected SDRAMs to be in self-refresh mode.

The EMIF receives a DEVICE_OFFWKUP_CORERSTACTST signal from the PRCM defining if an EMIF cold reset was due to a global reset or to exiting off mode;

- In case of a global cold reset, the full SDRAM init phase is performed.
- In case of off mode exit, only the self-refresh exit sequence is performed and auto-refresh commands are immediately sent.

If the memory was in deep power-down state during the chip off mode, the sequence performed by EMIF is not compliant with the JEDEC specification and could result in an unexpected behavior on the memory side. Exit from DPD actually requires the same full init sequence as after a global cold reset.

WORKAROUND

Software workaround:

- Before getting into off mode, force the value stored in the control module EMIF_SDRAM_REF_CTRL.REG_INITREF_DIS to 1.
  - This forces the value for the EMIF register to 1 when its content is restored when returning from off mode.
- When returning from off mode, and before making any access to the memory in DPD state:
  1. Put CORE PLL in MN bypass mode CM_CLKMODE_DPLL_CORE.DPLL_EN = 0x4.
  2. Program the DLL override CM_DLL_CTRL.DLL_OVERRIDE = 1.
  3. Force the configuration field EMIF_SDRAM_CONFIG.REG_SDRAM_TYPE register to 0x1 (reserved), then back to 0x4 (LPDDR2-S4) or 0x5 (LPDDR2-S2) according to memory configuration. This forces the controller back into its init state instead of self-refresh state.
  4. Reconfigure EMIF_SDRAM_REF_CTRL.REG_INITREF_DIS to 0.
  5. Perform normal init phase as from global cold reset.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.20. RTA Feature Is Not Supported

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i608

CRITICALITY

High

DESCRIPTION

RTA (retention till access) feature is not supported and leads to device stability issues when enabled.

The following modules are embedding memories with RTA support:

- MPU subsystem (cache memories)
- OCM RAM
- SGX
- Display subsystem
- HS USB OTG
- IVA-HD subsystem
- Face detect
- Imaging subsystem
- DMM
- DSP subsystem
- AESS

WORKAROUND

PRM_LDO_SRAM_<Memory Voltage Domain>_SETUP[0] DISABLE_RTA_EXPORT default value is loaded by an eFuse value. On OMAP4430 ES1.0 and ES2.0, this value enabled by default this RTA feature so these bits must be set to 0x1 as soon as the device is booted for correct operation. RTA should be disabled at boot time then consistently kept disabled. Starting with ES2.1 the fuse value disables this RTA feature, so these bits must be kept at default value.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.21. I/O Daisy Wakeup During Device Off Mode Transition Stalls The Device Power Transition

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i609

CRITICALITY

High

DESCRIPTION

If a wakeup from I/O daisy-chain is triggered in a specific short time window of the off mode transition (IOSwakeup internal signal asserted within one system clock cycle after go_in_offmode signal assertion), the device does not wake-up correctly and stays locked.

WORKAROUND

No

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Not impacted	Not impacted

1.22. Off Mode Power Consumption On VDD_WKUP

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i611

CRITICALITY

Medium

DESCRIPTION

In OMAP4 off mode (VDD_CORE=0V, VDD_WKUP=0.83V) VDD_WKUP power consumption exceeds estimation budget by approximately 100 µA. This is an isolation cell issue, which creates a leakage path from VDD_WKUP to VDD_CORE.

WORKAROUND

No

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Not impacted	Not impacted

1.23. Wkup Clk Recycling Needed After Warm Reset

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i612

CRITICALITY

Low

DESCRIPTION

Hardware does not recycle the I/O wake-up clock upon a global warm reset. When a warm reset is done, wakeups of daisy I/Os are disabled, but without the wake-up clock running, this change is not latched. Hence there is a possibility of seeing unexpected I/O wake-up events after warm reset.

WORKAROUND

Software must set bit WUCLK_CTRL in PRCM register PRM_IO_PMCTRL and it must poll on bit WUCLK_STATUS to become 1.

After this WUCLK_CTRL bit can be set back to 0 to enable/disable the wakeup feature for each pad.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.24. DMM Hang Issue During Unmapped Accesses

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i614

CRITICALITY

Medium

DESCRIPTION

DMM is assigned an address range of 2GB in the system address map. Internal registers (DMM_LISA_MAP_i) are used to program sections which define which part of the 2GB is actually mapped to external memories.

A mapped access is a request to an address which hits at least one DMM section. An unmapped access is a request to an address which does not hit any DMM section; DMM replies with an OCP error response in that case.

A hang occurs if an unmapped read is issued after a mapped read.

WORKAROUND

First software workaround: Do not issue unmapped read accesses.

An unmapped read to the DMM is due to an incorrect system address mapping in the MPU, most likely an invalid MMU setting. Therefore, impact should be limited to the chip debug phase.

Second software workaround: Define LISA section to have response error when unmapped addresses. Define LISA section in such a way that all transactions reach the EMIF, which will return an error response.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.25. HS USB Host HSIC Not Functional

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i620

CRITICALITY

High

DESCRIPTION

Due to timing issue, the HSIC interface of the HS USB Host is not functional.

The issue does not impact ULPI and TLL interfaces.

WORKAROUND

None

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.26. I2C SCL and SDA Glitch At Reset Release

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i622

CRITICALITY

High

DESCRIPTION

OMAP4430 will not boot in SYS_BOOT configurations involving USB or MMC1 due to negative glitches generated on I2C1 SCL and SDA lines after reset (nRESPWRON) deassertion.

This can be interpreted by a START command of the I2C protocol and Phoenix power management IC does not respond correctly to second and subsequent requests. The lack of response to the first request blocks the boot of OMAP.

Because I2C2/3/4 are impacted as well, side-effects on devices connected to those buses are possible.

This issue is caused by two things:

- Slew on the HHV internal signal of I/O which is too high. The HHV controls the state of I/O while power on reset is active.
- After reset release, I2C internal pullup is not activated.

Glitches duration is dependant on process, voltage, temperature conditions as well as the value of external pull-up resistors and can be higher than 50 ns with default OMAP pullup resistors.

WORKAROUND

For proper boot up of OMAP, customers must ensure that the size of glitches on I2C1 SCL/SDA are less than the 50 ns, as it will be filtered in Phoenix Power management IC.

Board pullup resistors on SCL/SDA lines must be adjusted to respect this timing. They must be calculated in respect of system parameters (I2C1 bus loading, strength of pullup of devices connected to the I2C bus)

The external pullup resistor value recommendation to fix the issue in most of the board configuration is: 1.8KOhm for a 10-pF load, 1KOhm for a 50-pF load, 450Ohm for a 100-pF load, and 100Ohm for 400-pF load.

The same analysis must be performed on I2C2/3/4 and the same recommendations can be applied to avoid side effects on connected I2C devices.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Not impacted

1.27. Retention/Sleep Voltage Transitions Ramp Time

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i623

CRITICALITY

Low

DESCRIPTION

In OMAP4, for each switchable voltage domain, two registers are specified:

- PRM_VOLTSETUP_<VD name>_OFF
- PRM_VOLTSETUP_<VD name>_RET_SLEEP

The first register specifies voltage ramp-up from OFF mode to ON mode, and ramp-down times from non-ON mode to OFF mode of the external regulator. The second register specifies voltage ramp-up from RET or SLEEP mode to ON mode, and ramp-down from ON mode to RET or SLEEP mode times of the external regulator. Times are specified in terms of system clock cycles through a prescaler (RAMP_*_PRESCAL) and count (RAMP_*_COUNT) values.

In RTL, prescaler of SLEEP-RET transition is always decoded like for OFF transition making granularity on ramp-up/down times a little bigger.

Because ramp-up/down times are of the order of tens of u-seconds, impact on PRCM functionality is minor.

Prescaler is specified over 2 bits, its decoding is:

OFF transition:

- 0x0: Ramp-up/down counter is incremented every 64 system clock cycles
- 0x1: Ramp-up/down counter is incremented every 256 system clock cycles
- 0x2: Ramp-up/down counter is incremented every 512 system clock cycles
- 0x3: Ramp-up/down counter is incremented every 2048 system clock cycles

SLEEP-RET transitions:

- 0x0: Ramp-down counter is incremented every 64 system clock cycles
- 0x1: Ramp-down counter is incremented every 256 system clock cycles
- 0x2: Ramp-down counter is incremented every 512 system clock cycles
- 0x3: Ramp-down counter is incremented every 2048 system clock cycles

WORKAROUND

None

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.28. Interrupt Enable Registers Not Restored

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i625

CRITICALITY

High

DESCRIPTION

When coming back from device off mode, the Cortex-A9 WUGEN enable registers are not restored by ROM code. The reset values are used instead.

This leads to increased/unexpected CPU1 wakeups and can prevent MPU low-power transitions.

WORKAROUND

Device OFF mode cannot be used in GP device.

The user can transition to the use of non-GP devices to avoid this issue and to use off mode in the system.

The user can use a GP device but use an alternative power state (instead of off mode) which maintains the proper register settings.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

1.29. MMCHS_HCTL.HSPE Is Not Functional

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i626

CRITICALITY

High

DESCRIPTION

Due to design issue MMCHS_HCTL.HSPE bit is not functional, this means that configuration is always the reset one "normal speed mode".

WORKAROUND

None

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

Chapter 2. Limitations

2.1. Transfer Of Multiple Command Packets Coming From L4/L3 Interconnect During A Blanking Period In Interleaving Mode

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i575

CRITICALITY

Low

DESCRIPTION

In video mode, the command mode packets, provided through the DSI protocol engine OCP port, can be interleaving during the blanking periods vertical and/or horizontal blanking periods of the video stream sequence.

When TX FIFO on the OCP slave port is empty and if the first packet written to TX FIFO is less than 13 words when 1 data lane is active or 17 words when 2 data lanes are active or 25 words when 3 or 4 data lanes are active, only this packet will be sent on the HS link during the next blanking period enabled for command packet transfer.

This is the only sent packet, because this packet is the only completely written packet when the FSM has read the last location of this packet from TX FIFO. Even if more packets are written in TX FIFO before the interleaving starts, these packets will not be sent during that blanking period.

WORKAROUND

No workaround is available. The impact is minor because:

- When interleaving is done on a vertical blanking period (VSA, VFP, VBP), as these blanking are expressed in a number of lines, the remaining packet(s) in TX FIFO are sent on HS link during the next line blanking interval within the same blanking period or during the next one.
- When interleaving is done on a horizontal blanking period (HSA, HFP, HBP), the remaining data in TX FIFO is sent on the next blanking period.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

2.2. Nonburst Video Mode Using Sync Pulses: NO HE Packets Sent VSA, VFP, And VBP Blanking.

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i576

CRITICALITY

Medium

DESCRIPTION

The DSI protocol engine is based on the MIPI DSI ver. 1.01 specification.

However the video mode using sync pulses is implemented using the timing described in MIPI DSI ver. 1.00 and not ver. 1.01:

- The DSI protocol engine sends only HE packets (when enabled) during VACT and not during VSA, VFP, and VBP.
- The DSI protocol engine sends VE (noted as VSE in MIPI DSI ver. 1.01 specification) during VSA and not during VBP.

Figure 2.1 represents actual implementation and Figure 2.2 represents MIPI DSI ver. 1.01 specification.

Figure 2.1. MIPI DSI 1.00 (Implemented) - Video Mode Interface Timing: Nonburst Transmission With Sync Start And End.

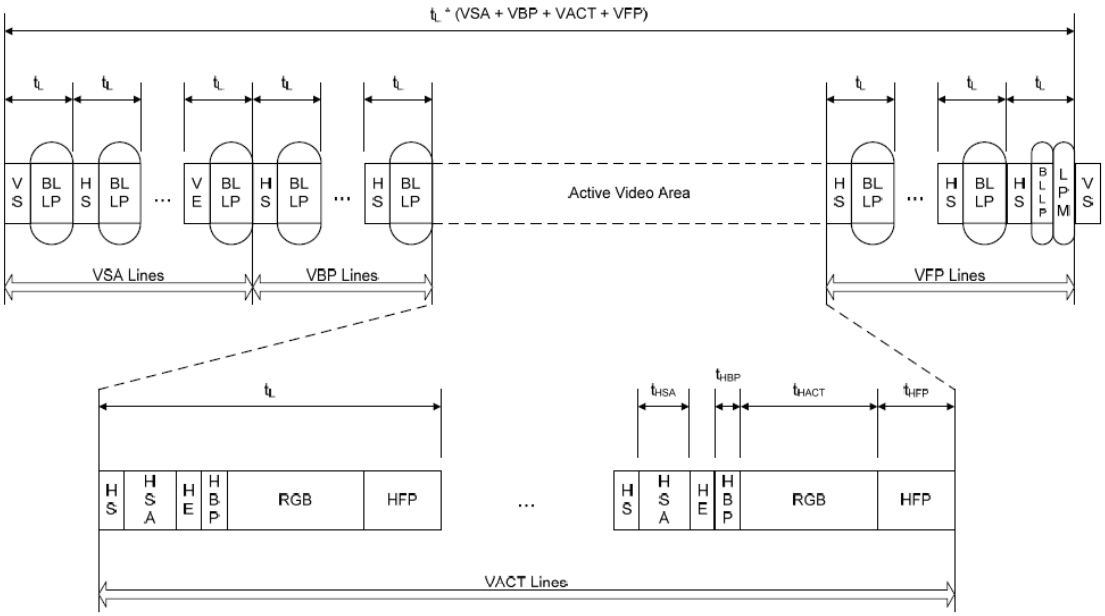
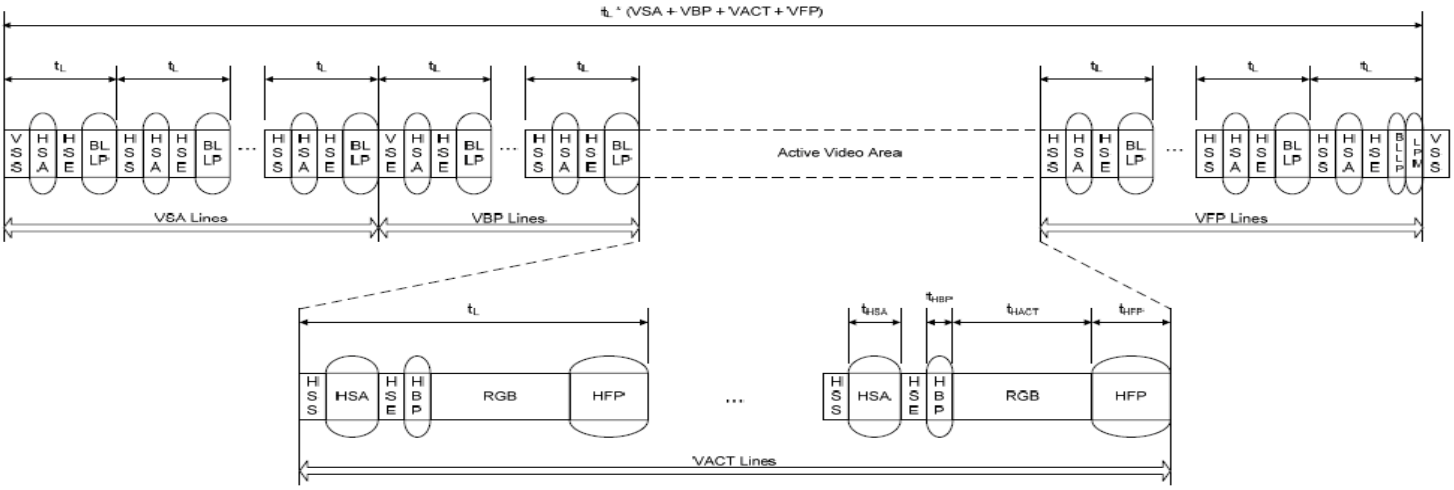


Figure 2.2. MIPI DSI 1.01 (Not Supported) - Video Mode Interface Timing: Nonburst Transmission With Sync Start And End.



WORKAROUND

NA

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

2.3. DPLL Fast Relock Idle Bypass Mode Not Supported

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i591

CRITICALITY

Medium

DESCRIPTION

CORE, MPU, IVA, ABE, and PER DPLLs are incorrectly controlled when switching to idle bypass power states. The ADPLL-M instances are forced to run in low-power mode when entering in idle bypass power state. To avoid a deadlock in the DPLLCtrl state-machine, fast relock mode must not be used.

WORKAROUND

For CORE, MPU, IVA, ABE, and PER DPLLs, the following registers programming must not be used:

- DPLL_EN = 6
- AUTO_DPLL_MODE = 2 or 6

For CORE DPLL, the following registers programming must not be used:

- CM_SHADOW_FREQ_CONFIG1.DPLL_CORE_DPLL_EN = 6
- CM_SHADOW_FREQ_CONFIG1_RESTORE.DPLL_CORE_DPLL_EN = 6

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

2.4. BITMAP1-2-4 Formats Not Supported By The Graphics Pipeline

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i596

CRITICALITY

Low

DESCRIPTION

BITMAP1, BITMAP2, and BITMAP4 are not supported by the graphics pipeline.

WORKAROUND

No workaround is available.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

2.5. Limitation On DISPC Dividers Settings When Using BITMAP Format

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i597

CRITICALITY

Low

DESCRIPTION

When Graphics pipeline input pixel is in BITMAP format, it cannot output pixel at the rate of one pixel per each clock cycle when LCD = 1 and PCD = 1.

The limitation is not applicable if PCD is greater than or equal to 2.

WORKAROUND

No workaround is available.

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

2.6. LPDDR2 Instability

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i615

CRITICALITY

High

DESCRIPTION

LPDDR2 memory accesses are not stable following two design issues on DQS:

- Improper control of the pullup/down resistors on DQS
- Excessive skew during the enable of the DQS

WORKAROUND

To have stable access the EMIF must work at 200 MHz on the LPDDR2 interface. This means that PHY_ROOT_CLK from DPLL_CORE must be programmed at 400 MHz.

Chip powerup and reset sequence begins:

- EMIF sends precharge command followed by MRW reset to memory.
- MPU completes EMIF configuration.

The following sequence is needed to set correctly pullup/down resistors on DQS:

1. Program the wd0/wd1 bits for the I/O as 1/1 (bus keeper mode). This ensures that the differential pads of DQS I/O cell are held at their last driven value.
   - CONTROL_LPDDR2IO1_1.LPDDR2IO1_GR6_WD = 0x11
   - CONTROL_LPDDR2IO1_1.LPDDR2IO1_GR7_WD = 0x11
   - CONTROL_LPDDR2IO1_1.LPDDR2IO1_GR8_WD = 0x11
   - CONTROL_LPDDR2IO1_2.LPDDR2IO1_GR9_WD = 0x11
   - CONTROL_LPDDR2IO2_1.LPDDR2IO2_GR6_WD = 0x11
   - CONTROL_LPDDR2IO2_1.LPDDR2IO2_GR7_WD = 0x11
   - CONTROL_LPDDR2IO2_1.LPDDR2IO2_GR8_WD = 0x11
   - CONTROL_LPDDR2IO2_2.LPDDR2IO2_GR9_WD = 0x11
2. Initialize the DQS inputs to a known value by a dummy read.
   - MR1 read for lpddr2 (dummy read for each channel) as an example
3. Issue a PHY reset to initialize FIFO pointers.

   Write 1 to bit 10 at the following address:
   - Assert PHY reset for EMIF1 @ x 4C00 0060
   - Assert PHY reset for EMIF2 @ x 4D00 0060

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Not impacted	Not impacted

2.7. HDQ™/1-Wire® Communication Constraints

ERRATA REFERENCE

Unique reference to be used for communication, Errata ID: i621

CRITICALITY

Medium

DESCRIPTION

HDQ/1-Wire protocols use a return-to-1 mechanism and it requires an external pullup resistor on the line. There is a timing limitation on this return-to-1 mechanism that requires a constraint on the external pullup resistor(R) and the capacitive load(C) of the wire.

WORKAROUND

There is a constraint in the design for the maximum allowed rise time of the wire. After writing data to the wire, the HDQ/1-Wire module samples the logic value of the wire 1 FSM (finite state machine) clock cycle later. The FSM expects to read back 1 value from the wire. This constraint must be taken into account, when calculating the pullup resistor(R) according to the capacitive load(C) of the wire.

The maximum RC (pullup resistor and capacitive load) value should be calculated as follow:

R <1200ns/(10e-12 + C)

REVISIONS IMPACTED

OMAP4430		
2.0	**2.1**	**2.2**
Impacted	Impacted	Impacted

Chapter 3. Cautions

The purpose of this section is to alert OMAP users about sensitive silicon concern. Items described in the following section comply with the specification (neither bug nor limitation), but it is mandatory to carefully respect guidelines to ensure correct OMAP behavior.

Appendix A. Errata per Chip Revision

A.1. Errata Impacting Revision 2.0 (36 Sections)

A.1.1. Bugs (29 Sections)

i339: Section 1.1, “DSI: Minimum Of 2 Pixels Should Be Transferred Through DISPC Video Port”

i340: Section 1.2, “DSI: Cancel Tearing Effect Transfer”

i341: Section 1.3, “DSI: RX FIFO Fullness”

i342: Section 1.4, “DSI: Access Restriction On DSI_TIMING2 Register”

i343: Section 1.5, “DSI: Tx FIFO Flush Is Not Supported”

i378: Section 1.6, “sDMA Channel Is Not Disabled After A Transaction Error”

i422: Section 1.7, “DSI SOF Packet Not Send”

i488: Section 1.8, “ISS: SOFTRESET Bit Status Not Working For Circular Buffer”

i489: Section 1.9, “ISS: SOFTRESET Bit Status Not Working For Burst Translation Engine”

i496: Section 1.10, “ISS State Can Be Corrupted During Debug Mode”

i483: Section 1.11, “DSI VSYNC HSYNC Detection In Video Mode”

i524: Section 1.12, “Dual Video Mode”

i525: Section 1.13, “Deadlock Between DISPC And DSI When PCD = 2, VP_CLK_RATIO = 0”

i588: Section 1.14, “McBSP Used In Slave Mode Can Create A Deadlock Situation When Doing Power Management”

i592: Section 1.15, “I2C: In SCCB Mode, Under Specific Conditions, The Module Might Hold The Bus By Keeping SCL Low.”

i593: Section 1.16, “I2C: Spurious Wake-Up Event When Sysclk Period Is Higher Than Ocpclk Period ”

i594: Section 1.17, “I2C: Wrong Behavior When A Data With MSB 0 Is Put In The FIFO Before A Transfer With SBLOCK Is Started ”

i595: Section 1.18, “I2C: After An Arbitration Is Lost, The Module Starts Incorrectly The Next Transfer Incorrectly”

i603: Section 1.19, “Deep Power-Down Support During Off Mode”

i608: Section 1.20, “RTA Feature Is Not Supported”

i609: Section 1.21, “I/O Daisy Wakeup During Device Off Mode Transition Stalls The Device Power Transition”

i611: Section 1.22, “Off Mode Power Consumption On VDD_WKUP”

i612: Section 1.23, “Wkup Clk Recycling Needed After Warm Reset”

i614: Section 1.24, “DMM Hang Issue During Unmapped Accesses”

i620: Section 1.25, “HS USB Host HSIC Not Functional”

i622: Section 1.26, “I2C SCL and SDA Glitch At Reset Release”

i623: Section 1.27, “Retention/Sleep Voltage Transitions Ramp Time”

i625: Section 1.28, “Interrupt Enable Registers Not Restored”

i626: Section 1.29, “MMCHS_HCTL.HSPE Is Not Functional”

A.1.2. Limitations (7 Sections)

i575: Section 2.1, “ Transfer Of Multiple Command Packets Coming From L4/L3 Interconnect During A Blanking Period In Interleaving Mode”

i576: Section 2.2, “Nonburst Video Mode Using Sync Pulses: NO HE Packets Sent VSA, VFP, And VBP Blanking.”

i591: Section 2.3, “DPLL Fast Relock Idle Bypass Mode Not Supported”

i596: Section 2.4, “BITMAP1-2-4 Formats Not Supported By The Graphics Pipeline ”

i597: Section 2.5, “Limitation On DISPC Dividers Settings When Using BITMAP Format”

i615: Section 2.6, “LPDDR2 Instability”

i621: Section 2.7, “HDQ™/1-Wire® Communication Constraints”

A.1.3. Cautions (0 Sections)

A.2. Errata Impacting Revision 2.1 (33 Sections)

A.2.1. Bugs (27 Sections)

A.2.2. Limitations (6 Sections)

i575: Section 2.1, " Transfer Of Multiple Command Packets Coming From L4/L3 Interconnect During A Blanking Period In Interleaving Mode"

i576: Section 2.2, "Nonburst Video Mode Using Sync Pulses: NO HE Packets Sent VSA, VFP, And VBP Blanking."

i591: Section 2.3, "DPLL Fast Relock Idle Bypass Mode Not Supported"

i596: Section 2.4, "BITMAP1-2-4 Formats Not Supported By The Graphics Pipeline "

i597: Section 2.5, "Limitation On DISPC Dividers Settings When Using BITMAP Format"

i621: Section 2.7, "HDQ™/1-Wire® Communication Constraints"

A.2.3. Cautions (0 Sections)

A.3. Errata Impacting Revision 2.2 (32 Sections)

A.3.1. Bugs (26 Sections)

i339: Section 1.1, “DSI: Minimum Of 2 Pixels Should Be Transferred Through DISPC Video Port”

i340: Section 1.2, “DSI: Cancel Tearing Effect Transfer”

i341: Section 1.3, “DSI: RX FIFO Fullness”

i342: Section 1.4, “DSI: Access Restriction On DSI_TIMING2 Register”

i343: Section 1.5, “DSI: Tx FIFO Flush Is Not Supported”

i378: Section 1.6, “sDMA Channel Is Not Disabled After A Transaction Error”

i422: Section 1.7, “DSI SOF Packet Not Send”

i488: Section 1.8, “ISS: SOFTRESET Bit Status Not Working For Circular Buffer”

i489: Section 1.9, “ISS: SOFTRESET Bit Status Not Working For Burst Translation Engine”

i496: Section 1.10, “ISS State Can Be Corrupted During Debug Mode”

i483: Section 1.11, “DSI VSYNC HSYNC Detection In Video Mode”

i524: Section 1.12, “Dual Video Mode”

i525: Section 1.13, “Deadlock Between DISPC And DSI When PCD = 2, VP_CLK_RATIO = 0”

i588: Section 1.14, “McBSP Used In Slave Mode Can Create A Deadlock Situation When Doing Power Management”

i592: Section 1.15, “I2C: In SCCB Mode, Under Specific Conditions, The Module Might Hold The Bus By Keeping SCL Low.”

i593: Section 1.16, “I2C: Spurious Wake-Up Event When Sysclk Period Is Higher Than Ocpclk Period ”

i594: Section 1.17, “I2C: Wrong Behavior When A Data With MSB 0 Is Put In The FIFO Before A Transfer With SBLOCK Is Started ”

i595: Section 1.18, “I2C: After An Arbitration Is Lost, The Module Starts Incorrectly The Next Transfer Incorrectly”

i603: Section 1.19, “Deep Power-Down Support During Off Mode”

i608: Section 1.20, “RTA Feature Is Not Supported”

i612: Section 1.23, “Wkup Clk Recycling Needed After Warm Reset”

i614: Section 1.24, “DMM Hang Issue During Unmapped Accesses”

i620: Section 1.25, “HS USB Host HSIC Not Functional”

i623: Section 1.27, “Retention/Sleep Voltage Transitions Ramp Time”

i625: Section 1.28, “Interrupt Enable Registers Not Restored”

i626: Section 1.29, “MMCHS_HCTL.HSPE Is Not Functional”

A.3.2. Limitations (6 Sections)

i575: Section 2.1, “ Transfer Of Multiple Command Packets Coming From L4/L3 Interconnect During A Blanking Period In Interleaving Mode”

i576: Section 2.2, “Nonburst Video Mode Using Sync Pulses: NO HE Packets Sent VSA, VFP, And VBP Blanking.”

i591: Section 2.3, “DPLL Fast Relock Idle Bypass Mode Not Supported”

i596: Section 2.4, “BITMAP1-2-4 Formats Not Supported By The Graphics Pipeline ”

i597: Section 2.5, “Limitation On DISPC Dividers Settings When Using BITMAP Format”

i621: Section 2.7, “HDQ™/1-Wire® Communication Constraints”

A.3.3. Cautions (0 Sections)

A.4. Errata Impacting All ICs Revision

Table A.1. Errata general table

Section	2.0	2.1	2.2
i339: Section 1.1, “DSI: Minimum Of 2 Pixels Should Be Transferred Through DISPC Video Port”	Impacted	Impacted	Impacted
i340: Section 1.2, “DSI: Cancel Tearing Effect Transfer”	Impacted	Impacted	Impacted
i341: Section 1.3, “DSI: RX FIFO Fullness”	Impacted	Impacted	Impacted
i342: Section 1.4, “DSI: Access Restriction On DSI_TIMING2 Register”	Impacted	Impacted	Impacted
i343: Section 1.5, “DSI: Tx FIFO Flush Is Not Supported”	Impacted	Impacted	Impacted
i378: Section 1.6, “sDMA Channel Is Not Disabled After A Transaction Error”	Impacted	Impacted	Impacted
i422: Section 1.7, “DSI SOF Packet Not Send”	Impacted	Impacted	Impacted
i488: Section 1.8, “ISS: SOFTRESET Bit Status Not Working For Circular Buffer”	Impacted	Impacted	Impacted
i489: Section 1.9, “ISS: SOFTRESET Bit Status Not Working For Burst Translation Engine”	Impacted	Impacted	Impacted
i496: Section 1.10, “ISS State Can Be Corrupted During Debug Mode”	Impacted	Impacted	Impacted
i483: Section 1.11, “DSI VSYNC HSYNC Detection In Video Mode”	Impacted	Impacted	Impacted
i524: Section 1.12, “Dual Video Mode”	Impacted	Impacted	Impacted
i525: Section 1.13, “Deadlock Between DISPC And DSI When PCD = 2, VP_CLK_RATIO = 0”	Impacted	Impacted	Impacted
i588: Section 1.14, “McBSP Used In Slave Mode Can Create A Deadlock Situation When Doing Power Management”	Impacted	Impacted	Impacted
i592: Section 1.15, “I2C: In SCCB Mode, Under Specific Conditions, The Module Might Hold The Bus By Keeping SCL Low.”	Impacted	Impacted	Impacted
i593: Section 1.16, “I2C: Spurious Wake-Up Event When Sysclk Period Is Higher Than Ocpclk Period ”	Impacted	Impacted	Impacted
i594: Section 1.17, “I2C: Wrong Behavior When A Data With MSB 0 Is Put In The FIFO Before A Transfer With SBLOCK Is Started ”	Impacted	Impacted	Impacted
i595: Section 1.18, “I2C: After An Arbitration Is Lost, The Module Starts Incorrectly The Next Transfer Incorrectly”	Impacted	Impacted	Impacted
i603: Section 1.19, “Deep Power-Down Support During Off Mode”	Impacted	Impacted	Impacted
i608: Section 1.20, “RTA Feature Is Not Supported”	Impacted	Impacted	Impacted
i609: Section 1.21, “I/O Daisy Wakeup During Device Off Mode Transition Stalls The Device Power Transition”	Impacted	Not impacted	Not impacted
i611: Section 1.22, “Off Mode Power Consumption On VDD_WKUP”	Impacted	Not impacted	Not impacted
i612: Section 1.23, “Wkup Clk Recycling Needed After Warm Reset”	Impacted	Impacted	Impacted
	Impacted	Impacted	Impacted

Section	2.0	2.1	2.2
i614: Section 1.24, “DMM Hang Issue During Unmapped Accesses”			
i620: Section 1.25, “HS USB Host HSIC Not Functional”	Impacted	Impacted	Impacted
i622: Section 1.26, “I2C SCL and SDA Glitch At Reset Release”	Impacted	Impacted	Not impacted
i623: Section 1.27, “Retention/Sleep Voltage Transitions Ramp Time”	Impacted	Impacted	Impacted
i625: Section 1.28, “Interrupt Enable Registers Not Restored”	Impacted	Impacted	Impacted
i626: Section 1.29, “MMCHS_HCTL.HSPE Is Not Functional”	Impacted	Impacted	Impacted
i575: Section 2.1, “ Transfer Of Multiple Command Packets Coming From L4/L3 Interconnect During A Blanking Period In Interleaving Mode”	Impacted	Impacted	Impacted
i576: Section 2.2, “Nonburst Video Mode Using Sync Pulses: NO HE Packets Sent VSA, VFP, And VBP Blanking.”	Impacted	Impacted	Impacted
i591: Section 2.3, “DPLL Fast Relock Idle Bypass Mode Not Supported”	Impacted	Impacted	Impacted
i596: Section 2.4, “BITMAP1-2-4 Formats Not Supported By The Graphics Pipeline ”	Impacted	Impacted	Impacted
i597: Section 2.5, “Limitation On DISPC Dividers Settings When Using BITMAP Format”	Impacted	Impacted	Impacted
i615: Section 2.6, “LPDDR2 Instability”	Impacted	Not impacted	Not impacted
i621: Section 2.7, “HDQ™/1-Wire® Communication Constraints”	Impacted	Impacted	Impacted

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