Application of TMS320C6400 in 3G Wireless Infrastructure Transceiver (BTS)

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Outline

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- 3G BTS Architecture
- C6400 Features
- Symbol-Rate functions on C6400
  - CRC Encoding/Decoding
  - Convolutional/Turbo Encoding/Decoding
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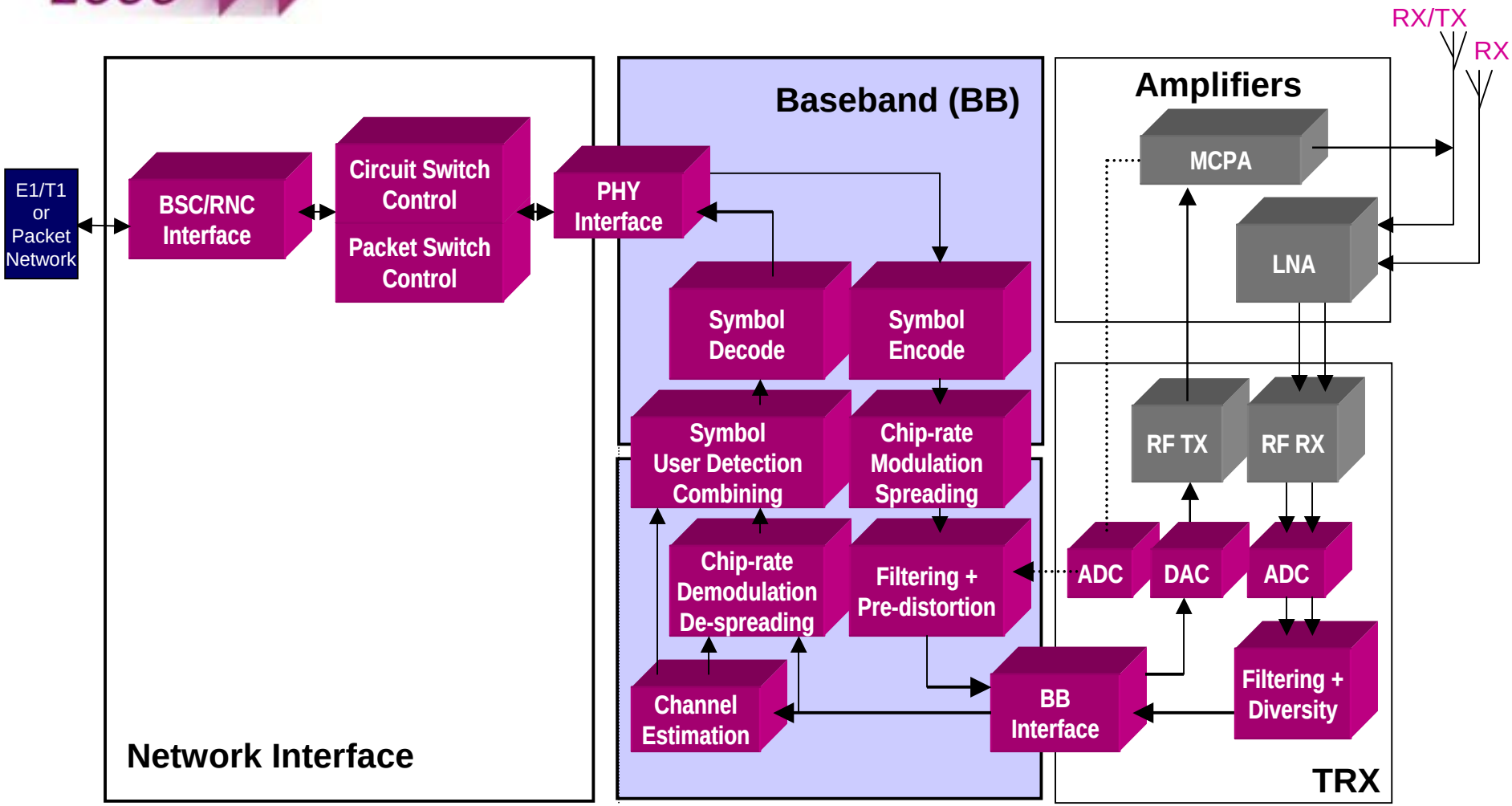
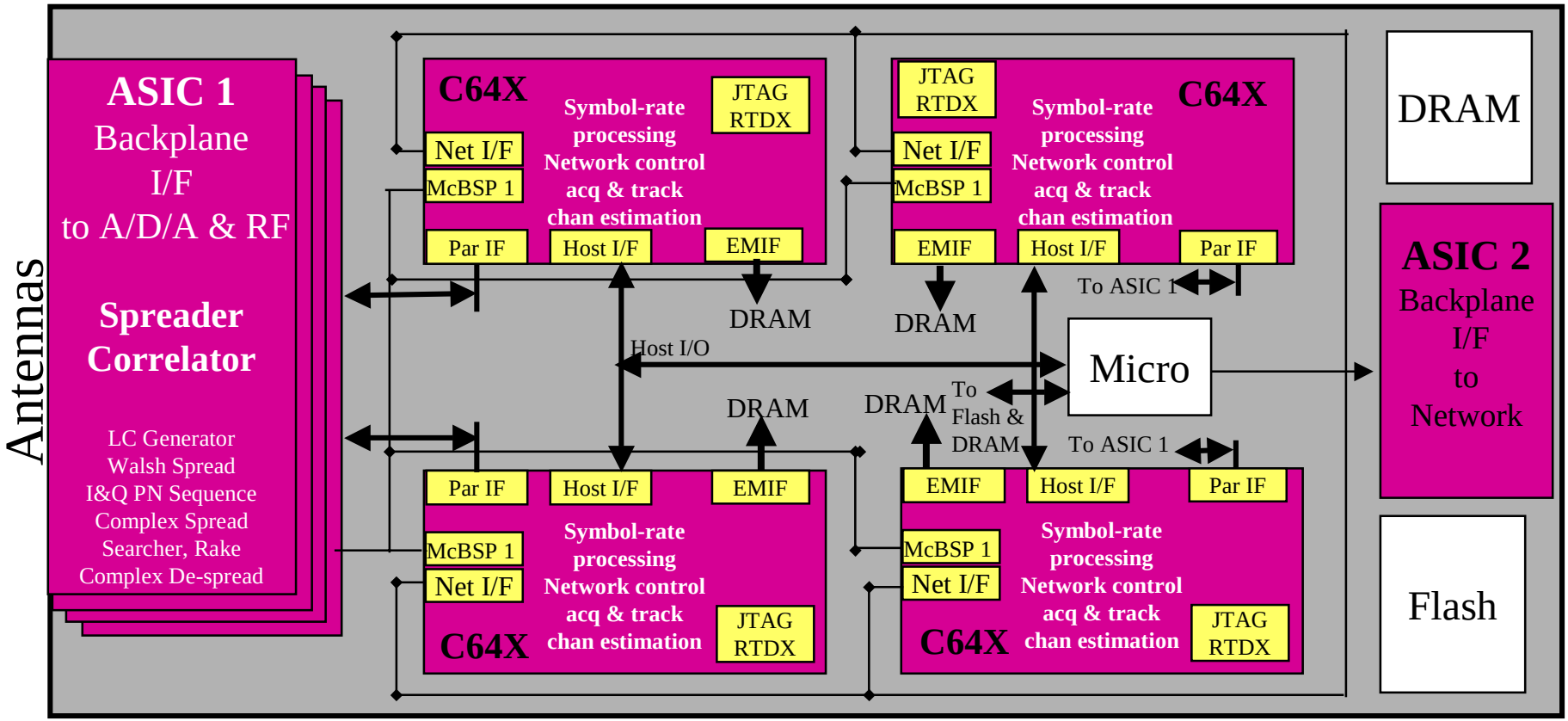
  - Rate Matching
- Summary and Conclusion

3G BTS Functionality



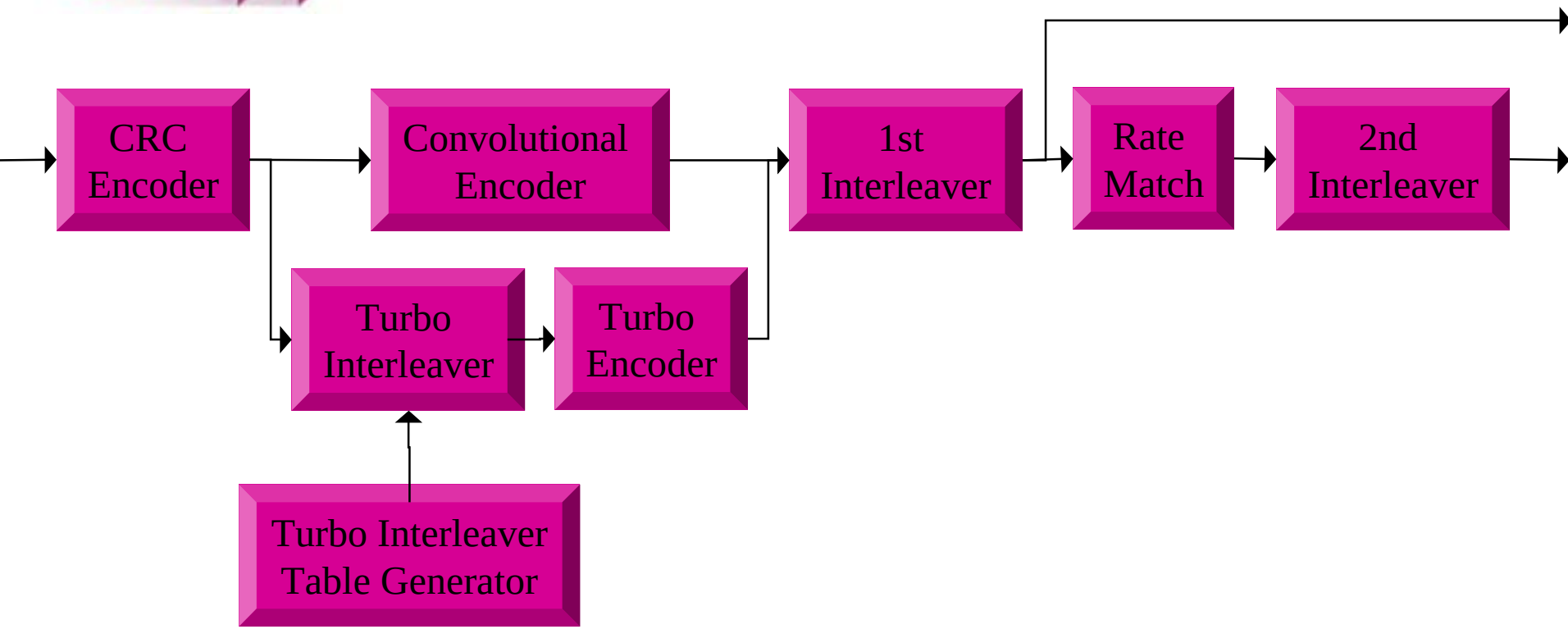
3G BTS Baseband Architecture



C6400 Features

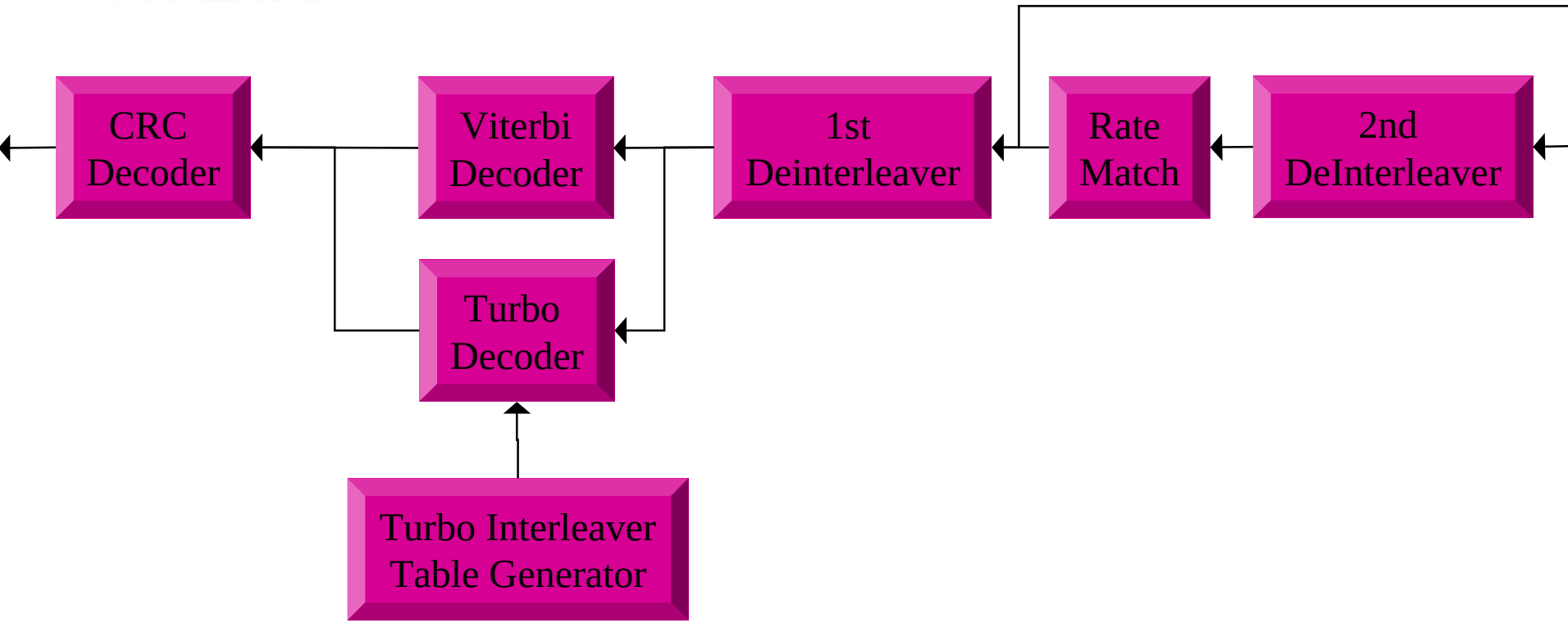
- Scalable speed up to 1.1GHz - firdt device at 800MHz
- Software compatible with C62X (re-use all the existing code), but:
  - More flexible resources (instructions available across more functional units);
  - New special-purpose instructions (Gmpy4, Deal, Swap4, Bitc4);
  - Extended parallelism (SIMD, pack/unpack,non-aligned loads);
  - Program code saving enhancements (special branch instructions, execution spans packet boundaries);
  - Double the bandwidth (64 registers, 64 bit data paths);
- Advanced emulation (non-intrusive debug, RTDX);
- Fast development environment with eXpressDSP.
- Diverse set of peripherals: multliple parallel and serial I/O s
- Two-level cache (L2, L1D/L1P) - various sizes

Symbol-Rate Functions - TX



- low user data rate (voice) or high user data rate (data)
- 3GPP or cdma2000

Symbol-Rate Functions - RX



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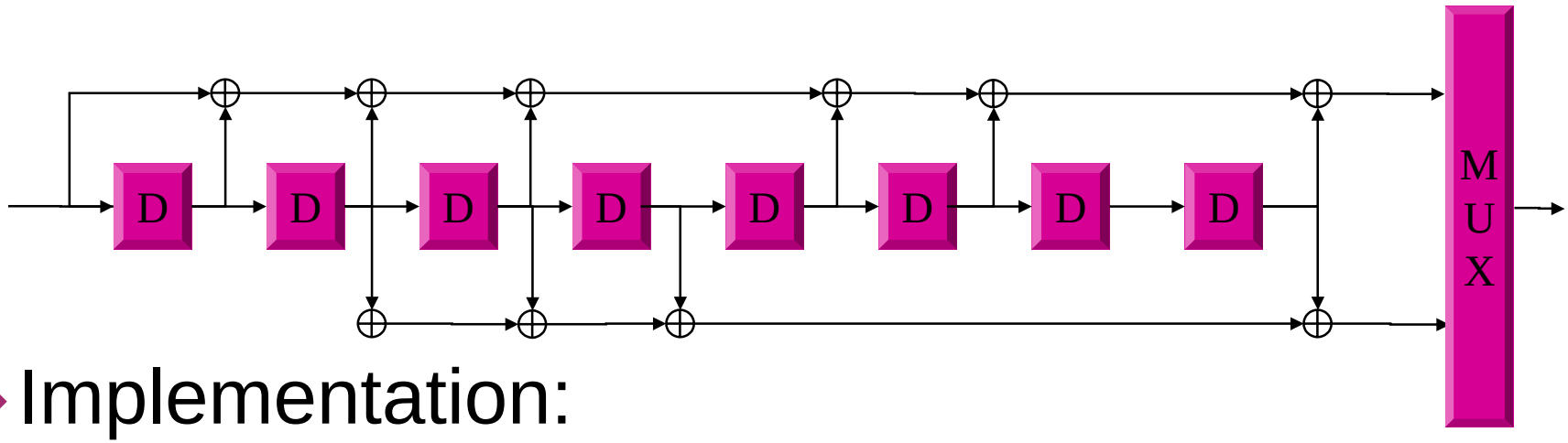
CRC

- Algorithm:
  - Cyclic Redundancy Check
  - 8th,12th or 16th order generator polynomial
- Implementation:
  - Based on look-up table;
  - 512 bytes for 16th order generator polynomial
  - native C code
    - 38 cycles / 32 input bits

Convolutional Encoder

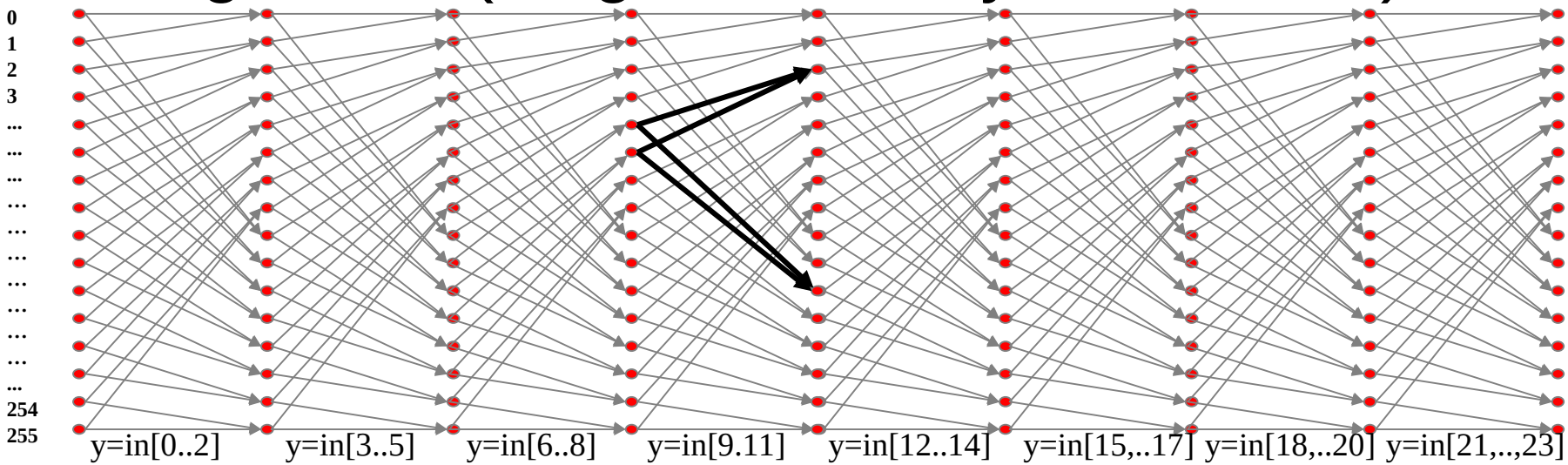
- Algorithm



- Implementation:
  - block-XOR operation (16 bits at a time)
  - tuned C, uses _pack2() and _shfl() intrinsics
    - 12 cycles/32 bits for rate 1/2
    - 37 cycles/32 bits for rate 1/3

Viterbi Decoder

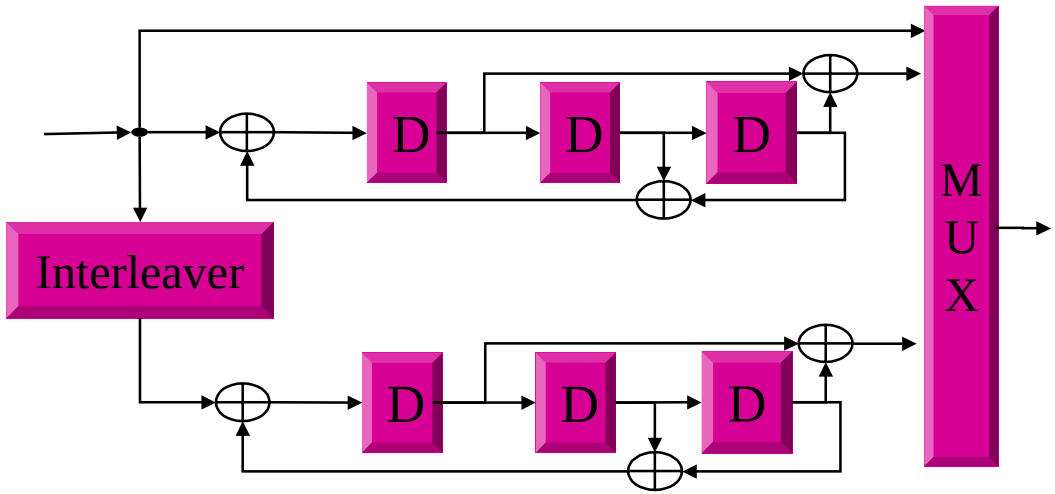
- Algorithm (stages, butterfly, traceback)



- Implementation
  - (10 cycles/8 butterflies)*128 butterflies / stage
  - 5 cycles for branch metrics/stage
  - 5 cycles for traceback/stage

Turbo Encoder

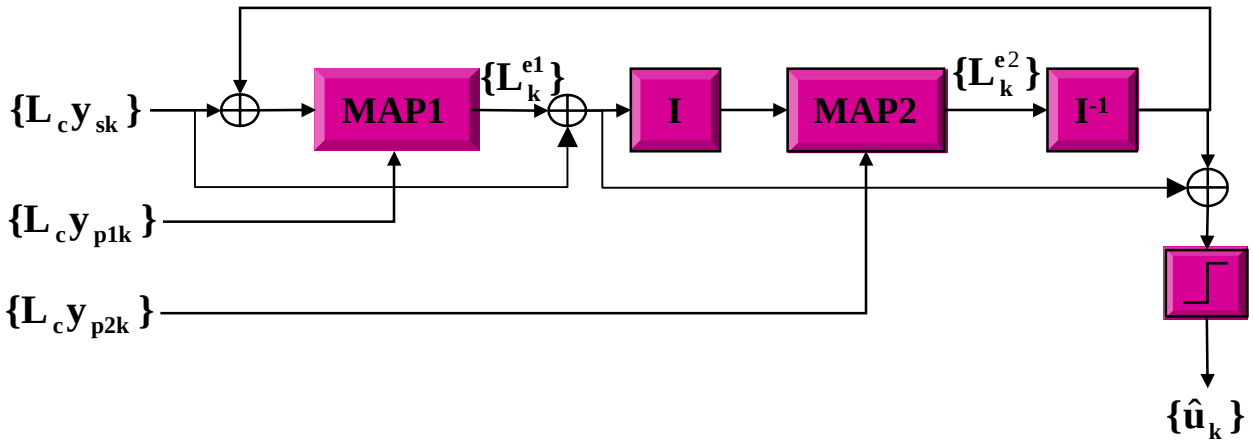
- Algorithm



- Implementation:
  - bit-wise XOR (block-wise XOR not possible)
  - tuned C, uses _rotl()
    - rate 1/2: 8 cycles/bit
    - rate 1/3: 9.7 cycles/bit

Turbo Decoder

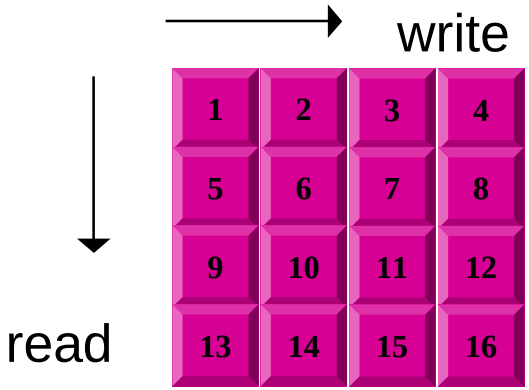
- Algorithm (high-level decoder)



- Implementation
  - 32-bit alpha/beta/extrinsic accumulations
  - tuned C (inner loop unrolling)
    - max*: 10 cycles/alpha/stage; 20 cycles/(beta+extrinsic)/stage
    - max : ~40% less than max*

Interleaving/Deinterleaving

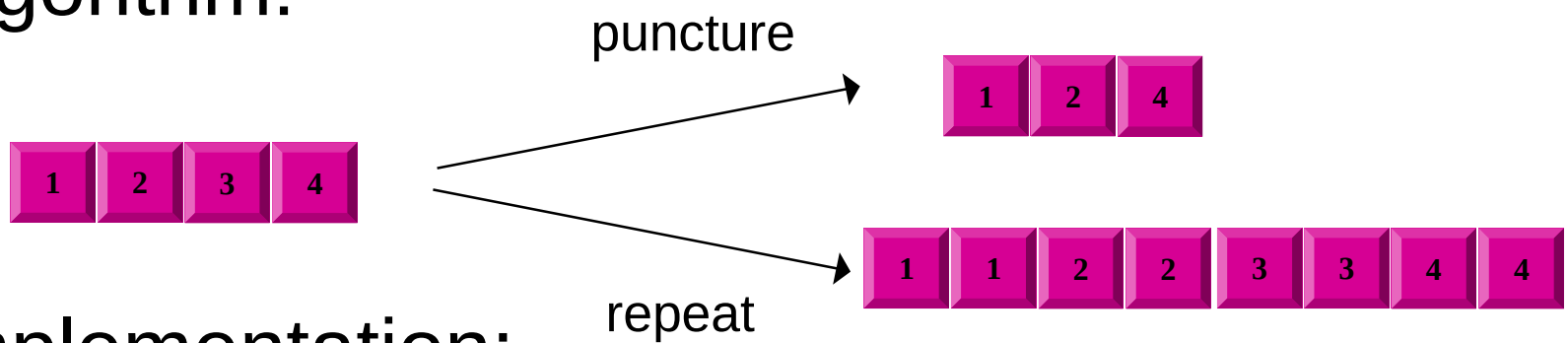
- Algorithm (block interleaver)



- Implementation
  - Interleaver operates on bits
  - Deinterleaver operates on bytes
    - tuned C, deinterleaver uses _pack4(); _unpack4()
  - Only small lookup tables required (64 bytes)

Rate Matching

- Algorithm:



- Implementation:
  - bit-level operation:
    - tuned C, uses _sshvr() and _bitr()
    - 4-5 cycles/bit
  - byte-level operation
    - native C
    - 3 cycles/bit

Performance Summary

FUNCTION		CPU Performance (MHz)			
		3GPP		cdma2000	
		voice	data	voice	data
Transmitter	CRC Encoder	0.04	0.47	0.02	0.37
	Convolutional Encoder	0.02	N/A	0.01	N/A
	Turbo Interleaver	N/A	1.17	N/A	1.00
	Turbo Encoder	N/A	3.75	N/A	2.47
	1st Interleaver	0.06	2.31	0.08	1.28
	Rate Match	0.17	4.65	N/A	N/A
	2nd Interleaver	0.11	1.97	N/A	N/A
	TOTAL	**0.40**	**14.32**	**0.11**	**5.12**
Receiver	2nd Deinterleaver	0.04	0.04	N/A	N/A
	Rate Dematch	0.12	0.12	N/A	N/A
	1st Deinterleaver	0.01	0.01	0.02	0.55
	Viterbi Decoder	1.50	N/A	1.40	N/A
	Turbo Decoder	N/A	225.00	N/A	180.00
	CRC Decoder	0.04	0.04	0.03	0.38
	TOTAL	**1.71**	**225.21**	**1.44**	**180.93**

- Data Rates
  - voice = 8kbps (3GPP), 9.6kbps (cdma2000)
  - data = 384kbps(3GPP), 307.2kbps(cdma2000)
- Memory model
  - flat memory model, close in performance to data/program in L1D/L1P
  - if data is in L2, average degradation is 5-7%

Conclusions

- At 800 MHz, C6400 can support symbol-rate processing of:
  - 2-3 384kbps channels
  - 320-400 voice channels
- A multistandard solution could consist of:
  - one C6400 for all symbol-rate processing
  - one ASIC for each standard for chip-rate processing