Thermally Enhanced ICs

Low Cost Plastic Package Improves Surface-Mount IC Cooling

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CMOS components have historically operated at low thermal power – typically less than one watt – due to the modest operating voltages, current, gate count, and operating frequency of the part. The thermal power for a component can be approximated by adding the power for the internal gates of the device to that generated in the input/output (IO) structures. Using the power approximation of a switched gate and knowing that only about 15% to 20% of the total gates of a circuit switch in any clock cycle, the internal power generated in the circuit can be easily determined. The IO power uses the same formula, adjusted by the assumption that at least 80% of the IOs will switch on each clock cycle.

Switched Gate Power Approximation = $[CV^2 \times f]N$

where:

C = Capacitance in pF

V = Switched voltage (V)

f = Switching frequency in Hz

N = number of gates switched/clock cycle

Results of examples created using 100 to 700 IO, 10000 to 5000000 gates, frequencies from 100MHz to 500MHz, and operating bias supply voltages from 5V to 1.8V are shown in *Figure 1* and *Figure 2*. The significance of the number of operating IOs on thermal power must be taken into account as the major source of heat generated in an integrated circuit . The switching power of the internal gates of the IC only becomes a dominating factor when a very large number of gates are used with respect to the number of IOs required.

The general trend in the industry is to reduce the operating bias voltage to get the benefit of reduced thermal and electrical power requirements for a given circuit, but in many cases, this potential saving is used to accommodate enhanced features or higher device operating frequencies. The net result of this activity is equal or higher thermal power as implemented in the system.

PowerPAD™ packages provide a cost effective method for improving traditional plastic package heat transfer from the semiconductor device junction to the p. c. board.

Conventional Packages

The semiconductor industry has created a number of variations in basic plastic packages to serve the various needs of the components contained within the packages and the connection to the p. c. board utilized in the system application. Relatively simple package cross sections can be used to understand the principles of the construction and the potential for thermal management for each of the options. *Figure 3* represents the principles found in the majority of plastic packages ranging from the standard package with only inherent thermal capability due to the leadframe material, to the case where a copper slug is attached to the lead fingers within the package and exposed to the outside world at the bottom of the package.

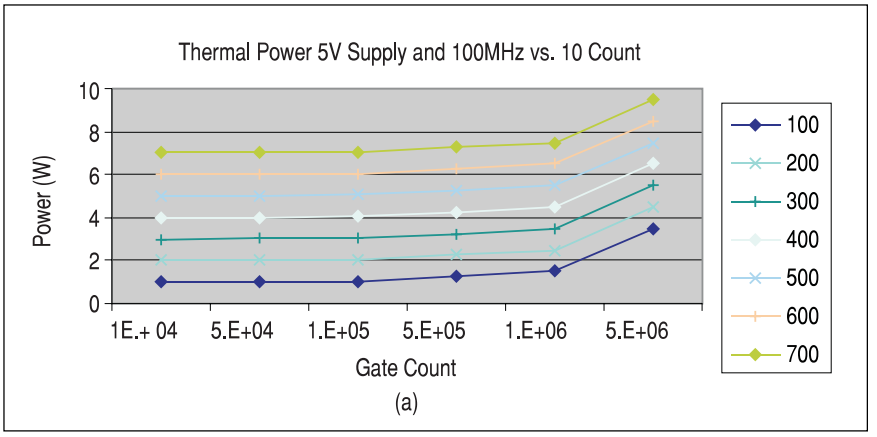
Each of the thermally enhanced

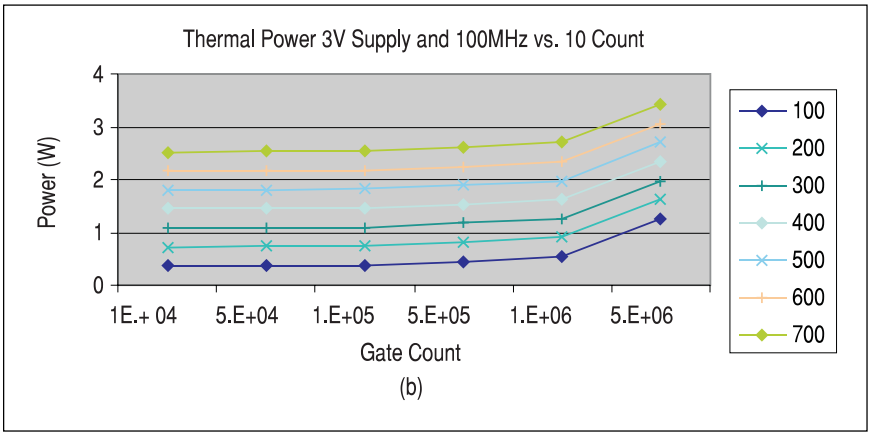
packages shown in *Figure 3* take heat away from the transistor junction of the chip with the efficiency improving as you go from *Figure 3(a)*, the standard package representation, to *Figure 3(f)*, the PowerPAD™ representation. The Drop-in Heat Spreader shown in *Figure 3(b)* provides improvement by adding metal within the package to help carry the heat closer to the lead fingers of the leadframe, with added improvement in *Figure 3(c)* – Leadframe Attached Heat Spreader – with the metal of the heat spreader replacing the conventional die pad of the leadframe and creating a very short distance between the lead fingers and this metal feature. The Drop-in Heat Slug in *Figure 3(d)* provides improvement by creating a path from the die pad of the leadframe to the external surface of the package with a metal (typically copper) slug, and the Leadframe Attached Heat Slug of *Figure 3(e)* creates an additional path for heat to the lead fingers of the leadframe. Each of these versions adds cost and complexity to the package assembly to gain the improvement in thermal removal efficiency.

The PowerPAD™ concept in *Figure 3(f)* solves the problem of heat removal without adding complexity to the package construction (heat spreaders or heat slugs), or adding the cost of the added elements. The thermal path to the outside world is the shortest possible, resulting in superior package thermal efficiency with a very simple construction.

With a standard package configuration 80% of the heat is removed by conduction through the leads of the package while only 20% is removed by convection from the body of the package. When a Leadframe Attached Heat Slug configuration is employed, 76% of the heat is removed through the package leads by conduction, and the remaining 24% by convection. This would be improved if the package slug can be soldered to the PCB, but most package slugs do not have a solderable surface.

In the TI PowerPAD™ package, 87% of the heat is removed from the package by conduction with the remaining 13% dissipated through convection from the external surfaces. The die pad of this package is easily soldered to a thermal land on the surface of the p.c. board with the heat removal limited





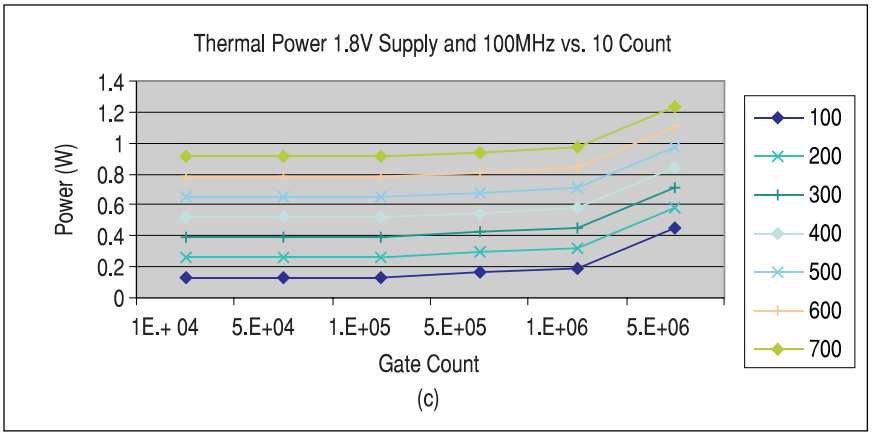
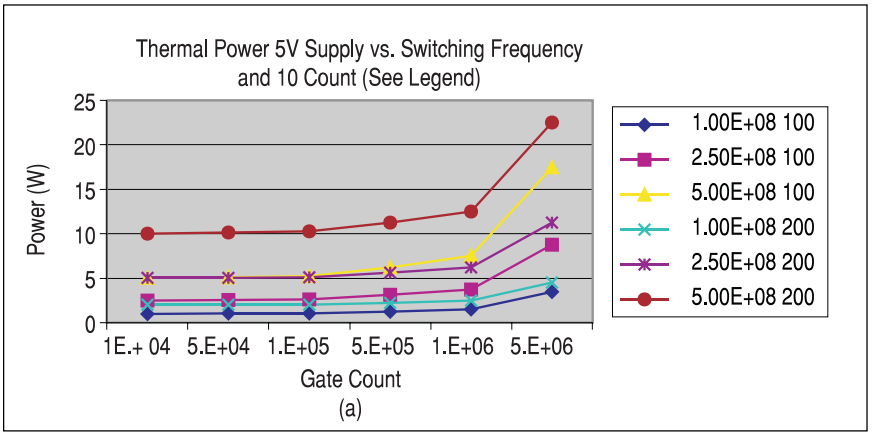
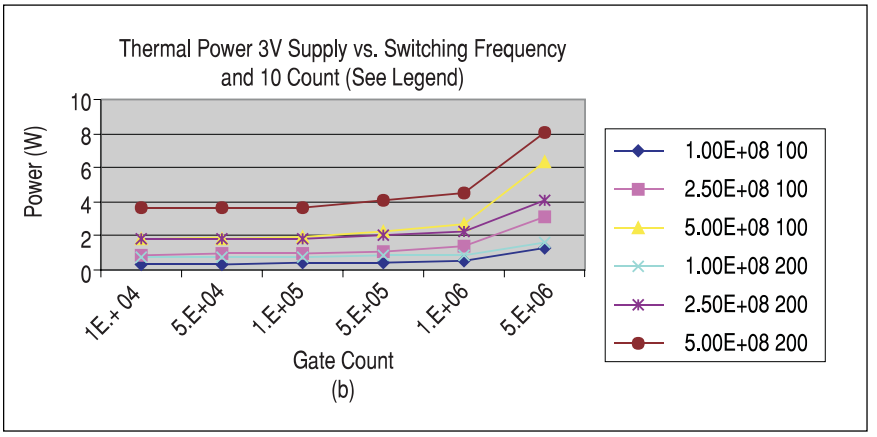


Figure 1. *The impact of the IO count and the gate count of an integrated circuit operating at 100MHz on the thermal power of candidate circuits is shown with (a) 5.0V bias supply; (b) 3.0V bias supply and (c) 1.8V bias supply.*





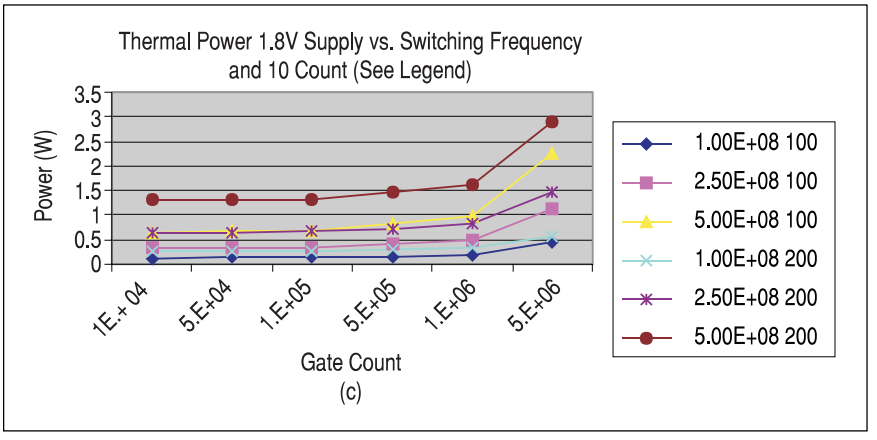


Figure 2. *Reduction in thermal power at a given gate count and number of IO can result in a large reduction in system power handling requirements. (a) 5.0V bias supply; (b) 3.0V bias supply and (c) 1.8V bias supply.*

only by the board's efficiency and system level thermal management process.

Heat Removal

Heat generated within the semiconductor lowers the circuit's operating performance (at higher temperatures, the transistor operation degrades due to increased resistances in material properties). This can reduce long-term reliability of the package/circuit combination. Thus, for best operation it is important to move the heat away from the transistor junctions as efficiently as possible.

Standard plastic packages use the leads of the package as the primary heat removal mechanism, with the metal of the leadframe carrying the heat away from the internal sites to the outside world by conduction. *Figure 4* shows the heat removal in this style package. The traditional rule that 80% of the heat is removed through the leads with the remaining 20% removed through the package body by convection continues to be valid for this package. Adding external heat spreaders to the package body will only impact the 20% problem, and is usually applied when only marginal improvement of heat removal is required.

The thermal efficiency of the package can be significantly improved by providing a thermal path directly to the surface of the package. This is shown in *Figure 5* by the leadframe attached heat slug implementation. In this variation, a metal slug is attached to the lead fingers of the leadframe internal to the package body with an adhesive tape material. This replaces the traditional die pad of the leadframe. The chip is mounted to the metal slug with a thermally conductive adhesive material. The resulting construction provides an effective thermal path away from the chip at the cost of added materials within the package, and increased package weight – both of which are undesirable features in a semiconductor package solution. Another limitation is its inability to solder the exposed portion of the metal slug to a p.c. board thermal land because many of the viable metal slug versions do not have a solderable surface finish available for this connection.

Employment of the PowerPAD shown in *Figure 6* overcomes the deficiencies of the heat spreader or heat slug packaging methodologies and results in a low cost, thermally efficient package solution. No added components are required for the implementation, resulting in assembly operations equivalent to the standard package versions, and the thermal path length is reduced to a minimum. The bottom of the die pad is exposed at the

package body surface, and can be easily soldered to a thermal land on the p. c. board. Packages created using this methodology cover the spectrum commonly used for semiconductors, with exactly the same handling characteristics as the standard package versions that the industry commonly uses (size, weight, form factor, reliability, etc.).

Figure 7 shows an enlarged cross section of a PowerPAD package. *Figure 8* shows the top and bottom of the 20-pin TSSOP PowerPAD package that was first introduced in 1995. This version has the four corner package leads tied to the die pad for enhanced thermal efficiency (a standard option in PowerPAD packages), in addition to the die pad exposed at the surface of the package body.

Package styles and lead counts available for use with PowerPAD features include virtually all standard leaded surface-mount package types used in the semiconductor industry. The newer thin package versions (<2.0mm body thickness) such as MSOP (8 and 10 pins), TSSOP (8 through 100 pins), LQFP (32 through 256 pins), and TQFP (32 through 256 pins), are readily suited for use with this technology. Thinner packages in the future – VSSOP, VQFP (0.8mm body thickness), and USSOP, UQFP (<0.8mm body thickness) will easily employ the PowerPAD solution. Both chip-up and chip-down versions are easily implemented to support the thermal removal requirements of the component, board, and system solutions. New package versions are added as required.

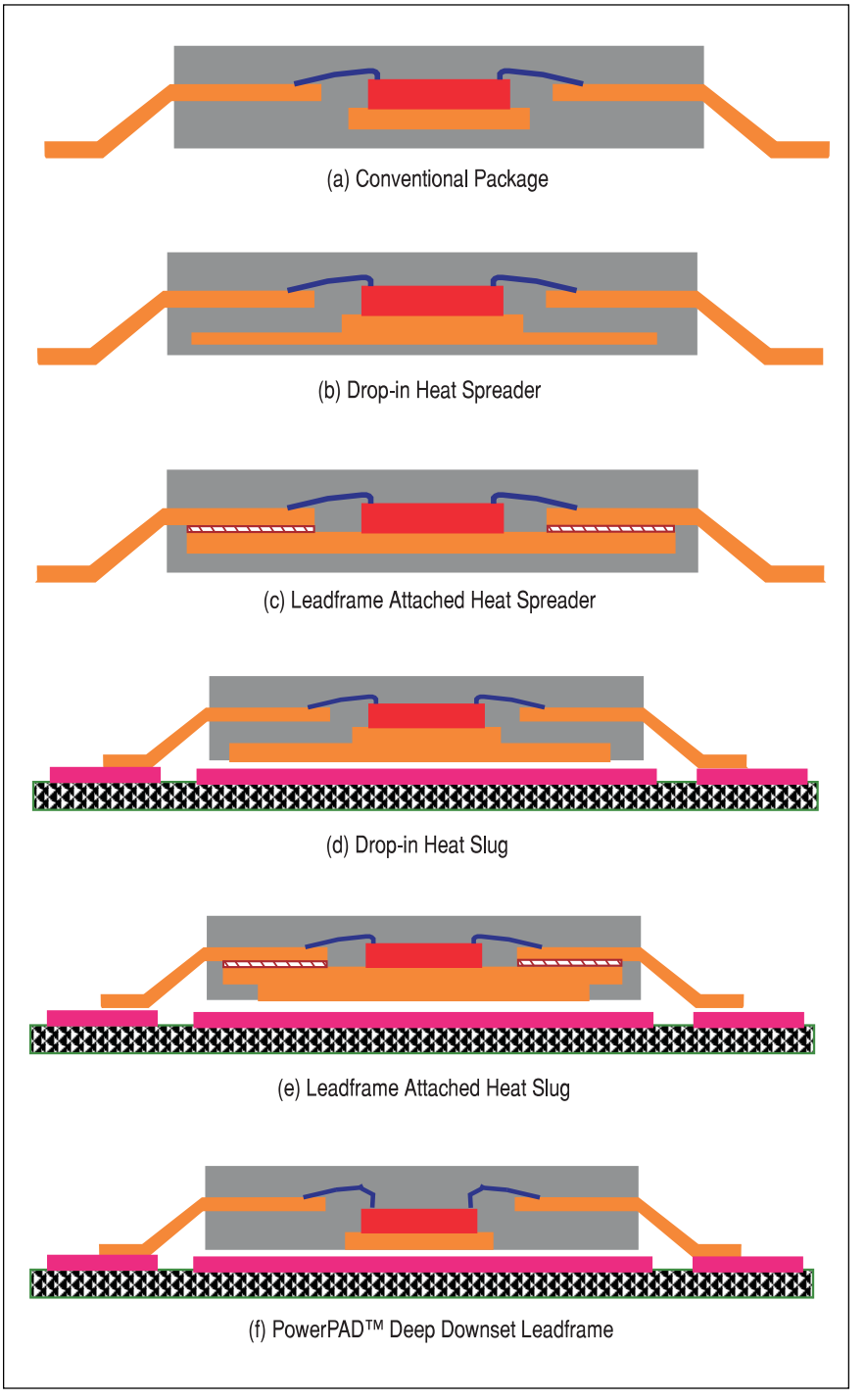


Figure 3. *Simplified representations of plastic semiconductor packaging methods for removal of thermal energy from the silicon chip to the outside world. (a) Conventional package; (b) Drop-in heat spreader; (c) Leadframe attached heat spreader; (d) Drop-in heat slug; (e) Leadframe attached heat slug and (f) PowerPAD deep downset leadframe.*

Package Creation

Most semiconductor packages in the industry today for through-hole or surface-mount applications start construction with a metal (typically copper) leadframe consisting of a number of lead fingers continuing from the package external leads to the interior of the package, and a die pad that the chip attaches to. The die pad is downset to a position within the package to allow for equal mold compound flow above and below the chip/die pad combination.

The PowerPAD package uses a downset of the die pad to the point that the bottom surface of the die

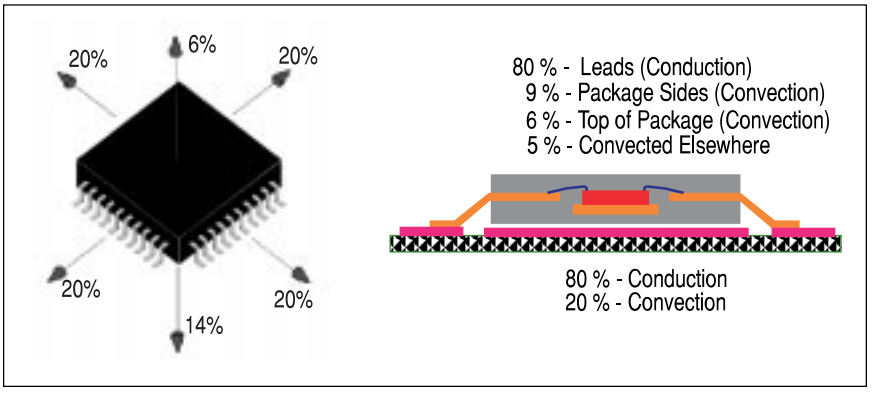


Figure 4. *Representation of the path followed in removing heat from a standard package.*

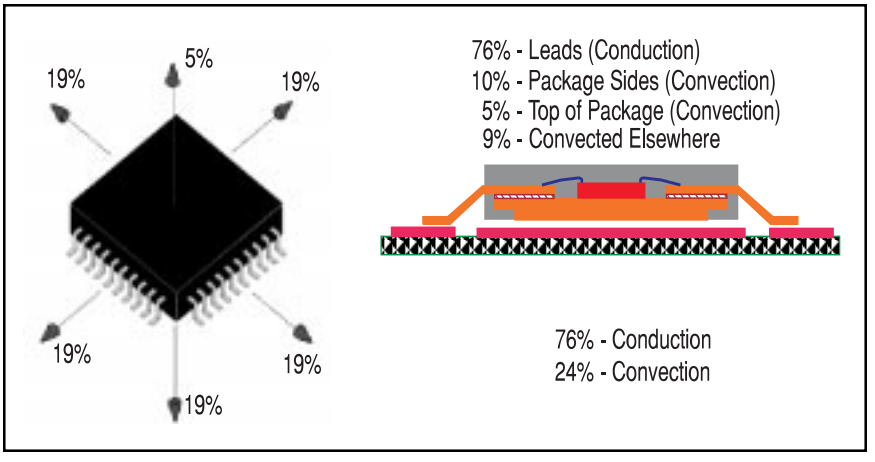


Figure 5. *Leadframe attached heat slug configuration.*

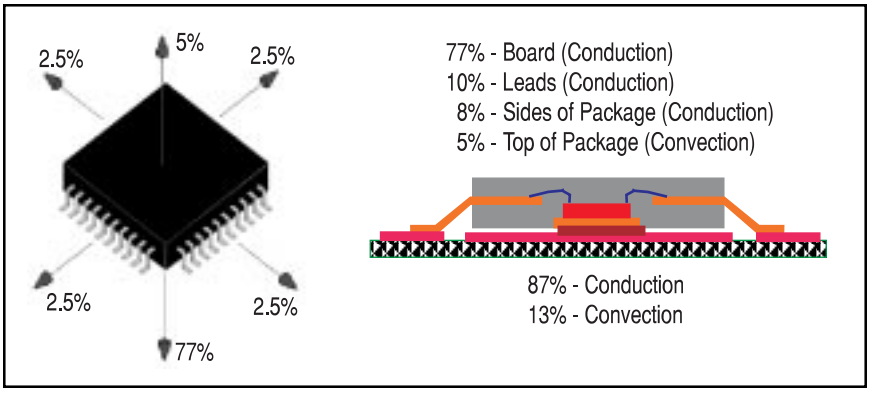


Figure 6. *PowerPAD package configuration.*

pad is exposed at the bottom surface of the package to create an optimum thermal path from the chip to the outside of the package body. Key attention must be paid to the leadframe material properties to allow this level of downset without cracking or breaking the tie strap that holds the die pad in position prior to the molding process. However, this simple extension of the die pad to the package surface generally results in an unreliable package implementation.

Features must be incorporated in the die pad design to provide a highly reliable package. Major features include a method to:

- Prevent molding material flash or bleed from covering the exposed die pad during the molding operation (otherwise, the thermal benefits of this structure will be lost)
- Lock the die pad into the package (to prevent the chip/die pad from being pushed out of the package during temperature or power cycling)
- Assure moisture performance of the molded plastic package (prevent popcorn effects and bond pad corrosion within the package)

All these methods have been included in the PowerPAD design to the effect that reliability and performance levels continue to meet those achieved by the low power standard configurations of the same packages.

Assembly Considerations

Assembly of PowerPAD components to a p.c. board was a priority during the development of the package concept. The goal was to use industry standard practices for the board design, construction, and assembly processes, and requiring changes only to incorporate thermal management features. Examples of the p. c. board layout are shown in *Figure 10* for a single layer TSSOP style board and in *Figure 11* for a multilayer LQFP/TQFP style board. The single layer board case illustrates the extension of the thermal land on the surface of the board beyond the body dimension of the semiconductor. This provides additional area for board heat removal by convection without having to add thermal vias within the board, or implementing features on the backside of the board.

A package such as the 64PAP PowerPAD shown in *Figure 11* normally requires a multilayer p.c. board for thermal removal because device leads are on all four sides. The vias connect the

surface thermal land to the ground plane within the board, which will act as the thermal spreader for heat removal, or may continue to features on the back side of the board for more efficient heat removal to other system components. *Figure 12* shows an example p.c. board thermal lands for use with PowerPAD or other thermally enhanced packages. The number of thermal vias shown is the theoretical maximum for each land pattern based on 1.5mm via pitch. These vias connect either to an internal ground plane, or to a plane on the back side of the board for thermal removal.

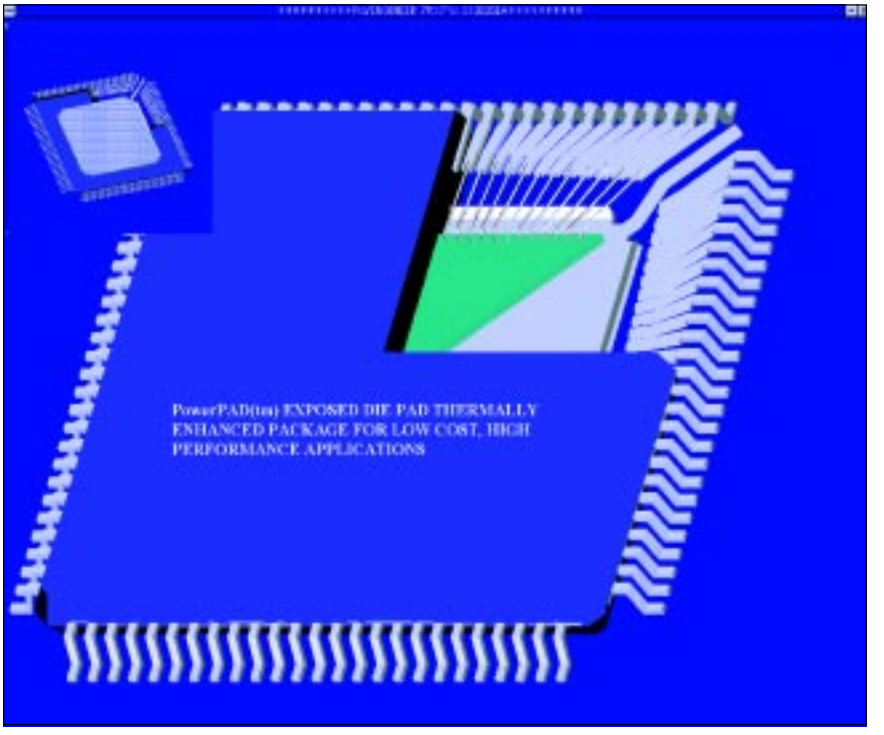


Figure 9. *100 pin TQFP PowerPAD package.*

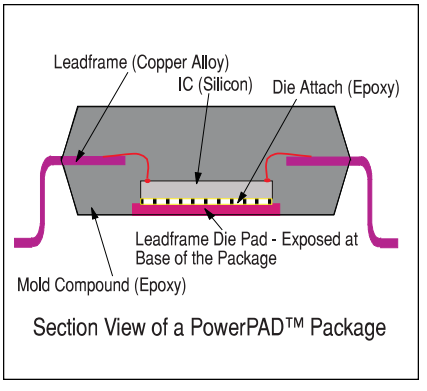


Figure 7. *Cross section of PowerPAD package.*

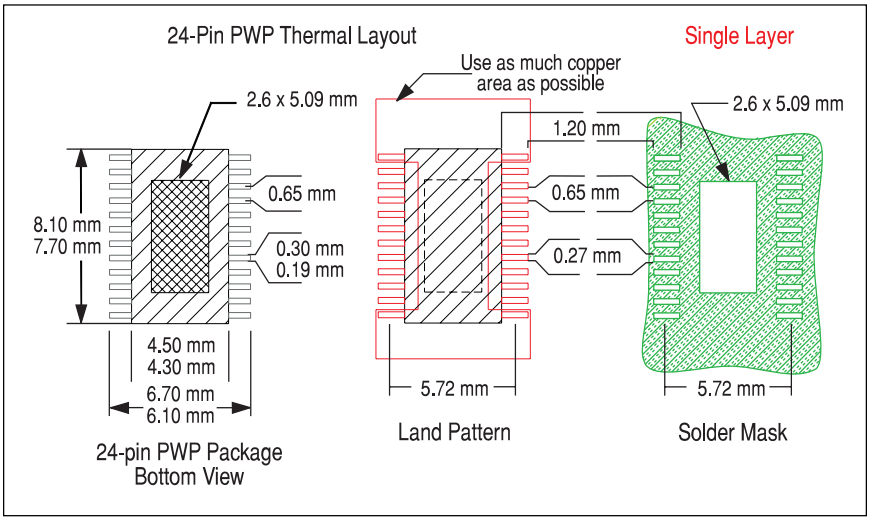


Figure 10. *Example of p.c . board features for the PowerPAD 24-pin TSSOP.*

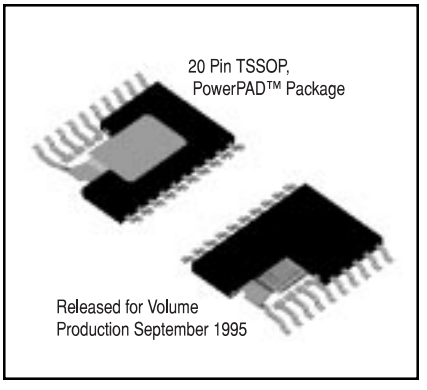


Figure 8. *Top and bottom section view of the 20 pin TSSOP PowerPAD package.*

Component assembly of PowerPAD packages to the p.c. board follows normal industry practice with no special considerations for solder paste thickness or reflow profiles required to achieve high quality attachment. Also, rework can be performed when needed after assembly using conventional component removal and replacement techniques. It should be noted that the thermally enhanced p. c. board normally used with thermally enhanced packages can sometimes make it difficult to re-solder a component to the board unless the whole board is reprocessed through the normal reflow. An alternative to solder attachment in this rework case is the use of thermally conductive epoxy materials (such as used with externally applied heat sinks) for the at-

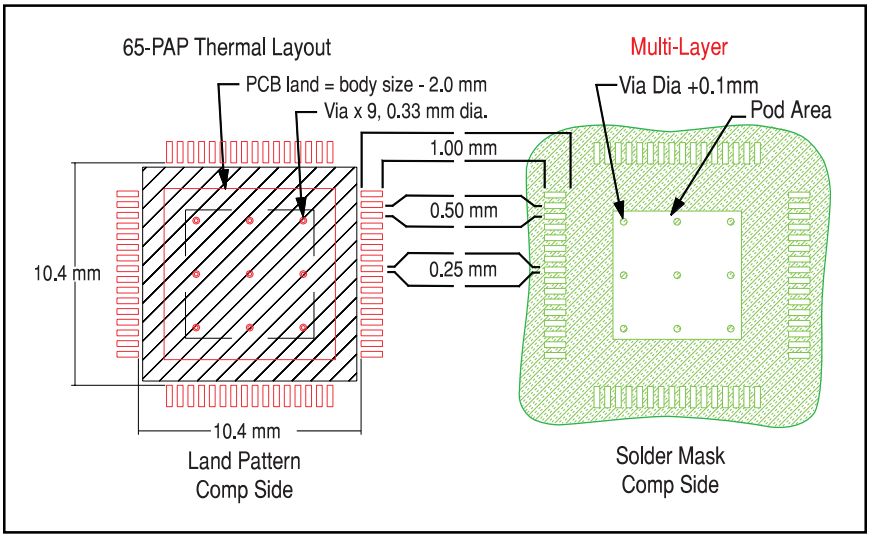


Figure 11. *P.c. board layout for a 64 pin PowerPAD TQFP with thermal vias and the approximate thermal land size with respect to the package body size.*

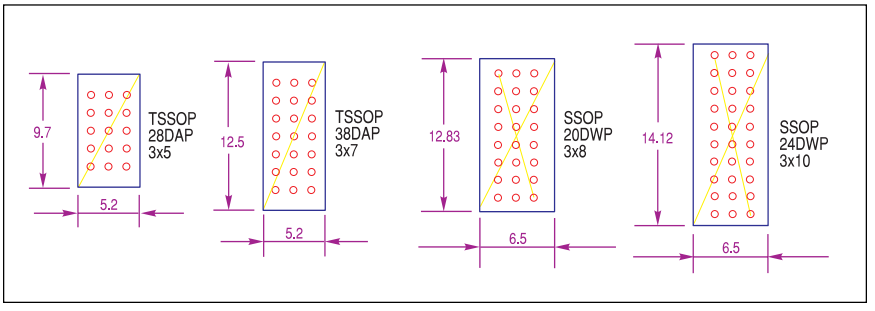


Figure 12. *Typical PCB thermal land and via patterns for use with thermally enhanced packages.*

tachment of the package thermal pad to the thermal land on the board.

References

Additional information about the Texas Instruments PowerPAD package can be found on the TI Internet Web page at http://www.ti.com/. Just search for "PowerPAD."

PowerPAD™ is a trademark of Texas Instruments, Incorporated.