A Fast, Efficient Synchronous-Buck Controller for Microprocessor Power Supplies

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ABSTRACT

A new fast and efficient buck-controller for microprocessor power supplies has been developed and tested under anticipated Intel workstation/server/desktop next-generation microprocessor operating conditions. The operating conditions include 12V input, 2V output, at maximum 20A load. The TPS5210 power supply control IC uses a ripple regulator control algorithm with droop compensation to tightly regulate the output voltage under both static and dynamic loading conditions. With the wide loop bandwidth of the ripple regulator, the load transient response is limited only by propagation delays and the output LC filter design. High efficient power conversion is accomplished by elimination of the series sense resistor commonly found in current-mode topologies and in topologies that use buried resistors to adjust the droop compensation setting. Design guidelines along with a design example are provided demonstrating the actual versus anticipated performance.

1. INTRODUCTION

Upcoming workstations driven by next-generation Intel microprocessors may require from 40 – 80 watts of power for the CPU alone. These workstation CPU power supplies may be fed off a 12V bus. Although the typical supply output voltage may be 2V, the supply should still be capable of providing an output voltage range from 1.3V to 3.5V - determined by a 5 bit DAC code. Parasitic interconnect impedances between the power supply and the processor must be kept to a minimum [1] since maximum current could be anywhere from 20A to 40A. Load current must be supplied with up to 30 A/μs slew rate while keeping the output voltage within tight regulation and response time tolerances [2]. The TPS5210 controller topology was optimized for tight Vout regulation under static and dynamic load conditions and for improved system efficiency, and can operate in systems that derive main power from either 12V, 5V, or 3.3V.

Conventional synchronous regulator control techniques include fixed frequency voltage-mode, fixed frequency current-mode, variable frequency current-mode, variable on-time only (constant off-time), or variable off-time only (constant on-time) control. CPU power supplies that are designed with these type of controllers require additional bulk storage capacitors on the output to maintain Vout within the regulation limits during the high di/dt load transients because of the limited bandwidth of the controller. Some controllers integrate a fast loop around the slower main control loop to improve the response time, but Vout must fall outside a fixed tolerance band before the fast loop becomes active.

2. TPS5210 CONTROLLER OPERATION

The TPS5210 is a controller for a high-performance ripple regulator. A simplified block diagram of the ripple regulator is given in figure 1. The main function blocks are shown: synchronous–buck gate drivers with adaptive deadtime control, 1% reference, hysteresis control, droop compensation control, and current sense control.

The main control block is a fast comparator with a hysteresis that is symmetrical about the reference voltage. Excluding delays, the high-side gate drive signal will toggle on when the instantaneous output voltage decreases below the lower hysteresis limit, Vlo; the gate drive signal will toggle off when the instantaneous output voltage increases above the upper hysteresis limit, Vhi. The hysteresis is symmetrical with respect to the reference voltage. The controller regulates the DC voltage level to the reference value while also regulating the ripple voltage on Vout. The ripple regulator provides a fast response to load transients and is well suited as a controller for CPU power supplies. The operating frequency of the ripple regulator depends upon Vin, Vout, the output inductor and the output capacitors and is very predictable because Vin typically has a 5% regulation limit in CPU systems. A section in this paper describes how to predict the operating frequency with design equations.

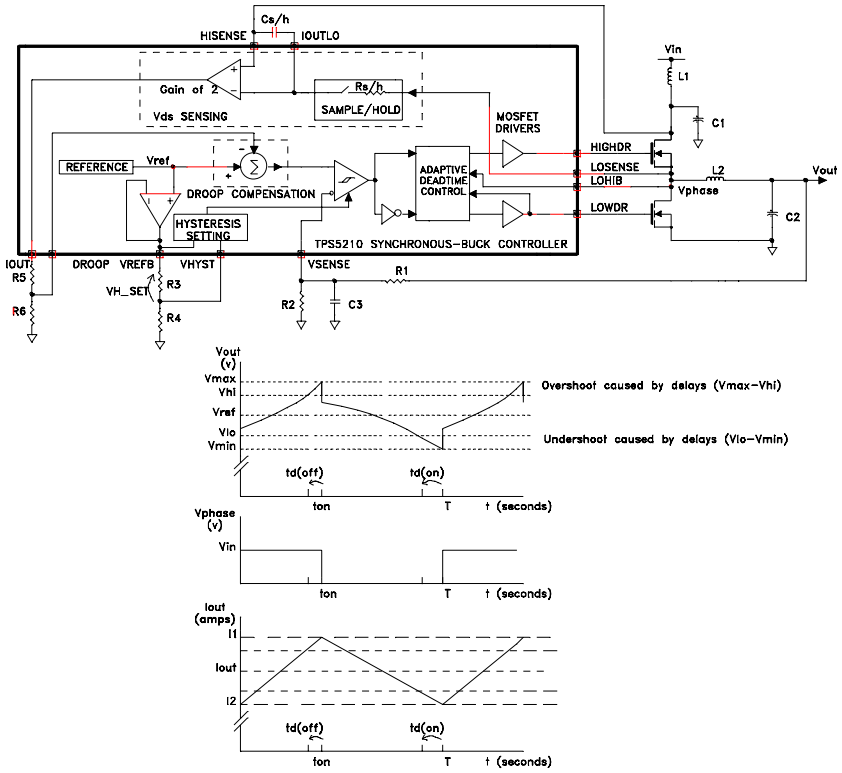


Figure 1. Simplified block diagram of the TPS5210 controller, and its ideal waveforms: Vout, Vphase, I(L2).

Delays in the feedback path will cause the ripple voltage to be higher than the level set by the controller. The source of the delays include the propagation delay from the comparator inputs to the MOSFET driver outputs (250ns max), the turn-on/turn-off delays of the power FETs, the non-overlap delay time of the deadtime control circuit (100ns max), and the delay from the external RC filter between Vout and the VSENSE pin (R1 and C3 in figure 1). The ripple voltage will be regulated to Vmax-Vmin. This extra window margin should be taken into account when determining the programmed window versus the final desired window.

The hysteresis window is set with a voltage divider from the buffered reference (VREFB); the hysteresis window is equal to twice the difference voltage between VREFB and VHYST (V_{H_SET} in figure 1). The hysteresis window is set to a percentage of Vref within the hysteretic comparator.
The synchronous-buck drivers have adaptive deadtime control to minimize the conduction time through the body-drain diode of the low-side FET, and prevent simultaneous conduction of the power MOSFETs which would cause shoot-through currents.
The output current is indirectly sensed by sampling and holding the voltage across the high-side FET. The RC time constant of the sample/hold switch resistance and hold capacitor is set to be greater than the conduction time of the high-side FET so that the average voltage across the high-side FET is sampled, which is proportional to the DC output current. The differential voltage across the sample/hold capacitor is amplified by 2 and converted to a single-ended signal on the IOUT pin; the voltage on IOUT is proportional to the output current.
The DROOP compensation circuit provides additional margin to maintain Vout within the load transient tolerance limits required by the processor. Vout is offset above the reference by the resistor divider from Vout to VSENSE (R1 and R2 in fig 1). The voltage on the DROOP pin is made proportional to the load current by the resistor divider from IOUT to DROOP (R5 and R6 in fig 1) such that Vout will be offset below the reference under full-load conditions. Test results that illustrate the advantage of DROOP compensation during a transient load will be shown later in the paper.

Operation of the hysteretic controller relies on the output ripple voltage waveform characteristics. The output voltage will exhibit an ac waveform riding on the average dc waveform. The ac component will be influenced predominantly by the output capacitor ESL, ESR, and capacitance values in conjunction with the inductor ripple current. The output voltage is composed of:

$$\text{vout}(t) = \text{Vdc} + \text{vac}(t) = \text{Vdc} + \text{ESL} \cdot \frac{d(i_{ripple}(t))}{dt} + \text{ESR} \cdot i_{ripple}(t) + \frac{1}{\text{Cout}} \cdot \int i_{ripple}(t)dt$$

The ripple component from ESL causes the voltage steps; ESR causes the ramps; and capacitance causes the curvature in the ripple voltage during the switching transitions, as shown in figure1. A more detailed analysis of the switching frequency and output voltage waveforms is given in section 5 “Switching Frequency of a Hysteretic Converter” and Appendix.

3. SYSTEM PERFORMANCE

Figure 2 shows the schematic for the evaluation circuit used to demonstrate the performance of the TPS5210 under typical server application operating conditions; namely, Vin=12V, Vout=2.0V, Iout=20A peak. Table 1 lists the critical components for the power supply design of figure 2.

Component Designator	Description
Q1 - Q5	Si4410
C2 - C4	470uF, 16v Sanyo OS-CON #16SA470M
L1	8 turns 18AWG on Micrometals T44-8 / 90 toroid
L2	7 turns 16AWG on Micrometals T68-8 / 90 toroid
C12 - C15	820uF, 4v Sanyo OS-CON #4SP820M
C16 - C19	10uF, 16v ceramic; Murata #GRM235Y5V106Z16
C5-C7,C25,C26,C28	1uF, 16v; Panasonic #ECSH1CY105R

Table 1. Critical component list for the evaluation power supply design of Figure 2.

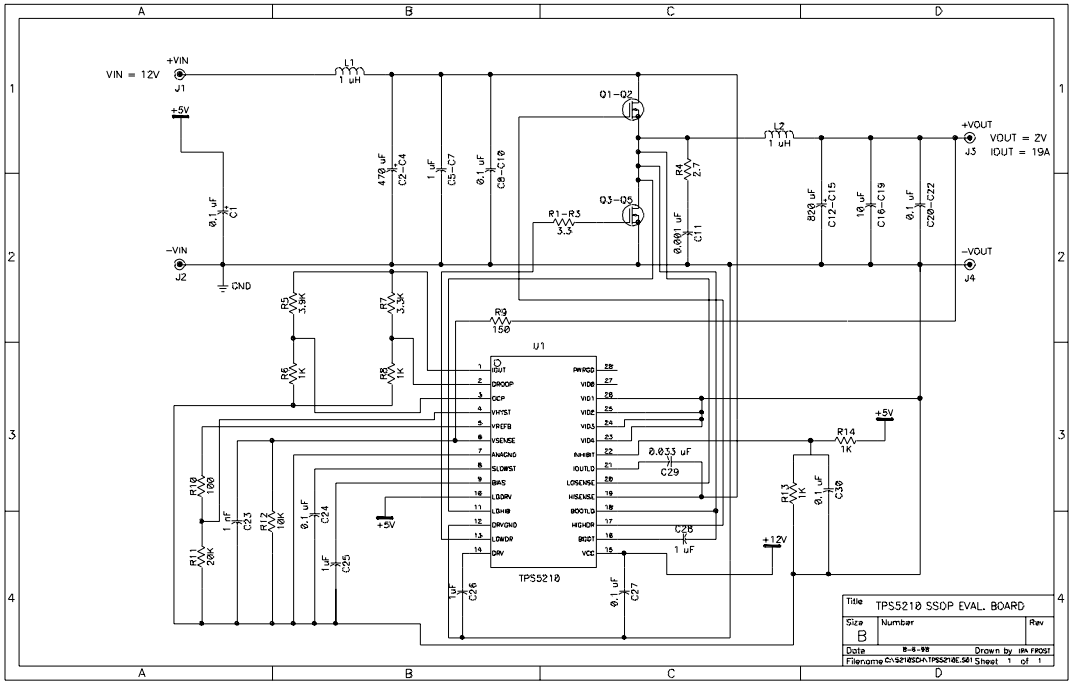


Figure 2. Evaluation power supply design schematic using the TPS5210 controller.

Output ripple voltage

Figure 3 shows the phase voltage, output voltage, and inductor current waveforms for the evaluation circuit of figure 2. The output voltage waveform is slightly different from the theoretical waveform of figure 1 due to the smoothing effect of the four 10uF ceramic capacitors, in parallel with the OS-CON bulk capacitors. Some resonance due to the ceramic and bulk capacitors is also noticeable as the voltage begins to drop. Figure 4 demonstrates how the waveforms, with the ceramic capacitors removed, closely resemble the theoretical waveforms of figure 1. The waveforms are very similar to ideal waveforms; ESL, ESR, and capacitive effect are noticeable.

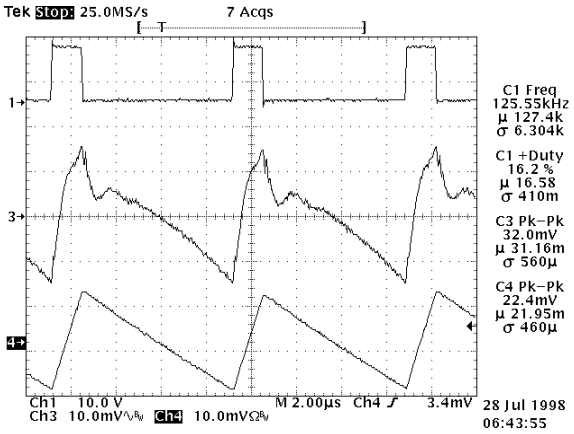


Figure 3. Output voltage ripple with 4x10uF ceramic capacitors. Ch1: voltage at junction of high-side FET with low-side FET; Ch3: output ripple voltage; Ch4: output inductor current (5A/div).

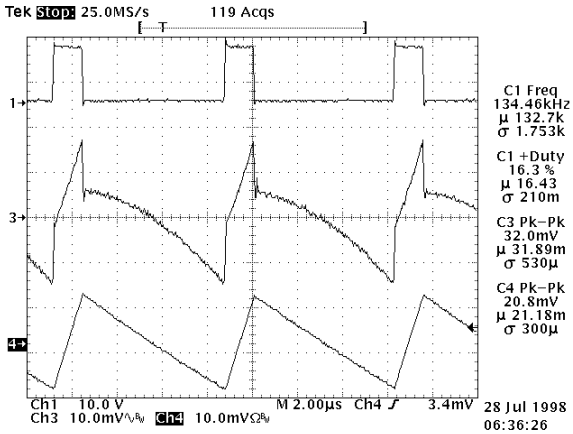


Figure 4. Output voltage ripple with ceramic capacitors removed. Ch1: voltage at junction of high-side FET with low-side FET; Ch3: output ripple voltage; Ch4: output inductor current (5A/div).

Transient load response

Transient load operation of the TPS5210 works similarly to the dc ripple regulation operation. The high-side gate drive signal maintains its state until the hysteresis band limit is reached, then the complement state remains fixed until the other hysteresis limit is exceeded. Propagation delays still apply. This characteristic allows extremely fast response times to load transitions. A transient response test was conducted with a 0.1A to 20.4A load step at a 30A/µs slew rate, and 1kHz repetition rate (Vin=12V, Vout=2.0V). Figures 5 and 6 show the transient response for a light-to-full load transition and a full-to light load transition, respectively, with droop active. After quickly regaining regulation, the voltage droop compensation circuit adjusts the regulation set point by -50mV in figure 5, and by +50mV in figure 6. With droop active, the transient regulation on Vout is ± 55mV. The controller response time is less than 1µs. With droop compensation disabled (grounded), the transient regulation on Vout is +115mV, -75mV; while the time to recover within the band is less than 2µs. The total transient regulation is increased by 80mV, or 4% of Vout, if droop is not active**. A major advantage of droop compensation is that the number of output capacitors can be reduced while maintaining the transient tolerance within specifications.**

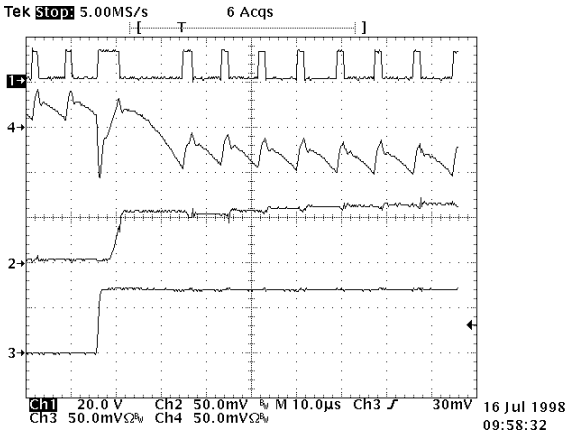


Figure 5. Light-to-full load transient response with Droop compensation. Ch1: voltage at junction of high-side FET with low-side FET (20V/div); Ch2: voltage at DROOP pin (50mV/div); Ch3: output load current (14.5A/div); Ch4: output ripple voltage (50mV/div).

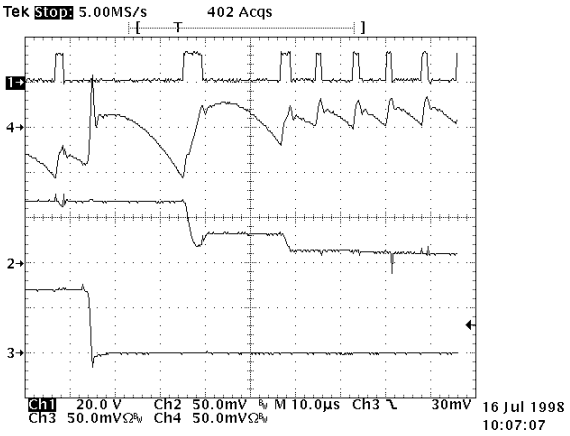


Figure 6. Full-to-light load transient response with Droop compensation. Ch1: voltage at junction of high-side FET with low-side FET (20V/div); Ch2: voltage at DROOP pin (50mV/div); Ch3: output load current; Ch4 (14.5A/div): output ripple voltage (50mV/div).

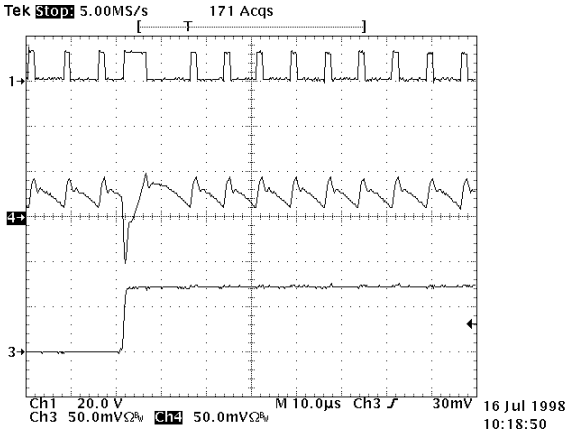


Figure 7. Light-to-full load transient response with Droop compensation disabled. Ch1: voltage at junction of high-side FET with low-side FET (20V/div); Ch3: output load current (14.5A/div); Ch4: output ripple voltage (50mV/div).

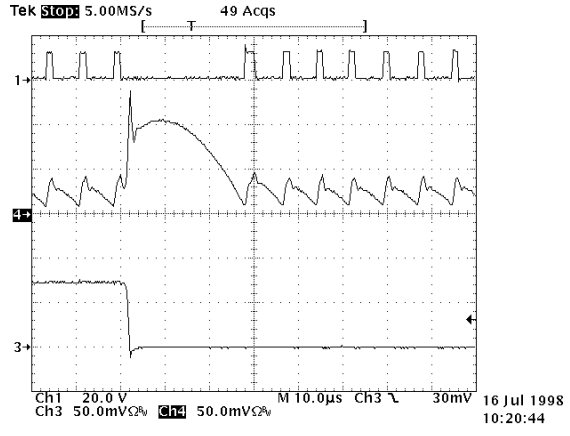


Figure 8. Full-to-light load transient response with Droop compensation disabled. Ch1: voltage at junction of high-side FET with low-side FET (20V/div); Ch3: output load current (14.5A/div); Ch4: output ripple voltage (50mV/div).

Other system performance

The load and line regulation, with droop disabled, are shown in figures 9 and 10 respectively with Vout=2.0V to demonstrate the tight line and load regulation of the ripple regulator. Regulation is maintained well below 1% . Since no current sense resistor is used, the efficiency is above 90% at 10A and 88% at 20A, as shown in figure 11. The power-up performance for the system is shown in figure 12 for a 20A load. Its performance, similar to no load, is well behaved with almost no output voltage overshoot. The +12V supply must be greater than the 10V UVLO start threshold, and the +5V must be greater than 4.2V (resistor divider from +5V to the INHIBIT pin in figure 2) before the TPS5210 controller is enabled. Over current protection, OCP, is demonstrated in figure 13 with load shorted, and figure 14 with the terminal common to FETs shorted.

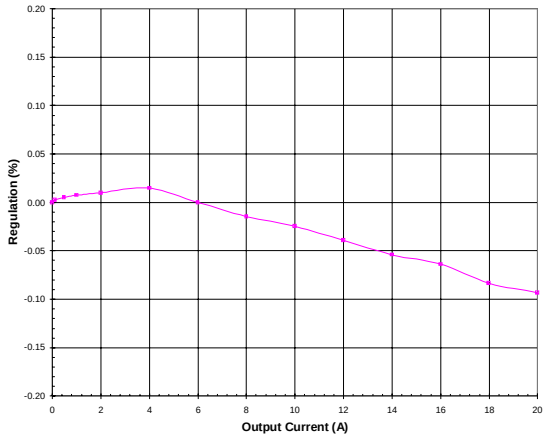


Figure 9. Normalized load regulation (Vin=12V, Vout=2.0V). Droop disabled.

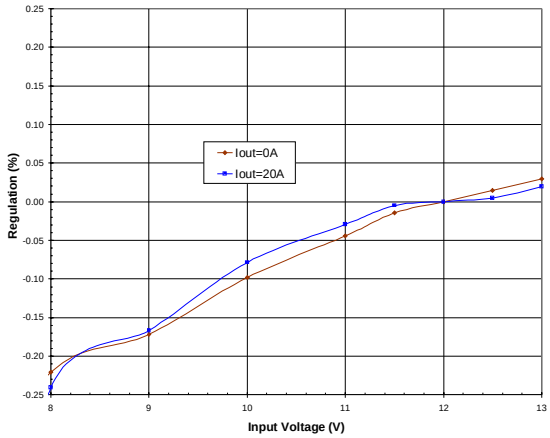


Figure 10. Normalized line regulation (Vout=2.0V, Iout=0A). Droop disabled.

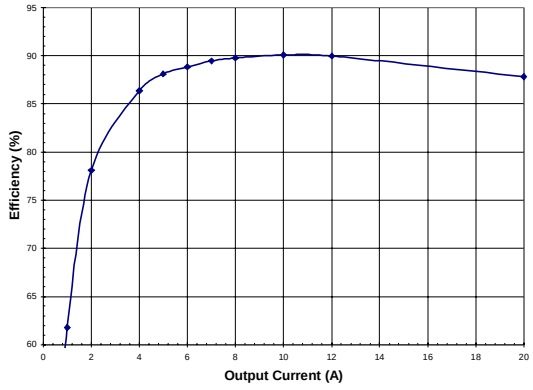


Figure 11. Efficiency versus load current. (Vin=12V, Vout=2.0V, 25°C).

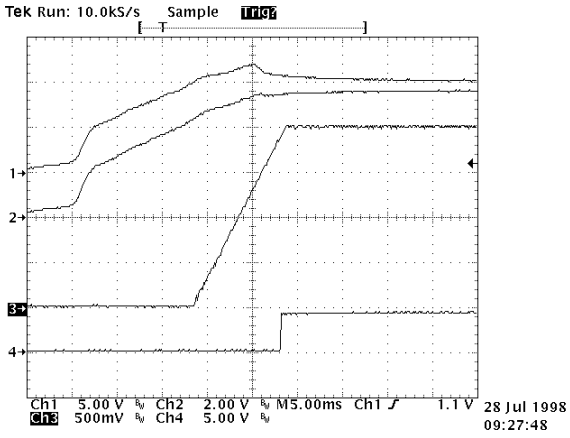


Figure 12. Power up performance (I=20A). Similar performance as with no load. Ch1: 12V supply (5V/div), Ch2: 5V supply (2V/div), Ch3: Vout (0.5V/div), Ch4: POWERGOOD pin (5V/div).

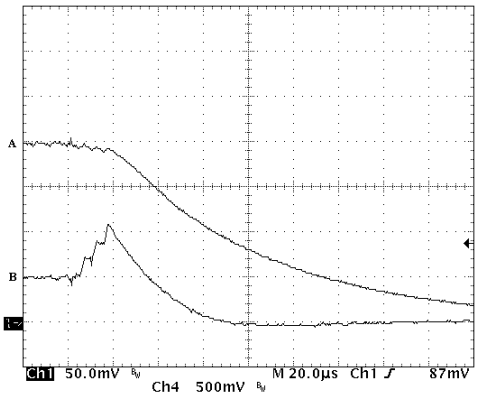


Figure 13. OCP Shorted Load Waveforms: Vin=12V, Vout=2V, Iout=19A.
A: Vout (500mV/div); B: V_{OCP} (50mV/div).

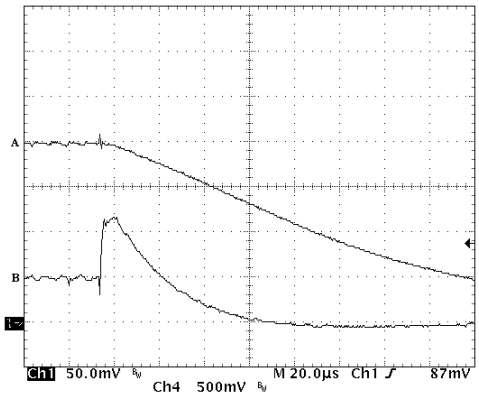


Figure 14. OCP Short-to-Ground Fault on the terminal common to the Power FETs: Vin=12V, Vout=2V, Iout=19A.
A: Vout (500mV/div); B: V_{OCP} (50mV/div).

4. CONTROLLER

The functional block diagram of the TPS5210 is given in figure 15. The controller has the following main features:

- VID / DAC that conforms to Intel's VRM8.3 specification; reference levels between 1.8V and 1.3V to decremented by 50mV, and 3.5V to 2.1V decremented by 0.1V.
- 1% reference over 0 ^{o}C to125 ^{o}C junction temperature range for reference voltages between 1.3V and 2.5V.
- Synchronous-Buck Drivers with adaptive deadtime control
- High-side MOSFET Driver voltage rating of 30V
- MOSFET Driver peak current rating of 2A
- Hysteretic comparator: 250ns prop delay to driver outputs, 2.5mV offset voltage, symmetrical hysteresis, hysteresis setting is a percentage of Vref.
- Lossless output current sensing circuit
- Accurate, fast Droop Compensation circuit.
- Slowstart circuit; slowstart time independent of VID setting.
- Internal 8V Drive Regulator for reduced gate charge power losses.
- POWERGOOD comparator, 93% of Vref trip.
- UVLO, Vcc undervoltage lockout, 10V start, 2V hysteresis.
- INHIBIT comparator that can also monitor UVLO of the system logic supply, 2.1V start, 100mV hysteresis.
- Latched Overcurrent Shutdown circuit
- Latched Overvoltage Shutdown circuit
- LODRV pin that activates the low-side FETs as a crowbar to protect against a short across the high-side FETs.

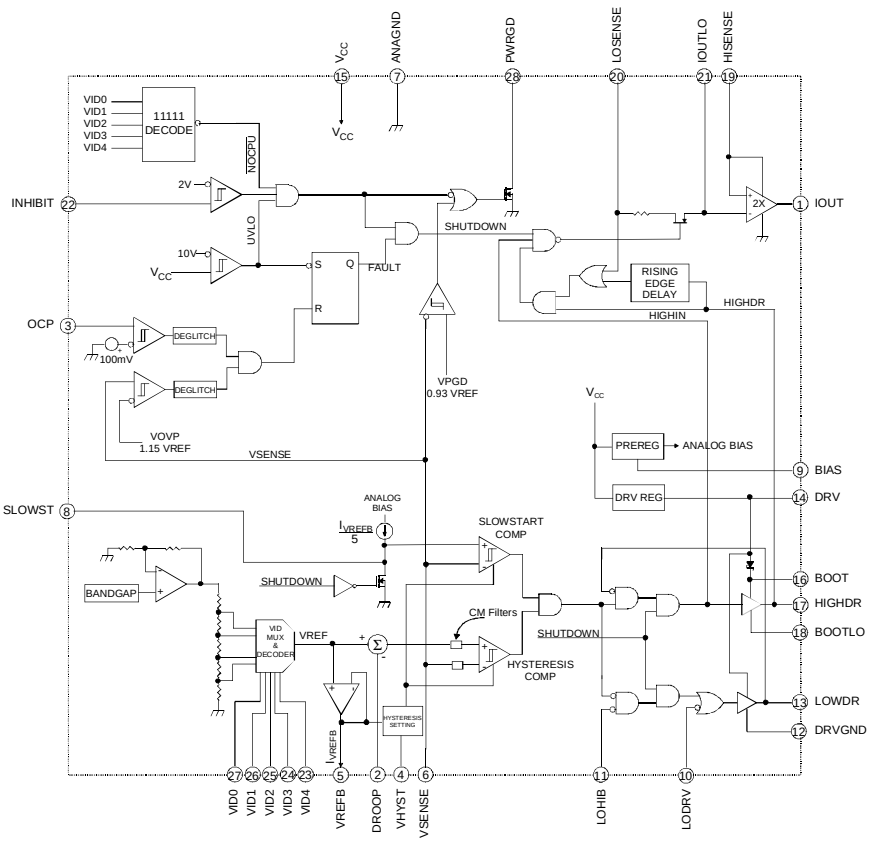


Figure 15. TPS5210 functional block diagram.

Vout Regulation

The initial accuracy of the internal reference is 1% over a VID range of 1.3V to 2.5V, and includes a junction temperature range of 0°C to 125°C and a Vcc range of 11.4V to 12.6V. Although an accurate internal reference is important, a systems designer is more concerned with the Vout regulation accuracy, which includes errors from the reference, the offset of the hysteretic comparator and the offset of the droop compensation circuit. A specification item was created, called cumulative reference accuracy, that accounts for these errors and is equal to 1.1% at a VID setting of 1.3V. Cumulative reference accuracy is defined as the percentage difference between the average value of the hysteretic comparator thresholds and the ideal 1.3V set point.

The droop compensation circuit improves the total regulation accuracy, which is the sum of the static accuracy and transient accuracy, as was shown in section 3, System Performance.

Hysteretic comparator

The hysteretic comparator is designed with low input offset voltage (± 2.5mV max) low propagation delays (250ns max to driver outputs with 10mV overdrive) and accurate hysteresis setting (± 3.5mV max). The hysteresis is proportional to the reference voltage; programming Vref to a new value automatically adjusts the hysteresis to be the same percentage of Vref.

Ripple regulators by nature have a fast response time to Vout transients and are thus inherently noise sensitive due to the very high bandwidth of the controller. If the ripple regulator controller is not properly designed, differential noise between the sensed Vout voltage and the internal reference can false trip the comparator, causing a high-frequency instability. The differential noise could be generated inside the control IC by the hysteretic comparator or the high-current MOSFET drivers, or be generated external to the controller during the switching transitions of the power MOSFETs. Noise suppression circuits were

added to the TPS5210 controller to improve the noise immunity, as shown in figure 16. Internal low-pass filters with a pole frequency of 5MHz were added to the inputs of the hysteretic comparator. These low-pass filters are referenced to the same analog ground as the hysteretic comparator. There is a common-mode filter with a 4MHz pole between VREFB and VHYST to filter out noise between these pins. A double pulse suppression circuit prohibits spurious pulses from propagating to the drivers. The double pulse suppression circuit becomes active when the comparator has toggled or when the LOHIB pin (which is connected to the power FETs) has transitioned providing additional noise immunity from internally and externally generated noise. The suppression circuit is active for 150ns. It is also recommended to include a low-pass filter between Vout and the VSENSE pin (R1 and C3 in fig 16); recommended values are 150 ohms and 1nF.

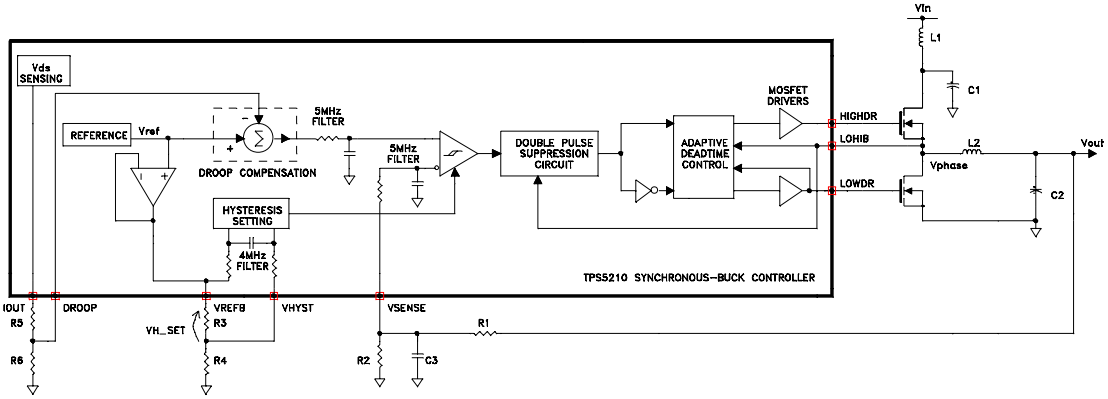


Figure 16. Block diagram showing noise suppression circuits.

Gate drivers

The gate drivers were designed to drive large capacitive loads quickly and efficiently. A block diagram of the drivers is given in figure 17. The output stage of the drivers consist of bipolar and MOS transistors in parallel. The bipolar transistors provide the majority of the 2 amp drive current. The driver outputs get pulled to ground (during sinking) or to the supply rail (during sourcing) by the MOS transistors. If the MOS transistors were not in the design, the voltage level on the driver outputs could only be driven to the saturation voltage level of the bipolar transistors. This could be a serious limitation, especially if logic-level power FETs are used in the power stage, resulting in shoot-through current through the power FETs. An I-V sweep of the low-side driver during sinking is given in figure 18. The Rds(on) of the MOS transistors for the sink stage is 5Ω at Tj = 125°C and is 45Ω for the source stage. The Rds(on) is lower for the sink stage to provide a low impedance path for the displacement current that flows through the miller capacitance of the power FET when the drain switches. This is especially important for the low-side driver to keep the low-side FET off when the high-side FET is turned on. The high-side driver is a bootstrap configuration with an internally integrated Schottky bootstrap diode. The voltage rating of the BOOT pin is 30v. The drivers are biased from an internal 8V Drive Regulator to minimize the gate drive power losses that are dissipated inside the controller. As an example, the gate charge requirements for a Si4410 power FET is 32nC at a Vgs of 8V, and is 49nC at a Vgs of 12V. If a system uses 6 Si4410's, and operates at 200KHz, the total power dissipation within the controller for both cases will be:

$$\text{8V gate drive} \quad - \; 6 \cdot 200\text{kHz} \cdot 32\text{nC} \cdot 12\text{V} = 0.46\text{watts}$$
$$\text{12V gate drive} - \; 6 \cdot 200\text{kHz} \cdot 49\text{nC} \cdot 12\text{V} = 0.71\text{watts}$$

With a package Θja of 84 °C/W, the controller will run 21°C hotter with a gate drive voltage of 12V, which can be a significant increase if the maximum ambient temperature is 70 °C. The drivers have also been optimized to reduce the amount of internal shoot-through current, which will result when either the low-side or high-side driver is switching states.

The adaptive deadtime control minimizes the deadtime between conduction intervals of the power FETs.

The low-side driver is not allowed to turn on until the Vphase voltage is below 2V; the high-side driver is not allowed to turn on until the LOWDR pin falls below 2V.
Figures 19, 20, and 21 show driver waveforms of the 12V to 2V, 20A processor power supply that is given in figure 2. In these figures, the high-side driver drives 2 Si4410's (Qg=64nC) and the low-side driver drives 3 Si4410's (Qg=96nC). The deadtime between the high-side FET turning off and the low-side FET turning on is 51.5ns, measured from when phase voltage equals 2V until gate of low-side FET begins to turn on. The deadtime between low-side FET turning off and high-side FET turning on is 69ns; measured from when LOWDR pin falls to 2V and high-side FET begins to turn on. Fast switching and short dead times improve efficiency. There is current limiting, 100mA, within the internal 8V voltage regulator to protect the regulator and I.C. against a short fault on one of the driver pins.

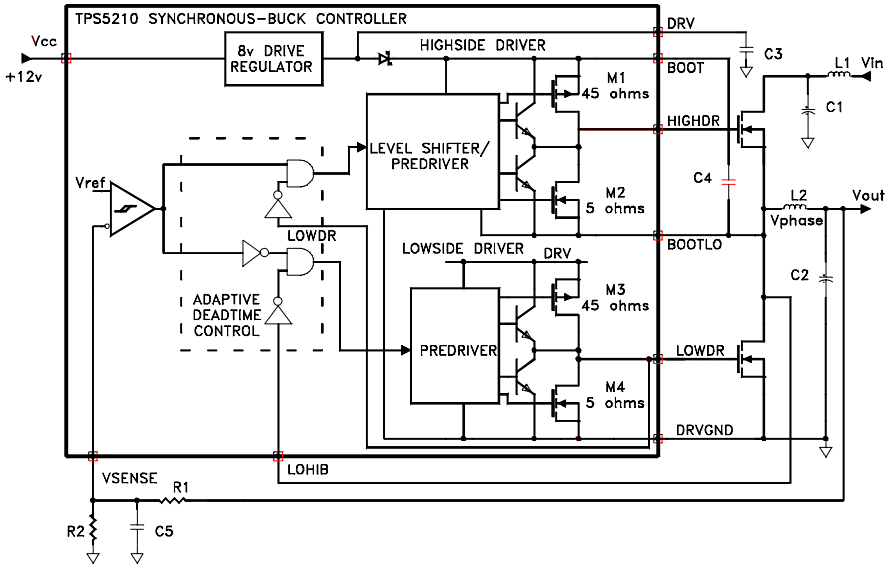


Figure 17. Gate Drivers.

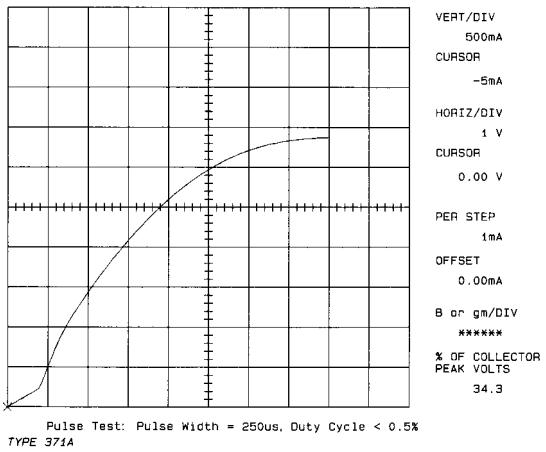


Figure 18. I-V characteristic curve for low-side sink driver. Horizontal axis is voltage, 1V/div. Vertical axis is current, 500mA/div. Curve shows initial MOSFET slope with 3Ω rdson, then after inflection point, the parallel bipolar npn allows up to 3.4A peak current at 8V.

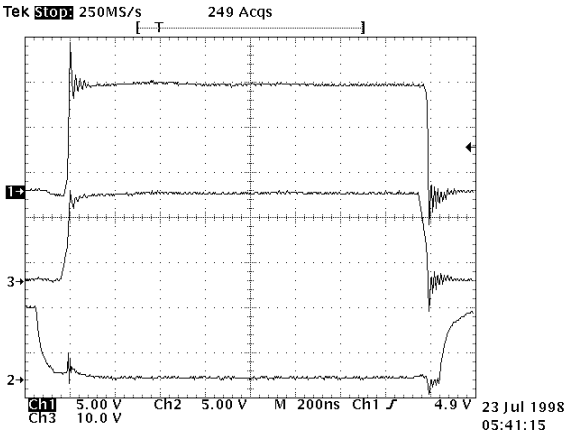


Figure 19. Gate drive waveforms of the 2V, 20amp power supply
Ch1: (Top) voltage at junction of high-side FET with low-side FET, (5V/div)
Ch2: gate voltage to ground of low-side FET at LOWDR pin, (5V/div)
Ch3: gate voltage to ground of high-side FET at HIGHDR pin, (10V/div).

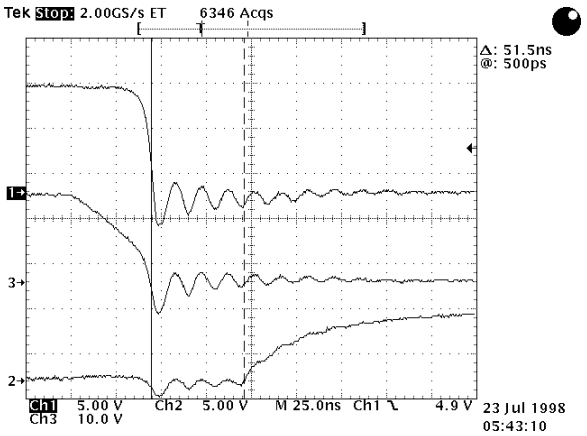


Figure 20. Gate drive waveforms of the 2V, 20amp processor power supply; high-side FET turn-off and low-side FET turn-on
Ch1: (Top) voltage at junction of high-side FET with low-side FET (phase voltage) (5V/div)
Ch2: gate voltage to ground of low-side FET at LOWDR pin (5V/div)
Ch3: gate voltage to ground of high-side FET at HIGHDR pin (10V/div).

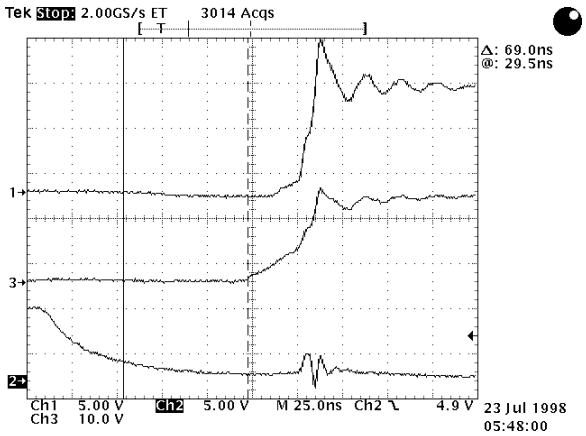


Figure 21. Gate drive waveforms of the 2V, 20amp processor power supply; low-side FET turn-off and high-side FET turn-on
Ch1: (Top) voltage at junction of high-side FET with low-side FET (phase voltage) (5V/div)
Ch2: gate voltage to ground of low-side FET at LOWDR pin (5V/div)
Ch3: gate voltage to ground of high-side FET at HIGHDR pin (10V/div).

Vds sensing

A simple block diagram of the Vds sensing circuit is given in figure 22. The Vds sensing circuit measures the average voltage across the high-side FET when the high-side FET is on and holds that value on a sample/hold capacitor when the high-side FET is off. The voltage on the sample/hold capacitor will be directly proportional to the load current. Sensing across the high-side FET rather than the low-side FET ensures that shorted loads can be detected. The RC time constant of the sample/hold network should be greater than the conduction-time of the high-side FET, otherwise the sample/hold circuit will function as a peak detector circuit and will not hold the average Vds voltage. The differential voltage across the sample/hold capacitor is amplified by 2 and converted to a single-ended signal on the IOUT pin. The DC CMRR of the Vds sensing amplifier is 69dB min. Logic is added to ensure that sampling begins and ends while the high-side FET is conducting. The turn-on and turn-off delays of the sample/hold switch are less than 100ns. Additional logic and a rising edge delay circuit is included to guarantee sampling during a short-to-ground fault across the low-side FET; the rising edge delay time is 500ns. Waveforms of the Vds sensing circuit are given in figure 23; the 2us RC time constant of the sample/hold circuit is less than the conduction-time of the high-side FET to more clearly illustrate the ripple waveform on the sample/hold capacitor. Viout lags V(Cs/h) by 1µs due to the response time of the Vds sensing amplifier.

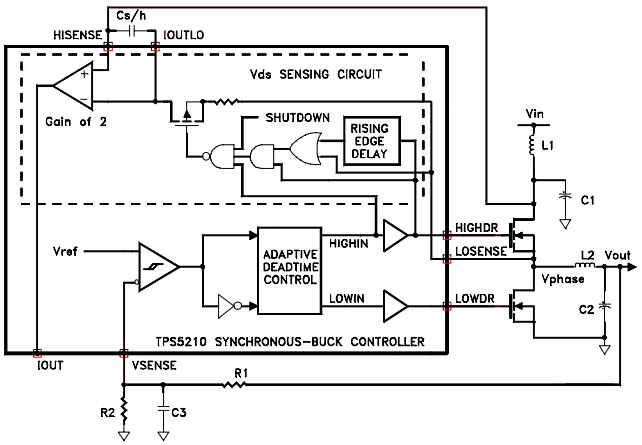


Figure 22. Vds sensing circuit.

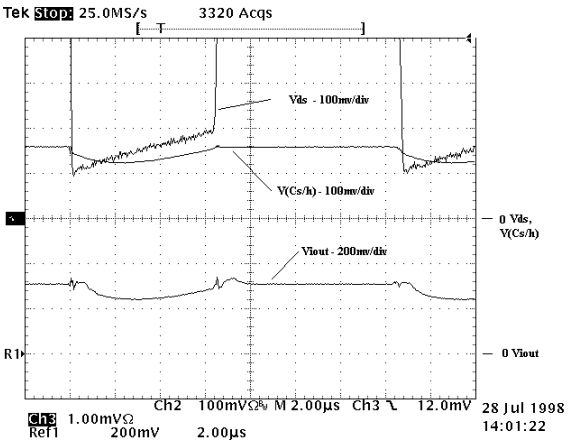


Figure 23. Vds sensing waveforms. Top: Vds of high-side FET (100mV/div); Center: voltage across the sample/hold capacitor (100mV/div); Bottom: Voltage on IOUT pin (200mV/div).

SLOWSTART

The slowstart circuit controls the rate at which Vout powers up. An external capacitor is charged with a current source which is proportional to the reference voltage; the slowstart time will be independent of the reference voltage. The internal current source that charges the slowstart capacitor is equal to $1/5^{th}$ of the current drawn out of the Vrefb pin. The equation to set the slowstart time is:

$$t_{SLOWSTART} = 5 \cdot C_{SLOWSTART} \cdot R_{VREFB}$$

where R_{VREFB} is the total external resistance connected to VREFB. Vout start-up waveforms for different VID settings is given in figure 24, showing that slowstart time is independent of the VID setting.

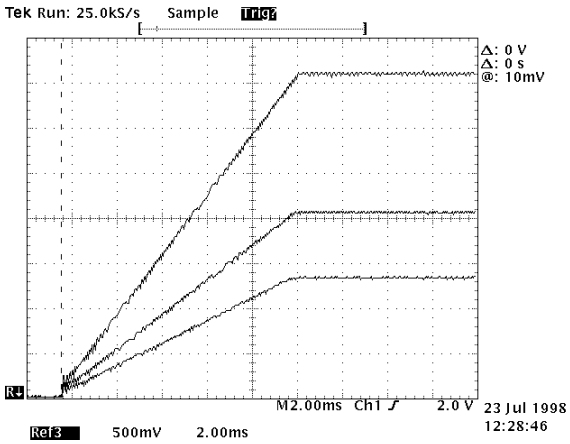


Figure 24. Slowstart output voltage rise at 1.3V, 2.0V, 3.5V settings (0.5V/div).

Overvoltage Protection

The overvoltage protection circuit will latch off the converter if Vout exceeds Vref by 15%. The controller supply (Vcc) must be recycled to reset the fault latch.

In addition to the standard OVP protection, the LODRV circuit is designed to protect the processor against overvoltages due to a short across the high-side power FET. External components to sense an overvoltage condition is required to use this feature. When a shorted high-side FET occurs, the low-side FETs are used as a crowbar. LODRV is pulled low and the low-side FET will be turned on, overriding all control signals inside the controller. The crowbar action will short the input supply to ground through the faulted high-side FETs. A fuse in series with Vin should be added to disconnect the short-circuit.

POWERGOOD
The powergood circuit monitors Vout for an undervoltage condition. If Vout falls below Vref by 7%, then the powergood pin is pulled low. The powergood pin is an open drain output.

Vcc Undervoltage Lockout
The Vcc undervoltage lockout circuit disables the controller while Vcc is below the 10V start threshold during power-up. While the controller is disabled, the output drivers will be low and the slowstart capacitor will be shorted. When Vcc exceeds the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. There is a 2V hysteresis in the undervoltage lockout circuit for noise immunity.

INHIBIT
The inhibit circuit is a comparator with a 2.1V start voltage and a 100mV hysteresis. When Inhibit is low, the output drivers are low and the slowstart capacitor is discharged. When Inhibit is above the start threshold, the short across the slowstart capacitor is released and normal converter operation begins. When the system logic supply is connected to the Inhibit pin, the Inhibit pin also controls power sequencing by locking out controller operation until the system logic supply exceeds the input threshold voltage of the inhibit circuit; thus the +12V supply and the system logic supply (either +5V or +3.3V) must be above UVLO thresholds before the controller is allowed to start up. In applications that derive main power from +5V or +3.3V for the power stage, the inhibit circuit can be the UVLO circuit for the main power supply.

5. SWITCHING FREQUENCY OF A HYSTERETIC CONVERTER

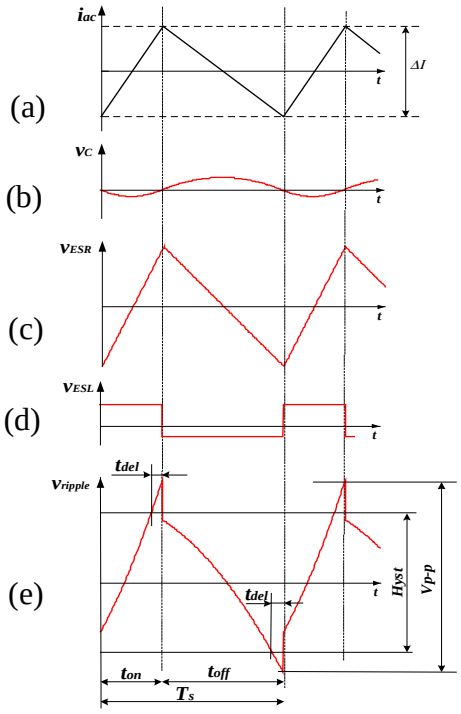
A predictable switching frequency of a hysteretic controller is an important characteristic for a power supply design. A simple and accurate method of determining the switching frequency is described below.

Assume that the input and output voltage ripple magnitudes are relatively negligible in comparison with the dc component. Also suppose that the time constant $L/(Rdson + R_L)$ that includes the output inductor, L, on-state resistance of the FET, $Rdson$, and inductor resistance, R_L, is high in comparison with the switching period. Assume the body diode conduction time and switching transition time are much smaller than the switching period. These assumptions are reasonable for low voltage ripple and high efficiency regulators. In such a case the output inductor current can be modeled as the sum of the dc component, which is equal to the output current Io, and the ac linear ramp component, which flows through the output capacitor (Fig.25). Peak to peak value of the inductor current ΔI is equal to the following equation:

$$\Delta I = \frac{Vin - Io \cdot (Rdson + R_L) - Vout}{L} \cdot D \cdot Ts \qquad (1)$$

where, Vin is the input voltage;
$Vout$ is the output voltage;
Ts is the switching period;
$D = \frac{Vout + Io \cdot (Rdson + R_L)}{Vin}$ is the duty cycle which is defined as: $D = ton / Ts$
ton is the on time of the high-side FET.

As was mentioned before in Section 2, the output capacitor can be modeled as the series connection of an ideal capacitor Co, ESR, and ESL. The voltage waveforms across each component of the output capacitor and the corresponding equations are shown in Fig. 25:



(a) Current waveform through output capacitor

(b) Voltage waveform through ideal capacitor with initial value at beginning of high-side FET on-time

High-side FET ON

$$v_C = \frac{\Delta I \cdot t^2}{2 \cdot Co \cdot D \cdot Ts} - \frac{\Delta I \cdot t}{2 \cdot Co}$$

High-side FET OFF

$$v_C = \frac{\Delta I \cdot t}{2 \cdot Co} - \frac{\Delta I \cdot t^2}{2 \cdot Co \cdot (1-D) \cdot Ts}$$

(c) Voltage waveform through ESR

High-side FET ON

$$v_{ESR} = ESR \cdot \left(\frac{\Delta I \cdot t}{D \cdot Ts} - \frac{\Delta I}{2} \right)$$

High-side FET OFF

$$v_{ESR} = ESR \cdot \left(\frac{\Delta I}{2} - \frac{\Delta I \cdot t}{(1-D) \cdot Ts} \right)$$

(d) Voltage waveform through ESL

High-side FET ON

$$v_{ESL} = \frac{ESL \cdot \Delta I}{D \cdot Ts}$$

High-side FET OFF

$$v_{ESL} = -\frac{ESL \cdot \Delta I}{(1-D) \cdot Ts}$$

(e) Summarized output voltage ripple waveform

$$v_{ripple} = v_C + v_{ESR} + v_{ESL}$$

Figure 25. Voltage waveforms across each component of the output capacitor and corresponding equations (time in each equation starts from zero at the beginning of the corresponding state).

One can see that the output voltage ripple, *Vpp*, is higher than the hysteresis window, *Hyst*, because of the delays, t_{del} , that were described in Section 2. Assume that delays for both switching moments are equal for simplicity. The ideal capacitor voltage component has the same initial value during switching moments t_{ON} and (*Ts-ton)* (see Fig. 25). In this case the voltage *Vpp* is:

$$Vpp = \frac{ESL}{L} \cdot Vin + \Delta I \cdot ESR \tag{2}$$

On the other hand the hysteresis window is equal to the difference between the peak-peak values of the Vout ripple, $v_{ripple,}$ at the moments t_{ON} - t_{del} and t_{OFF} - t_{del}

$$Hyst = v_{ripple}(t_{ON} - t_{del}) - v_{ripple}(t_{OFF} - t_{del}) \tag{3}$$

After substituting equation (1) into equations for v_C, v_{ESR} and v_{ESL} (Fig.25) and using equations (2) and (3) the following equation for the switching frequency, f_S, can be derived:

$$f_S = \frac{Vout \cdot (Vin - Vout) \cdot (ESR - t_{del} / Co)}{Vin \cdot (Vin \cdot ESR \cdot t_{del} + Hyst \cdot L - ESL \cdot Vin)} \tag{4}$$

It shows that the switching frequency strongly depends on *ESR* and *ESL*. It is important that *ESL* should meet the following condition: $\mathrm{ESL} < (\mathrm{ESR} \cdot \mathrm{t_{del}} + \mathrm{Hyst} \cdot \mathrm{L} \cdot \mathrm{D} / \mathrm{Vout})$. If it is not, the voltage step through ESL during switching exceeds the hysteresis window and switching frequency becomes too high and uncontrollable.

One can see that the switching frequency does not depend on the load current in equation (4). This is because the synchronous regulator has the same two stages of operation during the switching period over the load current range - including no load condition. In reality there is a weak dependence of the switching frequency on the load current because of power losses and additional voltage drops through non-ideal components. Equation (4) should be sufficiently accurate for the first frequency evaluation at the beginning of a design. For a more precise frequency evaluation, one can use the equation that is shown in the Appendix where dependence on the load current and static loss resistances is included. Also, a detailed derivation of this equation is represented in the Appendix.
Theoretical prediction and measurement results of the frequency for the evaluation power supply of figure 2 without the 4×10µF ceramic decoupling capacitors, under no load and 20A load conditions, is given in figure 26. Four Os-Con 820µF, 4V capacitors were used in this power supply. The measured values for ESR and ESL for each capacitor were 8mΩ, and 4.8nH, respectively, using an impedance analyzer with lead length error compensation. These values were divided by four because of four capacitors in parallel. The other values that were substituted in equation (4) are the following:
L = 1.2µH; R_L, = 11mohm; *Hyst* = 20.25mV, t_{del} = 570ns.
There is good agreement with theoretical and measured results; the maximum difference is less than 7%.

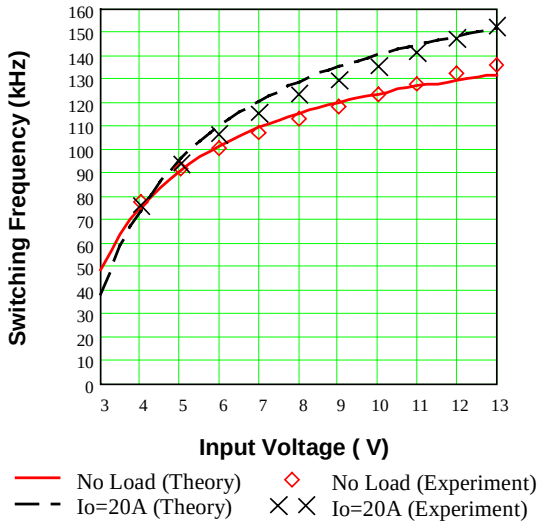


Figure 26. Theoretical and measured switching frequency comparison for no load and full load conditions (without Droop, Vout = 2.035V), without ceramic decoupling capacitors.

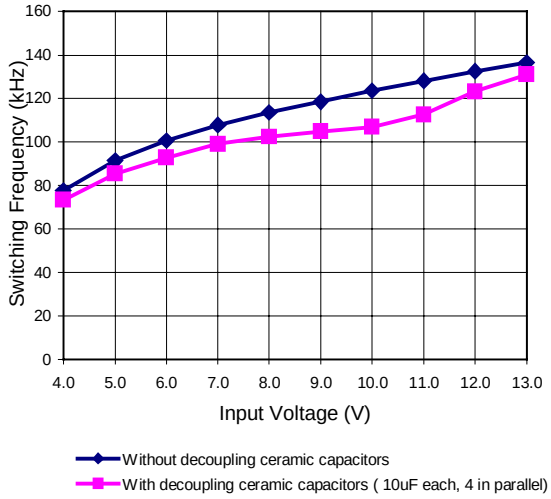
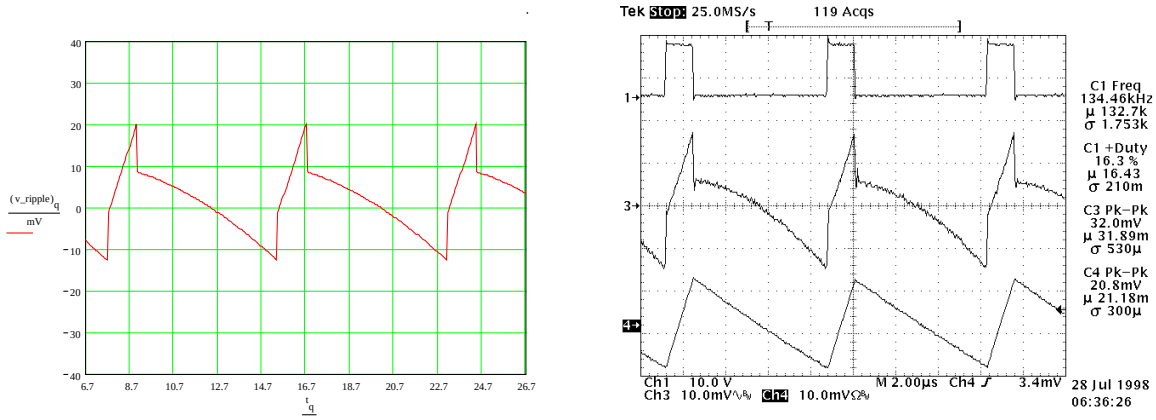


Figure 27. Measured switching frequency comparison with and without ceramic decoupling capacitors.

The switching frequency was also measured with the 4×10µF ceramic capacitors on the evaluation board of figure 2. Comparison results with and without ceramics are given in figure 27. For low input voltages, the switching frequencies are about the same. For Vin range between 7V and 11V, the frequency is lower with ceramics because the resonant period between ceramics and the OS-CON capacitors is close to the on-time of the converter, resulting in a longer on-time; the off-time increases to regulate Vout to the correct value, causing a decrease in switching frequency. Adding decoupling ceramic capacitors decreases ESL from 1.2nH to 0.8nH; consequently, decreasing the switching frequency.

Theoretical output voltage waveforms based on the frequency calculation were obtained using Mathcad software. These calculations are very close to the experimental waveforms measured without decoupling capacitors (Fig. 28).



(a) (b)

Figure 28. Theoretical (a) and measured (b) output ripple waveforms (without decoupling ceramic capacitors).

6. CONCLUSION

The operation and performance of a 12V to 2V at 20A evaluation power supply design using the TPS5210 ripple regulator controller was illustrated. Experimental data shows: tight static and dynamic regulation (± 55mV), fast transient response (within 1us), high efficiency (up to 90%), and stable operation with good noise immunity. TPS5210 architecture was also presented describing the major functional blocks: 1% reference, fast hysteretic comparator with noise suppression, droop compensation, 30V rating from BOOT pin to ground, 8V/2A gate drive with adaptive deadtime control, Vds current sensing , Slowstart, OVP, Powergood, UVLO, and INHIBIT. Finally, a simple mathematical description of switching frequency and output voltage for a ripple regulator was derived and presented showing good correlation with experimental data.

The TPS5210 ripple regulator controller was designed specifically to address the issues faced when designing a power supply for next-generation microprocessors. Efficiency is kept high - the absence of a sense resistor reduces conduction losses, and 8V/2A drive capability with adaptive-deadtime-control reduces switching losses. The ripple regulator architecture, 1.1% cumulative reference, and droop compensation provide a very tight static and dynamic regulation, greatly relieving the output capacitor requirements, while meeting tight regulation specifications.

ACKNOWLEDGMENTS

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[2] Intel document, “VRM 8.3 DC-DC Converter Design Guidelines,” Order number: 243870-001, June 1998.

APPENDIX: DERIVATION OF THE EQUATION FOR THE SWITCHING FREQUENCY

The following equation can be written in accordance with Fig. 25 (e):

$$Hyst = \Delta v_{ESL} + v_{ESR}(D \cdot Ts - t_{del}) - v_{ESR}(0) + v_C(D \cdot Ts - t_{del}) - ...$$
$$... - (v_{ESR}(D \cdot Ts) + v_{ESR}((1-D) \cdot Ts - t_{del}) + v_C((1-D) \cdot Ts - t_{del}))$$

Substituting:

$$\Delta v_{ESL} = \frac{Vin \cdot ESL}{L};$$

$$v_{ESR}(D \cdot Ts - t_{del}) - v_{ESR}(0) = \frac{\Delta I \cdot ESR \cdot (D \cdot Ts - t_{del})}{D \cdot Ts};$$

$$v_C(D \cdot Ts - t_{del}) = \frac{\Delta I}{2 \cdot Co} \cdot \left(\frac{(D \cdot Ts - t_{del})^2}{D \cdot Ts} - (D \cdot Ts - t_{del}) \right);$$

$$v_{ESR}(D \cdot Ts) + v_{ESR}((1-D) \cdot Ts - t_{del}) = \frac{\Delta I \cdot ESR \cdot t_{del}}{(1-D) \cdot Ts},$$

$$v_C((1-D) \cdot Ts - t_{del}) = \frac{\Delta I}{2 \cdot Co} \cdot \left(((1-D) \cdot Ts - t_{del}) - \frac{((1-D) \cdot Ts - t_{del})^2}{(1-D) \cdot Ts} \right)$$

and removing relatively small magnitude $t_{del}{}^2$, yields:

$$Hyst = \frac{Vin \cdot ESL}{L} - \frac{\Delta I \cdot ESR \cdot t_{del}}{Ts \cdot D \cdot (1-D)} + \Delta I \cdot ESR - \frac{\Delta I \cdot t_{del}}{Co}$$

After substituting $\Delta I = \frac{Vin - Io \cdot (Rdson + R_L) - Vout}{L} \cdot D \cdot Ts$ and $D = \frac{Vout + Io \cdot (Rdson + R_L)}{Vin}$

the following equation for the switching period can be derived:

$$Ts = \frac{Vin \cdot (Vin \cdot ESR \cdot t_{del} + Hyst \cdot L - Vin \cdot ESL)}{(Vin - Io \cdot (Rdson + R_L) - Vout) \cdot (Vout + Io \cdot (Rdson + R_L)) \cdot (ESR - t_{del} / Co)}$$

For no load condition and for preliminary frequency prediction simplified equation might be used if to substitute: $Rdson + R_L = 0$ and *fs=1/Ts*. This equation is:

$$f_S = \frac{Vout \cdot (Vin - Vout) \cdot (ESR - t_{del} / Co)}{Vin \cdot (Vin \cdot ESR \cdot t_{del} + Hyst \cdot L - ESL \cdot Vin)}$$