

Order the new  
**THS1206**

**High-Speed  
ADC  
Designer's  
Kit Today!**



(See back cover for details)

# Sine On

AN ANALOG AND  
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PRODUCT CATALOG

*this issue:*

# Data Converters

2Q 2000

Issue 3

## DSPcodec

- 2** ▶ Industry's first DSPcodecs maximize DSP performance  
▶ 18-bit, 48-kSPS audio-band DSPcodec

## ADC

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- 4** ▶ 10-bit, 60-MSPS IF sampling communications ADC  
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- 5** ▶ 10-bit, 30-MSPS data acquisition system with integrated PGA  
▶ Low-power, 10-bit, 200-kSPS ADCs with reference and FIFO
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## DAC

- 7** ▶ 2.7-V to 5.5-V, low-power, 10-bit DAC with power down  
▶ Low-power, 10- and 12-bit octal DACs with power down

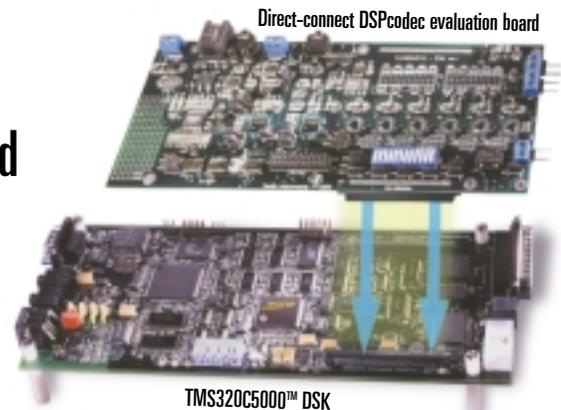
## Imaging

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▶ Triple-channel, 8-bit, 20-MSPS ADC for YUV and RGB conversion

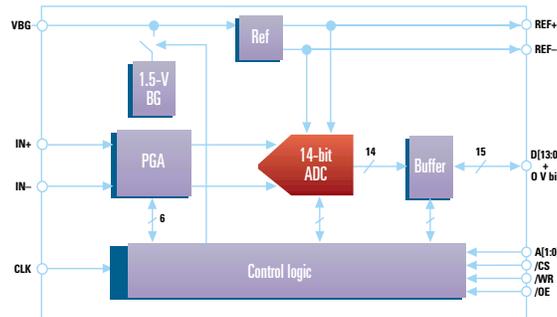
## Selection Guides and Resources

- 9** ▶ Selection guides
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Evaluate the industry's first DSP-optimized codecs **Page 2**

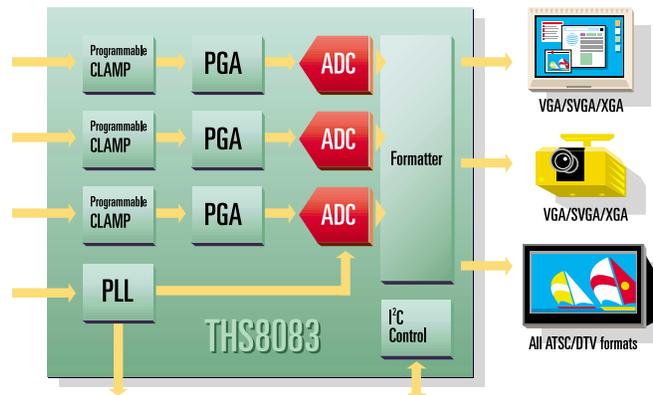


THS1401/03/08 block diagram



Choose from three new 14-bit ADCs for low power at high speeds **Page 3**

Video/graphics digitizer for PC/DTV **Page 8**



DSPcodec

# Industry's first DSPcodecs maximize DSP performance

## TLV320AIC10/11



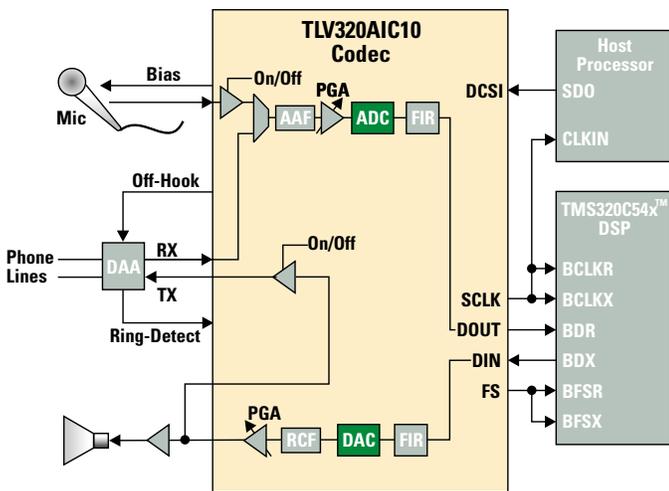
Get datasheets, samples and evaluation modules at:

[www.ti.com/sc/docs/products/analog/tlv320aic10.html](http://www.ti.com/sc/docs/products/analog/tlv320aic10.html)

and [www.ti.com/sc/docs/products/analog/tlv320aic11.html](http://www.ti.com/sc/docs/products/analog/tlv320aic11.html)

- 16 bit, 22 kSPS
- Low power dissipation: 39 mW at 8 kSPS
- 85-dB SNR for analog-to-digital converter (ADC) and digital-to-analog converter (DAC)
- Powerful glueless serial interface to SPI and TMS320™ DSPs
- 3.0-V to 5.5-V analog operation
- Built-in microphone bias and interface
- Supports up to seven slaves with one master
- TLV320AIC11 supports I/O voltages between 1.8 V and 2.2 V
- Packaging: available in 48-pin TQFP
- Pricing (in quantities of 1,000):  
TLV320AIC10 starts at \$3.75 each  
TLV320AIC11 starts at \$3.99 each

### TLV320AIC10 typical application



DSPcodec

# 18-bit, 48-kSPS, audio-band DSPcodec

## TLV320AIC27

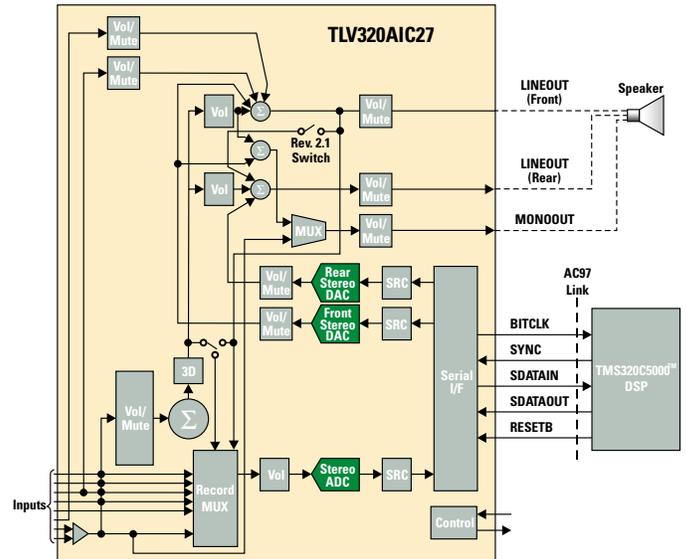


Get datasheets and samples at:

[www.ti.com/sc/docs/products/analog/tlv320aic27.html](http://www.ti.com/sc/docs/products/analog/tlv320aic27.html)

- AC97 version 2.1 compliant codec
- SNR: 95 dB (typ)
- Power dissipation: 139 mW at 3.3 V
- Four modes of operation: 2 channel/6 channel I<sup>2</sup>S/quad/modem
- Variable sampling rates: 8000, 11025, 16000, 22050, 44100, 48000 kHz
- Packaging: available in 48-pin TQFP
- Pricing for TLV320AIC27 starts at \$3.75 each in quantities of 1,000

### TLV320AIC27 typical application



For technical support and ordering literature, see page 15.

ADC

# 14-bit ADCs with internal programmable gain amplifier (PGA)

THS1401/03/08

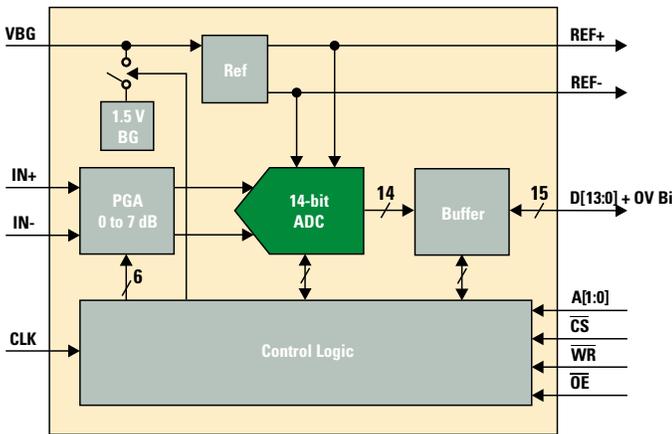


Get datasheets, samples and evaluation modules at:

[www.ti.com/sc/docs/products/analog/device.html](http://www.ti.com/sc/docs/products/analog/device.html)  
 Replace *device* in URL with ths1401, ths1403 or ths1408

- 1-, 3-, and 8-MSPS speed grades available
- 3.3-V single supply
- Differential inputs
- Programmable gain amplifier (PGA)
- Microprocessor-compatible parallel interface
- Timing compatible with TMS320C6000™ DSP
- Monolithic CMOS design
- Differential non-linearity (DNL)  $\pm 0.6$  LSB (typ)
- Integral non-linearity (INL)  $\pm 1.5$  LSB (typ)
- Characterized across commercial and industrial temperature ranges
- Packaging: available in 48-pin TQFP
- Pricing (in quantities of 1,000):  
 THS1401 starts at \$9.00 each  
 THS1403 starts at \$12.00 each  
 THS1408 starts at \$15.00 each

## THS1408 functional diagram



ADC

# Simultaneous sampling ADCs optimize DSP efficiency

THS1206, THS12082, THS10064, THS10082



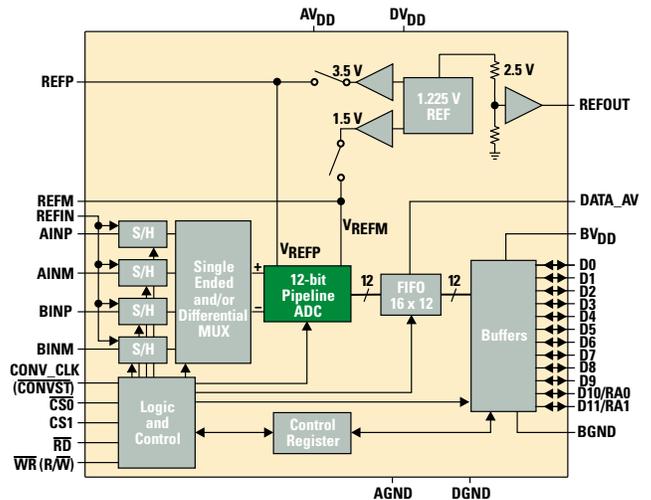
Get datasheets, samples, evaluation modules and application reports at:

[www.ti.com/sc/docs/products/analog/device.html](http://www.ti.com/sc/docs/products/analog/device.html)  
 Replace *device* in URL with ths1206, ths12082, ths10064 or ths10082

- Simultaneous or combined sampling of four single-ended or two differential signals (THS1206, THS10064)
- Buffered common-mode output
- Integrated 16-word FIFO increases processor throughput
- 5-V analog supply; 3-V or 5-V digital supply
- Glueless interface to DSPs and microprocessors
- Internal or external reference
- Packaging: available in 32-pin TSSOP
- Pricing (in quantities of 1,000):  
 THS1206 starts at \$13.00 each  
 THS12082 starts at \$9.95 each  
 THS10064 starts at \$7.95 each  
 THS10082 starts at \$5.95 each

THS1206  
 Designer's Kit Available  
 (see back page)

## THS1206 functional diagram



## Available options

Device	Bits	Speed (MSPS)	Analog Inputs	Differential Inputs
THS1206CDA	12	6	4	2
THS12082CDA	12	8	2	1
THS10064CDA	10	6	4	2
THS10082CDA	10	8	2	1

ADC

### 10-bit, 60-MSPS IF sampling communications ADC

**THS1060**

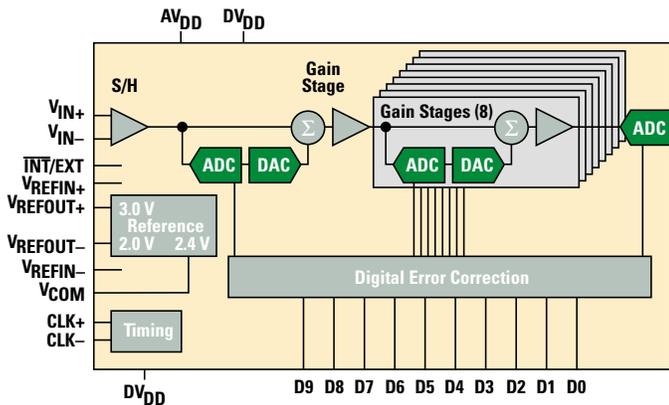


Get datasheets, samples and evaluation modules at:

[www.ti.com/sc/docs/products/analog/ths1060.html](http://www.ti.com/sc/docs/products/analog/ths1060.html)

- No missing codes
- 5-V analog and digital supply
- 9.5-bit ENOB at  $F_{IN} = 31$  MHz
- 60-dB signal-to-noise ratio at  $F_{IN} = 31$  MHz
- On-chip sample and hold
- 73-dB typical spurious-free dynamic range at  $F_{IN} = 15.5$  MHz
- 82-MHz bandwidth differential analog input
- 3-V and 5-V CMOS-compatible digital output
- Buffered 900- $\Omega$  analog input impedance
- Characterized across commercial and industrial temperature ranges
- Packaging: available in 48-pin TQFP
- Pricing for THS1060 starts at \$4.99 each in quantities of 1,000

**THS1060 functional diagram**



ADC

### Dual, high-speed, 8-bit, baseband sampling ADC

**THS0842**

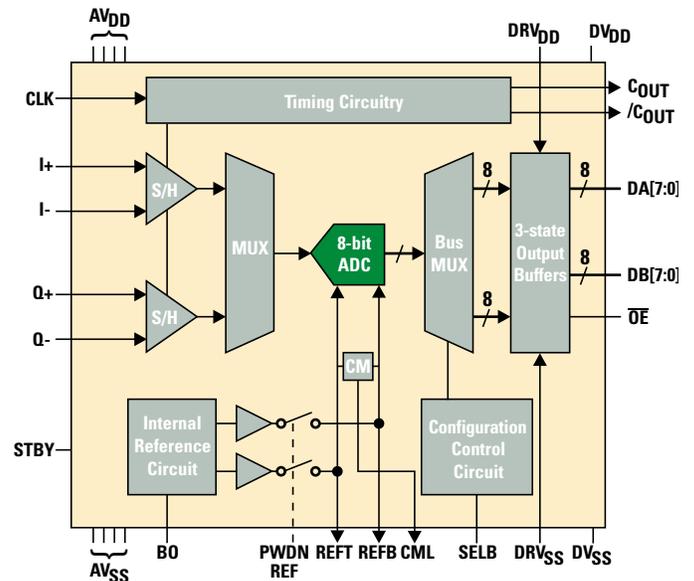


Get datasheets, samples and evaluation modules at:

[www.ti.com/sc/docs/products/analog/ths0842.html](http://www.ti.com/sc/docs/products/analog/ths0842.html)

- 40 MSPS (each input channel)
- Dual differential or single-ended analog inputs
- Dual simultaneous sample and holds
- Flexible interface—single or dual parallel output
- 3.3-V single-supply operation
- 3.3-V TTL/CMOS-compatible digital I/O
- Superior I & Q channel matching due to single 80-MSPS ADC
- Internal  $V_{ref}$  with power down or external  $V_{ref}$
- Packaging: available in 48-pin TQFP
- Pricing for THS0842 starts at \$3.94 each in quantities of 1,000

**THS0842 functional diagram**



For technical support and ordering literature, see page 15.

ADC

### 10-bit, 30-MSPS data acquisition system with integrated PGA

**THS1030/31**



Get datasheets, samples

and evaluation modules at:

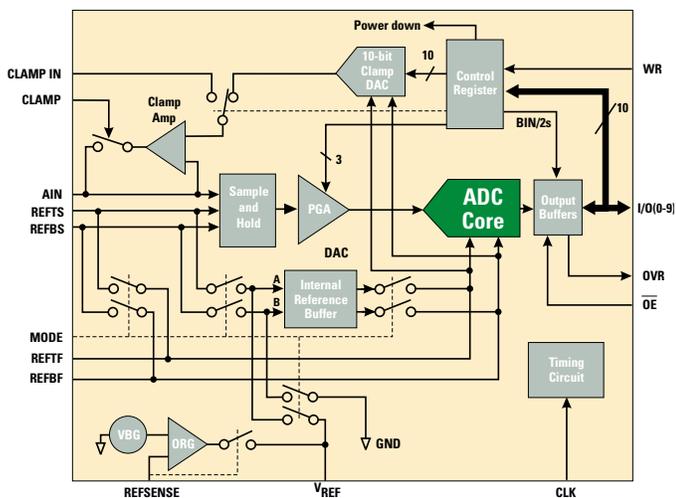
[www.ti.com/sc/docs/products/analog/th1030.html](http://www.ti.com/sc/docs/products/analog/th1030.html)

and

[www.ti.com/sc/docs/products/analog/th1031.html](http://www.ti.com/sc/docs/products/analog/th1031.html)

- Integrated 3-bit programmable gain amplifier (PGA) maintains small-signal SNR
- Integrated programmable 10-bit clamp DAC allowing 1 LSB accuracy on ADC input
- Configurable operation modes
- Wide power supply range of 2.7 V to 5.5 V
- Adjustable internal voltage reference
- Power as low as 91.8 mW
- THS1030 offers the same features as THS1031 without the on-chip digital clamp or PGA
- THS1030 is a drop-in replacement for TLC876 with 50% more speed at the same power consumption
- Packaging: available in 28-pin TSSOP and SOIC
- Pricing (in quantities of 1,000): THS1030 starts at \$3.50 each THS1031 starts at \$3.87 each

**THS1031 functional diagram**



ADC

### Low power, 10-bit, 200-kSPS ADCs with reference and FIFO

**TLV1504/08**



Get datasheets and samples at:

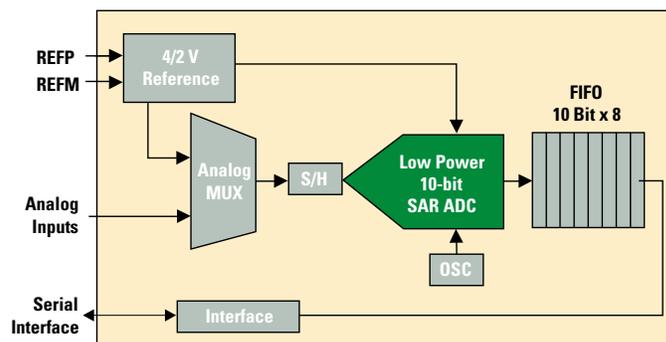
[www.ti.com/sc/docs/products/analog/tlv1504.html](http://www.ti.com/sc/docs/products/analog/tlv1504.html)

and

[www.ti.com/sc/docs/products/analog/tlv1508.html](http://www.ti.com/sc/docs/products/analog/tlv1508.html)

- Single 2.7-V to 5.5-V supply voltage
- 4- and 8-input channels
- Built-in reference, conversion clock and 8x FIFO
- DNL/INL:  $\pm 0.5$  LSB max
- SPI/DSP-compatible serial interfaces with SCLK up to 20 MHz
- Analog input range 0 V to supply voltage with 500-kHz bandwidth
- Power: 2.7 mW (typ)
- Power down: software/hardware power-down mode (1  $\mu$ A max, ext ref), auto power-down mode (1  $\mu$ A, ext ref)
- Programmable auto-channel sweep
- Pin-compatible, 12-bit upgrades available including TLV2544, TLV2548, TLC2554 and TLC2558
- Packaging: TLV1504 is available in small 16-pin SOIC and TSSOP. TLV1508 is available in small 20-pin SOIC and TSSOP.
- Pricing (in quantities of 1,000): TLV1504 starts at \$3.25 each TLV1508 starts at \$3.35 each

**TLV1504/08 functional diagram**



Read *Sine On* online at [www.ti.com/sc/sineon](http://www.ti.com/sc/sineon)

ADC

# 10-bit, 400-kSPS, CMOS successive approximation ADCs

**TLC1514/18**

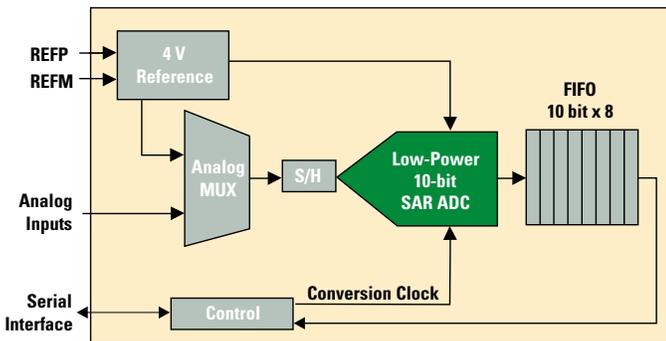


Get datasheets and samples at:

[www.ti.com/sc/docs/products/analog/tlc1514.html](http://www.ti.com/sc/docs/products/analog/tlc1514.html)  
and  
[www.ti.com/sc/docs/products/analog/tlc1518.html](http://www.ti.com/sc/docs/products/analog/tlc1518.html)

- Single 5-V supply voltage
- Serial interface
- 4- and 8-input channels
- Power : 22 mW (typ)
- Built-in reference and 8x FIFO
- DNL/INL:  $\pm 0.5$  LSB max
- SPI/DSP-compatible serial interfaces with SCLK up to 20 MHz
- Analog input range 0 V to supply voltage with 500-kHz bandwidth
- Software/hardware power-down mode (1  $\mu$ A max, ext ref), auto power-down mode (5  $\mu$ A, ext ref)
- Programmable auto-channel sweep
- Pin-compatible, 12-bit upgrades available including TLC2554 and TLC2558
- Packaging: TLC1514 is available in 16-pin SOIC and TSSOP. TLC1518 is available in 20-pin SOIC and TSSOP.
- Pricing (in quantities of 1,000):  
TLC1514 starts at \$3.39 each  
TLC1518 starts at \$3.49 each

**TLC1514/18 functional diagram**



ADC

# Low-power, miniature, 12-bit, serial ADCs with power down

**TLV2541/42/45, TLC2551/52/55**

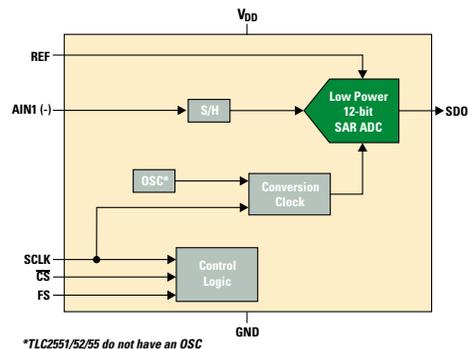


Get datasheets at:

[www.ti.com/sc/docs/products/analog/device.html](http://www.ti.com/sc/docs/products/analog/device.html)  
Replace *device* in URL with tlv2541, tlv2542, tlv2545, tlc2551, tlc2552 or tlc2555

- High speed
  - 200 kSPS (TLV2541/42/45)
  - 400 kSPS (TLC2551/52/55)
- Built-in conversion clock (TLV2541/42/45)
- INL/DNL:  $\pm 1$  LSB (max)
- SINAD equal to 72 dB,  $f_i = 20$  kHz
- SFDR equal to 85 dB,  $f_i = 20$  kHz
- SPI/DSP-compatible serial interfaces with SCLK up to 20 MHz
- Single supply: 2.7 V to 5.5 V (TLV2541/42/45), 5 V (TLC2551/52/55)
- Three options available
  - TLV2541/TLC2551 (single-channel input)
  - TLV2542/TLC2552 (dual-channel input with auto sweep)
  - TLV2545/TLC2555 (single-channel, pseudo-differential input)
- Optimized DSP interface (requires FS signal only)
- Low power with auto power down
  - TLV2541/42/45 operating current 1 mA at 2.7 V, auto power down 1  $\mu$ A at 2.7 V
  - TLC2551/52/55 operating current 4 mA at 5.5 V, auto power down 1  $\mu$ A (max)
- Packaging: available in 8-pin MSOP and SOIC
- Pricing (in quantities of 1,000):  
TLV2541/42/45 starts at \$3.60 each  
TLC2551/52/55 starts at \$3.70 each

**TLV2541 and TLC2551 functional diagram**



\*TLC2551/52/55 do not have an OSC

For technical support and ordering literature, see page 15.

DAC

## 2.7-V to 5.5-V, low-power, 10-bit DAC with power down

**TLV5606**

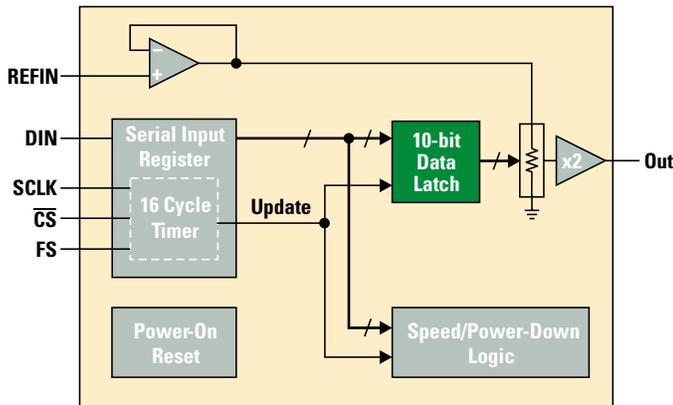


Get datasheets and samples at:

[www.ti.com/sc/docs/products/analog/tlv5606.html](http://www.ti.com/sc/docs/products/analog/tlv5606.html)

- 10-bit voltage output DAC
- Programmable settling time versus power consumption
  - 3  $\mu$ s in fast mode
  - 9  $\mu$ s in slow mode
- Ultra-low power consumption:
  - 900  $\mu$ W (typ) in slow mode at 3 V
  - 2.1 mW (typ) in fast mode at 3 V
- DNL: <0.2 LSB (typ)
- Compatible with TMS320™ DSP and SPI serial ports
- Power-down mode (10 nA)
- Buffered high-impedance reference input
- Voltage output range 2x the reference input voltage
- Monotonic over temperature
- Packaging: available in small 8-pin MSOP and SOIC
- Pricing for TLV5606 starts at \$1.75 each in quantities of 1,000

**TLV5606 functional diagram**



DAC

## Low-power, 10- and 12-bit, octal DACs with power down

**TLV5610/30**

Available June 2000



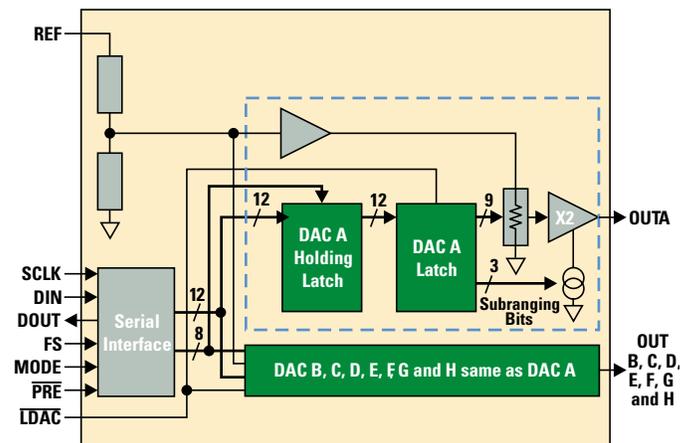
Get datasheets at:

[www.ti.com/sc/docs/products/analog/tlv5610.html](http://www.ti.com/sc/docs/products/analog/tlv5610.html)  
and

[www.ti.com/sc/docs/products/analog/tlv5630.html](http://www.ti.com/sc/docs/products/analog/tlv5630.html)

- Eight voltage output DACs in one package
- Programmable settling time versus power consumption:
  - 1  $\mu$ s in fast mode
  - 3  $\mu$ s in slow mode
- Compatible with TMS320™ DSP and SPI serial ports
- Differential nonlinearity <1 LSB
- Low power consumption:
  - 10 mW in slow mode at 3 V
  - 20 mW in fast mode at 3 V
- Power-down mode
- Data output for daisy chaining
- Packaging: to be available in 20-pin SOIC and TSSOP

**TLV5610 functional diagram**



Imaging

# Video/graphics digitizer for PC and digital TV applications

**THS8083\***



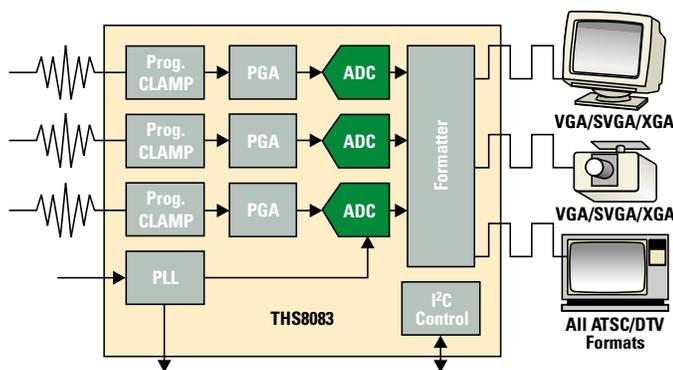
Get datasheets and samples at:

[www.ti.com/sc/docs/products/analog/ths8083.html](http://www.ti.com/sc/docs/products/analog/ths8083.html)

- 8-bit, 80/95-MSPS\*\* triple ADC
- First triple ADC to directly accept and digitize YPbPr/YUV (digital TV) and RGB (PC graphics) signals
- Integrated programmable gain amplifier (PGA) allows full-scale video formats between 0.4 V and 1.2 V peak-to-peak
- Integrated digital PLL generates pixel clock for all ATSC digital TV and PC graphic formats up to XGA (1024 x 768) resolution
- PLL also offers 5-bit phase control and internal loop filter
- Integrated sync-on-green/sync-on-luminance separator
- 256-step programmable clamp for YPbPr and RGB input
- Single and double pixel width output buses supporting 4:4:4 and 4:2:2 sampling
- Video mode detection by integrated horizontal sync (HS), vertical sync (VS) and pixel clock frequency monitoring
- Packaging: 100-pin TQFP footprint with thermally enhanced PowerPAD™
- Pricing for THS8083 starts at \$12.00 each in quantities of 1,000

\* Application reports and EVM available July 2000.  
 \*\*95-MSPS version is expected to be available by July 2000.

**THS8083 functional block diagram**



**THS8083 typical applications**

- CRT- or plasma-based monitor and TV set
- LCD desktop monitor
- LCD- or DMD-based projector
- Set-top box
- Video conferencing
- Video production equipment

Imaging

# Triple-channel, 8-bit, 20-MSPS ADC for YUV and RGB conversion

**TLC5733A**

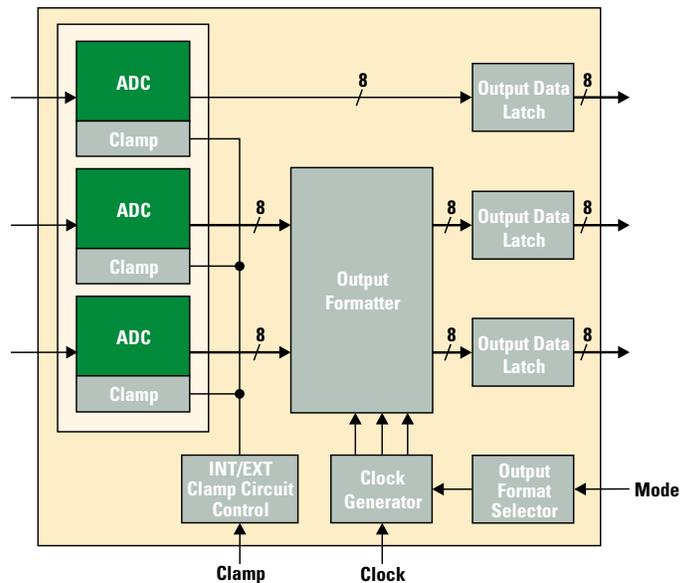


Get datasheets and samples at:

[www.ti.com/sc/docs/products/analog/tlc5733a.html](http://www.ti.com/sc/docs/products/analog/tlc5733a.html)

- Triple 8-bit, 20-MSPS ADC
- High-precision digital clamp optimized for NTSC, PAL and YUV to 1-LSB accuracy
- Automatic clamp pulse generator with composite sync detect
- Output data format multiplexer
  - YUV of 4:4:4, 4:2:2 or 4:1:1 sampling
  - RGB of 4:4:4 sampling
- Packaging: available in 64-pin LQFP
- Pricing for TLC5733A starts at \$5.98 each in quantities of 1,000

**TLC5733A functional block diagram**



For technical support and ordering literature, see page 15.

## Selection Guide for Data Converters

ADCs (< 1 MSPS)										
Device	Resolution (Bits)	Sample Rate (kSPS)	Supply (V)	Data-Bus Interface (Bits)	Analog Inputs	Power (typ) (mW)	V <sub>ref</sub> (Int/Ext)	DNL (max) (±LSB)	INL (max) (±LSB)	Comments
TLV2548	12	200	2.7 to 5.5	Serial	8	4.5	Int	1	1	8x Int FIFO; Int clk; analog input 0 V to V <sub>CC</sub> w/500-kHz BW; SFDR -84 dB, ENOB 11.57 bits, THD -82 dB @ f <sub>i</sub> = 12 kHz
TLV2545	12	200	2.7 to 5.5	Serial	1	2.3	Ext	1	1	Single channel pseudo-differential input, low power, small packages power down
TLV2544	12	200	2.7 to 5.5	Serial	4	4.5	Int	1	1	8x Int FIFO; Int clk; analog input 0 V to V <sub>CC</sub> w/500-kHz BW; SFDR -84 dB, ENOB 11.57 bits, THD -82 dB @ f <sub>i</sub> = 12 kHz
TLV2543	12	66	3.3	Serial	11	3.3	Ext	1	1	System clock; unipolar/bipolar output; auto S&H
TLV2542	12	200	2.7 to 5.5	Serial	2	2.3	Ext	1	1	Low power, small packages, power down
TLV2541	12	200	2.7 to 5.5	Serial	1	2.3	Ext	1	1	Low power, small packages, power down
TLC2558	12	400	5	Serial	8	3.3	Int	1	1	8x Int FIFO; Int clk; analog input 0 V to V <sub>CC</sub> w/50
TLC2555	12	400	5	Serial	1	15	Ext	1	1	Single channel pseudo-differential input, low power, small packages, power down
TLC2554	12	400	5	Serial	4	4.5	Int	1	1	8x Int FIFO; Int clk; analog input 0 V to V <sub>CC</sub> w/50
TLC2552	12	400	5	Serial	2	15	Ext	1	1	Low power, small packages, power down
TLC2551	12	400	5	Serial	1	15	Ext	1	1	Low power, small packages, power down
TLC2543	12	66	5	Serial	11	5	Ext	1	1	System clock; unipolar/bipolar output; auto S&H
TLV1578	10	1250	2.7 to 5.5	Parallel	8	12	Int	1	1	SFDR -63 dB, ENOB 9.3, SINAD 60 dB, SNR 60 dB, THD -60 dB @ f <sub>i</sub> = 100 kHz
TLV1572	10	1250	2.7 to 5.5	Serial	1	8	Ext	1	1	SFDR -73 dB, ENOB 9.3, SINAD 58 dB, SNR 61 dB, THD -70 dB @ f <sub>i</sub> = 100 kHz
TLV1571	10	1250	2.7- 5.5	Parallel	1	12	Int	1	1	SFDR -63 dB, ENOB 9.3, SINAD 60 dB, SNR 60 dB, THD -60 dB @ f <sub>i</sub> = 100 kHz
TLV1570	10	1250	2.7 to 5.5	Serial	8	8	Int	1	1	SFDR -73 dB, ENOB 9.3, SINAD 58 dB, SNR 61 dB, THD -70 dB @ f <sub>i</sub> = 100 kHz
TLV1549	10	38	3.3	Serial	1	1.32	Ext	1	1	System clock; S&H; compatible w/TLC1549
TLV1548	10	85	2.7 to 5.5	Serial	8	1.05	Ext	1	1	Sync/async modes; extended sampling capability; programmable power vs. conversion rate
TLV1544	10	85	2.7 to 5.5	Serial	4	1.05	Ext	1	1	Sync/async modes; extended sampling capability; programmable power vs. conversion rate
TLV1543	10	38	3.3	Serial	11	2.7	Ext	1	1	System clock; compatible w/TLC1543
TLV1508	10	200	2.7 to 5.5	Serial	8	2.7	Int	0.5	0.5	8x Int FIFO; Int clk; analog input 0 V to V <sub>CC</sub> w/500-kHz BW; SFDR 72 dB
TLV1504	10	200	2.7 to 5.5	Serial	4	2.7	Int	0.5	0.5	8x Int FIFO; Int clk; analog input 0 V to V <sub>CC</sub> w/500-kHz BW; SFDR 72 dB
TLC1551	10	164	5	P10	1	10	Ext	1	1	Int/Ext clock option
TLC1550	10	164	5	P10	1	10	Ext	0.5	0.5	Int/Ext clock option
TLC1549	10	38	5	Serial	1	4	Ext	1	1	System clock; input S&H
TLC1543	10	38	5	Serial	11	4	Ext	1	1	System clock; S&H; terminal compatible w/TLC542
TLC1542	10	38	5	Serial	11	4	Ext	0.5	0.5	System clock; S&H; terminal compatible w/TLC542
TLC1541	10	32	5	Serial	11	6.5	Ext	1	1	S&H; simultaneous Read/Write; compatible to 8-bit TLC540
TLC1518	10	400	5	Serial	8	22	Int	0.5	0.5	8x Int FIFO; Int clk; analog input 0 V to V <sub>CC</sub> w/500-kHz BW; SFDR 72 dB
TLC1514	10	400	5	Serial	4	22	Int	0.5	0.5	8x Int FIFO; Int clk; analog input 0 V to V <sub>CC</sub> w/500-kHz BW; SFDR 72 dB
TLV571	8	1250	2.7 to 5.5	Parallel	1	12	Int	0.5	0.5	Low power with auto or S/W powerdown; hardware configurable

(continued on next page)

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## Selection Guide for Data Converters (continued)

ADCs (< 1 MSPS) (continued)										
Device	Resolution (Bits)	Sample Rate (kSPS)	Supply (V)	Data-Bus Interface (Bits)	Analog Inputs	Power (typ) (mW)	V <sub>ref</sub> (Int/Ext)	DNL (max) (±LSB)	INL (max) (±LSB)	Comments
TLV0838	8	37.9	3.3	Serial	8	2.7	Ext	0.5	0.5	TTL/MOS I/O compatible; 0- to 3.6-V input range; inputs configurable for single-ended, differential, or pseudo-differential modes
TLV0834	8	41	3.3	Serial	4	2.7	Ext	0.5	0.5	TTL/MOS I/O compatible; 0- to 3.6-V input range; inputs configurable for single-ended, differential, or pseudo-differential modes
TLV0832	8	44.7	3.3	Serial	2	5	Int	0.5	0.5	MUX'd twin input channels; single-ended or differential input
TLV0831	8	49	3.3	Serial	1	0.67	Ext	0.5	0.5	One differential input channel, can configure as single-ended inputs
TLC549	8	40	3 to 6	Serial	1	9	Ext	0.5	0.5	4-MHz typ Int system clock; I/O clk input to 1.1 MHz; S&H; compatible w/10-bit TLC1540
TLC548	8	45.5	3 to 6	Serial	1	9	Ext	0.5	0.5	4-MHz typ Int system clk; I/O clk input to 2.048 MHz; S&H; compatible w/10-bit TLC1540
TLC546	8	40	5	Serial	19	6	Ext	0.5	0.5	System clock input to 2.1 MHz; I/O clk input to 1.1 MHz; S&H; simultaneous Read/Write
TLC545	8	76	5	Serial	19	6	Ext	0.5	0.5	System clock input to 4 MHz; I/O clk input to 2.048 MHz; S&H; simultaneous Read/Write
TLC542	8	25	5	Serial	11	6	Ext	0.5	0.5	Int System clock; typ I/O clk input to 1.1 MHz; compatible w/10-bit TLC1542/1543
TLC541	8	40	5	Serial	11	6	Ext	0.5	0.5	System clock input to 2.1 MHz; I/O clk input to 1.1 MHz; S&H
TLC540	8	75	5	Serial	11	6	Ext	0.5	0.5	System clock input to 4 MHz; I/O clk input to 2.048 MHz; S&H
TLC0838	8	20	5	Serial	8	3	Ext	0.4	0.4	Easily configure for pseudo-differential input
TLC0834	8	20	5	Serial	4	3	Ext	0.4	0.4	TTL/MOS I/O compatible; 0- to 5-V input range
TLC0832	8	22	5	Serial	2	12.5	Int	0.4	0.4	MUX'd twin input channels; single-ended or differential input
TLC0831	8	31	5	Serial	1	3	Ext	0.4	0.4	One differential input channel, can configure as single-ended inputs
TLC0820A	8	392	5	P8	1	37.5	Ext	0.5	1	Differential reference inputs; Track & Hold; Int clk
TLC7135	4.5	0.003	-5 to +5	BCD	1	5	Ext	0.01	0.5	4 1/2 digit precision ADC; MUX'd BCD output; true differential input; 1-pA typ input current

For technical support and ordering literature, see page 15.

## Selection Guide for Data Converters (continued)

ADCs ( $\geq 1$ MSPS)									
Device	Resolution (Bits)	Sample Rate (MSPS)	Supply (V)	Analog Inputs	Power (typ) (mW)	Analog Input BW (MHz)	DNL (max) ( $\pm$ LSB)	INL (max) ( $\pm$ LSB)	Comments
THS1408	14	8	3.3	1	270	140	1	5	Differential inputs, integrated programmable gain amplifier, internal $V_{ref}$ 80-dB SFDR @ 4 MHz, 11.5-bit ENOB
THS1403	14	3	3.3	1	270	140	1	2.5	Differential inputs, integrated programmable gain amplifier, internal $V_{ref}$ 80-dB SFDR @ 1 MHz, 11.5-bit ENOB
THS1401	14	1	3.3	1	270	140	1	2.5	Differential inputs, integrated programmable gain amplifier, internal $V_{ref}$ 80-dB SFDR @ 100 kHz, 11.5-bit ENOB
THS12082*	12	8	3 to 5	2	216	96	1	1.5	Two single-ended or 1 diff input channel; 16-word FIFO; ENOB = 11 bits (diff. mode); Available June 2000
THS1206	12	6	3 to 5	4	216	96	1	1.5	Integrated FIFO, 4 S&H, 3-V/5-V digital i/f; SFDR 75 dB @ $f_i = 2$ MHz, $f_s = 6$ MHz & $-1$ dBFS; ENOB = 11 bits (diff. mode)
TLV1578	10	1.25	2.7 to 5.5	8	12	30	1	1	SFDR $-63$ dB, ENOB 9.3, SINAD 60 dB, SNR 60 dB, THD $-60$ dB @ $f_i = 100$ kHz
TLV1572	10	1.25	2.7 to 5.5	1	8	12	1	1	SFDR $-62$ dB, ENOB 9.35, SINAD 58 dB, THD $-60$ dB @ $f_i = 200$ kHz; BW to 12 MHz
TLV1571	10	1.25	2.7 to 5.5	1	12	30	1	1	SFDR $-63$ dB, ENOB 9.3, SINAD 60 dB, SNR 60 dB, THD $-60$ dB @ $f_i = 100$ kHz
TLV1570	10	1.25	2.7 to 5.5	8	8	25	1	1	SFDR $-73$ dB, ENOB 9.3, SINAD 58 dB, SNR 61 dB, THD $-70$ dB @ $f_i = 100$ kHz
TLV1562	10	2	2.7 to 5.5	4	15	120	1.5	1.5	4- to 10-bit programmable ADC w/dual matched S&H; 2 to 7 MSPS; SFDR $-70.3$ dB, THD $-68.8$ dB, ENOB 9.4 @ $f_i = 800$ kHz
THS10082*	10	8	3 to 5	2	186	96	1	1	Two single-ended or 1 differential input channel; 16-word FIFO; ENOB = 11 bits (diff. mode); Available June 2000
THS1031	10	30	2.7 to 5.5	1	94	150	1	2	Integrated programmable digital clamp & gain amplifier
THS1030	10	30	2.7 to 5.5	1	87	150	1	2	Pin compatible with TLC876
THS1060	10	60	5	1	600	82	1	3	9.5-bit ENOB @ $F_{IN} = 31$ MHz
THS1050	10	50	5	1	500	82	0.6	2.5	9.7-bit ENOB @ $F_{IN} = 31$ MHz; 73-dB SFDR @ $F_{IN} = 15.5$ MHz
THS10064	10	6	3 to 5	4	186	96	1	1	Simultaneous sampling of 4 SE/2 differential input signals, or combination of both; 16-word FIFO; ENOB 9.6 bits
TLC876	10	20	5	1	107	200	0.75	1.2	5-V or 3.3-V digital I/O; SFDR $-64$ dB, THD $-62$ dB, ENOB 8.5 @ $f_i = 3.58$ MHz
TLV5580	8	80	3.3	1	165	700	1.3	2.4	3.3-V TTL/CMOS digital I/O; SFDR 48.5 dB, THD $-45.5$ dB, ENOB 6.6 @ $f_i = 76$ MHz
TLV571	8	1.25	2.7 to 5.5	1	12	30	0.5	0.5	Low power with auto or s/w powerdown; hardware configurable
TLV5535	8	35	3.3	1	90	600	1.3	1.5	3.3-V TTL/CMOS digital I/O; SFDR 58 dB, THD $-54$ dB
TLV5510	8	10	3	1	42	36	0.75	1	SFDR 41 dB, SNR 40 dB @ $f_i = 1$ MHz
TLC5733A	8	20	5	3	250	14	0.5	1	3 ch ADC w/precision clamp; 2.7- to 5.25-V digital supply
TLC5540	8	40	5	1	85	75	0.75	1	SFDR $-46$ dBc, SNR 47, THD $-42$ , ENOB 7.61 @ $f_i = 3$ MHz
TLC5510A	8	20	5	1	90	14	0.5	0.75	SFDR $-46$ dBc, SNR 46 @ $f_i = 3$ MHz
TLC5510	8	20	5	1	90	14	0.5	0.75	SFDR $-46$ dBc, SNR 46 @ $f_i = 3$ MHz
THS8083	8	80	3.3	3	1200	500	0.75	1.5	Video digitizer for digital TV/PC Graphics
THS8083-95*	8	95	3.3	3	1200	500	0.75	1.5	Video digitizer for digital TV/PC graphics
THS0842	8	40	3.3	2	275	600	2	2.2	Dual simultaneous S&H inputs; differential or single

\*Estimated specifications

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Selection Guide for Data Converters (continued)

DACs (< 10 MHz)											
Device	Resolution (Bits)	Supply (V)	Data-Bus Interface (Bits)	Settling Time (µs)	Number of DACs	Power (typ) (mW)	Output (I or V)	V <sub>ref</sub> (Int/Ext)	DNL (max) (±LSB)	INL (max) (±LSB)	Comments
TLV5639	12	2.7 to 5.5	P12	1	1	2.7	V	Int	0.5	3	Programmable: int ref, pwr consumption, settling time; SNR 78 dB, SFDR -74 dB @ f <sub>out</sub> = 1 kHz
TLV5638	12	2.7 to 5.5	Serial	1	2	4.5	V	Int	1	4	Simultaneous dual DAC update; programmable: int ref, pwr consumption, settling time; SNR 78 dB, SFDR -74 dB @ f <sub>out</sub> = 1 kHz
TLV5636	12	2.7 to 5.5	Serial	1	1	4.5	V	Int	1	4	Programmable: int ref, pwr consumption, settling time; SNR 75 dB, SFDR -69 dB @ f <sub>out</sub> = 1 kHz
TLV5633	12	2.7 to 5.5	P8	1	1	2.7	V	Int	0.5	3	Programmable: int ref, pwr consumption, settling time; SNR 78 dB, SFDR -74 dB @ f <sub>out</sub> = 1 kHz
TLV5619	12	2.7 to 5.5	P12	1	1	4.3	V	Ext	1	4	Asynchronous update; SNR 78 dB, SFDR -72 dB @ f <sub>out</sub> = 1 kHz
TLV5618A	12	2.7 to 5.5	Serial	2.5	2	2.4	V	Ext	1	4	Programmable: pwr consumption, settling time; SNR 76 dB, SFDR -72 dB @ f <sub>out</sub> = 1 kHz
TLV5616	12	2.7 to 5.5	Serial	3	1	0.9	V	Ext	1	4	Programmable pwr consumption; super small MSOP-8 package; SNR 74 dB @ f <sub>out</sub> = 1.1 kHz
TLV5614	12	2.7 to 5.5	Serial	3	4	3.6	V	Ext	1	4	Simultaneous quad DAC update; programmable pwr consumption; independent digital/analog supplies
TLV5613	12	2.7 to 5.5	P8	1	1	1.2	V	Ext	1	4	Programmable pwr consumption; separate digital/analog supplies; synchronous/asynchronous update
UCC5950	10	5		2.5	1	7.5	V		1	2	10-bit serial D/A converter with sleep mode
TLV5637	10	2.7 to 5.5	Serial	1	2	4.2	V	Int	0.5	1	Programmable: int ref, pwr consumption, settling time; SNR 56 dB, SFDR -62 dB @ f <sub>out</sub> = 1 kHz
TLV5617A	10	2.7 to 5.5	Serial	2.5	2	2.1	V	Ext	1	1	Programmable: pwr consumption, settling time; SNR 56 dB, SFDR -64 dB @ f <sub>out</sub> = 1 kHz
TLV5606	10	2.7 to 5.5	Serial	3/9	1	0.9	V	Ext	1	1.5	8-pin MSOP, programmable speed, high-speed serial interface, single 5V/3V supply, voltage-output buffer, power-down mode
TLV5604	10	2.7 to 5.5	Serial	3	4	3.3	V	Ext	0.5	0.5	Simultaneous quad DAC update; programmable pwr consumption; separate digital/analog supplies
TLC5615	10	5	Serial	12.5	1	0.75	V	Ext	0.5	1	1.21-MHz update rate; SINAD 60 dB @ 1 kHz
TLV5628	8	2.7 to 5.5	Serial	10	8	12	V	Ext	0.9	1	Octal; programmable for 1x or 2x output; simultaneous update
TLV5627	8	2.7 to 5.5	Serial	3	4	3	V	Ext	0.5	0.5	Programmable: pwr consumption, settling time; SNR 57 dB, SFDR -60 dB @ f <sub>out</sub> = 1.1 kHz
TLV5626	8	2.7 to 5.5	Serial	1	2	5.1	V	Int	0.5	1	Programmable: int ref, pwr consumption, settling time; SNR 57 dB, SFDR -62 dB @ f <sub>out</sub> = 1 kHz
TLV5625	8	2.7 to 5.5	Serial	2.5 or 12	2	2.1	V	Ext	0.2	0.5	Programmable: pwr consumption, settling time; SNR 54 dB, SFDR -50 dB @ f <sub>out</sub> = 1 kHz
TLV5624	8	2.7 to 5.5	Serial	1.0 to 3.5	1	4.5	V	Int	0.2	0.5	Programmable: int ref, pwr consumption, settling time; SNR 57 dB, SFDR -62 dB @ f <sub>out</sub> = 1 kHz
TLV5623	8	2.7 to 5.5	Serial	3	1	0.9	V	Ext	0.2	0.5	Programmable: pwr consumption, settling time; SNR 57 dB, SFDR -60 dB @ f <sub>out</sub> = 1.1 kHz
TLV5621	8	2.7 to 5.5	Serial	10	4	3.6	V	Ext	0.9	1	Simple two-wire interface in single-buffered mode; simultaneous update in double-buffered mode; one very low pwr DAC
TLV5620	8	2.7 to 5.5	Serial	10	4	6	V	Ext	0.9	1	Simultaneous-update quad; programmable 1x or 2x output range

(continued next page)

For technical support and ordering literature, see page 15.

## Selection Guide for Data Converters (continued)

## DACs (&lt; 10 MHz) (continued)

Device	Resolution (Bits)	Supply (V)	Data-Bus Interface (Bits)	Settling Time ( $\mu$ s)	Number of DACs	Power (typ) (mW)	Output (I or V)	V <sub>ref</sub> (Int/Ext)	DNL (max) ( $\pm$ LSB)	INL (max) ( $\pm$ LSB)	Comments
TLC7628	8	11 to 15	Parallel	0.1	2	20	I	Ext	0.5	0.5	Dual multiplying DAC; TTL-compatible digital inputs; super easy micro interface
TLC7528	8	5 to 15	Parallel	0.1	2	7.5	I	Ext	0.5	0.5	Dual TLC7524 (multiplying DAC)
TLC7524	8	5 to 15	Parallel	0.1	1	5	I	Ext	0.5	0.5	MDAC; fast control signaling; low glitch output; on-chip data latches; super easy micro interface
TLC7226	8	15	Parallel	5	4	60	V	Ext	1	1	Quad multiplying DAC; single or dual supply; TTL/CMOS compatible
TLC7225	8	5 to 15	Parallel	5	4	60	V	Ext	1	1	Quad; single or dual supply; direct bipolar operation without an external level-shift amplifier; TTL/CMOS compatible
TLC5628	8	5	Serial	10	8	15	V	Ext	0.9	1	Octal; programmable for 1x or 2x output; simultaneous update
TLC5620	8	5	Serial	10	4	8	V	Ext	0.9	1	Quad; programmable 1x or 2x output range

DACs ( $\geq$  10 MHz)

Device	Resolution (Bits)	Supply (V)	Update Rate (MSPS)	Settling Time ( $\mu$ s)	Number of DACs	Power (typ) (mW)	DNL (max) ( $\pm$ LSB)	INL (max) ( $\pm$ LSB)	Comments
THS5671A	14	3.0 to 5.0	125	35	1	175	3.5	7	CommsDAC; 81 dBc SFDR @ f <sub>clk</sub> = 25 MSPS, f <sub>out</sub> = 1 MHz
THS5661A	12	3.0 to 5.0	125	35	1	175	2	4	CommsDAC; 76 dBc SFDR @ f <sub>clk</sub> = 25 MSPS, f <sub>out</sub> = 1 MHz
THS8133/A/B†	10	3.0 to 5.0	80	5	3	525	1.2	1	SMPTE compliant tri-level sync generation, multiplexed YPbPr/GBR input mode
THS8134/A/B	8	3.0 to 5.0	80	5	3	635	1.2	1	SMPTE compliant tri-level sync generation, multiplexed YPbPr/GBR input mode
THS5651A	10	3.0 to 5.0	125	35	1	175	0.5	1	CommsDAC; 79 dBc SFDR @ f <sub>clk</sub> = 25 MSPS, f <sub>out</sub> = 1 MHz
TLC5602	8	5	30	30	1	80	0.5	0.5	TTL digital input voltage
TL5632	8	5	60	10	3	350	0.5	0.5	High performance at lowest cost for high-speed system
THS5641A	8	3.0 to 5.0	100	35	1	100	0.25	0.25	CommsDAC; 50 dB SINAD @ f <sub>clk</sub> = 50 MSPS, f <sub>out</sub> = 5 MHz

†THS8133B will be available in June 2000.

## DSPcodec

Device	Resolution (Bits)	Sampling Rate (kHz)	Bandwidth (kHz)	SNR (dB)	Number of Channels	Supply Voltage (V)	Power (typ) (mW)	Comments
TLV320AIC27	18	48	up to 9.92	90/95	2	3.3 to 5	171	AC97 compliant stereo codec, 4 modes of operation, variable sampling rate (8 kHz to 48 kHz)
TLV320AIC11	16	22.05	up to 9.92	84/85	1	3.3 to 5	39	Single, 16-bit, 3.0 to 5.5 V, ultra low power, master/slave capability, microphone interface, low I/O voltage
TLV320AIC10	16	22.05	up to 9.92	84/85	1	3.3 to 5	39	Single, 16-bit, 3.0 to 5.5 V, ultra low power, master/slave capability, microphone interface

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**Data Converter Application Reports**

To access any of the following application reports, type the URL [www.ti.com/sc/docs/psheets/abstract/apps/litnumber.htm](http://www.ti.com/sc/docs/psheets/abstract/apps/litnumber.htm) and replace *litnumber* with the number in parentheses beside the title.

- Interfacing A/D Converters TLC5540/10 to the DSKPlus DSP Starter Kit TMS320C54x (slaae14)
- Interfacing the TLC5510 Analog-to-Digital Converter to the TMS320C203 DSP (slaa029)
- Using References to Generate Offsets for the TLV55xx Family Data Converters (slaa063)
- Designing with the THS1206 High-Speed Data Converter (slaa094)

**Data Converter Evaluation Modules**

The following evaluation modules (EVMs) are available. To order any of the EVM kits listed, please call our toll free order desk number, 1-800-477-8924, and ask for ext. 5800 in North America. To order in other regions, please contact the TI Product Information Center for your region (see listings on this page) or contact your local TI distributor; see [www.ti.com/sc/docs/distmenu.htm](http://www.ti.com/sc/docs/distmenu.htm) for distributor listings.

Each EVM kit contains an evaluation board and a user's guide.

Device	Description	Price
C54XADAPTEVM	TMS320C54x™ DSKplus Adaptor Kit	\$50
THS0842EVM	Dual-channel (configurable), dual simultaneous sample and hold, low power, power down	\$99
THS1030EVM	2.7 V to 5.5 V, 10-bit, 30-MSPS CMOS ADC	\$99
THS1031EVM	2.7 V to 5.5 V, 10-bit, 30-MSPS CMOS ADC with PGA front end	\$99
THS1050EVM	10-bit, 50-MSPS IF sampling communications ADC	\$99
THS1060EVM	10-bit, 60-MSPS IF sampling communications ADC	\$99
THS1206EVM*	12-bit, 6-MSPS ADC	\$99
THS1408EVM	14-bit, 8-MSPS DSP-compatible ADC with internal reference and PGA	\$99
THS5641EVM	THS56X1 EVM for THS5641/5651/5661/5671 DACs	\$99

Device	Description	Price
THS5651EVM	THS56X1 EVM for THS5641/5651/5661/5671 DACs	\$99
THS5661EVM	THS56X1 EVM for THS5641/5651/5661/5671 DACs	\$99
THS5671EVM	THS56X1 EVM for THS5641/5651/5661/5671 DACs	\$99
THS8133EVM	Triple 10-bit, 80-MSPS video DAC with tri-level sync generation	\$99
THS8134EVM	Triple 8-bit, 80-MSPS video DAC with tri-level sync generation	\$99
THS10064EVM*	10-bit, 6-MSPS ADC	\$99
THS10082EVM**	10-bit, 8-MSPS ADC	\$99
THS12082EVM**	12-bit, 8-MSPS ADC	\$99
TLC2543EVM	5-V, 12-bit ADC	\$50
TLC2554EVM	12-bit, 400-KSPS, four-channel ADC with serial interface	\$99
TLC2558EVM	12-bit, 400-KSPS, eight-channel ADC with serial interface	\$99
TLC2932EVM	50-MHz Phase Lock Loop	\$99
TLC320AD50EVM	16-bit sigma delta AIC	\$99
TLC320AD545	Single-channel codec with hybrid op amps and speaker driver	\$75
TLC5510EVM	8-bit high-speed ADC	\$50
TLC5540EVM	8-bit, 40-MSPS ADC	\$50
TLC876EVM	10-bit, 20-MSPS ADC	\$50
TLV1544EVM	10-bit ADC with serial control and 4/8 analog inputs	\$50
TLV1562EVM	10-bit CMOS, high-speed programmable ADC	\$99
TLV1570EVM	10-bit, 1.25-MSPS, 2.7- to 5.5-V serial ADC with power down	\$50
TLV1571EVM	1-channel, 10-bit, 1.25-MSPS parallel ADC	\$50
TLV1572EVM	10-bit, 1.25-MSPS, 2.7- to 5.5-V serial ADC with power down	\$50
TLV1578EVM	8-channel, 10-bit, 1.25-MSPS parallel ADC	\$50
TLV2543EVM	3-V, 12-bit ADC	\$50
TLV2544EVM	12-bit, 200-KSPS ADC	\$99
TLV2548EVM	12-bit, 200-KSPS ADC	\$99
TLV320AIC10EVM	General-purpose 16-bit, 22-KSPS DSP codec	\$99
TLV5510EVM	8-bit, 10-MSPS ADC	\$50
TLV5535EVM	8-bit, 35-MSPS, low-power ADC	\$99
TLV5580EVM	8-bit, 80-MSPS ADC	\$99
TLV571EVM	2.7- to 5.5-V, 1-channel, 8-bit parallel ADC	\$99

\* Available June 2000  
\*\* Available July 2000



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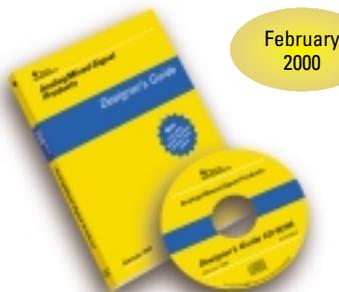
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