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Product Bulletin

HyperSAR+™ ATM Chipset
ABR Traffic Management Solution

Key specifications
- Two chip chipset with full ATM Available Bit Rate (ABR) traffic management solutions
- TNETA1575 Segmentation and Reassembly (SAR) device
  - Backwards pin-compatible with TNETA1570
  - Fully defined scheduler interface
  - Extended receive channel and VPI/VCI support
  - Supports up to 2,048 simultaneous segmentation and reassembly operations
- TNETA1585 Traffic Management Solution
  - Interfaces through COPI interface to TNETA1575 SAR
  - Provides scheduling for up to 2,048 ABR connections
  - Supports applicable ATM Forum standards
  - Software downloadable for easy upgrades

Two new ATM devices from Texas Instruments give designers a flexible and cost-effective way to fully implement an ATM traffic management solution. Part of TI's ThunderNET networking family, the HyperSAR+ chipset consists of the TNETA1575 high performance segmentation and reassembly (SAR) and the TNETA1585 traffic management scheduler. This solution provides high performance connections between legacy LANs and ATM networks.

The HyperSAR+ high performance SAR is a backwards-pin-compatible and software-compatible upgrade for the TNETA1570 HyperSAR™. By using the SAR device in conjunction with the traffic management scheduler, designers can build ATM traffic management solutions that fully support the ATM Forum's Available Bit Rate (ABR) traffic specification.

TNETA1575 High Performance SAR
The TNETA1575 SAR adds to the TNETA1570's functionality with additional, performance enhancing features, including a fully defined scheduler interface, extended transmit and receive channel support, extended virtual path identifier (VPI)/virtual channel identifier (VCI) support, two sideband controlled free buffer rings, increased on-chip receive FIFO and a free buffer cache.

The scheduler interface contributes to the solution's versatility with support for all ATM service categories. Functionally, it provides connection to an external scheduler, such as the TNETA1585 traffic management scheduler, to create a two-tiered scheduler mechanism. Scheduling mechanisms in the TNETA1575 SAR are used for Constant Bit Rate (CBR) traffic. The TNETA1585 traffic management scheduler is used for other service categories, including ABR, variable bit rate (VBR) and unspecified bit rate (UBR). The TNETA1575 SAR incorporates support for the full range of VPI/VCI addresses

required for large, scalable virtual LANs. This large address range allows the device to access all possible combinations of VPI and VCI addresses and supports up to 2,048 simultaneous segmentation and reassembly operations.

The TNETA1575 is designed to enable high performance on both the transmit and receive sides. For the transmit side, this includes a Transmit Channel Sleep Mode that prevents polling of transmit channels when no data is queued. For the receive side, the device makes use of PCI Bus Sideband signals to provide implicit handshaking between the host processor and

ThunderNET: The Architectural Approach to Networking

The TNETA1575 SAR and TNETA1585 TMS give designers a flexible and cost-effective way to fully implement an ATM traffic management solution.

the SAR. This eliminates the use of PCI bus transactions to check the status of control structures like completion rings. Together, these features reduce the amount of bus bandwidth needed to transmit and receive ATM packets and provide increased performance.

The TNETA1585 Traffic Management Solutions

The TNETA1585 traffic management scheduler is a highly flexible, software downloadable traffic management scheduler that implements the International Telecommunications Union's (ITU) and ATM Forum's ABR service category specifications. The device interfaces directly to the TNETA1575 SAR via the scheduler interface and can provide scheduling for up to 2,048 ABR connections. It provides configuration support for all primary and optional ATM Forum Traffic Management 4.0 (TM4.0) parameters, supports TM4.0-defined Resource Management Cell formats and is receive UTOPIA 2.01 compliant.

The TNETA1585 is also designed with the ability to track changes to the ATM Traffic Management specification. The updated software is simply downloaded to the scheduler, rather than changing hardware designs.

ATM System Block Diagram
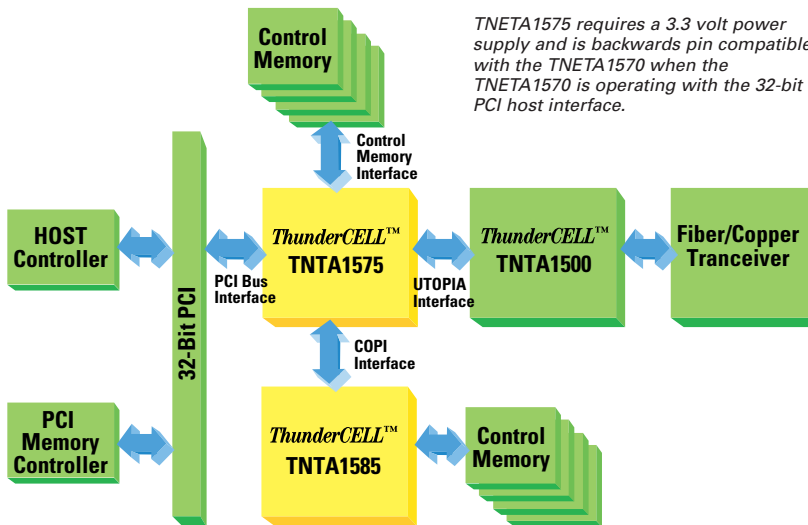
TNETA1575 requires a 3.3 volt power supply and is backwards pin compatible with the TNETA1570 when the TNETA1570 is operating with the 32-bit PCI host interface.

Development Support

Texas Instruments provides a Windows-based, 32-bit PCI evaluation kit to help designers evaluate the HyperSAR+ traffic management solution in their system. Functional features of the module include transmit and receive of ATM data, RM cell extractions, incoming traffic monitoring and test and alarm conditions. Third party software drivers are also available to provide turnkey ATM internetworking solutions. In addition, TI provides application notes to further assist designers in creating optimized ATM designs.

For More Information

The HyperSAR+ TNETA1575 high performance SAR and TNETA1585 TMS are part of TI's full line of ThunderCELL™ ATM internetworking products. In addition, TI also provides networking and internetworking chipsets for high speed Ethernet and token ring systems. All of TI's networking silicon is designed for maximum flexibility, upgradability and interoperability.

If you would like more information on the HyperSAR+ SAR and the traffic management scheduler or any of TI's internetworking products, please visit our World Wide Web site at http//www.ti.com or contact your local TI Field Sales Office.

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