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Basic Clock Module, Oscillator and Clock Generator

Chapter 8

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Preface

Read This First

About This Manual

This user's guide is a preliminary book for the MSP430 family basic clock module, oscillator and clock generator which is also Chapter 8 of the *MSP430 Family Architecture Guide and Module Library User's Guide.*

Related documentation is listed on pages iii and iv.

How to Use This Manual

This document contains the following chapters:

- **Chapter 8** includes a list of features, a block diagram, a pinout, signal descriptions, references for different oscillators, digitally controlled oscillators, operation of the DCO modulator, system clocks and operating modes for the basic clock module, registers, and typical DCO characteristics.

Related Documentation From Texas Instruments

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MSP430 Family Architecture Guide and Module Library User's Guide (Literature Number: SLAU012) which presents detailed hardware and software information for the MSP430 family of devices.

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Chapter 8

Basic Clock Module, Oscillator and Clock Generator

The basic clock module, oscillator, and system clock generator meet the major design targets of low system cost and low power consumption. Using three internal clock signals optimizes the system performance. A configuration with three internal clock signals gives the MSP device the flexibility of various external configurations. The user can configure the MSP device with no external components, with one external resistor, with one or two external crystals or resonators, or any combination.

By reducing the external component count, the designer achieves a lower cost package. The user can configure the module to use the internal, RC-type, digitally controlled oscillator (DCO), to supply the clock for the package.

Topic **Page**

The basic clock module includes:

- One digital controlled oscillator (DCO) with RC-type characteristics
- One crystal oscillator used for low-frequency crystals (watch crystals, e.g., 32,768 Hz) or for crystals in the range of 450 kHz to 8 MHz. See the specific data sheet for the operating frequency range of the target device.
- One optional crystal oscillator for crystals in the range of 450 kHz to 8 MHz. See the specific data sheet for the operating frequency range of the target device.

The basic clock module supplies the MSP430 with three clock signals:

- ACLK, crystal oscillator signal
- MCLK, controllers main system clock
- SMCLK, sub main system clock used to run the peripheral module function

The three clock signals come from three clock sources:

- DCO clock (DCOCLK)
- low/high frequency oscillators clock (LFXT1CLK)
- high frequency oscillator (XT2CLK, optional).

The selected clock frequencies can be divided by 1, 2, 4, or 8. The division rate is software selectable.

8.1 Features for Current Limited Applications

Devices that are considered to be low power consumers have unique features that should be taken into account. Some of these features include:

- Varity of operating modes, driven by application requirements and be software selectable.
- Support of a burst mode, that when activated, rapidly starts and stops the entire system (in active mode)
- Sufficient stabilization of voltage, temperature, and time including a highly stable time base for real-time clocks.

Current-limited real-time applications have two conflicting requirements:

- Low system clock frequency for energy conservation
- High system clock frequency for fast reactions to event requests.

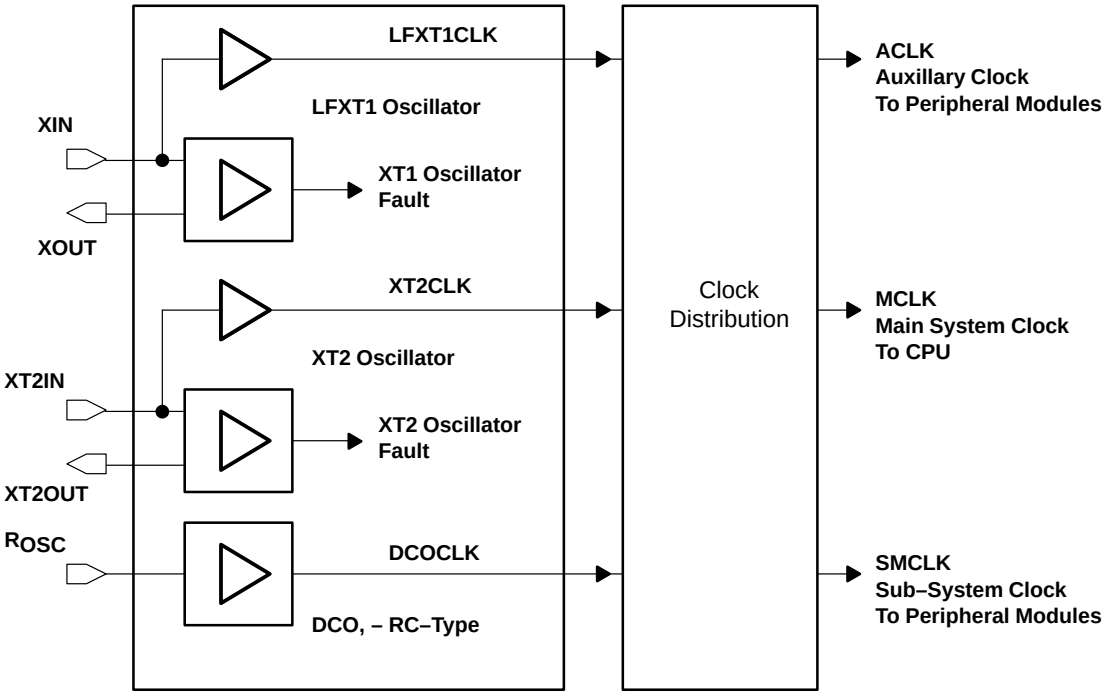
Current consumption in battery based applications is of great concern to the design engineer. In real-time applications, a response to an external event or time request occasionally requires high speed. A clock generator with a fast start-up allows complete use of different power dissipation modes that could theoretically solve these concerns. Unfortunately, fast start-up and low frequency instability are closely associated. Multiple clock source designs or different clock operations take into account the clock requirements of certain peripheral components for real-time applications. These applications include low frequency communications, displays (i.e., LCDs), timers, and counters.

The different requirements of the CPU and associated modules, driven by system cost and current consumption objectives, lead to the use of three clock signals.

- Auxiliary Clock (ACLK), with LF crystals frequency
- Main System Clock (MCLK), used by the CPU and system
- Sub–System Clock (SMCLK), used by the peripheral modules.

The implementation of the basic clock module into MSP430 devices can have two or three oscillators.

Figure 8–1. Basic Clock Module with Three Oscillators



The two-oscillator configuration uses the LFXT1CLK signal in place of the XT2CLK signal.

Figure 8–2. Basic Clock Module with Two Oscillators

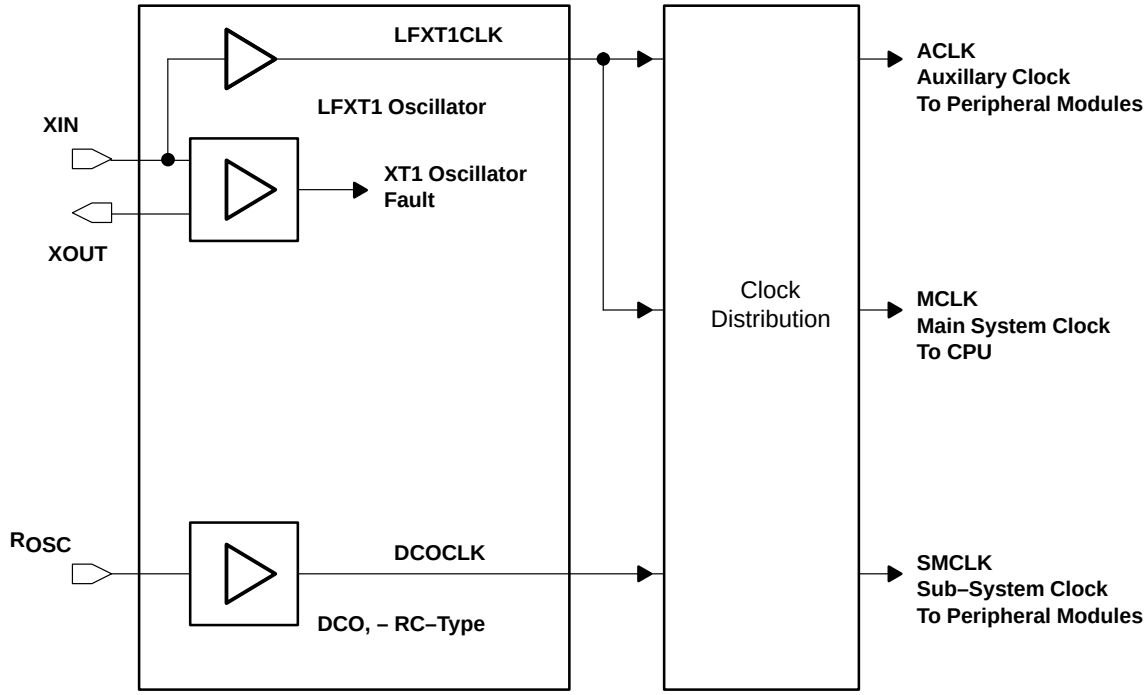
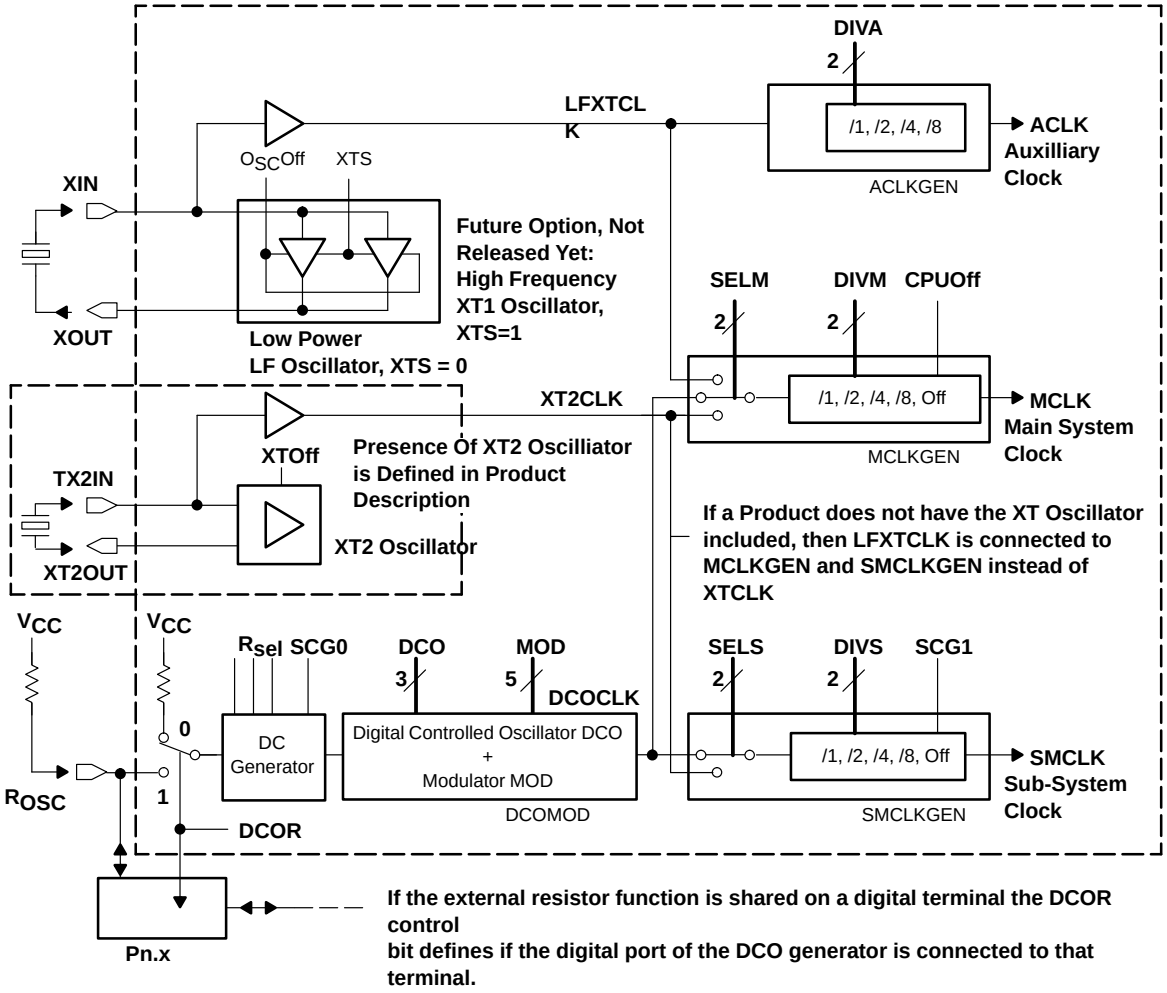


Figure 8–3. Principle of Clock Generation



The clock distribution system selects a clock source, individually, for each of the three clock outputs:

- One clock source for the CPU clock; MCLK signal
- Two clock sources for the peripheral module clocks; SMCLK and ACLK

The auxiliary clock (ACLK) is the buffered output of the LFXT1 oscillator and provides clock signals for peripheral modules. The control bit XTS selects whether the LFXT1 oscillator operates as a low-frequency (LF) crystal oscillator or as a high-frequency (XT1) oscillator.

Note: The XTS bit option: Software selection of the LF or XT1 oscillator

The oscillator can be selected, in the future, for low frequency (LF) or medium/high frequency (XT1) operation using the control bit XTS. Presently control bit XTS must be reset. The XT1 function may not be selected.

The source of the main system clock (MCLK) is determined by which clock is selected.

- LFXT1CLK
- XT2CLK
- DCOCLK

The control bit DIVM determines the division of the clock source, 1, 2, 4, or 8. The CPUOff bit is located in the status register and halts the selected clock source.

The source of the subsystem clock (SMCLK) is:

- XT2CLK (or LFXT1CLK with the two oscillator implementation)
- DCOCLK.

The control bit DIVS selects how the clock source is divided, 1, 2, 4, or 8. The SCG1 bit is located in the status register and halts the selected clock source.

8.2 LF Oscillator

Two factors determine the choice of the watch crystal (LF oscillator):

- An oscillator and time base for low current consumption
- Optimization of system costs.

The special design of the LF oscillator supports low current consumption and the use of a 32,768 Hz crystal or resonator. The crystal or resonator connects to the clock module via two terminals without any other external components. All the necessary components for stabilizing clock operation or phase shifter capacitors have been integrated into the MSP430.

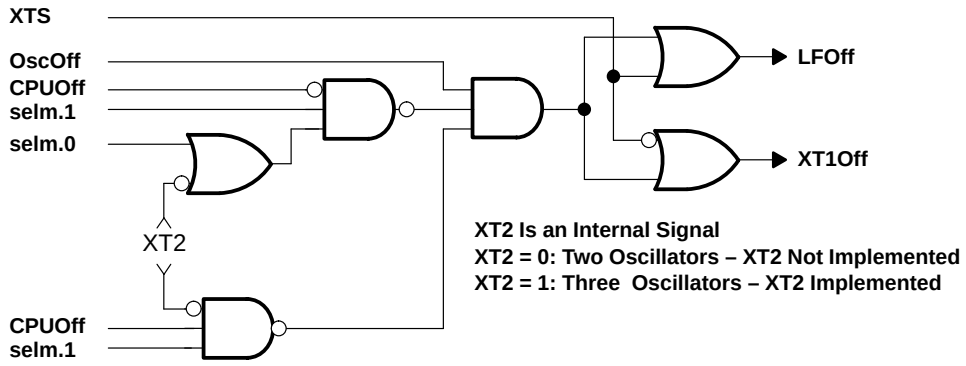
The clock distribution selects the LF oscillator when the control bit XTS is reset. The oscillator starts operating after V_{CC} has been applied due to a reset of the control bit (OscOff) in the status register (SR). Setting the OscOff bit stops the LFXT1 oscillator.

Figure 8–4. Status Register SR

15	8	7							0
reserved for future enhancements	V	SCG 1	SCG 0	Osc Off	CPU Off	GIE	N	Z	C
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

If the LFXT1CLK clock signal is used for the main system clock (MCLK), or the sub-system clock (SMCLK), then it cannot be switched off. The LFXT1CLK forms MCLK if the CPUOff bit is reset and SELM = 3 (or 2). The LFXT1CLK forms SMCLK if the SCG1 bit is set and SELS = 1**.** When the XT2 oscillator is not part of the oscillator system (defined in the device specification) the LFXT1CLK signal connects to the MCLKGEN block instead of the XT2CLK signal (which is selected when SELM = 2).

Figure 8–5. Off Signals for the LF and XT1 Oscillator in the LFXT1 Block



OscOff	CPUOff	SELM.x	SCG1	SELS	LFXT1CLK	Comment
0	x	x	x	x	on	Oscillator Active
1	0	3 or 2+3†	x	x	on‡	Clock Signal Needed For MCLK
1	x	x	0	1	on‡	Clock Signal Needed For SMCLK

† Two oscillators: SELM.x = 3. Three oscillators: SELM.x = 3 and 2

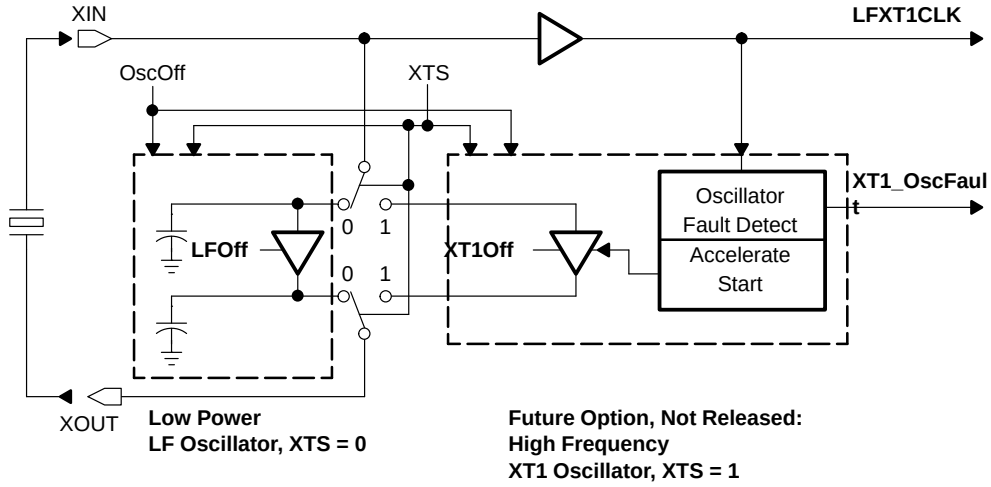
‡ LFXT1CLK is switched off in all other bit combinations

8.3 XT1 Oscillator – Future Option for LFXT1CLK Signal

The design of the XT1/XT2 oscillator supports crystal or resonator components. The XT1 and XT2 oscillators have the same features. The crystal or resonator is connected on two pins, and requires, on both the terminals external capacitors to be sized according to the specification for that crystal or resonator. All other components for stabilizing clock operation are integrated into the clock module. The software selects XT1 crystal oscillator whenever operation requires frequency stability for accurate internal clocks. Setting the control bit XTS to a logic 1 selects the XT1 oscillator in the LFXT1 block.

The oscillator halts and resets when initially applying V_{CC} or when setting the RST/NMI terminal to the reset state. Since the POR signal is used to stop the XT1 oscillator, (using the XTS bit) the watchdog does not stop the oscillator regardless of whether the security key has been violated or the time has expired. The system clock (MCLK) is then selected to be generated from the digitally controlled oscillator DCOCLK. If a watchdog security violation or time expiration occurs, along with the power up clear (PUC), software will modify the control bits in such a way that the MCLK will come from the DCO.

Figure 8–6. Principle of LFXT1 Oscillator

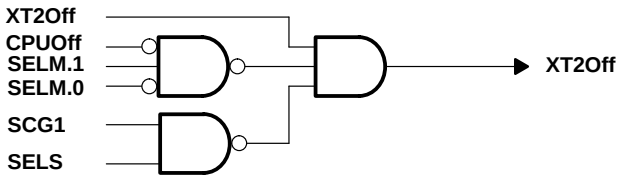


The oscillator fault detection and start acceleration of the XT1/XT2 operation is described in the following *XT2 Oscillator* section.

8.4 XT2 Oscillator

The XT2Off control bit disables the XT2 oscillator if the XT2CLK signal is not used for the MCLK or the SMCLK. If the CPUOff bit is reset and SELM = 2, XT2CLK generates MCLK . The XT2CLK generates SMCLK if SCG1 is reset and SELS = 1.

Figure 8–7. XT Oscillator Fault Detection, Identical for XT1 and XT2 Oscillator



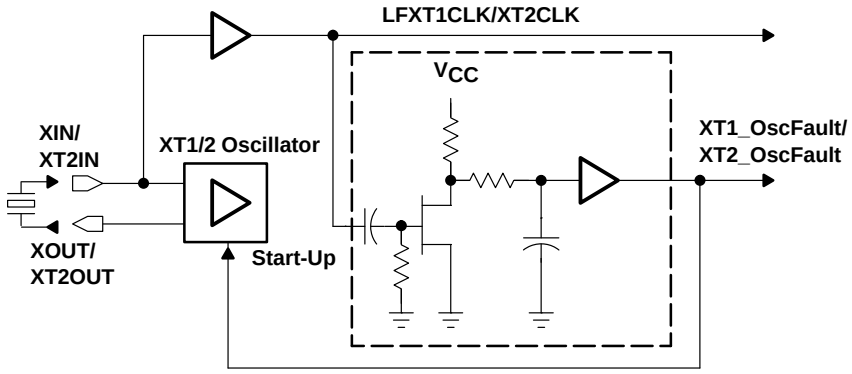
OscOff	CPUOff	SELM.x	SCG1	SELS	LFXT1CLK	Comment
0	x	x	x	x	on	Oscillator Active
1	0	2	x	x	on†	Clock Signal Needed For MCLK
1	x	x	0	1	on†	Clock Signal Needed For SMCLK

† XTCLK is switched off in all other bit combinations

8.4.1

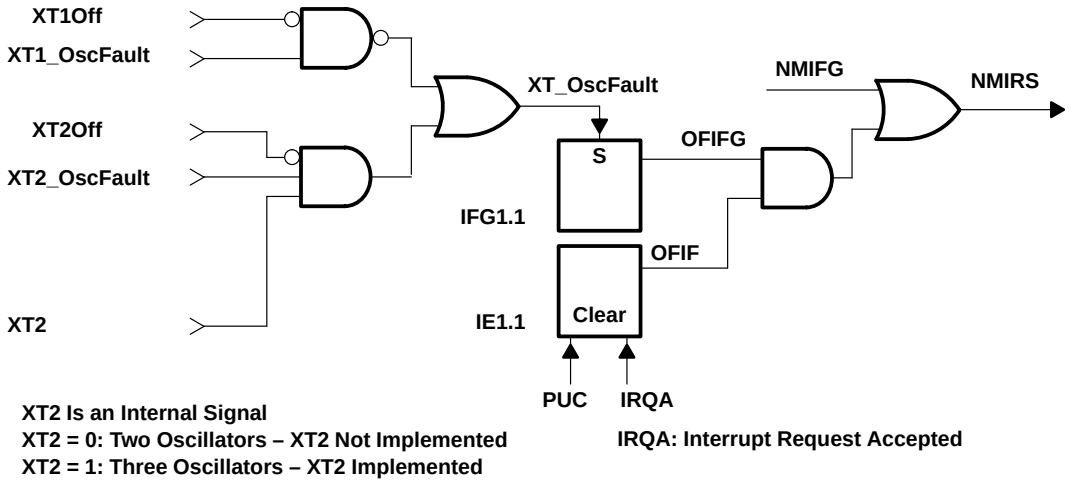
An analog circuit controls the operation of the XT oscillator, which flags an oscillator fault when approximately 100 cycles (at 1 MHz) of the crystal are missed. The active OSCFault signal sets the oscillator fault interrupt flag (OFIFG) and requests a non-maskable interrupt when the oscillator fault interrupt enable bit (OFIE) is set. At the same time, the oscillator fault flag switches the crystal oscillator to a faster start–up function. However, the faster start-up operation increases the current consumption of the crystal oscillator.

Figure 8–8. Principle of a XT Oscillator



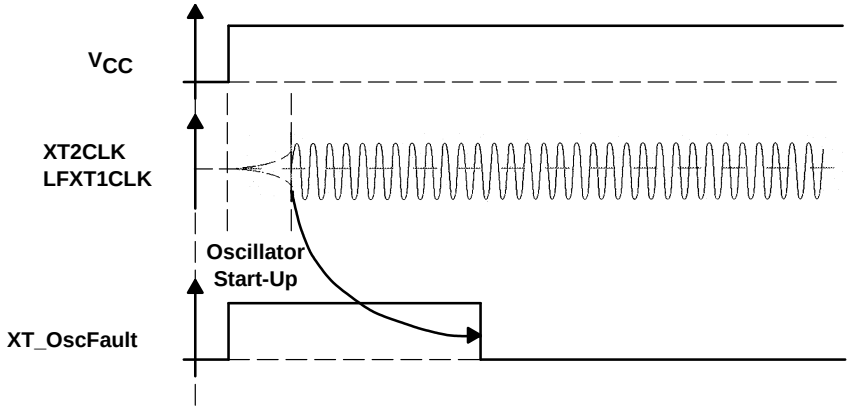
The XT2_OscFault signal of the XT2 oscillator and the XT1_OscFault signal of the XT1 oscillator (in the LFXT1 oscillator) will set the oscillator fault interrupt flag (OFIFG) independently. During two-oscillator implementation, the oscillator fault interrupt flag can be reset by software if the XT1_OscFault signal is a logic low. During three-oscillator implementation, the oscillator fault interrupt flag can be reset by software only if both oscillator fault signals, XT1_OscFault and XT2_OscFault, are low.

Figure 8–9. Oscillator Fault Interrupt



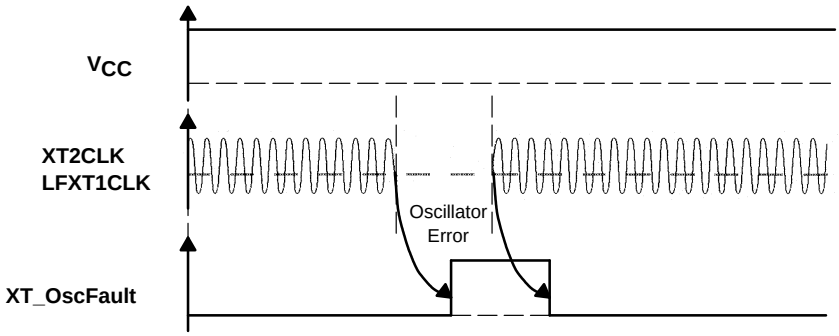
After applying V_{CC} the oscillator fault signal (XT_OscFault), is active. The XT_OscFault signal becomes inactive when the XT2CLK and/or the LFXT1CLK begin oscillating which is after approximately 100 clock cycles (at 1 MHz).

Figure 8–10. Oscillator Fault Signal in XT Oscillator



XT_OscFault becomes active after the XT2CLK and/or LFXT1CLK stop oscillating. The delay associated with the XT_OscFault signal is approximately 100 clock cycles/MHz).

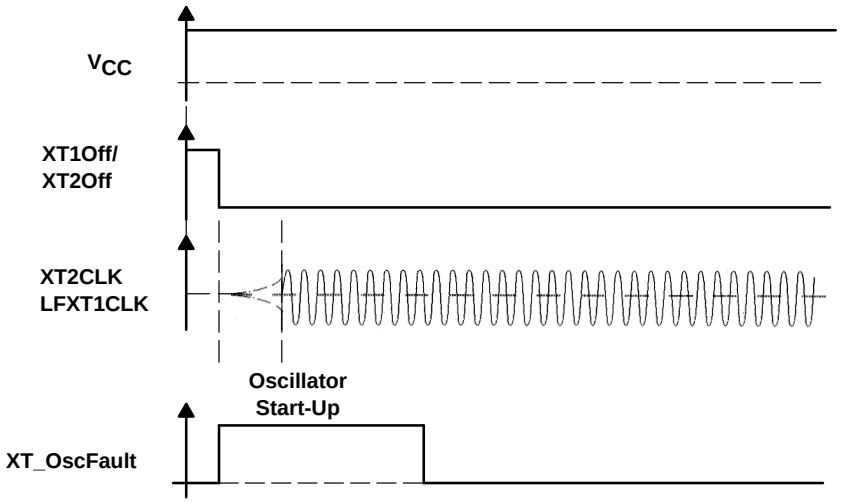
Figure 8–11. Oscillator Fault in Oscillator Error Condition



The oscillator fault signal returns to a logic low if the oscillator starts operating again. The delay is typically 100 clock cycles/MHz.

When an XT oscillator has stopped, and is then restarted, the oscillator fault signal (XT_OscFault), is active until the oscillator is operating, with a delay of typically 100 clock cycles/MHz.

Figure 8–12. Oscillator Fault in Oscillator Error Condition



8.5 Digitally Controlled Oscillator (DCO)

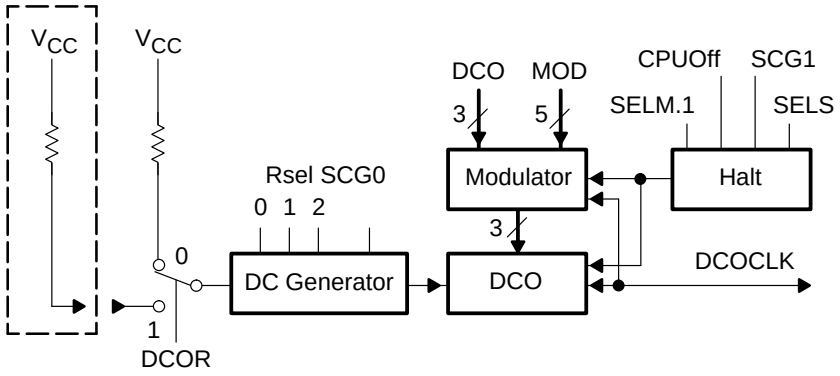
The DCO meets different requirements according to the application and system conditions. They include the following:

- ❏ Contributes to a low system cost; it operates from internal resistors or with one external resistor. The resistor selected defines the nominal frequency
- ❏ Starts immediately on external or internal system hardware requests or events
- ❏ Exhibits low current consumption
- ❏ The frequency is software controlled

The frequency of the DCO varies with the individual device, the external resistor, the supply voltage, and the temperature. The DCO is absolutely monotone. Software can control the actual frequency using the DCO control bits and the modulator input using the modulator control bits (MOD).

The power–up clear condition (PUC), occurs after applying V_{CC} or a reset condition to the RST/NMI terminal, if the watchdog expires or if the security key was violated. During a PUC, the control bits for the resistor (Rsel) are set to 4, the control bits for the DCO are set to 3. MOD bits , are reset and the DCO operates with a medium range frequency that has been defined with the internal resistor.

Figure 8–13. Schematic of System Frequency Generator

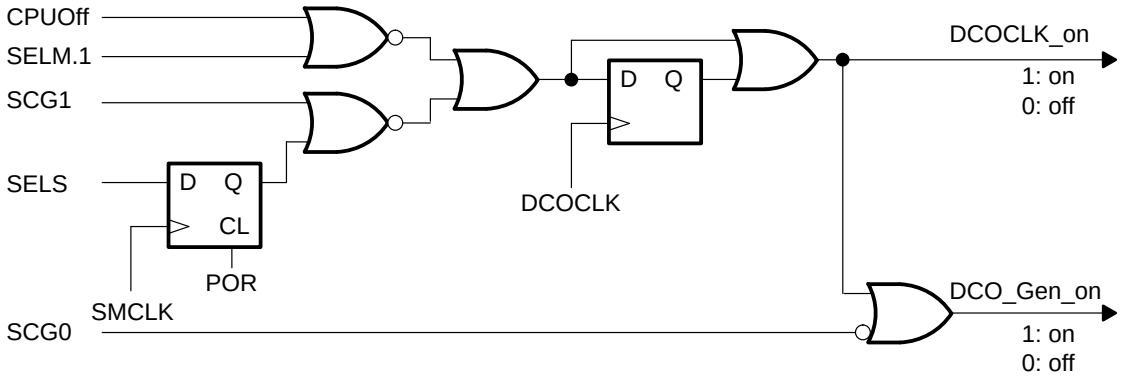


The internal resistor is also connected to the DC–generator, which determines the operating frequency of the DCO clock signal (DCOCLK). The DCO clock signal (DCOCLK) and the DC-generator, which is needed for DCOCLK operation, are always switched on automatically if the DCOCLK frequency is used for a MCLK (CPUOff = 0 and SELM.1 = 0) or SMCLK (SCG1=0 and SELS=0). If the DCOCLK is needed for operation, the SCG0 bit can not switch off the DC–generator.

8.5.1 Digitally Controlled Oscillator

Five bits (SCG0, CPUOff, SELM.1, SCG1, and SELS) control the operation of the oscillator, the modulator, and the DC-generator.

Figure 8–14. On/Off Control of DCO



SCG0	CPUOff	SELM.1	SCG1	SELS	DCOCLK	DCOGEN	Comment
x	0	0	x	x	on	on	DCO Clock Needed For MCLK
x	x	x	0	0	on	on	DCO Clock Needed For SMCLK
0	0	1	(see Note A)		off	on	DCO Clock is Not Needed
0	1	x			off	on	For MCLK (and SMCLK)
0	(see Note B)		0	1	off	on	DCO Clock is Not Needed
0			1	x	off	on	For SMCLK (and MCLK)
1	(see Note C)				off	off	DCO Clock is Not Needed: SCG0 Bit Switch Off DCOGEN

NOTES: A. SMCLK does not need the DCOCLK signal, if:
SMCLK is switched off (SCG1 = 1) or DOCCLK is not selected for SMCLK (SELS = 0).
B. MCLK does not need the DCOCLK signal, if:
MCLK is switched off (CPUOff = 1) or DOCCLK is not selected for MCLK (SELM.1 = 1).
C. MCLK and SMCLK does not need the DCOCLK signal, if:
The control bit SCG0 in the status register can switch off (SCG0 = 1) the DCOGEN.

The initial state of the control bits after a PUC are reset and the DCO starts operating. The software decides immediately after starting the program execution which clock source to use for the MCLK and which clock source to use for the SMCLK.

The DC-generator, when switched off, requires some minimal start-up time due to its low current design. Once the current is switched off, the resistor injects current in the microamp range, into the DC-generator and the internal and external parasitic capacitance form a delay in the microsecond range. In operating modes that do not require to switch off the DC–generator current, no delay occurs.

The frequency of DCOCLK is determined by the following functions:

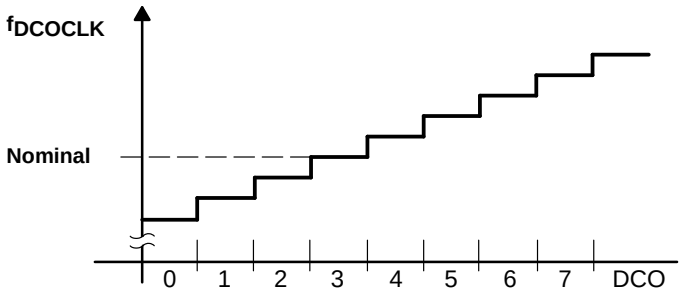
- The circuit injects current into the DC-generator (DCGEN) at a rate set by an external resistor and/or an internal resistor. The type of resistor depends on the configuration selected. The internal resister value is controlled by the four bits Roff, Rsel2, Rsel1, and Rsel0, and the injected current defines the nominal frequency.

If the external resistor option is selected (DCOR=1) and the device terminal is shared with a secondary function, then connect the external resistor terminal to the DC-generator.

- The three control bits, DCO0 to DCO2, can modify the frequency around the nominal frequency
- The five modulation bits, MOD0 to MOD4, switch between the frequency selected by the DCO bits and the next higher frequency set by DCO+1.

The current injected into the DC-generator, when the control bits in the DCO are set to 3, defines the oscillator's nominal frequency. The nominal frequency varies with the selection of the individual components (internal or external), the operating temperature and the operating voltage. The clock period of the DCOCLK signal is changed by roughly ten percent per step of the control bits DCO.

Figure 8–15. Principle Period Steps of the DCO



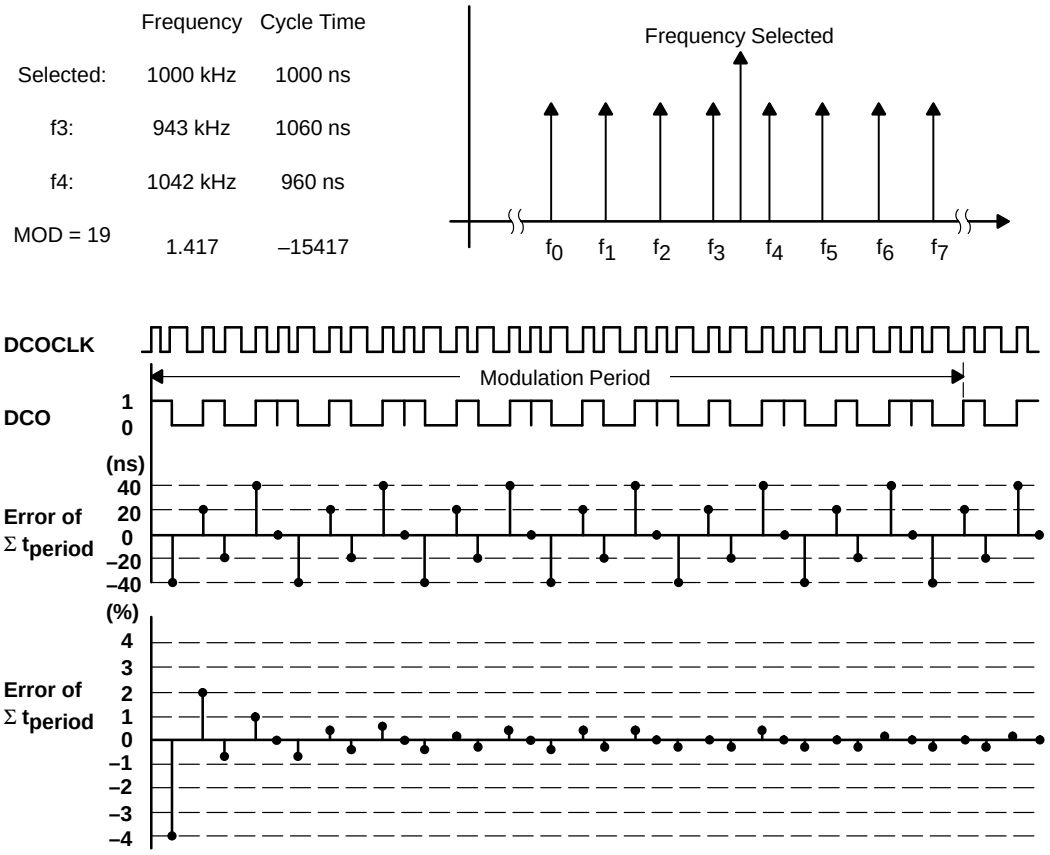
8.5.2 Operation of the DCO Modulator

The modulator is intended to reduce the period between steps by averaging the period intervals in the processing time. The modulator has a period of 32 DCOCLK clock cycles. The MOD control bits define the timing interval of the DCO+1 period that is run in the oscillator. The remaining 32-MOD time slots use DCO period. If the modulation constant is 0, the DCO data in the control register defines the period. The following formula defines the accumulating periods:

$$t = (32 - MOD) \times t_{DCO} + MOD \times t_{DCO+1})$$

The basic modulation frequency is the same as the DCOCLK frequency and the frequency is as high as feasible. The modulator selects f_{dco} or $f_{dco}+1$ individually for each DCO cycle. This is the highest possible rate that can be modulated between two discrete frequency steps. The following example illustrates the principle operation of the modulator.

Figure 8–16. Operation of the DCO Modulator



The user should consider two factors when reviewing the timing accuracy generated from the DCOCLK signal:

- ❏ short term accuracy: each individual cycle is as inaccurate as the DCO steps define
- ❏ long term accuracy: the averaging of a lot of individual cycles reduces the relative error down to less than 1/3 percent, assuming a step delta of 10% and a modulation period of 32.

Proper use of the modulation feature on the DCOCLK period increases the accuracy by averaging the periods. The DCOCLK periods are defined by the selected frequency that is set via the control bits in the DCO and the modulation fraction that is defined by the control bits in MOD .

Note: Control of DCOCLK Frequency

The frequency of the digitally controlled oscillator varies with temperature and voltage and is different for each individual sample. The frequency can be controlled by software if an external reference (i.e., ACLK signal) is used to measure the difference and to readjust the DCO frequency.

8.6 System Clocks and Operating Modes for the Basic Clock Module

The software, using control signals, controls the DCO and the crystal oscillators (XT2 and LFXT1). The status register contains four signals and these signals reset during the four different PUC conditions. Local registers in the basic clock module contain the other signals.

The four control bits in the status register provide the system application with different operating conditions. These bits also provide the maximum flexibility to optimize the overall system power consumption. Additionally, the control bits in the basic clock module provide further options to reduce the power consumption. The clock sources, clock frequencies, and external crystals can be set to the minimum frequency. A separate clock exists for the control of the CPU core system versus the peripheral modules. The CPU core system uses MCLK while the peripheral modules use SMCLK.

The selected clock source operates with the original frequency or may be divided down.

The digitally controlled oscillator is disabled when not used for MCLK or for SMCLK. The DC–generator must be switched off separately, but is switched on automatically when the DCOCLK signal is used, either for MCLK or SMCLK.

The different operating modes of the basic clock system provide a wide range for the system operating frequency. The basic clock system supports burst mode operation with the smallest operating time slot possible and an optimized current consumption in each time slot.

8.6.1 Starting from Power Up Clear (PUC)

When coming out of a PUC, the control bits for the internal resistor (R_{sel}), are set to 4, the control bits for the oscillator DCO are set to 3, and the control bits for the modulator (MOD) are reset. The oscillator starts with a medium frequency for DCOCLK. The internal resistor supplies the necessary current for the oscillator's DC–generator so that the oscillator can operate independently from any external condition. The system clock (MCLK) and the peripheral module clock (SMCLK) are driven by DCOCLK signal. The software starts immediately after applying V_{CC} or by removing a reset condition at RST/NMI. The software then selects the clock system configuration that is optimal for further operations:

- Combine which oscillators are active; LFXT1 oscillator, XT2 oscillator or the DCO
- Select the source for the ACLKGEN, MCLKGEN and SMCLKGEN
- Select the division rate for the selected clock source for the ACLKGEN, MCLKGEN and SMCLKGEN

8.6.2 Internal Bias Resistor for the DC–Generator

The internal bias resistor ensures fail safe operation during start up of the controller. It can be used if the requirements to the system frequency are met by the characteristics of the integrated solution (see data sheets).

8.6.3 Low-Power Modes

The combination of three oscillators and control features enable various low power modes. They include the following:

- CPUOff; the controller stops operation and there is no activity on the MCLK line
- SCG1; the clock signal SMCLK for the peripherals is inactive
- OscOff; LFXT1 oscillator off**,** the LFXT1 oscillator is stopped, but only if it is not used for MCLK or SMCLK
- XT2Off, XT1 oscillator off; the XT2 oscillator is stopped, but only if it is not used for MCLK or SMCLK
- DCO and DC-generator off; the DCO operates if the DCOCLK signal is used by MCLK or SMCLK. The DC oscillator is completely switched off and starts immediately when the DC-generator becomes active. The DCO clock starts after a short delay (in the microsecond range) if the DC-generator was switched off. The current consumption of the DCO system is switched off if the DCO and the DC-generator are off.

8.7 Basic Clock Module Control Register

The system clock generator interacts with other processor parts using three module registers and four bits of the status register. The module registers are mapped into the lower peripheral file address range where all byte modules are located. The operating mode control bits in the status register (SR) include; CPUOff, SCG1, SCG0 and OscOff. The SR is part of the CPUs register set.

Three eight-bit registers control the basic clock generator. The user software handles the clock system requirements using these registers which are only addressable using byte instructions.

8.7.1 Digitally Controlled Oscillator (DCO) Clock Frequency Control

All control bits of the DCO and the modulator are reset with the PUC condition which occurs by applying V_{CC}, reset at RST/NMI terminal, watchdog timer (WDT) security key violation, or the expiration of the watchdog timer.

DCOCTL
056h

7							0
DCO.2	DCO.1	DCO.0	MOD.4	MOD.3	MOD.2	MOD.1	MOD.0
rw–0	rw–1	rw–1	rw–0	rw–0	rw–0	rw–0	rw–0

MOD.0 .. MOD.4: The MOD bits define how often the discrete frequency ($f_{DCO+1)}$ within the period of 32 DCOCLK cycles is used. During the remaining clock cycles, 32–MOD, the discrete frequency f_{DCO} is used. When the DCO constant is set to seven, no modulation is possible since the highest feasible frequency has then been selected.

DCO.0 .. DCO.2: The DCO constant defines which one of the eight discrete frequencies is selected. The frequency is defined by the current injected into the DC–generator.

8.7.2 Oscillator and Clock Control Register

Three control bits of the digitally controlled oscillator and the five volt operation of the XT1/XT2 oscillators are set or reset as a result of the PUC condition: applying V_{CC}, a reset at RST/NMI terminal, a watchdog timer (WDT) security key violation, or an expiration of the WDT. The other four control bits are set or reset as a result of the power on reset (POR) conditions: (applying V_{CC} or a reset condition at the RST/NMI terminal).

BCSCTL1
057h

7							0
XT2Off	XTS	DIVA.1	DIVA.0	XT5V	Rsel.2	Rsel.1	Rsel.0
rw–(1)	rw–(0)	rw–(0)	rw–(0)	rw–0	rw–1	rw–0	rw–0

Bit0 to Bit2: The internal resistor is selected in eight different steps.

Rsel.0 to Rsel.2 The value of the resistor defines the nominal frequency. The lowest nominal frequency is selected by setting Rsel=0.

Bit3, XT5V: The XT1 and XT2 oscillators (also in LFXT1 block) operate over the full supply voltage swing, or in a reduced voltage range of approximately 5 V. By selecting the operation voltage to be the same as the supply voltage, current consumption can be reduced. For example, the selection of a 5-V operation reduces the current consumption of the oscillator using a 5-V supply voltage:

XT5V=0: The oscillator operates across the full supply voltage, but has an increased current consumption at 5 V.

XT5V = 1: The current consumption for the oscillator is reduced if the supply voltage is around 5 V. The XT5V works on both XT oscillators; XT1 and XT2.

Bit4 to Bit5: The selected source for ACLK is divided by:

DIVA = 0: 1
DIVA = 1: 2
DIVA = 2: 4
DIVA = 3: 8

Bit6, XTS: The LFXT1 oscillator operates with a low-frequency clock crystal or with a high-frequency crystal:

XTS = 0: the low-frequency oscillator is selected.

XTS = 1: the high-frequency oscillator is selected.

The oscillator selection must meet the external crystals operating condition.

Bit7, XT2Off: The XT2 oscillator is switched on or off:

XT2Off = 0: the oscillator is on

XT2Off = 1: the oscillator is off, if it is not used for MCLK or SMCLK.

BCSCTL2
058h

7							0
SELM.1	SELM.0	DIVM.1	DIVM.0	SELS	DIVS.1	DIVS.0	DCOR
rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0	rw–0

Bit0, DCOR: The DCOR bit selects an internal resistor for injecting current into the DC–generator. Based on this current, the oscillator operates if activated.

DCO = 0: Internal resistor on, the oscillator can operate. The fail safe mode is on.

DCO = 1: Internal resistor off, the current must be injected externally if the DCO output drives any clock using the DCOCLK.

Bit1, Bit2: The selected source for SMCLK is divided by:

DIVS.0 .. DIVS DIVS = 0: 1
DIVS = 1: 2
DIVS = 2: 4
DIVS = 3: 8

Bit3, SELS: Selects the source for generating SMCLK:
SELS = 0: Use the DCOCLK
SELS = 1: Use the XT2CLK signal (in the 3 oscillator system)
or
LFXT1CLK signal (in the 2 oscillator system)

Bit4, Bit5: The selected source for MCLK is divided by:

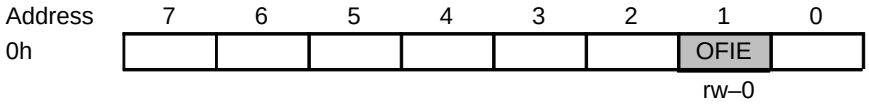
DIVM.0 .. DIVM.1 DIVM = 0: 1
DIVM = 1: 2
DIVM = 2: 4
DIVM = 3: 8

Bit6, Bit7: Selects the source for generating MCLK:
SELM.0 .. SELM.1 SELM = 0: Use the DCOCLK
SELM = 1: Use the DCOCLK
SELM = 2: Use the XT2CLK
SELM = 3: Use the LFXT1CLK

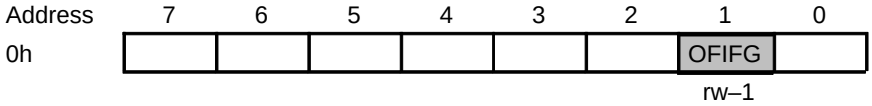
8.7.3 Special Function Register Bits

The basic clock module uses two bits in the special function registers, OFIFG and OFIE. The oscillator fault interrupt enable (OFIE) bit is located in bit 1 of the interrupt enable register IE1. The oscillator fault interrupt flag (OFIFG) bit is located in bit 1 of the interrupt flag register IFG1.

Interrupt Enable IE1



Interrupt Flag Register IFG1



The oscillator fault signal XT_OscFault sets the OFIFG as long as the oscillator fault condition is active. The detection and effect of the oscillator fault condition is described in section 8.4.1. The oscillator fault interrupt requests (if the OFIE bit is set) a non–maskable interrupt. The oscillator interrupt enable bit is reset automatically if a non-maskable interrupt is accepted. The initial state of the OFIE bit is reset and no oscillator fault requests an interrupt even if there is a fault condition.

8.8 Basic Clock Module, Typical Digitally Controlled Oscillator (DCO) Characteristics

The DCO varies with the individual device, the external resistor, the temperature and the supply voltage. Details regarding the electrical characteristics are shown in the data sheet of the device using the Basic Clock Module.