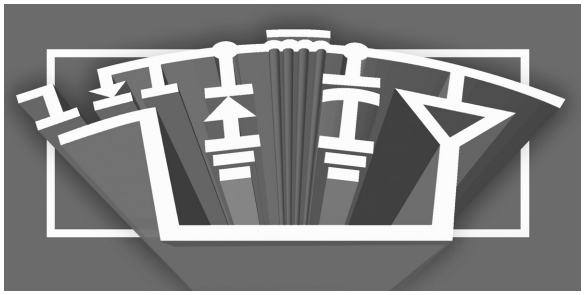

Power Supply Design Seminar

Design Review: 150 Watt Current-Mode Flyback

Topic Categories:
Basic Switching Technology
Specific Power Topologies
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SEM400, Topic 6
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Product Update:
This topic references the UC3842. While this TI device may still be available, the later-generation UCC38C42 may offer performance enhancements.

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Texas Instruments

Design Review: 150 Watt Current-Mode Flyback

Raoji Patel, Dave Reilly, Roger Adair

This paper describes the design of a low cost 150 Watt flyback switching regulated power supply. Output voltage regulation is achieved through the UC3842, a low cost current mode control IC, and the UC3901 isolated feedback generator. The complete schematic is shown in Figure 1.

The adverse effect of flyback transformer leakage inductance on power transfer to the output is discussed in detail.

SPECIFICATIONS:

Switching frequency, f_S:	100 kHz	
Efficiency, η:	80% minimum	
Output Voltages, V_{out}:	+5 V ±1%,	7.5 - 15 A
	+12 V ±3%,	1.5 - 3.0 A
	+24 V ±10%,	.75 - 1.5 A

TOPOLOGY SELECTION:

Current mode control used in this supply provides inherent good line regulation and optimum dynamic response. The two-transistor discontinuous mode flyback circuit shown in Figure 2 is a low cost approach with multiple output capability. Advantages and disadvantages of this topology are:

Discontinuous Mode Flyback - Advantages:

1. Because there are no filter inductors in series with each output (as in buck regulator circuits), all output voltages will track each other within ±5-10% without post-regulation. This minimizes the headroom required and its associated losses in the +12 V linear post-regulator. Dynamic cross-regulation is also very good with this topology.

2. Only one rectifier is required in each output instead of the two required in buck regulator circuits, reducing overall component and assembly costs.

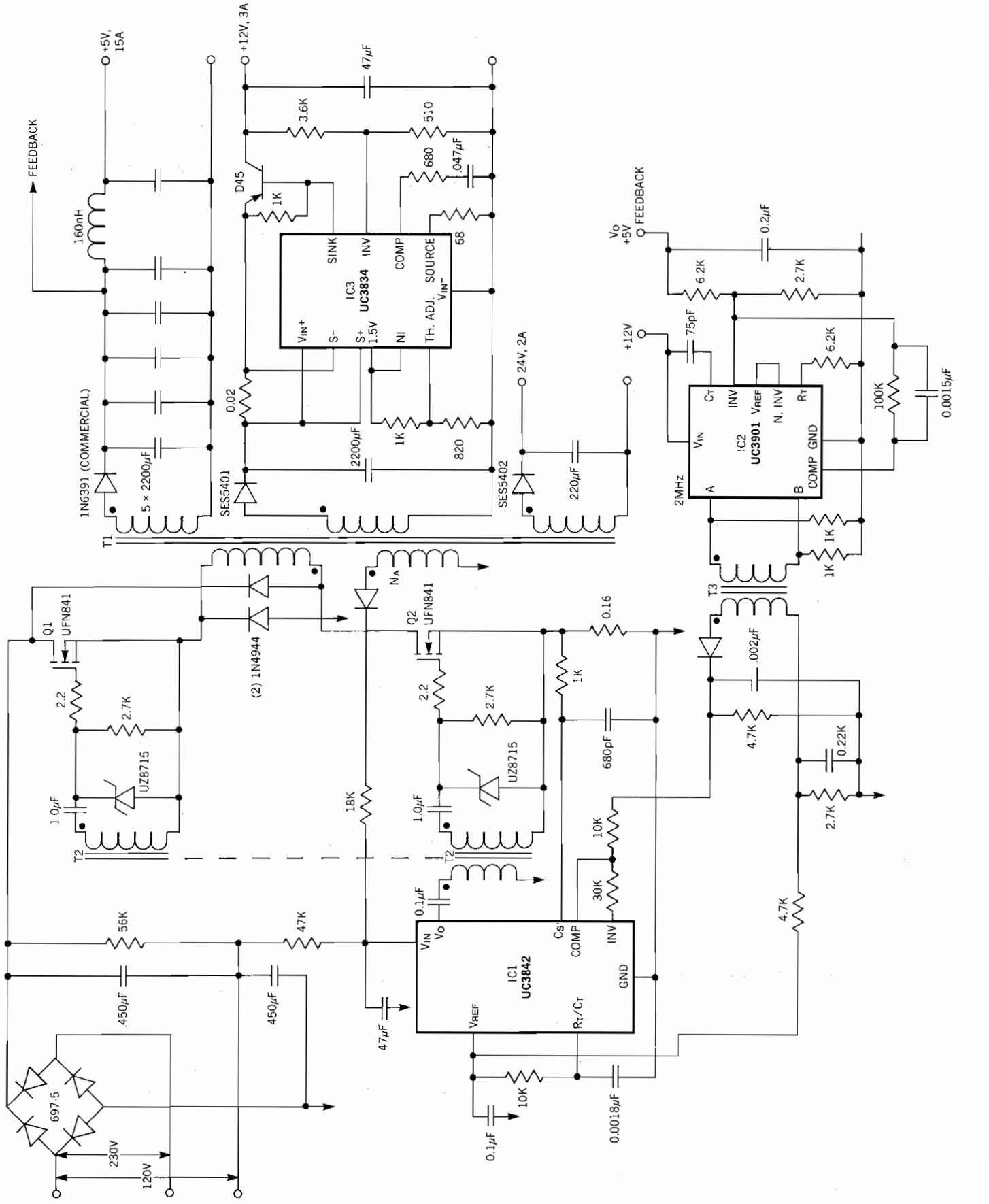
3. Rectifier reverse recovery time is not critical because forward current is zero well before reverse voltage is applied.

4. The flyback transformer used in the discontinuous mode is much smaller because the inductive energy stored is only 1/5 to 1/10 of the energy required in comparable continuous mode circuits.

5. Turn-on circuits are simplified because load current in the power switch is zero during turn-on. There is no concern for turn-on losses or turn-on snubber circuits.

6. Closing the feedback loop is simplified because of the single pole roll-off characteristic of the power circuit.

Figure 1. 150 Watt Flyback Supply -- Complete Schematic



7. Transient response is excellent. The circuit can be designed to correct for large step changes in line or load in little more than one cycle of the switching frequency

8. Conducted EMI is reduced because transistor turn-on occurs with zero collector current. The triangular waveforms of the discontinuous mode contain only the odd harmonics which are attenuated much more rapidly than the even harmonics present in the rectangular waveforms of continuous mode flyback circuits or buck regulators.

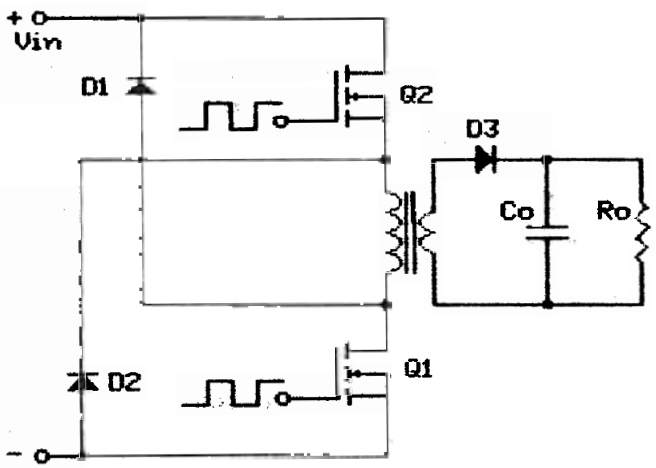


Fig. 2 - Two Transistor Flyback

Discontinuous Mode Flyback - Disadvantages:

1. Switching transistor and rectifier peak currents are nearly two times greater than in the comparable continuous mode circuit. However, the average currents are the same and transistor and diode dissipation is only slightly greater than in the continuous mode.

2. Output filter capacitor ESR and ESL requirements are quite stringent because of the high peak currents encountered in the discontinuous mode. Capacitance values must be nearly twice the comparable continuous mode requirements, and 10-20 times larger than a buck regulator with the same output capability. Nevertheless, transient response is much better because the flyback transformer inductance is so small.

Two-Transistor vs. Single Transistor - Advantages:

1. Voltage rating requirements of MOSFET power switches Q1 and Q2 are half that of a single transistor. This results in much better switching dynamics and much less than half the chip area for the same saturation voltage drop.

2. Cross-coupled diodes D1 and D2 provide a simple non-dissipative way to clamp the voltage backswing caused by T1 leakage inductance. The clamp energy is returned to the bulk input filter capacitor, thus the efficiency is not significantly impaired. Single transistor circuits require an additional transformer winding closely coupled to the primary to obtain non-dissipative clamping, or else the dump the energy (which usually amounts to 15-20% of the output power) into a dissipative snubber circuit.

3. Conducted and radiated EMI is significantly reduced because switching voltages at each end of the transformer move simultaneously in equal and opposite directions. Thus the current spikes that result from charging the stray capacitance to ground (from the wiring, switching transistors and within the transformer) tend to cancel, especially if the capacitance to ground from each end of the transformer is deliberately balanced.

Two-Transistor vs. Single Transistor - Disadvantages:

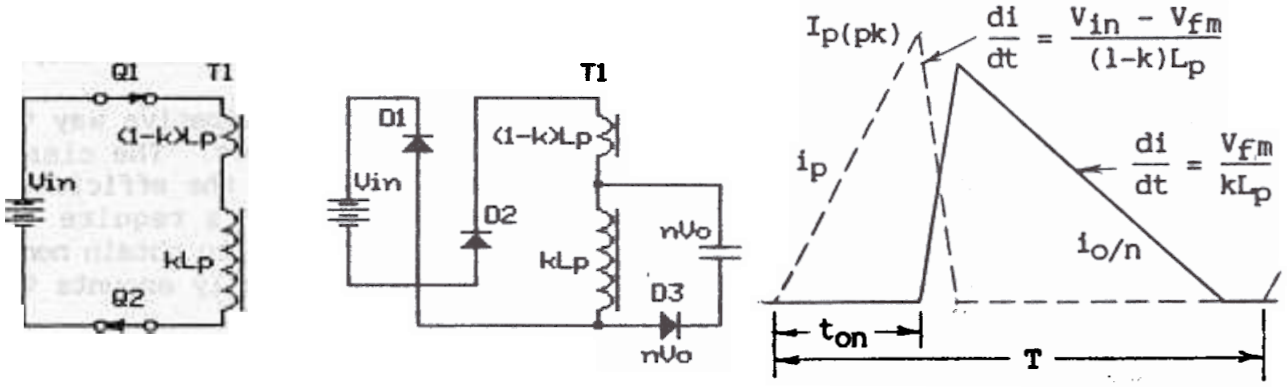
1. Two transistors are required rather than one, but for a 150 watt application, devices are available in the TO-220 package. Because of the lower voltage and smaller size, lower cost can be realized.

2. Requires more complex drive circuit for the upper of the two transistors.

ENERGY TRANSFER IN THE FLYBACK CONVERTER -- LEAKAGE INDUCTANCE EFFECTS

In a flyback converter operated in the discontinuous mode, the energy stored in the flyback transformer (actually an inductor) must be zero at the beginning and end of each switching period. During the "on" time, energy taken from the input is stored in the transformer. When the switching transistors turn off, this stored energy is all delivered somewhere -- mostly to the output. However, the transformer leakage inductance causes much of the stored energy to be dumped into the primary side snubber or clamp, diverting it from the output. The leakage inductance dumps not only its own energy, but also causes much of the energy stored in the mutual inductance to be diverted into the clamp circuit. The amount of energy diverted is typically 15-25% of the total energy stored. In the two-transistor circuit, this diverted energy is returned to the input so the efficiency is not hurt, but peak primary current is greater and the total stored energy in the flyback transformer must be increased.

The amount of energy returned depends upon the transformer turns ratio as well as its leakage inductance. To explain the power transfer process, the simplified equivalent converter circuits during "on" and "off" times are shown in Fig. 3.



3A - "On" time 3B - "Off" time 3C - Current Waveforms

When switches Q1 and Q2 are closed as shown in Figure 3A, energy from the input filter capacitor is transferred to the transformer primary mutual inductance, kL_p, and the leakage inductance, $(1-k)L_p$, where k is the coupling coefficient between primary and secondary. The total energy stored equals $1/2\ LI_p^2$. Energy cannot be transferred to the secondary side at this

time because the output rectifiers are reverse biased.

During the "off" time (see Figure 3B), the current established in the inductor forces the transformer voltage to reverse, or "flyback", until the output rectifier D3 conducts and hopefully transfers the energy stored in the mutual inductance to the output. The current flowing in the leakage inductance causes its voltage to reverse an *additional* amount so that clamp diodes D1 and D2 conduct. This transfers the leakage inductance energy back to the bulk input filter capacitor. Unfortunately, the leakage inductance also causes some of the *mutual* inductance energy to be returned to the input through D1 and D2. This is because whatever current flows in the leakage inductance forces the same current flow on the primary side through the mutual inductance. Thus the leakage inductance delays current transfer to the secondary (see Fig. 3C) and diverts a substantial portion of the mutual inductance energy back to the input. This diversion of energy raises peak primary currents and requires a larger flyback transformer which must store more energy for the same output power. Energy diversion is reduced by making the leakage inductance smaller and by providing a large additional flyback voltage across the leakage inductance so as to reset its current to zero as rapidly as possible.

As shown in Figure 3B and 3C, during the "off" time the output voltage, V_O, and forward rectifier drop, V_f, are reflected across the mutal inductance on the primary side by the transformer turns ratio, $n = N_P/N_S$. The flyback voltage across the mutual inductance is:

(1 $$V_{fm} = n(V_O+V_f)$$

The voltage across the entire primary side inductance L_p is clamped by diodes D1 and D2 to the supply voltage V_{in}. The flyback voltage, $V_{f\ell}$, which resets leakage inductance $(1-k)L_p$ is therefore:

(2) $$V_{f\ell} \quad V_{in} - V_{fm} = V_{in} - n(V_O+V_f)$$

Referring to Fig. 3C, the time required for the current through the primary side leakage inductance to reach zero is proportional to $V_{f\ell}$. This determines how fast the current can transfer to the secondary side and therefore the amount of mutual inductance energy that will be transferred to the output rather than being diverted into the clamp (see Fig. 3C). Equation 3 shows the total flyback transformer energy, W_L, required to make up for losses and for energy diverted back to the input:

(3) $$\frac{W_L}{W_{out}} = \frac{W_L f_s}{P_{out}} = \frac{1-V_{fm}/V_{in}}{\eta(k-V_{fm}/V_{in})}$$

Higher efficiency, η, and better transformer coupling, k, improve the energy transfer and reduce the stored energy required in the transformer. The leakage inductance in a flyback transformer with high voltage insulation is typically 5% of the primary inductance, corresponding to a k of 0.95. A smaller turns ratio decreases V_{fm} which increases reset voltage $V_{f\ell}$ across the leakage inductance, reducing the energy diverted back to the input.

However, the smaller V_{fm} decreases duty ratio D and increases peak primary current, $I_{p(pk)}$, at a given power output:

$$D = \frac{1}{1+kV_{in}/V_{fm}} \qquad (4)$$

D_{max} occurs at min V_{in}

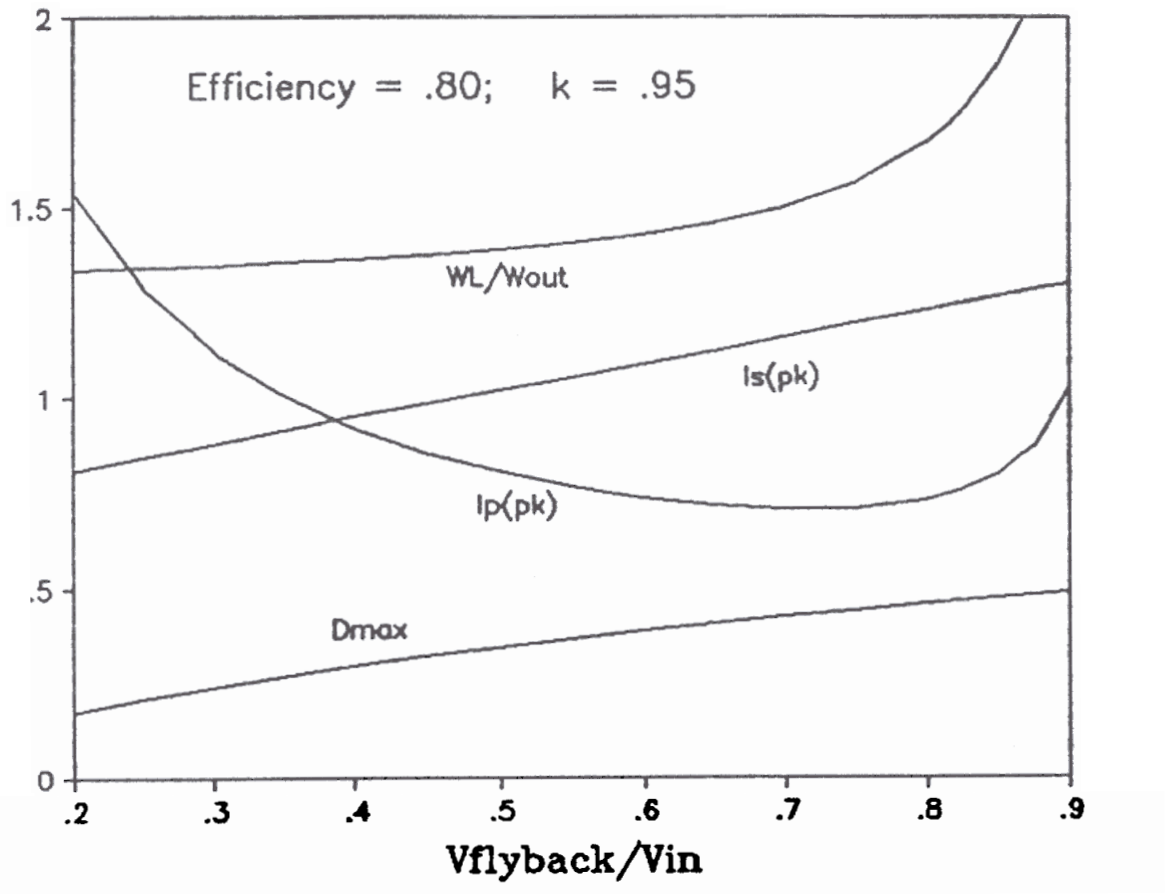
$$I_{p(pk)} = \frac{2\ W_L\ f_s}{V_{in}\ D} \qquad (5)$$

On the other hand, smaller V_{fm} *reduces* peak currents on the secondary side, $I_{s(pk)}$:

$$I_{s(pk)} = \frac{2\ I_{out}}{(1-D)} \qquad (6)$$

Figure 4 shows the values calculated from Equations 3 - 6: W_L/W_{out}, D_{max}, $I_{p(pk)}$, and $I_{s(pk)}$, plotted against the ratio V_{fm}/V_{in}. Note that $i_{p(pk)}$ and $I_{s(pk)}$ are calculated at minimum V_{in} and maximum P_{out} values and are plotted on a *relative* basis. These curves suggest that a good design compromise is to use a transformer turns ratio such that $n(V_{out}+V_f) = V_{fm}$ is approximately 1/2 of the worst case minimum V_{in} at low line voltage. The energy transfer process will be more efficient at line voltages above the minimum because V_{fm} remains constant but reset voltage $V_{f\ell}$ across the leakage inductance becomes larger.

Figure 4. Peak Current and Energy Requirements vs. Clamp Ratio.



DESIGNING THE INPUT RECTIFIER AND FILTER

Refer to Design Reference Section I1, "Line Input AC to DC Conversion and Input Filter Capacitor Selection". The input circuit may be connected as a voltage doubler from the 120 V line or as a full-wave bridge from the 230 V line. In either case the input bulk filter capacitors must store enough energy to provide 200 Vdc minimum to the switching converter during the milliseconds that the instantanteous AC line voltage is below 200 V.

Section I1, Table I shows that for a 100 Watt input supply in the worst case doubler configuration, two 160 µF capacitors maintain the required 200 V at mimimum RMS line voltage. The full load input power required for 150 Watt output is 150/η, or 187.5 Watts. This requires 160x187.5/100, or 300 µF for each voltage doubler capacitor. Considering tolerances and temperature coefficients of aluminum electrolytic capacitors, 450µF is used. Peak repetitive charging current from Table I is 3.28x187.5/100 = 6.15 A. RMS charging current is 1.126x187.5/100 = 2.11 A.

DESIGN OF THE POWER INVERTER

Table A below shows the winding turns definition that comes reasonably close to achieving the desired output voltages and the desired 100 V primary side flyback voltage (approximately 1/2 of the 200 V minimum V_{in}):

TABLE A:	Winding	Turns	Vfm	$V_{out}+V_f$	V_f	V_{out}
	Primary	36	100.8			
	5 V, 15A	2		5.6	0.6	5.0
	12 V, 3A	5		14.0	1.0	13.0
	24 V,1.5A	9		25.2	1.0	24.2
	16 V Aux.	6		16.8	.8	16.0

The 16 V Auxiliary output provides power for the control and gate drive circuits. It is not closely coupled to the other secondaries because it is on the primary side of the isolation boundary, so its load regulation is an acceptable 20%. The 12 volt secondary provides 13 V, allowing 1 Volt of headroom for the linear post-regulator which achieves 3% regulation.

During the flyback time all windings will have 2.8 Volts per turn. The turns ratios between secondaries are critical because they determine the output voltage ratios. Each winding must have an integral number of turns, making it impossible to use fewer secondary turns than Table A without hurting the output voltage ratios. The number of primary turns is not as critical because flyback voltage V_{fm} is not rigidly defined. Obviously the number of turns could be any integral number times the values given above.

The total maximum energy storage, W_L, required in the primary inductance of the flyback transformer at full load output and minimum V_{in} is:

$$(3R) \quad \frac{W_L}{W_{out}} = \frac{W_L f_s}{P_{out}} = \frac{1-V_{fm}/V_{in}}{\eta(k-V_{fm}/V_{in})} = \frac{1-100/200}{0.8(.95-100/200)} = 1.3889$$

$$W_L = 1.3889 \times P_{out}/f_s = 1.3889 \times 150/100{,}000 = 2083\ \mu J$$

From Equation 4, the maximum duty ratio and t_{on} at min. V_{in} are calculated:

$$(4R) \qquad D_{max} = \frac{1}{1+kV_{in}/V_{fm}} = \frac{1}{1+.95x200/100} = .3448$$

$$\max t_{on} = DT = D/f_s = .3448/100{,}000 = 3.448\ \mu sec$$

The maximum peak primary current is, from Equation 5:

$$(5R) \qquad I_{p(pk)} = \frac{2\ W_L\ f_s}{V_{in}\ D} = \frac{2x2083x0.1}{200x0.3448} = 6.04\ A$$

The primary current limit need not exceed 6.04 A because it represents a combination of worst case conditions that are not likely to coexist. For example, with minimum V_{in} slightly larger than 200 V (because the bulk filter capacitors are larger than required), less energy is returned to the source, so that less inductor energy and less $I_{p(pk)}$ is required for full load output.

The total primary inductance required is:

$$(7) \qquad L_p = 2\ W_L/I_{p(pk)}^2 = 2x2083/6.04^2 = 114.2\ \mu H$$

Transformer Design: Design Reference Section M6, "Filter Inductor and Flyback Transformer Design for Switching Power Supplies", defines the approach and the equations used. An EC41 core is chosen based on operating frequency, maximum flux density and hot spot temperature rise limitations.

At 100 kHz operating frequency, the maximum flux density, B_{max}, is limited by core losses, not magnetic saturation. The EC41 core has an effective thermal resistance of 16.5°C/W to the centerpost hot spot. An acceptable hot spot temperature rise of 33°C allows 2 Watts total dissipation -- 1 Watt winding and 1 Watt core losses. Since the EC41 core volume is 11 cm^3, 1 Watt total core loss equals .091 W/cm^3. This occurs with a flux density swing of 0.155 Tesla (1550 Gauss) at 100 kHz, from the core loss data in Design Reference Section M3. Flux remnance is nearly zero at the beginning of each switching period because of the air gap used to store energy in the flyback transformer. Therefore the 0.155 Tesla flux density swing results in B_{max} of 0.155 T for normal conditions at full load. Under the temporary conditions requiring maximum stored energy at V_{in} = 200 V, B_{max} is allowed to reach 0.17 Tesla.

The *minimum* number of primary turns, N_p, needed to store the worst case energy requirement at minimum V_{in} without exceeding 0.17 T flux density is:

$$(8) \qquad N_{p(min)} = \frac{L_p\ I_{max}}{B_{max}\ A_e} = \frac{114x10^{-6}x6.04}{0.17x1.25x10^{-4}} = 32.4\ ; \quad N_p = 36\ turns$$

Referring back to Table I, N_p must be 36 turns or an integer multiple such as 72 or 108. The 32.4 turns defined in Eq. 8 is the *minimum* N_p, so 36 turns is the obvious choice. This will require a slightly larger gap to obtain the desired inductance. The flux swing and core losses will be less than would be obtained with $N_{p(min)}$, but winding losses will be greater.

The actual flux swing can be recalculated from Eq. 8, plugging in 36 turns and solving for B_{max} = 0.153 Tesla. In this case, N_p is not much more than $N_{p(min)}$ and there will be little increase in total transformer dissipation and temperature rise. If N_p had to be much larger than $N_{p(min)}$, winding losses would be much higher and might force the use of a larger core size.

The core center-post is ground to the desired gap length calculated by the classic inductance formula, using the actual N_p of 36 turns:

(9) $\ell_g = \mu_0 N^2 A_e / L_p = 4\pi x10^{-7} x36^2 x1.25x10^{-4} / 114x10^{-6} = .00178 \text{ m} = .178 \text{ cm}$

The required gap can also be obtained without grinding the center-post by spacing the core halves apart by one-half the total gap. This puts half the gap in the center-post and half in the outer legs of the core (provided the combined area of the outer legs is the same as the center-post area). Using this method, considerable magnetic field is propagated outside the core, and EMI problems may be worsened.

Designing the Windings: AC eddy current losses (skin effect and proximity effect) will be very significant in the 100 kHz flyback transformer unless the windings are designed specifically to minimize these effects. The skin or penetration depth, Δ = .024 cm at 100 kHz, so even a single layer of AWG 24 starts to incur AC losses. Another major concern is to minimize the leakage inductance between primary and secondaries, in spite of the high voltage isolation requirements which force them to be physically separated. Good coupling between secondaries is easier to achieve because they may be co-mingled or even wound multifilar.

First, the 36 turn primary winding is split into two 18 turn portions. The secondaries are in a single closely coupled group. One primary portion is wound around the center post inside of the grouped secondaries, the other primary portion is wound on top of the secondaries. This interleaving results in a dramatic reduction of the magnetic field (energy) between the windings. Leakage inductance between primary and secondary, $L_p(1-k)$, is reduced by a factor of 3, and there is a similar beneficial effect in reducing eddy current losses in both primary and secondaries.

Second, windings are made up of many paralleled wires with diameters less than 2 times the penetration depth, Δ, so that AC current is not excluded from the central portions of the conductors. Thin copper strip may also be used for the same purpose in low voltage, high current windings.

The total cross-section area of all windings is limited by the core window area, A_W = 2.15 cm² for the EC41 core. Much of the window area is wasted, taken up by insulation around wires, voids between round wires, insulation between winding portions, and necessary creepage distance at the ends of the windings. Window utilization factor, k_u = 0.4 is the fraction of the window area that is actual conductor. All windings in the flyback transformer are single ended, so that winding losses are minimized by apportioning equal winding cross-section areas to the primary and to the group of secondaries, hence primary area factor, k_p = 0.5. The maximum primary conductor area available is:

(10) $A_p = A_w \cdot k_u \cdot k_p = 2.15x0.4x0.5 = 0.43 \text{ cm}^2$

The average length of each turn around the core is ℓ_t = 6 cm (otherwise known as MLT -- mean length per turn). The total length of the entire 36 turn primary is then 6x26 = 216 cm. The RMS primary current, I_p, is:

$$(11) \qquad I_p = I_{p(pk)} \cdot (D_{max}/3)^{1/2} = 6.04x(.345/3)^{1/2} = 2.05 \text{ A}$$

Total power dissipation allowed in all windings is 1 Watt, so the primary may dissipate 0.5 watts. The maximum resistance of the primary winding is therefore:

$$R_p = P_p/I_p^2 = 0.5/2.05^2 = 0.119 \text{ Ohms}$$

$$R_p/cm = 0.119/216 = .000551 \text{ Ohms/cm}$$

AWG 21 copper wire comes close to this with .000561 Ohms/cm at 100°C. But a single layer (after interleaving) of AWG 21 at 100 kHz has an AC resistance factor, $F_R = R_{ac}/R_{dc}$ of 2.45, which more than doubles the loss.

An acceptable F_R value of 1.4 is obtained by using 7 AWG 29 wires paralleled in place of a single AWG 21 wire. The 7 wires are twisted together into a 7-strand cable, or Litz wire, with 6 outer strands packed in a hexagonal pattern about the 7th central strand. The DC resistance of the paralleled strands is .000512 Ohms/cm, less than a single AWG 21 conductor. The 36 turn primary is wound with 18 turns of the seven strand cable inside the secondaries and 18 turns top of (outside) the secondaries. The breadth of the winding window in the EC41 core is 2.78 cm. The 18 turns of 7-strand cable will occupy the central 1.75 cm of the window, leaving plenty of creepage distance.

Peak and rms secondary currents are proportional to the DC output currents as follows. The results of these calculations are given in Table B below:

$$I_{s(pk)} = 2 \cdot I_{out}/(1-D_{max}) = 3.05 \cdot I_{out}$$

$$I_s = I_{s(pk)} \cdot ((1-D_{max})/3)^{1/2} = .467 \cdot I_{s(pk)}$$

The conductor area for each winding is proportioned to operate at the same rms current density as the primary. The results are shown in Table B.

TABLE B WINDING DATA

Winding	$I_{s(pk)}$	Irms	Area(cm^2)	Configuration
Primary		2.05	.0041	18+18 turns, 7xAWG29
5V, 15A	45.75	21.36	.0429	2 turns, .025x1.75 cm strip
12V, 3A	9.15	4.27	.0086	5 turns, 2 - 7xAWG29 paralleled
24V,1.5A	4.58	2.14	.0043	9 turns, 7xAWG29
16V Aux	.21	.05	.0001	6 turns, AWG 29

Three layers of 1 mil mylar tape (.016 cm - 6.6 mil incl. adhesive) are used to meet VDE 3750 V isolation requirements, applied between the two primary halves and the secondary bundle.

Copper strip is used for the two turn 5 Volt secondary. The thickness of the strip is comparable to the skin depth, Δ, so that F_R is only slightly

greater than 1.0

Note that the same 7-strand AWG29 cable is used for the primary and the 12 and 24 Volt secondaries. The 12 and 24 Volt windings are mingled in a single layer as follows: Four lengths of cable -- A, B, C, and D are wound simultaneously side by side for 5 turns. This results in a single smooth layer 20 cable diameters wide across the winding breadth, in the sequence A,B,C,D,A,B,C,D,A....etc. A and C are paralleled for the 5 turn 12 Volt output. One turn is taken off D, leaving a total of 19 cable diameters across the winding. The 5 turns of B are put in series with the 4 turns left in D for the 9 turn 24 Volt output.

The 16 Volt auxiliary windings are put on last, spread over the outer half primary. The auxiliary winding must be separated from the other secondaries because of the line isolation requirements.

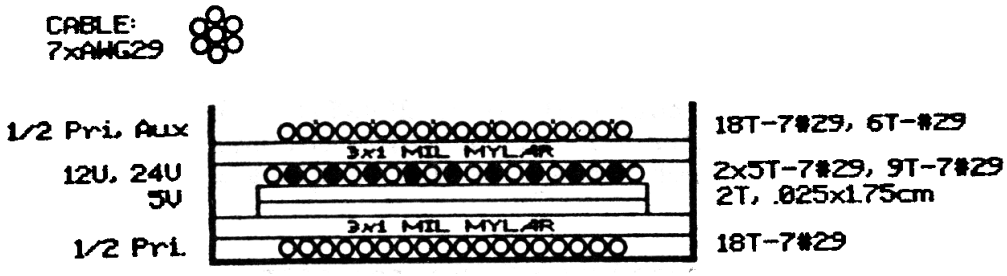


Figure 5. Transformer Winding Layout

Output Filter Capacitors: Aluminum electolytic capacitors have the lowest cost and are therefore most widely used in commercial/industrial supplies. Filter capacitor selection is dominated entirely by the ESR (Equivalent Series Resistance) necessary to obtain acceptable peak-peak ripple voltage.

$$ESR_{max} = V_{ripple}/I_{s(pk)}$$

Table C shows the parameters and results of the capacitor selection process:

TABLE C -- OUTPUT FILTER CAPACITORS

Output	V_{ripple}	$I_{s(pk)}$	ESR_{max}	Capacitor Selection
5V, 15A	0.3	45.75	.0066	(5) 2200 µF, 16 V, Panasonic HF
12V, 3A	0.3	9.15	.033	(1) 2200 µF, 16 V, "
24V,1.5A	0.5	4.58	.11	(1) 220 µF, 50 V, "
16V Aux	0.3	.21	1.42	(1) 47 µF, 25 V, "

The 5 Volt output ripple voltage is further reduced to below 0.1 V by the additional L-C filter section (actually L-R because of ESR). The 160 nH inductor is 0.1 Ω at 100 kHz, and the additional 2200 µF capacitor has an ESR of .03 Ω, for a ripple reduction factor of 3.3.

CONTROL AND GATE DRIVE CIRCUITS:

The auxiliary supply provides an average current of 50 mA to power the UC3842 control IC and power MOSFET gate drive circuits. The auxiliary supply is maintained from the 7 turn auxiliary winding on T1 through an 18 Ω resistor which limits the peak charging current and prevents the supply from charging to the high peak voltage of the leakage inductance spike.

During initial startup of the supply, the UC3842 undervoltage lockout disables the control and drive circuits so that the total current drawn is less than 1 mA. This enables the 47K resistor from the input bulk filter to initially charge the auxiliary supply capacitor to 16 volts, where the circuit comes alive and starts the converter. It takes 200 - 300 switching periods for the output voltages and the T1 auxiliary winding voltage to rise to normal levels and recharge the aux supply capacitor, so the capacitor must be large enough to supply 50 mA for 300x10μs without dropping below 11 Volts (where the UC3842 turns off).

The totem pole output of the UC3842 drives the gates of the two MOSFETs through transformer T2, consisting of three 20 turn windings of AWG 30 wire on a 1/2 inch O.D. ferrite toriodal core, 204XT250, 3E2A material. The three wires are wound together (trifilar). High voltage insulation between primary and secondaries is not needed, as all windings are on the same side of the isolation boundary.

Primary current in T1 is sensed by a 0.16 Ω resistor. This current sense voltage is applied through a spike filter to the current sense terminal of the UC1840, where it is compared against the amplified output error voltage. The comparator input voltage is clamped to 1 V, which effectively limits the peak primary current to 1/0.16 = 6.25 A and indirectly limits the duty ratio. The error amplifier output (pin 1 - Compensation) must swing from 1 to 4.5 Volts in order to swing the comparator input from 0 to 1 Volt for full range control of the current. This is because there are two forward diode offsets and a 3 to 1 divider between the error amplifier output and the comparator input within the IC.

The 30K feedback resistor and 10K input resistor together establish an error amplifier gain of 3. Combining this with the 3/1 divider at output of the error amplifier results in an overall gain of 1 from the input of the 10K resistor to the current control comparator. The inverting input of the error amplifier normally sits at 2.5 V. This makes it necessary to provide +1.8 V bias to the input demodulator so that the input will swing from 1.8 to 3.0 V in order to swing the output full range from 4.5 to 1 V.

A UC3901 isolated feedback generator compares the 5 volt output against an internal reference, amplifies the resulting error and uses it to amplitude modulate a 2 mHz carrier. This signal is easily coupled through a tiny isolation transformer T3 back to the primary side where it is demodulated and the error voltage recovered and applied to the UC3842 error amplifier input. Transformer T3 has two 15 turn, AWG 30 windings on the same 1/2" O.D. epoxy coated ferrite toriodal core (204XT250, 3E2A material) used for T2. These windings must be wound individually on opposite sides of the core to provide 3750 Volt isolation. Although the coupling is hurt because the windings are not distributed uniformly around the entire core, leakage inductance in this application is not critical.

CLOSING THE FEEDBACK LOOP:

The 5 Volt output has the most critical regulation requirement. and is used as the basis for closed loop control. The 12 Volt output uses a simple linear post-regulation technique to achieve better than 3% regulation. The 24 Volt output achieves better than 10% line and load regulation by simply tracking the 5 Volt output without additional post-regulation.

The feedback loop design approach is taken from Design Reference Section C1 - "Closing the Feedback Loop". The Bode plot of Figure 6 shows the overall loop gain and phase, along with its two major components -- the control to output gain and the feedback circuit gain.

The overall loop gain Bode plot shows the 0 dB crossover frequency to be 8.4 kHz. The solid lines show the gain and phase with maximum filter capacitor ESR. Minimum ESR, shown in the dash lines, is assumed to be 1/5 of the maximum. The worst case phase shift of 135 degrees which occurs with minimum ESR provides an adaquate phase margin of 45 degrees. The gain of 333 (50 dB) below 60 Hz is sufficient that a .015 Volt error on the 5 Volt output swings the output over its full range, which is much better than the 1% regulation required.

The control to output portion of the loop gain includes the current control comparater and pulse width modulator in the UC3842, the power switching circuit, flyback transformer and filter. The formulae from which the plots were calculated are from Design Reference Section C1, Appendix C, pages 5 and 6. These equations give no consideration to the power transformer turns ratio, so the control to output gain must be multiplied by n = 36/2. (These equations apply to current mode control, and the current is stepped up.)

Before beginning the calculations, the primary inductance, filter capacitance and load resistance values are all referred into the 5 Volt output according to their respective turns ratios squared:

$$C' = 2200x6 + 2200x(5/2)^2 + 220x(9/2)^2 \quad 31400\ \mu F$$

$$ESR' = .03x2200/31400 = .002\ \Omega \text{ max}, \quad .002/5 = .0004\ \Omega \text{ min}$$

$$R_O' = V_O^2/P_O = 5^2/150 = .1667\ \Omega \text{ min}; \quad = 5^2/75 = .333\ \Omega \text{ max}$$

$$L' = L_p/n^2 = 114.2/(36/2)^2 = 0.352\ \mu H$$

$$k = I_{p(pk)}/\text{max}V_C = 6/1 = 6 \quad (6A \text{ controlled by } 1V \text{ comparator swing})$$

Below 60 Hz, the control to output gain at full load is 14 dB:

$$(14) \quad v_O/v_C = nK(R_O'L'f/2)^{1/2} = 18x6x(.1667x.352x0.1/2)^{1/2} = 5.85$$

Considering losses, actual gain will be slightly less -- assume gain of 5, or 14 dB. The gain rolls off above 60 Hz with a single pole characteristic (-20 dB/decade with -90° phase shift). This pole frequency is determined by output filter capacitance and load resistance:

$$(15) \quad f_p = 2/(2\pi RoC) = 2/(2\pi x.1667x.0314) = 60.8\ Hz$$

At 2400 Hz, a zero is encountered attributable to the maximum ESR of the filter capacitor. This zero cancels the pole, flattening out the gain and bringing the phase lag gradually back to zero.

(16) $f_Z = 1/(2\pi x ESR x C)$ $\quad 1/(2\pi x.002x.0314) = 2413$ Hz (ESR max)
$\quad 1/(2\pi x.0004x.0314) = 12670$ Hz (ESR min)

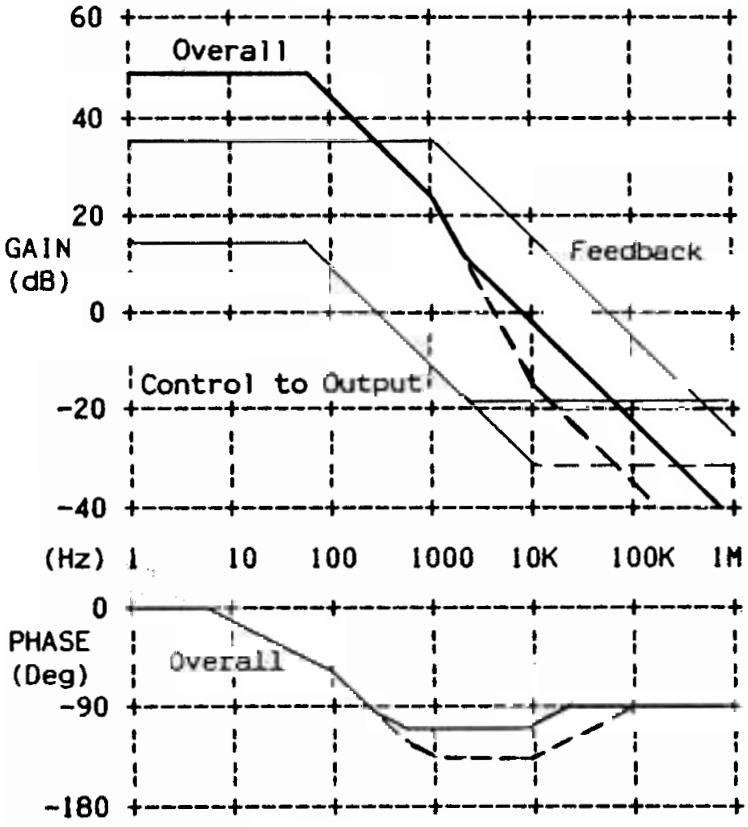


Figure 6. Loop Gain Bode Plot

Stability considerations dictate that the overall loop gain must cross 0 dB below 1/4 or 1/5 of the switching frequency. In designing the gain of the feedback circuits, it is necessary to add a pole to compensate (cancel) the ESR zero, otherwise the ESR zero would cause the overall loop gain to flatten out and not cross 0 dB as required. If the compensating pole is put exactly at the ESR zero frequency, the overall loop gain will have a single pole -20 dB/decade slope with -90' phase shift from 60 Hz to well above 100 kHz. The phase margin would be 90', which is much more than necessary. The overall low frequency loop gain can be increased by putting the compensating pole *below* the ESR zero frequency. This results in a 2 pole slope between the compensating pole and the ESR zero, increasing phase shift and reducing phase margin. A pole frequency of 1 kHz is used in this design, which reduces the phase margin to 45' with the worst case *minimum* ESR.

The control to output gain at 20 kHz is -18 dB. To set the crossover frequency at 20 kHz ($f_S/5$) requires +18 dB feedback circuit gain. However, this causes another problem: With feedback circuit gain of +18 db at 20 kHz, decreasing 20 dB/decade as it must to compensate the ESR zero, the feedback gain is 4 dB at the 100 kHz switching frequency. There is nearly 0.3 V of switching frequency ripple at the 5 Volt output where it is sampled

for feedback control. The 0.3 Volts ripple will be amplified 4 dB to 0.48 Volts by the feedback circuit and applied to the current sense comparator in the UC3842 along with the amplified output error voltage. The sawtooth waveform representing primary current at the other input of the comparator is a *maximum* 1 Volt amplitude at full load, and 0.5 Volts at 1/4 load. The 0.48 Volts of 100 kHz ripple will cause erratic behavior of the modulator at moderate load levels. Solving this problem requires lower feedback circuit gain at 100 kHz, which lowers the gain at all frequencies and reduces the crossover frequency. In this application, 0.2 Volts ripple amplitude at the current sense comparator input is acceptable, which dictates a feedback circuit gain of 2/3, or .667 (-3.5 dB) at 100 kHz. Thus the gain is 7.5 dB (2.37) less than originally attempted, and the crossover frequency is 2.37 less, or 8.4 kHz. With a gain of .667 at 100 kHz, the feedback circuit gain at the pole frequency, 1 kHz, is .667x100K/1K = 66.7 (36 dB).

As stated earlier, the gain from the demodulator at the input of the UC3842 to the input of the current sense comparator is 1 (0 dB), to well above 100 kHz. The AC gain through the coupling transformer and demodulator is also 1. The gain of the driver section of the UC3901 isolated feedback generator is fixed at 4. The 100K feedback resistor around the UC3901 error amplifier together with the 6.2K input resistor to provides a gain of 16.5, for a total gain of 16.5x4 = 66, as required. the .0015 µF across the 100K resistor establishes the 1 kHz pole frequency.

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