Topic 3 Presentation:

Designing an LLC Resonant Half-Bridge Power Converter

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Topic 3

Designing an LLC Resonant Half-Bridge Power Converter

Hong Huang
Agenda

1. Introduction
   – Brief review
   – Advantages

2. Design Prerequisites
   – Configuration
   – Operation
   – Modeling
   – Voltage gain function

3. Design Considerations
   – Voltage gain and switching frequency
   – Line and load regulation
   – Zero voltage switching (ZVS)
   – Steps for designing and a design example

4. Conclusions
Introduction

• Brief review of resonant converters
  – Series resonant converter (SRC)
  – Parallel resonant converter (PRC)

- Single resonant frequency
- Circuit frequency increases with lighter load

- Resonant point changes with load
- Large amount of circulating current
Introduction

• Brief review of resonant converters
  – Combination of SRC and PRC $\rightarrow$ LCC
    • Two resonant frequencies
    • Requires three elements
  – LLC: alternative LCC
    • $L_r$ and $L_m$ integrated in a transformer

• Advantages of LLC
  – High efficiency (ZVS)
  – Less frequency variation and lower circulating current
  – ZVS over operating range

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Design Prerequisites

- **Configuration**
  - Variable-frequency square-wave generator
  - Divider formed by resonant network and $R_L$
  - Rectifier to get DC output
  - Changing frequency varies voltage across $R_L$
  - Frequency-modulated converter instead of PWM
Design Prerequisites

- Operation
  - $f_{sw}$ switching frequency
  - $f_0$ series resonant frequency ($C_r$ and $L_r$)
  - $f_{co}$ circuit resonant frequency ($C_r$, $L_r$, and $L_m$, together $R_L$)

\[
\begin{align*}
  f_{sw} &= f_0 \\
  f_{sw} &< f_0 \\
  f_{sw} &> f_0
\end{align*}
\]
Design Prerequisites

• Modeling
  – First harmonic approximation (FHA)

(a) (b)

• Input and output: Square wave voltages
• Sinusoidal current in resonant circuit

• Input and output: Fundamental components to approximate FHA
• Rectifier and $R_L$ equivalent to $R_e$
• AC circuit method can be used
Design Prerequisites

- Voltage gain function
  - Expression from impedance divider

\[ M_{g\_DC} = \frac{n \times V_o}{V_{in}/2} \approx M_{g\_sw} = \frac{V_{so}}{V_{sq}} \approx M_{g\_ac} = \frac{V_{oe}}{V_{ge}} \]

\[ M_{g\_DC} = \frac{n \times V_o}{V_{in}/2} \approx \frac{V_{oe}}{V_{ge}} \]

\[ = \left| \frac{(j\omega L_m) \parallel R_e}{(j\omega L_m) \parallel R_e + j\omega L_r + \frac{1}{j\omega C_r}} \right| \]

where \( \omega = 2\pi f = 2\pi f_{sw} \) and \( j = \sqrt{-1} \)
Design Prerequisites

- Voltage gain function
  - Expression (Normalization)

\[ M_{g\_DC} = \frac{n \times V_o}{V_{in}/2} \approx M_{g\_sw} = \frac{V_{so}}{V_{sq}} \approx M_{g\_ac} = \frac{V_{oe}}{V_{ge}} \]

\[ M_g = \left| \frac{L_n \times f_n^2}{[(L_n + 1) \times f_n^2 - 1] + j[(f_n^2 - 1) \times f_n \times Q_e \times L_n]} \right| \]

<table>
<thead>
<tr>
<th>Normalized Gain</th>
<th>Resonant Frequency</th>
<th>Quality Factor</th>
<th>Normalized Frequency</th>
<th>Inductor Ratio</th>
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<td>( M_g = \frac{V_o}{V_{in}/2} )</td>
<td>( f_0 = \frac{1}{2\pi \sqrt{L_r/C_r}} )</td>
<td>( Q_e = \frac{\sqrt{L_r/C_r}}{R_e} )</td>
<td>( f_n = \frac{f_{sw}}{f_0} )</td>
<td>( L_n = \frac{L_m}{L_r} )</td>
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Eq. Load R.

\[ R_e = \frac{8 \times n^2}{\pi^2} \times R_L \]
Design Prerequisites

- Voltage gain function
  - Plots of gain magnitude, fixed $L_n = 5$
  - $Q_e$ (load current) increases $\Rightarrow$ peak gain decreases $\Rightarrow$ curves shrink

![Gain vs Normalized Frequency Graph]

$Q_e = 0.5$
$Q_e = 0.1$
$Q_e = 10$

$G_{m_{pk}}$

$M_{g_{pk}}$
Design Prerequisites

- Voltage gain function
  - Plots of gain magnitude, fixed $Q_e = 0.5$
  - $L_n$ decreases $\Rightarrow$ peak gain increases $\Rightarrow$ ZVS obtained but conduction losses increase

![Graph showing gain vs normalized frequency with different $L_n$ values](image)

- $L_n = 10$
- $L_n = 5$
- $L_n = 3$

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Design Considerations

- Where to base a design?
  - In the vicinity of series resonance, \( f_n = 1 \Rightarrow \) narrowest frequency variation
    \( \Rightarrow M_g \) able to = 1, >1, and <1
  - Right side of the resonant peak \( \Rightarrow \) ZVS requirement
Design Considerations

- Line and load regulation
  - Properly set up $M_{g_{\text{max}}}$ and $M_{g_{\text{min}}}$
  - Frequency limit set up

\[
Q_e = \begin{cases} 
0 & \text{at no load} \\
\text{max at full load} & \text{at full load} \\
\text{max} & \text{at max load}
\end{cases}
\]

\[
M_{g_{\text{max}}} = \frac{n \times V_{o_{\text{max}}}}{V_{\text{in_{min}}}/2}
\]

\[
M_{g_{\text{min}}} = \frac{n \times V_{o_{\text{min}}}}{V_{\text{in_{max}}}/2}
\]
Design Considerations

- Overload current operation
  - \( Q_e = \text{max} \) to include and meet the required \( M_{g_{\text{max}}} \)
  - Operation still on the right side of resonant peak
Design Considerations

- Load short circuit
- Protection options
  - Increase $f_{sw}$ rapidly to reduce $M_g$ to zero
  - Operation with $f_n > 1$, i.e., $f_{sw} > f_0$ at all times
  - Independent protection function
Design Considerations

• Zero voltage switching (ZVS)
  – How ZVS is achieved?

Vg \_ Q1
Vg \_ Q2

Q1 Turns Off
Q2 Turns On

V_{ds\_Q2} = 0

I_r
I_m

C_{DS1}
C_{DS2}

L_r
L_m

V_{sq}

n:1:1

C_{r\_j}

V_{g\_Q1}
V_{g\_Q2}

V_{in}
Design Considerations

• Zero voltage switching (ZVS)
  – **Necessary** condition
    • Input impedance of the resonant network → *inductive*
    • Operation on the right side of the resonant peak
  – **Sufficient** condition
    • Enough energy stored in the magnetic field, mainly $L_m$
    • Enough time to discharge the capacitors, mainly $C_{DS}$
Design Considerations

• Why not design on the left side of the resonant peak?
  – Capacitive current results
  – ZVS lost
    → Hard switching
    → Switching losses increase
  – Body diode reverse recovery losses
    → Primary MOSFET failure
  – Higher EMI noise
  – Reversed frequency relationship to feedback loop
Design Considerations

• Design Steps – How to initially select?
  
  – $f_{sw}$, switching frequency
  
  – $n$, transformer turns ratio
  
  – $L_n$, inductance ratio
  
  – $Q_e$, series resonant quality factor
Design Considerations

• Design Steps – Switching frequency
  – Usually selected for particular applications
    • Example in off-line applications: Typical below 150 kHz
  – Selecting the switching frequency
    • f decrease ⇒ Bulkier converter
    • f decrease ⇒ Switching losses decrease ⇒ ZVS benefit decrease
    • f increase ⇒ ZVS benefits increase vs. hard switching converters
  • Very High f :
    – Component availability
    – Additional switching losses
    – Additional concerns due to parasitic effects
Design Considerations

• Design Steps – Transformer turns ratio, n
  – Voltage gain can be larger and smaller than unity
  – Flexibility in selecting the turns ratio, n
  – Turns ratio design with $M_g = 1, initially$, and nominal $V_{in}$ and $V_o$

\[ n = M_g \times \frac{V_{in}/2}{V_o} = \frac{V_{in\_nom}/2}{V_{o\_nom}} \quad \left| M_g = 1 \right. \]
Design Considerations

- **Design Steps –** $L_n$ and $Q_e$
  - $L_n$ and $Q_e$ to achieve $M_{g_{pk}} > M_{g_{max}}$ for maximum load
  - Select $L_n$ and $Q_e$ from pre-plotted peak gain curves
  - Initial selection
    - $L_n = 5$
    - $Q_e = 0.5$
  - Example: Select $L_n$ and $Q_e$ for $M_{g_{max}} = 1.2$
  - To achieve design margin – Final selection
    - $L_n = 3.5$, $Q_e = 0.45$
    - 30% margin over

![Diagram showing attainable peak gain curves and selection](image)
Design Considerations

• Design Steps – Trade-offs to select $L_n$ and $Q_e$
  – Different requirements for different applications
  – Fixed $Q_e$, $L_n$ decrease $\Rightarrow$ peak gain increase $\Rightarrow$ good for ZVS and avoids capacitive current
  – But, $L_n$ decrease $\Rightarrow$ $L_m$ decrease $\Rightarrow$ conduction losses increase
  – Fixed $L_n$, $Q_e$ decrease $\Rightarrow$ peak gain increase $\Rightarrow$ frequency variation increase
  – Recommend starting with $L_n = 5$, and $Q_e = 0.5$ (from design practice)
Design Considerations

• Resonant circuit design flow

Converter Specifications

\[ n = \frac{V_{in}}{2V_o} \]

Magnetizing Inductance

\[ M_{g_{min}} = \frac{n \times V_{o_{min}}}{V_{in_{max}} / 2} \]

\[ M_{g_{max}} = \frac{n \times V_{o_{max}}}{V_{in_{min}} / 2} \]

Choose \( L_n \) and \( Q_e \)

Resonant Inductor

\[ L_r = \frac{1}{(2f_{sw})^2 \times C_r} \]

Resonant Capacitor

\[ C_r = \frac{1}{2 \pi f_{sw} \times R_c \times Q_c} \]

Are Values Within Limits?

\( M_{g_{max}} \)
\( M_{g_{min}} \)
\( f_{n_{max}} \)
\( f_{n_{min}} \)

Calculate \( R_e \)

\[ R_e = \frac{8 \times n^2}{\pi^2} \times R_L = \frac{8 \times n^2}{\pi^2} \times \frac{V_o^2}{P_{out}} \]
Design Considerations

• Design example

  – Specifications

    • Rated output power: 300 W
    • Input voltage: 375 to 405 VDC
    • Output voltage: 12 VDC
    • Rated output current: 25 A
    • Efficiency ($V_{in} = 390$ VDC and $I_o = 25$ A): >90%
    • Switching frequency: 70 kHz to 150 kHz
    • Topology: LLC resonant half-bridge converter
Design Considerations

- Design example
  - Proposed converter circuit block diagram
Design Considerations

• Design example – UCC25600 Features
  
  – 8-pin SOIC package
  
  – Programmable:
    • dead time
    • \( f_{\text{min}} \) and \( f_{\text{max}} \)
    • soft start time
  
  – Protection
    • OCP: hiccup and latch-off
    • VDD UVLO and OVP
    • OTP
  
  – Burst operation
Design Considerations

- Resonant circuit design flow

Converter Specifications

\[
n = \frac{V_{in}}{2V_o}
\]

\[
M_{g_{\text{min}}} = \frac{n \times V_{O_{\text{min}}}}{V_{in_{\text{max}}}} / 2
\]

\[
M_{g_{\text{max}}} = \frac{n \times V_{O_{\text{max}}}}{V_{in_{\text{min}}}} / 2
\]

Choose \( L_n \) and \( Q_e \)

Check \( M_g \) and \( f_n \) Against Graph

Are Values Within Limits? \( M_{g_{\text{max}}} \)

Are Values Within Limits? \( M_{g_{\text{min}}} \)

\[
f_{n_{\text{max}}} = \frac{1}{\pi f_{sw}}
\]

\[
f_{n_{\text{min}}} = \frac{1}{\pi f_{sw}}
\]

\[box{\text{Calculate } R_e}
\]

\[
R_e = \frac{8 \times n^2}{\pi^2} \times R_L = \frac{8 \times n^2}{\pi^2} \times \frac{V_o^2}{P_{\text{out}}}
\]

Magnetizing Inductance

\[
L_{\text{in}} = L_n \times L_r
\]

Resonant Inductor

\[
L_r = \frac{1}{(2\pi f_{sw})^2 \times C_r}
\]

Resonant Capacitor

\[
C_r = \frac{1}{2\pi f_{sw} \times R_e \times Q_e}
\]

\[
L_m = 210 \mu H
\]

\[
L_r = 60 \mu H
\]

\[
C_r = 27.3 \text{ nF}
\]
Design Considerations

- Design check

![Diagram showing normalized frequency, gain, and various Q and M values.]

- $Q_e = 0$
- $Q_e = 0.47$
- $Q_e = 0.52$
- $M_{g_{\text{max}}} = 1.3$
- $M_{g_{\text{min}}} = 0.99$
- $f_{n_{\text{min}}} = 0.65$ (80.9 kHz)
- $f_{n_{\text{max}}} = 1.02$ (126.9 kHz)
- $f_{\text{min}} = 70$ kHz
- $f_{\text{max}} = 150$ kHz

- $L_n = 3.5$
Design Considerations

• Design check
  – Verification with computer-based circuit simulation
  – Design reiteration, if needed
  – Size/select components
  – Build the board
  – Verification with bench tests
  – Re-spin the board/design, if needed
Design Considerations

• Experiment results ($L_m = 280 \, \mu H$, $L_r = 60 \, \mu H$, $C_r = 24 \, nF$)
Test Result versus FHA from the Design

- In the vicinity of $f_0$, FHA-based result very accurate to the final test result ($L_r = 60 \, \mu\text{H}$ and $C_r = 24 \, \text{nF}$)

- Away from $f_0$, less accuracy from FHA-based result

- Equation (18)

$$M_g = \frac{V_{oc}}{V_{ge}} = \left| \frac{jX_{L_m} \parallel R_e}{(jX_{L_m} \parallel R_e + j(X_{L_r} - X_{C_r})} \right|$$

$$= \left| \frac{(j\omega L_m) \parallel R_e}{(j\omega L_m) \parallel R_e + j\omega L_r + \frac{1}{j\omega C_r}} \right|$$

Bench Test Measurements

Plot Based on Equation 18

Frequency, $f_{\text{sw}}$ (kHz)

Gain, $M_g$

$\text{f}_0 = 135 \, \text{kHz}$
Conclusions

• FHA-based method approximately, while effectively, converted complicated LLC resonant-converter circuit to standard AC circuit – greatly simplified its analysis and design

• Method results effective for LLC converter design, especially for initial parameters determination

• Design example with comprehensive design considerations in procedural design steps demonstrating method effectiveness

• Possibility of FHA-based approach for other resonant converters
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